

# DLPC3432 ディスプレイ・コントローラ

## 1 特長

- **DLP230GP (0.23 qHD) DMD 向けディスプレイ・コントローラ**
  - qHD までの入力解像度に対応
  - インターフェイス・トレーニング付きの低消費電力 DMD インターフェイス
- 最高 **240Hz** の入力フレーム・レート
- ピクセル・データ処理:
  - 画像処理アルゴリズムの IntelliBright™ スイート
    - コンテンツ適応型の照明制御 (CAIC)
    - 局所的輝度ブースト (LABB)
  - 画像のサイズ変更 (スケーリング)
  - 1D 台形補正
  - 色座標調整
  - アクティブ電力管理処理
  - 逆ガンマ補正をプログラム可能
  - 色空間の変換
  - 4:2:2 から 4:4:4 への色差補間
- 24 ビットの入力ピクセル・インターフェイスに対応:
  - パラレルまたは **BT656** インターフェイス・プロトコル
  - 最高 **155MHz** のピクセル・クロック
  - 複数の入力ピクセル・データ・フォーマットに対応
- **MIPI® DSI** (ディスプレイ・シリアル・インターフェイス) タイプ 3:
  - 1~4 レーン、最高 **470Mbps** のレーン速度
- 外付けフラッシュ対応
- 電源オフ時の自動 DMD パーキング
- 組み込みフレーム・メモリ (eDRAM)
- システム機能:
  - I<sup>2</sup>C デバイス制御
  - スプラッシュ・スクリーンをプログラム可能
  - LED 電流制御をプログラム可能
  - 表示画像の回転
- LED ドライバ内蔵 PMIC (電力管理 IC) **DLPA2000**、**DLPA2005**、または **DLPA3000** と組み合わせ

## 2 アプリケーション

- モバイル・プロジェクト
- スマート・ディスプレイ
- スマートフォン
- 拡張現実 (AR) メガネ
- スマート・ホーム・ディスプレイ
- Pico プロジェクト

## 3 概要

**DLPC3432** デジタル・コントローラは **DLP230GP (0.23 qHD)** チップセットの一部で、**DLP230GP** デジタル・マイクロミラー・デバイス (DMD) の動作を可能にします。**DLPC3432** コントローラは、ユーザー用電子機器と DMD との間を接続する便利な多機能インターフェイスとして機能し、小型で低消費電力のディスプレイ・アプリケーションを実現します。

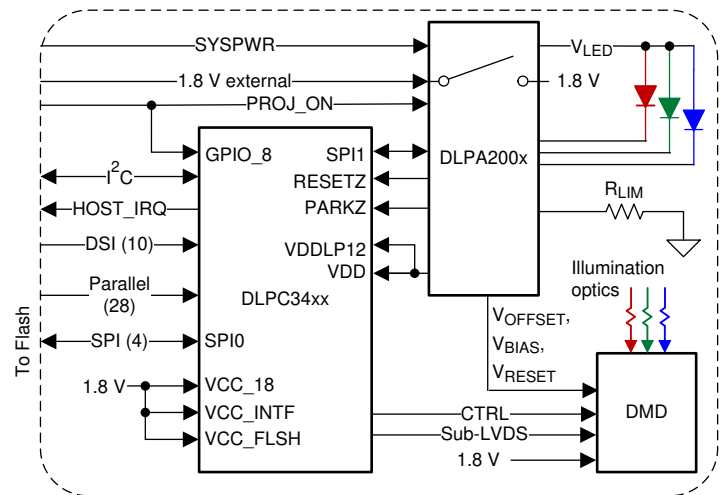
設計を始める方法については、「**TI DLP®Pico™ ディスプレイ・テクノロジーを使用した設計の開始**」ページを参照し、「**Programmer's Guide**」(英語)をご覧ください。

このチップセットには、設計期間の短縮に役立つ定評あるリソースが用意されており、これには **すぐに量産可能な光モジュール**、**光モジュール・メーカー**、**デザインハウス**などが含まれます。

### 製品情報 (1)

| 部品番号     | パッケージ       | 本体サイズ (公称)      |
|----------|-------------|-----------------|
| DLPC3432 | NFBGA (176) | 7.00mm × 7.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



標準的なシステムの概略図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (June 2019) to Revision D (October 2020)   | Page |
|--|------|
| • 文書全体にわたって表、図、相互参照の採番方法を更新.....   | 1    |
| • 一般的なデータシートフォーマットと注文情報を更新.....  | 1    |
| • 「特長」セクションを更新し、最大 qHD までのサポートされる入力解像度を追加.....   | 1    |
| • Changed JTAG pin names from Reserved to proper names .....   | 6    |
| • Deleted support for adjustable DATAEN_CMD polarity .....   | 7    |
| • Deleted mention of a specific 3D command .....   | 7    |
| • Deleted support for adjusting PCLK capture edge in software .....  | 7    |
| • Changed the description of how to use the CMP_OUT pin and corrected how the comparator must use GPIO_10 (RC_CHARGE) instead of CMP_PWM ..... | 10   |
| • Deleted support for CMP_PWM.....   | 10   |
| • Added note about VCC_INTF power up recommendations if secondary devices are on the I <sup>2</sup> C bus .....                                | 10   |
| • Deleted mention of unsupported keypad inputs .....   | 11   |
| • Corrected optional MTR_SENSE support to GPIO_18 instead of GPIO_19 .....   | 11   |
| • Deleted mention of unsupported light sensor on GPIO_13 and GPIO_12 .....   | 11   |

|  |    |
|--|----|
| • Deleted reference of the RC_CHARGE circuit being used for the light sensor and added reference of it being used for the thermistor .....                                   | 11 |
| • Deleted reference of the LS_PWR circuit being used for the light sensor.....   | 11 |
| • Deleted mention of the unsupported LABB output sample and hold sensor control signal.....  | 11 |
| • Clarified GPIO_03 - GPIO_01 pins are required to be used as a SPI1 port.....   | 11 |
| • Deleted misleading note about GPIO pins defaulting to inputs .....   | 11 |
| • Added missing I/O definition 10 .....  | 13 |
| • Deleted unneeded VCC_INTF and VCC_FLSH absolute maximum values .....   | 15 |
| • Added high voltage tolerant note to Absolute Maximum Ratings table .....   | 15 |
| • Changed incorrect pin tolerance .....  | 16 |
| • Changed Power Electrical Characteristics table to reflect updated power measurement values and techniques .....  | 17 |
| • Deleted reference to IDLE mode .....   | 17 |
| • Added note that the power numbers vary depending on the utilized software.....   | 17 |
| • Changed and fixed incorrect test conditions for current drive strengths.....   | 18 |
| • Deleted redundant  V <sub>OD</sub>   specification which is referenced in later sections.....  | 18 |
| • Added minimum and maximum values for V <sub>OH</sub> for I/O type 4.....   | 18 |
| • Added minimum and maximum values for V <sub>OL</sub> for I/O type 4.....   | 18 |
| • Deleted incorrect reference to 2.5-V, 24-mA drive .....  | 18 |
| • Corrected I <sup>2</sup> C buffer test conditions.....   | 18 |
| • Deleted incorrect steady-state common mode voltage reference .....   | 18 |
| • Changed high voltage tolerant I/O note to only refer to the I <sup>2</sup> C buffer and changed VCC to VCC_INTF.....   | 18 |
| • Added  V <sub>OD</sub>   minimum and maximum values, and changed the typical value.....  | 21 |
| • Added high-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value ..... | 21 |
| • Added low-level output voltage minimum and maximum values for the sub-LVDS DMD interface, deleted redundant mention of specification, and changed the typical value. ....  | 21 |
| • Corrected the name of the DMD Low-Speed signals from inputs to outputs. ....   | 22 |
| • Deleted V <sub>OH(DC)</sub> maximum and V <sub>OL(DC)</sub> minimum values. ....   | 22 |
| • Added note about DMD input specs being met if a proper series termination resistor is used .....   | 22 |
| • Deleted reference of selecting unsupported oscillator frequency .....  | 23 |
| • Corrected system oscillator clock period to match clock frequency .....  | 23 |
| • Changed pulse duration percent spec from a maximum to a minimum .....  | 23 |
| • Added condition for VDD rise time .....  | 23 |
| • Deleted the incorrect part of the t <sub>p_tvb</sub> definition.....   | 24 |
| • Deleted unneeded total horizontal blanking equation .....  | 24 |
| • Changed minimum total vertical blanking equation .....   | 24 |
| • Increased maximum PCLK from 150 MHz to 155 MHz .....   | 25 |
| • Deleted reference to various signal's active edges being configurable .....  | 25 |
| • Changed the minimum flash SPI_CLK frequency.....   | 27 |
| • Corrected flash interface clock period to match clock frequency .....  | 27 |
| • Added セクション 6.17 section to more clearly list signal transition time requirements.....   | 28 |
| • Changed GPIO_08 (HOST_IRQ) pulse width requirement and added a requirement to keep GPIO_08 high until HOST_IRQ goes low.....   | 28 |
| • Changed DMD HS clock switching rate from maximum to nominal and added accompanying clock specification .....   | 28 |
| • Added セクション 6.19 section.....  | 28 |
| • Added the セクション 6.20 section to clarify chipset support requirements.....  | 28 |
| • Changed how chipset support is mentioned in the Detailed Description section .....   | 29 |
| • Deleted support for 3D video over DSI .....  | 30 |
| • Deleted reference to internal software tools and clarified how firmware affects the supported resolution and frame rates .....   | 30 |
| • Added note that up to four DSI lanes may be required to fully utilize the bandwidth .....  | 30 |
| • Deleted mention of sequencer sync mode as its generally assumed to be auto.....  | 30 |
| • Clarified note about VSYNC_WE needing to remain active .....   | 32 |

- Deleted support for changing the clock active edge and clarified support of changing the sync active edge.. 32
- Changed the DATAEN\_CMD signal to not be optional ..... 32
- Added note that LP mode is required during vertical time for DSI ..... 33
- Changed requirement related to DSI initialization ..... 33
- Deleted incorrect DSI data type; see software programmers guide instead..... 35
- Added information that the parallel interface isn't ready to accept data until the auto-initialization process is completed..... 37
- Changed how the 500-ms startup time is described ..... 37
- Changed SPI flash key timing parameter access frequency minimum and maximum values..... 37
- Changed maximum flash size supported from 16 Mb to 128 Mb ..... 37
- Deleted SPI signal routing section ..... 40
- Deleted support for a light sensor integrated with the DLPC34xx controller ..... 42
- Added missing timing definitions ..... 42
- Clarified that the mentioned SDR clock speed is the typical value..... 46
- Changed the description of how PROJ\_ON affects the power supplies ..... 51
- Changed which signals are listed as tri-stated at power up and which signals are pulled low ..... 56
- Changed 1-oz copper plane recommendation ..... 58
- Deleted reference to unsupported option of variable frequency reference clock..... 60
- Added additional DMD data and DMD clock signal matching requirements ..... 63
- Changed maximum mismatch from  $\pm 0.1''$  to  $\pm 1.0''$  ..... 63
- Changed incorrect signal matching requirement table note..... 63
- Changed differential signal layer change to a recommendation..... 65
- Changed wording requiring no more than two vias on certain DMD signals ..... 66
- Updated the description of the device marking to correspond to the actual device package designator..... 68

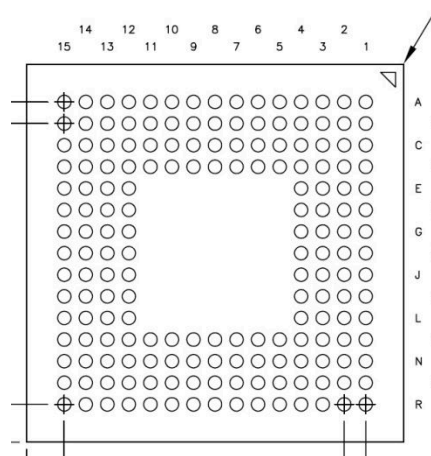
**Changes from Revision B (April 2018) to Revision C (June 2019) Page**

- Changed mirror parking time from "500  $\mu$ s" to "20 ms" for PARKZ description in *Pin Functions* table.....6
- Updated mirror parking time from "500  $\mu$ s" to "20 ms" in *Figure 27. DLPC343x Power-Up / PARKZ = 0 Initiated Fast PARK and Power-Down* ..... 52

**Changes from Revision \* (February 2018) to Revision A (March 2018) Page**

- In *セクション 11.1.2.1*, definition of 'x' in 'DLPC343x' is redefined as 2 instead of 0 or 5..... 68

**5 Pin Configuration and Functions**



**5-1. ZVB Package 176-Pin NFBGA Bottom View**

|          | 1             | 2            | 3               | 4               | 5               | 6               | 7            | 8               | 9               | 10              | 11              | 12        | 13        | 14        | 15        |
|----------|---------------|--------------|-----------------|-----------------|-----------------|-----------------|--------------|-----------------|-----------------|-----------------|-----------------|-----------|-----------|-----------|-----------|
| <b>A</b> | DMD_LS_CLK    | DMD_LS_WDATA | DMD_HS_WDATAH_P | DMD_HS_WDATAG_P | DMD_HS_WDATAF_P | DMD_HS_WDATAE_P | DMD_HS_CLK_P | DMD_HS_WDATAD_P | DMD_HS_WDATAC_P | DMD_HS_WDATAB_P | DMD_HS_WDATAA_P | CMP_OUT   | SPI0_CLK  | SPI0_CS20 | CMP_PWM   |
| <b>B</b> | DMD_DEN_ARSTZ | DMD_LS_RDATA | DMD_HS_WDATAH_N | DMD_HS_WDATAG_N | DMD_HS_WDATAF_N | DMD_HS_WDATAE_N | DMD_HS_CLK_N | DMD_HS_WDATAD_N | DMD_HS_WDATAC_N | DMD_HS_WDATAB_N | DMD_HS_WDATAA_N | SPI0_DIN  | SPI0_DOUT | LED_SEL_1 | LED_SEL_0 |
| <b>C</b> | DD3P          | DD3N         | VDD             | VSS             | VDD             | VSS             | VCC          | VSS             | VCC             | HWTEST_EN       | RESETZ          | SPI0_CS21 | PARKZ     | GPIO_00   | GPIO_01   |
| <b>D</b> | DD2P          | DD2N         | VDD             | VCC             | VDD             | VSS             | VDD          | VSS             | VDD             | VSS             | VCC_FLSH        | VDD       | VDD       | GPIO_02   | GPIO_03   |
| <b>E</b> | DCLKP         | DCLKN        | VDD             | VSS             |                 |                 |              |                 |                 |                 |                 | VCC       | VSS       | GPIO_04   | GPIO_05   |
| <b>F</b> | DD1P          | DD1N         | RREF            | VSS             |                 |                 |              |                 |                 |                 |                 | VCC       | VDD       | GPIO_06   | GPIO_07   |
| <b>G</b> | DD0P          | DD0N         | VSS_PLLM        | VSS             |                 |                 |              |                 |                 |                 |                 | VSS       | VSS       | GPIO_08   | GPIO_09   |
| <b>H</b> | PLL_REFCLK_J  | VDD_PLLM     | VSS_PLLD        | VSS             |                 |                 |              |                 |                 |                 |                 | VSS       | VDD       | GPIO_10   | GPIO_11   |
| <b>J</b> | PLL_REFCLK_O  | VDD_PLLD     | VSS             | VDD             |                 |                 |              |                 |                 |                 |                 | VDD       | VSS       | GPIO_12   | GPIO_13   |
| <b>K</b> | PDATA_1       | PDATA_0      | VDD             | VSS             |                 |                 |              |                 |                 |                 |                 | VSS       | VCC       | GPIO_14   | GPIO_15   |
| <b>L</b> | PDATA_3       | PDATA_2      | VSS             | VDD             |                 |                 |              |                 |                 |                 |                 | VDD       | VDD       | GPIO_16   | GPIO_17   |
| <b>M</b> | PDATA_5       | PDATA_4      | VCC_INTF        | VSS             | VSS             | VDD             | VCC_INTF     | VSS             | VDD             | VDD             | VCC             | VSS       | JTAGTMS1  | GPIO_18   | GPIO_19   |
| <b>N</b> | PDATA_7       | PDATA_6      | VCC_INTF        | PDM_CVSTE       | HSYNC_CS        | 3DR             | VCC_INTF     | HOST_IRQ        | IIC0_SDA        | IIC0_SCL        | JTAGTMS2        | JTAGTDO2  | JTAGTDO1  | TSTPT_6   | TSTPT_7   |
| <b>P</b> | VSYNC_WE      | DATEN_CMD    | PCLK            | PDATA_11        | PDATA_13        | PDATA_15        | PDATA_17     | PDATA_19        | PDATA_21        | PDATA_23        | JTAGTRSTZ       | JTAGTCK   | JTAGTDI   | TSTPT_4   | TSTPT_5   |
| <b>R</b> | PDATA_8       | PDATA_9      | PDATA_10        | PDATA_12        | PDATA_14        | PDATA_16        | PDATA_18     | PDATA_20        | PDATA_22        | IIC1_SDA        | IIC1_SCL        | TSTPT_0   | TSTPT_1   | TSTPT_2   | TSTPT_3   |

Note: The lower image view is from the top.

## 5.1 Test Pins and General Control

| PIN       |                    | I/O | TYPE <sup>(4)</sup> | DESCRIPTION  |
|-----------|--------------------|-----|---------------------|--|
| NAME      | NO.                |     |                     |  |
| HWTEST_EN | C10                | I   | 6                   | Manufacturing test enable signal. Connect this signal directly to ground on the PCB for normal operation.  |
| PARKZ     | C13                | I   | 6                   | DMD fast park control (active low Input with a hysteresis buffer). This signal is used to quickly park the DMD when loss of power is imminent. The longest lifetime of the DMD may not be achieved with the fast park operation; therefore, this signal is intended to only be asserted when a normal park operation is unable to be completed. The PARKZ signal is typically provided from the DLPxxxx interrupt output signal.                 |
| JTAGTCK   | P12                | I   | 6                   | TI internal use. Leave this pin unconnected.   |
| JTAGTDI   | P13                | I   | 6                   | TI internal use. Leave this pin unconnected.   |
| JTAGTDO1  | N13 <sup>(1)</sup> | O   | 1                   | TI internal use. Leave this pin unconnected.   |
| JTAGTDO2  | N12 <sup>(1)</sup> | O   | 1                   | TI internal use. Leave this pin unconnected.   |
| JTAGTMS1  | M13                | I   | 6                   | TI internal use. Leave this pin unconnected.   |
| JTAGTMS2  | N11                | I   | 6                   | TI internal use. Leave this pin unconnected.   |
| JTAGTRSTZ | P11                | I   | 6                   | TI internal use.<br>This pin must be tied to ground, through an external resistor for normal operation. Failure to tie this pin low during normal operation can cause start up and initialization problems. <sup>(2)</sup>   |
| RESETZ    | C11                | I   | 6                   | Power-on reset (active low input with a hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All controller power and clocks must be stable before this reset is de-asserted. No signals are in their active state while RESETZ is asserted. This pin is typically connected to the RESETZ pin of the DLPA200x or RESET_Z of the DLPA3000.   |
| TSTPT_0   | R12                | I/O | 1                   | Test pins (includes weak internal pulldown). Pins are tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 $\mu$ s after de-assertion of RESETZ, and then driven as outputs. <sup>(2) (3)</sup><br>Normal use: reserved for test output. Leave open for normal use.<br>Note: An external pullup may put the DLPC34xx in a test mode. See <a href="#">セクション 7.3.8</a> for more information. |
| TSTPT_1   | R13                | I/O | 1                   |  |
| TSTPT_2   | R14                | I/O | 1                   |  |
| TSTPT_3   | R15                | I/O | 1                   |  |
| TSTPT_4   | P14                | I/O | 1                   |  |
| TSTPT_5   | P15                | I/O | 1                   |  |
| TSTPT_6   | N14                | I/O | 1                   |  |
| TSTPT_7   | N15                | I/O | 1                   |  |

- (1) If the application design does not require an external pullup, and there is no external logic that can overcome the weak internal pulldown resistor, then this I/O pin can be left open or unconnected for normal operation. If the application design does not require an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown is recommended to ensure a logic low.
- (2) External resistor must have a value of 8 k $\Omega$  or less to compensate for pins that provide internal pullup or pulldown resistors.
- (3) If the application design does not require an external pullup and there is no external logic that can overcome the weak internal pulldown, then the TSTPT I/O can be left open (unconnected) for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.
- (4) See [表 5-2](#) for type definitions.

## 5.2 Parallel Port Input

| PIN <sup>(1) (2)</sup>   |   | I/O | TYPE <sup>(4)</sup> | DESCRIPTION   |  |
|--|---|-----|---------------------|---|--|
| NAME   | NO.   |     |                     | PARALLEL RGB MODE   | BT656 INTERFACE MODE   |
| PCLK   | P3  | I   | 11                  | Pixel clock   | Pixel clock  |
| PDM_CVS_TE   | N4  | I/O | 5                   | Parallel data mask. Programmable polarity with default of active high. Optional signal.   | Unused   |
| VSYNC_WE   | P1  | I   | 11                  | Vsync <sup>(3)</sup>  | Unused   |
| HSYNC_CS   | N5  | I   | 11                  | Hsync <sup>(3)</sup>  | Unused   |
| DATAEN_CMD   | P2  | I   | 11                  | Data valid  | Unused   |
| PDATA_0<br>PDATA_1<br>PDATA_2<br>PDATA_3<br>PDATA_4<br>PDATA_5<br>PDATA_6<br>PDATA_7         | K2<br>K1<br>L2<br>L1<br>M2<br>M1<br>N2<br>N1  | I   | 11                  | <b>(TYPICAL RGB 888)</b><br>Blue (bit weight 1)<br>Blue (bit weight 2)<br>Blue (bit weight 4)<br>Blue (bit weight 8)<br>Blue (bit weight 16)<br>Blue (bit weight 32)<br>Blue (bit weight 64)<br>Blue (bit weight 128)   | BT656_Data (0)<br>BT656_Data (1)<br>BT656_Data (2)<br>BT656_Data (3)<br>BT656_Data (4)<br>BT656_Data (5)<br>BT656_Data (6)<br>BT656_Data (7) |
| PDATA_8<br>PDATA_9<br>PDATA_10<br>PDATA_11<br>PDATA_12<br>PDATA_13<br>PDATA_14<br>PDATA_15   | R1<br>R2<br>R3<br>P4<br>R4<br>P5<br>R5<br>P6  | I   | 11                  | <b>(TYPICAL RGB 888)</b><br>Green (bit weight 1)<br>Green (bit weight 2)<br>Green (bit weight 4)<br>Green (bit weight 8)<br>Green (bit weight 16)<br>Green (bit weight 32)<br>Green (bit weight 64)<br>Green (bit weight 128)   | Unused   |
| PDATA_16<br>PDATA_17<br>PDATA_18<br>PDATA_19<br>PDATA_20<br>PDATA_21<br>PDATA_22<br>PDATA_23 | R6<br>P7<br>R7<br>P8<br>R8<br>P9<br>R9<br>P10 | I   | 11                  | <b>(TYPICAL RGB 888)</b><br>Red (bit weight 1)<br>Red (bit weight 2)<br>Red (bit weight 4)<br>Red (bit weight 8)<br>Red (bit weight 16)<br>Red (bit weight 32)<br>Red (bit weight 64)<br>Red (bit weight 128)   | Unused   |
| 3DR  | N6  | I   | 11                  | 3D reference<br><ul style="list-style-type: none"> <li>For 3D applications: left or right 3D reference (left = 1, right = 0). To be provided by the host. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC).</li> <li>If a 3D application is not used, pull this input low through an external resistor.</li> </ul> |  |

- (1) PDATA(23:0) bus mapping depends on pixel format and source mode. See later sections for details.  
(2) Connect unused inputs to ground or pulldown to ground through an external resistor (8 kΩ or less).  
(3) VSYNC and HSYNC polarity can be adjusted by software.  
(4) See 表 5-2 for type definitions.

### 5.3 DSI Input Data and Clock

| PIN  |  | I/O | TYPE <sup>(2)</sup> | DESCRIPTION   |
|--|--|-----|---------------------|---|
| NAME   | NO.  |     |                     |   |
| DCLKN<br>DCLKP   | E2<br>E1                                     | I/O | 10                  | DSI LVDS differential clock for DSI interface.  |
| DD0N<br>DD0P<br>DD1N<br>DD1P<br>DD2N<br>DD2P<br>DD3N<br>DD3P | G2<br>G1<br>F2<br>F1<br>D2<br>D1<br>C2<br>C1 | I/O | 10                  | Differential data bus for DSI data lane LVDS differential pair inputs 0 through 3.<br>(support a maximum of 4 input DSI lanes) <sup>(1)</sup>   |
| RREF   | F3   | —   |                     | DSI reference resistor. RREF is an analog signal that requires a fixed precision 30-k $\Omega$ $\pm$ 1% resistor connected from this pin to ground when DSI is used. If DSI is NOT used, leave this pin unconnected and floating. |

- (1) Differential data bus 0 (DD0x) is required for DSI operation. The remaining three data lanes are optional and only needed depending on the implementation and required video bandwidth. Leave any unused DSI LVDS pairs unconnected and floating.
- (2) See [表 5-2](#) for type definitions.

### 5.4 DMD Reset and Bias Control

| PIN           |     | I/O | TYPE <sup>(1)</sup> | DESCRIPTION   |
|---------------|-----|-----|---------------------|---|
| NAME          | NO. |     |                     |   |
| DMD_DEN_ARSTZ | B1  | O   | 2                   | DMD driver enable (active high). DMD reset (active low). When corresponding I/O power is supplied, the controller drives this signal low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC34xx is independent of the 1.8-V power to the DMD, then TI recommends including a weak, external pulldown resistor to hold the signal low in case DLPC34xx power is inactive while DMD power is applied. |
| DMD_LS_CLK    | A1  | O   | 3                   | DMD low speed (LS) interface clock  |
| DMD_LS_WDATA  | A2  | O   | 3                   | DMD low speed (LS) serial write data  |
| DMD_LS_RDATA  | B2  | I   | 6                   | DMD low speed (LS) serial read data   |

- (1) See [表 5-2](#) for type definitions.

### 5.5 DMD Sub-LVDS Interface

| PIN                          |          | I/O | TYPE <sup>(1)</sup> | DESCRIPTION                         |
|------------------------------|----------|-----|---------------------|-------------------------------------|
| NAME                         | NO.      |     |                     |                                     |
| DMD_HS_CLK_P<br>DMD_HS_CLK_N | A7<br>B7 | O   | 4                   | DMD high speed (HS) interface clock |



| PIN              |     | I/O | TYPE <sup>(1)</sup> | DESCRIPTION  |
|------------------|-----|-----|---------------------|--|
| NAME             | NO. |     |                     |  |
| DMD_HS_WDATA_H_P | A3  | O   | 4                   | DMD sub-LVDS high speed (HS) interface write data lanes. The true numbering and application of the DMD_HS_WDATA pins depend on the software configuration. See <a href="#">表 7-9</a> . |
| DMD_HS_WDATA_H_N | B3  |     |                     |  |
| DMD_HS_WDATA_G_P | A4  |     |                     |  |
| DMD_HS_WDATA_G_N | B4  |     |                     |  |
| DMD_HS_WDATA_F_P | A5  |     |                     |  |
| DMD_HS_WDATA_F_N | B5  |     |                     |  |
| DMD_HS_WDATA_E_P | A6  |     |                     |  |
| DMD_HS_WDATA_E_N | B6  |     |                     |  |
| DMD_HS_WDATA_D_P | A8  |     |                     |  |
| DMD_HS_WDATA_D_N | B8  |     |                     |  |
| DMD_HS_WDATA_C_P | A9  |     |                     |  |
| DMD_HS_WDATA_C_N | B9  |     |                     |  |
| DMD_HS_WDATA_B_P | A10 |     |                     |  |
| DMD_HS_WDATA_B_N | B10 |     |                     |  |
| DMD_HS_WDATA_A_P | A11 |     |                     |  |
| DMD_HS_WDATA_A_N | B11 |     |                     |  |

(1) See [表 5-2](#) for type definitions.

## 5.6 Peripheral Interface

| PIN <sup>(1)</sup>      |     | I/O | TYPE <sup>(2)</sup> | DESCRIPTION   |
|-------------------------|-----|-----|---------------------|---|
| NAME                    | NO. |     |                     |   |
| CMP_OUT                 | A12 | I   | 6                   | Successive approximation ADC (analog-to-digital converter) comparator output (DLPC34xx Input). To implement, use a successive approximation ADC with a thermistor feeding one input of the external comparator and the DLPC34xx controller GPIO_10 (RC_CHARGE) pin driving the other side of the comparator. It is recommended to use the DLPAXxx to achieve this function. CMP_OUT must be pulled-down to ground if this function is not used. (hysteresis buffer)   |
| CMP_PWM                 | A15 | O   | 1                   | TI internal use. Leave this pin unconnected.  |
| HOST_IRQ <sup>(3)</sup> | N8  | O   | 9                   | Host interrupt (output)<br>HOST_IRQ indicates when the DLPC34xx auto-initialization is in progress and most importantly when it completes. This pin is tri-stated during reset. An external pullup must be included on this signal.   |
| IIC0_SCL <sup>(4)</sup> | N10 | I/O | 7                   | I <sup>2</sup> C secondary (port 0) SCL (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The secondary I <sup>2</sup> C I/Os are 3.6-V tolerant (high-voltage-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I <sup>2</sup> C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V <sub>IH</sub> specification of the secondary I <sup>2</sup> C input buffers).  |
| IIC1_SCL                | R11 | I/O | 8                   | TI internal use. TI recommends an external pullup resistor.   |
| IIC0_SDA <sup>(4)</sup> | N9  | I/O | 7                   | I <sup>2</sup> C secondary (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): This pin requires an external pullup resistor. The secondary I <sup>2</sup> C port is the control port of controller. The secondary I <sup>2</sup> C I/O pins are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I <sup>2</sup> C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage does not typically satisfy the V <sub>IH</sub> specification of the secondary I <sup>2</sup> C input buffers). |
| IIC1_SDA                | R10 | I/O | 8                   | TI internal use. TI recommends an external pullup resistor.   |
| LED_SEL_0               | B15 | O   | 1                   | LED enable select. Automatically controlled by the DLPC34xx programmable DMD sequence.<br><br>LED_SEL(1:0)<br>00                    Enabled LED<br>01                    None<br>10                    Red<br>11                    Green<br>Blue   |
| LED_SEL_1               | B14 | O   | 1                   | The controller drives these signals low when RESETZ is asserted and the corresponding I/O power is supplied. The controller continues to drive these signals low throughout the auto-initialization process. A weak, external pulldown resistor is recommended to ensure that the LEDs are disabled when I/O power is not applied.  |
| SPI0_CLK                | A13 | O   | 13                  | SPI (Serial Peripheral Interface) port 0, clock. This pin is typically connected to the flash memory clock.   |
| SPI0_CSZ0               | A14 | O   | 13                  | SPI port 0, chip select 0 (active low output). This pin is typically connected to the flash memory chip select. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.  |
| SPI0_CSZ1               | C12 | O   | 13                  | SPI port 0, chip select 1 (active low output). This pin typically remains unused. TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during controller reset assertion.  |
| SPI0_DIN                | B12 | I   | 12                  | Synchronous serial port 0, receive data in. This pin is typically connected to the flash memory data out.   |
| SPI0_DOUT               | B13 | O   | 13                  | Synchronous serial port 0, transmit data out. This pin is typically connected to the flash memory data in.  |

- (1) External pullup resistor must be 8 kΩ or less.
- (2) See [表 5-2](#) for type definitions.
- (3) For more information about usage, see [セクション 7.3.2](#).
- (4) When VCC\_INTF is powered and VDD is not powered, the controller may drive the IIC0\_xxx pins low which prevents communication on this I<sup>2</sup>C bus. Do not power up the VCC\_INTF pin before powering up the VDD pin for any system that has additional secondary devices on this bus.

## 5.7 GPIO Peripheral Interface

| PIN <sup>(1)</sup> |     | I/O | TYPE <sup>(3)</sup> | DESCRIPTION <sup>(2)</sup>  |
|--------------------|-----|-----|---------------------|---|
| NAME               | NO. |     |                     |   |
| GPIO_19            | M15 | I/O | 1                   | General purpose I/O 19 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_18            | M14 | I/O | 1                   | General purpose I/O 18 (hysteresis buffer). Options:<br><ol style="list-style-type: none"> <li>Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.</li> <li>MTR_SENSE, Motor Sense (Input): For focus motor control applications, this GPIO must be configured as an input to the DLPC34xx and supplied from the focus motor position sensor.</li> </ol> |
| GPIO_17            | L15 | I/O | 1                   | General purpose I/O 17 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_16            | L14 | I/O | 1                   | General purpose I/O 16 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_15            | K15 | I/O | 1                   | General purpose I/O 15 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_14            | K14 | I/O | 1                   | General purpose I/O 14 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_13            | J15 | I/O | 1                   | General purpose I/O 13 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_12            | J14 | I/O | 1                   | General purpose I/O 12 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_11            | H15 | I/O | 1                   | General purpose I/O 11 (hysteresis buffer). Options:<br><ol style="list-style-type: none"> <li>Thermistor power enable (output). Turns on the power to the thermistor when it is used and enabled.</li> <li>Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.</li> </ol>   |
| GPIO_10            | H14 | I/O | 1                   | General purpose I/O 10 (hysteresis buffer). Options:<br><ol style="list-style-type: none"> <li>RC_CHARGE (output): Intended to feed the RC charge circuit of the thermistor interface.</li> <li>Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.</li> </ol>   |
| GPIO_09            | G15 | I/O | 1                   | General purpose I/O 09 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_08            | G14 | I/O | 1                   | General purpose I/O 08 (hysteresis buffer). Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the DLPC34xx to PARK the DMD, but it does not power down the DMD (the DLPAXxxx does that instead). At power-up, GPIO_08 must remain high until HOST_IRQ goes low (see <a href="#">セクション 9.3</a> ).  |
| GPIO_07            | F15 | I/O | 1                   | General purpose I/O 07 (hysteresis buffer). If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.   |
| GPIO_06            | F14 | I/O | 1                   | General purpose I/O 06 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |

| PIN <sup>(1)</sup> |     | I/O | TYPE <sup>(3)</sup> | DESCRIPTION <sup>(2)</sup>  |
|--------------------|-----|-----|---------------------|---|
| NAME               | NO. |     |                     |   |
| GPIO_05            | E15 | I/O | 1                   | General purpose I/O 05 (hysteresis buffer). Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input.  |
| GPIO_04            | E14 | I/O | 1                   | General purpose I/O 04 (hysteresis buffer). Options:<br>1. 3D glasses control (output): Controls the shutters on 3D glasses (Left = 1, Right = 0).<br>2. SPI1_CSZ1 (active-low output): Optional SPI1 chip select 1 signal. Requires an external pullup resistor to deactivate this signal during reset and auto-initialization processes.<br>3. Optional GPIO. If unused TI recommends this pin be configured as a logic zero GPIO output and left unconnected. Otherwise this pin requires an external pullup or pulldown to avoid a floating GPIO input. |
| GPIO_03            | D15 | I/O | 1                   | General purpose I/O 03 (hysteresis buffer). SPI1_CSZ0 (active low output): SPI1 chip select 0 signal. This pin is typically connected to the DLPAXxxx SPI_CSZ pin. Requires an external pullup resistor to deactivate this signal during reset and auto-initialization processes.   |
| GPIO_02            | D14 | I/O | 1                   | General purpose I/O 02 (hysteresis buffer). Options:<br>1. SPI1_DOUT (output): SPI1 data output signal. This pin is typically connected to the DLPAXxxx SPI_DIN pin.<br>2. Optional DSI Bus Width Config 1 (input): The controller samples this pin during boot and is used to define the number of lanes used for DSI operation. Requires an external pullup or pulldown resistor to configure as defined in 表 5-1. After boot, this GPIO pin will continue to be used as SPI1_DOUT. Select the external pullup or pulldown resistor to not interfere.     |
| GPIO_01            | C15 | I/O | 1                   | General purpose I/O 01 (hysteresis buffer). Options:<br>1. SPI1_CLK (output): SPI1 clock signal. This pin is typically connected to the DLPAXxxx SPI_CLK pin.<br>2. Optional DSI Bus Width Config 0 (input): The controller samples this pin during boot and is used to define the number of lanes used for DSI operation. Requires an external pullup or pulldown resistor to configure as defined in 表 5-1. After boot, this GPIO pin will continue to be used as SPI1_CLK. Select the external pullup or pulldown resistor to not interfere.             |
| GPIO_00            | C14 | I/O | 1                   | General purpose I/O 00 (hysteresis buffer). SPI1_DIN (input): SPI1 data input signal. This pin is typically connected to the DLPAXxxx SPI_DOUT pin.   |

- (1) GPIO pins must be configured through software for input, output, bidirectional, or open-drain operation. Some GPIO pins have one or more alternative use modes, which are also software configurable. An external pullup resistor is required for each signal configured as open-drain.
- (2) General purpose I/O for the DLPC3432 controllers. These GPIO pins are software configurable.
- (3) See 表 5-2 for type definitions.

**表 5-1. GPIO\_01 and GPIO\_02**

| GPIO_02           | GPIO_01           | Number of DSI Data Lanes |
|-------------------|-------------------|--------------------------|
| DSI Lane Config 1 | DSI Lane Config 0 |                          |
| 0                 | 0                 | 1                        |
| 0                 | 1                 | 2                        |
| 1                 | 0                 | 3                        |
| 1                 | 1                 | 4                        |

## 5.8 Clock and PLL Support

| PIN          |     | I/O | TYPE <sup>(1)</sup> | DESCRIPTION  |
|--------------|-----|-----|---------------------|--|
| NAME         | NO. |     |                     |  |
| PLL_REFCLK_I | H1  | I   | 11                  | Reference clock crystal input. If an external oscillator is used instead of a crystal, use this pin as the oscillator input.                                 |
| PLL_REFCLK_O | J1  | O   | 5                   | Reference clock crystal return. If an external oscillator is used instead of a crystal, leave this pin unconnected (floating with no added capacitive load). |

(1) See 表 5-2 for type definitions.

## 5.9 Power and Ground

| PIN      |  | I/O | TYPE | DESCRIPTION   |
|----------|--|-----|------|---|
| NAME     | NO.  |     |      |   |
| VDD      | C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3                 | —   | PWR  | Core 1.1-V power (main 1.1 V)   |
| VDDL12   | C3   | —   | PWR  | DSI PHY Low Power mode driver supply. It is recommended to externally tie this pin to VDD.  |
| VSS      | C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 | —   | GND  | Core ground (eDRAM, DSI, I/O ground, thermal ground)  |
| VCC18    | C7, C9, D4, E12, F12, K13, M11   | —   | PWR  | All 1.8-V I/O power: (1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ, LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins) |
| VCC_INTF | M3, M7, N3, N7   | —   | PWR  | Host or parallel interface I/O power: 1.8 V to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)   |
| VCC_FLSH | D11  | —   | PWR  | Flash interface I/O power: 1.8 V to 3.3 V (Dedicated SPI0 power pin)  |
| VDD_PLLM | H2   | —   | PWR  | MCG PLL (primary clock generator phase lock loop) 1.1-V power   |
| VSS_PLLM | G3   | —   | RTN  | MCG PLL return  |
| VDD_PLLD | J2   | —   | PWR  | DCG PLL (DMD clock generator phase lock loop) 1.1-V power   |
| VSS_PLLD | H3   | —   | RTN  | DCG PLL return  |

表 5-2. I/O Type Subscript Definition

| I/O       |  | SUPPLY REFERENCE   | ESD STRUCTURE                    |
|-----------|--|--|----------------------------------|
| SUBSCRIPT | DESCRIPTION  |  |                                  |
| 1         | 1.8-V LVCMOS I/O buffer with 8-mA drive              | $V_{CC18}$   | ESD diode to GND and supply rail |
| 2         | 1.8-V LVCMOS I/O buffer with 4-mA drive              | $V_{CC18}$   | ESD diode to GND and supply rail |
| 3         | 1.8-V LVCMOS I/O buffer with 24-mA drive             | $V_{CC18}$   | ESD diode to GND and supply rail |
| 4         | 1.8-V sub-LVDS output with 4-mA drive                | $V_{CC18}$   | ESD diode to GND and supply rail |
| 5         | 1.8-V, 2.5-V, 3.3-V LVCMOS with 4-mA drive           | $V_{CC\_INTF}$   | ESD diode to GND and supply rail |
| 6         | 1.8-V LVCMOS input                                   | $V_{CC18}$   | ESD diode to GND and supply rail |
| 7         | 1.8-V, 2.5-V, 3.3-V I <sup>2</sup> C with 3-mA drive | $V_{CC\_INTF}$   | ESD diode to GND and supply rail |
| 8         | 1.8-V I <sup>2</sup> C with 3-mA drive               | $V_{CC18}$   | ESD diode to GND and supply rail |
| 9         | 1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive           | $V_{CC\_INTF}$   | ESD diode to GND and supply rail |
| 10        | DSI LVDS I/O   | $V_{DD}$ for high speed transmit, high speed receive, and low power receive.<br>$V_{DDL12}$ for low power transmit | ESD diode to GND and supply rail |
| 11        | 1.8-V, 2.5-V, 3.3-V LVCMOS input                     | $V_{CC\_INTF}$   | ESD diode to GND and supply rail |
| 12        | 1.8-V, 2.5-V, 3.3-V LVCMOS input                     | $V_{CC\_FLSH}$   | ESD diode to GND and supply rail |
| 13        | 1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive           | $V_{CC\_FLSH}$   | ESD diode to GND and supply rail |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

|  |                                | MIN  | MAX                | UNIT |
|--|--------------------------------|------|--------------------|------|
| <b>SUPPLY VOLTAGE<sup>(2)</sup></b>                        |                                |      |                    |      |
| V <sub>(VDD)</sub>   |                                | -0.3 | 1.21               | V    |
| V <sub>(VDDL P12)</sub>                                    |                                | -0.3 | 1.32               | V    |
| V <sub>(VCC18)</sub>                                       |                                | -0.3 | 1.96               | V    |
| DMD Sub-LVDS Interface (DMD_HS_CLK_x and DMD_HS_WDATA_x_y) |                                | -0.3 | 1.96               | V    |
| V <sub>(VCC_INTF)</sub>                                    |                                | -0.3 | 3.60               | V    |
| V <sub>(VCC_FLSH)</sub>                                    |                                | -0.3 | 3.60               | V    |
| V <sub>(VDD_PLLM)</sub> (MCG PLL)                          |                                | -0.3 | 1.21               | V    |
| V <sub>(VDD_PLLD)</sub> (DCG PLL)                          |                                | -0.3 | 1.21               | V    |
| V <sub>I2C</sub> buffer (I/O type 7)                       |                                | -0.3 | See <sup>(3)</sup> | V    |
| <b>GENERAL</b>   |                                |      |                    |      |
| T <sub>J</sub>   | Operating junction temperature | -30  | 125                | °C   |
| T <sub>stg</sub>   | Storage temperature            | -40  | 125                | °C   |

- (1) Stresses beyond those listed under [セクション 6.1](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [セクション 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to VSS (GND).
- (3) I/O is high voltage tolerant; that is, if VCC\_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC\_INTF = 3.3 V, the input is 5-V tolerant.

### 6.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                         |  | MIN         | NOM   | MAX   | UNIT |   |
|-------------------------|--|-------------|-------|-------|------|---|
| V <sub>(VDD)</sub>      | Core power 1.1 V (main 1.1 V)  | 1.045       | 1.10  | 1.155 | V    |   |
| V <sub>(VDDL12)</sub>   | DSI PHY low power mode driver supply   | See (3) (4) | 1.10  | 1.155 | V    |   |
| V <sub>(VCC18)</sub>    | All 1.8-V I/O power:<br>(1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins.) | 1.64        | 1.80  | 1.96  | V    |   |
| V <sub>(VCC_INTF)</sub> | Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)  | See (1)     | 1.64  | 1.80  | 1.96 | V |
|                         |  |             | 2.28  | 2.50  | 2.72 |   |
|                         |  |             | 3.02  | 3.30  | 3.58 |   |
| V <sub>(VCC_FLSH)</sub> | Flash interface I/O power: 1.8 to 3.3 V  | See (1)     | 1.64  | 1.80  | 1.96 | V |
|                         |  |             | 2.28  | 2.50  | 2.72 |   |
|                         |  |             | 3.02  | 3.30  | 3.58 |   |
| V <sub>(VDD_PLLM)</sub> | MCG PLL 1.1-V power  | See (2)     | 1.100 | 1.155 | V    |   |
| V <sub>(VDD_PLLD)</sub> | DCG PLL 1.1-V power  | See (2)     | 1.100 | 1.155 | V    |   |
| T <sub>A</sub>          | Operating ambient temperature <sup>(5)</sup>   | -30         |       | 85    | °C   |   |
| T <sub>J</sub>          | Operating junction temperature   | -30         |       | 105   | °C   |   |

(1) These supplies have multiple valid ranges.

(2) The minimum voltage is lower than other 1.1-V supply minimum to enable additional filtering. This filtering may result in an IR drop across the filter.

(3) It is recommended that VDDL12 rail is tied to the VDD rail. The DSI LP supply (VDDL12) is only used for read responses from the controller which are not supported. Because of this, a separate 1.2-V rail is not required. If a separate 1.2-V supply is already being used to power this rail, a voltage tolerance of ±6.67% is allowed on this separate 1.2-V supply.

(4) When the DSI-PHY LP supply (VDDL12) is fed from a supply separate from VDD, the VDDL12 power must sequence ON after the 1.1-V core supply and must sequence OFF before the 1.1-V core supply.

(5) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow (R<sub>θJA</sub> at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, and this affects R<sub>θJA</sub>. Thus, maximum operating ambient temperature varies by application.

$$\bullet T_{a\_min} = T_{j\_min} - (P_{d\_min} \times R_{\theta JA}) = -30^{\circ}\text{C} - (0.0\text{ W} \times 30.3^{\circ}\text{C/W}) = -30^{\circ}\text{C}$$

$$\bullet T_{a\_max} = T_{j\_max} - (P_{d\_max} \times R_{\theta JA}) = +105^{\circ}\text{C} - (0.348\text{ W} \times 30.3^{\circ}\text{C/W}) = +94.4^{\circ}\text{C}$$

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |   | DLPC3432                                  | UNIT |
|-------------------------------|---|---|------|
|                               |   | ZVB (NFBGA)                               |      |
|                               |   | 176 PINS                                  |      |
| R <sub>θJC</sub>              | Junction-to-case top thermal resistance   | 11.2                                      | °C/W |
| R <sub>θJA</sub>              | Junction-to-air thermal resistance  | at 0 m/s of forced airflow <sup>(2)</sup> | 30.3 |
|                               |   | at 1 m/s of forced airflow <sup>(2)</sup> | 27.4 |
|                               |   | at 2 m/s of forced airflow <sup>(2)</sup> | 26.6 |
| Ψ <sub>JT</sub>               | Temperature variance from junction to package top center temperature, per unit power dissipation <sup>(3)</sup> | 0.27                                      | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Thermal coefficients abide by JEDEC Standard 51. R<sub>θJA</sub> is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC34xx PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.

(3) Example: (0.5 W) × (0.2°C/W) ≈ 0.1°C temperature rise.



## 6.5 Power Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(1) (2) (3)</sup>   |   | TEST CONDITIONS     | MIN | TYP <sup>(4)</sup> | MAX <sup>(5)</sup> | UNIT |
|--|---|---------------------|-----|--------------------|--------------------|------|
| I <sub>(VDD)</sub> +<br>I <sub>(VDD_PLLM)</sub> +<br>I <sub>(VDD_PLLD)</sub> | 1.1-V rails   | Frame rate = 60 Hz  |     | 124                | 184                | mA   |
|  |   | Frame rate = 120 Hz |     | 161                | 243                |      |
|  |   | Frame rate = 240 Hz |     | 214                | 373                |      |
| I <sub>(VDD_PLLM)</sub>  | MCG PLL 1.1-V current <sup>(6)</sup>  | Frame rate = 60 Hz  |     | 6                  |                    | mA   |
|  |   | Frame rate = 120 Hz |     | 6                  |                    |      |
|  |   | Frame rate = 240 Hz |     | 6                  |                    |      |
| I <sub>(VDD_PLLD)</sub>  | DCG PLL 1.1-V current <sup>(6)</sup>  | Frame rate = 60 Hz  |     | 6                  |                    | mA   |
|  |   | Frame rate = 120 Hz |     | 6                  |                    |      |
|  |   | Frame rate = 240 Hz |     | 6                  |                    |      |
| I <sub>(VCC18)</sub>   | All 1.8-V I/O current: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface) | Frame rate = 60 Hz  |     | 32                 | 44                 | mA   |
|  |   | Frame rate = 120 Hz |     | 32                 | 44                 |      |
|  |   | Frame rate = 240 Hz |     | 32                 | 44                 |      |
| I <sub>(VCC_INTF)</sub>  | Host or parallel interface I/O current: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins) <sup>(6)</sup>    | Frame rate = 60 Hz  |     | 2                  |                    | mA   |
|  |   | Frame rate = 120 Hz |     | 2                  |                    |      |
|  |   | Frame rate = 240 Hz |     | 2                  |                    |      |
| I <sub>(VCC_FLASH)</sub>   | Flash interface I/O current: 1.8 to 3.3 V <sup>(6)</sup>  | Frame rate = 60 Hz  |     | 1                  |                    | mA   |
|  |   | Frame rate = 120 Hz |     | 1                  |                    |      |
|  |   | Frame rate = 240 Hz |     | 1                  |                    |      |

- (1) Values assume all pins using 1.1 V are tied together (including VDDL12), and programmable host and flash I/O are at the minimum nominal voltage (that is 1.8 V).
- (2) Input image is 960 × 540 (qHD) 24 bits using VESA reduced blanking v2 timings on the parallel interface at the frame rate shown with the 0.23-in qHD (DLP230GP) DMD. The controller has the CAIC and LABB algorithms turned off.
- (3) The values do not take into account software updates or customer changes that may affect power performance.
- (4) Assumes nominal process, voltage, and temperature (25°C nominal ambient) with nominal input images.
- (5) Assumes worst case process, maximum voltage, and high nominal ambient temperature of 65°C with worst case input image.
- (6) This rail was not measured due to board limitations. Simulation values are used instead. Simulations assume 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT (standard threshold voltage) or HVT (high threshold voltage) cells

## 6.6 Pin Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |                                    | TEST CONDITIONS <sup>(2)</sup>                             | MIN              | TYP  | MAX            | UNIT               |   |
|--------------------------|------------------------------------|--|------------------|------|----------------|--------------------|---|
| V <sub>IH</sub>          | High-level input threshold voltage | I <sup>2</sup> C buffer (I/O type 7)                       |                  |      | 0.7 × VCC_INTF | See <sup>(3)</sup> | V |
|                          |                                    | I/O type 1, 2, 3, 6, 8 except pins noted in <sup>(4)</sup> | VCC18 = 1.8 V    | 1.17 |                | 3.6                |   |
|                          |                                    | I/O type 1, 6 for pins noted in <sup>(4)</sup>             | VCC18 = 1.8 V    | 1.3  |                | 3.6                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 1.8 V | 1.17 |                | 3.6                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 1.8 V | 1.17 |                | 3.6                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 2.5 V | 1.7  |                | 3.6                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 2.5 V | 1.7  |                | 3.6                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 3.3 V | 2.0  |                | 3.6                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 3.3 V | 2.0  |                | 3.6                |   |
| V <sub>IL</sub>          | Low-level input threshold voltage  | I <sup>2</sup> C buffer (I/O type 7)                       |                  | −0.5 |                | 0.3 × VCC_INTF     | V |
|                          |                                    | I/O type 1, 2, 3, 6, 8 except pins noted in <sup>(4)</sup> | VCC18 = 1.8 V    | −0.3 |                | 0.63               |   |
|                          |                                    | I/O type 1, 6 for pins noted in <sup>(4)</sup>             | VCC18 = 1.8 V    | −0.3 |                | 0.5                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 1.8 V | −0.3 |                | 0.63               |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 1.8 V | −0.3 |                | 0.63               |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 2.5 V | −0.3 |                | 0.7                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 2.5 V | −0.3 |                | 0.7                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 3.3 V | −0.3 |                | 0.8                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 3.3 V | −0.3 |                | 0.8                |   |
| V <sub>OH</sub>          | High-level output voltage          | I/O type 1, 2, 3, 6, 8                                     | VCC18 = 1.8 V    | 1.35 |                |                    | V |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 1.8 V | 1.35 |                |                    |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 1.8 V | 1.35 |                |                    |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 2.5 V | 1.7  |                |                    |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 2.5 V | 1.7  |                |                    |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 3.3 V | 2.4  |                |                    |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 3.3 V | 2.4  |                |                    |   |
| V <sub>OL</sub>          | Low-level output voltage           | I <sup>2</sup> C buffer (I/O type 7)                       | VCC_INTF > 2 V   |      |                | 0.4                | V |
|                          |                                    | I <sup>2</sup> C buffer (I/O type 7)                       | VCC_INTF < 2 V   |      |                | 0.2 × VCC_INTF     |   |
|                          |                                    | I/O type 1, 2, 3, 6, 8                                     | VCC18 = 1.8 V    |      |                | 0.45               |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 1.8 V |      |                | 0.45               |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 1.8 V |      |                | 0.45               |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 2.5 V |      |                | 0.7                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 2.5 V |      |                | 0.7                |   |
|                          |                                    | I/O type 5, 9, 11  | VCC_INTF = 3.3 V |      |                | 0.4                |   |
|                          |                                    | I/O type 12, 13  | VCC_FLSH = 3.3 V |      |                | 0.4                |   |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |  | TEST CONDITIONS <sup>(2)</sup>       | MIN              | TYP  | MAX | UNIT |
|--------------------------|--|--------------------------------------|------------------|------|-----|------|
| I <sub>OH</sub>          | High-level output current <sup>(5)</sup> | I/O type 2, 4                        | VCC18 = 1.8 V    | 2    |     | mA   |
|                          |  | I/O type 5                           | VCC_INTF = 1.8 V | 2    |     |      |
|                          |  | I/O type 1                           | VCC18 = 1.8 V    | 3.5  |     |      |
|                          |  | I/O type 9                           | VCC_INTF = 1.8 V | 3.5  |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 1.8 V | 3.5  |     |      |
|                          |  | I/O type 3                           | VCC18 = 1.8 V    | 10.6 |     |      |
|                          |  | I/O type 5                           | VCC_INTF = 2.5 V | 5.4  |     |      |
|                          |  | I/O type 9, 13                       | VCC_INTF = 2.5 V | 10.8 |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 2.5 V | 10.8 |     |      |
|                          |  | I/O type 5                           | VCC_INTF = 3.3 V | 7.8  |     |      |
|                          |  | I/O type 9                           | VCC_INTF = 3.3 V | 15   |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 3.3 V | 15   |     |      |
| I <sub>OL</sub>          | Low-level output current <sup>(6)</sup>  | I <sup>2</sup> C buffer (I/O type 7) |                  | 3    |     | mA   |
|                          |  | I/O type 2, 4                        | VCC18 = 1.8 V    | 2.3  |     |      |
|                          |  | I/O type 5                           | VCC_INTF = 1.8 V | 2.3  |     |      |
|                          |  | I/O type 1                           | VCC18 = 1.8 V    | 4.6  |     |      |
|                          |  | I/O type 9                           | VCC_INTF = 1.8 V | 4.6  |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 1.8 V | 4.6  |     |      |
|                          |  | I/O type 3                           | VCC18 = 1.8 V    | 13.9 |     |      |
|                          |  | I/O type 5                           | VCC_INTF = 2.5 V | 5.2  |     |      |
|                          |  | I/O type 9                           | VCC_INTF = 2.5 V | 10.4 |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 2.5 V | 10.4 |     |      |
|                          |  | I/O type 5                           | VCC_INTF = 3.3 V | 4.4  |     |      |
|                          |  | I/O type 9                           | VCC_INTF = 3.3 V | 8.9  |     |      |
|                          |  | I/O type 13                          | VCC_FLSH = 3.3 V | 8.9  |     |      |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(1)</sup> |                                       | TEST CONDITIONS <sup>(2)</sup>         | MIN  | TYP | MAX | UNIT |    |
|--------------------------|---------------------------------------|--|--|-----|-----|------|----|
| I <sub>oz</sub>          | High-impedance leakage current        | I <sup>2</sup> C buffer (I/O type 7)   | V <sub>I2C buffer</sub> < 0.1 × VCC_INTF or V <sub>I2C buffer</sub> > 0.9 × VCC_INTF | -10 |     | 10   | μA |
|                          |                                       | I/O type 1, 2, 3, 6, 8                 | VCC18 = 1.8 V  | -10 |     | 10   |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 1.8 V   | -10 |     | 10   |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 1.8 V   | -10 |     | 10   |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 2.5 V   | -10 |     | 10   |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 2.5 V   | -10 |     | 10   |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 3.3 V   | -10 |     | 10   |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 3.3 V   | -10 |     | 10   |    |
| C <sub>i</sub>           | Input capacitance (including package) | I <sup>2</sup> C buffer (I/O type 7)   |  |     |     | 5    | pF |
|                          |                                       | I/O type 1, 2, 3, 6, 8                 | VCC18 = 1.8 V  | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 1.8 V   | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 1.8 V   | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 2.5 V   | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 2.5 V   | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 5, 9, 11                      | VCC_INTF = 3.3 V   | 2.6 |     | 3.5  |    |
|                          |                                       | I/O type 12, 13                        | VCC_FLSH = 3.3 V   | 2.6 |     | 3.5  |    |
|                          |                                       | Sub-LVDS – DMD high speed (I/O type 4) | VCC18 = 1.8 V  |     |     |      |    |

(1) The I/O type refers to the type defined in 表 5-2.

(2) Test conditions that define a value for VCC18, VCC\_INTF, or VCC\_FLSH show the nominal voltage that the specified I/O's supply reference is set to.

(3) I/O is high voltage tolerant; that is, if VCC\_INTF = 1.8 V, the input is 3.3-V tolerant, and if VCC\_INTF = 3.3 V, the input is 5-V tolerant.

(4) Controller pins CMP\_OUT, PARKZ, RESETZ, and GPIO\_00 through GPIO\_19 have slightly varied V<sub>IH</sub> and V<sub>IL</sub> range from other 1.8-V I/O.

(5) At a high level output signal, the given I/O will be able to output at least the minimum current specified.

(6) At a low level output signal, the given I/O will be able to sink at least the minimum current specified.

## 6.7 Internal Pullup and Pulldown Electrical Characteristics

over operating free-air temperature (unless otherwise noted)<sup>(2)</sup>

| INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS | TEST CONDITIONS <sup>(1)</sup> | MIN | MAX | UNIT |
|---|--------------------------------|-----|-----|------|
| Weak pullup resistance                                | VCCIO = 3.3 V                  | 29  | 63  | kΩ   |
|   | VCCIO = 2.5 V                  | 38  | 90  |      |
|   | VCCIO = 1.8 V                  | 56  | 148 |      |
| Weak pulldown resistance                              | VCCIO = 3.3 V                  | 30  | 72  | kΩ   |
|   | VCCIO = 2.5 V                  | 36  | 101 |      |
|   | VCCIO = 1.8 V                  | 52  | 167 |      |

(1) The resistance is dependent on VCCIO, the pin's supply reference (see a given pins supply reference in 表 5-2).

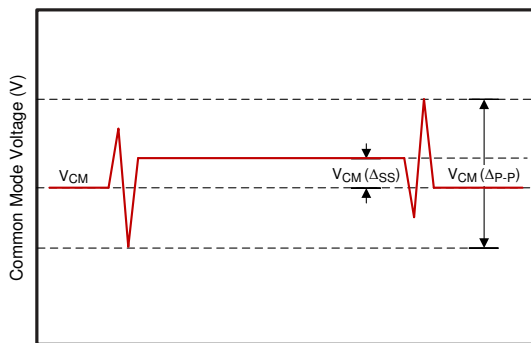
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

## 6.8 DMD Sub-LVDS Interface Electrical Characteristics

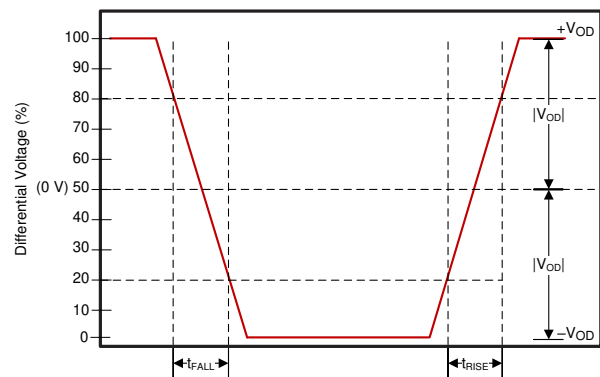
over operating free-air temperature range (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS   | MIN   | TYP   | MAX   | UNIT     |
|------------------------------|---|-------|-------|-------|----------|
| $V_{CM}$                     | Common mode voltage   | 0.8   | 0.9   | 1.0   | V        |
| $V_{CM} (\Delta_{pp})^{(1)}$ | $V_{CM}$ change peak-to-peak (during switching)                           |       |       | 75    | mV       |
| $V_{CM} (\Delta_{ss})^{(1)}$ | $V_{CM}$ change steady state  | -10   |       | 10    | mV       |
| $ V_{OD} ^{(2)}$             | Differential output voltage magnitude                                     | 170   | 250   | 350   | mV       |
| $V_{OD} (\Delta)$            | $V_{OD}$ change (between logic states)                                    | -10   |       | 10    | mV       |
| $V_{OH}$                     | Single-ended output voltage high  | 0.825 | 1.025 | 1.175 | V        |
| $V_{OL}$                     | Single-ended output voltage low   | 0.625 | 0.775 | 0.975 | V        |
| $T_{Xterm}$                  | Internal differential termination   | 80    | 100   | 120   | $\Omega$ |
| $T_{Xload}$                  | 100- $\Omega$ differential PCB trace<br>(50- $\Omega$ transmission lines) | 0.5   |       | 6     | in       |

- (1) See [Figure 6-1](#).  
 (2)  $V_{OD}$  is the differential voltage measured across a 100- $\Omega$  termination resistance connected directly between the transmitter differential pins.  $V_{OD} = V_P - V_N$ , where P and N are the differential output pins.  $|V_{OD}|$  is the magnitude of the peak-to-peak voltage swing across the P and N output pins (see [Figure 6-2](#)).  $V_{CM}$  cancels out between signals when measured differentially, thus the reason  $V_{OD}$  swings relative to zero.



**Figure 6-1. Common Mode Voltage**



$V_{CM}$  is removed when the signals are viewed differentially.

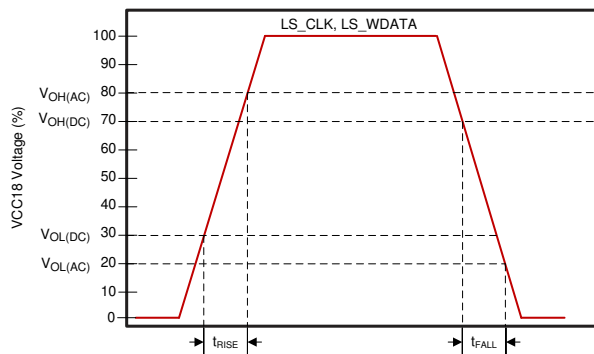
**Figure 6-2. Differential Output Signal**

## 6.9 DMD Low-Speed Interface Electrical Characteristics

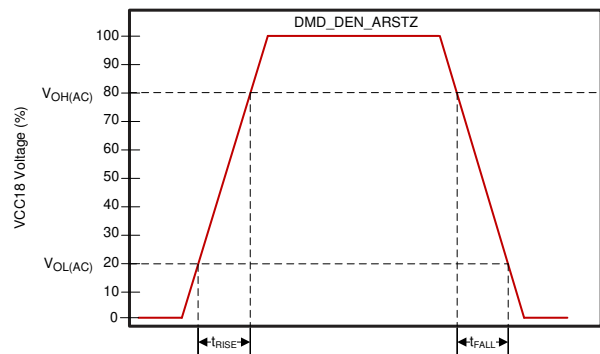
over operating free-air temperature range (unless otherwise noted)

| PARAMETER <sup>(3)</sup>    |  | TEST CONDITIONS  | MIN                   | TYP                   | MAX                   | UNIT |
|-----------------------------|--|--|-----------------------|-----------------------|-----------------------|------|
| $V_{OH(DC)}$                | DC output high voltage for DMD_LS_WDATA and DMD_LS_CLK |  | $0.7 \times V_{CC18}$ |                       |                       | V    |
| $V_{OL(DC)}$                | DC output low voltage for DMD_LS_WDATA and DMD_LS_CLK  |  |                       |                       | $0.3 \times V_{CC18}$ | V    |
| $V_{OH(AC)}$ <sup>(1)</sup> | AC output high voltage for DMD_LS_WDATA and DMD_LS_CLK |  | $0.8 \times V_{CC18}$ | $V_{CC18} + 0.5$      |                       | V    |
| $V_{OL(AC)}$ <sup>(2)</sup> | AC output low voltage for DMD_LS_WDATA and DMD_LS_CLK  |  | -0.5                  | $0.2 \times V_{CC18}$ |                       | V    |
| Slew rate                   | DMD_LS_WDATA and DMD_LS_CLK                            | $V_{OL(DC)}$ to $V_{OH(AC)}$ for rising edge and $V_{OH(DC)}$ to $V_{OL(AC)}$ for falling edge | 1.0                   |                       | 3.0                   | V/ns |
|                             | DMD_DEN_ARSTZ  | $V_{OL(AC)}$ to $V_{OH(AC)}$ for rising edge   | 0.25                  |                       |                       |      |
|                             | DMD_LS_RDATA   |  | 0.5                   |                       |                       |      |

- $V_{OH(AC)}$  maximum applies to overshoot. When the DMD\_LS\_WDATA and DMD\_LS\_CLK lines include a proper 43- $\Omega$  series termination resistor, the DMD operates within the LPSDR input AC specifications.
- $V_{OL(AC)}$  minimum applies to undershoot. When the DMD\_LS\_WDATA and DMD\_LS\_CLK lines include a proper 43- $\Omega$  series termination resistor, the DMD operates within the LPSDR input AC specifications.
- See [Figure 6-3](#) for DMD\_LS\_CLK, and DMD\_LS\_WDATA rise and fall times. See [Figure 6-4](#) for DMD\_DEN\_ARSTZ rise and fall times.



**Figure 6-3. LS\_CLK and LS\_WDATA Slew Rate**

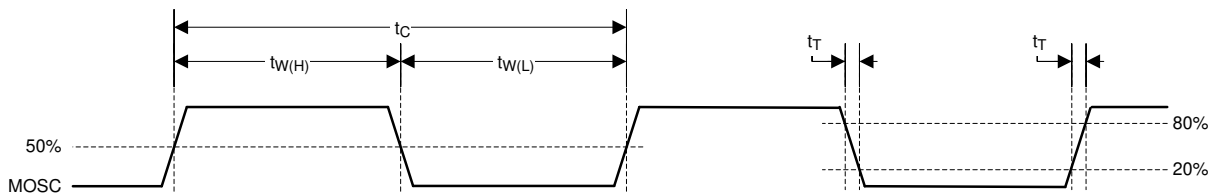


**Figure 6-4. DMD\_DEN\_ARSTZ Slew Rate**

## 6.10 System Oscillator Timing Requirements

|            |  |   | MIN    | NOM    | MAX    | UNIT |
|------------|--|---|--------|--------|--------|------|
| $f_{clk}$  | Clock frequency, MOSC (primary oscillator clock) <sup>(1)</sup>  |   | 23.998 | 24.000 | 24.002 | MHz  |
| $t_c$      | Cycle time, MOSC (clock period) <sup>(1)</sup>   | See <a href="#">Figure 6-5</a>  | 41.663 | 41.667 | 41.670 | ns   |
| $t_{w(H)}$ | Pulse duration as percent of $t_c$ <sup>(2)</sup> , MOSC, high   | 50% to 50% reference points (signal)  | 40%    | 50%    |        |      |
| $t_{w(L)}$ | Pulse duration as percent of $t_c$ <sup>(2)</sup> , MOSC, low  | 50% to 50% reference points (signal)  | 40%    | 50%    |        |      |
| $t_t$      | Transition time <sup>(2)</sup> , MOSC  | 20% to 80% reference points (rising signal)<br>80% to 20% reference points (falling signal) |        |        | 10     | ns   |
| $t_{jp}$   | Long-term, peak-to-peak, period jitter <sup>(2)</sup> , MOSC (that is the deviation in period from ideal period due solely to high frequency jitter) |   |        |        | 2%     |      |

- (1) The frequency accuracy for MOSC is  $\pm 200$  PPM. This includes impact to accuracy due to aging, temperature, and trim sensitivity. The MOSC input does not support spread spectrum clock spreading.
- (2) Applies only when driven by an external digital oscillator.

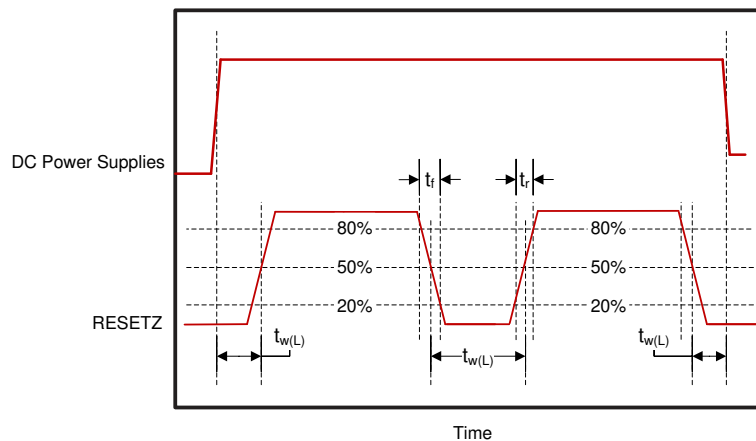


**Figure 6-5. System Oscillators**

## 6.11 Power Supply and Reset Timing Requirements

|            |  |                                      | MIN  | MAX | UNIT    |
|------------|--|--------------------------------------|------|-----|---------|
| $t_{w(L)}$ | Pulse duration, active low, RESETZ             | 50% to 50% reference points (signal) | 1.25 |     | $\mu$ s |
| $t_r$      | Rise time, RESETZ <sup>(1)</sup>               | 20% to 80% reference points (signal) |      | 0.5 | $\mu$ s |
| $t_f$      | Fall time, RESETZ <sup>(1)</sup>               | 80% to 20% reference points (signal) |      | 0.5 | $\mu$ s |
| $t_{rise}$ | Rise time, VDD (during VDD ramp up at turn-on) | 0.3 V to 1.045 V (VDD)               |      | 1   | ms      |

- (1) For more information on RESETZ, see [Section 5](#).



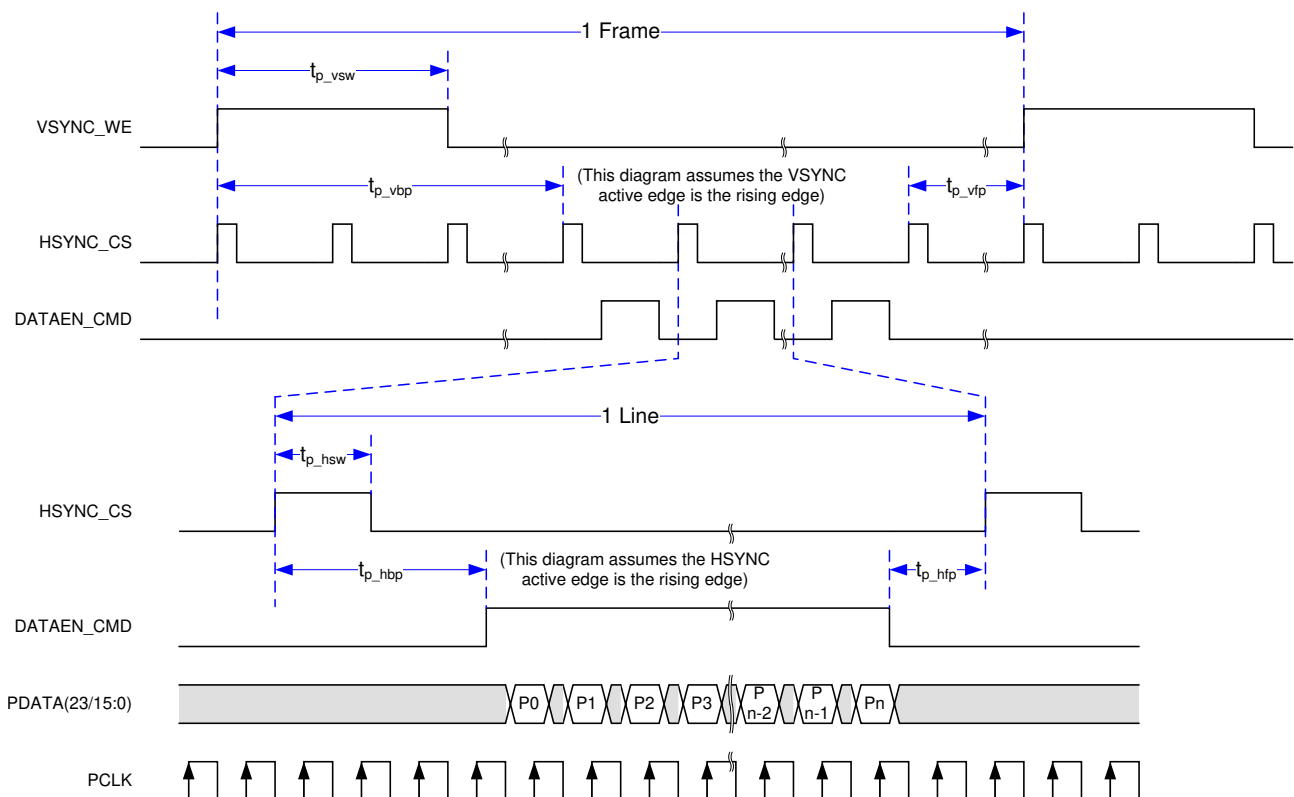
**Figure 6-6. Power-Up and Power-Down RESETZ Timing**

## 6.12 Parallel Interface Frame Timing Requirements

See [セクション 11.1.3](#) for additional information

|              |  |                      | MIN     | MAX | UNIT  |
|--------------|--|----------------------|---------|-----|-------|
| $t_{p\_vsw}$ | Pulse duration – default VSYNC_WE high   | 50% reference points | 1       |     | lines |
| $t_{p\_vbp}$ | Vertical back porch (VBP) – time from the active edge of VSYNC_WE to the active edge of HSYNC_CS for the first active line <sup>(1)</sup>                      | 50% reference points | 2       |     | lines |
| $t_{p\_vfp}$ | Vertical front porch (VFP) – time from the active edge of the HSYNC_CS following the last active line in a frame to the active edge of VSYNC_WE <sup>(1)</sup> | 50% reference points | 1       |     | lines |
| $t_{p\_tvb}$ | Total vertical blanking – the sum of VBP and VFP ( $t_{p\_vbp} + t_{p\_vfp}$ )   | 50% reference points | See (1) |     | lines |
| $t_{p\_hsw}$ | Pulse duration – default HSYNC_CS high   | 50% reference points | 4       | 128 | PCLKs |
| $t_{p\_hbp}$ | Horizontal back porch (HBP) – time from the active edge of HSYNC_CS to the rising edge of DATAEN_CMD   | 50% reference points | 4       |     | PCLKs |
| $t_{p\_hfp}$ | Horizontal front porch (HFP) – time from the falling edge of DATAEN_CMD to the active edge of HSYNC_CS   | 50% reference points | 8       |     | PCLKs |

- (1) The minimum total vertical blanking is defined by the following equation:  $t_{p\_tvb}(\min) = 6 + [8 \times \text{Max}(1, \text{Source\_ALPF} / \text{DMD\_ALPF})]$  lines  
 where:
- SOURCE\_ALPF = Input source active lines per frame
  - DMD\_ALPF = Actual DMD used lines per frame supported



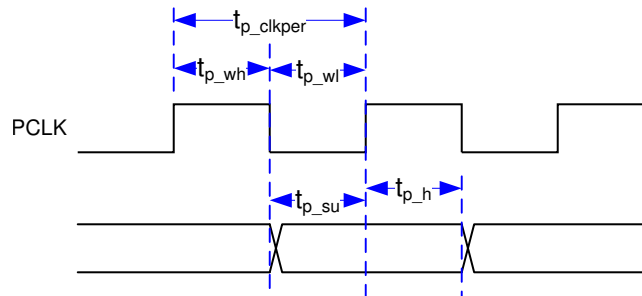
6-7. Parallel Interface Frame Timing



### 6.13 Parallel Interface General Timing Requirements

|                         |   |   | MIN  | MAX     | UNIT |
|-------------------------|---|---|------|---------|------|
| $f_{\text{clock}}$      | PCLK frequency  |   | 1.0  | 155.0   | MHz  |
| $t_{\text{p\_clkper}}$  | PCLK period   | 50% reference points  | 6.45 | 1000    | ns   |
| $t_{\text{p\_clkjit}}$  | PCLK jitter   | Max $f_{\text{clock}}$  |      | See (1) |      |
| $t_{\text{p\_wh}}$      | PCLK pulse duration high  | 50% reference points  | 2.43 |         | ns   |
| $t_{\text{p\_wl}}$      | PCLK pulse duration low   | 50% reference points  | 2.43 |         | ns   |
| $t_{\text{p\_su}}$      | Setup time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid before the active edge of PCLK | 50% reference points  | 0.9  |         | ns   |
| $t_{\text{p\_h}}$       | Hold time – HSYNC_CS, DATAEN_CMD, PDATA(23:0) valid after the active edge of PCLK   | 50% reference points  | 0.9  |         | ns   |
| $t_{\text{t}}$          | Transition time – all signals   | 20% to 80% reference points (rising signal)<br>80% to 20% reference points (falling signal) | 0.2  | 2.0     | ns   |
| $t_{\text{setup, 3DR}}$ | This is the setup time with respect to VSYNC(2)                                     | 50% reference points  | 1.0  |         | ms   |
| $t_{\text{hold, 3DR}}$  | This is the hold time with respect VSYNC(3)   | 50% reference points  | 1.0  |         | ms   |

- (1) Calculate clock jitter (in ns) using this formula:  $\text{Jitter} = [1 / f_{\text{clock}} - 5.76 \text{ ns}]$ . Setup and hold times must be met even with clock jitter.
- (2) In other words, the 3DR signal must change at least 1.0 ms before VSYNC changes.
- (3) In other words, the 3DR signal must not change for at least 1.0 ms after VSYNC changes.



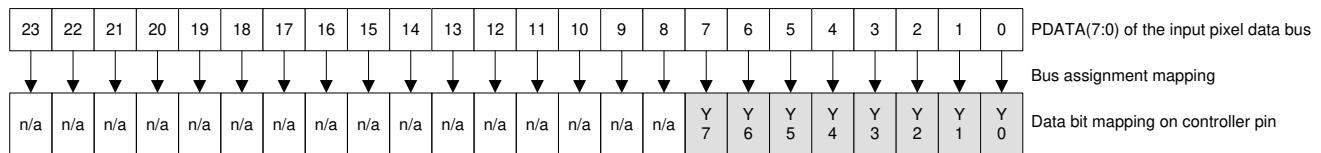
**6-8. Parallel Interface Pixel Timing**

## 6.14 BT656 Interface General Timing Requirements

The DLPC34xx controller input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.<sup>(2)</sup>

|                        |  | MIN   | MAX                | UNIT |    |
|------------------------|--|---|--------------------|------|----|
| $f_{\text{cll}}$       | PCLK frequency   | 1.0   | 33.5               | MHz  |    |
| $t_{\text{p\_clkper}}$ | PCLK period  | 50% reference points  | 29.85              | 1000 | ns |
| $t_{\text{p\_clkjit}}$ | PCLK jitter  | Max $f_{\text{clock}}$  | See <sup>(1)</sup> |      |    |
| $t_{\text{p\_wh}}$     | PCLK pulse duration high                               | 50% reference points  | 10.0               | ns   |    |
| $t_{\text{p\_wl}}$     | PCLK pulse duration low                                | 50% reference points  | 10.0               | ns   |    |
| $t_{\text{p\_su}}$     | Setup time – PDATA(7:0) before the active edge of PCLK | 50% reference points  | 3.0                | ns   |    |
| $t_{\text{p\_h}}$      | Hold time – PDATA(7:0) after the active edge of PCLK   | 50% reference points  | 0.9                | ns   |    |
| $t_{\text{t}}$         | Transition time – all signals                          | 20% to 80% reference points (rising signal)<br>80% to 20% reference points (falling signal) | 0.2                | 3.0  | ns |

- Calculate clock jitter (in ns) using this formula: Jitter =  $[1 / f_{\text{clock}} - 5.76 \text{ ns}]$ . Clock jitter must maintain setup and hold times. BT.656 data bits must be mapped to the DLPC34xx PDATA bus as shown in [Figure 6-9](#) shows BT.656 bus mode YCbCr 4:2:2 source PDATA (23:0) mapping.
- The BT.656 interface accepts 8-bits per color, 4:2:2 YCbCr data encoded per the industry standard through PDATA(7:0) on the active edge of PCLK. See [Figure 6-9](#).



**Figure 6-9. BT.656 Interface Mode Bit Mapping**

## 6.15 DSI Host Timing Requirements

These timing requirements describe specific host minimum values that are higher than those specified in the MIPI standards. It is critical for proper operation that the host meet these minimum timing requirements for specified MIPI parameters. The decoded DSI data must also follow all [Section 6.12](#).

|  |   | MIN                                       | MAX                | UNIT  |
|--|---|---|--------------------|-------|
| Clock lane                                   | Frequency   | 80  | 235                | MHz   |
| Data lane                                    | Effective data rate   | 160                                       | 470                | Mbps  |
| Number of data lanes                         | Selectable  | 1   | 4                  | lanes |
| $t_{\text{HS-PREPARE}} + t_{\text{HS-ZERO}}$ | During a LP to HS transition, the time that the transmitter drives the HS-0 state prior to transmitting the synchronization sequence  | 80-MHz to 94-MHz HS clock                 | 565                | ns    |
|  |   | 95-MHz to 235-MHz HS clock <sup>(1)</sup> | 465 <sup>(2)</sup> |       |
| $t_{\text{HS-SETTLE}}$                       | Time interval during which the HS receiver ignores any data lane HS transitions, starting from the beginning of $T_{\text{HS-PREPARE}}$ ; the HS receiver ignores any data lane transitions before the minimum value, and responds to any data lane transitions after the maximum value | 80-MHz to 94-MHz HS clock                 | 565 <sup>(3)</sup> | ns    |
|  |   | 95-MHz to 235-MHz HS clock                | 465 <sup>(3)</sup> |       |

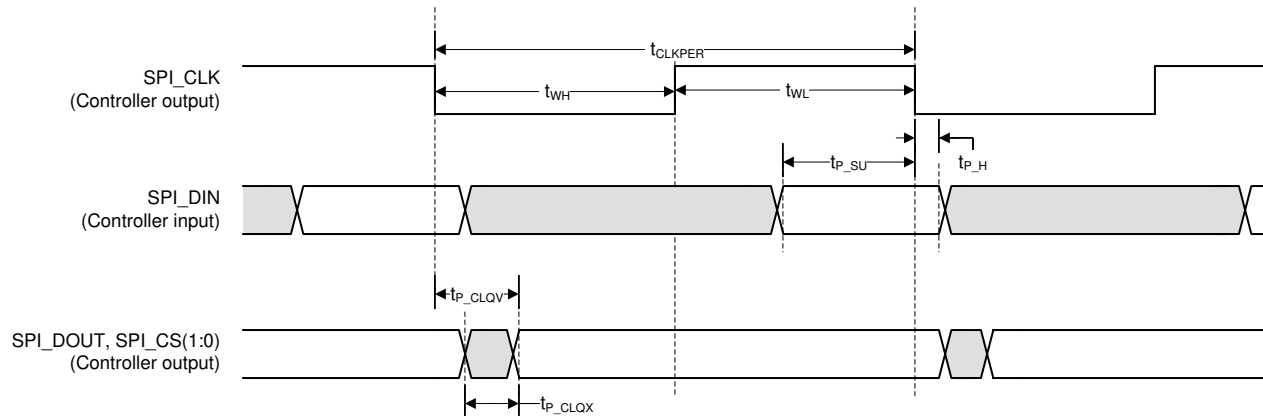
- Example: At 172 MHz and  $t_{\text{HS-PREPARE}} = 51.46 \text{ ns} \rightarrow 51.46 \text{ ns} + t_{\text{HS-ZERO}} \geq 465 \text{ ns}$ . Therefore  $t_{\text{HS-ZERO}} \geq 413.54 \text{ ns}$ .
- Minimum values are higher than those required by the MIPI standard.  $t_{\text{HS-PREPARE}}$  must be within the MIPI specified range.
- Maximum values are higher than those required by the MIPI standard.

## 6.16 Flash Interface Timing Requirements

The DLPC34xx flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC34xx can support 1- to 128-Mb flash memories. <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup>

|                        |  |   | MIN  | MAX  | UNIT |
|------------------------|--|---|------|------|------|
| $f_{\text{clock}}$     | SPI_CLK frequency  | See <sup>(1)</sup>  | 1.4  | 36.0 | MHz  |
| $t_{\text{p\_clkper}}$ | SPI_CLK period   | 50% reference points  | 27.8 | 704  | ns   |
| $t_{\text{p\_wh}}$     | SPI_CLK pulse duration high  | 50% reference points  | 352  |      | ns   |
| $t_{\text{p\_wl}}$     | SPI_CLK pulse duration low   | 50% reference points  | 352  |      | ns   |
| $t_t$                  | Transition time – all signals  | 20% to 80% reference points (rising signal)<br>80% to 20% reference points (falling signal) | 0.2  | 3.0  | ns   |
| $t_{\text{p\_su}}$     | Setup time – SPI_DIN valid before SPI_CLK falling edge                 | 50% reference points  | 10.0 |      | ns   |
| $t_{\text{p\_h}}$      | Hold time – SPI_DIN valid after SPI_CLK falling edge                   | 50% reference points  | 0.0  |      | ns   |
| $t_{\text{p\_clqv}}$   | SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ | 50% reference points  |      | 1.0  | ns   |
| $t_{\text{p\_clqx}}$   | SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ     | 50% reference points  | -3.0 | 3.0  | ns   |

- (1) This range include the  $\pm 200$  ppm of the external oscillator (but no jitter).
- (2) Standard SPI protocol is to transmit data on the falling edge of SPI\_CLK and capture data on the rising edge. The DLPC34xx does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC34xx hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
- (3) With the above output timing, DLPC34xx provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI\_CLK.
- (4) For additional requirements of the external flash device view the [セクション 7.3.3.1](#) section.



**6-10. Flash Interface Timing**

## 6.17 Other Timing Requirements

|  |                             | MIN | MAX | UNIT |
|--|-----------------------------|-----|-----|------|
| $t_{rise, all}^{(1)(2)}$                                 | 20% to 80% reference points |     | 10  | ns   |
| $t_{fall, all}^{(1)(2)}$                                 | 80% to 20% reference points |     | 10  | ns   |
| $t_{rise, PARKZ}^{(2)}$                                  | 20% to 80% reference points |     | 150 | ns   |
| $t_{fall, PARKZ}^{(2)}$                                  | 80% to 20% reference points |     | 150 | ns   |
| $t_w, GPIO\_08$ (PROJ_ON) pulse width low <sup>(3)</sup> |                             | 200 |     | ms   |
| I <sup>2</sup> C baud rate                               |                             |     | 100 | kHz  |

(1) Unless noted elsewhere, the following signal transition times are for all DLPC34xx signals.

(2) This is the recommended signal transition time to avoid input buffer oscillations.

(3) When the controller is turned off by setting PROJ\_ON low, PROJ\_ON must not be brought high again for at least 200 ms. View [セクション 9.3](#) for additional requirements.

## 6.18 DMD Sub-LVDS Interface Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER    |                                | TEST CONDITIONS | MIN | TYP  | MAX | UNIT |
|--------------|--------------------------------|-----------------|-----|------|-----|------|
| $t_R^{(1)}$  | Differential output rise time  |                 |     |      | 250 | ps   |
| $t_F^{(1)}$  | Differential output fall time  |                 |     |      | 250 | ps   |
| $t_{switch}$ | DMD HS clock switching rate    |                 |     | 1200 |     | Mbps |
| $f_{clock}$  | DMD HS clock frequency         |                 |     | 600  |     | MHz  |
| DCout        | DMD HS clock output duty cycle |                 | 45% | 50%  | 55% |      |

(1) Rise and fall times are defined for the differential  $V_{OD}$  signal as shown in [図 6-2](#).

## 6.19 DMD Parking Switching Characteristics

See [\(2\)](#)

| PARAMETER        |                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT    |
|------------------|---------------------------------|-----------------|-----|-----|-----|---------|
| $t_{park}$       | Normal park time <sup>(1)</sup> |                 |     |     | 20  | ms      |
| $t_{fast\ park}$ | Fast park time <sup>(3)</sup>   |                 |     |     | 32  | $\mu$ s |

(1) Normal park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the normal park request (GPIO\_08 goes low).

(2) The oscillator and power supplies must remain active for at least the duration of the park time. The power supplies must additionally be held on for a time after parking is completed to satisfy DMD requirements. See [セクション 9.2](#) and the appropriate DMD or PMIC datasheet for more information.

(3) Fast park time is defined as how long it takes the DLPC34xx controller to complete the parking of the DMD after it receives the fast park request (PARKZ goes low).

## 6.20 Chipset Component Usage Specification

The DLPC3432 is a component of a DLP chipset. Reliable function and operation of the DLP chipset requires that it be used with all components (DMD, PMIC, and controller) of the applicable DLP chipset.

**表 6-1. DLPC3432 Supported DMDs and PMICs**

| DLPC3432 DLP Chipset |          |
|----------------------|----------|
| DMD                  | DLP230GP |
| PMIC                 | DLPA2000 |
|                      | DLPA2005 |
|                      | DLPA3000 |

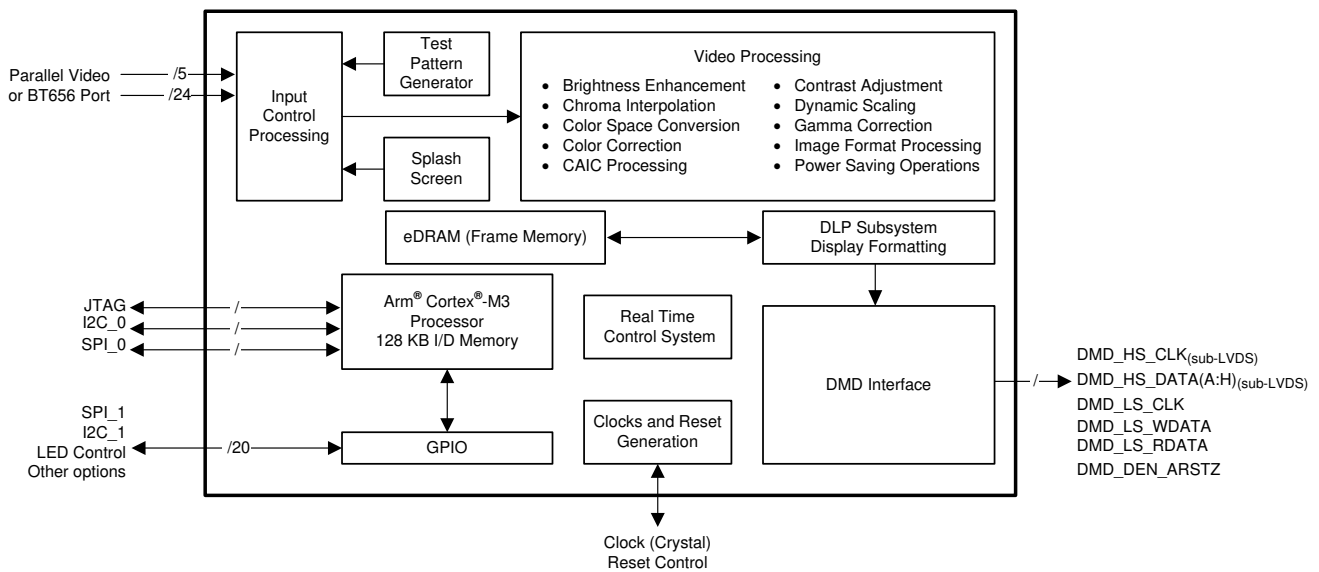
## 7 Detailed Description

### 7.1 Overview

The DLPC3432 part is a display controller for the DLP230GP (.23 qHD) DMD. The DLPC3432 controller is part of the chipset composed of the controller, DLP230GP (.23 qHD) DMD, and DLPAXxxx PMIC (which includes an LED driver). To ensure reliable operation of the DLP chipset, the DLPC34xx must always be used with the supported devices shown in 表 6-1.

The DLPC34xx display controller provides interfaces along with data and image processing functions that are optimized for small form factor and power-constrained display applications. Applications include projection within mobile projectors, smart displays, smartphones, tablets, augmented reality glasses, mobile accessories, smart home displays, and pico projectors. The DLPC3432 is not a front-end processor; therefore, standalone projectors must include a separate front-end chip to interface to the outside world (for example, a video decoder, HDMI receiver, or USB I/F chip).

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Input Source Requirements

#### 7.3.1.1 Supported Resolution and Frame Rates

**表 7-1. Supported Input Source Ranges<sup>(1) (2) (3)</sup>**

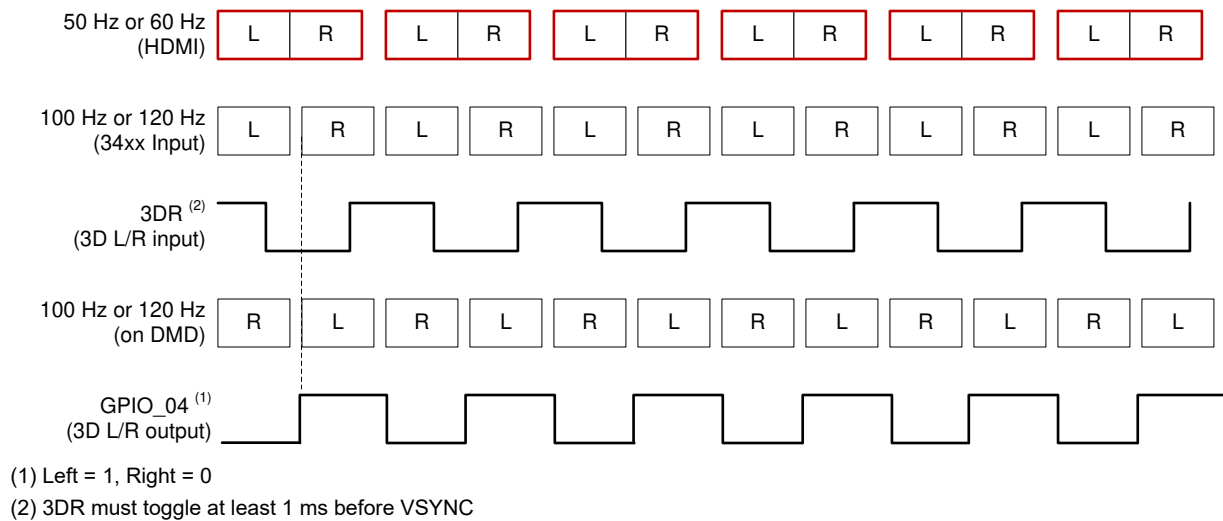
| INTERFACE                  | BITS PER PIXEL<br>(max) <sup>(5)</sup> | IMAGE TYPE | SOURCE RESOLUTION RANGE <sup>(7)</sup> (pixels) |            |            |            | FRAME RATE<br>RANGE<br>(Hz) |
|----------------------------|--|------------|---|------------|------------|------------|-----------------------------|
|                            |  |            | HORIZONTAL                                      |            | VERTICAL   |            |                             |
|                            |  |            | Landscape                                       | Portrait   | Landscape  | Portrait   |                             |
| Parallel                   | 24                                     | 2D only    | 400 to 960                                      | 200 to 540 | 200 to 540 | 400 to 960 | 10 to 242                   |
|                            | 24                                     | 3D only    | 400 to 960                                      | 200 to 540 | 200 to 540 | 400 to 960 | 100 ± 2<br>120 ± 2          |
| DSI <sup>(8)</sup>         | 24                                     | 2D only    | 400 to 960                                      | 200 to 540 | 200 to 540 | 400 to 960 | 10 to 122                   |
| BT.656-NTSC <sup>(4)</sup> | See <sup>(6)</sup>                     | 2D only    | 720   | N/A        | 240        | N/A        | 60 ± 2                      |
| BT.656-PAL <sup>(4)</sup>  | See <sup>(6)</sup>                     | 2D only    | 720   | N/A        | 288        | N/A        | 50 ± 2                      |

- (1) The application must remain within specifications for all source interface parameters such as maximum clock rate and maximum line rate.
- (2) The maximum DMD size for all rows in the table is 960 × 540 pixels.
- (3) To achieve the ranges stated, the firmware must support the source parameters. Review the firmware release notes or contact TI to determine the latest available frame rate and input resolution support for a given firmware image.
- (4) All parameters in this row follow the BT.656 standard. The image format is always landscape.
- (5) Bits per pixel does not necessarily equal the number of data pins used on the DLPC34xx controller.
- (6) BT.656 uses 16-bit 4:2:2 YCbCr.
- (7) By using an I<sup>2</sup>C command, the controller can rotate portrait image inputs on the DMD by minus 90 degrees so that the image displays in landscape format.
- (8) Applications may require up to four DSI lanes in order to fully utilize the available DSI bandwidth (and therefore achieve the maximum display rates and resolutions).

### 7.3.1.2 3D Display

For 3D sources on the video input interface, images must be frame sequential (L, R, L, ...) when input to the DLPC34xx controller. Any processing required to unpack 3D images and to convert them to frame sequential input must be done by external electronics prior to inputting the images to the controller. Each 3D source frame input must contain a single eye frame of data, separated by a VSYNC, where an eye frame contains image data for a single left or right eye. The signal 3DR input to the controller indicates whether the input frame is for the left eye or right eye.

Each DMD frame is displayed at the same rate as the input interface frame rate. [Figure 7-1](#) below shows the typical timing for a 50-Hz or 60-Hz 3D HDMI source frame, the input interface of the DLPC34xx controller, and the DMD. In general, video frames sent over the HDMI interface pack both the left and right content into the same video frame. GPIO\_04 is optionally sent to a transmitter on the system PCB for wirelessly transmitting a synchronization signal to 3D glasses (usually an IR sync signal). The glasses are then in phase with the DMD images displayed. Alternately, the *3D Glasses Operation* section shows how DLP link pulses can be used instead.



**Figure 7-1. 3D Display Left and Right Frame Timing**

### 7.3.1.3 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes the signals listed in [表 7-2](#).

**表 7-2. Parallel Interface Signals**

| SIGNAL     | DESCRIPTION                   |
|------------|-------------------------------|
| VSYNC_WE   | vertical sync                 |
| HSYNC_CS   | horizontal sync               |
| DATAEN_CMD | data valid                    |
| PDATA      | 24-bit data bus               |
| PCLK       | pixel clock                   |
| PDM_CVS_TE | parallel data mask (optional) |

#### 注

VSYNC\_WE must remain active at all times when using parallel RGB mode. When this signal is no longer active, the display sequencer stops and causes the LEDs to turn off.

The active edge of both sync signals are variable. The *Parallel Interface Frame Timing Requirements* section shows the relationship of these signals.

An optional parallel data mask signal (PDM\_CVS\_TE) allows periodic frame updates to be stopped without losing the displayed image. When active, PDM\_CVS\_TE acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. PDM\_CVS\_TE defaults to active high. To disable the data mask function, tie PDM\_CVS\_TE to a logic low signal. PDM\_CVS\_TE must only change during vertical blanking.

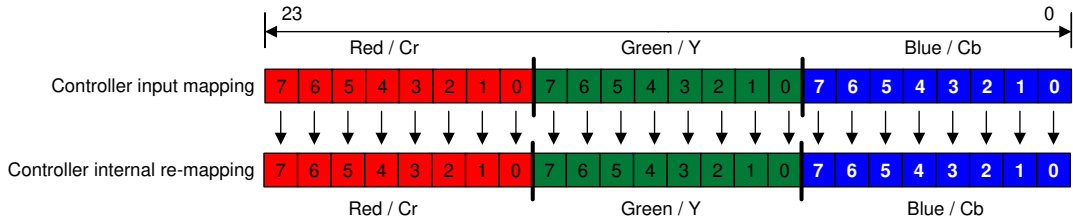
The parallel interface supports six data transfer formats. They are as follows:

- 24-bit RGB888 or 24-bit YCbCr888 on a 24 data wire interface
- 18-bit RGB666 or 18-bit YCbCr666 on an 18 data wire interface
- 16-bit RGB565 or 16-bit YCbCr565 on a 16 data wire interface
- 16-bit YCbCr 4:2:2 (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, ...)
- 8-bit RGB888 or 8-bit YCbCr888 serial (1 color per clock input; 3 clocks per displayed pixel) on an 8 data wire interface
- 8-bit YCbCr 4:2:2 serial (1 color per clock input; 2 clocks per displayed pixel) on an 8 data wire interface

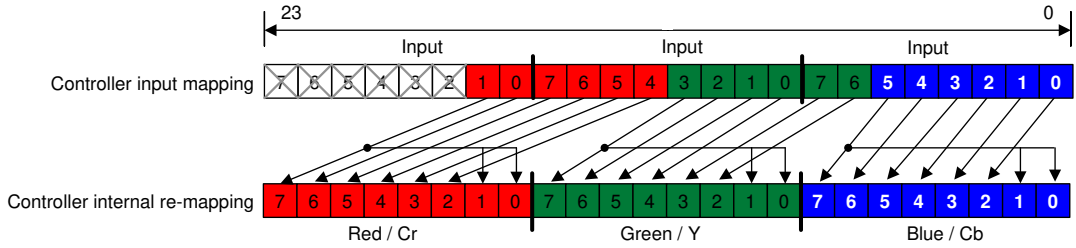
The [セクション 7.3.1.3.1](#) section shows the required PDATA(23:0) bus mapping for these six data transfer formats.



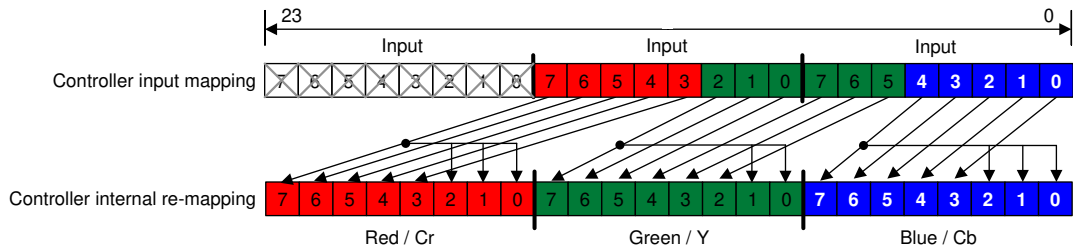
### 7.3.1.3.1 PDATA Bus – Parallel Interface Bit Mapping Modes



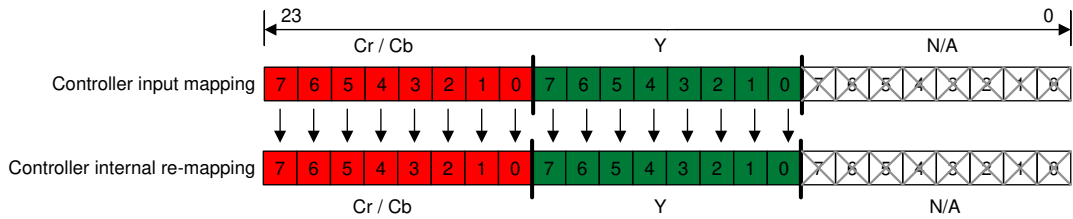
**7-2. RGB-888 and YCbCr-888 I/O Mapping**



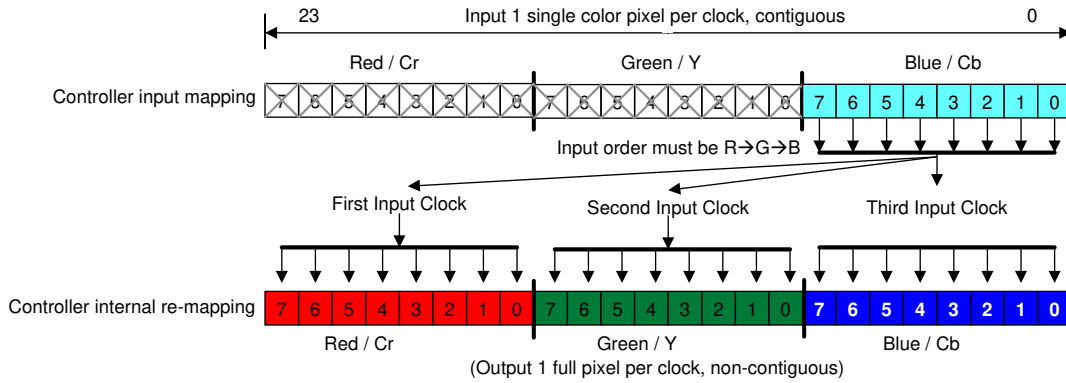
**7-3. RGB-666 and YCbCr-666 I/O Mapping**



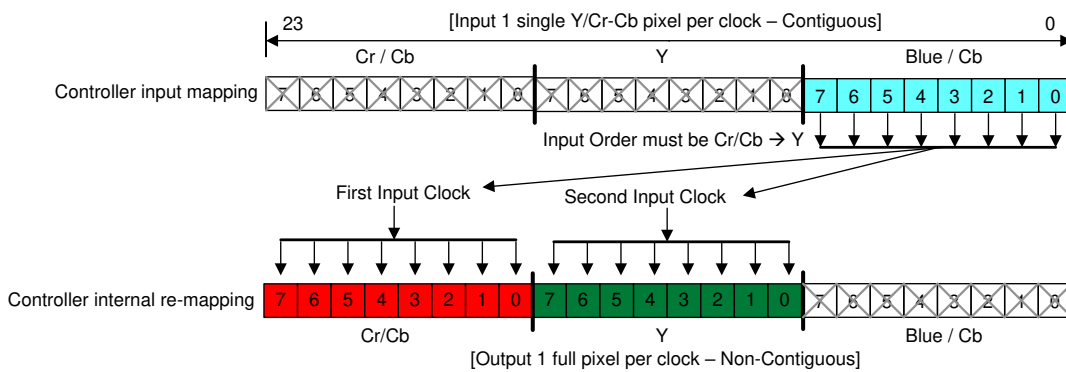
**7-4. RGB-565 and YCbCr-565 I/O Mapping**



**7-5. 16-Bit YCbCr-880 I/O Mapping**



**7-6. 8-Bit RGB-888 or YCbCr-888 I/O Mapping**



**7-7. 8-Bit Serial YCbCr-422 I/O Mapping**

### 7.3.1.4 DSI Interface

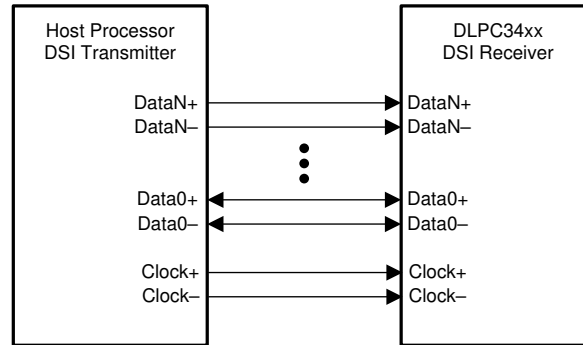
The DLPC34xx controller supports the industry standard DSI (Display Serial Interface) Type-3 LVDS video interface with up to four lanes. DSI is a source-synchronous, high-speed, low-power, low-cost physical layer. The DSI-PHY unit receives data when it operates in high-speed (HS) mode. The DSI-PHY unit receives and transmits data when it operates in low-power (LP) mode for unidirectional data lanes. Point-to-point lane interconnect can be used for either data or clock signal transmission. The high-speed receiver is a differential line receiver circuit. The low-power receiver is an unterminated, single-ended receiver circuit. [Figure 7-8](#) shows a high-level view of the DSI interface.

For a given frame rate, the DSI high-speed (HS) clock frequency must be fixed. If a different DSI clock frequency is ever needed (such as to support another frame rate), an I<sup>2</sup>C command must be sent to the controller with the updated HS clock frequency.

MIPI refers to the Mobile Industry Processor Interface standard.

Various DSI requirements and features of the DLPC34xx are as follows:

- compliant with the DSI-MIPI Specification for Display Serial Interface (V 1.02.00) except for those items noted in the DSI Host Timing Requirements table
- compliant with D-PHY standard MIPI Specification (V 1.0)
- MIPI DSI Type 3 architecture
- supports display resolutions from 320 × 200 to 1280 × 800
- supports video mode (command mode not supported)
- MIPI DCS<sup>SM</sup> (Display Command Set<sup>SM</sup>) commands sent over DSI not supported (send commands via I<sup>2</sup>C instead)
- supports multiple packets per transmission
- supports trigger messages in the forward direction
- data lanes configurable from one to four channels
- EOT (End of Transfer) command is supported and must be enabled
- CRC (cyclic redundancy check) and ECC (error correction code) for header supported
  - CRC and ECC can be disabled
- checksum for long packets with error reporting (but no ECC)
- supports one virtual channel for video mode
- supports burst mode
- supports non-burst with sync pulses and with sync event
- BTA (bus turn-around) mode not supported and must be disabled in the DSI host processor
- LP mode is required during vertical blanking and vertical sync. LP mode is not supported between pixel lines (i.e. HS blanking must be used for horizontal blanking and horizontal sync)
- an active DSI HS clock is required during LP blanking



- one clock lane
- one bi-directional data lane (Data0)
- up to three additional uni-directional data lanes (Data1, Data2, and Data3)

### 7-8. DSI High Level View

The differential DSI clock lane (DCLKN and DCLKP) must be in the LP11 (Idle) state upon the de-assertion of RESETZ (zero-to-one transition) and must remain in this state until HOST\_IRQ is de-asserted (one-to-zero transition) to ensure proper DSI initialization.

The controller requires differential data lane '0' (DD0N:DD0P) for DSI operation. The three remaining data lanes are optional depending on the desired input resolution and frame rate. Not all display resolutions and frame rates are supported without using all four data lanes.

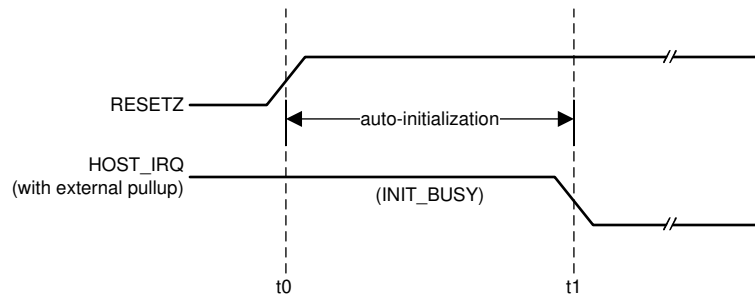
The state of GPIO (2:1) pins upon the de-assertion of RESETZ (zero-to-one transition) determines the number of DSI data lanes that are enabled for both LP and HS bus operation.

DSI supported data transfer formats are as follows:

- 24-bit RGB888 - each pixel uses 3 bytes
- 18-bit RGB666 - each pixel packed into 2 or more bytes
- 18-bit RGB666 - each pixel loosely packed into 3 bytes
- 16-bit RGB565 - each pixel uses 2 bytes
- 16-bit 4:2:2 YCbCr - each pixel uses 2 bytes

### 7.3.2 Device Startup

- The HOST\_IRQ signal is provided to indicate when the system has completed auto-initialization.
- While reset is applied, HOST\_IRQ is tri-stated (an external pullup resistor pulls the line high).
- HOST\_IRQ remains tri-stated (pulled high externally) until the boot process completes. While the signal is pulled high, this indicates that the controller is performing boot-up and auto-initialization.
- As soon as possible after the controller boots-up, the controller drives HOST\_IRQ to a logic high state to indicate that the controller is continuing to perform auto-initialization (no real state changes occur on the external signal).
- The software sets HOST\_IRQ to a logic low state at the completion of the auto-initialization process. At the falling edge of the signal, the initialization is complete.
- The DLPC34xx controller is ready to receive commands through I<sup>2</sup>C or accept video over the DSI or the parallel interface only after auto-initialization is complete.
- The controller initialization typically completes (HOST\_IRQ goes low) within 500 ms of RESETZ being asserted. However, this time may vary depending on the software version and the contents of the user configurable auto initialization file.



t0: rising edge of RESETZ; auto-initialization begins  
t1: falling edge of HOST\_IRQ; auto-initialization is complete

**7-9. HOST\_IRQ Timing**

### 7.3.3 SPI Flash

#### 7.3.3.1 SPI Flash Interface

The DLPC34xx controller requires an external SPI serial flash memory device to store the firmware. Follow the below guidelines and requirements in addition to the requirements listed in the *Flash Interface Timing Requirements* section.

The controller supports a maximum flash size of 128 Mb (16 MB). See the DLPC34xx Validated SPI Flash Device Options table for example compatible flash options. The minimum required flash size depends on the size of the utilized firmware. The firmware size depends upon a variety of factors including the number of sequences, lookup tables, and splash images.

The DLPC34xx controller uses a single SPI interface that complies to industry standard SPI flash protocol. The device will begin accessing the flash at a nominal 1.42-MHz frequency before running at a nominal 30-MHz rate. The flash device must support these rates.

The controller has two independent SPI chip select (CS) control lines. Ensure that the chip select pin of the flash device is connects to SPI0\_CSZ0 as the controller boot routine is executes from the device connected to chip select zero. The boot routine uploads program code from flash memory to program memory then transfers control to an auto-initialization routine within program memory.

The DLPC34xx is designed to support any flash device that is compatible with the modes of operation, features, and performance as defined in the Additional DLPC34xx SPI Flash Requirements table below [表 7-3](#), [表 7-4](#), and [表 7-5](#).

**表 7-3. Additional DLPC34xx SPI Flash Requirements**

| FEATURE   | DLPC34xx REQUIREMENT  |
|---|---|
| SPI interface width   | Single  |
| SPI polarity and phase settings                               | SPI mode 0  |
| Fast READ addressing  | Auto-incrementing   |
| Programming mode  | Page mode   |
| Page size   | 256 B   |
| Sector size   | 4-KB sector   |
| Block size  | Any   |
| Block protection bits   | 0 = Disabled  |
| Status register bit(0)  | Write in progress (WIP), also called flash busy   |
| Status register bit(1)  | Write enable latch (WEN)  |
| Status register bits(6:2)                                     | A value of 0 disables programming protection  |
| Status register bit(7)  | Status register write protect (SRWP)  |
| Status register bits(15:8)<br>(that is expansion status byte) | Because the DLPC34xx controller supports only single-byte status register R/W command execution, it may not be compatible with flash devices that contain an expansion status byte. However, as long as the expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the flash device is likely compatible with the DLPC34xx. |

The DLPC34xx controller is intended to support flash devices with program protection defaults of either enabled or disabled. The controller assumes the default is enabled and proceeds to disable any program protection as part of the boot process.

The DLPC34xx issues these commands during the boot process:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction that writes 0 to all 8 bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC34xx controller issues similar commands:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction

Note that the flash device automatically clears the write enable status after each program and erase instruction.

表 7-4 和 表 7-5 below list the specific instruction OpCode and timing compatibility requirements. The DLPC34xx controller does not adapt protocol or clock rate based on the flash type connected.

**表 7-4. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements**

| SPI FLASH COMMAND    | BYTE 1 (OPCODE) | BYTE 2    | BYTE 3             | BYTE 4    | BYTE 5                 | BYTE 6                 |
|----------------------|-----------------|-----------|--------------------|-----------|------------------------|------------------------|
| Fast READ (1 output) | 0x0B            | ADDRS(0)  | ADDRS(1)           | ADDRS(2)  | dummy                  | DATA(0) <sup>(1)</sup> |
| Read status          | 0x05            | N/A       | N/A                | STATUS(0) |                        |                        |
| Write status         | 0x01            | STATUS(0) | See <sup>(2)</sup> |           |                        |                        |
| Write enable         | 0x06            |           |                    |           |                        |                        |
| Page program         | 0x02            | ADDRS(0)  | ADDRS(1)           | ADDRS(2)  | DATA(0) <sup>(1)</sup> |                        |
| Sector erase (4 KB)  | 0x20            | ADDRS(0)  | ADDRS(1)           | ADDRS(2)  |                        |                        |
| Chip erase           | 0xC7            |           |                    |           |                        |                        |

- (1) Shows the first data byte only. Data continues.  
(2) Access to a second (expansion) write status byte not supported by the DLPC34xx controller.

表 7-5 below and the *Flash Interface Timing Requirements* section list the specific timing compatibility requirements for a DLPC34xx compatible flash device.

**表 7-5. SPI Flash Key Timing Parameter Compatibility Requirements**

| SPI FLASH TIMING PARAMETER <sup>(1) (2)</sup>                 | SYMBOL            | ALTERNATE SYMBOL | MIN   | MAX    | UNIT |
|---|-------------------|------------------|-------|--------|------|
| Access frequency (all commands)                               | FR                | f <sub>C</sub>   | ≤ 1.4 | ≥ 30.1 | MHz  |
| Chip select high time (also called chip select deselect time) | t <sub>SHSL</sub> | t <sub>CSH</sub> | ≤ 200 |        | ns   |
| Output hold time  | t <sub>CLQX</sub> | t <sub>HO</sub>  | ≥ 0   |        | ns   |
| Clock low to output valid time                                | t <sub>CLQV</sub> | t <sub>V</sub>   |       | ≤ 11   | ns   |
| Data in set-up time   | t <sub>DVCH</sub> | t <sub>DSU</sub> | ≤ 5   |        | ns   |
| Data in hold time   | t <sub>CHDX</sub> | t <sub>DH</sub>  | ≤ 5   |        | ns   |

- (1) The timing values apply to the specification of the peripheral flash device, not the DLPC34xx controller. For example, the flash device minimum access frequency (FR) must be 1.4 MHz or less and the maximum access frequency must be 30.1 MHz or greater.  
(2) The DLPC34xx does not drive the  $\overline{\text{HOLD}}$  or  $\overline{\text{WP}}$  (active low write protect) pins on the flash device, and thus these pins must be tied to a logic high on the PCB through an external pullup.

In order for the DLPC34xx controller to support 1.8-V, 2.5-V, or 3.3-V serial flash devices, the VCC\_FLSH pin must be supplied with the corresponding voltage. The DLPC34xx Validated SPI Flash Device Options table contains a list of validated 1.8-V, 2.5-V, or 3.3-V compatible SPI serial flash devices supported by the DLPC34xx controller.

**表 7-6. DLPC34xx Validated SPI Flash Device Options<sup>(1) (2) (3)</sup>**

| DENSITY (Mb)                            | VENDOR   | PART NUMBER       | PACKAGE SIZE         |
|---|----------|-------------------|----------------------|
| <b>1.8-V COMPATIBLE DEVICES</b>         |          |                   |                      |
| 4 Mb                                    | Winbond  | W25Q40BWUXIG      | 2 × 3 mm USON        |
| 4 Mb                                    | Macronix | MX25U4033EBAI-12G | 1.43 × 1.94 mm WLCSP |
| 8 Mb                                    | Macronix | MX25U8033EBAI-12G | 1.68 × 1.99 mm WLCSP |
| <b>2.5- OR 3.3-V COMPATIBLE DEVICES</b> |          |                   |                      |
| 16 Mb                                   | Winbond  | W25Q16CLZPIG      | 5 × 6 mm WSON        |

- (1) The flash supply voltage must equal VCC\_FLSH supply voltage on the DLPC34xx controller. Make sure to order the device that supports the correct supply voltage as multiple voltage options are often available.  
(2) Numonyx (Micron) serial flash devices typically do not support the 4-KB sector size compatibility requirement for the DLPC34xx controller.  
(3) The flash devices in this table have been formally validated by TI. Other flash options may be compatible with the DLPC34xx controller, but they have not been formally validated by TI.

### 7.3.3.2 SPI Flash Programming

The SPI pins of the flash can directly be driven for flash programming while the DLPC34xx controller I/Os are tri-stated. SPI0\_CLK, SPI0\_DOUT, and SPI0\_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the controller. The logic state of the SPI0\_CSZ1 pin is not affected by this action. Alternatively, the DLPC34xx controller can program the SPI flash itself when commanded via I<sup>2</sup>C if a valid firmware image has already been loaded and the controller is operational.

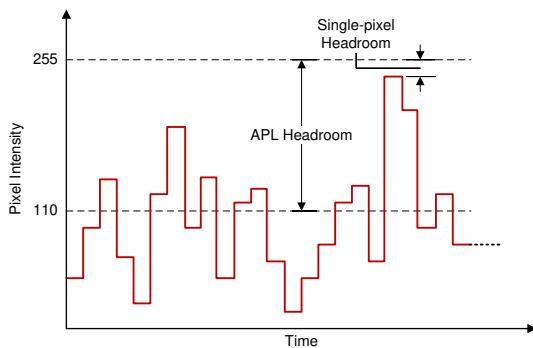
### 7.3.4 I<sup>2</sup>C Interface

Both of the DLPC34xx I<sup>2</sup>C interface ports support a 100-kHz baud rate. Because I<sup>2</sup>C interface transactions operate at the speed of the slowest device on the bus, there is no requirement to match the speed of all devices in the system.

### 7.3.5 Content Adaptive Illumination Control (CAIC)

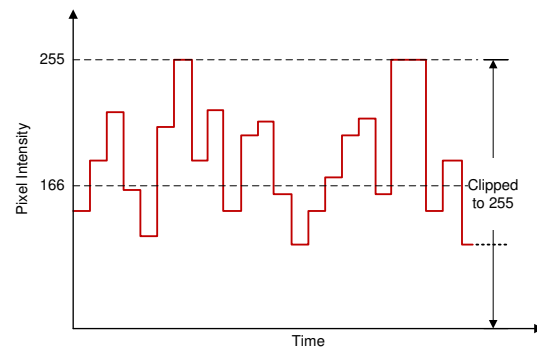
Content Adaptive Illumination control (CAIC) is part of the IntelliBright® suite of advanced image processing algorithms that adaptively enhances brightness and reduces power. In common real-world image content most pixels in the images are well below full scale for the R (red), G (green), and B (blue) digital channels input to the DLPC34xx. As a result of this, the average picture level (APL) for the overall image is also well below full scale, and the dynamic range for the collective set of pixel values is not fully used. CAIC takes advantage of the headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images on a frame-by-frame basis and derives three unique digital gains, one for each of the R, G, and B color channel. During image processing, CAIC applies each gain to all pixels in the associated color channel. The calculated gain is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. The [Source Pixels for a Color Channel](#) and [Pixels for a Color Channel After CAIC Processing](#) figures below show an example of the application of CAIC for one color channel.



(1) APL = 110

☒ 7-10. Source Pixels for a Color Channel



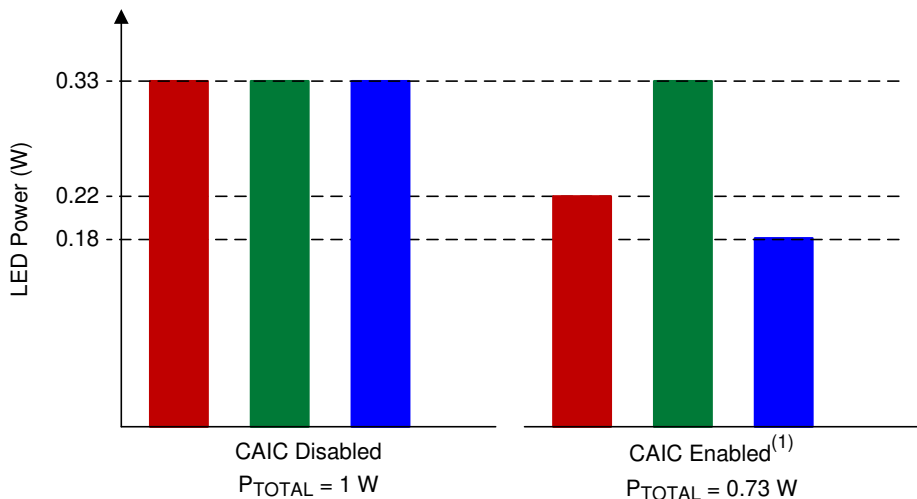
(1) APL = 166

(2) Channel gain =  $166/110 = 1.51$

☒ 7-11. Pixels for a Color Channel After CAIC Processing

Above, ☒ 7-11 shows the gain that is applied to a color processing channel inside the DLPC34xx. Additionally, CAIC adjusts the power for the R, G, and B LED by commanding different LED currents. For each color channel of an individual frame, CAIC intelligently determines the optimal combination of digital gain and LED power. The user configurable CAIC settings heavily influence the amount of digital gain that is applied to a color channel and the LED power for that color.





(1) With CAIC enabled, if red and blue LEDs require less than nominal power for a given input image, the red and blue LED power will reduce.

### 7-12. CAIC Power Reduction Mode (for Constant Brightness)

As CAIC applies a digital gain to each color channel and adjusts the power to each LED, CAIC ensures the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

CAIC can be used to increase the overall image brightness while holding the total power for all LEDs constant, or CAIC can be used to hold the overall image brightness constant while decreasing LED power. In summary, CAIC has two primary modes of operation:

- Power reduction mode holds overall image brightness constant while reducing LED power
- Enhanced brightness mode holds overall LED power constant while enhancing image brightness

In power reduction mode, since the R, G, and B channels can be gained up by CAIC inside the DLPC34xx, the LED power can be reduced for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. 7-12 shows an example of LED power reduction by CAIC for an image where the red and blue LEDs can consume less power.

In enhanced brightness mode the R, G, and B channels can be gained up by CAIC with LED power generally being held constant. This results in an enhanced brightness with no power savings.

While there are two primary modes of operation described, the DLPC34xx actually operates within the extremes of pure power reduction mode and enhanced brightness mode. The user can configure which operating mode the DLPC34xx will more closely follow by adjusting the CAIC gain setting as described in the software programmer's guide.

In addition to the above functionality, CAIC also can be used as a tool with which FOFO (full-on full-off) contrast on a projection system can be improved. While operating in power reduction mode, the DLPC34xx reduces LED power as the intensity of the image content for each color channel decreases. This will result in the LEDs operating at nominal settings with full-on content (a white screen) and reducing power output until the dimmest possible content (a black screen) is reached. In this latter case, the LEDs will be operating at minimum power output capacity and thus producing the minimum possible amount of off-state light. This optimization provided by CAIC will thereby improve FOFO contrast ratio. The given contrast ratio will further increase as nominal LED current (full-on state) is increased.

### 7.3.6 Local Area Brightness Boost (LABB)

Local area brightness boost (LABB), part of the IntelliBright™ suite of advanced image processing algorithms, adaptively gains up regions of an image that are dim relative to the average picture level. The controller applies significant gain to some regions of the image, and applies little or no gain to other regions. The LABB algorithm evaluates images frame-by-frame and calculates the local area gains to be used for each image. Since many images have a net overall boost in gain, even if the controller applies no gain to some parts of the image, the controller boosts the overall perceived brightness of the image.

☒ 7-13 below shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.



☒ 7-13. LABB enabled (left side) and LABB disabled (right side)

The LABB algorithm operates most effectively when ambient light conditions are used to help determine the decision about the strength of gains utilized. For this reason, it may be useful to include an ambient light sensor in the system design that is used to measure the display screen's reflected ambient light. This sensor can assist in dynamically controlling the LABB strength. Set the LABB gain higher for bright rooms to help overcome washed out images. Set the LABB gain lower in dark rooms to prevent overdriven pixel intensities in images.

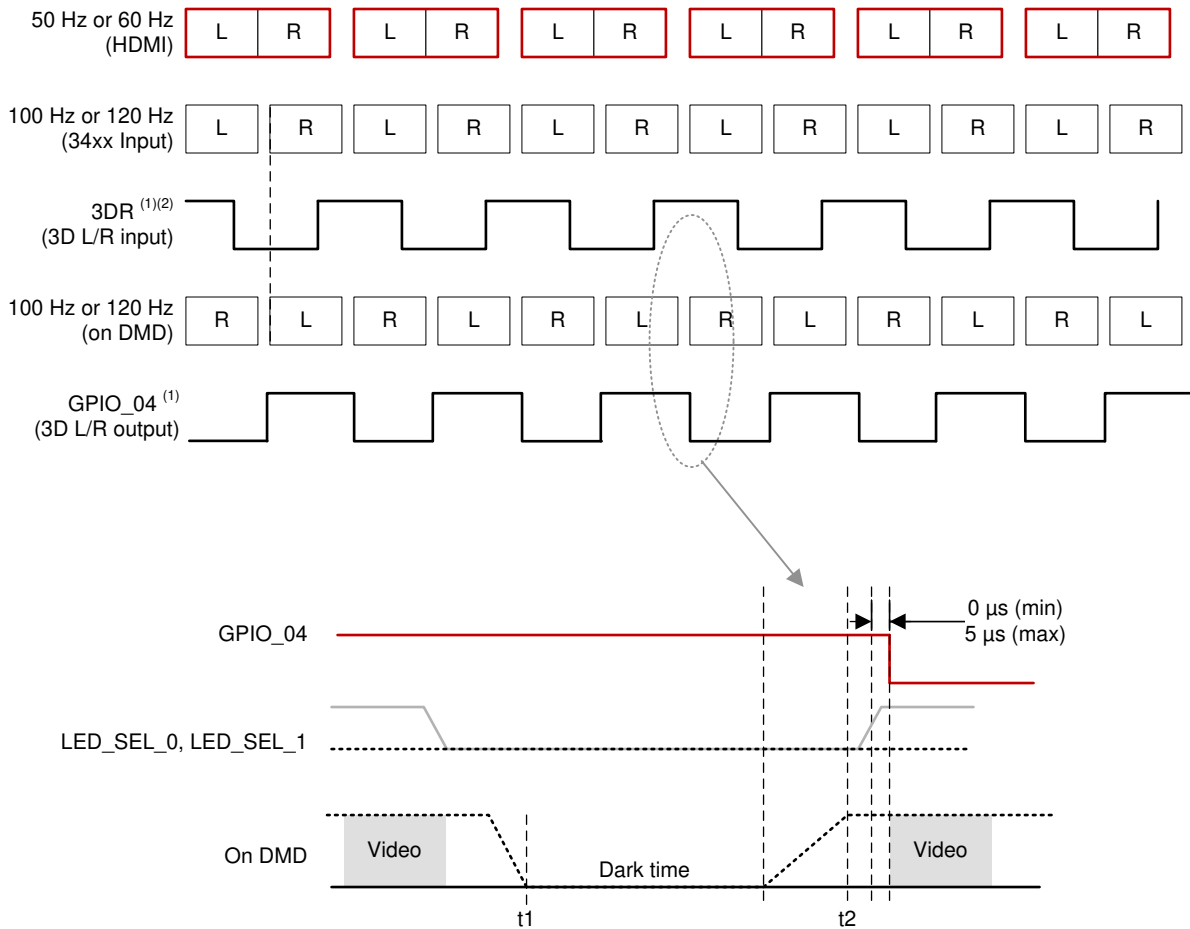
### 7.3.7 3D Glasses Operation

When using 3D glasses (with 3D video input and appropriate software support), the controller outputs sync information to align the left eye and right eye shuttering in the glasses with the displayed DMD image frames. 3D glasses typically use either Infrared (IR) transmission or DLP Link™ technology to achieve this synchronization.

One glasses type uses an IR transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case DLPC34xx controller output signal GPIO\_04 can be used to cause the IR transmitter to send an IR sync signal to the glasses. The ☒ 7-14 figure shows the timing sequence for the GPIO\_04 signal.

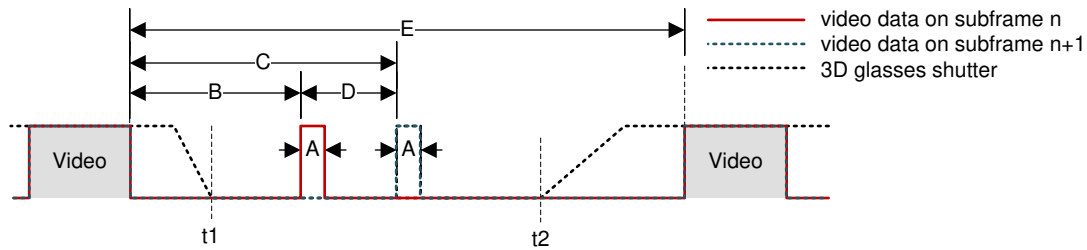
The second type of glasses relies on sync information that is encoded into the light being output from the projection lens. This approach uses the DLP Link feature for 3D video. Many 3D glasses from different suppliers have been built using this method. The advantage of using the DLP Link feature is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This method may give an advantage in cost, size and power savings in the projector.

When using DLP Link technology, one light pulse per DMD frame is output from the projection lens while the glasses have both shutters closed. To achieve this, the DLPC34xx tells the DLPxxxx when to turn on the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Because the shutters in the glasses are both off when the pulse is sent, the projector illumination source is also off except when the light is sent to create the pulse. The pulses may use any color; however, due to the transmission property of the eye-glass LCD shutter lenses and the sensitivity of the white-light sensor used on the eye-glasses, it is highly recommended that blue is not used for pulses. Red pulses are the recommended color to use. The [Figure 7-14](#) below shows 3D timing information. [Figure 7-15](#) and [Table 7-7](#) show the timing for the light pulses when using the DLP Link feature.



- (1) Left = 1, Right = 0
- (2) 3DR must toggle 1 ms before VSYNC
- t1: both shutters turned off
- t2: next shutter turned on

**Figure 7-14. 3D Display Left and Right Frame and Signal Timing**



The time offset of DLP Link pulses at the end of a subframe alternates between B and B+D where D is the delta offset.

图 7-15. 3D DLP Link Pulse Timing

表 7-7. 3D DLP Link Timing

| HDMI Source Frame Rate (Hz) <sup>(1)</sup> | DLPC34xx Input Frame Rate (Hz) | A (μs)                    | B (μs) | C (μs) | D (μs)                       | E (μs) |
|--|--------------------------------|---------------------------|--------|--------|------------------------------|--------|
| 49.0                                       | 98                             | 20 - 32<br>(31.8 nominal) | > 500  | > 622  | 128 - 163<br>(161.6 nominal) | > 2000 |
| 50.0                                       | 100                            | 20 - 32<br>(31.2 nominal) | > 500  | > 658  | 128 - 163<br>(158.4 nominal) | > 2000 |
| 51.0                                       | 102                            | 20 - 32<br>(30.6 nominal) | > 500  | > 655  | 128 - 163<br>(155.3 nominal) | > 2000 |
| 59.0                                       | 118                            | 20 - 32<br>(26.4 nominal) | > 500  | > 634  | 128 - 163<br>(134.2 nominal) | > 2000 |
| 60.0                                       | 120                            | 20 - 32<br>(26.0 nominal) | > 500  | > 632  | 128 - 163<br>(132.0 nominal) | > 2000 |
| 61.0                                       | 122                            | 20 - 32<br>(25.6 nominal) | > 500  | > 630  | 128 - 163<br>(129.8 nominal) | > 2000 |

(1) Timing parameter C is always the sum of B+D.

### 7.3.8 Test Point Support

The DLPC34xx test point output port, TSTPT\_(7:0), provides selected system calibration and controller debug support. These test points are inputs when reset is applied. These test points are outputs when reset is released. The controller samples the signal state upon the release of system reset and then uses the captured value to configure the test mode until the next time reset is applied. Because each test point includes an internal pulldown resistor, external pullups must be used to modify the default test configuration.

The default configuration (b000) corresponds to the TSTPT\_(2:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, a jumper to external pullup resistors is recommended for TSTPT\_(2:0). The pullup resistors on TSTPT\_(2:0) can be used to configure the controller for a specific mode or option. TI does not recommend adding pullup resistors to TSTPT\_(7:3) due to potentially adverse effects on normal operation. For normal use TSTPT\_(7:3) should be left unconnected. The test points are sampled only during a 0-to-1 transition on the RESETZ input, so changing the configuration after reset is released does not have any effect until the next time reset asserts and releases. 表 7-8 describes the test mode selections for one programmable scenario defined by TSTPT\_(2:0).

**表 7-8. Test Mode Selection Scenario Defined by TSTPT\_(2:0)**

| TSTPT OUTPUT VALUE <sup>(1)</sup> | NO SWITCHING ACTIVITY | CLOCK DEBUG OUTPUT  |
|-----------------------------------|-----------------------|---------------------|
|                                   | TSTPT_(2:0) = 0b000   | TSTPT_(2:0) = 0b010 |
| TSTPT_0                           | HI-Z                  | 60 MHz              |
| TSTPT_1                           | HI-Z                  | 30 MHz              |
| TSTPT_2                           | HI-Z                  | 0.7 to 22.5 MHz     |
| TSTPT_3                           | HI-Z                  | HIGH                |
| TSTPT_4                           | HI-Z                  | LOW                 |
| TSTPT_5                           | HI-Z                  | HIGH                |
| TSTPT_6                           | HI-Z                  | HIGH                |
| TSTPT_7                           | HI-Z                  | 7.5 MHz             |

(1) These are default output selections. Software can reprogram the selection at any time.

### 7.3.9 DMD Interface

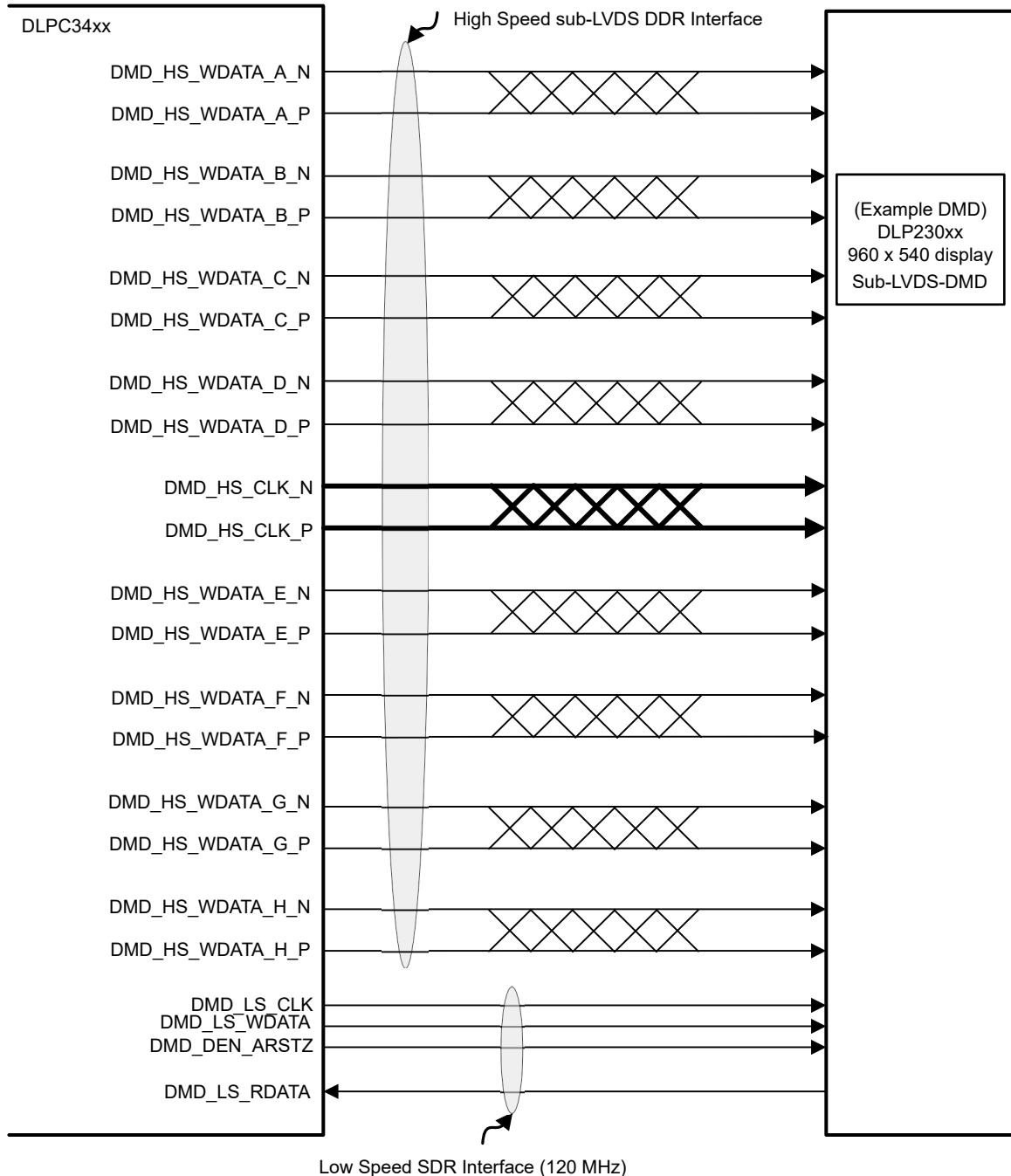
The DLPC34xx controller DMD interface consists of one high-speed (HS), 1.8-V sub-LVDS, output-only interface and one low speed (LS), 1.8-V LVCMOS SDR interface with a typical fixed clock speed of 120 MHz.

#### 7.3.9.1 Sub-LVDS (HS) Interface

Internal software selection allows the controller to support multiple DMD interface swap configurations. These options can improve board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. 表 7-9 shows the two options available for the DLP230GP DMD.

**表 7-9. DLP230GP (.23 qHD) DMD – Controller to 8-Lane DMD Pin Mapping Options**

| DLPC3432 Controller 8 LANE DMD ROUTING OPTIONS |                              | DMD PINS                         |
|--|------------------------------|----------------------------------|
| OPTION 1                                       | OPTION 2                     |                                  |
| HS_WDATA_D_P<br>HS_WDATA_D_N                   | HS_WDATA_E_P<br>HS_WDATA_E_N | Input DATA_p_0<br>Input DATA_n_0 |
| HS_WDATA_C_P<br>HS_WDATA_C_N                   | HS_WDATA_F_P<br>HS_WDATA_F_N | Input DATA_p_1<br>Input DATA_n_1 |
| HS_WDATA_B_P<br>HS_WDATA_B_N                   | HS_WDATA_G_P<br>HS_WDATA_G_N | Input DATA_p_2<br>Input DATA_n_2 |
| HS_WDATA_A_P<br>HS_WDATA_A_N                   | HS_WDATA_H_P<br>HS_WDATA_H_N | Input DATA_p_3<br>Input DATA_n_3 |
| HS_WDATA_H_P<br>HS_WDATA_H_N                   | HS_WDATA_A_P<br>HS_WDATA_A_N | Input DATA_p_4<br>Input DATA_n_4 |
| HS_WDATA_G_P<br>HS_WDATA_G_N                   | HS_WDATA_B_P<br>HS_WDATA_B_N | Input DATA_p_5<br>Input DATA_n_5 |
| HS_WDATA_F_P<br>HS_WDATA_F_N                   | HS_WDATA_C_P<br>HS_WDATA_C_N | Input DATA_p_6<br>Input DATA_n_6 |
| HS_WDATA_E_P<br>HS_WDATA_E_N                   | HS_WDATA_D_P<br>HS_WDATA_D_N | Input DATA_p_7<br>Input DATA_n_7 |



**Figure 7-16. DLP230GP (.23 qHD) DMD Interface Example**

The sub-LVDS high-speed interface waveform quality and timing on the DLPC34xx controller depends on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the *DMD Control and Sub-LVDS Signals* layout section is provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB signal integrity). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

## 7.4 Device Functional Modes

The DLPC34xx controller has two functional modes (ON and OFF) controlled by a single pin, PROJ\_ON (GPIO\_08).

- When the PROJ\_ON pin is set high, the controller powers up and can be programmed to send data to the DMD.
- When the PROJ\_ON pin is set low, the controller powers down and consumes minimal power.

## 7.5 Programming

The DLPC34xx controller contains an Arm® Cortex®-M3 processor with additional functional blocks to enable video processing and control. TI provides software as a firmware image. The customer is required to flash this firmware image onto the SPI flash memory. The DLPC34xx controller loads this firmware during startup and regular operation. The controller and its accompanying DLP chipset requires this proprietary software to operate. The available controller functions depend on the firmware version installed. Different firmware is required for different chipset combinations (such as when using different PMIC devices). See *Documentation Support* at the end of this document or contact TI to view or download the latest published software.

Users can modify software behavior through I<sup>2</sup>C interface commands. For a list of commands, view the software user's guide accessible through the *Documentation Support* page.



## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

The DLPC34xx controller is used with the DLP230GP DMD to provide a reliable display solution for many data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into projection or collection optics. The optical architecture of the system and the format of the image digital data coming into the DLPC34xx are what primarily determine the application requirements.

Click these links to find more information about typical applications:

[Mobile projector](#), [Smart display](#), [Smartphone](#), [Tablet \(multimedia\)](#), [Augmented reality glasses](#), [Smart home display](#), or [Pico projector](#).

### 8.2 Typical Application

A common application when using the DLPC34xx controller with the DLP230GP DMD and the DLPAxxxx PMIC/LED driver is to create a pico projector embedded in a handheld product. For example, a pico projector may be embedded in a smartphone, a tablet, or a camera. The controller in the pico projector embedded module typically receives images from a host processor within the product.

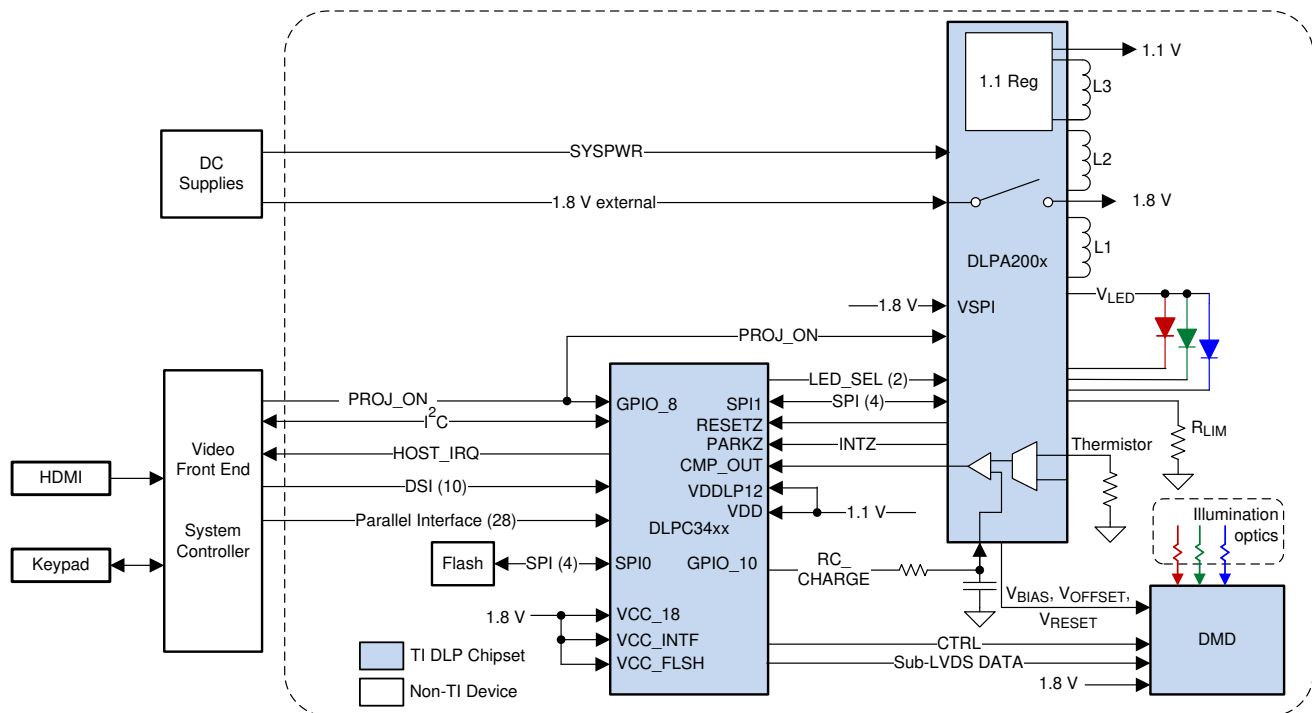
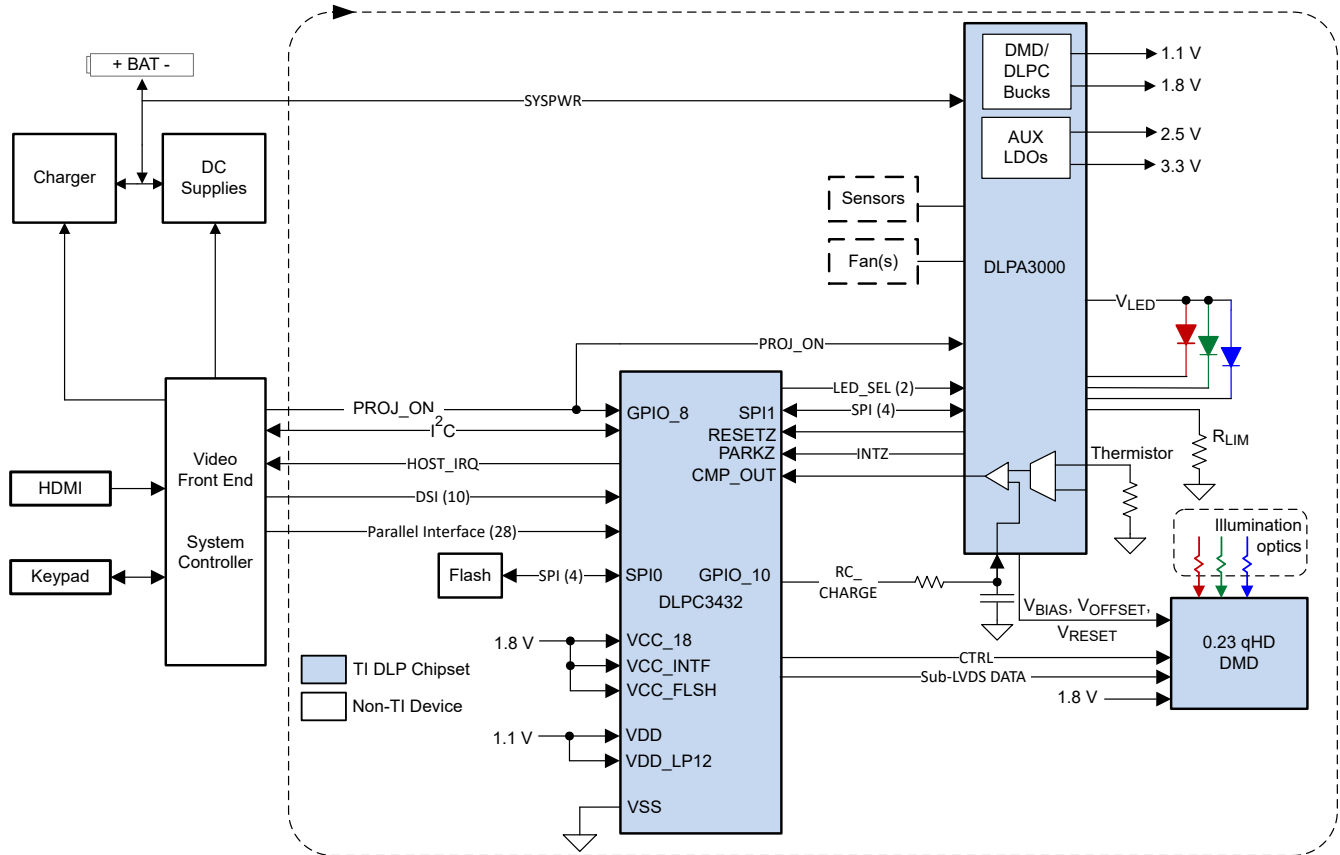


図 8-1. Typical Simplified Application Schematic (using DLPA200x)



8-2. Typical Simplified Application Schematic (using DLPA3000)

### 8.2.1 Design Requirements

A pico projector can be created by using the DLP chipset that includes the DLP230GP (.23 qHD) DMD, the DLPC34xx controller, and the DLPAxxxx PMIC/LED driver. The DLPC34xx controller processes the digital images, the DLPAxxxx PMIC provides the analog functions for the chipset, and the DMD displays the image for projection.

In addition to the three DLP devices in the chipset, other components may be needed. At a minimum, a flash device is needed to store the firmware that controls the DLPC34xx controller.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These LEDs are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico projector.

To receive images, connect the DLPC34xx controller to the host processor using the parallel (or potentially DSI) interface. To send commands to the controller, connect it to the host processor using the I<sup>2</sup>C interface.

The only required power supplies that are external to the projector system chipset are the battery (SYSPWR) and possibly a regulated 1.8-V supply (some TI PMICs generate the 1.8-V supply but the DLPA200x does not).

The entire projector chipset can be turned on and off by using a single signal called PROJ\_ON. When PROJ\_ON is high, the chipset turns on and can begin displaying images. When PROJ\_ON is set low, the projector chipset turns off and draws just microamps of current on SYSPWR. If 1.8 V is supplied separately from the PMIC (as is the case with the DLPA200x), when PROJ\_ON is set low, the 1.8-V supply can continue to be left at 1.8 V and used by other non-projector sections of the product.

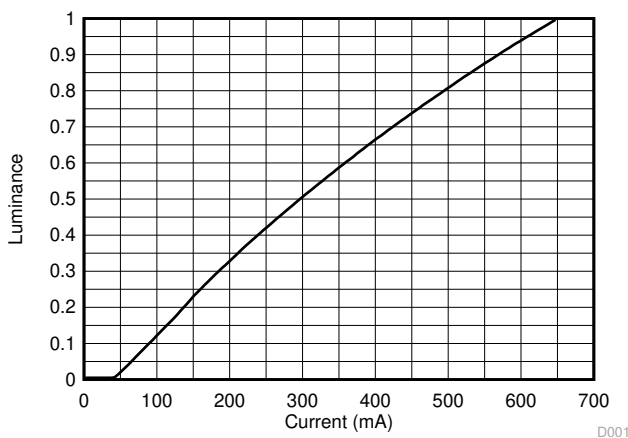
### 8.2.2 Detailed Design Procedure

For connecting the DLP230GP (.23 qHD) DMD, DLPC34xx controller, and DLPAxxxx PMIC, see the reference design schematic and board layout [TIDA-080002](#). When a circuit board layout is created from this schematic, a small circuit board is possible. Follow the layout guidelines to design a reliable projector.

It is typical for an optical engine manufacturer to supply the optical engine that includes the LED packages and a mounted DMD. These manufacturers specialize in designing optics for DLP projectors. There exists [production-ready optical modules](#), [optical module manufacturers](#), and [design houses](#).

### 8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in [Figure 8-3](#). For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs. The shape of the curve depends on the LED devices used as well as the LED system-level heat sink implementation.



**Figure 8-3. Typical Luminance vs Current**

## 9 Power Supply Recommendations

### 9.1 PLL Design Considerations

It is acceptable for the VDD\_PLLD and VDD\_PLLM to be derived from the same regulator as the core VDD. However, to minimize the AC noise component, apply a filter as recommended in the *PLL Power Layout* section.

### 9.2 System Power-Up and Power-Down Sequence

Although the DLPC34xx controller requires an array of power supply voltage pins (for example, VDD, VDDL12, VDD\_PLLM/D, VCC18, VCC\_FLSH, and VCC\_INTF), if VDDL12 is tied to the 1.1-V VDD supply (which is assumed to be the typical configuration), then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC34xx controller (this remains true for both power-up and power-down scenarios). The controller requires no minimum delay time between powering-up and powering-down the individual supplies if the VDDL12 is tied to the 1.1-V VDD supply.

However, if the VDDL12 pin is not tied to the VDD supply, then the VDDL12 pin must be powered-on only after the VDD supply is powered-on. And in a similar sequence, the VDDL12 pin must be powered-off before the VDD supply is powered-off. If the VDDL12 pin is not tied to VDD, then the VDDL12 pin and VDD supply pins must be powered-on or powered-off within 100 ms of each other.

Although there is no risk of damaging the DLPC34xx controller when the above power sequencing rules are followed, these additional power sequencing recommendations must be considered to ensure proper system operation:

- To ensure that the DLPC34xx controller output signal states behave as expected, all controller I/O supplies are encouraged to remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC\_INTF) is applied, then the output signal states associated with the inactive I/O supply go to a high impedance state.
- Because additional power sequencing rules may exist for devices that share the supplies with the DLPC34xx controller (such as the PMIC and DMD), these devices may force additional system power sequencing requirements.

[☒ 9-1](#), [☒ 9-2](#), and [☒ 9-3](#) show the DLPC34xx power-up sequence, the normal PARK power-down sequence, and the fast PARK power-down sequence of a typical DLPC34xx system.

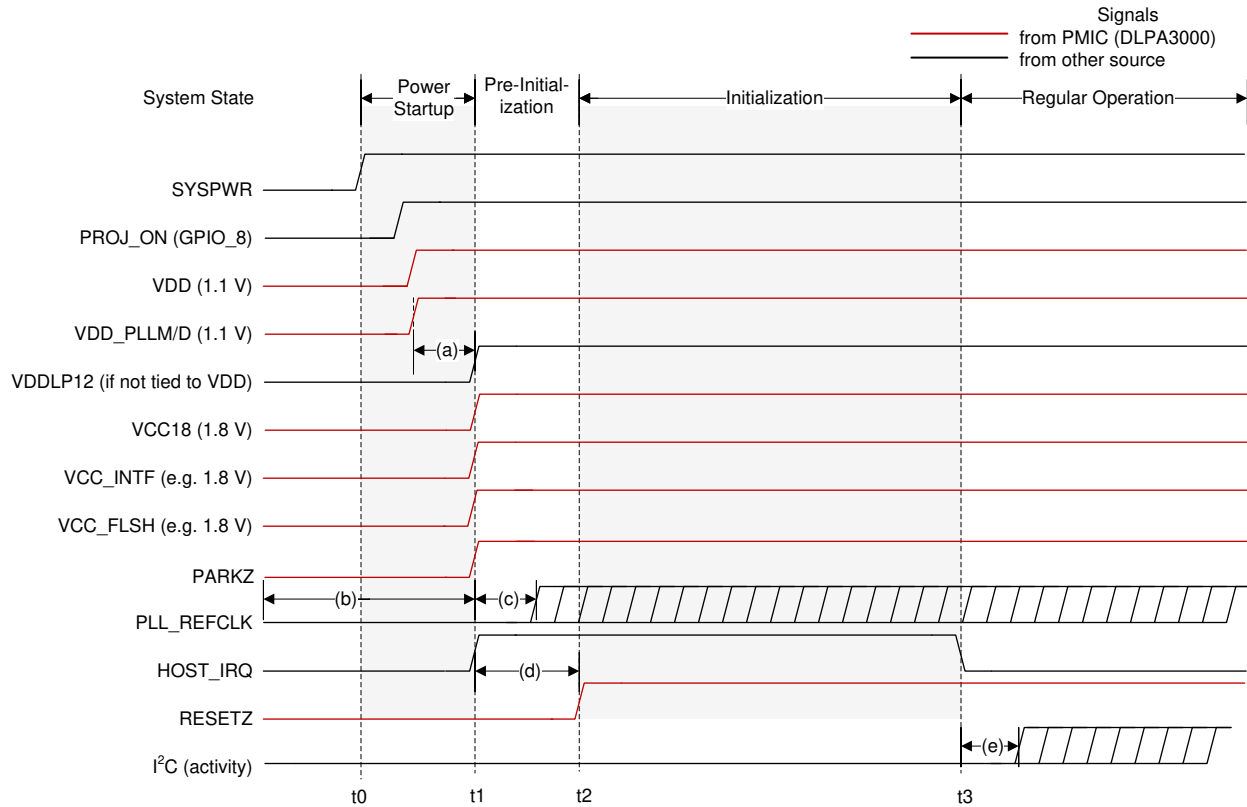
When the VDD core power is applied, but I/O power is not applied, the controller may draw additional leakage current. This leakage current does not affect the normal DLPC34xx controller operation or reliability.

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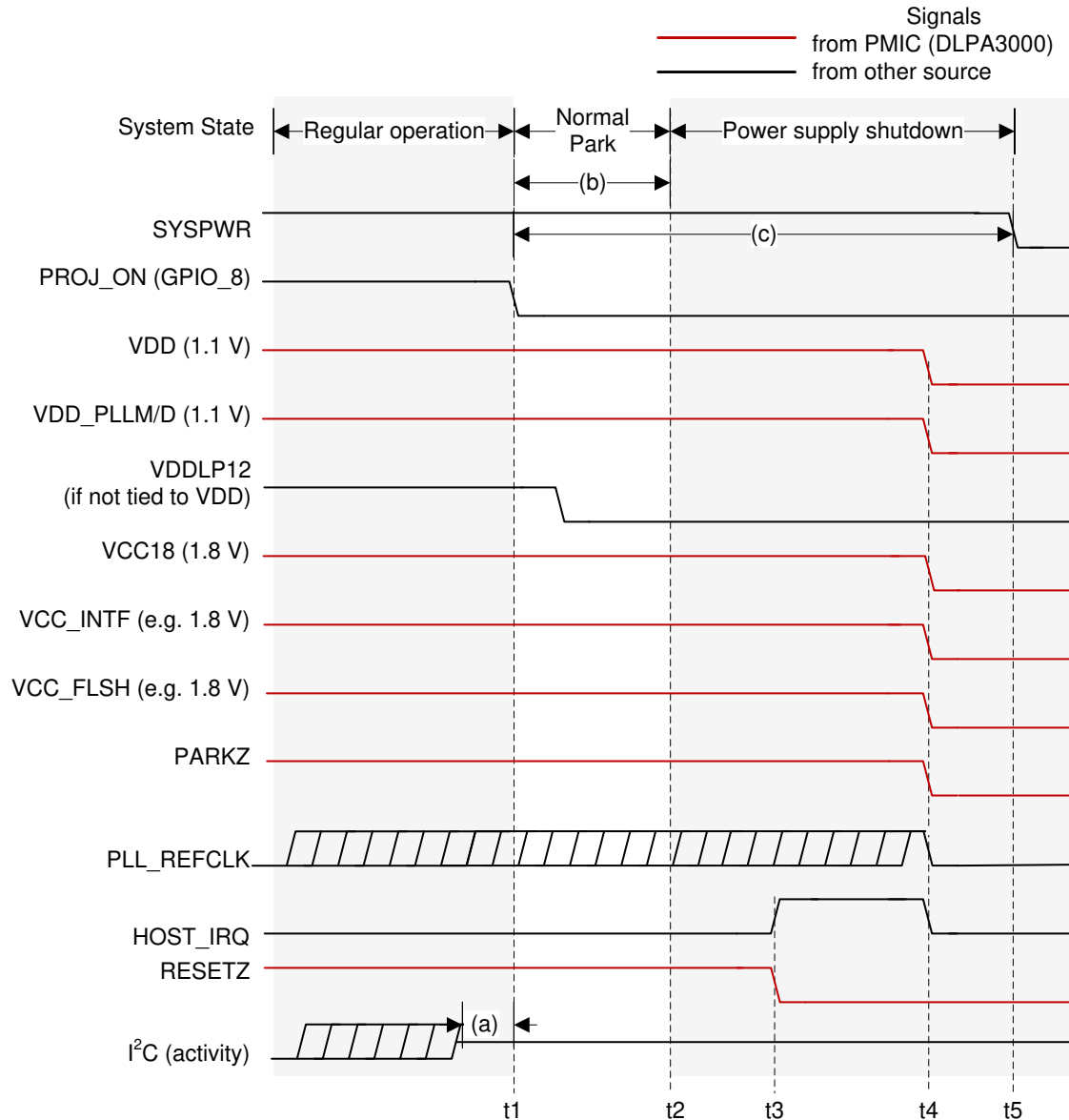
#### 注

During a Normal Park it is recommended to maintain SYSPWR within specification for at least 50 ms after PROJ\_ON goes low. This is to allow the DMD to be parked and the power supply rails to safely power down. After 50 ms, SYSPWR can be turned off. If a DLPA200x is used, it is also recommended that the 1.8-V supply fed into the DLPA200x load switch be maintained within specification for at least 50 ms after PROJ\_ON goes low.

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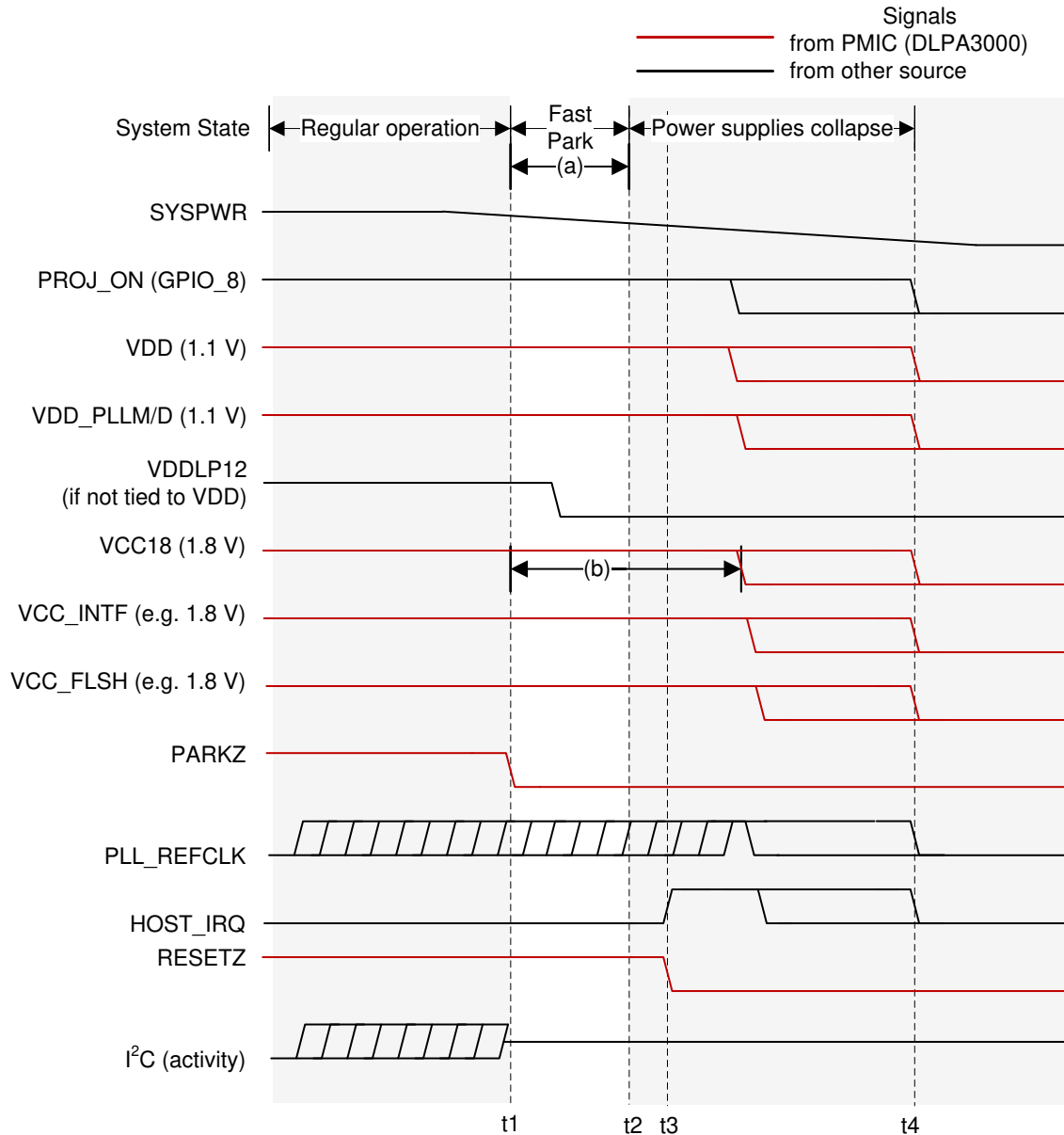



**9-1. System Power-Up Waveforms (With DLPA3000)**



- t1: PROJ\_ON goes low to begin the power down sequence.
- t2: The controller finishes parking the DMD.
- t3: RESETZ is asserted which causes HOST\_IRQ to be pulled high.
- t4: All controller power supplies are turned off.
- t5: SYSPWR is removed now that all other supplies are turned off.
- (a): I<sup>2</sup>C activity must stop before PROJ\_ON is deasserted (goes low).
- (b): The DMD will be parked within 20 ms of PROJ\_ON being deasserted (going low). VDD, VDD\_PLLM/D, VCC18, VCC\_INITF, and VCC\_FLSH power supplies and the PLL\_REFCLK must be held within specification for a minimum of 20 ms after PROJ\_ON is deasserted (goes low). However, 20 ms does not satisfy the typical shutdown timing of the entire chipset. It is therefore recommended to follow note (c).
- (c): It is recommended that SYSPWR not be turned off for 50 ms after PROJ\_ON is deasserted (goes low). This time allows the DMD to be parked, the controller to turn off, and the PMIC supplies to shut down.

## 9-2. Normal Park Power-Down Waveforms



- t1: A fault is detected (in this example the PMIC detects a UVLO condition) and PARKZ is asserted (goes low) to tell the controller to initiate a fast park of the DMD.
- t2: The controller finishes the fast park procedure.
- t3: RESETZ is asserted which puts the controller in a reset state which causes HOST\_IRQ to be pulled high.
- t4: Eventually all power supplies that were derived from SYSPWR collapse.
- (a): VDD, VDD\_PLLM/D, VCC18, VCC\_INITF, and VCC\_FLSH power supplies and the PLL\_REFCLK must be held within specification for a minimum of 32  $\mu$ s after PARKZ is asserted (goes low).
- (b): VCC18 must remain in specification long enough to satisfy DMD power sequencing requirements defined in the DMD datasheet. Also see the DLPxxxx datasheets for more information.

### 9-3. Fast Park Power-Down Waveforms

### 9.3 Power-Up Initialization Sequence

An external power monitor is required to hold the DLPC34xx controller in system reset during the power-up sequence by driving RESETZ to a logic-low state. It shall continue to drive RESETZ low until all controller voltages reach the minimum specified voltage levels, PARKZ goes high, and the input clocks are stable. The external power monitoring is automatically done by the DLPAXxxx PMIC.

No signals output by the DLPC34xx controller will be in their active state while RESETZ is asserted. The following signals are tri-stated while RESETZ is asserted:

- SPI0\_CLK
- SPI0\_DOUT
- SPI0\_CSZ0
- SPI0\_CSZ1
- GPIO [19:00]

Add external pullup (or pulldown) resistors to all tri-stated output signals (including bidirectional signals to be configured as outputs) to avoid floating controller outputs during reset if they are connected to devices on the PCB that can malfunction. For SPI, at a minimum, include a pullup to any chip selects connected to devices. Unused bidirectional signals can be configured as outputs in order to avoid floating controller inputs after RESETZ is set high.

The following signals are forced to a logic low state while RESETZ is asserted and the corresponding I/O power is applied:

- LED\_SEL\_0
- LED\_SEL\_1
- DMD\_DEN\_ARSTZ

After power is stable and the PLL\_REFCLK\_I clock input to the DLPC34xx controller is stable, then RESETZ should be deactivated (set to a logic high). The DLPC34xx controller then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ, all DLPC34xx I/Os will become active. Immediately following the release of RESETZ, the HOST\_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST\_IRQ, this signal will have already gone high before the controller actively drives it high. Upon completion of the auto-initialization routine, the DLPC34xx controller will drive HOST\_IRQ low to indicate the initialization done state of the controller has been reached.

To ensure reliable operation, during the power-up initialization sequence, GPIO\_08 (PROJ\_ON) must not be deasserted. In other words, once the startup routine has begun (by asserting PROJ\_ON), the startup routine must complete (indicated by HOST\_IRQ going low) before the controller can be commanded off (by deasserting PROJ\_ON).

---

#### 注

No I<sup>2</sup>C or DSI (if applicable) activity is permitted until HOST\_IRQ goes low.

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## 9.4 DMD Fast Park Control (PARKZ)

PARKZ is an input early warning signal that must alert the controller at least 32  $\mu$ s before DC supply voltages drop below specifications. Typically, the PARKZ signal is provided by the DLPxxxx interrupt output signal. PARKZ must be deasserted (set high) prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input) for normal operation. When PARKZ is asserted (set low) the controller performs a Fast Park operation on the DMD which assists in maintaining the lifetime of the DMD. The reference clock must continue running and RESETZ must remain deactivated for at least 32  $\mu$ s after PARKZ has been asserted (set low) to allow the park operation to complete.

Fast Park operation is only intended for use when loss of power is imminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with Fast Park operation. The longest lifetime is achieved with a Normal Park operation (initiated through GPIO\_08). Hence, PARKZ is typically only used instead of a Normal Park request if there is not enough time for a Normal Park. A Normal Park operation takes much longer than 32  $\mu$ s to park the mirrors. During a Normal Park operation, the DLPxxxx keeps on all power supplies, and keeps RESETZ high, until the longer mirror parking has completed. Additionally, the DLPxxxx may hold the supplies on for a period of time after the parking has been completed. View the relevant DLPxxxx datasheet for more information. The longer mirror parking time ensures the longest DMD lifetime and reliability. The *DMD Parking Switching Characteristics* section specifies the park timings.

## 9.5 Hot Plug I/O Usage

The DLPC34xx controller provides fail-safe I/O on all host interface signals (signals powered by VCC\_INTF). This allows these inputs to externally be driven even when no I/O power is applied. Under this condition, the controller does not load the input signal nor draw excessive current that could degrade controller reliability. For example, the I<sup>2</sup>C bus from the host to other components is not affected by powering off VCC\_INTF to the DLPC34xx controller. This allows additional devices on the I<sup>2</sup>C bus to be utilized even if the controller is not powered on. TI recommends weak pullup or pulldown resistors to avoid floating inputs for signals that feed back to the host.

If the I/O supply (VCC\_INTF) powers off, but the core supply (VDD) remains on, then the corresponding input buffer may experience added leakage current; however, the added leakage current does not damage the DLPC34xx controller.

However, if VCC\_INTF is powered and VDD is not powered, the controller may drive the IIC0\_xx pins low which prevents communication on this I<sup>2</sup>C bus. Do not power up the VCC\_INTF pin before powering up the VDD pin for any system that has additional secondary devices on this bus.

## 10 Layout

### 10.1 Layout Guidelines

For a summary of the PCB design requirements for the DLPC34xx controller see [PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices](#). Some applications (such as high frame rate video) may require the use of 1-oz (or greater) copper planes to manage the controller package heat.

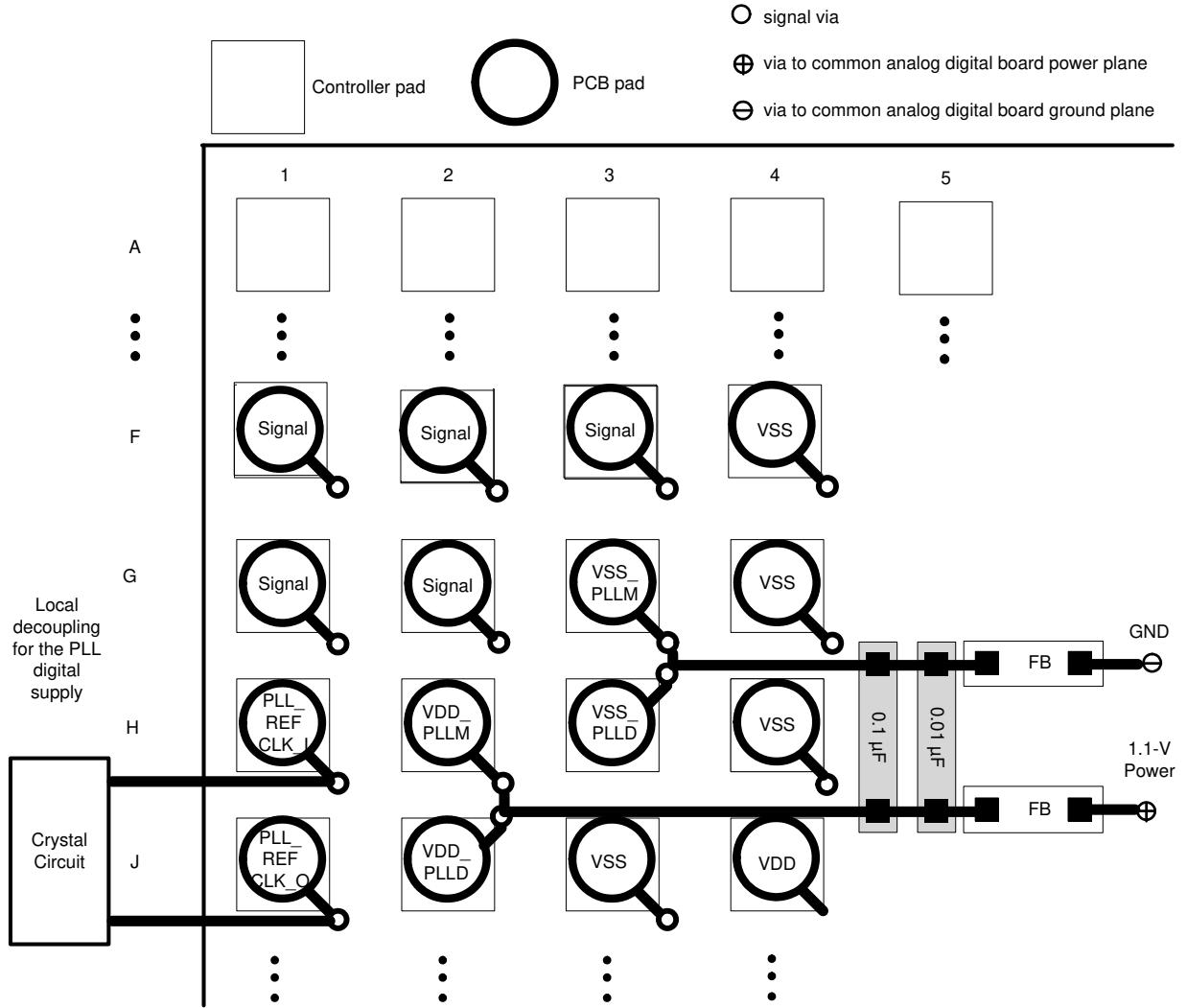
#### 10.1.1 PLL Power Layout

Follow these recommended guidelines to achieve acceptable controller performance for the internal PLL. The DLPC34xx controller contains two internal PLLs which have dedicated analog supplies (VDD\_PLLM, VSS\_PLLM, VDD\_PLLD, and VSS\_PLLD). At a minimum, isolate the VDD\_PLLx power and VSS\_PLLx ground pins using a simple passive filter consisting of two series ferrite beads and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be 0.1  $\mu\text{F}$  and one be 0.01  $\mu\text{F}$ . Place all four components as close to the controller as possible. It's especially important to keep the leads of the high frequency capacitors as short as possible. Connect both capacitors from VDD\_PLLM to VSS\_PLLM and VDD\_PLLD to VSS\_PLLD on the controller side of the ferrite beads.

Select ferrite beads with these characteristics:

- DC resistance less than 0.40  $\Omega$
- Impedance at 10 MHz equal to or greater than 180  $\Omega$
- Impedance at 100 MHz equal to or greater than 600  $\Omega$

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD\_PLLM and VDD\_PLLD must be a single trace from the DLPC34xx controller to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

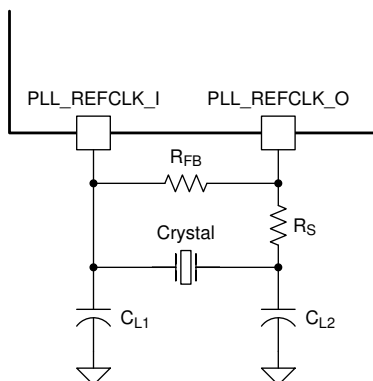



**10-1. PLL Filter Layout**

### 10.1.2 Reference Clock Layout

The DLPC34xx controller requires an external reference clock to feed the internal PLL. Use either a crystal or oscillator to supply this reference. The DLPC34xx reference clock must not exceed a frequency variation of  $\pm 200$  ppm (including aging, temperature, and trim component variation).

Figure 10-2 shows the required discrete components when using a crystal.



$C_L$  = Crystal load capacitance (farads)

$C_{L1} = 2 \times (C_L - C_{stray\_pll\_refclk\_i})$

$C_{L2} = 2 \times (C_L - C_{stray\_pll\_refclk\_o})$

where:

- $C_{stray\_pll\_refclk\_i}$  = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin  $pll\_refclk\_i$ .
- $C_{stray\_pll\_refclk\_o}$  = Sum of package and PCB stray capacitance at the crystal pin associated with the controller pin  $pll\_refclk\_o$ .

#### Figure 10-2. Required Discrete Components

##### 10.1.2.1 Recommended Crystal Oscillator Configuration

Table 10-1. Crystal Port Characteristics

| PARAMETER                       | NOM | UNIT |
|---------------------------------|-----|------|
| PLL_REFCLK_I TO GND capacitance | 1.5 | pF   |
| PLL_REFCLK_O TO GND capacitance | 1.5 | pF   |

Table 10-2. Recommended Crystal Configuration

| PARAMETER <sup>(1) (2)</sup>  | RECOMMENDED   | UNIT       |
|---|---|------------|
| Crystal circuit configuration   | Parallel resonant   |            |
| Crystal type  | Fundamental (first harmonic)                              |            |
| Crystal nominal frequency   | 24  | MHz        |
| Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity) | $\pm 200$   | PPM        |
| Maximum startup time  | 1.0   | ms         |
| Crystal equivalent series resistance (ESR)  | 120 (max)   | $\Omega$   |
| Crystal load  | 6   | pF         |
| $R_S$ drive resistor (nominal)  | 100   | $\Omega$   |
| $R_{FB}$ feedback resistor (nominal)  | 1   | M $\Omega$ |
| $C_{L1}$ external crystal load capacitor  | See equation in Figure 10-2 notes                         | pF         |
| $C_{L2}$ external crystal load capacitor  | See equation in Figure 10-2 notes                         | pF         |
| PCB layout  | A ground isolation ring around the crystal is recommended |            |

(1) Temperature range of  $-30^\circ\text{C}$  to  $85^\circ\text{C}$ .

(2) The crystal bias is determined by the controllers VCC\_INTF voltage rail, which is variable (not the VCC18 rail).

If an external oscillator is used, then the oscillator output must drive the PLL\_REFCLK\_I pin on the DLPC34xx controller, and the PLL\_REFCLK\_O pin must be left unconnected.

**表 10-3. Recommended Crystal Parts**

| MANUFACTURER<br>(1) (2) | PART NUMBER                    | SPEED<br>(MHz) | TEMPERATURE<br>AND AGING<br>(ppm) | MAXIMUM<br>ESR ( $\Omega$ ) | LOAD<br>CAPACITANCE<br>(pF) | PACKAGE<br>DIMENSIONS<br>(mm) |
|-------------------------|--------------------------------|----------------|-----------------------------------|-----------------------------|-----------------------------|-------------------------------|
| KDS                     | DSX211G-24.000M-8pF-50-50      | 24             | $\pm 50$                          | 120                         | 8                           | 2.0 × 1.6                     |
| Murata                  | XRCGB24M000F0L11R0             | 24             | $\pm 100$                         | 120                         | 6                           | 2.0 × 1.6                     |
| NDK                     | NX2016SA 24M<br>EXS00A-CS05733 | 24             | $\pm 145$                         | 120                         | 6                           | 2.0 × 1.6                     |

- (1) The crystal devices in this table have been validated to work with the DLPC34xx controller. Other devices may also be compatible but have not necessarily been validated by TI.
- (2) Operating temperature range:  $-30^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  for all crystals.

### 10.1.3 DSI Interface Layout

Follow these PCB layout guidelines for the DSI LVDS interface to ensure proper DSI operation.

- Route the differential clock and data lines to match 50-Ω single-ended and 100-Ω differential impedance.
- The length of dp and dn should be matched. If that is not possible, ensure that dp is only slightly longer than dn (delta delay not to exceed 8-10 ps), especially for the clock-lane. This is to prevent propagation on the clock lane during the HS to LP transition.
- No thru-hole vias permitted on high-speed traces.
- Create trace routes on top or bottom layers preferably.
- Must have a ground reference plane.
- Avoid power plane transitions in upper or lower layers.
- Avoid using SMD (surface mount device) resistors larger than 0402. If resistors are used in the traces, ensure that the layer below has a void.
- No thru-hole SMA (SubMiniature version A) connectors.
- Minimize trace length as much as possible.
- Perform signal integrity simulations to ensure board performance.

### 10.1.4 Unused Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends tying unused controller input pins through a pullup resistor to its associated power supply or a pulldown resistor to ground. For controller inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive an external device. The DLPC34xx controller implements very few internal resistors and are listed in the tables found in the *Pin Configuration and Functions* section. When external pullup or pulldown resistors are needed for pins that have weak pullup or pulldown resistors, choose a maximum resistance of 8 kΩ.

Never tie unused output-only pins directly to power or ground. Leave them open.

When possible, TI recommends that unused bidirectional I/O pins are configured to their output state such that the pin can remain open. If this control is not available and the pins may become an input, then include an appropriate pullup (or pulldown) resistor.

### 10.1.5 DMD Control and Sub-LVDS Signals

**表 10-4. Maximum Pin-to-Pin PCB Interconnect Recommendations**

| DMD BUS SIGNAL <sup>(1) (2)</sup>    | SIGNAL INTERCONNECT TOPOLOGY       |                                   | UNIT       |
|--------------------------------------|------------------------------------|-----------------------------------|------------|
|                                      | SINGLE-BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH |            |
| DMD_HS_CLK_P<br>DMD_HS_CLK_N         | 6.0<br>(152.4)                     | See <sup>(3)</sup>                | in<br>(mm) |
| DMD_HS_WDATA_A_P<br>DMD_HS_WDATA_A_N | 6.0<br>(152.4)                     | See <sup>(3)</sup>                | in<br>(mm) |
| DMD_HS_WDATA_B_P<br>DMD_HS_WDATA_B_N |                                    |                                   |            |
| DMD_HS_WDATA_C_P<br>DMD_HS_WDATA_C_N |                                    |                                   |            |
| DMD_HS_WDATA_D_P<br>DMD_HS_WDATA_D_N |                                    |                                   |            |
| DMD_HS_WDATA_E_P<br>DMD_HS_WDATA_E_N |                                    |                                   |            |
| DMD_HS_WDATA_F_P<br>DMD_HS_WDATA_F_N |                                    |                                   |            |
| DMD_HS_WDATA_G_P<br>DMD_HS_WDATA_G_N |                                    |                                   |            |
| DMD_HS_WDATA_H_P<br>DMD_HS_WDATA_H_N |                                    |                                   |            |
| DMD_LS_CLK                           | 6.5<br>(165.1)                     | See <sup>(3)</sup>                | in<br>(mm) |
| DMD_LS_WDATA                         | 6.5<br>(165.1)                     | See <sup>(3)</sup>                | in<br>(mm) |
| DMD_LS_RDATA                         | 6.5<br>(165.1)                     | See <sup>(3)</sup>                | in<br>(mm) |
| DMD_DEN_ARSTZ                        | 7.0<br>(177.8)                     | See <sup>(3)</sup>                | in<br>(mm) |

- (1) Maximum signal routing length includes escape routing.
- (2) Multi-board DMD routing length is more restricted due to the impact of the connector.
- (3) Due to PCB variations, these recommendations cannot be defined. Any board design should SPICE simulate with the controller IBIS model (found under the *Tools & Software* tab of the controller web page) to ensure routing lengths do not violate signal requirements.

**表 10-5. High Speed PCB Signal Routing Matching Requirements**

| SIGNAL GROUP LENGTH MATCHING <sup>(1) (2) (3)</sup> |                                      |                              |                             |            |
|---|--------------------------------------|------------------------------|-----------------------------|------------|
| INTERFACE   | SIGNAL GROUP                         | REFERENCE SIGNAL             | MAX MISMATCH <sup>(4)</sup> | UNIT       |
| DMD <sup>(5)</sup>                                  | DMD_HS_WDATA_A_P<br>DMD_HS_WDATA_A_N | DMD_HS_CLK_P<br>DMD_HS_CLK_N | ±1.0<br>(±25.4)             | in<br>(mm) |
|   | DMD_HS_WDATA_B_P<br>DMD_HS_WDATA_B_N |                              |                             |            |
|   | DMD_HS_WDATA_C_P<br>DMD_HS_WDATA_C_N |                              |                             |            |
|   | DMD_HS_WDATA_D_P<br>DMD_HS_WDATA_D_N |                              |                             |            |
|   | DMD_HS_WDATA_E_P<br>DMD_HS_WDATA_E_N |                              |                             |            |
|   | DMD_HS_WDATA_F_P<br>DMD_HS_WDATA_F_N |                              |                             |            |
|   | DMD_HS_WDATA_G_P<br>DMD_HS_WDATA_G_N |                              |                             |            |
|   | DMD_HS_WDATA_H_P<br>DMD_HS_WDATA_H_N |                              |                             |            |
| DMD   | DMD_HS_WDATA_x_P                     | DMD_HS_WDATA_x_N             | ±0.025<br>(±0.635)          | in<br>(mm) |
| DMD   | DMD_HS_CLK_P                         | DMD_HS_CLK_N                 | ±0.025<br>(±0.635)          | in<br>(mm) |
| DMD   | DMD_LS_WDATA<br>DMD_LS_RDATA         | DMD_LS_CLK                   | ±0.2<br>(±5.08)             | in<br>(mm) |
| DMD   | DMD_DEN_ARSTZ                        | N/A                          | N/A                         | in<br>(mm) |

- (1) The length matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC34xx controller or the DMD require no additional consideration.
- (2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.
- (3) DMD LS signals are single ended.
- (4) Mismatch variance for a signal group is always with respect to the reference signal.
- (5) DMD HS data lines are differential, thus these specifications are pair-to-pair.



**表 10-6. Signal Requirements**

| PARAMETER                 | REFERENCE        | REQUIREMENT                                      |
|---------------------------|------------------|--|
| Source series termination | DMD_LS_WDATA     | Required   |
|                           | DMD_LS_CLK       | Required   |
|                           | DMD_DEN_ARSTZ    | Acceptable                                       |
|                           | DMD_LS_RDATA     | Required   |
|                           | DMD_HS_WDATA_x_y | Not acceptable                                   |
|                           | DMD_HS_CLK_y     | Not acceptable                                   |
| Endpoint termination      | DMD_LS_WDATA     | Not acceptable                                   |
|                           | DMD_LS_CLK       | Not acceptable                                   |
|                           | DMD_DEN_ARSTZ    | Not acceptable                                   |
|                           | DMD_LS_RDATA     | Not acceptable                                   |
|                           | DMD_HS_WDATA_x_y | Not acceptable                                   |
|                           | DMD_HS_CLK_y     | Not acceptable                                   |
| PCB impedance             | DMD_LS_WDATA     | 68 Ω ±10%  |
|                           | DMD_LS_CLK       | 68 Ω ±10%  |
|                           | DMD_DEN_ARSTZ    | 68 Ω ±10%  |
|                           | DMD_LS_RDATA     | 68 Ω ±10%  |
|                           | DMD_HS_WDATA_x_y | 100 Ω ±10%                                       |
|                           | DMD_HS_CLK_y     | 100 Ω ±10%                                       |
| Signal type               | DMD_LS_WDATA     | SDR (single data rate) referenced to DMD_LS_DCLK |
|                           | DMD_LS_CLK       | SDR referenced to DMD_LS_DCLK                    |
|                           | DMD_DEN_ARSTZ    | SDR  |
|                           | DMD_LS_RDATA     | SDR referenced to DMD_LS_DCLK                    |
|                           | DMD_HS_WDATA_x_y | sub-LVDS   |
|                           | DMD_HS_CLK_y     | sub-LVDS   |

### 10.1.6 Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers. Ideally ensure that the signals of a given pair do not change layers.

### 10.1.7 Stubs

- Avoid using stubs.

### 10.1.8 Terminations

- DMD\_HS differential signals require no external termination resistors.
- Make sure the DMD\_LS\_CLK and DMD\_LS\_WDATA signal paths include a 43-Ω series termination resistor located as close as possible to the corresponding controller pins.
- Make sure the DMD\_LS\_RDATA signal path includes a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- The DMD\_DEN\_ARSTZ pin requires no series resistor.

### 10.1.9 Routing Vias

- The number of vias on DMD\_HS signals must be minimized and ideally not exceed two.
- Any and all vias on DMD\_HS signals must be located as close to the controller as possible.
- The number of vias on the DMD\_LS\_CLK and DMD\_LS\_WDATA signals must be minimized and ideally not exceed two.
- Any and all vias on the DMD\_LS\_CLK and DMD\_LS\_WDATA signals must be located as close to the controller as possible.

### 10.1.10 Thermal Considerations

The underlying thermal limitation for the DLPC34xx controller is that the maximum operating junction temperature ( $T_J$ ) not be exceeded (this is defined in the *Recommended Operating Conditions* section).

Some factors that influence  $T_J$  are as follows:

- operating ambient temperature
- airflow
- PCB design (including the component layout density and the amount of copper used)
- power dissipation of the DLPC34xx controller
- power dissipation of surrounding components

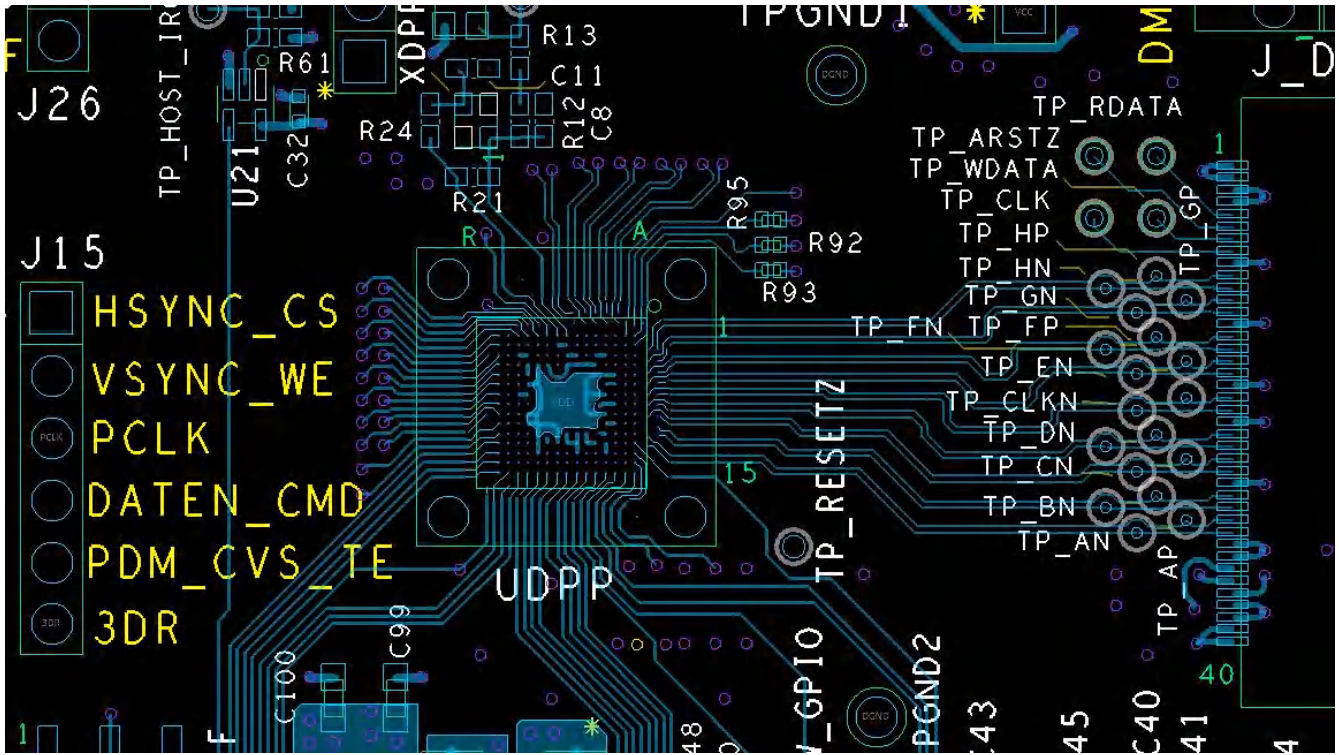
The controller package is designed to primarily extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature ( $T_A$ ) is provided primarily as a design target and is based on maximum DLPC34xx controller power dissipation and  $R_{\theta JA}$  at 0 m/s of forced airflow, where  $R_{\theta JA}$  is the thermal resistance of the package as measured using a JEDEC defined standard test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC34xx controller PCB, so the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommends that thermal performance be measured and validated after the PCB is designed and the application is built.

To evaluate the thermal performance, measure the top center case temperature under the worse case product scenario (maximum power dissipation, maximum voltage, maximum ambient temperature), and validate the controller does not exceed the maximum recommended case temperature ( $T_C$ ). This specification is based on the measured  $\phi_{JT}$  for the DLPC34xx controller package and provides a relatively accurate correlation to junction temperature.

Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. Place the bead and thermocouple wire so that they contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

## 10.2 Layout Example



10-3. Layout Recommendation

## 11 Device and Documentation Support

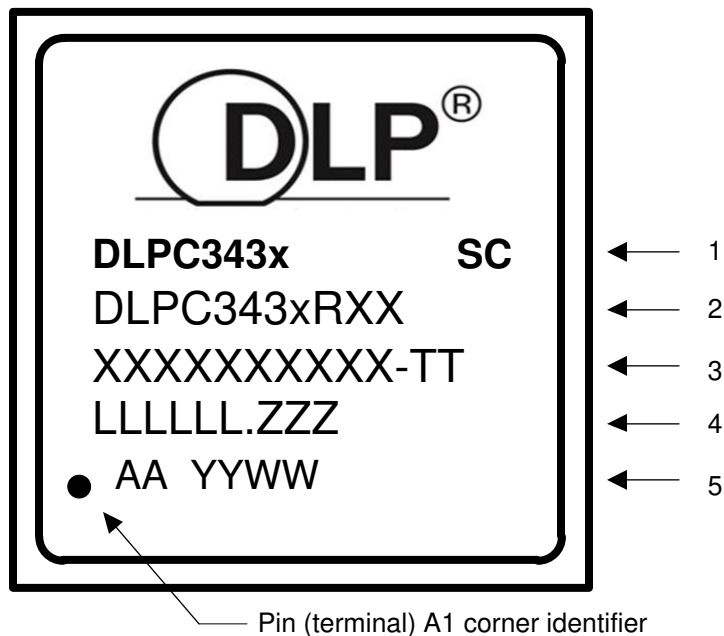
### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

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#### 11.1.2 Device Nomenclature

##### 11.1.2.1 Device Markings



#### Marking Definitions:

- Line 1: DLP Device Name: DLPC343x where x is a "2" for this device  
 SC: Solder ball composition  
 e1: Indicates lead-free solder balls consisting of SnAgCu  
 G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green
- Line 2: TI Part Number  
 DLP Device Name: DLPC343x where x is a "2" for this device  
**R**: corresponds to the TI device revision letter; for example A, B, or C  
**XX**: corresponds to the last two letters of the device package designator
- Line 3: XXXXXXXXXXXX-TT: Manufacturer Part Number
- Line 4: LLLLLL.ZZZ: Foundry lot code for semiconductor wafers and lead-free solder ball marking  
 LLLLLL: Fab lot number  
 ZZZ: Lot split number
- Line 5: AA YYWW ES: Package assembly information  
 AA: Manufacturing site  
 YYWW: Date code (YY = Year :: WW = Week)

注

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.
2. See 表 7-1, for DLPC343x resolutions on the DMD supported per part number.

### 11.1.3 Video Timing Parameter Definitions

See 図 11-1 for a visual description.

|  |  |
|--|--|
| <b>Active Lines Per Frame (ALPF)</b>         | Defines the number of lines in a frame containing displayable data. ALPF is a subset of the TLPF.  |
| <b>Active Pixels Per Line (APPL)</b>         | Defines the number of pixel clocks in a line containing displayable data. APPL is a subset of the TPPL.  |
| <b>Horizontal Back Porch (HBP) Blanking</b>  | Defines the number of blank pixel clocks after the active edge of horizontal sync but before the first active pixel.   |
| <b>Horizontal Front Porch (HFP) Blanking</b> | Defines the number of blank pixel clocks after the last active pixel but before horizontal sync.   |
| <b>Horizontal Sync (HS or Hsync)</b>         | Timing reference point that defines the start of each horizontal interval (line). The active edge of the HS signal defines the absolute reference point. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.   |
| <b>Total Lines Per Frame (TLPF)</b>          | Total number of active and inactive lines per frame; defines the vertical period (or frame time).  |
| <b>Total Pixel Per Line (TPPL)</b>           | Total number of active and inactive pixel clocks per line; defines the horizontal line period in pixel clocks.   |
| <b>Vertical Sync (VS or Vsync)</b>           | Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured. |
| <b>Vertical Back Porch (VBP) Blanking</b>    | Defines the number of blank lines after the active edge of vertical sync but before the first active line.   |
| <b>Vertical Front Porch (VFP) Blanking</b>   | Defines the number of blank lines after the last active line but before the active edge of vertical sync.  |

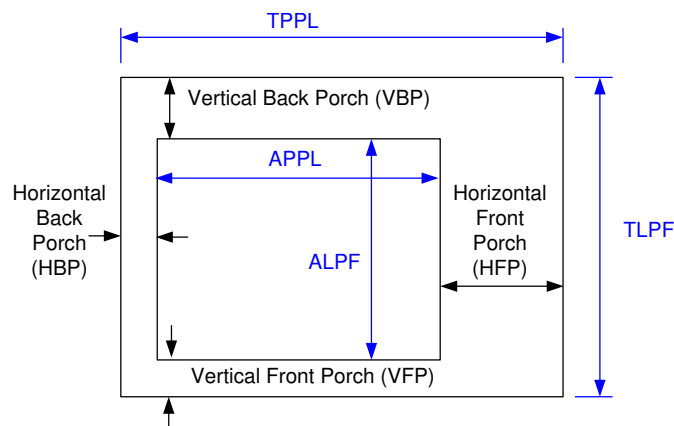


图 11-1. Parameter Definitions

## 11.2 Related Documentation

The following table lists quick access links for associated parts of the DLP chipset.

**表 11-1. Chipset Documentation**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|
| DLPA2000 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DLPA2005 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DLPA3000 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| DLP230GP | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**表 11-2. Related Links**

| PARTS    | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DLPC3432 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

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## 11.8 用語集

**TI 用語集** この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

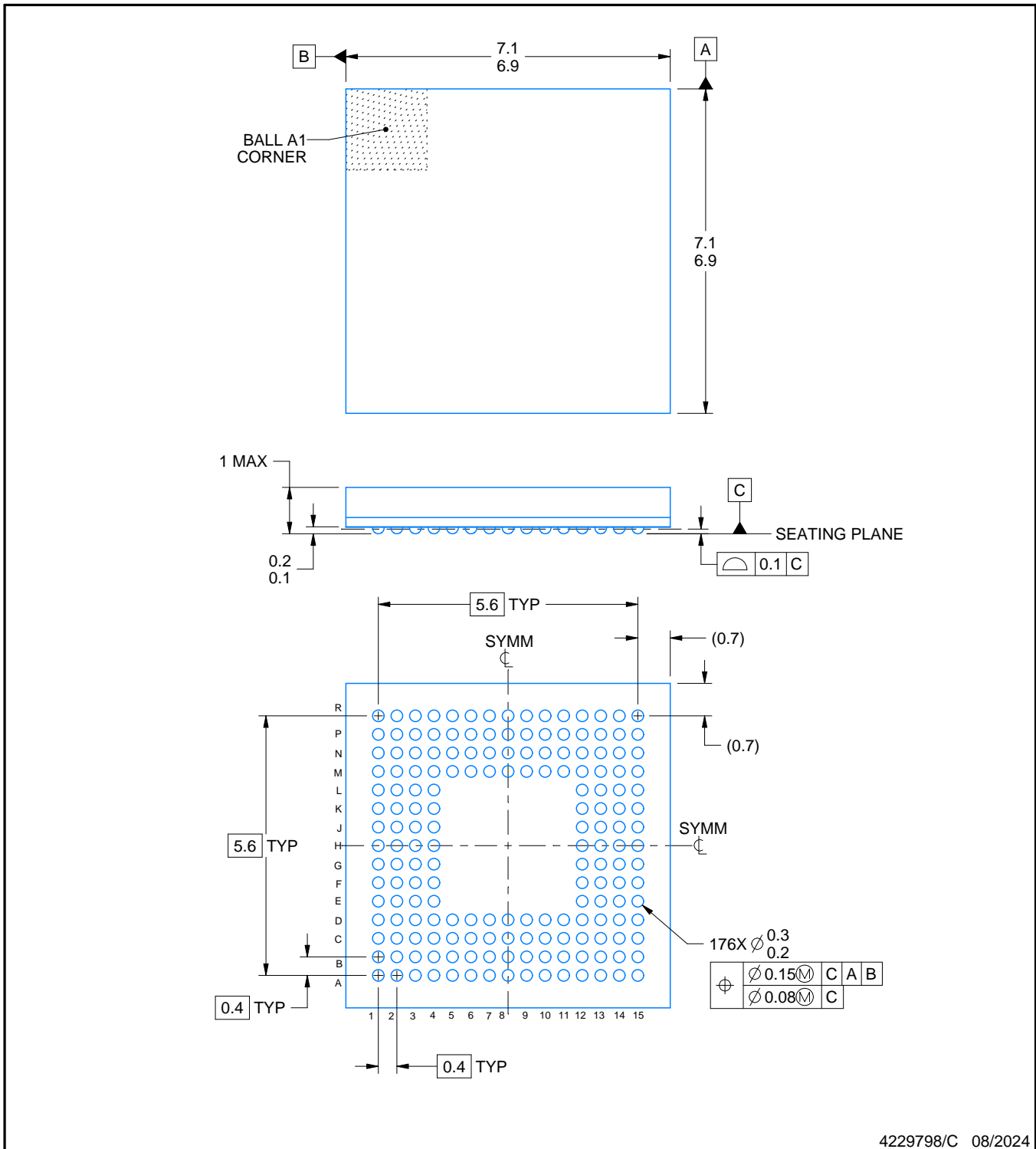
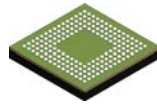
## 13 Package Option Addendum

### 13.1 Packaging Information

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3)    | Op Temp (°C) | Device Marking(4) (5) |
|------------------|------------|--------------|-----------------|------|-------------|--------------|------------------|----------------------|--------------|-----------------------|
| DLPC3432CZVB     | ACTIVE     | NFBGA        | ZVB             | 176  | 260         | TBD          | Call TI          | Level-3-260C-168 HRS | -30 to 85°C  | DLPC343x              |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.  
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NOTES:

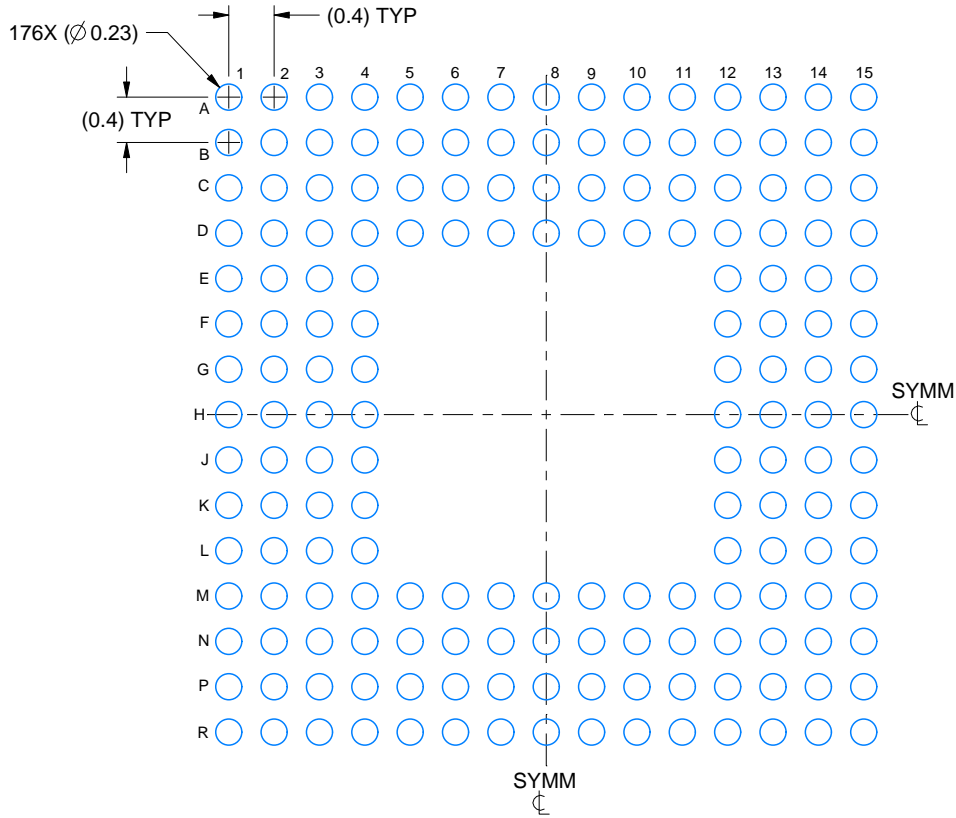
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

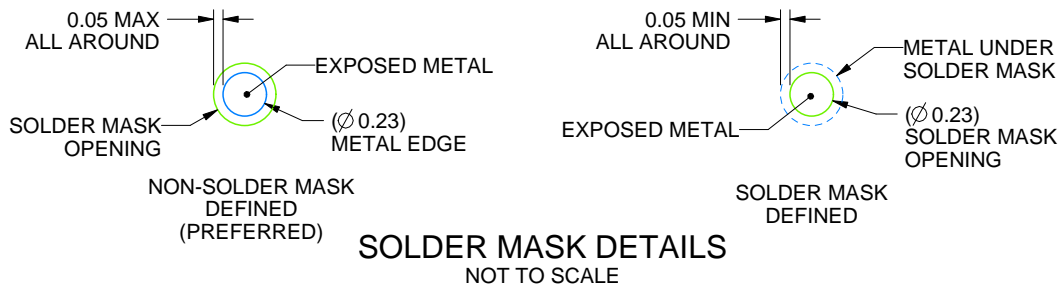
ZVB0176A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE: 15X



4229798/C 08/2024

NOTES: (continued)

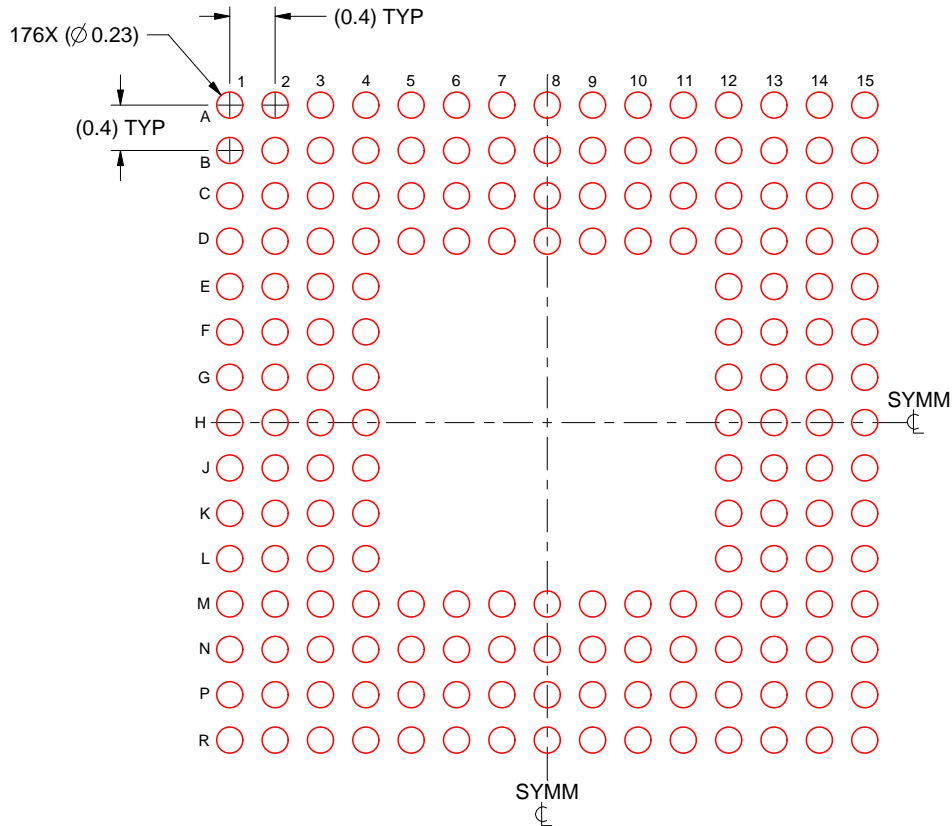
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZVB0176A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 15X

4229798/C 08/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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