DP83825I 低消費電力 10/100Mbps イーサネット物理層トランシーバ

1 特長

- 超小型の 10/100Mbps PHY：QFN 3mm × 3mm、24 ピン
- ケーブル伝送距離：150m 超
- 超低消費電力：127mW 未満
- 小型のシステム・ソリューション：MDI および MAC 終端抵抗を内蔵
- プログラム可能な省エネルギー・モード
  - アクティブ・スリープ
  - ディープ・パワーダウン
  - Energy Efficient Ethernet (EEE) IEEE 802.3az
  - レガシー MAC での EEE サポート
  - Wake-on-LAN (WoL)
- 電圧モード・ライン・ドライバ
- MAC インターフェイス：RMII (マスタおよびスレーブ・モード)
- 単一 3.3V 電源
- I/O 電圧：1.8V、3.3V
- リピータ：アンマネージド・モードでの RMII バック・ツー・バック・モード
- 構成およびステータス用 MDC/MDIO インターフェイス
- 高速なリンク・ドロップ・モード
- 診断機能
  - TDR ベースのケーブル断線および短絡診断
  - パケット・ジェネレータ内蔵
  - 複数ループバック
- プログラム可能なハードウェア割り込みピン
- 動作温度範囲：-40℃～85℃
- IEEE 802.3 100BASE-TX および 10BASE-Te 仕様に準拠

2 アプリケーション

- ビルディング・オートメーション：IP カメラ、HMI
- 消費者向け電子機器：STB、OTT、IPTV、ゲーム機
- プリンタ
- POS システム
- ファクトリ・オートメーション

3 概要

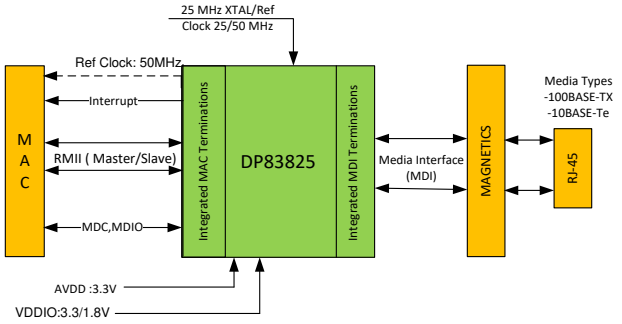
DP83825I は、10BASE-Te および 100BASE-TX イーサネット・プロトコルをサポートする PMD サブレイヤを内蔵した超小型、超低消費電力のイーサネット物理層トランシーバです。CAT5e ケーブルで最大 150m の伝送距離をサポートします。DP83825I は、外付けトランスを介してツイスト・ペア・メディアに直接接続できます。マスタ・モードとスレーブ・モードの両方で RMII (Reduced MII) により MAC 層に接続します。RMII マスタ・モードで 50MHz の出力クロックを供給します。このクロックは、システムのジッタを低減するため、MDI を基準とするクロックに同期しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DP83825I	QFN (24)	3.00mm × 3.00mm、0.4mm ピッチ

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

DP83825I アプリケーション図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年12月発行のものから更新 **Page**

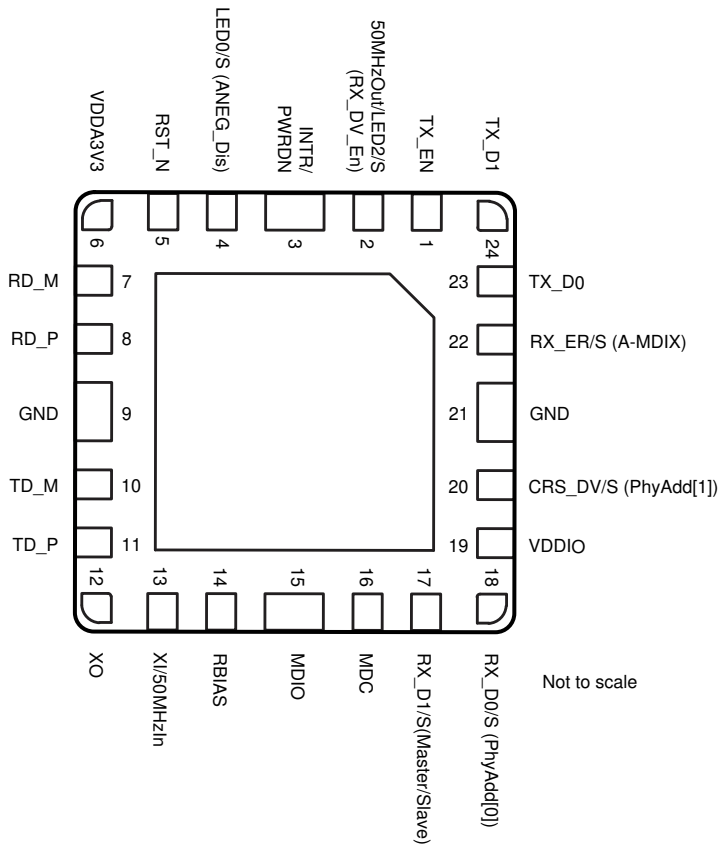
- デバイスのステータスを「事前情報」から「量産データ」に変更 ... 1

5 概要 (続き)

DP83825I は、Energy Efficient Ethernet、Wake-on-LAN、MAC 絶縁にも対応しているため、システムの消費電力をさらに低減できます。MAC 上での EEE 信号処理をサポートしていないレガシー MAC でも、レジスタ設定を使って Energy Efficient モードを有効にできます。DP83825I はアンマネージド・リピータ・モードで動作できます。このモードでは、DP83825I はレジスタ設定なしでリピータとして動作します。 DP83825I は、開発とデバッグを簡単にするため、内蔵ケーブル診断ツール、組み込み自己テスト、ループバック機能を備えています。

6 Pin Configuration and Functions

DP83825 RMQ Package
24-Pin QFN
Top View



DP83825I Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TX_EN	1	Reset: I, PD Active: I, PD	RMII Transmit Enable: TX_EN is active high signal and is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D [1:0].
50MHzOut/LED2	2	Reset: I, PD, S Active: O	RMII Master Mode: 50 MHz Clock Out(default). RMII Slave Mode: LED_2(default). This pin can be configured as GPIO using register configuration.

(1) The pin functions are defined below:
Type I: Input
Type O: Output
Type I/O: Input/Output
Type PD or PU: Internal Pulldown or Pullup
Type S: Strap Configuration Pin

DP83825I Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
INTR/PWRDN	3	Reset: I, PU Active: I, PU	Interrupt / Power Down(default): The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power-down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup (9.5KΩ). Some applications may require an external pullup resistor.
LED0	4	Reset: I, PD, S Active: O	LED0 : Activity Indication LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when Link is good. The LED blinks when the transmitter or receiver is active. This pin can also act as GPIO through register configuration. **This pin is at 3.3 V always and not linked to voltage supplied to VDDIO pin. This is to avoid external components when operating PHY at VDDIO 1.8 V.**
RST_N	5	Reset: I, PU Active: I, PU	RST_N: This pin is an active low reset input. Asserting this pin low for at least 1 μs will force a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.
VDDA3V3	6	Power	Input Analog Supply: 3.3 V. For decoupling capacitor requirements, refer to the *Application and Implementation* section.図 20
RD_M	7	A	Differential Receive Input (PMD): These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX specific signaling mode
RD_P	8	A	
GND	9	GND	Ground: Connect to Ground
TD_M	10	A	Differential Transmit Output (PMD): These differential outputs are configured to either 10BASE-Te, 100BASE-TX signaling mode based on configuration chosen for PHY.
TD_P	11	A	
XO	12	A	Crystal Output: Reference Clock output. XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	13	A	Crystal / Oscillator Input Clock RMII Master mode: 25-MHz ±50 ppm-tolerance crystal or oscillator clock RMII Slave mode: 50-MHz ±50 ppm-tolerance CMOS-level oscillator clock
RBIAS	14	A	RBIAS value 6.49 KΩ 1% connected to ground
MDIO	15	Reset: I, PU-10K Active: IO, PU-10K	Management Data I/O: Bidirectional management data signal that may be source by the management station or the PHY. This pin has internal pullup of 10 KΩ. External pullup of up to 2.2 KΩ can be added if needed
MDC	16	Reset: I, PD Active: I, PD	Management Data Clock: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25 MHz. There is no minimum clock rate.
RX_D1	17	Reset: I, PD, S Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. They contain valid data when RX_DV is asserted.
RX_D0	18	Reset: I, PD, S Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. They contain valid data when RX_DV is asserted.
VDDIO	19	Power	I/O Supply : 3.3 V/1.8 V. For decoupling capacitor requirements, refer to the *Application and Implementation* section.
CRS_DV	20	Reset: I, PD, S Active: O	Carrier Sense / Receive Data Valid: This pin combines the RMII Carrier and Receive Data Valid indications.
GND	21	GND	Ground pin
RX_ER	22	Reset: I, PD, S Active: O	RMII Receive Error: This pin indicates an error symbol has been detected within a received packet in RMII mode. RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in RMII because the PHY will automatically corrupting data on a receive error.
TX_D0	23	Reset: I, PD Active: I, PD	RMII Transmit Data: TX_D[1:0] received from the MAC and shall be synchronous to the rising edge of the reference clock.
TX_D1	24	Reset: I, PD Active: I, PD	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1](

PARAMETER		MIN	MAX	UNIT
Analog supply voltage	AVDD3V3	–0.3	4	V
IO supply voltage	VDDIO3V3	–0.3	4	V
	VDDIO1V8	–0.3	2.1	V
Junction Temperature	Tj		105	°C
Storage Temperature	Tstg	–65	150	°C
MDI pins	TD–, TD+, RD–, RD+	-0.3	4	V
MAC interface pins		–0.3	4	V
SMI interface pins		–0.3	4	V
XI		–0.3	4	V
Reset		–0.3	4	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All Pins (except MDI)	±1.5		kV
	MDI (Media Dependent Interface) pins	±5		kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500-V HBM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD3V3	3	3.3	3.6	V
IO supply voltage	VDDIO3V3	3	3.3	3.6	V
	VDDIO1V8	1.62	1.8	1.98	V
Operating Free Air Temperature (DP83825I)	Ta	–40	25	85	C
Pins	TX_EN, TX_D0, TX_D1, RX_D0, RX_D1, RX_DV, RX_ER, MDIO, MDC, INT/PWDN, RESET	VDDIO-10%	VDDIO	VDDIO+10 %	V
Pins	XI Osclliator Input	VDDIO-10%	VDDIO	VDDIO+10 %	V
Pins	LED0	AVDD3V3-10%	AVDD3V3	AVDD3V3+10%	V

7.4 Thermal Information

THERMAL METRIC(1)			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.3	°C/W
Y_{JT}	Junction-to-top characterization parameter	28.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	14.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx CONFORMANCE (100BaseTx)						
	Differential Output Voltage	100 Base Tx idle transmission		1.0		V
IEEE Tx CONFORMANCE (10BaseTe)						
	Differential Voltage	10BaseTe data transmission		1.75		V
POWER CONSUMPTION (Power Optimised Mode)						
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 50%		37.5		mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 50%		37.5		mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 50%		7.5		mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 50%		3.5		mA
I(VDDIO=1V8)	RMII Master (100BaseTx)	Traffic = 50%		4.5		mA
I(VDDIO=1V8)	RMII Slave (100BaseTx)	Traffic = 50%		1.6		mA
POWER CONSUMPTION (Cable Reach Optimised Mode)						
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 50%		41		mA
I(AVDD3V3)	RMII Master (100BaseTx)	Traffic = 100%		41	50	mA
I(AVDD3V3)	RMII Master (10BaseTe)	Traffic = 50%		28		mA
I(AVDD3V3)	RMII Master (10BaseTe)	Traffic = 100%		32	40	mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 50%		41	50	mA
I(AVDD3V3)	RMII Slave (100BaseTx)	Traffic = 100%		41	50	mA
I(AVDD3V3)	RMII Slave (10BaseTe)	Traffic = 50%		28		mA
I(AVDD3V3)	RMII Slave (10BaseTe)	Traffic = 100%		32	40	mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 50%		7.5		mA
I(VDDIO=3V3)	RMII Master (100BaseTx)	Traffic = 100%		10	14	mA
I(VDDIO=3V3)	RMII Master (10BaseTe)	Traffic = 50%		6.5		mA
I(VDDIO=3V3)	RMII Master (10BaseTe)	Traffic = 100%		7.5	12	mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 50%		3.5		mA
I(VDDIO=3V3)	RMII Slave (100BaseTx)	Traffic = 100%		5	8	mA
I(VDDIO=3V3)	RMII Slave (10BaseTe)	Traffic = 50%		2.5	6	mA
I(VDDIO=3V3)	RMII Slave (10BaseTe)	Traffic = 100%		2.5	6	mA
I(VDDIO=1V8)	RMII Master (100BaseTx)	Traffic = 50%		4	14	mA

(1) Ensured by production test, characterization or design

Electrical Characteristics (continued)

over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO =1V8)	RMII Master (100BaseTx)	Traffic = 100%		5.5	14	mA
I(VDDIO =1V8)	RMII Master (10BaseTe)	Traffic = 50%		4		mA
I(VDDIO =1V8)	RMII Master (10BaseTe)	Traffic = 100%		4	14	mA
I(VDDIO =1V8)	RMII Slave (100BaseTx)	Traffic = 50%		1.5		mA
I(VDDIO =1V8)	RMII Slave (100BaseTx)	Traffic = 100%		2.5	6	mA
I(VDDIO =1V8)	RMII Slave (10BaseTe)	Traffic = 50%		1		mA
I(VDDIO =1V8)	RMII Slave (10BaseTe)	Traffic = 100%		1	6	mA
POWER CONSUMPTION (Low Power Modes)						
I(AVDD= 3V3)	100 BaseTx EEE mode	100 BaseTx link in EEE mode with LPIs ON		15.5		mA
	Deep Power Down			3.5		mA
	IEEE Power Down			4		mA
	Active Sleep			11		mA
	Active but not Link			37		mA
	RESET			5.5		mA
I(VDDIO =3V3)	100 BaseTx EEE mode			2		mA
	Deep Power Down			2.5		mA
	IEEE Power Down			2		mA
	Active Sleep			5		mA
	Active but not Link			5		mA
	RESET			2.5		mA
I(VDDIO =1V8)	100 BaseTx EEE mode			2		mA
	Deep Power Down			1.5		mA
	IEEE Power Down			1.5		mA
	Active Sleep			3		mA
	Active but not Link			3		mA
	RESET			1.5		mA
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{IH_3v3}	High Level Bootstrap Threshold : 3V3		1.3			V
V_{IL_3v3}	Low Level Bootstrap Threshold : 3V3				0.6	V
V_{IH_1v8}	High Level Bootstrap Threshold:1V8		1.3			V
V_{IL_1v8}	Low Level Bootstrap Threshold :1V8				0.6	V
Crystal oscillator						
	Load Capacitance			15	30	pF
IO						
3V3	V_{IH} High Level Input Voltage	VDDIO= 3V3+/- 10%	1.7			V
	V_{IL} Low Level Input Voltage	VDDIO= 3V3+/- 10%			0.8	V
	V_{OH} High Level Output Voltage	I_{oH}= -2mA, VDDIO=3V3 +/-10%	2.4			V
	V_{OL}Low Level Output Voltage	I_{oL}= 2mA, VDDIO=3V3 +/- 10%			0.4	V

Electrical Characteristics (continued)

over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1V8	V_{IH} High Level Input Voltage	VDDIO= 1V8+/- 10%	0.65*VDDIO			V
	V_{IL} Low Level Input Voltage	VDDIO= 1V8+/- 10%			0.35*VDDIO	V
	V_{OH} High Level Output Voltage	I_{oH}= -2mA, VDDIO=1V8 +/-10%	VDDIO-0.45			V
	V_{OL}Low Level Output Voltage	I_{oL}= 2mA, VDDIO=1V8 +/- 10%			0.45	V
	Iih (VIN=VCC)	T_A=-40 TO 85C, VIN=VDDIO			15	uA
	Iil (VIN=GND)	T_A=-40 TO 85C, VIN=GND			15	uA
	Iozh	Tri State Output High Current	-15		15	uA
	Iozl	Tri State Output Low Current	-15		15	uA
	Cin (Input Capacitance)			5		pF
	R Pull Down		8	10	13	Kohms
	R Pull UP		8	10	13	Kohms
	XI input osc clock pk-pk			VDDIO		V
	XI input osc clock common mode			VDDIO/2		V

7.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
POWER-UP TIMING					
T1	Voltage Ramp Duration (0 to 100% VDDIO) (1)	0.5		40	ms
T2	Supply Sequencing AVDD followed by VDDIO			200	ms
T3	Voltage Ramp Duration (0 to 100% of AVDD)	0.5		40	ms
T4	POR release time / Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access			50	ms
T5	Powerup to FLP		1500		ms
	Pedestal Voltage on AVDD, VDDIO before Power Ramp			0.3	V
RESET TIMING					
T1	RESET PULSE Width: Miminum Reset pulse width to be able to reset (w/o debouncing caps)	25			us
T2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access			2	ms
T3	Reset to FLP		1500		ms
	Reset to 100M signaling (strapped mode)		0.5		ms
	Reset to RMII Master clock		0.2		ms
100M EEE timings					
	Sleep time (Ts)		210		us
	Quiet time (Tq)		20		ms
	Refresh time (Tr)		200		us
	Wake time (Tw_sys_tx)		36		us
RMII Master TIMING (100M)					
	RMII Master Clock Period		20		ns
	RMII Master Clock Duty Cycle	35		65	%
T2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock	4			ns
T3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock	2			ns
T4	RX_D[1:0], RX_ER, CRS_DV Delay from RMII Master Clock rising edge	4	10	14	ns
RMII Slave TIMING (100M)					
T1	Input Reference Clock Period		20		ns
	Reference Clock Duty Cycle	35		65	%
T2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising (2)	4			ns
T3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising	2			ns
T4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising	4		14	ns
SMI TIMING					
T1	MDC to MDIO (Output) Delay Time	0		10	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	20	MHz
OUTPUT CLOCK TIMING (50M RMII Master Clock)					
	Frequency (PPM)	-50		50	ppm
	Duty Cycle	35		65	%
	Rise time			4000	ps
	Fall Time			4000	ps
	Jitter (Long Term)			450	ps
	RefCLK to clock out delay with multiple resets			40	ns
INPUT CLOCK tolerance					
25MHz	Frequency Tolerance	-50		50	ppm

(1) Clock shall be available at power ramp. If Clock is provided after power ramp, external Reset of PHY is needed once clock is available
(2) RMII Slave Output Timing default supports setup time upto 7.5 ns. For 7.5ns to 10.5ns, program register 0x0017.8 = 1, 0x0042=0x0014

Timing Requirements (continued)

PARAMETER		MIN	NOM	MAX	UNIT
	Rise / Fall Time			5	ns
	Jitter Tolerance (Accumulated over 100,000 cycles)			1.75	ns
	Duty Cycle	40		60	%
	input phase noise at 1KHz			-98	dBc/Hz
	input phase noise at 10KHz			-113	dBc/Hz
	input phase noise at 100KHz			-113	dBc/Hz
	input phase noise at 1MHz			-113	dBc/Hz
	input phase noise at 10MHz			-113	dBc/Hz
50MHz	Frequency Tolerance	-50		50	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (Accumulated over 100,000 cycles)			1.75	ns
	Duty Cycle	40		60	%
	input phase noise at 1KHz			-87	dBc/Hz
	input phase noise at 10KHz			-107	dBc/Hz
	input phase noise at 100KHz			-107	dBc/Hz
	input phase noise at 1MHz			-107	dBc/Hz
	input phase noise at 10MHz			-107	dBc/Hz
LATENCY TIMING					
Tx	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI (100M)		105		ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI (100M)		105		ns
	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI (10M)		1350		ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI (10M)		1300		ns
Rx	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV (100M)		350		ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV (100M)		325		ns
	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV (10M)		2150		ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV (10M)		2150		ns

7.7 Timing Diagrams

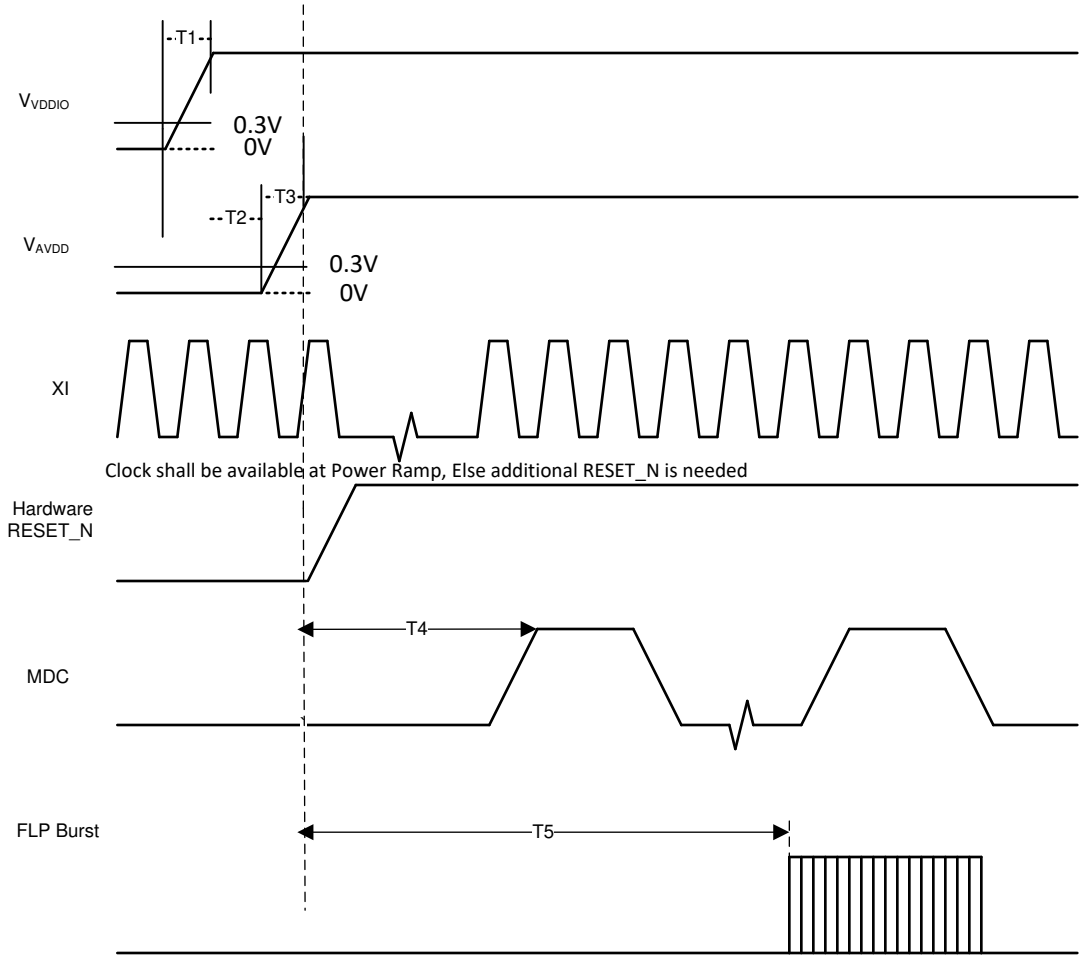


図 1. Power-Up Timing

Timing Diagrams (continued)

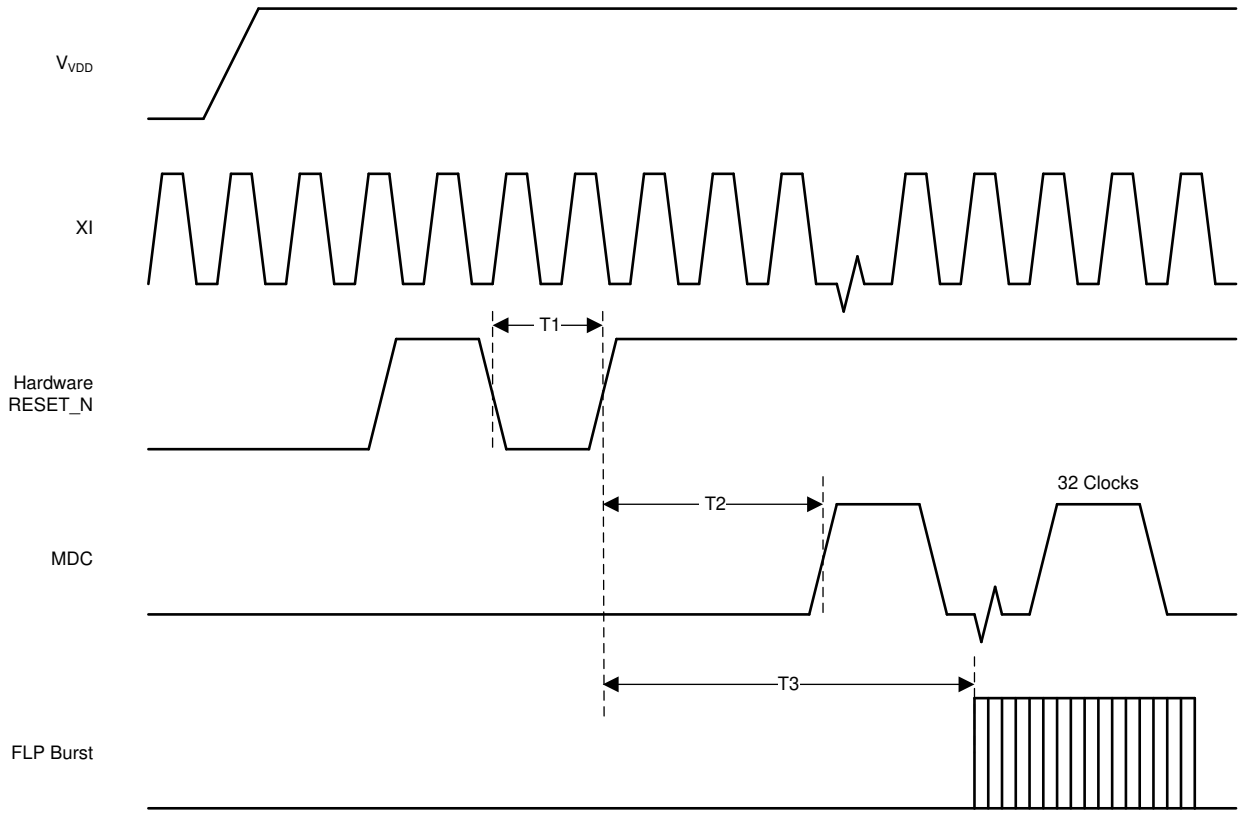


図 2. Reset Timing

Timing Diagrams (continued)

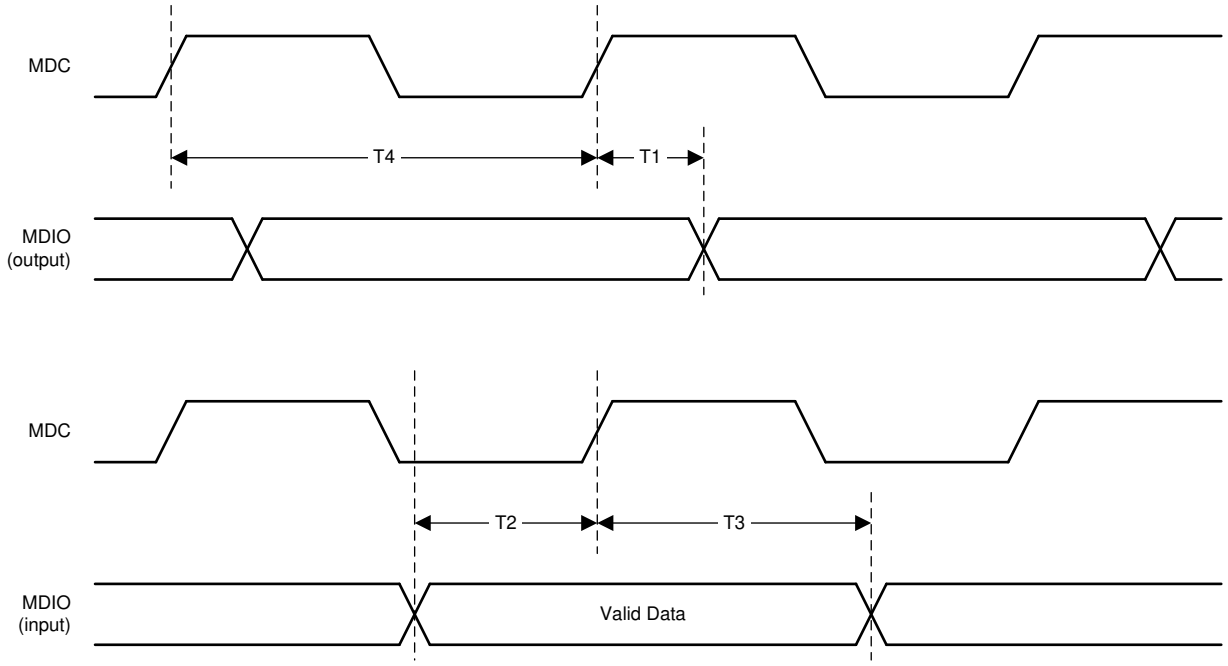


図 3. Serial Management Timing

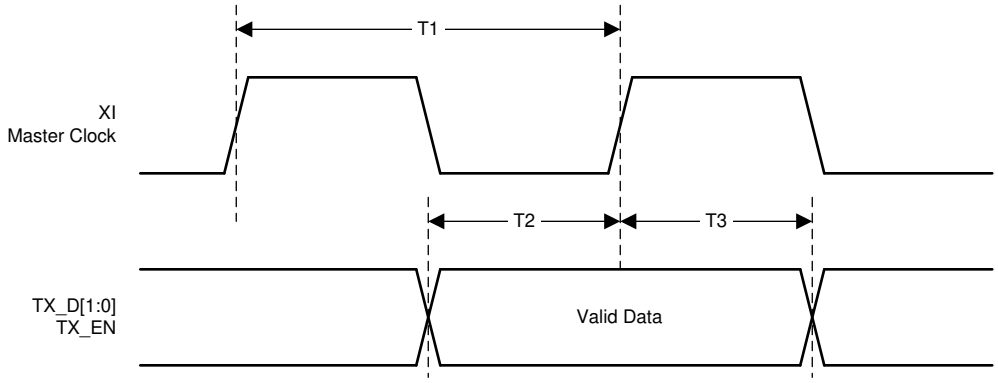


図 4. RMII Transmit Timing

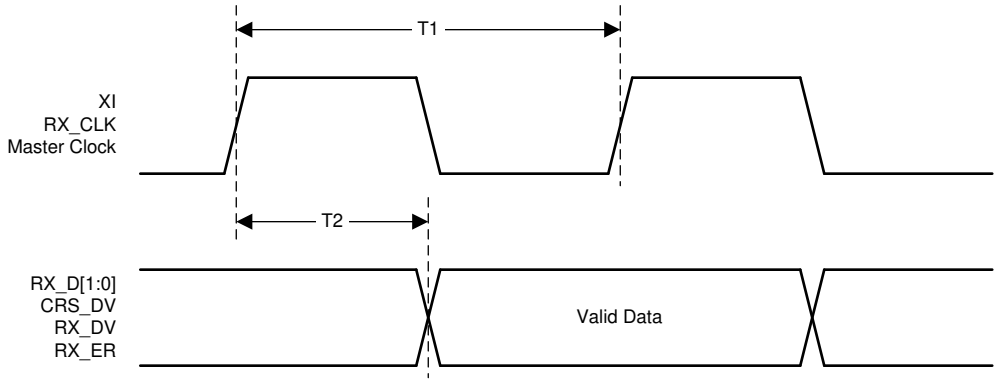


図 5. RMII Receive Timing

7.8 Typical Characteristics

This section describes the DP83825 Drive characteristics for VDDIO 3.3 V and 1.8 V.

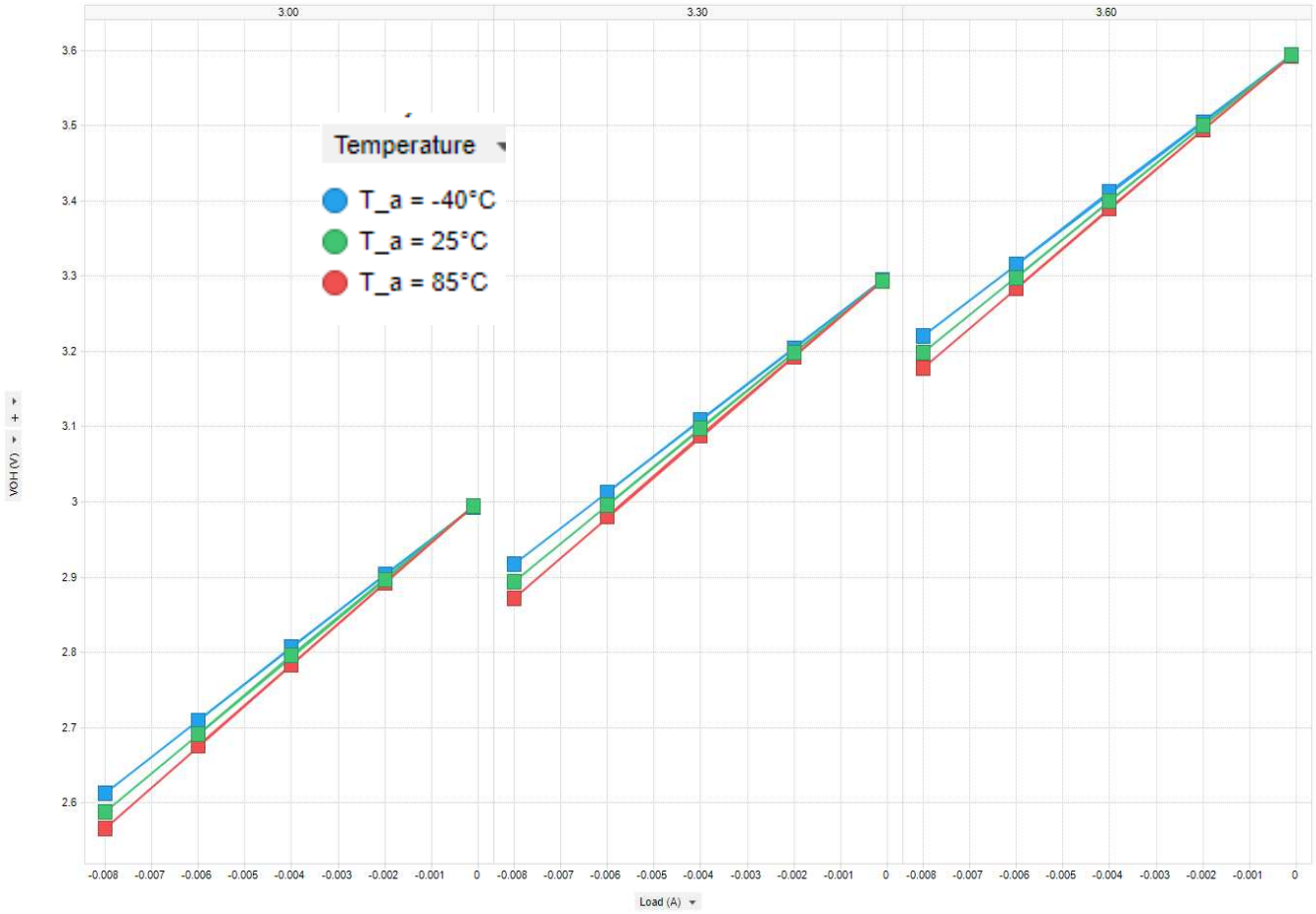


図 6. LED_0, LED_1, CLKOUT VOH 3.3 V

Typical Characteristics (continued)

This section describes the DP83825 Drive characteristics for VDDIO 3.3 V and 1.8 V.

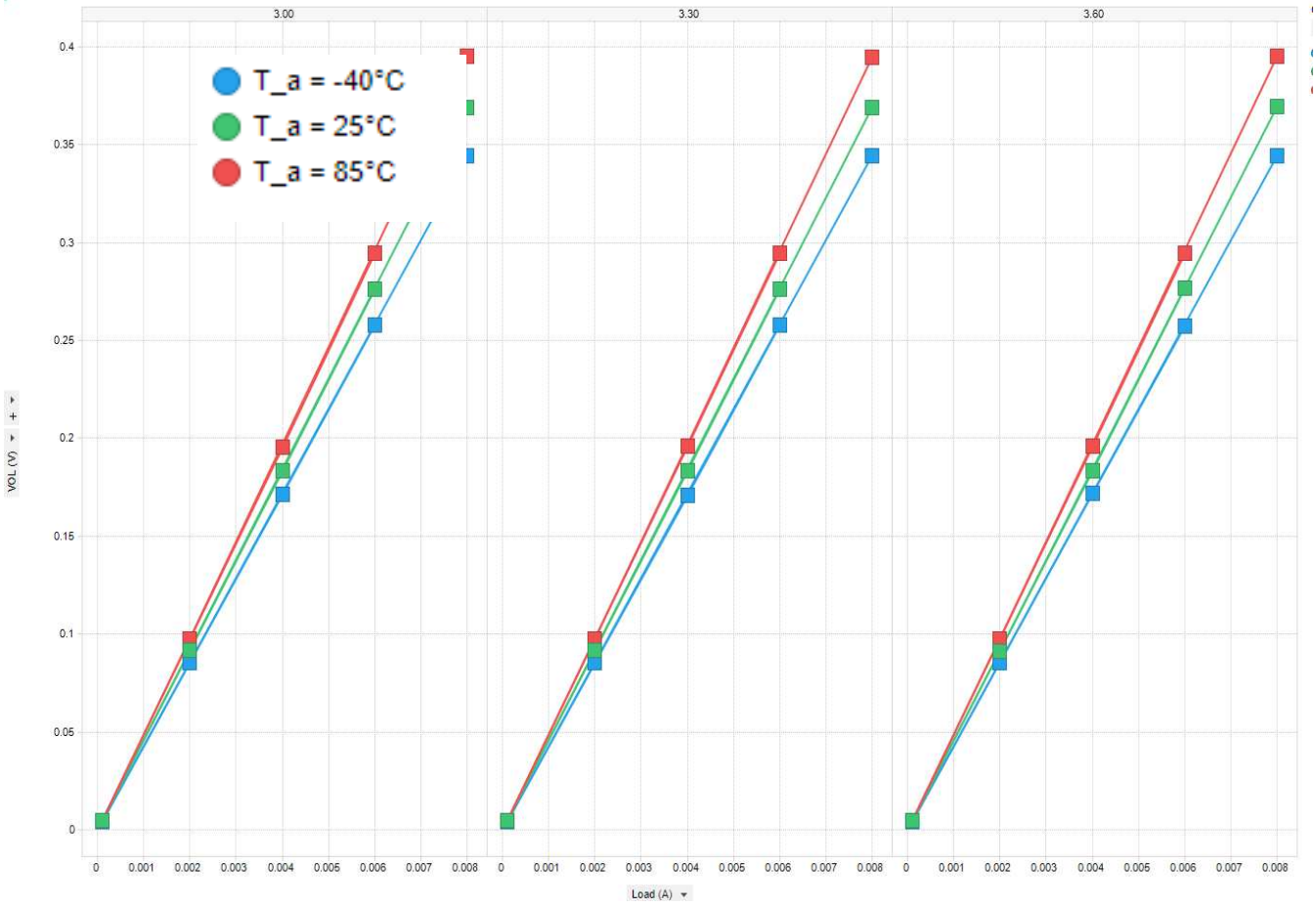


図 7. LED_0, LED_1, CLKOUT VOL 3.3 V

Typical Characteristics (continued)

This section describes the DP83825 Drive characteristics for VDDIO 3.3 V and 1.8 V.

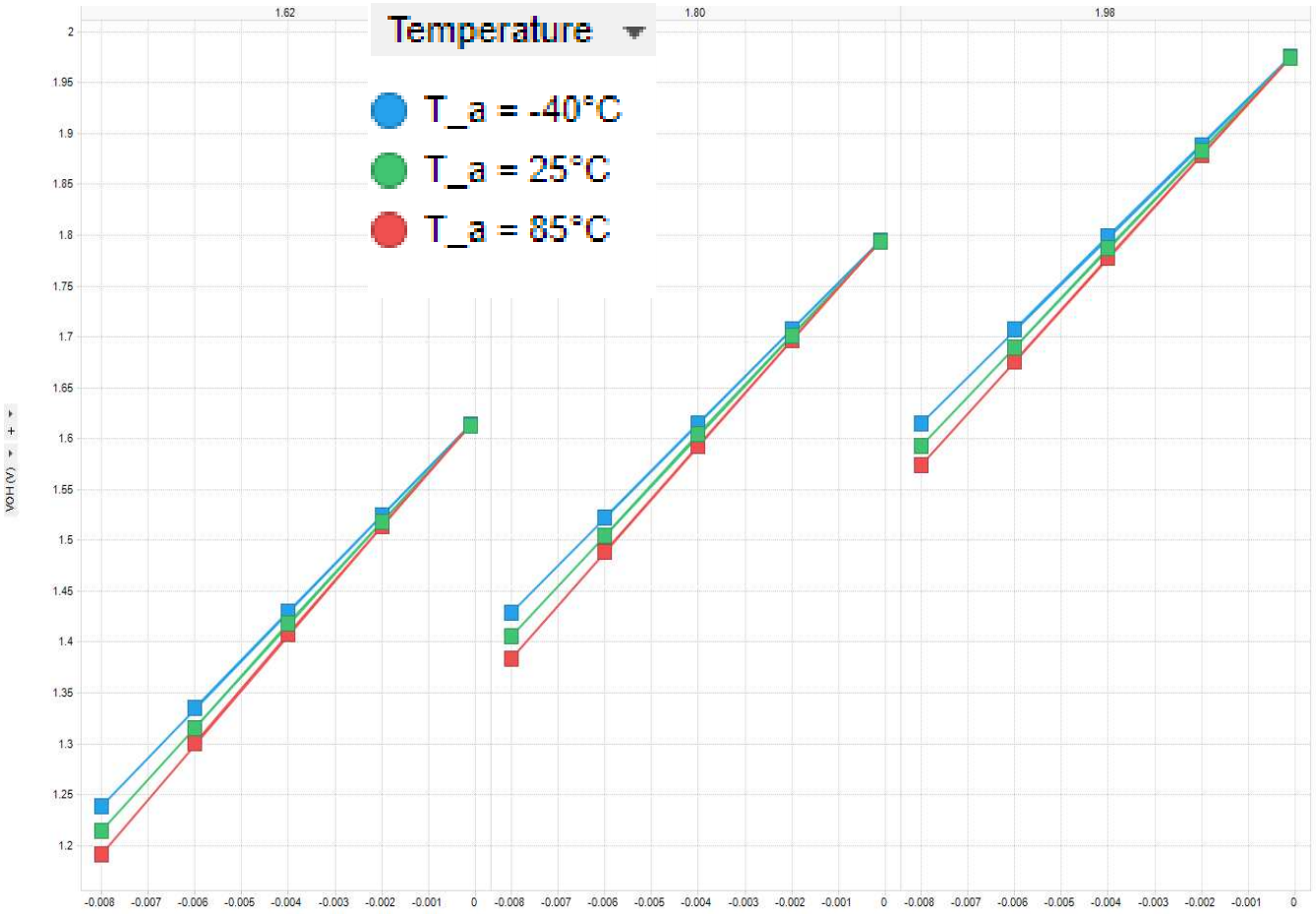


図 8. LED_1, CLKOUT VOH 1.8 V

Typical Characteristics (continued)

This section describes the DP83825 Drive characteristics for VDDIO 3.3 V and 1.8 V.

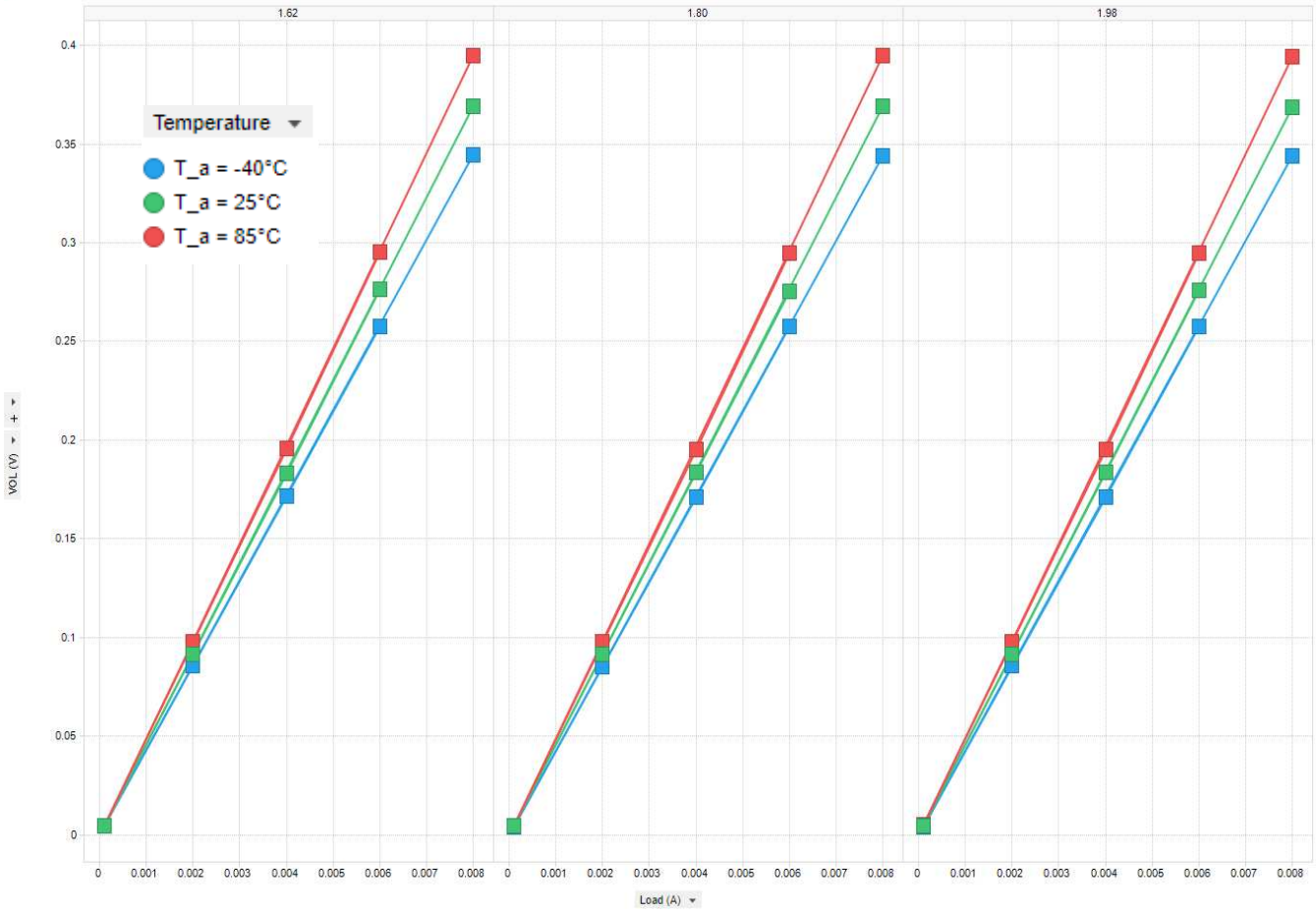


図 9. LED_1, CLKOUT VOL 1.8 V

8 Detailed Description

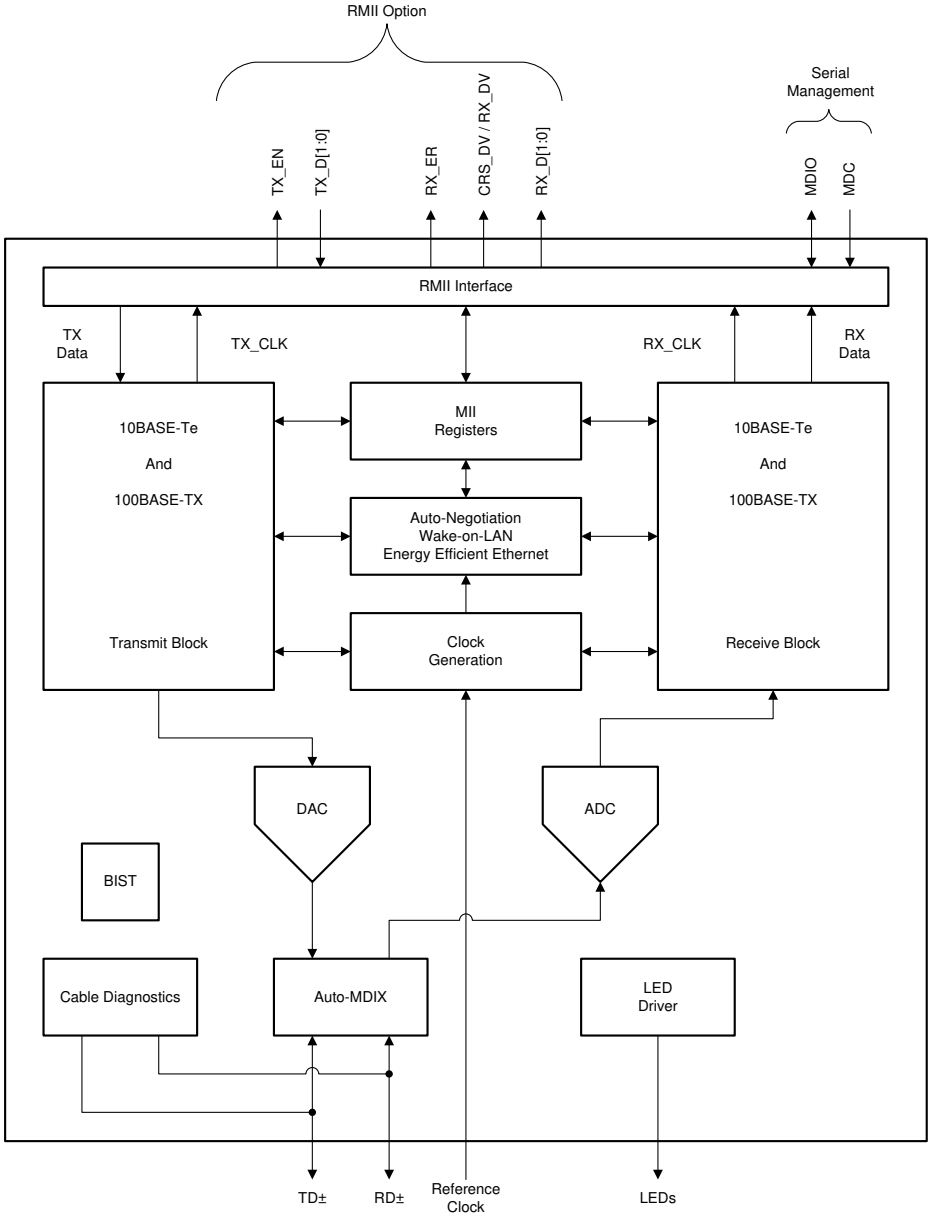
8.1 Overview

The DP83825I is a fully-featured single-port Physical Layer transceiver compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The device supports the standard Reduced Media Independent Interface (RMII) for direct connection to Media Access Controller (MAC).

The device is designed for a single 3.3-V power supply with an integrated LDO to provide voltage rails needed for internal blocks. The device allows I/O voltage interfaces for 3.3 V or 1.8 V. Automatic supply configuration within the DP83825I allows for any combination of VDDIO supply and AVDD supply without the need for additional configuration settings.

The DP83825I uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over a CAT5e twisted-pair cable greater than 150 meters. DP83825I supports various Low Power features like Active Sleep, IEEE Power Down and Deep Power Down. It also supports Energy Efficient Ethernet and Wake-on-LAN.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto-Negotiation (Speed / Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83825I supports 100BASE-TX and 10BASE-Te modes of operation for Auto-Negotiation. Auto-Negotiation ensures that the highest common speed is selected based on the advertised abilities of the Link Partner and the local device. Auto-Negotiation can be enabled or disabled in hardware, using the bootstrap, or by register configuration, using bit[12] in the Basic Mode Control Register (BMCR, address 0x0000). For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification.

Feature Description (continued)

8.3.2 Auto-MDIX Resolution

The DP83825I can determine if a “straight” or “crossover” cable is used to connect to the link partner. It can automatically re-assign channel A and B to establish link with the link partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Forced modes.

Auto-MDIX can be enabled or disabled in hardware, using the hardware bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished using register configuration, using bit[14] of the PHYCR.

8.3.3 Energy Efficient Ethernet

8.3.3.1 EEE Overview

Energy Efficient Ethernet (EEE), defined by IEEE 802.3az, is a capability integrated into Layer 1 (Physical Layer) and Layer 2 (Data Link Layer) to operate in Low Power Idle (LPI) mode. In LPI mode, power is saved during periods of low packet utilization. EEE defines the protocol to enter and exit LPI mode without dropping the link or corrupting packets.

The DP83825I EEE supports 100-Mbps and 10-Mbps speeds. In 10BASE-Te operation, EEE operates with a reduced transmit amplitude that is fully interoperable with a 10BASE-T PHY.

8.3.3.2 EEE Negotiation

EEE is advertised during Auto-Negotiation. Auto-Negotiation is performed at power up, on management command, after link failure, or due to user intervention. EEE is supported if and only if both link partners advertise EEE capabilities. If EEE is not supported, all EEE functions are disabled and the MAC should not assert LPI. To advertise EEE capabilities, the PHY needs to exchange an additional formatted next page and unformatted next page in sequence.

EEE Negotiation can be activated using Register Access. IEEE 802.3az defines MMD3 and MMD7 as the locations for EEE control and status registers. The MMD3 registers 0x1014, 0x1001, 0x1016, and MMD7 registers 0x203C and 0x203D contain all the required controls and status indications for operating EEE. The Energy Efficient Ethernet Configuration Register #3 (EEECFG3, address 0x04D1) contains controls for EEE configuration bypass. By default, EEE capabilities are bypassed. To advertise EEE based on MMD3 and MMD7 registers, EEE capabilities bypass needs to be disabled (0x04D1.0 = 0, 0x04D1.3 = 0) and EEE Advertisement shall be enabled (MMD7 0x203C.1 = 1).

8.3.4 EEE for Legacy MACs Not Supporting 802.3az

The device can be configured to initiate LPI signaling (Idle and Refresh) through register programming as well. This feature enables the system to perform EEE even when the MAC used is not supporting EEE. In this mode, responsibility of enabling and disabling LPI signaling lies on the Host Controller Application. While the DP83825I is in LPI signaling mode, this application will move the DP83825I into active mode before sending any data over the MAC interface. The DP83825I does not have buffering capability to store the data while in LPI signaling mode. To enable EEE through register configuration, the following registers must be configured:

1. Enable EEE capabilities by writing 0x04D1.0 = 0, 0x04D1.3 = 0
2. Advertise EEE capabilities during auto-negotiation by writing (MMD7 0x203C.1 = 1)
3. Renegotiate the link by writing 0x0000.9 = 1
4. Forced Tx LPI idles by writing 0x04D1.12 = 1
5. Write 0x04D1.12=0 to stop transmitting LPI Idles

Feature Description (continued)

8.3.5 Wake-on-LAN Packet Detection

Wake-on-LAN (WoL) provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83825I allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet and Magic Packet with Secure-ON Match. When a qualifying WoL frame is received, the DP83825I WoL logic circuit is able to generate a user-defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. Additionally, the DP83825I includes a CRC Gate to prevent invalid packets from triggering a wake-up event. The Wake-on-LAN feature includes:

- Identification of WoL frames in all supported speeds (100BASE-TX and 10BASE-Te).
- Wake-up interrupt generation upon reception of a WoL frame.
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames.

8.3.5.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83825I scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF.

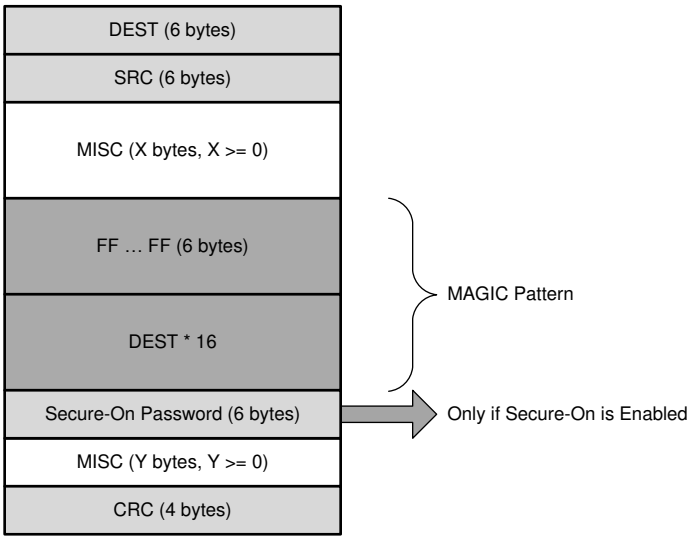


図 10. Magic Packet Structure

8.3.5.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a secure-on password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

Feature Description (continued)

8.3.5.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Receiver Status Register (RXFS, address 0x04A1). The Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register #2 (MISR2, address 0x0013).

8.3.6 Low Power Modes

The DP83825I supports three Low Power Modes. This section discusses the principles behind these low power modes and configuration to enable them.

8.3.6.1 Active Sleep

When the DP83825I enters into Active Sleep mode, all internal circuitry shuts down in the PHY except for the SMI and energy detection circuitry on the TD± and RD± pins. In this mode, the DP83825 sends out NLPs every 1.4 seconds to wake up the link partner. Automatic power up occurs when a link partner is detected.

Active Sleep is enabled by setting bits[14:12] = 0b110 in the PHY Specific Control Register (PHYSCR, address 0x0011).

8.3.7 IEEE Power Down

IEEE Power Down shuts down all PHY circuitry except the SMI and internal clock circuitry.

IEEE Power Down can be activated by either register access or through the INTR/PWRDN pin when the pin is configured for power-down function.

To enable IEEE Power Down through the INTR/PWRDN pin, the pin must be driven LOW to ground.

To enable IEEE Power Down through the SMI, set bit[11] = 1 in the Basic Mode Control Register (BMCR, address 0x0000).

8.3.8 Deep Power Down

Deep Power Down shuts down all PHY circuitry except the SMI. In this mode, the PHY PLL is shut-down to further reduce power consumption.

Deep Power Down is activated by first enabling IEEE Power Down (from either the SMI or INT/PWDN_N pin) and then setting bit[2] = 1 in the Deep Power Down Control Register (DPDWN, address 0x0428).

8.3.9 RMII Repeater Mode

The DP83825I provides an option to enable repeater mode functionality to extend the cable reach in un-managed mode (without the need of additional register configuration). Two DP83825I can be connected in back-to-back mode without any external configuration. It provides a Hardware Strap to configure the CRS_DV pin of RMII interface to RX_DV pin for back-to-back operation. 図 11 shows the RMII pin connection that can enable DP83825I Repeater mode. If using managed mode, external Reset to both PHYs will be triggered at the same time.

Feature Description (continued)

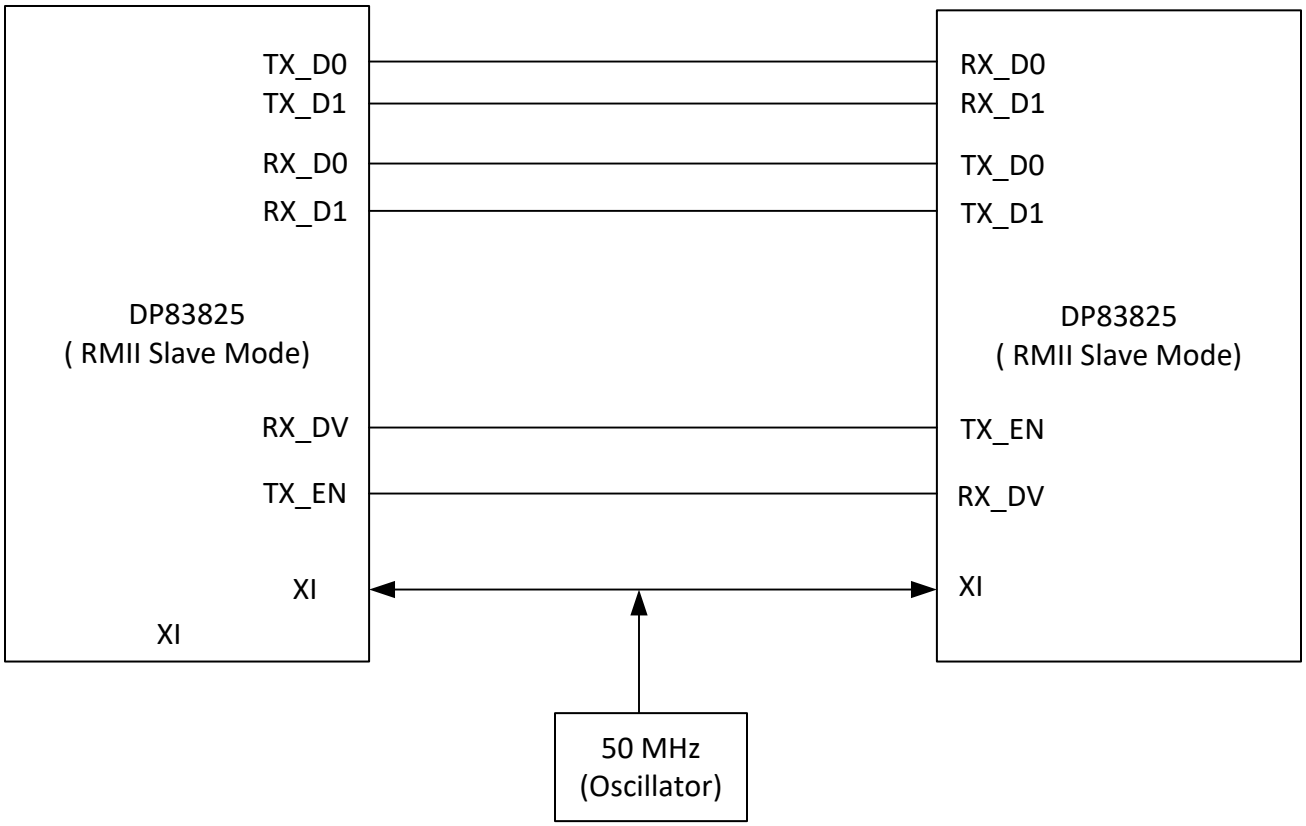


図 11. RMII Repeater Mode

Feature Description (continued)

8.3.10 Reduced Media Independent Interface (RMII)

The DP83825I incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83825I offers two types of RMII operations: RMII Slave and RMII Master. In RMII Master operation, the DP83825I operates off either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referenced from DP83825I can be connected to the MAC. In RMII Slave operation, the DP83825I operates off of a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII Slave mode, the PHY can run from 50MHz clock provided by the Host MAC.

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te.
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are two bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in 表 1:

表 1. RMII Signals

FUNCTION	PINS
Receive Data Lines	TX_D[1:0]
Transmit Data Lines	RX_D[1:0]
Receive Control Signal	TX_EN
Transmit Control Signal	CRS_DV

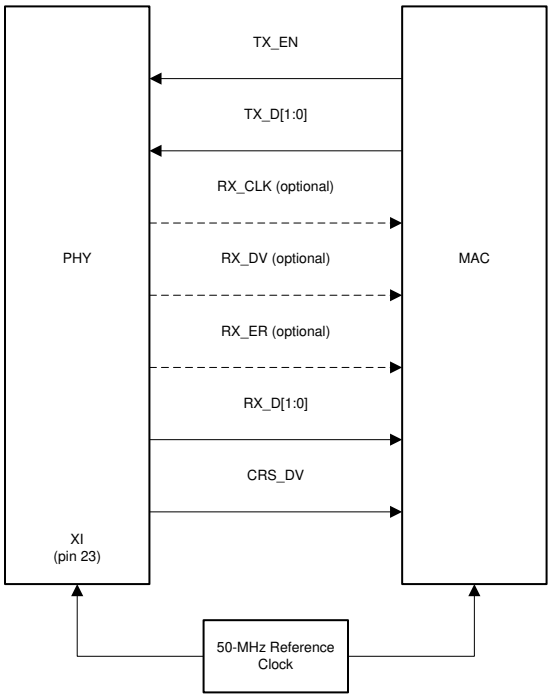


図 12. RMII Slave Signaling

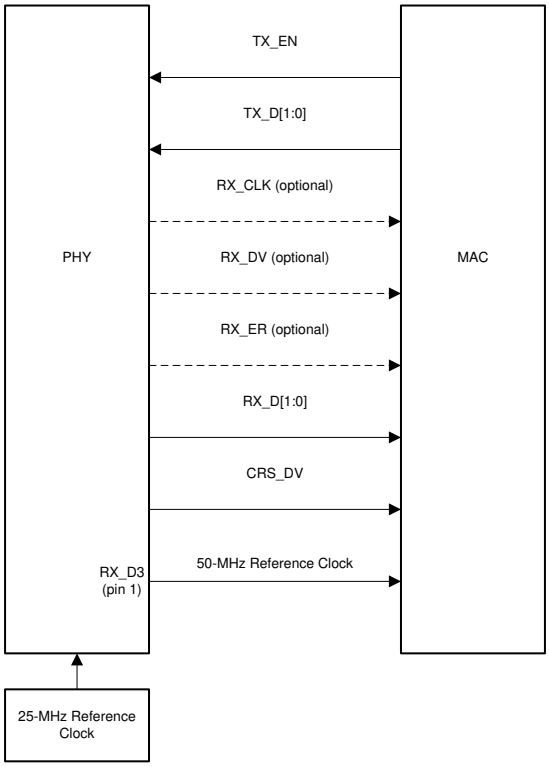


図 13. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the clock edges on the XI pin. Data on RX_D[1:0] are latched at the MAC with reference to the same clock edges on the XI pin.

In addition, CRX_DV can be configured as RX_DV signal. It allows a simpler method of recovering received data without the need to separate RX_DV from the CRS_DV indication.

8.3.11 Serial Management Interface

The Serial Management Interface provides access to the DP83825I internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22 and clause 45. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83825I.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ or 1.5KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 4 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83825I latches the Phy_Address[1:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor-specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83825I drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83825I, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

表 2. SMI Protocol

SMI PROTOCOL	<idle><start><op code><PHY address><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

8.3.11.1 Extended Register Space Access

The DP83825I SMI function supports read and write access to the extended register set using the Register Control Register (REGCR, address 0x000D), the Data Register (ADDAR, address 0x000E), and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah draft for Clause 22 for accessing the Clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR and register ADDAR, which are accessed only using the normal MDIO transaction. The SMI function will ignore indirect access to these registers.

REGCR is the MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of the ADDAR register to the appropriate MMD.

The DP83825I supports three MMD device addresses:

1. The Vendor-Specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00011 is used for Energy Efficient Ethernet MMD register accesses. Register names for registers accessible at this device address are preceded by MMD3.
3. DEVAD[4:0] = 00111 is used for Energy Efficient Ethernet MMD registers accesses. Register names for registers accessible at this device address are preceded by MMD7.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111). For register accesses to the MMD3 or MMD7 registers the corresponding device address would be used.

8.3.11.2 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.3.11.3 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

8.3.11.4 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.11.5 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.11.6 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.3.11.7 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.3.11.8 Example Write Operation (No Post Increment)

The following example will demonstrate a write operation with no post increment. In this example, the MAC impedance will be adjusted to 99.25 Ω using the IO MUX GPIO Control Register (IOCTRL, address 0x0461).

1. Write the value 0x001F to register 0x000D.
2. Write the value 0x0461 to register 0x000E. (Sets desired register to the IOCTRL)
3. Write the value 0x401F to register 0x000D.
4. Write the value 0x0400 to register 0x000E. (Sets MAC impedance to 99.25 Ω)

8.3.11.9 Example Read Operation (No Post Increment)

The following example will demonstrate a read operation with no post increment. In this example, the MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY, address 0x703D) will be read.

1. Write the value 0x0007 to register 0x000D.
2. Write the value 0x003D to register 0x000E. (Sets desired register to the MMD7_EEE_LP_ABILITY)
3. Write the value 0x4007 to register 0x000D.
4. Read the value of register 0x000E. (Data read is the value contained within the MMD7_EEE_LP_ABILITY)

8.3.12 100BASE-TX

8.3.12.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in 表 3 below.

The transmitter section consists of the following functional blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83825I implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

表 3. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T, and R in data fields will be mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

8.3.12.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to 表 3 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

8.3.12.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed-loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed-loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB.

8.3.12.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI-encoded to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5, unshielded twisted-pair cable. There is no ability to bypass this block within the DP83825I. The NRZI data is sent to the 100-Mbps Driver.

8.3.12.1.4 Binary to MLT-3 Converter

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted-pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output Pair common driver is controlled by the slew rate. The designer should consider this when selecting AC-coupling magnetics to ensure TP-PMD standard-compliant transition times (3 ns < Trise/fall < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83825I is capable of sourcing only MLT-3-encoded data. Binary output from the PMD Output Pair is not possible in 100-Mbps mode. Fully-encoded MLT-3 on both Tx+ and Tx– and can be configured through Register 0x0404 (for example, in transformer-less designs).

8.3.12.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125-Mbps serial data stream to synchronous 2-bit wide data that is provided to the RMII.

The receive section consists of the following functional blocks:

1. Input and BLW Compensation
2. Signal Detect
3. Digital Adaptive Equalization
4. MLT-3 to Binary Decoder
5. Clock Recovery Module
6. NRZI to NRZ Decoder
7. Descrambler
8. Serial to Parallel
9. Code-Group Alignment

10. 4B/5B Decoder
11. Link Integrity Monitor
12. Bad SSD Detection

8.3.13 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3-compliant. It includes the receiver, transmitter, collision detection, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

8.3.13.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50 ns. Finally, the signal must again exceed the original squelch level no earlier than 50 ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

8.3.13.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

8.3.13.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83825I output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100 ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be deasserted for approximately 500 ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te mode.

8.3.13.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair can cause polarity errors, and the wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because it uses MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

8.3.14 Loopback Modes

There are several loopback options within the DP83825I that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83825I may be configured to any one of the Near-End Loopback modes or to the Far-End (reverse) Loopback mode. MII Loopback is configured using the Basic Mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

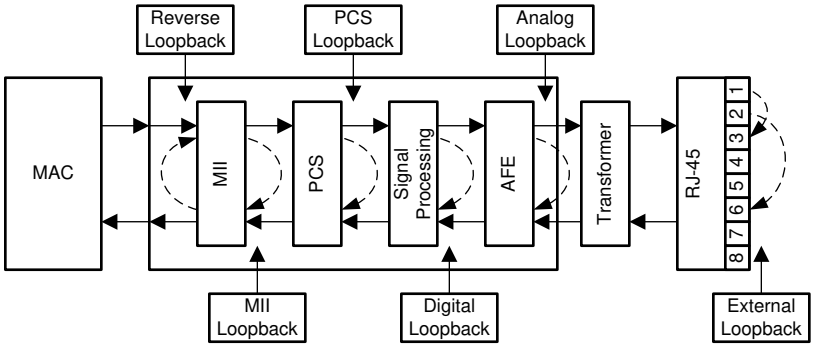


図 14. Loopback Test Modes

8.3.14.1 Near-End Loopback

Near-End Loopback provides the ability to loop the transmitted data back to the receiver through the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits[3:0] in the BISCR register. Auto-Negotiation should be disabled before selecting the Near-End Loopback modes. This constraint does not apply for external-loopback mode.

8.3.14.2 MII Loopback

MII Loopback is the most shallow loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83825I to the RX pins where it can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR and bit[2] in BISCR.

8.3.14.3 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

8.3.14.4 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuitry.

Digital Loopback is enabled by setting bit[2] in the BISCR.

8.3.14.5 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end. Analog Loopback requires 100-Ω terminations across pins #1 and #2, as well as 100-Ω terminations across pins #3 and #6 at the RJ45.

Analog Loopback is enabled by setting bit[3] in the BISCR.

8.3.14.6 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the Link Partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored. It requires 100-Ω terminations across pins #1 and #2.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

8.3.15 BIST Configurations

The DP83825I incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST Packet Length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG Length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This will lock the current value of the BIST errors for reading. Note that setting bit[15] also clears the BIST Error Counter.

8.3.16 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive, and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed require a non-intrusively way to identify and report cable faults. The DP83825I offers Time Domain Reflectometry (TDR) capabilities to detect opens and shorts on the cable.

8.3.16.1 TDR

The DP83825I uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations, in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The DP83825I transmits a test pulse of known amplitude (1 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, connector and from the end of the cable itself. After the pulse transmission, the DP83825I measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1m accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the Link Partner is disconnected – cable is unplugged at the other side
- Link Partner is connected but remains “quiet” (for example, in power down mode)
- TDR could be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Register #1 (CR1, address 0x0009). When a link drops, TDR will automatically execute and store the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170).

8.3.16.2 Fast Link Down Functionality

The DP83825I includes advanced link-down capabilities that support various real-time applications. The link-down mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83825I supports an enhanced link drop mechanism, also called Fast Link Drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference. Fast Link Drop can be enabled in software using register configuration. FLD can be configured using the Control Register #3 (CR3, address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When a link drop occurs, the indication of a particular fault condition can be read from the Fast Link Down Status Register (FLDS, address 0x000F).

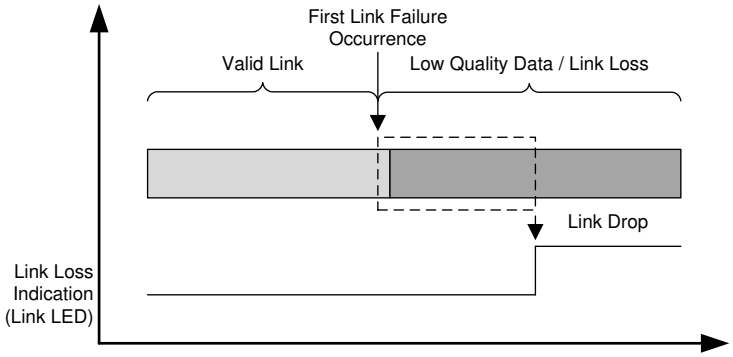


図 15. Fast Link Down

Fast Link Down criteria include:

- RX Error Count - when a predefined number of 32 RX_ERs occur in a 10-µs window, the link will be dropped.
- MLT3 Error Count - when a predefined number of 20 MLT3 errors occur in a 10-µs window, the link will be dropped.
- Low SNR Threshold - when a predefined number of 20 threshold crossings occur in a 10-µs window, the link will be dropped.
- Signal/Energy Loss - when the energy detector indicates energy loss, the link will be dropped.

The Fast Link Down functionality allows the use of each of these options separately or in any combination.

注

Because this mode enables extremely quick reaction time, it is more exposed to temporary bad link-quality scenarios.

8.3.17 Single Voltage Supply

The DP83825I integrates the LDO to generate internal power rails needed for the device

8.4 Device Functional Modes

DP83825I offers modes to optimize cable reach and power consumption. In default mode, it offers a cable reach of 100 meters and above. To achieve a 150-meter cable with the lowest power consumption and Energy Efficient Ethernet, the designer must program a configuration after PHY is out of reset. The following section describes the various modes available and configuration required to achieve these.

- **Default Mode**
  This mode offers a 100+ meters cable reach mode where no additional configuration programming is needed.
- **Power Optimized Mode**
  This mode offers the lowest power consumption along with a cable reach of 130 meters and more. 表 4 shows the required register configuration that is programmed through the MDC/MDIO interface.

Device Functional Modes (continued)

表 4. Configurations for Power Optimized Mode, 130-Meter Cable Reach

Register Address	Value
0x0416	0x1F30
0x040D	0x000D
0x0429	0x0200
0x030B	0x0BC0
0X030C	0x0011
0x033C	0x0001
0X0311	0x0000
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0000
0x001F	0x4000
0x033D	0x8110
0x031B	0x0048

- **Cable Reach Optimized Mode**

  This mode offers a cable reach of 150 meters and more. 表 5 shows the required register configuration that is programmed through the MDC/MDIO interface.

表 5. Configurations for Cable Reach Optimized Mode, 150-Meter Cable Reach

Register Address	Value
0x0416	0x1F30
0x040D	0x000D
0x0429	0x0200
0x030B	0x0BC0
0X030C	0x0011
0x033C	0x0001
0X0311	0x0000
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0080
0x001F	0x4000
0x033D	0x8110
0x031B	0x0048

- **Cable Reach Optimized Mode with EEE**

  Energy Efficient Ethernet (EEE) is disabled by default in the DP83825I. EEE must be enabled through register programming. 表 6 shows the required register configuration that is programmed through the MDC/MDIO interface

表 6. Configurations for EEE

Register Address	Value
0x0416	0x1F30
0x040D	0x000d
0x0429	0x0200
0x030B	0x0BC0
0x30C	0x0011
0x33C	0x0001
0x0311	0x0000

表 6. Configurations for EEE (continued)

Register Address	Value
0x0313	0x06E3
0x033A	0x579C
0x0404	0x0080
0x0130	0x4750
0x0123	0x0800
0x030F	0x0400
0x04D4	0x6633
0x4D5	0x027F
0x4D6	0x01B0
0x4D7	0x01B0
0x031F	0xFC36
0x031C	0x1103
0x0101	0x0882
0x010A	0x2010
0x04CE	0x00FF
0x04CD	0xA5A5
0x0308	0x0982
0x04CF	0x231D
0x04D0	0x0F8F
0x033E	0x861E
0x04D1	0x00C2
0x04D2	0x215B
0x001F	0x4000
0x033D	0x8110
0x031B	0x0048

8.5 Programming

The DP83825I provide IEEE-defined register set for programming and status. It also provides an additional register set to configure other features not supported through IEEE registers.

8.5.1 Straps Configuration

The DP83825 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below. Configuration of the device may be done through the strap pins or through the management register interface. A pullup resistor or a pulldown resistor of suggested values may be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes. The MAC interface pins must support I/O voltages of 3.3 V and 1.8 V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3-V and 1.8-V supplies depending on what voltage was selected for I/O. All strap pins have two levels.

Programming (continued)

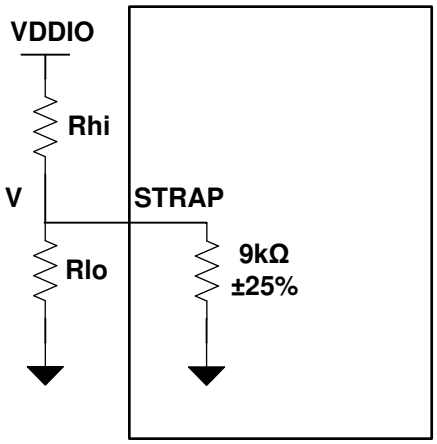


図 16. Strap Circuit

表 7. 2-Level Strap Resistor Ratio

MODE	TARGET VOLTAGE			IDEAL RESISTORS	
	Vmin (V)	Vtyp (V)	Vmax (V)	Rhi (kΩ)	Rlo (kΩ)
0	0		0.35 x VDDIO	OPEN	2.49
1	0.7 x VDDIO		VDDIO	2.49	OPEN

8.5.1.1 Straps for PHY Address

表 8. PHY Address Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_D0	PhyAdd[0]	18	0		PHY_ADD0
				MODE 0	0
				MODE 1	1
CRS_DV	PhyAdd[1]	20	0		PHY_ADD1
				MODE 0	0
				MODE 1	1
PHY Address strap is 2-bit strap on pin 20 and 18 and shall be read as [1:0] respectively as 00 01 10 11. Default PHY Address is 00.					

表 9. RMII MAC Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_D1	Master/Slave	17	0	0	RMII Master Mode
				1	RMII Slave Mode
50MHzOut/LED2	RX_DV_En	2	0	0	Pin 20 is configured as CRS_DV
				1	Pin 20 is configured as RX_DV (For RMII Repeater Mode)

表 10. Auto_Neg Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_ER	A-MDIX	22	0	0	Auto MDIX Enable
				1	Auto MDIX Disable

表 10. Auto_Neg Strap Table (continued)

PIN NAME	STRAP NAME	PIN #	DEFAULT		
LED0	ANeg_Dis	4	0	0	Auto Negotiation Enable
				1	Auto-Negotiation Disable. Force Mode 100M Enabled

8.6 Register Maps

Table 11 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. Device Registers

Offset	Acronym	Register Name	Section
0x0	BMCR_Register		Go
0x1	BMSR_Register		Go
0x2	PHYIDR1_Register		Go
0x3	PHYIDR2_Register		Go
0x4	ANAR_Register		Go
0x5	ALNPAR_Register		Go
0x6	ANER_Register		Go
0x7	ANNPTR_Register		Go
0x8	ANLNPTR_Register		Go
0x9	CR1_Register		Go
0xA	CR2_Register		Go
0xB	CR3_Register		Go
0xC	Register_12		Go
0xD	REGCR_Register		Go
0xE	ADDAR_Register		Go
0xF	FLDS_Register		Go
0x10	PHYSTS_Register		Go
0x11	PHYSCR_Register		Go
0x12	MISR1_Register		Go
0x13	MISR2_Register		Go
0x14	FCSCR_Register		Go
0x15	RECR_Register		Go
0x16	BISCR_Register		Go
0x17	RCSR_Register		Go
0x18	LEDCR_Register		Go
0x19	PHYCR_Register		Go
0x1A	10BTSCR_Register		Go
0x1B	BICSR1_Register		Go
0x1C	BICSR2_Register		Go
0x1E	CDCR_Register		Go
0x1F	PHYRCR_Register		Go
0x25	MLEDCR_Register		Go
0x27	COMPT_Regsiter		Go
0x101	Register_101		Go
0x10A	Register_10a		Go
0x123	Register_123		Go
0x130	Register_130		Go
0x170	CDSCR_Register		Go
0x171	CDSCR2_Register		Go
0x172	TDR_172_Register		Go
0x173	CDSCR3_Register		Go
0x174	TDR_174_Register		Go
0x175	TDR_175_Register		Go

Table 11. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x176	TDR_176_Register		Go
0x177	CDSCR4_Register		Go
0x178	TDR_178_Register		Go
0x180	CDLRR1_Register		Go
0x181	CDLRR2_Register		Go
0x182	CDLRR3_Register		Go
0x183	CDLRR4_Register		Go
0x184	CDLRR5_Register		Go
0x185	CDLAR1_Register		Go
0x186	CDLAR2_Register		Go
0x187	CDLAR3_Register		Go
0x188	CDLAR4_Register		Go
0x189	CDLAR5_Register		Go
0x18A	CDLAR6_Register		Go
0x302	IO_CFG_Register		Go
0x308	SPARE_OUT		Go
0x30B	DAC_CFG_0		Go
0x30C	DAC_CFG_1		Go
0x30F	DSP_CFG_0		Go
0x311	DSP_CFG_2		Go
0x313	DSP_CFG_4		Go
0x31C	DSP_CFG_13		Go
0x31F	DSP_CFG_16		Go
0x33C	DSP_CFG_25		Go
0x33E	DSP_CFG_27		Go
0x404	ANA_LD_PROG_SL_Register		Go
0x40D	ANA_RX10BT_CTRL_Register		Go
0x416	Register_416		Go
0x429	Register_429		Go
0x456	GENCFG_Register		Go
0x460	LEDCFG_Register		Go
0x461	IOCTRL_Register		Go
0x467	SOR1_Register		Go
0x468	SOR2_Register		Go
0x469	Register_0x469_Register		Go
0x4A0	RXFCFG_Register		Go
0x4A1	RXFS_Register		Go
0x4A2	RXFPMD1_Register		Go
0x4A3	RXFPMD2_Register		Go
0x4A4	RXFPMD3_Register		Go
0x4CD	Register_0x4cd		Go
0x4CE	Register_0x4ce		Go
0x4CF	Register_0x4cf		Go
0x4D0	EEECFG2_Register		Go
0x4D1	EEECFG3_Register		Go
0x4D2	Register_0x4d2		Go
0x4D4	Register_0x4d4		Go

Table 11. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x4D5	DSP_100M_STEP_2_Register		Go
0x4D6	DSP_100M_STEP_3_Register		Go
0x4D7	DSP_100M_STEP_4_Register		Go
0x1000	MMD3_PCS_CTRL_1_Register		Go
0x1001	MMD3_PCS_STATUS_1		Go
0x1014	MMD3_EEE_CAPABILITY_Register		Go
0x1016	MMD3_WAKE_ERR_CNT_Register		Go
0x203C	MMD7_EEE_ADVERTISEMENT_Register		Go
0x203D	MMD7_EEE_LP_ABILITY_Register		Go

Complex bit access types are encoded to fit into small table cells. Table 12 shows the codes that are used for access types in this section.

Table 12. Device Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
Write Type		
W	W	Write
W, SC	W	Write
W, STRAP	W	Write
W, STRAP (A-MDIX)	W	Write
W, STRAP (ANEG_Dis)	W	Write
W, STRAP (ANGE_Dis)	W	Write
W, STRAP(Master/Slave)	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 BMCR_Register Register (Offset = 0x0) [reset = 0x3100]

BMCR_Register is shown in Table 13.

Return to Summary Table.

Table 13. BMCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reset	W,SC	0x0	PHY Software Reset: Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared. 0x0 = Normal Operation 0x1 = Initiate software Reset / Reset in Progress

Table 13. BMCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	MII_Loopback	R/W	0x0	MII Loopback: When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally. Applicable for the only available RMII interface. It also needs to set following additional bit BISCR 0x0016[4:0] = 0b00100 for 100Base-TX and BISCR 0x0016[4:0] = 00001b for 10Base-Te 0x0 = Normal Operation 0x1 = MII Loopback enabled
13	Speed_Selection	R/W	0x1	Speed Select: When Auto-Negotiation is disabled (bit [12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected. 0x0 = 10 Mbps 0x1 = 100 Mbps
12	Auto-Negotiation_Enable	R/W,STRAP(ANEG_Dis)	0x1	Auto-Negotiation Enable: 0x0 = Disable Auto-Negotiation - bits [8] and [13] determine the port speed and duplex mode 0x1 = Enable Auto-Negotiation - bits [8] and [13] of this register are ignored when this bit is set
11	IEEE_Power_Down	R/W	0x0	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set. 0x0 = Normal Operation 0x1 = IEEE Power Down
10	Isolate	R/W	0x0	Isolate: 0x0 = Normal Operation 0x1 = Isolates the port from the MII with the exception of the serial management interface. It also disables50MHz clock in RMII Master Mode
9	Restart_Auto-Negotiation	R/W,SC	0x0	Restart Auto-Negotiation: If Auto-Negotiation is disabled (bit [12] = 0), bit [9] is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0x0 = Normal Operation 0x1 = Restarts Auto-Negotiation, Re-initiates the Auto-Negotiation process
8	Duplex_Mode	R/W	0x1	Duplex Mode: When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected. 0x0 = Half-Duplex 0x1 = Full-Duplex
7	Collision_Test	R/W	0x0	Collision Test: When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN. 0x0 = Normal Operation 0x1 = Enable COL Signal Test
6-0	RESERVED	R	0x0	Reserved

8.6.2 BMSR_Register Register (Offset = 0x1) [reset = 0x7849]

BMSR_Register is shown in Table 14.

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Table 14. BMSR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4		0x0	100Base-T4 Capable: This protocol is not available. Always reads as 0.
14	100Base-TX_Full-Duplex		0x1	100Base-TX Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 100Base-TX 0x1 = Device able to perform Full-Duplex 100Base-TX
13	100Base-TX_Half-Duplex		0x1	100Base-TX Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 100Base-TX 0x1 = Device able to perform Half-Duplex 100Base-TX
12	10Base-T_Full-Duplex		0x1	10Base-T Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 10Base-T 0x1 = Device able to perform Full-Duplex 10Base-T
11	10Base-T_Half-Duplex		0x1	10Base-T Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 10Base-T 0x1 = Device able to perform Half-Duplex 10Base-T
10-7	RESERVED	R	0x0	Reserved
6	SMI_Preamble_Suppression		0x1	Preamble Suppression Capable: If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. he device requires minimum of 500ns gap between two transactions, followed by one posedge of MDC and MDIO=1, before starting the next transaction. 0x0 = Device not able to perform management transaction with preambles suppressed 0x1 = Device able to perform management transaction with preamble suppressed
5	Auto-Negotiation_Complete		0x0	Auto-Negotiation Complete: 0x0 = Auto Negotiation process not completed (either still in process, disabled or reset) 0x1 = Auto-Negotiation process completed
4	Remote_Fault	H	0x0	Remote Fault: Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset. 0x0 = No remote fault condition detected 0x1 = Remote fault condition detected
3	Auto-Negotiation_Ability		0x1	Auto-Negotiation Ability: 0x0 = Device is not able to perform Auto-Negotiation 0x1 = Device is able to perform Auto-Negotiation
2	Link_Status		0x0	Link Status: 0x0 = Link not established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps operation)
1	Jabber_Detect	H	0x0	Jabber Detect: 0x0 = No jabber condition detected This bit only has meaning for 10Base-T operation. 0x1 = Jabber condition detected

Table 14. BMSR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Extended_Capability		0x1	Extended Capability: 0x0 = Basic register set capabilities only 0x1 = Extended register capabilities

8.6.3 PHYIDR1_Register Register (Offset = 0x2) [reset = 0x2000]

PHYIDR1_Register is shown in Table 15.

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Table 15. PHYIDR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally_Unique_Identifier_Bits_21:6		0x2000	PHY Identifier Register #1

8.6.4 PHYIDR2_Register Register (Offset = 0x3) [reset = 0xA140]

PHYIDR2_Register is shown in Table 16.

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Table 16. PHYIDR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally_Unique_Identifier_Bits_5:0		0x28	PHY Identifier Register #2
9-4	Model_Number		0x14	Vendor Model Number: The six bits of vendor model number are mapped from bits [9] to [4]
3-0	Revision_Number		0x0	Model Revision Number: Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

8.6.5 ANAR_Register Register (Offset = 0x4) [reset = 0x1E1]

ANAR_Register is shown in Table 17.

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Table 17. ANAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0x0	Next Page Indication: 0x0 = Next Page Transfer not desired 0x1 = Next Page Transfer desired
14	RESERVED	R	0x0	Reserved
13	Remote_Fault	R/W	0x0	Remote Fault: 0x0 = No Remote Fault detected 0x1 = Advertises that this device has detected a Remote Fault. Please note DP83825 does not support Remote Fault. This bit shall not be set by Application
12	RESERVED	R	0x0	Reserved
11	Asymmetric_Pause	R/W	0x0	Asymmetric Pause Support For Full-Duplex Links: 0x0 = Do not advertise asymmetric pause ability 0x1 = Advertise asymmetric pause ability

Table 17. ANAR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	Pause	R/W	0x0	Pause Support for Full-Duplex Links: 0x0 = Do not advertise pause ability 0x1 = Advertise pause ability
9	100Base-T4		0x0	100Base-T4 Support: 0x0 = Do not advertise 100Base-T4 ability 0x1 = Advertise 100Base-T4 ability
8	100Base-TX_Full-Duplex	R/W,STRAP(ANGE_Dis)	0x1	100Base-TX Full-Duplex Support: Values does not matter in forced-mode 0x0 = Do not advertise 100Base-TX Full-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex	R/W,STRAP(ANGE_Dis)	0x1	100Base-TX Half-Duplex Support: Values does not matter in forced-mode 0x0 = Do not advertise 100Base-TX Half-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex	R/W,STRAP(ANGE_Dis)	0x1	10Base-T Full-Duplex Support: Values does not matter in forced-mode 0x0 = Do not advertise 10Base-T Full-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 10Base-T Full-Duplex ability
5	10Base-T_Half-Duplex	R/W,STRAP(ANGE_Dis)	0x1	10Base-T Half-Duplex Support: Values does not matter in forced-mode 0x0 = Do not advertise 10Base-T Half-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 10Base-T Half-Duplex ability
4-0	Selector_Field	R/W	0x1	Protocol Selection Bits: Technology selector field (IEEE802.3u <00001>)

8.6.6 ALNPAR_Register Register (Offset = 0x5) [reset = 0x0]

ALNPAR_Register is shown in Table 18.

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Table 18. ALNPAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page		0x0	Next Page Indication: 0x0 = Link partner does not desire Next Page Transfer 0x1 = Link partner desires Next Page Transfer
14	Acknowledge		0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code word 0x1 = Link partner acknowledges reception of link code word
13	Remote_Fault		0x0	Remote Fault: 0x0 = Link partner does not advertise remote fault event detection 0x1 = Link partner advertises remote fault event detection
12	RESERVED	R	0x0	Reserved

Table 18. ALNPAR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	Asymmetric_Pause		0x0	Asymmetric Pause: 0x0 = Link partner does not advertise asymmetric pause ability 0x1 = Link partner advertises asymmetric pause ability
10	Pause		0x0	Pause: 0x0 = Link partner does not advertise pause ability 0x1 = Link partner advertises pause ability
9	100Base-T4		0x0	100Base-T4 Support: 0x0 = Link partner does not advertise 100Base-T4 ability 0x1 = Link partner advertises 100Base-T4 ability
8	100Base-TX_Full-Duplex		0x0	100Base-TX Full-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Full-Duplex ability 0x1 = Link partner advertises 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex		0x0	100Base-TX Half-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Half-Duplex ability 0x1 = Link partner advertises 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex		0x0	10Base-T Full-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Full-Duplex ability 0x1 = Link partner advertises 10Base-T Full-Duplex ability
5	10Base-T_Half-Duplex		0x0	10Base-T Half-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Half-Duplex ability 0x1 = Link partner advertises 10Base-T Half-Duplex ability
4-0	Selector_Field		0x0	Protocol Selection Bits: Technology selector field (IEEE802.3 <00001>)

8.6.7 ANER_Register Register (Offset = 0x6) [reset = 0x4]

ANER_Register is shown in Table 19.

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Table 19. ANER_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4	Parallel_Detection_Fault	H	0x0	Parallel Detection Fault: 0x0 = No fault detected 0x1 = A fault has been detected during the parallel detection process
3	Link_Partner_Next_Page_Able		0x0	Link Partner Next Page Ability: 0x0 = Link partner is not able to exchange next pages 0x1 = Link partner is able to exchange next pages
2	Local_Device_Next_Page_Able		0x1	Next Page Ability: 0x0 = Local device is not able to exchange next pages 0x1 = Local device is able to exchange next pages

Table 19. ANER_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	Page_Received	H	0x0	Link Code Word Page Received: 0x0 = A new page has not been received 0x1 = A new page has been received
0	Link_Partner_Auto-Negotiation_Able		0x0	Link Partner Auto-Negotiation Ability: 0x0 = Link partner does not support Auto-Negotiation 0x1 = Link partner supports Auto-Negotiation

8.6.8 ANNPTR_Register Register (Offset = 0x7) [reset = 0x2001]

ANNPTR_Register is shown in Table 20.

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Table 20. ANNPTR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	RESERVED	R	0x0	Reserved
13	Message_Page	R/W	0x1	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge_2	R/W	0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle		0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	CODE	R/W	0x1	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.6.9 ANLNPTR_Register Register (Offset = 0x8) [reset = 0x0]

ANLNPTR_Register is shown in Table 21.

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Table 21. ANLNPTR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page		0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	Acknowledge		0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code work 0x1 = Link partner acknowledges reception of link code word
13	Message_Page		0x0	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge_2		0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle		0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	Message/Unformatted_Field		0x0	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.6.10 CR1_Register Register (Offset = 0x9) [reset = 0x0]

CR1_Register is shown in Table 22.

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Table 22. CR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	TDR_Auto-Run	R/W	0x0	TDR Auto-Run at Link Down 0x0 = Disable automatic execution of TDR 0x1 = Enable execution of TDR procedure after link down event
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

Table 22. CR1_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Robust_Auto_MDIX	R/W	0x0	Robust Auto-MDIX: If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. 0x0 = Disable Auto-MDIX 0x1 = Enable Robust Auto-MDIX
4	RESERVED	R	0x0	Reserved
3-2	RESERVED	R	0x0	Reserved
1	Fast_RXDV_Detection	R/W	0x0	Fast RXDV Detection: 0x0 = Disable Fast RX_DV detection. The PHY operates in normal mode. RX_DV assertion after detection of /JK/. 0x1 = Enable assertion high of RX_DV on receive packet due to detection of /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated.
0	RESERVED	R	0x0	Reserved

8.6.11 CR2_Register Register (Offset = 0xA) [reset = 0x0]

CR2_Register is shown in Table 23.

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Table 23. CR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13-7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	Extended_Full-Duplex_Ability	R/W	0x0	Extended Full-Duplex Ability: 0x0 = Diable Extended Full-Duplex Ability. Decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification 0x1 = Enable Full-Duplex while working with link partner in forced 100Base-TX. When the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RX_ER_During_IDLE	R/W	0x0	Detection of Receive Symbol Error During IDLE State: 0x0 = Disable detection of Receive symbol error during IDLE state 0x1 = Enable detection of Receive symbol error during IDLE state
1	Odd-Nibble_Detection_Disable	R/W	0x0	Detection of Transmit Error: 0x0 = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle 0x1 = Disable detection of transmit error in odd-nibble boundary
0	RESERVED	R	0x0	Reserved

8.6.12 CR3_Register Register (Offset = 0xB) [reset = 0x0]

CR3_Register is shown in Table 24.

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Table 24. CR3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	Descrambler_Fast_Link_Down_Mode	R/W	0x0	Descrambler Fast Link Drop: This option can be enabled in parallel to the other fast link down modes in bits [3:0]. 0x0 = Do not drop the link on descrambler link loss 0x1 = Drop the link on descrambler link loss
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	Polarity_Swap	R/W	0x0	Polarity Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [5] high. 0x1 = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0h = Normal polarity
5	MDI/MDIX_Swap	R/W	0x0	MDI/MDIX Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [6] high. 0x0 = MDI pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = Swap MDI pairs (Receive on TD pair, Transmit on RD pair)
4	RESERVED	R	0x0	Reserved
3-0	Fast_Link_Down_Mode	R/W	0x0	Fast Link Down Modes: a) Bit 3 Drop the link based on RX Error count of the MII interface. When a predefined number of 32 RX Error occurences in a 10us interval is reached, the link will be dropped. b) Bit 2 Drop the link based on MLT3 Error count (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in10us interval is reached, the link will be dropped. c) Bit 1 Drop the link based on Low SNR Threshold. When a predefined number of 20 Threshold crossing occurences in a 10us interval is reached, the link will be dropped. d) Bit 0 Drop the link based on Signal/Energy Loss indication. When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10us. The Fast Link Down function is an OR of all 5 options (bits [10] and [3:0]), the designer can enable any combination of these conditions.

8.6.13 Register_12 Register (Offset = 0xC) [reset = 0x0]

Register_12 is shown in Table 25.

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Table 25. Register_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_interrupt		0x0	interrupt for Link quality indication
14	energy_detect_interrupt		0x0	interrupt for energy detect indication
13	link_interrupt		0x0	Interrupt for link status
12	speed_interrupt		0x0	interrupt for speed status
11	duplex_interrupt		0x0	interrupt for duplex

Table 25. Register_12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	auto_negotiation_complete_interrupt		0x0	interrupt for autonegotiation
9	false_carrier_half_full_interrupt		0x0	interrupt for false carrier
8	rhf_interrupt		0x0	interrupt for rhf
7	Link_Quality_interrupt_enable	R/W	0x0	interrupt enable for Link quality indication
6	energy_detect_interrupt_enable	R/W	0x0	interrupt enable for energy detect indication
5	link_interrupt_enable	R/W	0x0	Interrupt enable for link status
4	speed_interrupt_enable	R/W	0x0	interrupt enalble for speed status
3	duplex_interrupt_enable	R/W	0x0	interrupt enable for duplex
2	auto_negotiation_complete_interrupt_enable	R/W	0x0	interrupt enable for autonegotiation
1	false_carrier_half_full_interrupt_enable	R/W	0x0	interrupt enable for false carrier
0	rhf_interrupt_enable	R/W	0x0	interrupt enable for rhf

8.6.14 REGCR_Register Register (Offset = 0xD) [reset = 0x0]

REGCR_Register is shown in Table 26.

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Table 26. REGCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended_Register_Command	R/W	0x0	Extended Register Command: 0x0 = Address 0x1 = Data, no post increment 0x2 = Data, post increment on read and write 0x3 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved
4-0	DEVAD	R/W	0x0	Device Address: Bits [4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the DP83825 uses the vendor specific DEVAD [4:0] = '11111' for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

8.6.15 ADDAR_Register Register (Offset = 0xE) [reset = 0x0]

ADDAR_Register is shown in Table 27.

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Table 27. ADDAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0x0	If REGCR register bits [15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

8.6.16 FLDS_Register Register (Offset = 0xF) [reset = 0x0]

FLDS_Register is shown in Table 28.

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Table 28. FLDS_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Reserved
8-4	Fast_Link_Down_Status	H	0x0	Fast Link Down Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled) 0x1 = Signal/Energy Lost 0x2 = SNR Level 0x4 = MLT3 Errors 0x8 = RX Errors 0x10 = Descrambler Loss Sync
3-0	RESERVED	R	0x0	Reserved

8.6.17 PHYSTS_Register Register (Offset = 0x10) [reset = 0x0]

PHYSTS_Register is shown in Table 29.

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Table 29. PHYSTS_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	MDI/MDIX_Mode		0x0	MDI/MDIX Mode Status: 0x0 = MDI Pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair)
13	Receive_Error_Latch	H	0x0	Receive Error Latch: This bit will be cleared upon a read of the RECR register 0x0 = No receive error event has occurred 0x1 = Receive error event has occurred since last read of RXERCNT register (0x0015)
12	Polarity_Status	H	0x0	Polarity Status: This bit is a duplication of bit [4] in the 10BTSCR register (0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
11	False_Carrier_Sense_Latch	H	0x0	False Carrier Sense Latch: This bit will be cleared upon a read of the FCSR register. 0x0 = No False Carrier event has occurred 0x1 = False Carrier even has occurred since last read of FCSCR register (0x0014)
10	Signal_Detect		0x0	Signal Detect: Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler_Lock		0x0	Descrambler Lock: Active high 100Base-TX Descrambler Lock indication from PMD

Table 29. PHYSTS_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Page_Received		0x0	Link Code Word Page Received: This bit is a duplicate of Page Received (bit [1]) in the ANER register and it is cleared on read of the ANER register (0x0006). 0x0 = Link Code Word Page has not been received 0x1 = A new Link Code Word Page has been received
7	MII_Interrupt	H	0x0	MII Interrupt Pending: Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR will clear this interrupt bit indication. 0x0 = No interrupt pending 0x1 = Indicates that an internal interrupt is pending
6	Remote_Fault		0x0	Remote Fault: Cleared on read of BMSR register (0x0001) or by reset. 0x1 = Remote Fault condition detected. Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation 0h = No Remote Fault condition detected
5	Jabber_Detect		0x0	Jabber Detection: This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No Jabber 0x1 = Jabber condition detected
4	Auto-Negotiation_Status		0x0	Auto-Negotiation Status: 0x0 = Auto-Negotiation not complete 0x1 = Auto-Negotiation complete
3	MII_Loopback_Status		0x0	MII Loopback Status: 0x0 = Normal operation 0x1 = Loopback enabled
2	Duplex_Status		0x0	Duplex Status: 0x0 = Half-Duplex mode 0x1 = Full-Duplex mode
1	Speed_Status		0x0	Speed Status: 0x0 = 100 Mbps mode 0x1 = 10 Mbps mode
0	Link_Status		0x0	Link Status: This bit is duplicated from the Link Status bit in the BMSR register (address 0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No link established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps)

8.6.18 PHYSCR_Register Register (Offset = 0x11) [reset = 0x108]

PHYSCR_Register is shown in Table 30.

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Table 30. PHYSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable_PLL	R/W	0x0	Disable PLL: Note: clock circuitry can be disabled only in IEEE power down mode. 0x0 = Normal operation 0x1 = Disable internal clocks circuitry

Table 30. PHYSCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	Power_Save_Mode_Enable	R/W	0x0	Power Save Mode Enable: 0x0 = Normal operation 0x1 = Enable power save modes
13-12	Power_Save_Modes	R/W	0x0	Power Save Mode: 0x0 = Normal operation mode. PHY is fully functional 0x1 = Reserved 0x2 = Active Sleep, Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected.
11	Scrambler_Bypass	R/W	0x0	Scrambler Bypass: 0x0 = Scrambler bypass disabled 0x1 = Scrambler bypass enabled
10	RESERVED	R	0x0	Reserved
9-8	Loopback_FIFO_Depth	R/W	0x1	Far-End Loopback FIFO Depth: This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles. 0x0 = 4 nibbles FIFO 0x1 = 5 nibbles FIFO 0x2 = 6 nibbles FIFO 0x3 = 8 nibbles FIFO
7-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	Interrupt_Polarity	R/W	0x1	Interrupt Polarity: 0x0 = Steady state (normal operation) is 0 logic and during interrupt is 1 logic 0x1 = Steady state (normal operation) is 1 logic and during interrupt is 0 logic
2	Test_Interrupt	R/W	0x0	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 0x0 = Do not generate interrupt 0x1 = Generate an interrupt
1	Interrupt_Enable	R/W	0x0	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register (0x0012). 0x0 = Disable event based interrupts 0x1 = Enable event based interrupts
0	Interrupt_Output_Enable	R/W	0x0	Interrupt Output Enable: Enable active low interrupt events via the INTR/PWERDN pin by configuring the INTR/PWRDN pin as an output. 0x0 = INTR/PWRDN is a Power Down pin 0x1 = INTR/PWRDN is an interrupt output

8.6.19 MISR1_Register Register (Offset = 0x12) [reset = 0x0]

MISR1_Register is shown in Table 31.

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Table 31. MISR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_Interrupt	H	0x0	Change of Link Quality Status Interrupt: 0x0 = Link quality is Good 0x1 = Change of link quality when link is ON
14	Energy_Detect_Interrupt	H	0x0	Change of Energy Detection Status Interrupt: 0x0 = No change of energy detected 0x1 = Change of energy detected
13	Link_Status_Changed_Interrupt	H	0x0	Change of Link Status Interrupt: 0x0 = No change of link status 0x1 = Change of link status interrupt is pending
12	Speed_Changed_Interrupt	H	0x0	Change of Speed Status Interrupt: 0x0 = No change of speed status 0x1 = Change of speed status interrupt is pending
11	Duplex_Mode_Changed_Interrupt	H	0x0	Change of Duplex Status Interrupt: 0x0 = No change of duplex status 0x1 = Change of duplex status interrupt is pending
10	Auto-Negotiation_Completed_Interrupt	H	0x0	Auto-Negotiation Complete Interrupt: 0x0 = No Auto-Negotiation complete event is pending 0x1 = Auto-Negotiation complete interrupt is pending
9	False_Carrier_Counter_Half-Full_Interrupt	H	0x0	False Carrier Counter Half-Full Interrupt: 0x0 = False Carrier half-full event is not pending 0x1 = False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending
8	Receive_Error_Counter_Half-Full_Interrupt	H	0x0	Receiver Error Counter Half-Full Interrupt: 0x0 = Receive Error half-full event is not pending 0x1 = Receive Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending
7	Link_Quality_Interrupt_Enable	R/W	0x0	Enable interrupt on change of link quality
6	Energy_Detect_Interrupt_Enable	R/W	0x0	Enable interrupt on change of energy detection
5	Link_Status_Changed_Enable	R/W	0x0	Enable interrupt on change of link status
4	Speed_Changed_Interrupt_Enable	R/W	0x0	Enable Interrupt on change of speed status
3	Duplex_Mode_Changed_Interrupt_Enable	R/W	0x0	Enable Interrupt on change of duplex status
2	Auto-Negotiation_Completed_Enable	R/W	0x0	Enable Interrupt on Auto-negotiation complete event
1	False_Carrier_HF_Enable	R/W	0x0	Enable Interrupt on False Carrier Counter Register half-full event
0	Receive_Error_HF_Enable	R/W	0x0	Enable Interrupt on Receive Error Counter Register half-full event

8.6.20 MISR2_Register Register (Offset = 0x13) [reset = 0x0]

MISR2_Register is shown in Table 32.

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Table 32. MISR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EEE_Error_Interrupt	H	0x0	Energy Efficient Ethernet Error Interrupt: 0x0 = EEE error has not occurred 0x1 = EEE error has occurred
14	Auto-Negotiation_Error_Interrupt	H	0x0	Auto-Negotiation Error Interrupt: 0x0 = No Auto-Negotiation error even pending 0x1 = Auto-Negotiation error interrupt is pending
13	Page_Received_Interrupt	H	0x0	Page Receiver Interrupt: 0x0 = Page has not been received 0x1 = Page has been received
12	Loopback_FIFO_OF/UF_Event_Interrupt	H	0x0	Loopback FIFO Overflow/Underflow Event Interrupt: 0x0 = No FIFO Overflow/Underflow event pending 0x1 = FIFO Overflow/Underflow event interrupt pending
11	MDI_Crossover_Change_Interrupt	H	0x0	MDI/MDIX Crossover Status Change Interrupt: 0x0 = MDI crossover status has not changed 0x1 = MDI crossover status changed interrupt is pending
10	Sleep_Mode_Interrupt	H	0x0	Sleep Mode Event Interrupt: 0x0 = No Sleep mode event pending 0x1 = Sleep mode event interrupt is pending
9	Inverted_Polarity_Interrupt__/_WoL_Packet_Received_Interrupt	H	0x0	Inverted Polarity Interrupt / WoL Packet Received Interrupt: 0x0 = No Inverted polarity event pending / No WoL oacket received 0x1 = Inverted Polarity interrupt pending / WoL packet was recieved
8	Jabber_Detect_Interrupt	H	0x0	Jabber Detect Event Interrupt: 0x0 = No Jabber detect event pending 0x1 = Jabber detect even interrupt pending
7	EEE_Error_Interrupt_Enable	R/W	0x0	Enable interrupt on EEE Error
6	Auto-Negotiation_Error_Interrupt_Enable	R/W	0x0	Enable Interrupt on Auto-Negotiation error event
5	Page_Received_Interrupt_Enable	R/W	0x0	Enable Interrupt on page receive event
4	Loopback_FIFO_OF/UF_Enable	R/W	0x0	Enable Interrupt on loopback FIFO Overflow/Underflow event
3	MDI_Crossover_Change_Enable	R/W	0x0	Enable Interrupt on change of MDI/X status
2	Sleep_Mode_Event_Enable	R/W	0x0	Enable Interrupt on sleep mode event
1	Polarity_Changed_/_WoL_Packet_Enable	R/W	0x0	Enable Interrupt on change of polarity status
0	Jabber_Detect_Enable	R/W	0x0	Enable Interrupt on Jabber detection event

8.6.21 FCSCR_Register Register (Offset = 0x14) [reset = 0x0]

FCSCR_Register is shown in Table 33.

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Table 33. FCSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	False_Carrier_Event_Counter		0x0	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

8.6.22 RECR_Register Register (Offset = 0x15) [reset = 0x0]

RECR_Register is shown in Table 34.

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Table 34. RECR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive_Error_Counter		0x0	RX_ER Counter: When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

8.6.23 BISCR_Register Register (Offset = 0x16) [reset = 0x100]

BISCR_Register is shown in Table 35.

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Table 35. BISCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	BIST_Error_Counter_Mode	R/W	0x0	BIST Error Counter Mode: 0x0 = Single mode, when BIST Error Counter reaches its max value, PRBS checker stops counting. 0x1 = Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again.
13	PRBS_Checker_Config	R/W	0x0	PRBS Checker Config:bit[13:12] 0x0 = PRBS Generator and Checker both are disabled 0x1 = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 0x2 = PRBS Generation is disabled. PRBS Checker is Enabled 0x3 = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C

Table 35. BISCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	Packet_Generation_Enable	R/W	0x0	Packet Generation Enable:bit[13:12] 0x0 = PRBS Generator and Checker both are disabled 0x1 = PRBS Generator Enabled, Trasnmit Single Packet with Constant Data as configured in register 0x001C. Checker is disabled 0x2 = PRBS Generation is disabled. PRBS Checker is Enabled 0x3 = PRBS Generator and Checker both enabled. PRBS Generating Continous Packets as configured in register 0x001C
11	PRBS_Checker_Lock/Sync		0x0	PRBS Checker Lock/Sync Indication: 0x0 = PRBS checker is not locked 0x1 = PRBS checker is locked and synced on received bit stream
10	PRBS_Checker_Sync_Loss	H	0x0	PRBS Checker Sync Loss Indication: 0x0 = PRBS checker has not lost sync 0x1 = PRBS checker has lost sync
9	Packet_Generator_Status		0x0	Packet Generation Status Indication: 0x0 = Packet Generator is off 0x1 = Packet Generator is active and generating packets
8	Power_Mode		0x1	Sleep Mode Indication: 0x0 = Indicates that the PHY is in active sleep mode 0x1 = Indicates that the PHY is in normal power mode
7	RESERVED	R	0x0	Reserved
6	Transmit_in_MII_Loopback	R/W	0x0	Transmit Data in MII Loopback Mode (valid only at 100 Mbps) 0x0 = Data is not transmitted to the line in MII loopback 0x1 = Enable transmission of data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit may be set only in MII Loopback mode - setting bit [14] in in BMCR register (0x0000)
5	RESERVED	R	0x0	Reserved
4-0	Loopback_Mode	R/W	0x0	Loopback Mode Select: The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the DP83825 digital and analog data paths 0x1 = PCS Input Loopback (Use for 10Base-Te only) 0x2 = PCS Output Loopback 0x4 = Digital Loopback (Use for 100Base-TX Only) 0x8 = Analog Loopback (requires 100Ω termination) 0x10 = Reverse Loopback

8.6.24 RCSR_Register Register (Offset = 0x17) [reset = 0x1]

RCSR_Register is shown in Table 36.

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Table 36. RCSR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved

Table 36. RCSR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RMII_TX_Clock_Shift	R/W	0x0	RMII TX Clock Shift: Applicable only in RMII Slave Mode 0x0 = Transmit path internal clock shift is disabled 0x1 = Transmit path internal clock shift is enabled
7	RMII_Clock_Select	R/W,STRAP(Master/Slave)	0x0	RMII Reference Clock Select: Strap (Master/Slave) determines the clock reference requirement. 0x0 = 25MHz clock reference, crystal or CMOS-level oscillator 0x1 = 50MHz clock reference, CMOS-level oscillator
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RMII_Revision_Select	R/W	0x0	RMII Revision Select: 0x0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS 0x1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet
3	RMII_Overflow_Status		0x0	RX FIFO Overflow Status: 0x0 = Overflow detected 0x1 = Normal
2	RMII_Underflow_Status		0x0	RX FIFO Underflow Status: 0x0 = Underflow detected 0x1 = Normal
1-0	Receive_Elasticity_Buffer_Size	R/W	0x1	Receive Elasticity Buffer Size: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for ±100ppm), divide the packet lengths by 2). 0x0 = 14 bit tolerance (up to 16800 byte packets) 0x1 = 2 bit tolerance (up to 2400 byte packets) 0x2 = 6 bit tolerance (up to 7200 byte packets) 0x3 = 10 bit tolerance (up to 12000 byte packets)

8.6.25 LEDCR_Register Register (Offset = 0x18) [reset = 0x400]

LEDCR_Register is shown in Table 37.

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Table 37. LEDCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved

Table 37. LEDCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	Blink_Rate	R/W	0x2	LED Blinking Rate (ON/OFF duration): 0x0 = 20Hz (50 ms) 0x1 = 10Hz (100 ms) 0x2 = 5Hz (200 ms) 0x3 = 2Hz (500 ms)
8	RESERVED	R	0x0	Reserved
7	LED_Link_Polarity	R/W	0x0	LED Link Polarity Setting: Link LED polarity defined by strapping value of this pin. This register allows for override of this strap value. 0x0 = Active Low polarity setting 0x1 = Active High polarity setting
6-5	RESERVED	R	0x0	Reserved
4	Drive_Link_LED	R/W	0x0	Drive Link LED Select: 0x0 = Normal operation 0x1 = Drive value of ON/OFF bit [1] onto LED_0 output pin
3-2	RESERVED	R	0x0	Reserved
1	Link_LED_ON/OFF_Setting	R/W	0x0	Value to force on Link LED output
0	RESERVED	R	0x0	Reserved

8.6.26 PHYCR_Register Register (Offset = 0x19) [reset = 0x8000]

PHYCR_Register is shown in Table 38.

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Table 38. PHYCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Auto_MDI/X_Enable	R/W,STRAP(A-MDIX)	0x1	Auto-MDIX Enable: 0x0 = Disable Auto-Negotiation Auto-MDIX capability 0x1 = Enable Auto-Negotiation Auto-MDIX capability
14	Force_MDI/X	R/W	0x0	Force MDIX: 0x0 = Normal operation (Receive on RD pair, Transmit on TD pair) 0x1 = Force MDI pairs to cross (Receive on TD pair, Transmit on RD pair)
13	Pause_RX_Status		0x0	Pause Receive Negotiation Status: Indicates that pause receive should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause_TX_Status		0x0	Pause Transmit Negotiated Status: Indicates that pause should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.

Table 38. PHYCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MII_Link_Status		0x0	MII Link Status: 0x0 = No active 100Base-TX Full-Duplex link, established using Auto-Negotiation 0x1 = 100Base-TX Full-Duplex link is active and it was established using Auto-Negotiation
10-8	RESERVED	R	0x0	Reserved
7	Bypass_LED_Stretching	R/W	0x0	Bypass LED Stretching: Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value. 0x0 = Normal LED operation 0x1 = Bypass LED stretching
6	RESERVED	R	0x0	Reserved
5	LED_Configuration	R/W	0x0	
4-0	PHY_Address	H	0x0	PHY ADDRESS

8.6.27 10BTSCR_Register Register (Offset = 0x1A) [reset = 0x0]

10BTSCR_Register is shown in Table 39.

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Table 39. 10BTSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	Receiver_Threshold_Enable	R/W	0x0	Lower Receiver Threshold Enable: 0x0 = Normal 10Base-T operation 0x1 = Enable 10Base-T lower receiver threshold to allow operation with longer cables
12-9	Squelch	R/W	0x0	Squelch Configuration: Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0x0 = 200mV 0x1 = 250mV 0x2 = 300mV 0x3 = 350mV 0x4 = 400mV 0x5 = 450mV 0x6 = 500mV 0x7 = 550mV 0x8 = 600mV
8	RESERVED	R	0x0	Reserved
7	NLP_Disable	R/W	0x0	NLP Transmission Control: 0x0 = Enable transmission of NLPs 0x1 = Disable transmission of NLPs
6-5	RESERVED	R	0x0	Reserved

Table 39. 10BTSCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	Polarity_Status		0x0	Polarity Status: This bit is a duplication of bit [12] in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
3-1	RESERVED	R	0x0	Reserved
0	Jabber_Disable	R/W	0x0	Jabber Disable: Note: This function is only applicable in 10Base-Te operation. 0x0 = Jabber function enabled 0x1 = Jabber function disabled

8.6.28 BICSR1_Register Register (Offset = 0x1B) [reset = 0x7D]

BICSR1_Register is shown in Table 40.

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Table 40. BICSR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	BIST_Error_Count		0x0	BIST Error Count: Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit [15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) Note: Writing '1' to bit [15] will lock the counter's value for successive read operation and clear the BIST Error Counter.
7-0	BIST_IPG_Length	R/W	0x7D	BIST IPG Length: Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes*4 = 500 bytes). Binary values shall be multiplied by 4 to get the actual IPG length

8.6.29 BICSR2_Register Register (Offset = 0x1C) [reset = 0x5EE]

BICSR2_Register is shown in Table 41.

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Table 41. BICSR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-0	BIST_Packet_Length	R/W	0x5EE	BIST Packet Length: Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5DC, which is equal to 1500 bytes.

8.6.30 CDCR_Register Register (Offset = 0x1E) [reset = 0x0]

CDCR_Register is shown in Table 42.

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Table 42. CDCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Cable_Diagnostic_Start	R/W	0x0	Cable Diagnostic Process Start: Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered. 0x0 = Cable Diagnostic is disabled 0x1 = Start cable measurement
14	cfg_rescal_en	R/W	0x0	Resistor calibration Start
13-2	RESERVED	R	0x0	Reserved
1	Cable_Diagnostic_Status		0x0	Cable Diagnostic Process Done: 0x0 = Cable Diagnostic had not completed 0x1 = Indication that cable measurement process is complete
0	Cable_Diagnostic_Test_Fail		0x0	Cable Diagnostic Process Fail: 0x0 = Cable Diagnostic has not failed 0x1 = Indication that cable measurement process failed

8.6.31 PHYRCR_Register Register (Offset = 0x1F) [reset = 0x0]

PHYRCR_Register is shown in Table 43.

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Table 43. PHYRCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software_Hard_Reset	R/W,SC	0x0	Software Hard Reset: 0x0 = Normal Operation 0x1 = Reset PHY. This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital_reset	R/W,SC	0x0	Software Restart: 0x0 = Normal Operation 0x1 = Restart PHY. This bit is self cleared and resets all PHY circuitry except the registers.
13	RESERVED	R	0x0	Reserved
12-0	RESERVED	R	0x0	Reserved

8.6.32 MLEDCR_Register Register (Offset = 0x25) [reset = 0x41]

MLEDCR_Register is shown in Table 44.

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Table 44. MLEDCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	MLED_Polarity_Swap	R/W	0x0	MLED Polarity Swap: The polarity of MLED depends on the routing configuration and the strap on COL pin. If the pin strap is Pull-Up then polarity is active low. If the pin strap is Pull-Down then polarity is active high.

Table 44. MLEDCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	RESERVED	R	0x0	Reserved
6-3	LED_0_Configuration	R/W	0x8	MLED Configurations: 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = LPI Mode (EEE) 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved
2-1	RESERVED	R	0x0	Reserved
0	cfg_mled_en	R/W	0x1	MLED Route to LED_0: 0x0 = Link status routed to LED_0 0x1 = MLED routed to LED_0

8.6.33 COMPT_Regsiter Register (Offset = 0x27) [reset = 0x0]

COMPT_Regsiter is shown in Table 45.

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Table 45. COMPT_Regsiter Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0x0	Reserved
3-0	Compliance_Test_Configuration	R/W	0x0	Compliance Test Configuration Select: Bit [4] in Register 0x0027 = 1, Enables 10Base-T Test Patterns Bit [4] in Register 0x0428 = 1, Enables 100Base-TX Test Modes Bits [3:0] select the 10Base-T test pattern, as follows: 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10 ') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001 ' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 100Base-TX Test Mode is determined by bits {[5] in register 0x0428, [3:0] in register 0x0027}. The bits determine the number of 0's to follow a '1'. 0,0001 = Single '0' after a '1' 0,0010 = Two '0' after a '1' 0,0011 = Three '0' after a '1' 0,0100 = Four '0' after a '1' 0,0101 = Five '0' after a '1' 0,0110 = Six '0' after a '1' 0,0111 = Seven '0' after a '1' 1,1111 = Thirty one '0' after a '1' 0,0000 = Clears the shift register Note 1: To reconfigure the 100Base-TX Test Mode, bit [4] must be cleared in register 0x0428 and then reset to '1' to configure the new pattern. Note 2: When performing 100Base-TX or 10Base-T tests modes, the speed must be forced using the Basic Mode Control Register (BMCR), address 0x0000.

8.6.34 Register_101 Register (Offset = 0x101) [reset = 0x2082]

Register_101 is shown in Table 46.

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Table 46. Register_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_energy_lost_th_normal	R/W	0x20	DSP_ENERGY_THR_VAL register
7	cfg_dfe_freeze	R/W	0x1	DSP_FRZ_CTRL_REGISTER
6-5	RESERVED	R	0x0	Reserved
4	cfg_seq_wd_off	R/W	0x0	WD_TIMER_CTRL Register
3-1	cfg_ss_bad_mse_tc_sel	R/W	0x1	DSP_100M_MSE_TIMER VAL
0	cfg_use_nrg_det_le_only_as_int	R/W	0x0	DSP_100M_CTRL register

8.6.35 Register_10a Register (Offset = 0x10A) [reset = 0x2040]

Register_10a is shown in Table 47.

Return to Summary Table.

Table 47. Register_10a Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_energy_window_len_normal	R/W	0x20	DSP_100M_ENERGY_VAL Register
7-0	cfg_energy_on_th_normal	R/W	0x40	DSP_ENERGY_THR_VAL register

8.6.36 Register_123 Register (Offset = 0x123) [reset = 0x51C]

Register_123 is shown in Table 48.

Return to Summary Table.

Table 48. Register_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-0	cfg_100m_mse_good2_th	R/W	0x51C	MSE threshold for loop convergence check

8.6.37 Register_130 Register (Offset = 0x130) [reset = 0x4F28]

Register_130 is shown in Table 49.

Return to Summary Table.

Table 49. Register_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-12	cfg_100m_retrain_tc_sel	R/W	0x4	Timer for gain recalibration
11	cfg_retrain_cagc_bypass	R/W	0x1	Enable Gain recalibration
10	cfg_retrain_cagc_gear	R/W	0x1	Gain recalibration step select
9	cfg_energy_lost_usec	R/W	0x1	Trigger select for energy lost
8	cfg_energy_lost_clear_sel	R/W	0x1	Selection for energy lost clr

Table 49. Register_130 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	cfg_seq_wd_sel	R/W	0x28	WD Timer cnt sel

8.6.38 CDSCR_Register Register (Offset = 0x170) [reset = 0x410]

CDSCR_Register is shown in Table 50.

Return to Summary Table.

Table 50. CDSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	Cable_Diagnostic_Cross_Disable	R/W	0x0	Cross TDR Diagnostic Mode: 0x0 = TDR looks for reflections on channel other than the transmit channel configured by 0x170[13] 0x1 = TDR looks for reflections on same channel as transmit channel configured by 0x170[13]
13	cfg_tdr_chan_sel	R/W	0x0	TDR TX channel select: 0x0 = Select channel A as transmit channel. 0x1 = Select channel B as transmit channel.
12	cfg_tdr_dc_rem_no_init	R/W	0x0	To make sure DC removal module is not reset before TDR and dc removal is effective on TDR reflection
11	RESERVED	R	0x0	Reserved
10-8	Cable_Diagnostic_Average_Cycles	R/W	0x4	Number of TDR Cycles to Average: 0x0 = 1 TDR cycle 0x1 = 2 TDR cycles 0x2 = 4 TDR cycles 0x3 = 8 TDR cycles 0x4 = 16 TDR cycles 0x5 = 32 TDR cycles 0x6 = 64 TDR cycles 0x7 = Reserved
7	RESERVED	R	0x0	Reserved
6-4	cfg_tdr_seg_num	R/W	0x1	Selects cable segment on which TDR is to be performed - 000b = Reserved 001b = 0m to 10m 010b = 10m to 20m 011b = 20m to 40m 100b = 40m to 80m 101b = 80m and beyond 110b = Reserved 111b = Reserved
3-0	RESERVED	R	0x0	Reserved

8.6.39 CDSCR2_Register Register (Offset = 0x171) [reset = 0x0]

CDSCR2_Register is shown in Table 51.

Return to Summary Table.

Table 51. CDSCR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.40 TDR_172_Register Register (Offset = 0x172) [reset = 0x0]

TDR_172_Register is shown in Table 52.

Return to Summary Table.

Table 52. TDR_172_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.41 CDSCR3_Register Register (Offset = 0x173) [reset = 0x1304]

CDSCR3_Register is shown in Table 53.

Return to Summary Table.

Table 53. CDSCR3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_tdr_seg_duration	R/W	0x13	Duration of the segment selected for TDR, calculated by - (Length_in_meters*2*5.2)/8 For Segment #1, 8'hD For Segment #2, 8'hD For Segment #3, 8'h1A For Segment #4, 8'h34 For Segment #5, 8'h8F
7-0	cfg_tdr_initial_skip	R/W	0x4	No of samples to be avoided before start of segment configured - For Segment #1, 8'h7 For Segment #2, 8'h14 For Segment #3, 8'h21 For Segment #4, 8'h3B For Segment #5, 8'h6F

8.6.42 TDR_174_Register Register (Offset = 0x174) [reset = 0x0]

TDR_174_Register is shown in Table 54.

Return to Summary Table.

Table 54. TDR_174_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.43 TDR_175_Register Register (Offset = 0x175) [reset = 0x1004]

TDR_175_Register is shown in Table 55.

Return to Summary Table.

Table 55. TDR_175_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-11	cfg_tdr_sdw_avg_loc	R/W	0x2	TDR shadow average location - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h2
10-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3-0	cfg_tdr_fwd_shadow	R/W	0x4	Length of forward shadow for the segment configured (to avoid shadow of a fault peak be seen as another fault peak) - For Segment #1, 4'h4 For Segment #2, 4'h4 For Segment #3, 4'h5 For Segment #4, 4'h8 For Segment #5, 4'hB

8.6.44 TDR_176_Register Register (Offset = 0x176) [reset = 0x5]

TDR_176_Register is shown in Table 56.

Return to Summary Table.

Table 56. TDR_176_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4-0	cfg_tdr_p_loc_thresh_seg	R/W	0x5	

8.6.45 CDSCR4_Register Register (Offset = 0x177) [reset = 0x1E00]

CDSCR4_Register is shown in Table 57.

Return to Summary Table.

Table 57. CDSCR4_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12-8	Short_Cables_Threshold	R/W	0x1E	TH to compensate for strong reflections in short cables
7-0	RESERVED	R	0x0	Reserved

8.6.46 TDR_178_Register Register (Offset = 0x178) [reset = 0x2]

TDR_178_Register is shown in Table 58.

Return to Summary Table.

Table 58. TDR_178_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0x0	Reserved
2-0	cfg_tdr_tx_pulse_width_seg	R/W	0x2	TDR TX Pulse width for Segment - For Segment #1, 3'h2 For Segment #2, 3'h2 For Segment #3, 3'h2 For Segment #4, 3'h2 For Segment #5, 3'h6

8.6.47 CDLRR1_Register Register (Offset = 0x180) [reset = 0x0]

CDLRR1_Register is shown in Table 59.

Return to Summary Table.

Table 59. CDLRR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	TD_Peak_Location_1		0x0	Location of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits need to be translated into distance from the PHY.

8.6.48 CDLRR2_Register Register (Offset = 0x181) [reset = 0x0]

CDLRR2_Register is shown in Table 60.

Return to Summary Table.

Table 60. CDLRR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.49 CDLRR3_Register Register (Offset = 0x182) [reset = 0x0]

CDLRR3_Register is shown in Table 61.

Return to Summary Table.

Table 61. CDLRR3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.50 CDLRR4_Register Register (Offset = 0x183) [reset = 0x0]

CDLRR4_Register is shown in Table 62.

Return to Summary Table.

Table 62. CDLRR4_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.51 CDLRR5_Register Register (Offset = 0x184) [reset = 0x0]

CDLRR5_Register is shown in Table 63.

Return to Summary Table.

Table 63. CDLRR5_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.52 CDLAR1_Register Register (Offset = 0x185) [reset = 0x0]

CDLAR1_Register is shown in Table 64.

Return to Summary Table.

Table 64. CDLAR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0x0	Reserved
6-0	TD_Peak_Amplitude_1		0x0	Amplitude of the First peak discovered by the TDR mechanism on Transmit Channel (TD). The value of these bits is translated into type of cable fault and/or interference.

8.6.53 CDLAR2_Register Register (Offset = 0x186) [reset = 0x0]

CDLAR2_Register is shown in Table 65.

Return to Summary Table.

Table 65. CDLAR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.54 CDLAR3_Register Register (Offset = 0x187) [reset = 0x0]

CDLAR3_Register is shown in Table 66.

Return to Summary Table.

Table 66. CDLAR3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.55 CDLAR4_Register Register (Offset = 0x188) [reset = 0x0]

CDLAR4_Register is shown in Table 67.

Return to Summary Table.

Table 67. CDLAR4_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.56 CDLAR5_Register Register (Offset = 0x189) [reset = 0x0]

CDLAR5_Register is shown in Table 68.

Return to Summary Table.

Table 68. CDLAR5_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.57 CDLAR6_Register Register (Offset = 0x18A) [reset = 0x0]

CDLAR6_Register is shown in Table 69.

Return to Summary Table.

Table 69. CDLAR6_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	TD_Peak_Polarity_1		0x0	Polarity of the First peak discovered by the TDR mechanism on Transmit Channel (TD).
10-6	RESERVED	R	0x0	Reserved
5	Cross_Detect_on_TD		0x0	Cross Reflections were detected on TD. Indicate on Short between TD and TD
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

Table 69. CDLAR6_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved
1-0	RESERVED	R	0x0	Reserved

8.6.58 IO_CFG_Register Register (Offset = 0x302) [reset = 0x0]

IO_CFG_Register is shown in Table 70.

Return to Summary Table.

Table 70. IO_CFG_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MaC_Impedance_Control	R/W	0x0	MAC Impedance Control: MAC interface impedance control sets the series termination for the digital pins. 0x0 = 50 Ohms termination 0x1 = 25 Ohms termination
13	RESERVED	R	0x0	Reserved
12-9	RESERVED	R	0x0	Reserved
12-9	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
15-6	RESERVED	R	0x0	Reserved
6	cfg_clkout25m_off	R/W	0x0	This bit shall be set by Application to reduce the current consumption 0x0 = CLKOUT25 available 0x1 = LED_1_GPIO is available
5-3	RESERVED	R	0x0	Reserved
2-0	Pin2_GPIO_Configuration	R/W	0x0	GPIO Configuration: 0x0 = clkout50m (only in master mode) 0x1 = LED_2 0x2 = WoL 0x3 = 0 0x4 = MDINT 0x5 = 0 0x6 = 1 0x7 = 0
5-0	RESERVED	R	0x0	Reserved

8.6.59 SPARE_OUT Register (Offset = 0x308) [reset = 0x2]

SPARE_OUT is shown in Table 71.

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Table 71. SPARE_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	spare_out	R/W	0x1	Analog Spare Bits Bit 1 - Tied to 1'b1 to act as revision ID Bit 2 - cfg_rmii_rx_clk_sel Bit 4 - Freeze all loops when rx_is_dis is high Bit 5: Bypass MSE checker in LPI_WAKE state Bit 6 - Enable freeze in STEADY_STATE before entering LPI_FREEZE Bit 7: Enable counter based Freeze mechanism for LPI Freeze cycle Bit 8: Choose tmer of 176us/192us for the Counter based Freeze during LPI refresh cycle Bit 10 - Freeze fagc in LPI_WAIT Bit 11 - Freeze ffe in LPI_WAIT Bit 12 - Freeze dfe in LPI_WAIT Bit 13 - Freeze kp loop in LPI_WAIT Bit 14 - Freeze kf loop in LPI_WAIT Bit 15 - Freeze dc removal in LPI_WAIT
0	cfg_clkout_25m_off_status		0x0	This bit is applicable in DP83825 only. And is only RO 0x0 = CLKOUT25 available 0x1 = LED_1_GPIO is available and is controlled by digpad3_3_gpio_ctrl

8.6.60 DAC_CFG_0 Register (Offset = 0x30B) [reset = 0xC00]

DAC_CFG_0 is shown in Table 72.

Return to Summary Table.

Table 72. DAC_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-6	cfg_dac_minus_one_val	R/W	0x30	LD data for mlt3 encoded data of minus one
5-0	cfg_dac_zero_val	R/W	0x0	LD data for mlt3 encoded data of zero

8.6.61 DAC_CFG_1 Register (Offset = 0x30C) [reset = 0x20]

DAC_CFG_1 is shown in Table 73.

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Table 73. DAC_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0x0	Reserved
5-0	cfg_dac_plus_one_val	R/W	0x20	LD data for mlt3 encoded data of plus one

8.6.62 DSP_CFG_0 Register (Offset = 0x30F) [reset = 0x464]

DSP_CFG_0 is shown in Table 74.

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Table 74. DSP_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-8	cfg_100m_ffe1_tc_sel	R/W	0x4	Timer for FFE_1 State
7	cfg_ffe1_freeze	R/W	0x0	Freeze FFE option in FFE_1 State. 1 -> Freeze.

Table 74. DSP_CFG_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	cfg_ffe2_freeze	R/W	0x1	Freeze FFE option in FFE_2 State. 1 -> Freeze.
5	cfg_ffe3_freeze	R/W	0x1	Freeze FFE option in FFE_3 State. 1 -> Freeze.
4-2	cfg_deq_thr_check_en	R/W	0x1	Enable bits for different metric checks during DEQ sweep. cfg_deq_thr_check_en[0] -> Enables DFE Coeff thr check. cfg_deq_thr_check_en[1] -> Enables MSE thr check. cfg_deq_thr_check_en[2] -> Enables pre-cursor value thr check.
1	cfg_tloop_freqacc_clr_deq sweep	R/W	0x0	Option to re-initialize tloop freq acc during DEQ sweep iterations.
0	cfg_dfe_reset_deqsweep	R/W	0x0	Option to reset DFE Coeff during DEQ sweep iterations.

8.6.63 DSP_CFG_2 Register (Offset = 0x311) [reset = 0x1FC]

DSP_CFG_2 is shown in Table 75.

Return to Summary Table.

Table 75. DSP_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	cfg_cagc_gain_mapping_ sel	R/W	0x0	Option to select different combinations of BPF, PGA gain by CAGC. 0 -> default option. Other options are 1 and 2. (There are only 3 options.)
13	cfg_deq_coeff_sel	R/W	0x0	Equalization mode ctrl register 0x0 = Optimal Coefficients for less pre-cursor. 0x1 = DEQ Coefficients from Table 2 (LS)
12-9	RESERVED	R	0x0	Reserved
8-1	cfg_deq_coeff_0_val_1	R/W	0xFE	Equalization Force coefficient_0 Value for CabeLength < 75m
0	RESERVED	R	0x0	Reserved

8.6.64 DSP_CFG_4 Register (Offset = 0x313) [reset = 0x6F8]

DSP_CFG_4 is shown in Table 76.

Return to Summary Table.

Table 76. DSP_CFG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_deq_coeff_0_val_4	R/W	0x6	Equalization Force coefficient_0 Value for CabeLength >130m
7-0	cfg_deq_coeff_1_val_1	R/W	0xF8	Equalization Force coefficient_1 Value for CabeLength < 75m

8.6.65 DSP_CFG_13 Register (Offset = 0x31C) [reset = 0x1101]

DSP_CFG_13 is shown in Table 77.

Return to Summary Table.

Table 77. DSP_CFG_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_kp_force_en	R/W	0x0	Enable forcing of timing loop prop arm gain
14	cfg_kf_force_en	R/W	0x0	Enable forcing of timing loop integral arm gain
13-11	cfg_kp_force_val	R/W	0x2	Value to force for timing loop prop arm gain
10-7	cfg_kf_force_val	R/W	0x2	Value to force for timing loop integral arm gain

Table 77. DSP_CFG_13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	cfg_kp_freeze_en	R/W	0x0	Enable to freeze prop arm
5	cfg_kp_freeze_val	R/W	0x0	Value to freeze prop arm. 0x0 = unfreeze 0x1 = freeze;
4	cfg_kf_freeze_en	R/W	0x0	Enable to freeze integral arm
3	cfg_kf_freeze_val	R/W	0x0	Value to freeze integral arm. 0x0 = unfreeze 0x1 = freeze
2	cfg_pd_pol	R/W	0x0	TED polarity inversion
1	cfg_energy_det_in_sel	R/W	0x0	Option to select input for Energy Calc. 0x0 = Slicer inp (default) 0x1 = ADC out (no DC)
0	cfg_compute_pre_cursor_metric_en	R/W	0x1	Enable pre cursor metric calculation

8.6.66 DSP_CFG_16 Register (Offset = 0x31F) [reset = 0xFC36]

DSP_CFG_16 is shown in Table 78.

Return to Summary Table.

Table 78. DSP_CFG_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	cfg_100m_frz_frz	R/W	0x1F	Freeze cmd at Seq State : LPI_FREEZE by groups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
10-6	cfg_100m_wake_frz	R/W	0x10	Freeze cmd at Seq State : LPI_Wake, by groups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
5-1	cfg_100m_flush_frz	R/W	0x1B	Freeze cmd at Seq State : LPI_Wake, by groups: [4] FFE [3] Tloop_Kf [2] Tloop_Kp [1] dfe [0] Fagc,ffe,mse
0	RESERVED	R	0x0	Reserved

8.6.67 DSP_CFG_25 Register (Offset = 0x33C) [reset = 0xEC00]

DSP_CFG_25 is shown in Table 79.

Return to Summary Table.

Table 79. DSP_CFG_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	deq_coeff_1		0xEC	Reserved
7	RESERVED	R	0x0	Reserved
6-0	cfg_deq_coeff_force	R/W	0x0	EQUALIZATION_FRC_CTRL REGISTER

8.6.68 DSP_CFG_27 Register (Offset = 0x33E) [reset = 0x261E]

DSP_CFG_27 is shown in Table 80.

Return to Summary Table.

Table 80. DSP_CFG_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	cfg_wait_lpi_el_dis	R/W	0x0	EEE_WAKE_CTRL register
14-13	cfg_dfe_coeff_lim_sel	R/W	0x1	Enable limit on the max limit of dfe coefficient
12-8	cfg_dfe_coeff_lim_val	R/W	0x6	Limit value for dfe coefficeint
7	cfg_wait_lpi_ed_dis		0x0	EEE_WAKE_CTRL register
6	cfg_mse_th_scaled_en	R/W	0x0	Enable scaling of mse threshold based on PGA gain for DEQ sweep
5	cfg_dfe_th_scaled_en	R/W	0x0	Enable scaling of dfe threshold based on PGA gain for DEQ sweep
4-0	cfg_dfe_mse_th_offset	R/W	0x1E	Offset to be added to PGA attenuation level used for scaling of mse and dfe thresholds

8.6.69 ANA_LD_PROG_SL_Register Register (Offset = 0x404) [reset = 0x80]

ANA_LD_PROG_SL_Register is shown in Table 81.

Return to Summary Table.

Table 81. ANA_LD_PROG_SL_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ld_prog_sl	R/W	0x80	<15:12> ld_bias <11:8> cm_control: debug mode for changing output common mode <7:5> iq_control: ld power consumption - 000-12.7mA; 100:15.7mA; 111:19.5mA <4:0> unused <0>ld_burnin_mode

8.6.70 ANA_RX10BT_CTRL_Register Register (Offset = 0x40D) [reset = 0x0]

ANA_RX10BT_CTRL_Register is shown in Table 82.

Return to Summary Table.

Table 82. ANA_RX10BT_CTRL_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4-0	rx10bt_comp_sl	R/W	0x0	10B-T current Gain, common for both POS and NEG, Starting from 200mV to 575mV, step size of 25mV PG1.1 change : Bit 3 is internally inverted

8.6.71 Register_416 Register (Offset = 0x416) [reset = 0x830]

Register_416 is shown in Table 83.

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Table 83. Register_416 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	hpf_cal_force_ctrl	R/W	0x0	ANA RX PATH CTRL REGISTER
11-8	hpf_cal_sl	R/W	0x8	Reserved
7	hpf_gain_force_ctrl	R/W	0x0	ANA RX PATH CTRL REGISTER

Table 83. Register_416 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0x0	Reserved
5-4	hpf_gain_sl	R/W	0x3	ANA RX PATH CTRL REGISTER
3-2	RESERVED	R	0x0	Reserved
1	hpf_en_force_ctrl	R/W	0x0	ANA RX PATH CTRL REGISTER
0	hpf_en_sl	R/W	0x0	ANA RX PATH CTRL REGISTER

8.6.72 Register_429 Register (Offset = 0x429) [reset = 0x0]

Register_429 is shown in Table 84.

Return to Summary Table.

Table 84. Register_429 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	top_prog_vbgbyr_control	R/W	0x0	IVBGR_CTRL register
7-0	RESERVED	R	0x0	Reserved

8.6.73 GENCFG_Register Register (Offset = 0x456) [reset = 0x8]

GENCFG_Register is shown in Table 85.

Return to Summary Table.

Table 85. GENCFG_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0x0	Reserved
3	Min_IPG_Enable	R/W	0x1	Min IPG Enable: 0x0 = IPG set to 0.20µs 0x1 = Enable Minimum Interpacket Gap (IPG is set to 120ns instead of 0.20µs)
2-0	RESERVED	R	0x0	Reserved

8.6.74 LEDCFG_Register Register (Offset = 0x460) [reset = 0x10]

LEDCFG_Register is shown in Table 86.

Return to Summary Table.

Table 86. LEDCFG_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-8	RESERVED	R	0x0	Reserved

Table 86. LEDCFG_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	LED_2_Control	R/W	0x1	LED_2 Control:Selects the source for LED_1. 0x0 = LINK OK 0x1 = RX/TX Activity 0x2 = TX Activity 0x3 = RX Activity 0x4 = Collision 0x5 = Speed, High for 100BASE-TX 0x6 = Speed, High for 10BASE-T 0x7 = Full-Duplex 0x8 = LINK OK / BLINK on TX/RX Activity 0x9 = Active Stretch Signal 0xA = MII LINK (100BT+FD) 0xB = LPI Mode (Energy Efficient Ethernet) 0xC = TX/RX MII Error 0xD = Link Lost (remains on until register 0x0001 is read) 0xE = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 0xF = Reserved
3-0	RESERVED	R	0x0	Reserved

8.6.75 IOCTRL_Register Register (Offset = 0x461) [reset = 0x0]

IOCTRL_Register is shown in Table 87.

Return to Summary Table.

Table 87. IOCTRL_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13-12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10-7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R	0x0	Reserved
4-0	RESERVED	R	0x0	Reserved

8.6.76 SOR1_Register Register (Offset = 0x467) [reset = 0x101]

SOR1_Register is shown in Table 88.

Return to Summary Table.

Table 88. SOR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	CRS_DV/RX_DV		0x0	Reserved
13	CFG_PHY_AD_1		0x0	Latched Value of PhyAddress[1]

Table 88. SOR1_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CFG_PHY_AD_0		0x0	Latched Value of PhyAddress[0]
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	CFG_AMDIX		0x1	1 = Auto MDI 0 = Manual MDI
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	CFG_RMII_Master/Slave		0x0	0 = RMII Master : 25MHz clock reference at XI 1 = RMII Slave : 50MHz clock reference at XI
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	Autonegotiation_enable		0x1	1: Auto Neg Enable 0: Auto Neg Disable

8.6.77 SOR2_Register Register (Offset = 0x468) [reset = 0x80]

SOR2_Register is shown in Table 89.

Return to Summary Table.

Table 89. SOR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	CRS_DV_vs_RX_DV		0x0	
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	CFG_LED_LINK_POL		0x1	1 = LED_LINK is active high 0 = LED_LINK is active low
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

8.6.78 Register_0x469_Register Register (Offset = 0x469) [reset = 0x40]

Register_0x469_Register is shown in Table 90.

Return to Summary Table.

Table 90. Register_0x469_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	led_2_polarity	R/W	0x1	led 2 polarity 0x0 = active low, 0x1 = active high
5	led_2_drv_val	R/W	0x0	led 2 drive value
4	led_2_drv_en	R/W	0x0	led 2 drive enable 0x0 = Normal operation 0x1 = drive LED polarity,
3	RESERVED	R	0x0	Reserved
2	led_1_polarity	R/W,STRAP	0x0	led 1 polarity 0x0 = active low, 0x1 = active high
1	led_1_drv_val	R/W	0x0	led1 drive value
0	led_1_drv_en	R/W	0x0	led 1 drive enable 0x0 = Normal operation 0x1 = drive LED polarity,

8.6.79 RXFCFG_Register Register (Offset = 0x4A0) [reset = 0x1081]

RXFCFG_Register is shown in Table 91.

Return to Summary Table.

Table 91. RXFCFG_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	CRC_Gate	R/W	0x1	CRC Gate: If Magic Packet has Bad CRC there will be no indication (status, interrupt, GPIO) when enabled. 0x0 = Bad CRC does not gate Magic Packet or Pattern Indications 0x1 = Bad CRC gates Magic Packet and Pattern Indications
11	WoL_Level_Change_Indication_Clear	W,SC	0x0	WoL Level Change Indication Clear: If WoL Indication is set for Level change mode, this bit clears the level upon a write. 0x0 = Clear

Table 91. RXFCFG_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	WoL_Pulse_Indication_Select	R/W	0x0	WoL Pulse Indication Select: Only valid when WoL Indication is set for Pulse mode. 0x0 = 8 clock cycles (of 125MHz clock) 0x1 = 16 clock cycles 0x2 = 32 clock cycles 0x3 = 64 clock cycles
8	WoL_Indication_Select	R/W	0x0	WoL Indication Select: 0x0 = Pulse mode 0x1 = Level change mode
7	WoL_Enable	R/W	0x1	WoL Enable: 0x0 = normal operation 0x1 = Enable Wake-on-LAN (WoL)
6	Bit_Mask_Flag	R/W	0x0	Bit Mask Flag
5	Secure-ON_Enable	R/W	0x0	Enable Secure-ON password for Magic Packets
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	WoL_Magic_Packet_Enable	R/W,STRAP	0x1	Enable Interrupt upon reception of Magic Packet

8.6.80 RXFS_Register Register (Offset = 0x4A1) [reset = 0x1000]

RXFS_Register is shown in Table 92.

Return to Summary Table.

Table 92. RXFS_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	WoL_Interrupt_Source	R/W	0x1	WoL Interrupt Source: Source of Interrupt for bit [1] of register 0x0013. When enabling WoL, this bit is automatically set to WoL Interrupt. 0x0 = Data Polarity Interrupt 0x1 = WoL Interrupt
11-8	RESERVED	R	0x0	Reserved
7	SFD_Error	H	0x0	SFD Error: 0x0 = No SFD error 0x1 = Packet with SFD error (without the SFD byte indicated in bit [13] register 0x04A0)
6	Bad_CRC	H	0x0	Bad CRC: 0x0 = No bad CRC received 0x1 = Bad CRC was received
5	Secure-On_Hack_Flag	H	0x0	Secure-ON Hack Flag: 0x0 = Valid Secure-ON Password 0x1 = Invalid Password detected in Magic Packet

Table 92. RXFS_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	WoL_Magic_Packet_Status	H	0x0	WoL Magic Packet Status:

8.6.81 RXFPMD1_Register Register (Offset = 0x4A2) [reset = 0x0]

RXFPMD1_Register is shown in Table 93.

Return to Summary Table.

Table 93. RXFPMD1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_4	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_5__MSB	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

8.6.82 RXFPMD2_Register Register (Offset = 0x4A3) [reset = 0x0]

RXFPMD2_Register is shown in Table 94.

Return to Summary Table.

Table 94. RXFPMD2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_2	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_3	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

8.6.83 RXFPMD3_Register Register (Offset = 0x4A4) [reset = 0x0]

RXFPMD3_Register is shown in Table 95.

Return to Summary Table.

Table 95. RXFPMD3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC_Destination_Address_Byte_0	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address
7-0	MAC_Destination_Address_Byte_1	R/W	0x0	Perfect Match Data: Configured for MAC Destination Address

8.6.84 Register_0x4cd Register (Offset = 0x4CD) [reset = 0x408]

Register_0x4cd is shown in Table 96.

Return to Summary Table.

Table 96. Register_0x4cd Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	cfg_lpi_energy_lost_th	R/W	0x4	CFG_EEE_ENERGY_CTRL register

Table 96. Register_0x4cd Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	cfg_lpi_energy_on_th	R/W	0x8	CFG_EEE_ENERGY_CTRL register

8.6.85 Register_0x4ce Register (Offset = 0x4CE) [reset = 0x12]

Register_0x4ce is shown in Table 97.

Return to Summary Table.

Table 97. Register_0x4ce Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	cfg_lpi_energy_window_len	R/W	0x12	CFG_EEE_ENERGY_CTRL register

8.6.86 Register_0x4cf Register (Offset = 0x4CF) [reset = 0x261D]

Register_0x4cf is shown in Table 98.

Return to Summary Table.

Table 98. Register_0x4cf Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	cfg_sd_on_win_len	R/W	0x2	EEE_WAKE_CTRL register
11-8	cfg_100m_tloop_kf_step_ss	R/W	0x6	DSP100M_TLOOP_CTRL register
7-4	cfg_sd_on_thr_100m	R/W	0x1	Reserved
3	cfg_100m_use_sd_en	R/W	0x1	Reserved
2	cfg_sd_cnt_level	R/W	0x1	Reserved
1	cfg_en_zc_cnt	R/W	0x0	Reserved
0	cfg_en_cmp_cnt	R/W	0x1	Reserved

8.6.87 EEECFG2_Register Register (Offset = 0x4D0) [reset = 0x0]

EEECFG2_Register is shown in Table 99.

Return to Summary Table.

Table 99. EEECFG2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13-7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R	0x0	Reserved
4-0	RESERVED	R	0x0	Reserved

8.6.88 EEECFG3_Register Register (Offset = 0x4D1) [reset = 0x18B]

EEECFG3_Register is shown in Table 100.

Return to Summary Table.

Table 100. EEECFG3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-13	Force_EEE_Enable	R/W	0x0	Force EEE: Note: Both Link Partners need to be configured to Force EEE. 0x0 = EEE Force Mode OFF 0x1 = Reserved0 0x2 = Reserved1 0x3 = EEE Forced LPI Enabled
12	Force_LPI_Request_TX	R/W	0x0	Force LPI Request TX: This bit shall be set after setting bits [14:13] to EEE Force LPI Enabled. 0x0 = normal operation 0x1 = Force LPI request on transmit enabled
11	RESERVED	R	0x0	Reserved
10	cfg_dis_lpi_bypass_rvrs_loop	R/W	0x0	Energy Efficient Ethernet Configuration Register #3
9	cfg_dis_lpi_bypass_fifo	R/W	0x0	Energy Efficient Ethernet Configuration Register #3
8	cfg_100m_en_lpi_wake_fallback	R/W	0x1	Energy Efficient Ethernet Configuration Register #3
7-4	cfg_lpi_mse_timer_tc_val	R/W	0x8	Energy Efficient Ethernet Configuration Register #3
3	EEE_Capabilities_Bypass	R/W	0x1	EEE Advertise Option: Allow for EEE Advertisment during Auto-Negotiation to be determined by bit [0] in register 0x04D1 rather than the Next Page Registers (Register 0x003C and Register 0x003D in MMD7). 0x0 = Registers in MMD3 and MMD7 determine EEE Auto-Negotiation Abilities 0x1 = Bit [0] determines EEE Auto-Negotiation Abilities
2	EEE_Next_Page_Disable	R/W	0x0	EEE Next Page Disable: 0x0 = Reception of EEE Next Pages is enabled 0x1 = Reception of EEE Next Pages is disabled
1	EEE_RX_Path_Shutdown	R/W	0x1	EEE RX Path Shutdown: 0x0 = Analog RX path is active during LPI_Quiet 0x1 = Enable shutdown of Analog RX path at LPI_Quiet
0	EEE_Capabilities_Enable		0x1	EEE Capabilities Disable 0x0 = PHY does not support EEE (Register 0x0014 in MMD3, Register 0x003C and Register 0x003D in MMD7 are ignored) 0x1 = PHY support EEE capability, Auto-Negotiation will negotiate to EEE as defined by Register 0x003C and Register 0x003D in MMD7.

8.6.89 Register_0x4d2 Register (Offset = 0x4D2) [reset = 0x354A]

Register_0x4d2 is shown in Table 101.

Return to Summary Table.

Table 101. Register_0x4d2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	cfg_flush_ph_shift_updn	R/W	0x0	PI_CTRL Register
13	cfg_ph_shift_toggle_en	R/W	0x1	PI_CTRL Register
12	cfg_fast_slave_wake_100	R/W	0x1	DSP_100M_EEE_LINK CTRL register
11	cfg_dis_dscr_100_tout	R/W	0x0	DSP_100M_EEE_LINK CTRL register
10	cfg_lpi_pre_flush_en	R/W	0x1	DSP_EEE_SEQ CTRL register
9-5	cfg_100m_rx_lpi_ts_timer	R/W	0xA	DSP_100M_EEE_LINK CTRL register
4-0	cfg_100m_rx_lpi_link_fail	R/W	0xA	DSP_100M_EEE_LINK CTRL register

8.6.90 Register_0x4d4 Register (Offset = 0x4D4) [reset = 0x6633]

Register_0x4d4 is shown in Table 102.

Return to Summary Table.

Table 102. Register_0x4d4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-12	cfg_100m_tloop_kp_step_1	R/W	0x6	DSP_100M_STEP_1_Register
11	RESERVED	R	0x0	Reserved
10-8	cfg_100m_tloop_kp_step_0	R/W	0x6	DSP_100M_STEP_0_Register
7	RESERVED	R	0x0	Reserved
6-4	cfg_100m_tloop_kf_step_1	R/W	0x3	DSP_100M_STEP_1_Register
3	RESERVED	R	0x0	Reserved
2-0	cfg_100m_tloop_kf_step_0	R/W	0x3	DSP_100M_STEP_0_Register

8.6.91 DSP_100M_STEP_2_Register Register (Offset = 0x4D5) [reset = 0x2F1]

DSP_100M_STEP_2_Register is shown in Table 103.

Return to Summary Table.

Table 103. DSP_100M_STEP_2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9-7	cfg_100m_tloop_kp_step_2	R/W	0x5	DSP_100M_STEP_2 Register
6-4	cfg_100m_tloop_kf_step_2	R/W	0x7	DSP_100M_STEP_2 Register
3-2	cfg_100m_mse_step_2	R/W	0x0	DSP_100M_STEP_2 Register
1	cfg_100m_dfe_step_2	R/W	0x0	DSP_100M_STEP_2 Register
0	cfg_100m_fagc_step_2	R/W	0x1	DSP_100M_STEP_2 Register

8.6.92 DSP_100M_STEP_3_Register Register (Offset = 0x4D6) [reset = 0x171]

DSP_100M_STEP_3_Register is shown in Table 104.

Return to Summary Table.

Table 104. DSP_100M_STEP_3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9-7	cfg_100m_tloop_kp_step_3	R/W	0x2	DSP_100M_STEP_3 Register
6-4	cfg_100m_tloop_kf_step_3	R/W	0x7	DSP_100M_STEP_3 Register
3-2	cfg_100m_mse_step_3	R/W	0x0	DSP_100M_STEP_3 Register
1	cfg_100m_dfe_step_3	R/W	0x0	DSP_100M_STEP_3 Register
0	cfg_100m_fagc_step_3	R/W	0x1	DSP_100M_STEP_3 Register

8.6.93 DSP_100M_STEP_4_Register Register (Offset = 0x4D7) [reset = 0x171]

DSP_100M_STEP_4_Register is shown in Table 105.

Return to Summary Table.

Table 105. DSP_100M_STEP_4_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9-7	cfg_100m_tloop_kp_step_4	R/W	0x2	DSP_100M_STEP_4 Register
6-4	cfg_100m_tloop_kf_step_4	R/W	0x7	DSP_100M_STEP_4 Register
3-2	cfg_100m_mse_step_4	R/W	0x0	DSP_100M_STEP_4 Register
1	cfg_100m_dfe_step_4	R/W	0x0	DSP_100M_STEP_4 Register
0	cfg_100m_fagc_step_4	R/W	0x1	DSP_100M_STEP_4 Register

8.6.94 MMD3_PCS_CTRL_1_Register Register (Offset = 0x1000) [reset = 0x0]

MMD3_PCS_CTRL_1_Register is shown in Table 106.

Return to Summary Table.

Table 106. MMD3_PCS_CTRL_1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS_Reset	R/W,SC	0x0	PCS Reset: Reset clears MMD3, MMD7 and PCS registers. Reset does not clear Vendor Specific Registers (DEVAD = 31). 0x0 = Normal operation 0x1 = Soft Reset of MMD3, MMD7 and PCS registers
14-11	RESERVED	R	0x0	Reserved
10	RX_Clock_Stoppable	R/W	0x0	RX Clock Stoppable: 0x0 = Receive Clock not stoppable 0x1 = Receive Clock stoppable during LPI
9-0	RESERVED	R	0x0	Reserved

8.6.95 MMD3_PCS_STATUS_1 Register (Offset = 0x1001) [reset = 0x40]

MMD3_PCS_STATUS_1 is shown in Table 107.

Return to Summary Table.

Table 107. MMD3_PCS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	TX_LPI_Received		0x0	TX LPI Received: 0x0 = LPI not received 0x1 = TX PCS has received LPI
10	RX_LPI_Received		0x0	RX LPI Received: 0x0 = LPI not received 0x1 = RX PCS has received LPI
9	TX_LPI_Indication		0x0	TX LPI Indication: 0x0 = TX PCS is not currently receiving LPI 0x1 = TX PCS is currently receiving LPI
8	RX_LPI_Indication		0x0	RX LPI Indication: 0x0 = RX PCS is not currenly receiving LPI 0x1 = RX PCS is currently receiving LPI
7	RESERVED	R	0x0	Reserved
6	TX_Clock_Stoppable		0x1	TX Clock Stoppable: 0x0 = TX Clock is not stoppable 0x1 = MAC may stop clock during LPI
5-0	RESERVED	R	0x0	Reserved

8.6.96 MMD3_EEE_CAPABILITY_Register Register (Offset = 0x1014) [reset = 0x2]

MMD3_EEE_CAPABILITY_Register is shown in Table 108.

Return to Summary Table.

Table 108. MMD3_EEE_CAPABILITY_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0x0	Reserved
2	EEE_1Gbps_Enable		0x0	EEE 1Gbps Enable: 0x0 = EEE is not supported for 1000Base-T 0x1 = EEE is supported for 1000Base-T
1	EEE_100Mbps_Enable		0x1	EEE 100Mbps Enable: 0x0 = EEE is not supported for 100Base-TX 0x1 = EEE is supported for 100Base-TX
0	RESERVED	R	0x0	Reserved

8.6.97 MMD3_WAKE_ERR_CNT_Register Register (Offset = 0x1016) [reset = 0x0]

MMD3_WAKE_ERR_CNT_Register is shown in Table 109.

Return to Summary Table.

Table 109. MMD3_WAKE_ERR_CNT_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	EEE_Wake_Error_Counter		0x0	EEE Wake Error Counter: This register counts the wake time faults where the PHY fails to complete its normal wake sequence within the time requiered for the specific PHY type. This counter is cleared after a read and holds at all ones in the case of overflow. PCS Reset also clears this register

8.6.98 MMD7_EEE_ADVERTISEMENT_Register Register (Offset = 0x203C) [reset = 0x0]

MMD7_EEE_ADVERTISEMENT_Register is shown in Table 110.

Return to Summary Table.

Table 110. MMD7_EEE_ADVERTISEMENT_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0x0	Reserved
1	Advertise_100Base-TX_EEE	R/W	0x0	Advertise 100Base-TX EEE: 0x0 = Energy Efficient Ethernet is not advertised 0x1 = Energy Efficient Ethernet is advertised for 100Base-TX
0	RESERVED	R	0x0	Reserved

8.6.99 MMD7_EEE_LP_ABILITY_Register Register (Offset = 0x203D) [reset = 0x0]

MMD7_EEE_LP_ABILITY_Register is shown in Table 111.

Return to Summary Table.

Table 111. MMD7_EEE_LP_ABILITY_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0x0	Reserved
1	Link_Partner_EEE_Capability		0x0	Link Partner EEE Capability: 0x0 = Link Partner is not advertising EEE capability for 100Base-TX 0x1 = Link Partner is advertising EEE capability for 100Base-TX
0	RESERVED	R	0x0	Reserved

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83825I is a single-port, 10/100-Mbps Ethernet PHY. It supports connections to an Ethernet MAC through RMII. Connections to the Ethernet media are made through the IEEE 802.3-defined Media Dependent Interface.

When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

9.2 Typical Applications

図 17 shows a typical application for the DP83825I.

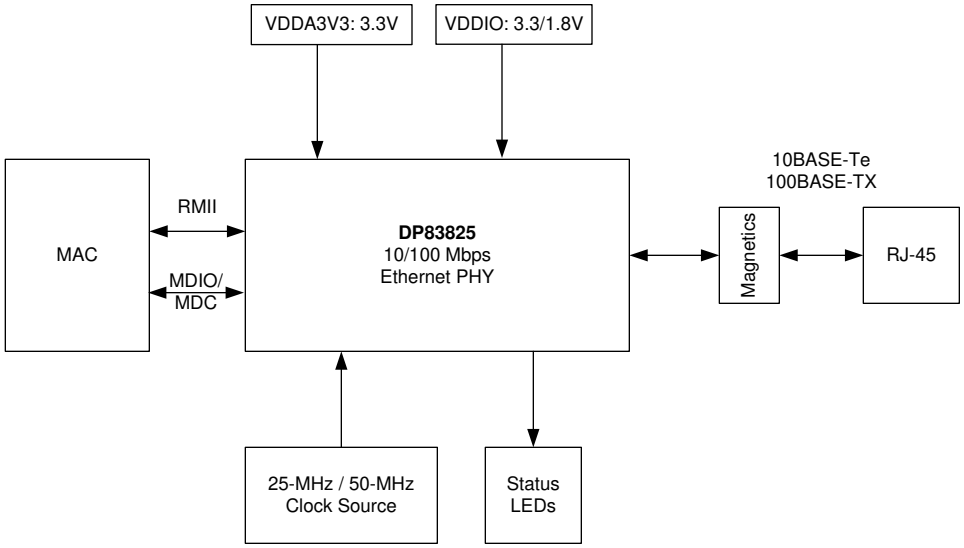

図 17. Typical DP83825I Application

9.2.1 Design Requirements

The design requirements for the DP83825I in TPI operation (100BASE-TX or 10BASE-Te) are:

1. AVD Supply = 3.3 V
2. VDDIO Supply = 3.3 V or 1.8 V
3. Reference Clock Input = 25-MHz or 50-MHz (RMII Slave)

9.2.1.1 Clock Requirements

The DP83825I supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

9.2.1.1.1 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating. The amplitude of the oscillator should be a nominal voltage of VDDIO.

Typical Applications (continued)

9.2.1.1.2 Crystal

The use of a 25-MHz, parallel resonant, 20-pF load crystal is recommended if operating with a crystal. A typical connection diagram is shown below for a crystal resonator circuit. Note that the load capacitor values will vary with the crystal vendors. Check with the vendor for the recommended loads. Series resistance value shall be adjusted to meet the crystal drive level. For more details, refer to the *Selection and Specification of Crystals for Texas Instruments Ethernet Physical Layer Transceivers* application report (SNLA290).

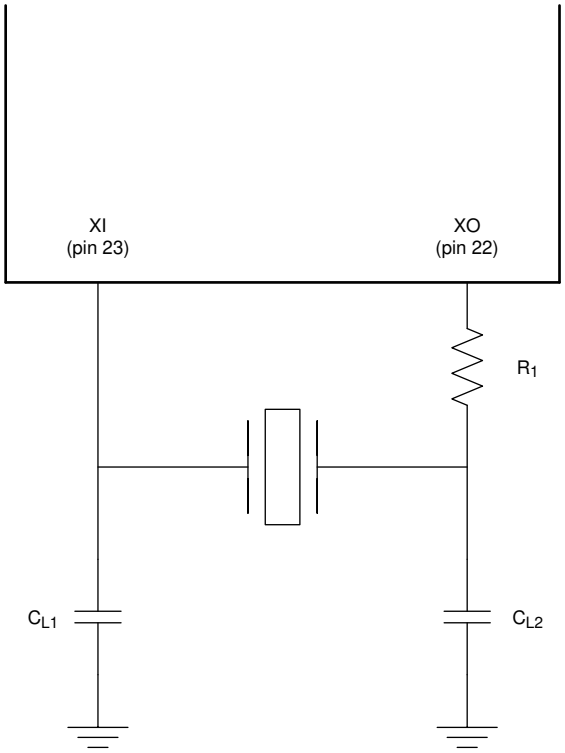

図 18. Crystal Oscillator Circuit

表 112. 25-MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Including Operational Temperature, aging and other factors	–50		50	ppm
Load Capacitance			15	40	pF
ESR				50	Ω

9.2.2 Detailed Design Procedure

The Media Independent Interface RMII connects the DP83825I to the Media Access Controller (MAC). The MAC may in fact be a discrete device or integrated into a microprocessor, CPU, FPGA, or ASIC. The Media Dependent Interface (MDI) connects the DP83825I to the transformer of the Ethernet network or to AC isolation capacitors when interfacing with a fiber transceiver.

9.2.2.1 RMII Layout Guidelines

1. Remember that RMII signals as single-ended signals.
2. Traces should be routed with 50-Ω impedance to ground.
3. Keep trace lengths as short as possible. TI recommends to keep the trace lengths between two to six inches long.

9.2.2.2 MDI Layout Guidelines

1. Remember that MDI signals are differential.
2. Traces should be routed with 50-Ω impedance to ground and 100-Ω differential controlled impedance.
3. Route MDI traces to the transformer on the same layer.
4. Use a metal-shielded RJ-45 connector and electrically connect the shield to chassis ground.
5. Avoid supplies and ground beneath the magnetics.
6. Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

9.2.2.3 TPI Network Circuit

図 19 shows the recommended twisted-pair interface network circuit for 10/100 Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

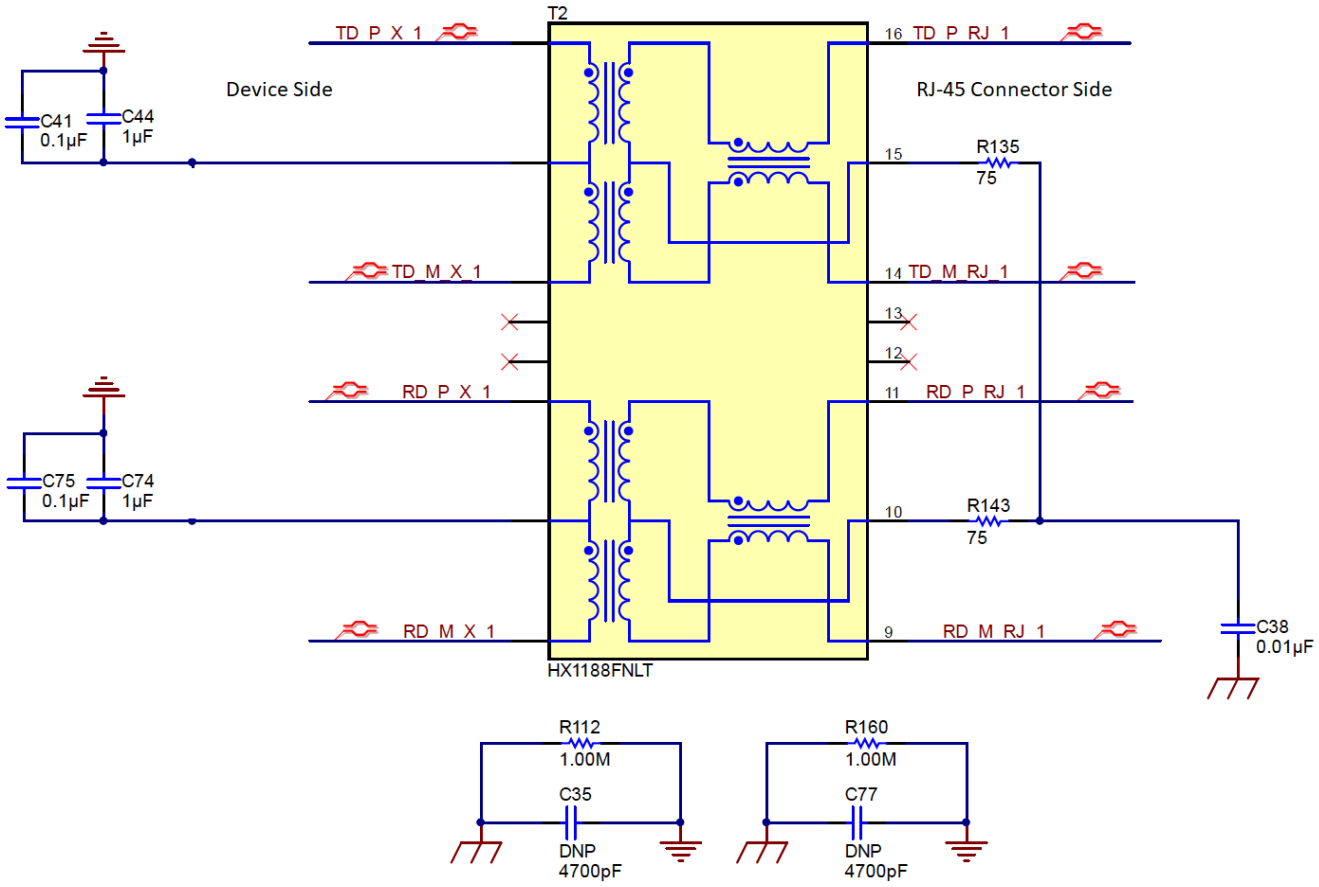

図 19. TPI Network Circuit

10 Power Supply Recommendations

The DP83825I is capable of operating with a 3.3-V or 1.8-V of I/O supply voltages along with analog supply of 3.3 V. DP83825I needs VDDA3V3 after VDDIO is fully ramped. Details are captured in the *Timing Diagrams*. If power sequencing is not feasible on the customer board, then an external Reset (RST_N) is needed on pin 5 when both power VDDA3V3 and VDDIO supplies are ramped.

図 20 shows the recommended power supply de-coupling network.

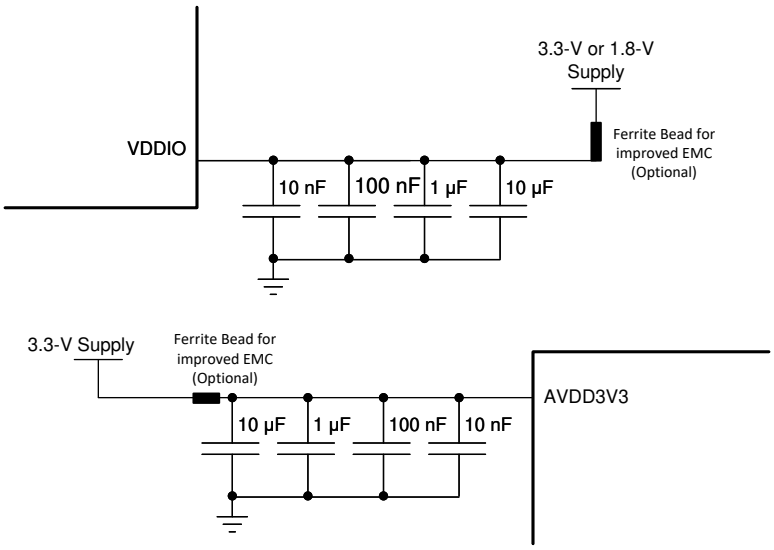

図 20. DP83825I Power Supply Decoupling Recommendation

11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy, and long traces can degrade signal quality. Traces should be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω single-ended impedance. Differential traces should be 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections, leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

Layout Guidelines (continued)

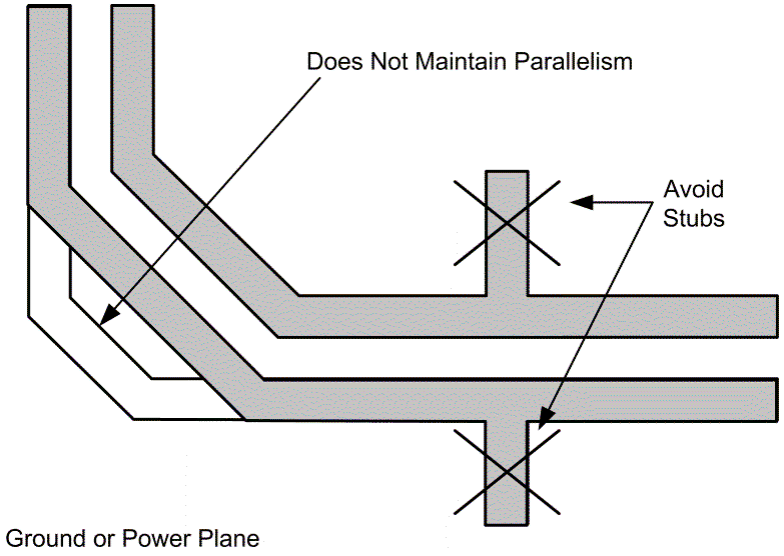

図 21. Differential Signal Traces

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and emissions. Length matching is also important for MAC interface connections. All RMII transmit signal trace lengths should match each other, and all RMII receive signal trace lengths should match each other, too.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

Layout Guidelines (continued)

11.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

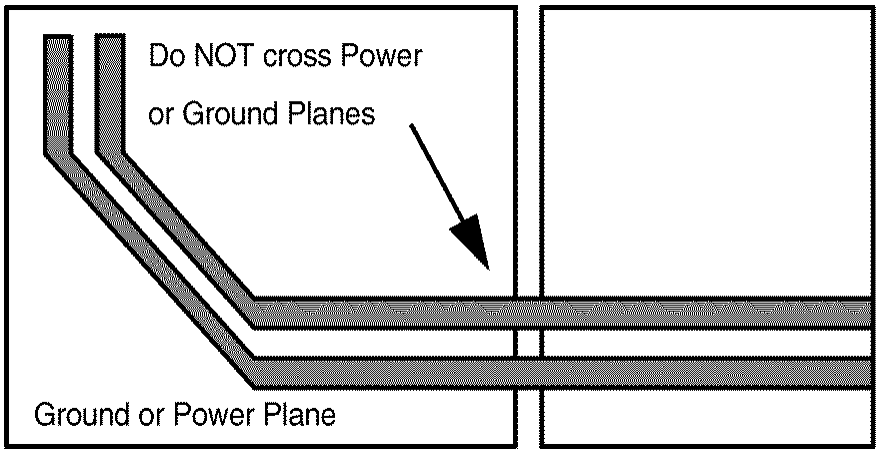

図 22. Differential Signal Pair and Plane Crossing

Layout Guidelines (continued)

11.1.3 Transformer Layout

Make sure there is no metal layer running beneath the transformer. Transformers can inject noise into the metal beneath them, which can affect the performance of the system. See 図 19.

11.1.3.1 Transformer Recommendations

The following magnetics have been tested with the DP83825I using the DP83825IEVM.

表 113. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse Electronics	HX1188NL
	HX1198FNL
	HX1188FNL

表 114. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn Ratio	±2%	1:1	-
Insertion Loss	1 - 100 MHz	–1	dB
Return Loss	1 - 30 MHz	–16	dB
	30 - 60 MHz	–10	dB
	60 - 80 MHz	–7.5	dB
Differential to Common Rejection Ratio	1	-61	dB
	50 MHz	–33	dB
	150 MHz	–25	dB
Crosstalk	30 MHz	–45	dB
	60 MHz	–39	dB
Isolation	HPOT	1500	Vrms

11.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

11.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB should be used when possible.

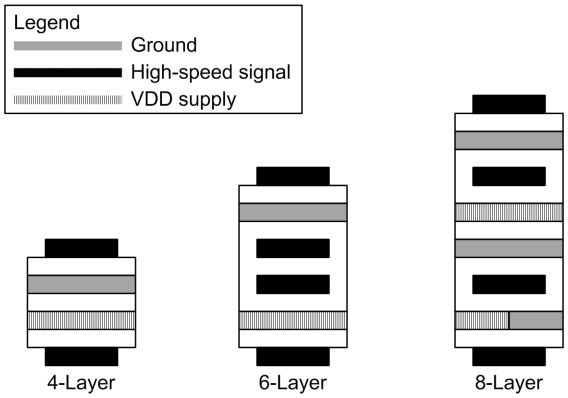

図 23. Recommended Layer Stack-Up

11.2 Layout Example

See the DP83825EVM for more information regarding layout.

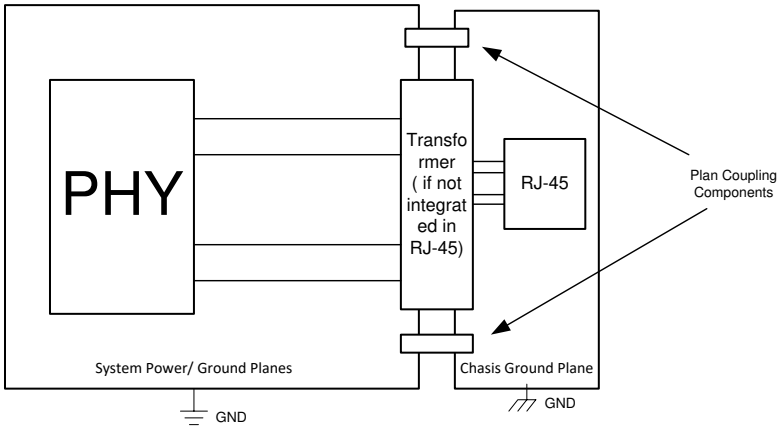

図 24. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Glossary

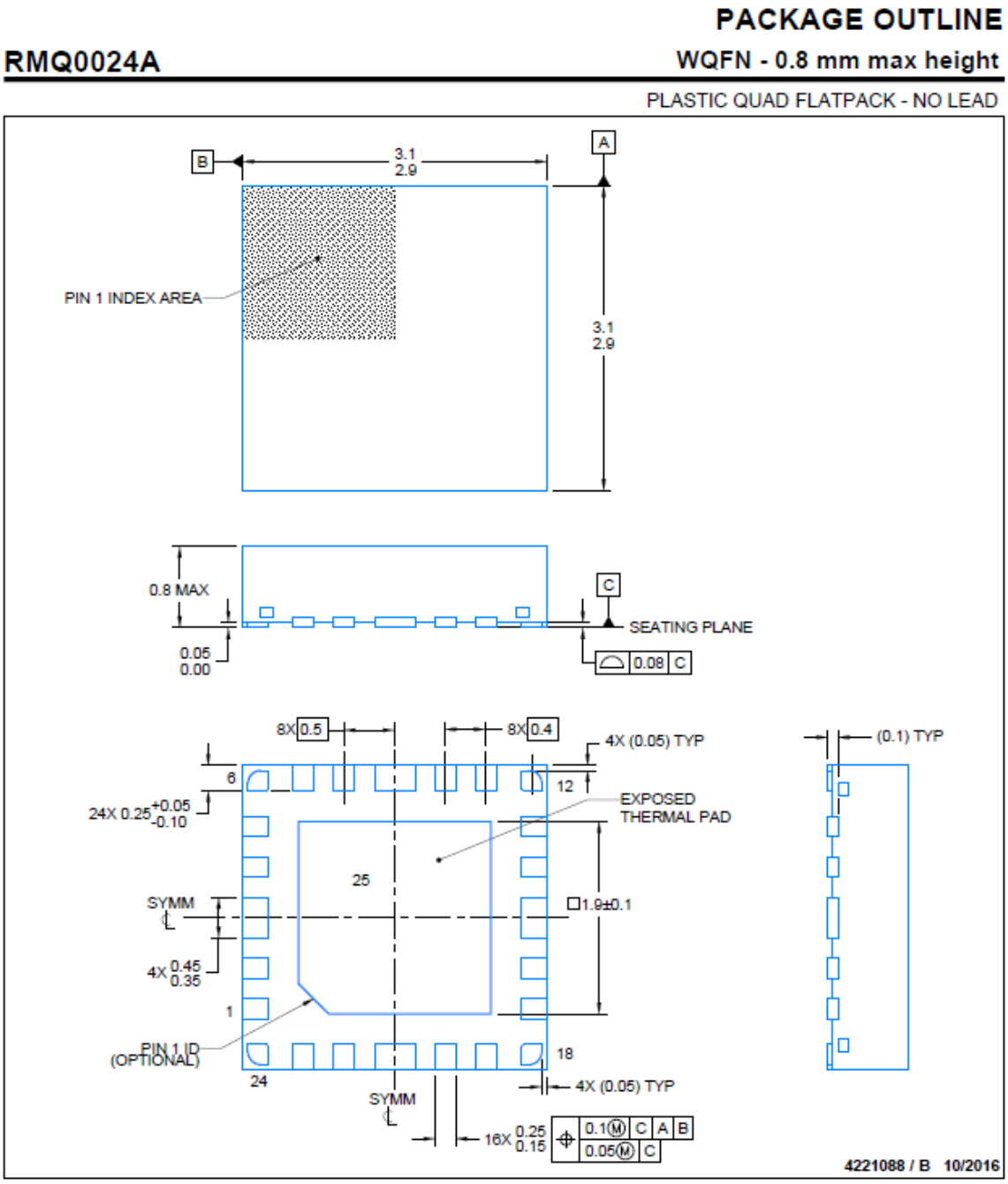
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

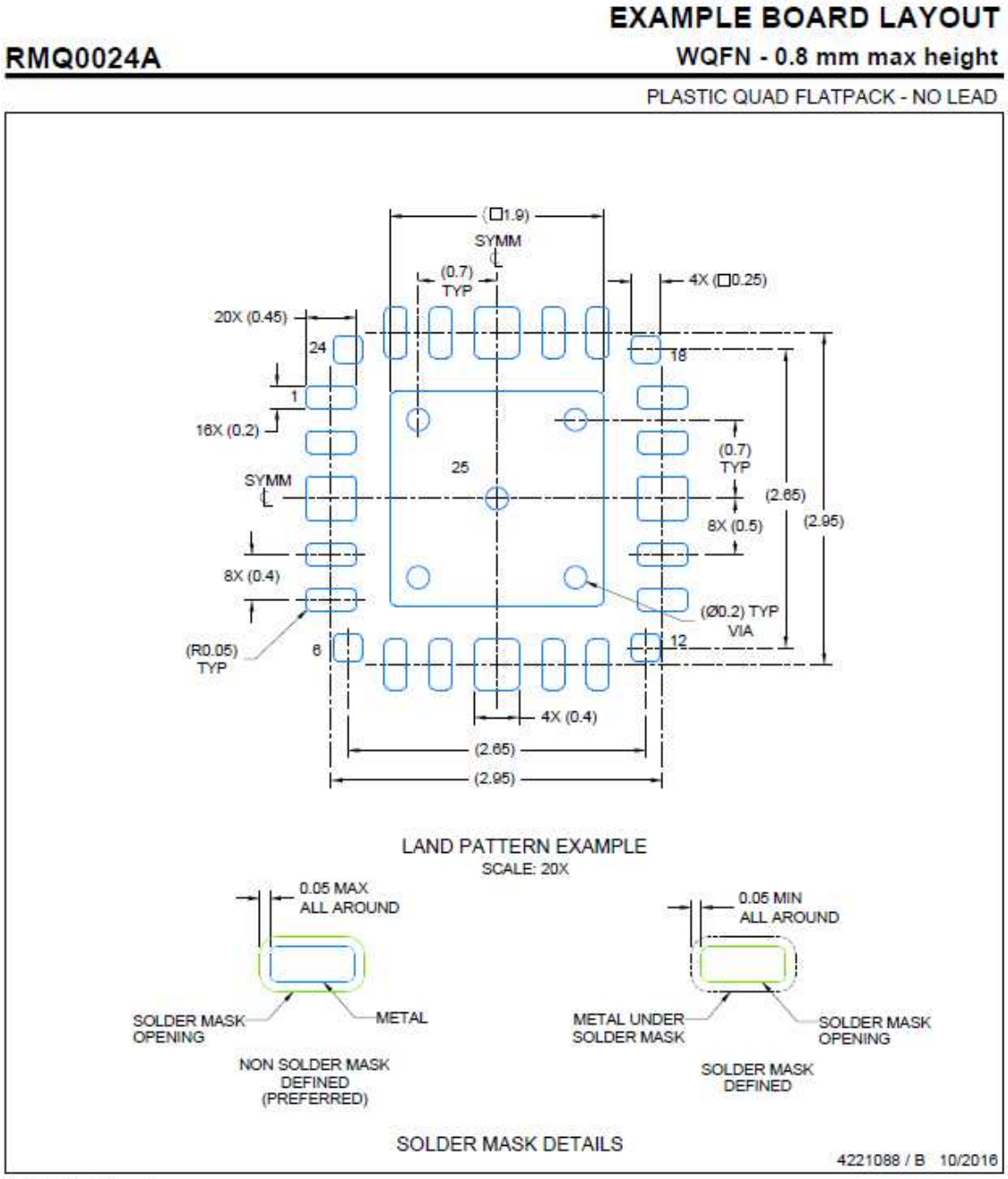
図 25. DP83825I パッケージ図



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

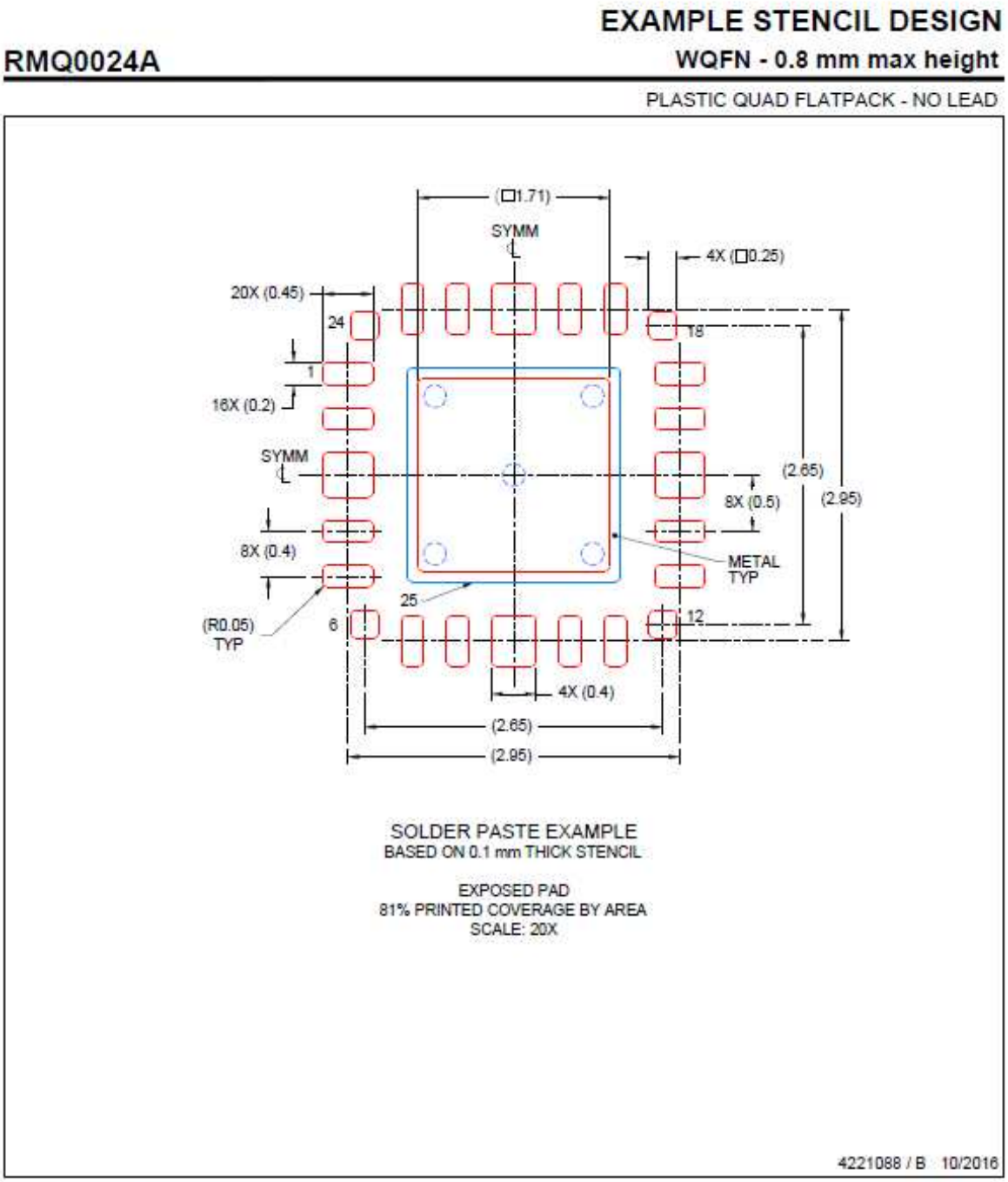
図 26. DP83825I パッケージ図



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

図 27. DP83825I パッケージ図



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83825IRMQR	ACTIVE	WQFN	RMQ	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I	Samples
DP83825IRMQT	ACTIVE	WQFN	RMQ	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	825I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

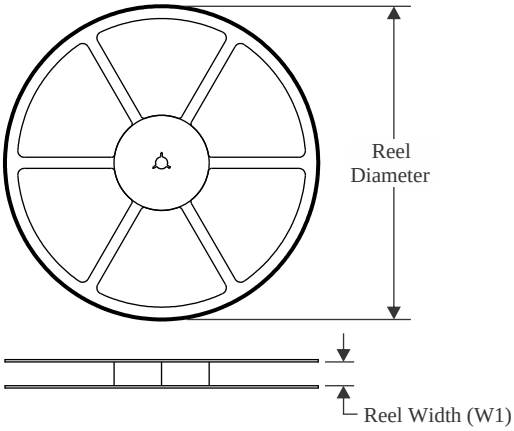
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

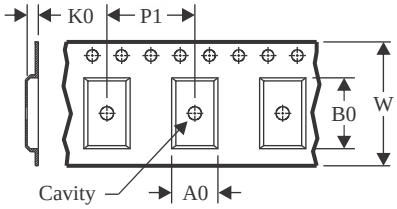
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

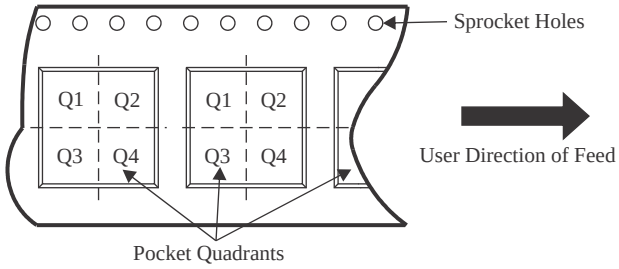


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

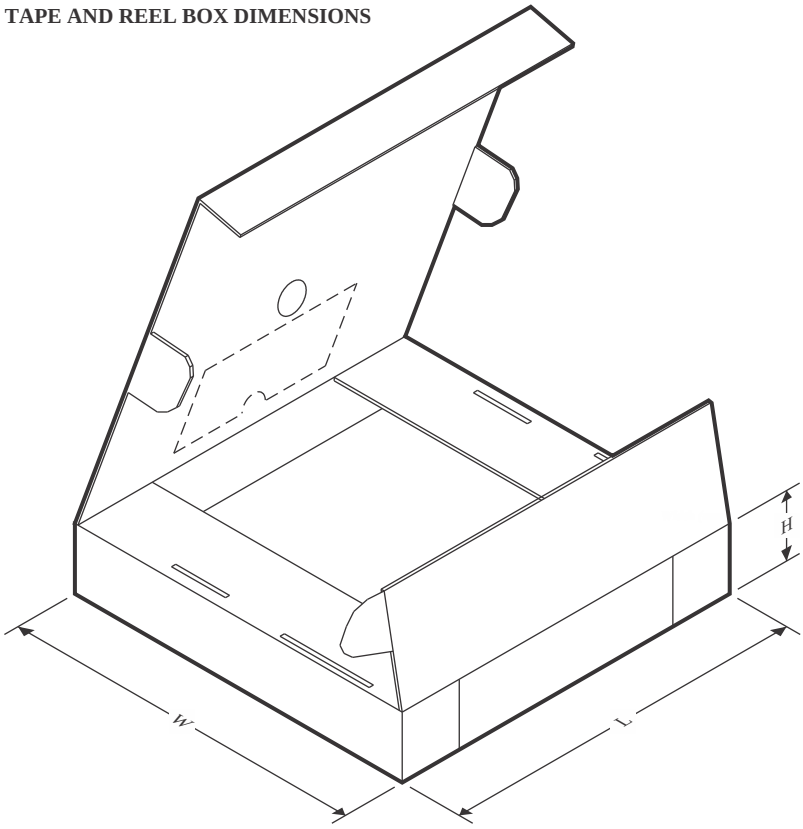
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83825IRMQR	WQFN	RMQ	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DP83825IRMQT	WQFN	RMQ	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

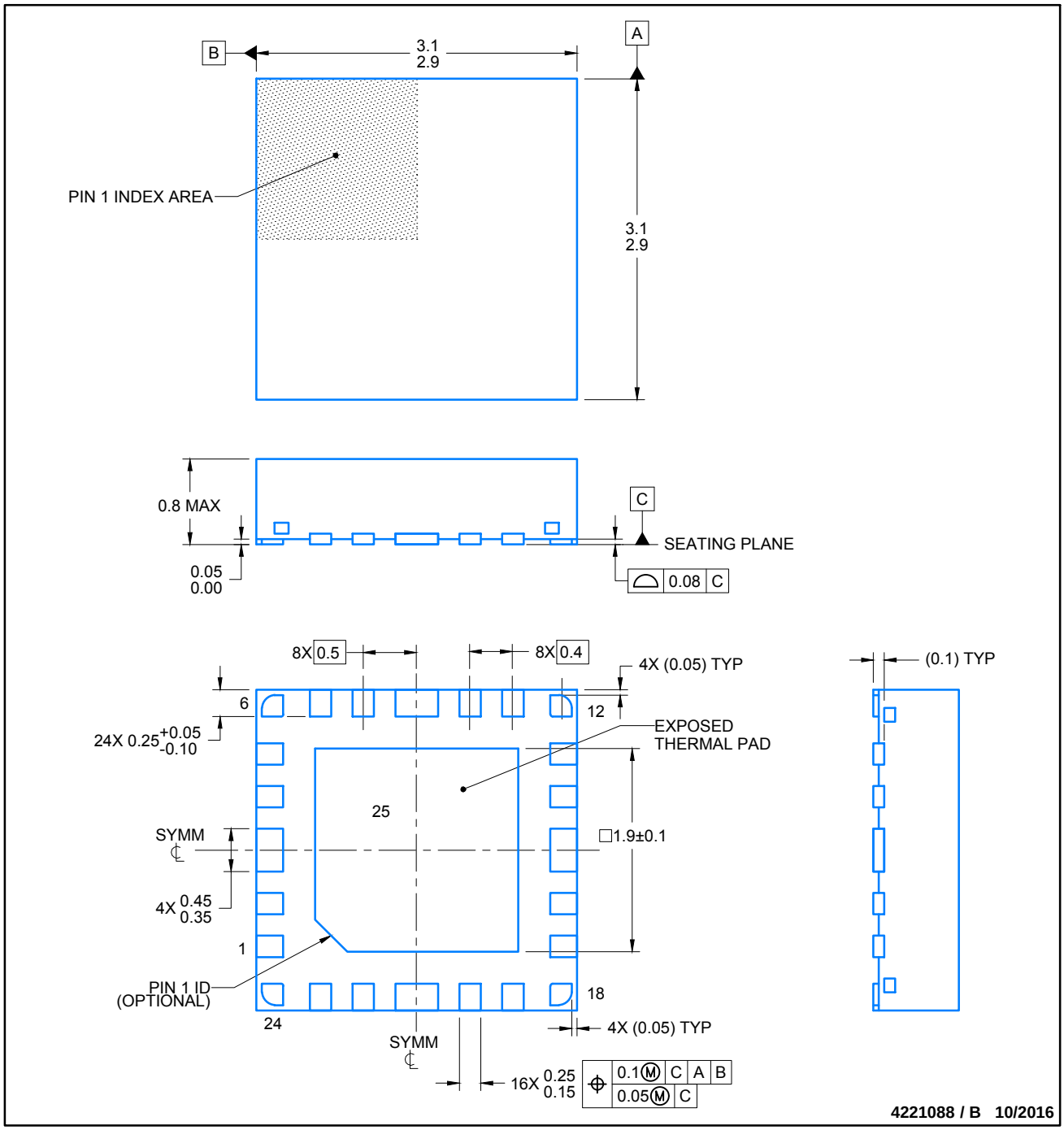
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83825IRMQR	WQFN	RMQ	24	3000	367.0	367.0	35.0
DP83825IRMQT	WQFN	RMQ	24	250	210.0	185.0	35.0

PACKAGE OUTLINE

RMQ0024A

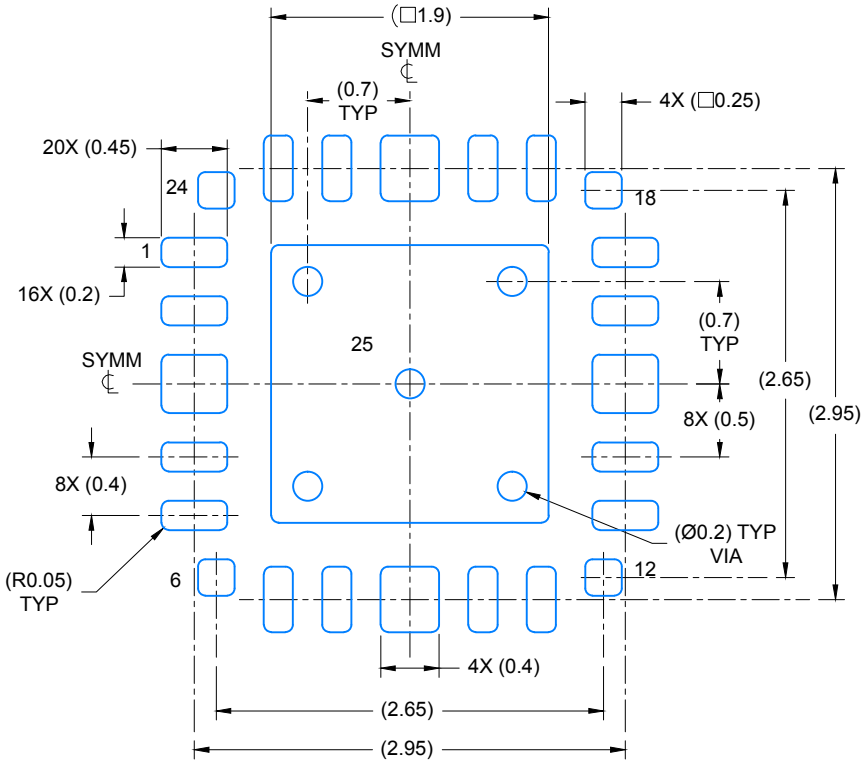
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



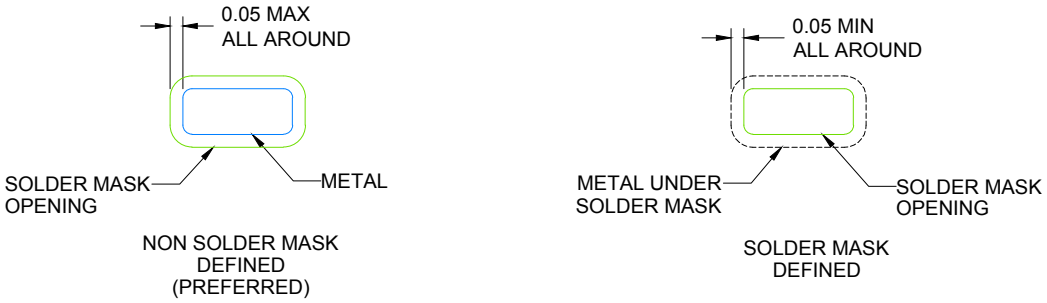
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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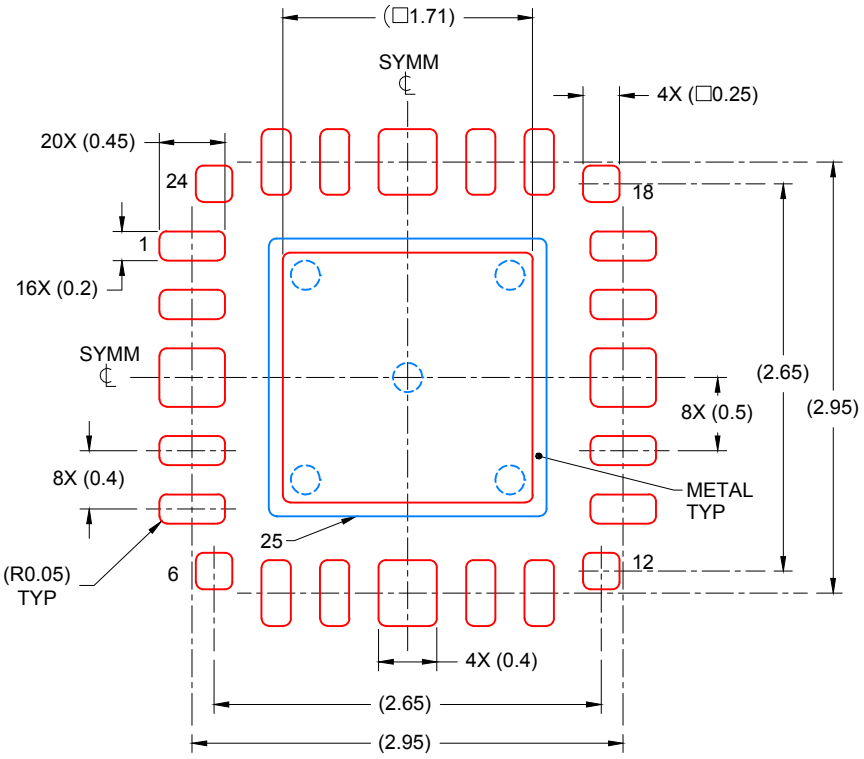
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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