

DRV10974 12V、3相、センサレス BLDC モータ・ドライバ

1 特長

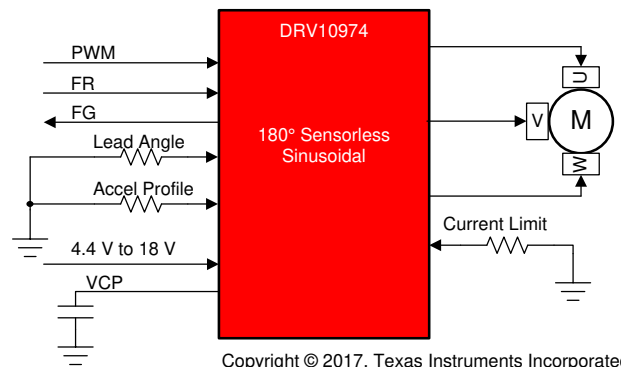
- 入力電圧範囲: 4.4V~18V
- ドライバ (H + L) の $r_{DS(on)}$ の合計: 750mΩ (標準値、 $T_A = 25^\circ\text{C}$)
- 位相駆動電流: 連続 1A (ピーク 1.5A)
- 180° 正弦波整流により音響性能を最適化
- 進角を抵抗で設定可能
- 電流制限を抵抗で設定可能
- ソフトスタートのアクセラレーション・プロファイルを抵抗で設定可能
- 電流センサを内蔵しているため外付け電流センサ抵抗が不要
- モータのセンター・タップがない独自のセンサレス制御
- シンプルなユーザー・インターフェイス:
 - スタートアップを 1 本のピンで設定
 - PWM 入力によりモータに印加する電圧の大きさを指定
 - オープン・ドレイン FG 出力により速度フィードバックを提供
 - 順方向 / 逆方向制御用ピン
- 包括的な保護機能:
 - モータ・ロック検出および再始動
 - 過電流、短絡、過熱、低電圧

相 BEMF を調整してドライバ効率を最適化できます。また、低 $r_{DS(on)}$ MOSFET の採用により、モータ駆動中も消費電力を抑えることができます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DRV10974	HTSSOP (16)	5.00mm × 4.40mm
	WQFN (16)	4.00mm × 4.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション回路図

2 アプリケーション

- 白物家電
- ファン、ブロワ、ポンプ
- BLDC モータ・モジュール

3 概要

DRV10974 は、パワー MOSFET を内蔵する 3 相センサレス・モータ・ドライバであり、最大 1A (rms) の連続駆動電流を供給できます。このデバイスは、低コスト、低ノイズ、さらに外付け部品の削減が求められるアプリケーション向けに設計されています。

DRV10974 は、独自のセンサレス制御方式を採用して、信頼性の高い整流機能を提供します。180° 正弦波整流により、120° (矩形波) 整流で一般に発生する純音響を大幅に低減できます。DRV10974 のスピンアップは、低消費電力の外付け抵抗 1 つで設定可能です。電流制限も低消費電力の外付け抵抗により設定できます。

DRV10974 デバイスを使うと、PWM 入力を印加し、駆動電圧の大きさを制御することで、またはアナログ電圧で PWM ピンを駆動し、速度帰還として FG ピンを監視することで、モータ速度を簡単に制御できます。

DRV10974 には効率を上げる多くの機能が搭載されています。抵抗により進角の設定が可能のため、位相電流と位



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4 Revision History

Changes from Revision D (June 2020) to Revision E (March 2021)	Page
• Updated Human-body model (HBM).....	5

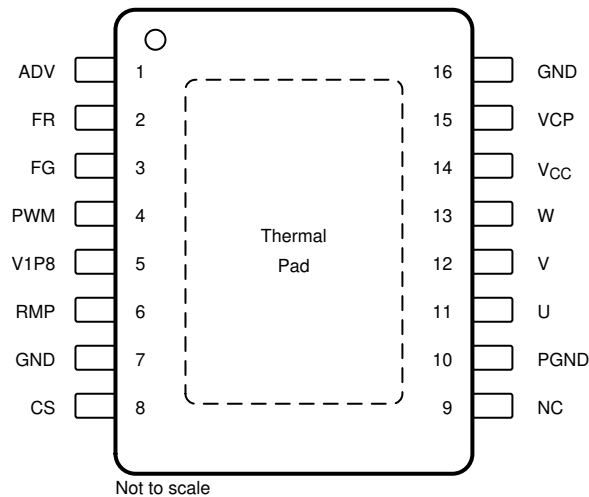
Changes from Revision B (June 2018) to Revision C (September 2018)	Page
• ドキュメントのステータスを「混合ステータス」から「量産データ」に変更.....	1
• 「製品情報」表の WQFN のエントリから「事前情報」指定を削除.....	1
• Deleted the "Advance informatoin" note from the WQFN pinout drawing.....	3
• Deleted the "Advance Information" note from the <i>Thermal Information</i> table.....	5
• Added description of Analog Mode Speed Control.....	12
• Added Kt High and Kt Low descriptions in abnormal Kt lock detect figure.....	16
• Added layout example for QFN package type.....	27

Changes from Revision A (April 2018) to Revision B (June 2018)	Page
• 「製品情報」表に WQFN パッケージを追加.....	1
• Added pinout drawing for the WQFN package.....	3
• Added a column to the <i>Pin Functions</i> table for the WQFN package, and added the TYPE column.....	3
• Added a column to the <i>Thermal Information</i> table for the VQFN package.....	5
• Changed $r_{DS(on)}$ vs. Temperature graph to include V_{CC} condition.....	10
• Changed Speed-Control Transfer Function figure to clearly show when the device enters and exits low power mode.....	12
• Updated Lock BEMF Abnormal text for clarity.....	16
• Changed <i>Detailed Design Procedure</i> to cover the high level tuning process of the RMP, ADV, and CS settings.....	25

Changes from Revision * (January 2018) to Revision A (April 2018)	Page
• 「セクション 1」の一覧で、いくつかの箇条書き項目を追加または変更.....	1
• 「セクション 3」セクションの 3 番目の段落でテキストを変更.....	1
• Added parameter symbol (f_{PWM_OUT}) to the 25-kHz PWM signal.....	12
• Added parameter symbol (f_{PWM_OUT}) to the 25-kHz PWM signal.....	12
• Added parameter symbol (DC_{STEP}) for the control resolution.....	12
• Added parameter symbol (DC_{ON_MIN}) for the minimum-operation duty cycle.....	12

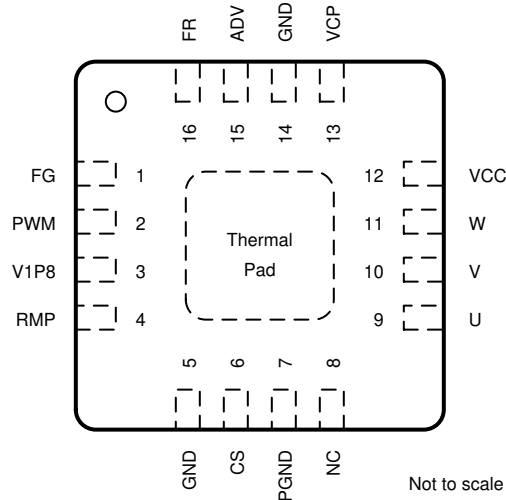
- Changed "pulse durations" to "duty cycles"..... 12
- Changed PWM_{DC} to PWM_{dc} 12
- Added parameter symbol (f_{FG_MIN}) for the motor speed..... 15
- Changed the number of lock-detect schemes from five to six..... 15
- Added a table note stating the required resistor tolerance..... 18
- Added a new セクション 7.4.1.2 section..... 19
- Added a parameter symbol (t_{ALIGN}) in the セクション 7.4.1.3 section, and rewrote the last sentence thereof.... 20
- Changed the column headings of the two rightmost columns in 表 7-2 20
- Added three table notes following 表 7-2 20
- Changed "programmed resistor" to "selected resistor"..... 21
- Added a table note stating the required resistor tolerance..... 21
- Added a table note stating the required resistor tolerance..... 22
- Added a $\pm 30\%$ tolerance to the V1P8 capacitor in 表 8-1 24
- Changed content of Row 4 in 表 8-2 to "Motor electrical constant"..... 25
- Deleted all previous content from the セクション 8.2.2 section and replaced it with a reference to the *DRV10974 Tuning Guide* 25
- Changed 図 8-3 25
- Added location information for the capacitor in the セクション 9 section..... 26

5 Pin Configuration and Functions



NC – No internal connection

図 5-1. PWP PowerPAD™ Package 16-Pin HTSSOP With Exposed Thermal Pad Top View



NC – No internal connection

图 5-2. RUM Package 16-Pin WQFN With Exposed Thermal Pad Top View

表 5-1. Pin Functions

NAME.	PIN NO.		I/O	TYPE ⁽¹⁾	DESCRIPTION
	HTSSOP	WQFN			
ADV	1	15	I	D	Selects the applied lead angle by 1/8-W resistor; not to be driven externally with a source; leaving the pin open results in the longest lead angle; the lead angle is determined by the ADV pin voltage at power up.
CS	8	6	I	D	Selects current limit by 1/8-W resistor; not to be driven externally with a source; leaving the pin open results in the highest current limit; the current limit is determined by the CS pin voltage at power up.
FG	3	1	O	D	Provides motor speed feedback; open-drain output with internal pullup to V3P3; needs a pullup resistor to limit current if pullup voltage is higher than V3P3
FR	2	16	I	D	Direction control. FR = 0: U→V→W; FR = 1: U→W→V; value is determined by the FR pin state on exit of low-power mode; internal pulldown
GND	7, 16	5, 14	—	—	Digital and analog ground
NC	9	8	—	NC	No internal connection
PGND	10	7	—	P	Power ground connection for motor power
PWM	4	2	I	D	Motor speed-control input; auto detect for analog or digital mode; internal pullup to 2.2 V
RMP	6	4	I	D	Acceleration ramp-rate control; 1/8-W resistor to GND to set acceleration rate; leaving the pin open results in the slowest acceleration rate; the acceleration rate is determined by the RMP pin voltage at power up.
U	11	9	I/O	A	Motor phase U
V	12	10	I/O	A	Motor phase V
V1P8	5	3	O	P	LDO regulator for internal operation; 1-μF, 6.3-V ceramic capacitor tied to GND. Can supply a maximum of 3 mA to an external load.
V _{CC}	14	12	I	P	Power-supply connection; 10-μF, 25-V ceramic capacitor tied to GND
VCP	15	13	O	A	Charge-pump output; 100-nF, 10-V ceramic capacitor tied to V _{CC}
W	13	11	I/O	A	Motor phase W
Thermal pad	—	—	—	—	The exposed thermal pad must be electrically connected to the ground plane by soldering to the PCB for proper operation, and connected to the bottom side of the PCB through vias for better thermal spreading.

(1) I = Input, O = Output, I/O = Input/output, P = Power, D = Digital, A = Analog, NC = No connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Pin voltage	V _{CC}	-0.3	20	V
	PWM, FR	-0.3	5.5	
	CS, RMP, ADV	-0.3	2	
	GND, PGND	-0.3	0.3	
	U, V, W	-1	20	
	V1P8	-0.3	2	
	FG	-0.3	20	
	VCP	-0.3	V _{CC} + 5.5	
Maximum junction temperature, T _{Jmax}		-40	150	°C
Storage temperature, T _{stg}		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V _{CC}	4.4		18	V
Voltage	U, V, W	-0.7		18	V
	PWM, FR	-0.1		5.5	
	FG	0.5		18	
	CS	-0.1		1.8	
	PGND, GND	-0.1		0.1	
	RMP, ADV	-0.1		1.8	
Current	V1P8 regulator-output current; external load	0		3	mA
Operating ambient temperature, T _A		-40		85	°C
Operating junction temperature, T _J		-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV10974		UNIT
		PWP (HTSSOP)	RUM (VQFN)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	37.8	34.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	25.2	27	°C/W
R _{θJB}	Junction-to-board thermal resistance	20.7	13.3	°C/W

THERMAL METRIC ⁽¹⁾		DRV10974		UNIT
		PWP (HTSSOP)	RUM (VQFN)	
		16 PINS	16 PINS	
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.5	13.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	4	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.5 Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{CC}	Supply current	$T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, no motor load		5	7	mA
$I_{CC(LP)}$	Low power mode	$T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$		380		μA
UVLO						
$V_{(UVLO_F)}$	V_{CC} UVLO falling		4.2	4.3	4.4	V
$V_{(UVLO_R)}$	V_{CC} UVLO rising		4.5	4.7	4.85	V
$V_{hys(UVLO)}$	V_{CC} UVLO hysteresis			400		mV
$V_{VCP(UVLO_F)}$	Charge pump UVLO falling	$V_{VCP} - V_{CC}$	3.35	3.7	4.05	V
$V_{VCP(UVLO_R)}$	Charge pump UVLO rising	$V_{VCP} - V_{CC}$	3.65	4.0	4.37	V
$V_{hys(VCP)}$	Charge pump UVLO hysteresis			330		mV
$V_{(V1P8_F)}$	V1P8 UVLO falling		1.25	1.4	1.55	V
$V_{(V1P8_R)}$	V1P8 UVLO rising		1.35	1.5	1.65	V
$V_{hys(V1P8)}$	V1P8 UVLO hysteresis			100		mV
VOLTAGE REGULATORS						
V_{V1P8}	V1P8 voltage	$T_A = 25^\circ\text{C}$, $C_{(V1P8)} = 1\ \mu\text{F}$	1.7	1.8	1.9	V
I_{V1P8}	Maximum external load from V1P8	$T_A = 25^\circ\text{C}$, $C_{(V1P8)} = 1\ \mu\text{F}$			3	mA
INTEGRATED MOSFET						
$r_{ds(on)_HS}$	High-side FET on-resistance	$T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $I_O = 100\text{ mA}$		0.375	0.425	Ω
$r_{ds(on)_LS}$	Low-side FET on-resistance	$T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $I_O = 100\text{ mA}$		0.375	0.425	Ω
PHASE DRIVER						
SL_{PH_LH}	Phase slew rate switching low to high	SlewRate = 0; measure 20% to 80%; $V_{CC} = 12\text{ V}$; phase current > 20 mA	70	120	170	V/ μs
SL_{PH_HL}	Phase slew rate switching high to low	SlewRate = 0; measure 80% to 20%; $V_{CC} = 12\text{ V}$; phase current > 20 mA	70	120	170	V/ μs
f_{PWM_OUT}	Phase output PWM frequency			25		kHz
t_{dead_time}	Recommended dead time		440			ns
CHARGE PUMP						
V_{VCP}	VCP voltage	$V_{CC} = 4.4\text{ V to }18\text{ V}$	$V_{CC} + 4$	$V_{CC} + 5$	$V_{CC} + 5.5$	V
CURRENT LIMIT						

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{LIMIT}	Current-limit threshold	V _{CC} = 12 V, R _(CS) = 7.32 kΩ ±1%		0.2		A
		V _{CC} = 12 V, R _(CS) = 16.2 kΩ ±1%		0.4		
		V _{CC} = 12 V, R _(CS) = 25.5 kΩ ±1%		0.6		
		V _{CC} = 12 V, R _(CS) = 38.3 kΩ ±1%		0.8		
		V _{CC} = 12 V, R _(CS) = 54.9 kΩ ±1%		1		
		V _{CC} = 12 V, R _(CS) = 80.6 kΩ ±1%		1.2		
		V _{CC} = 12 V, R _(CS) = 115 kΩ ±1%		1.4		
		V _{CC} = 12 V, R _(CS) = 182 kΩ ±1%, open loop and closed loop current limit		1.6		
		V _{CC} = 12 V, R _(CS) = 182 kΩ ±1%, align current limit		1.5		
RANGE OF MOTORS SUPPORTED						
R _m	Motor resistance measurement	Phase to center tap	1		20	Ω
K _t	Motor BEMF constant measurement	Phase to center tap	5		150	mV/Hz
t _{ALIGN}	Motor align time			0.67		s

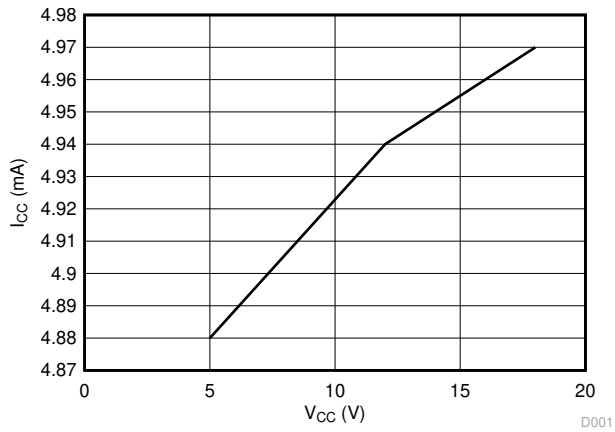
over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM - DIGITAL MODE						
V _{IH(DIG)}	PWM input high voltage		2.2			V
V _{IL(DIG)}	PWM input low voltage				0.6	V
f _{PWM}	PWM input frequency		0.1		100	kHz
DC _{MAX}	Maximum output PWM duty cycle	V _{VCC} < 14 V		100 %		
		V _{VCC} ≥ 14 V		[(14 / V _{VCC}) × 100] %		
DC _{MIN}	Minimum output PWM duty cycle device needs to guarantee (irrespective of input PWM DC)	Lower duty cycle from 15% down		15%		
DC _{ON_MIN}	Minimum input duty cycle that device uses to drive motor			1.5 %		
DC _{STEP}	Duty cycle step size/resolution			0.2 %		
V _{IH(AUTO)}	PWM input high voltage for auto detection		1.62	1.695	1.77	V
V _{IL(AUTO)}	PWM input low voltage for exiting PWM mode		1.315	1.39	1.465	V
R _{pu(PWM)}	Internal PWM pullup resistor to V3P3			120		kΩ
LOW-POWER MODE						
t _(EX_LPM)	PWM pulse duration to exit low-power mode	PWM > V _{IH(DIG)}	1			μs
V _(EX_LPM)	PWM voltage to exit low-power mode		1.5			V
t _(EN_LPM)	PWM low time to enter low-power mode	PWM < V _{IL(DIG)} ; motor stationary	25			ms
PWM - ANALOG MODE						
V _{ANA_FS}	Analog full-speed voltage			1.8		V
V _{ANA_ZS}	Analog zero-speed voltage		20			mV
R _{out(PWM)}	External analog driver output impedance				50	kΩ
t _{SAM}	Analog speed sample period			320		μs
V _{ANA_RES}	Analog voltage resolution			3.5		mV
DIGITAL I/O (FG OUTPUT, FR INPUT)						
f _{FG_MIN}	Minimum FG output frequency during coast			10		Hz
V _{IH(FR)}	Input high		2.2			V
V _{IL(FR)}	Input low				0.6	V
I _(FG_SINK)	Output sink current, FG	V _O = 0.3 V	5			mA
R _{pu(FG)}	Internal FG pullup resistor to 3.3V			20		kΩ
R _{pd(FR)}	Internal FR pulldown resistor to ground			100		kΩ
LOCK DETECTION RELEASE TIME						
t _(LOCK_OFF)	Lock release time			5		s
OVERCURRENT PROTECTION						
I _{OC_limit}	Overcurrent protection	T _A = 25°C	2.5			A
t _{OC_retry}	Overcurrent protection retry time			5		s
THERMAL SHUTDOWN						
T _{SD}	Shutdown temperature threshold		140	150		°C
T _{SD(hys)}	Shutdown temperature threshold hysteresis			15		°C

over operating junction temperature range (unless otherwise noted)

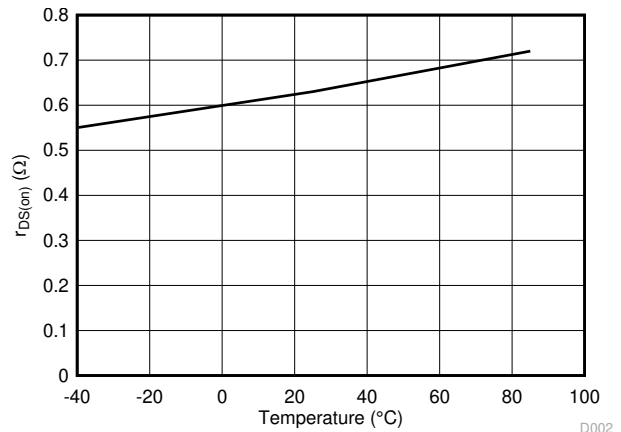
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LEAD ANGLE						
ADV _{select}	Lead angle selection	V _{CC} = 12 V, R _(ADV) = 10.7 kΩ ±1%		10		μs
		V _{CC} = 12 V, R _(ADV) = 14.3 kΩ ±1%		25		
		V _{CC} = 12 V, R _(ADV) = 17.8 kΩ ±1%		50		
		V _{CC} = 12 V, R _(ADV) = 22.1 kΩ ±1%		100		
		V _{CC} = 12 V, R _(ADV) = 28 kΩ ±1%		150		
		V _{CC} = 12 V, R _(ADV) = 34 kΩ ±1%		200		
		V _{CC} = 12 V, R _(ADV) = 41.2 kΩ ±1%		250		
		V _{CC} = 12 V, R _(ADV) = 49.9 kΩ ±1%		300		
		V _{CC} = 12 V, R _(ADV) = 59 kΩ ±1%		400		
		V _{CC} = 12 V, R _(ADV) = 71.5 kΩ ±1%		500		
		V _{CC} = 12 V, R _(ADV) = 86.6 kΩ ±1%		600		
		V _{CC} = 12 V, R _(ADV) = 105 kΩ ±1%		700		
		V _{CC} = 12 V, R _(ADV) = 124 kΩ ±1%		800		
		V _{CC} = 12 V, R _(ADV) = 150 kΩ ±1%		900		
		V _{CC} = 12 V, R _(ADV) = 182 kΩ ±1%		1000		
ACCELERATION RAMP RATE						
RMP _{select}	RMP selection for acceleration profile	V _{CC} = 12 V, R _(RMP) = 7.32 kΩ ±1%		0		code
		V _{CC} = 12 V, R _(RMP) = 10.7 kΩ ±1%		1		
		V _{CC} = 12 V, R _(RMP) = 14.3 kΩ ±1%		2		
		V _{CC} = 12 V, R _(RMP) = 17.8 kΩ ±1%		3		
		V _{CC} = 12 V, R _(RMP) = 22.1 kΩ ±1%		4		
		V _{CC} = 12 V, R _(RMP) = 28 kΩ ±1%		5		
		V _{CC} = 12 V, R _(RMP) = 34 kΩ ±1%		6		
		V _{CC} = 12 V, R _(RMP) = 41.2 kΩ ±1%		7		
		V _{CC} = 12 V, R _(RMP) = 49.9 kΩ ±1%		8		
		V _{CC} = 12 V, R _(RMP) = 59 kΩ ±1%		9		
		V _{CC} = 12 V, R _(RMP) = 71.5 kΩ ±1%		10		
		V _{CC} = 12 V, R _(RMP) = 86.6 kΩ ±1%		11		
		V _{CC} = 12 V, R _(RMP) = 105 kΩ ±1%		12		
		V _{CC} = 12 V, R _(RMP) = 124 kΩ ±1%		13		
		V _{CC} = 12 V, R _(RMP) = 150 kΩ ±1%		14		
V _{CC} = 12 V, R _(RMP) = 182 kΩ ±1%		15				

6.6 Typical Characteristics



6-1. Supply Current vs Power Supply

D001



V_{CC} = 12 V

6-2. r_{DS(on)} vs Temperature When V_{CC} = 12 V

D002

7 Detailed Description

7.1 Overview

The DRV10974 device is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive-current capability up to 1 A continuous (rms). The device is specifically designed for low-noise, low external-component count, 12-V motor-drive applications. The 180° commutation requires no configuration beyond setting the peak current, the lead angle, and the acceleration profile, each of which is configured by an external resistor.

The 180° sensorless-control scheme provides sinusoidal output voltages to the motor phases as shown in [Figure 7-1](#).

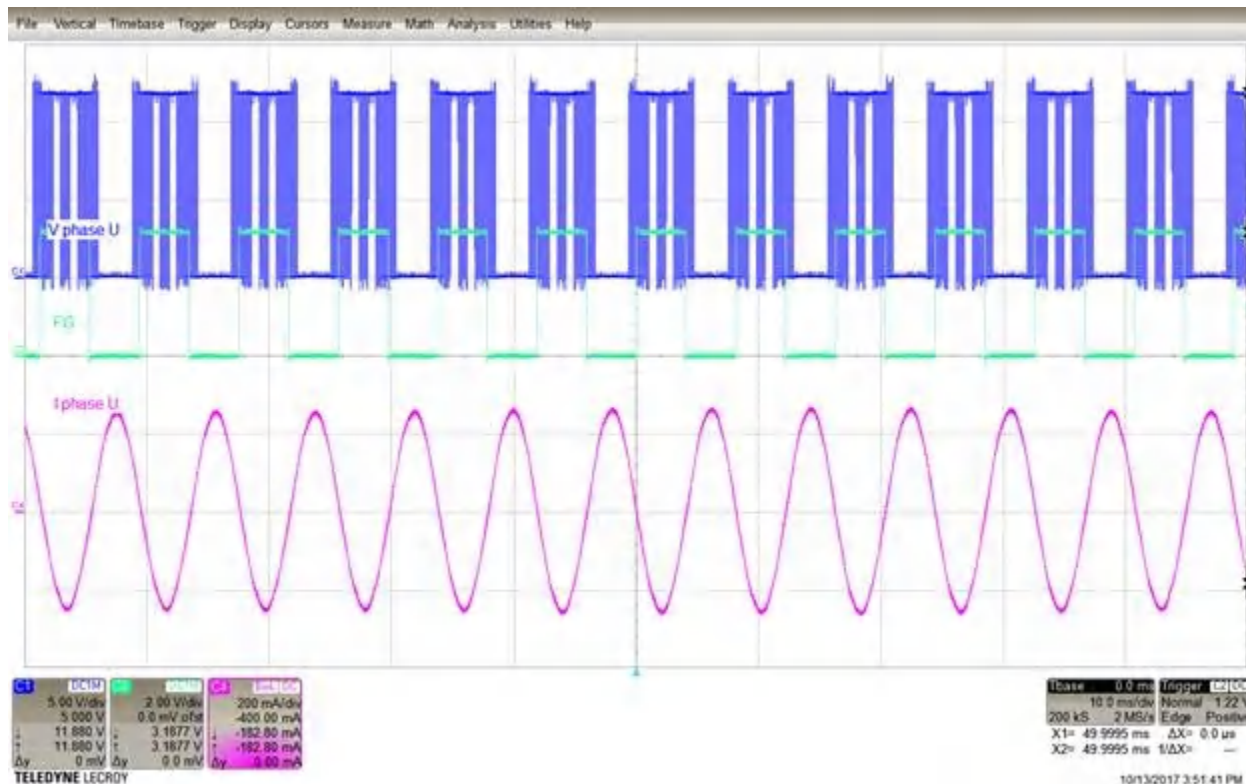
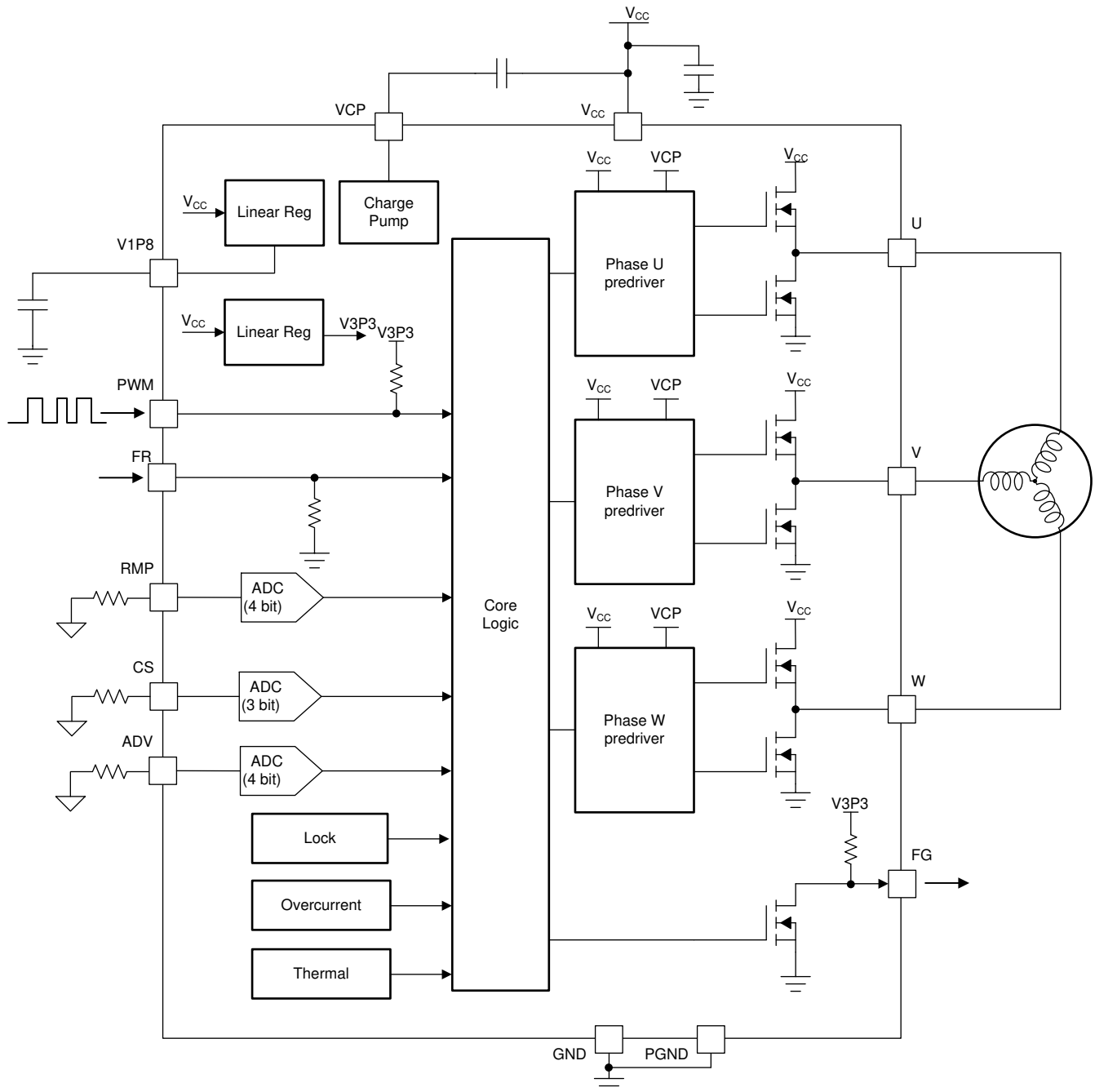


Figure 7-1. 180° Sensorless-Control Scheme

Interfacing to the DRV10974 device is simple and intuitive. The DRV10974 device receives a PWM input that it uses to control the speed of the motor. The duty cycle of the PWM input is used to determine the magnitude of the voltage applied to the motor. The resulting motor speed can be monitored on the FG pin. The FR pin is used to control the direction of rotation for the motor. The acceleration ramp rate is controlled by the RMP pin. The current limit is controlled by a resistor on the CS pin. The lead angle is controlled by a resistor on the ADV pin. When the motor is not spinning, a low-power mode turns off unused circuits to conserve power.

The DRV10974 device features extensive protection and fault-detect mechanisms to ensure reliable operation. The device provides overcurrent protection without the requirement for an external current-sense resistor. Rotor-lock detect uses several methods to reliably determine when the rotor stops spinning unexpectedly. The device provides additional protection for undervoltage lockout (UVLO), for thermal shutdown, and for phase short circuit (phase to phase, phase to ground, phase to supply).

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Speed Input and Control

The DRV10974 device has a three-phase 25-kHz PWM (f_{PWM_OUT}) output that has an average value of sinusoidal waveforms from phase to phase as shown in [Figure 7-2](#). When any phase is measured with reference to ground, the waveform observed is a PWM-encoded sinusoid coupled with third-order harmonics as shown in [Figure 7-3](#). This encoding scheme simplifies the driver requirements because one phase output is always equal to zero.

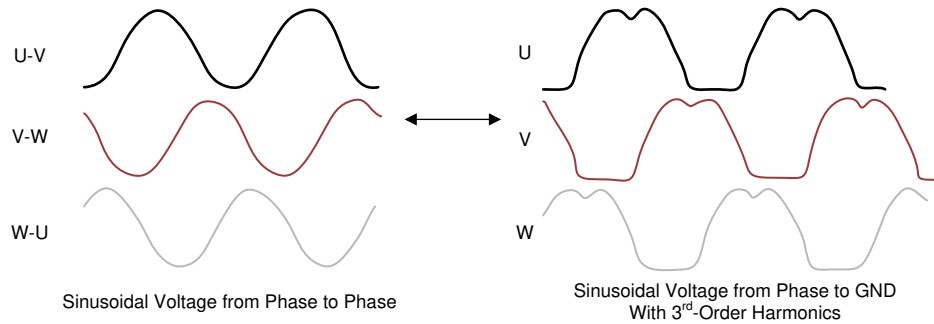


图 7-2. Sinusoidal Voltage

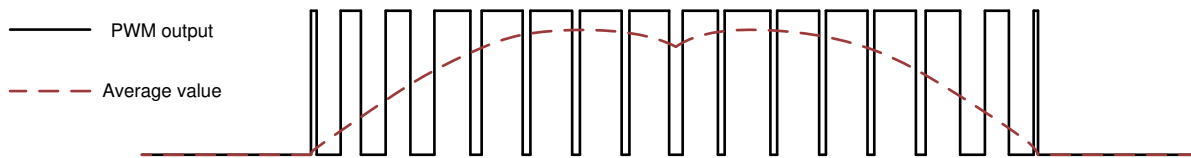


图 7-3. PWM Encoded Phase Output and the Average Value

The output amplitude is determined by the supply voltage (V_{CC}) and the PWM-commanded duty cycle (PWM) as calculated in 式 1 and shown in 图 7-4. The maximum amplitude is applied when the commanded PWM duty cycle is slightly less than 100% in order to keep the 25-kHz PWM rate (f_{PWM_OUT}).

$$V_{ph_pk} = PWM_{dc} \times V_{CC} \quad (1)$$

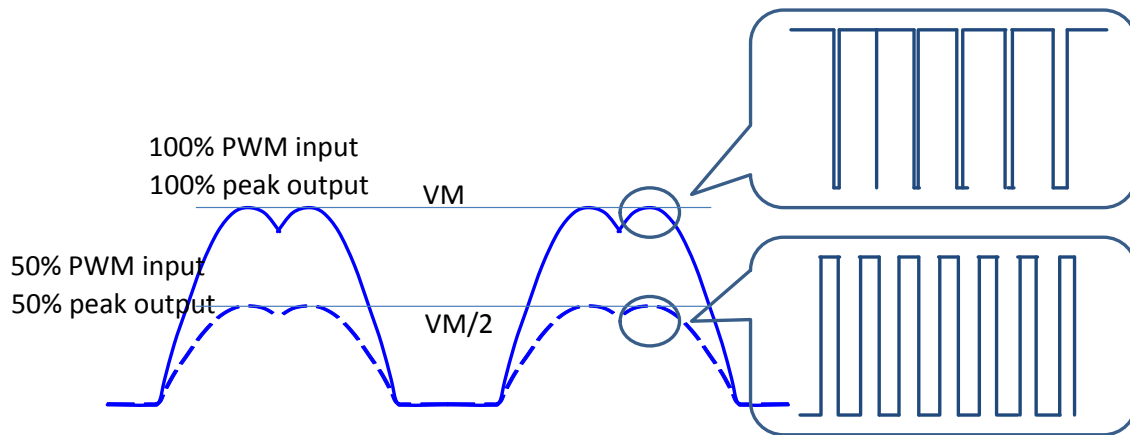


图 7-4. Output Voltage Amplitude Adjustment

The motor speed is controlled indirectly by using the PWM command to control the amplitude of the phase voltages which are applied to the motor. The PWM pin can be driven by either a digital duty cycle or an analog voltage.

The duty cycle of the PWM input (PWM) is passed through a low-pass filter that ramps from 0% to 100% duty cycle in 120 ms. The control resolution is approximately 0.2% (DC_{STEP}). The signal path from PWM input to PWM motor is shown in 图 7-5.

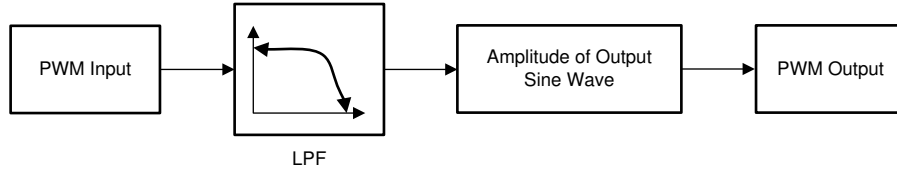


图 7-5. PWM Command Input Control Diagram

The output peak amplitude is described by 式 1 when $PWM_{dc} > 15\%$ (the minimum-operation duty cycle). When the PWM-commanded duty cycle is lower than the minimum-operation duty cycle and higher than 1.5% (DC_{ON_MIN}), the output is controlled the by the minimum-operation duty cycle (DC_{MIN}). This is shown in 图 7-6 for analog input, and for duty cycles greater than 1.5% (DC_{ON_MIN}) for digital input. If the supply voltage (V_{VCC}) > 14 V, the maximum PWM_{dc} is limited to $14 V / V_{VCC}$.

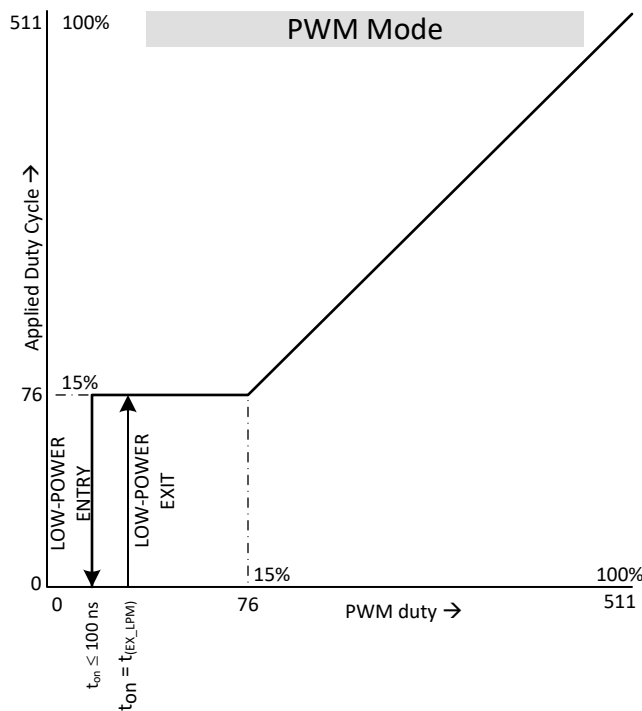
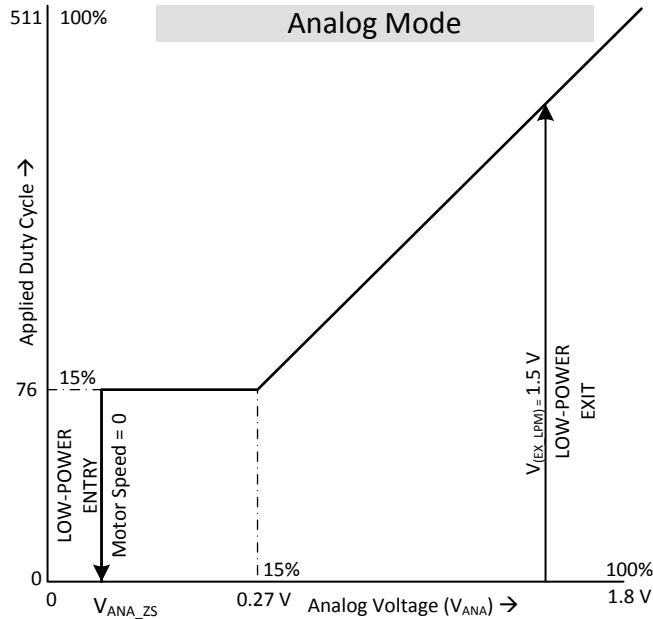


图 7-6. PWM-Mode Speed-Control Transfer Function

When the PWM pin is driven with an analog voltage, the output peak amplitude depends on the supply voltage, the analog voltage on the PWM pin (V_{ANA}), and the voltage of V1P8 (V_{V1P8}). This is shown in 式 2:

$$V_{ph_pk} = \frac{V_{ANA}}{V_{1P8}} \times V_{CC} \tag{2}$$

Note the output peak amplitude is described by 式 2 when the $V_{ANA} > 0.27 V$ or 15% of 1.8 V. This is the equivalent of the minimum-operation duty cycle percentage of 15% (DC_{MIN}). When the analog voltage on the PWM pin is lower than the minimum-operation duty-cycle percentage but higher than the zero-speed analog voltage (V_{ANA_ZS}), the output is controlled by the minimum-operation duty cycle. When the analog voltage on the PWM pin is below zero-speed analog voltage, the DRV10974 enters low-power mode. This is shown in 图 7-7.



7-7. Analog-Mode Speed-Control Transfer Function

7.3.2 Motor Direction Change

The DRV10974 device can be easily configured to drive the motor in either direction by setting the input on the FR (forward-reverse) pin to a logic 1 or logic 0 state. The direction of commutation as described by the commutation sequence is defined as follows:

FR = 0	U→V→W
FR = 1	U→W→V

7.3.3 Motor-Frequency Feedback (FG)

During operation of the DRV10974 device, the FG pin provides an indication of the speed of the motor. The FG pin toggles at a rate of one time during an electrical cycle. Using this information and the number of pole pairs in the motor, use 式 3 to calculate the mechanical speed of the motor.

$$\text{RPM} = \frac{f_{(\text{FG})} \times 60}{\text{pole_pairs}} \quad (3)$$

During open-loop acceleration the FG pin indicates the frequency of the signal that is driving the motor. The lock condition of the motor is unknown during open-loop acceleration and therefore the FG pin could toggle during this time even though the motor is not moving.

During spin down, the DRV10974 device continues to provide speed feedback on the FG pin. The DRV10974 device provides the output of the U-phase comparator on the FG pin until the motor speed drops below 10 Hz ($f_{\text{FG_MIN}}$). When the motor speed falls below 10 Hz, the device enters into the low-power mode and the FG output is held at a logic high.

7.3.4 Lock Detection

When the motor is locked by some external condition, the DRV10974 device detects the lock condition and acts to protect the motor and the device. The lock condition must be properly detected whether the condition occurs as a result of a slowly increasing load or a sudden shock.

The DRV10974 device reacts to the lock condition by stopping the motor drive. To stop driving the motor, the phase outputs are placed into a high-impedance state. After successfully transitioning into a high-impedance

state as the result of a lock condition, the DRV10974 device attempts to restart the motor after $t_{(LOCK_OFF)}$ seconds.

The DRV10974 device has a comprehensive lock-detect function that includes six different lock-detect schemes. Each of these schemes detects a particular condition of the lock as shown in [Figure 7-8](#).

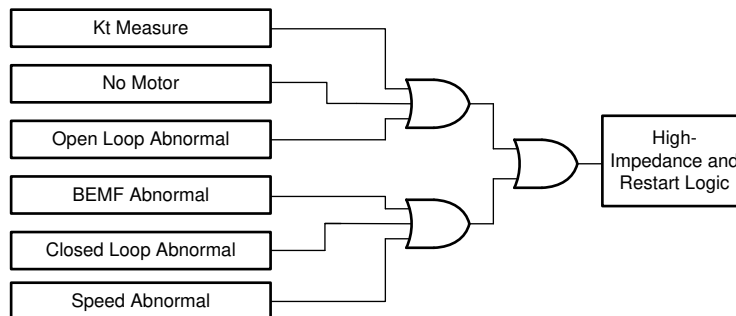


Figure 7-8. Lock Detect

The following sections describe each lock-detect scheme.

7.3.4.1 Lock Kt Measure

The DRV10974 device measures the actual Kt of the motor when transitioning from open-loop acceleration to closed-loop acceleration. If the measured Kt is less than 200 mV, the device indicates that the handoff Kt level was not properly reached and the lock is triggered.

7.3.4.2 Lock No Motor

The phase-U current is checked at the end of the align state. If the phase-U current is not greater than 50 mA, then the motor is not connected. This condition is reported as a lock condition.

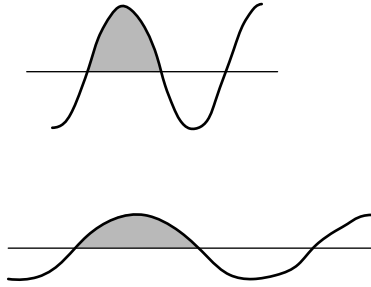
7.3.4.3 Lock Open Loop Abnormal

Transition from open loop to closed loop is based on the estimated value of BEMF. If during open-loop acceleration the electrical commutation rate exceeds 200 Hz without reaching the handoff threshold, this lock is triggered.

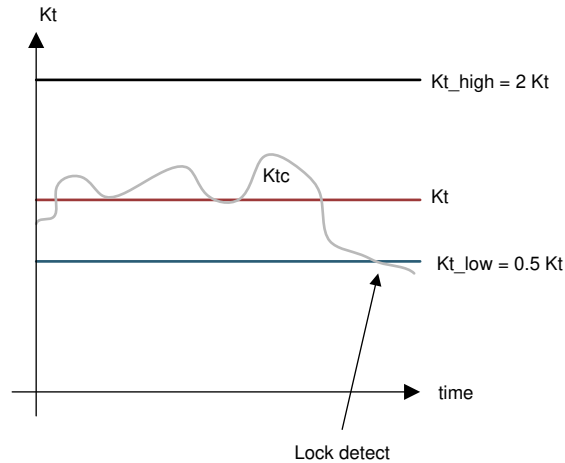
7.3.4.4 Lock BEMF Abnormal

For any specific motor, the integrated value of BEMF during half of an electrical cycle is a constant as shown by the shaded gray area in [Figure 7-9](#). This value is constant regardless of whether the motor runs fast or slow. The DRV10974 device monitors this value and uses it as a criterion to determine if the motor is in a lock condition.

The DRV10974 device uses the integrated BEMF to determine the Kt value of the motor during the initial motor start. Based on this measurement, a range of acceptable Kt values is established. Then, during closed-loop motor operation the Ktc (Kt calculated) value is continuously updated. Finally, the Ktc value is checked to see if it is within the range between $\frac{1}{2} Kt$ and $2Kt$. If the Ktc value goes beyond the acceptable range, a lock condition is triggered as shown in [Figure 7-10](#). Note, there is a blanking period of 0.3 s after the transition from open loop to closed loop where the abnormal BEMF lock is momentarily disabled. The device uses this time to finalize the Kt value that Ktc is compared against.



7-9. BEMF Integration



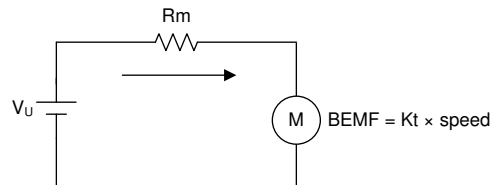
7-10. Abnormal Kt Lock Detect

7.3.4.5 Lock Closed Loop Abnormal

This lock condition is active when the DRV10974 device is operating in the closed-loop mode. The motor is indicated as not moving when the closed-loop commutation period becomes lower than half the previous commutation period. This condition triggers the closed-loop abnormal-lock condition.

7.3.4.6 Lock Speed Abnormal

If the motor is in normal operation, the motor BEMF is always less than the voltage applied to the phase. The sensorless-control algorithm of the DRV10974 device is continuously updating the value of the motor BEMF based on the speed of the motor and the motor Kt as shown in 7-11. If the calculated value for motor BEMF is 1.5 times higher than the applied voltage on phase U (V_U) for an electrical period then an error is present in the system, and the calculated value for motor BEMF is wrong or the motor is out of phase with the commutation logic. When this condition is detected, a lock is triggered.



If speed > $\frac{V_U}{K_t}$
Lock is triggered

7-11. BEMF Monitoring

7.3.5 Soft Current-Limit

The current-limit function provides active protection for preventing damage as a result of high current. The soft current-limit does not use direct-current measurement for protection, but rather, uses the measured motor resistance (R_m) and motor velocity constant (K_t) to limit the voltage applied to the phase (U) such that the current does not exceed the limit value ($I_{(LIMIT)}$). The soft current-limit scheme is shown in 图 7-12 based on the calculation in 式 4.

The soft current-limit is only active when in normal closed-loop mode and does not result in a fault condition nor does it result in the motor being stopped. The soft current-limit is typically useful for limiting the current that results from heavy loading during motor acceleration. The $I_{(LIMIT)}$ current is configured by an external resistor ($R_{(CS)}$) as shown in 表 7-1.

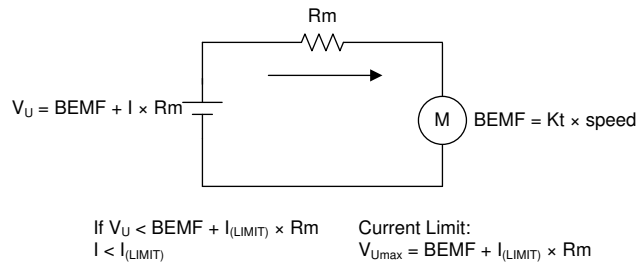


图 7-12. Current Limit

Use 式 4 to calculate the $I_{(LIMIT)}$ value.

$$I_{(LIMIT)} = \frac{V_{(U)LIMIT} - \text{Speed} \times K_t}{R_m} \tag{4}$$

表 7-1 can be used to determine the $I_{(LIMIT)}$ value.

表 7-1. Soft Current-Limit Selections

$R_{(CS)}$ [kΩ] ⁽¹⁾	$I_{(LIMIT)}$ [mA]
7.32	200
16.2	400
25.5	600
38.3	800
54.9	1000
80.6	1200
115	1400
182	1600 (1500 during align)

(1) All resistors are ±1 %.

注

The soft current-limit is not correct if the motor is out of phase with the commutation control logic (locked rotor). The soft current-limit is not effective under this condition.

7.3.6 Short-Circuit Current Protection

The short-circuit current protection function shuts off drive to the motor by placing the motor phases into a high-impedance state if the current in any motor phase exceeds the short-circuit protection limit $I_{(OC_LIMIT)}$. The DRV10974 device goes through the initialization sequence and attempts to restart the motor after the short-

circuit condition is improved. This function is intended to protect the device and the motor from catastrophic failure when subjected to a short-circuit condition.

7.3.7 Overtemperature Protection

The DRV10974 device has a thermal shutdown function which disables the motor operation when the device junction temperature has exceeded the T_{SD} temperature. Motor operation resumes when the junction temperature becomes lower than $T_{SD} - T_{SD(hys)}$.

7.3.8 Undervoltage Protection

The DRV10974 device has an undervoltage lockout feature, which prevents motor operation whenever the supply voltage (V_{CC}) becomes too low. Upon power up, the DRV10974 device operates when V_{CC} rises above $V_{(UVLO_F)} + V_{hys(UVLO)}$. The DRV10974 device continues to operate until V_{CC} falls below $V_{(UVLO_F)}$.

7.4 Device Functional Modes

7.4.1 Spin-Up Settings

7.4.1.1 Motor Start

The DRV10974 device starts the motor using a procedure which is shown in [Figure 7-13](#).

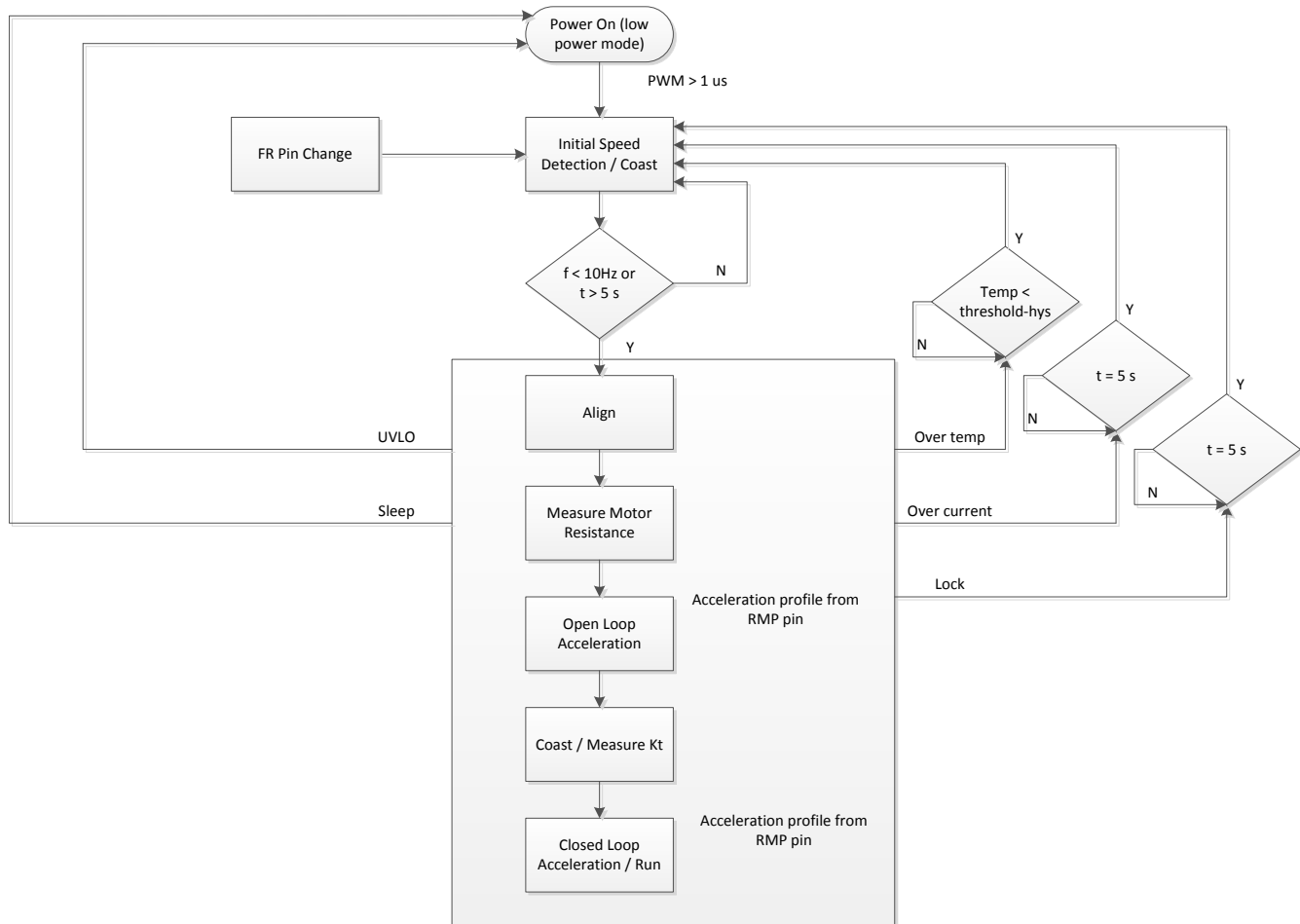


Figure 7-13. DRV10974 Initialization and Motor Start-Up Sequence

7.4.1.2 Initial Speed Detect

Every time the DRV10974 device exits low-power mode, it determines if the motor is spinning using a function called initial speed detect. If the frequency on the FG pin is less than 10 Hz, the motor is considered stationary. If

the frequency is greater than 10 Hz the motor is decelerated until it is below 10 Hz or a 5-second time-out has occurred.

7.4.1.3 Align

To align the rotor to the commutation logic, the DRV10974 device applies a current equivalent to the closed-loop run current to phase U by driving phases V and W equally. This condition is maintained for a maximum of 0.67 s (t_{ALIGN}). To avoid a sudden change in current that could result in undesirable acoustics, the voltage applied to the motor is changed gradually to obtain a current change of 12 A/s.

7.4.2 Open-Loop Acceleration

After the motor is confirmed to be stationary and after completing the motor initialization, the DRV10974 device begins to accelerate the motor. This acceleration is accomplished by applying a voltage to the motor at the appropriate drive state and increasing the rate of commutation without regard to the actual position of the motor (referred to as *open-loop operation*). The function of the open-loop operation is to drive the motor to a minimum speed so that the motor generates sufficient BEMF to allow the commutation control logic to drive the motor accurately.

The motor start-up profile can be configured using an external resistor to set the acceleration profile before transitioning to closed-loop operation. [图 7-14](#) shows this acceleration profile. During closed-loop operation the RMP pin controls the closed-loop acceleration and deceleration. [表 7-2](#) lists the selectable acceleration parameters.

表 7-2. Acceleration Profile Settings

RMP SELECTION	R_{RMP} [k Ω] ⁽¹⁾	Accel2 [Hz/s ²]	Accel1 [Hz/s]	CLOSED-LOOP-ACCELERATION TRANSITION TIME [s] ⁽²⁾	CLOSED-LOOP-DECELERATION TRANSITION TIME [s] ⁽³⁾
0	7.32	0.22	4.6	2.7	44
1	10.7	1.65	9.2	2.7	22
2	14.3	1.65	15	1	22
3	17.8	3.3	25	1	11
4	22.1	7	25	0.2	44
5	28	7	35	0.2	22
6	34	14	50	0.2	22
7	41.2	27	75	0.2	11
8	49.9	27	75	5.4	11
9	59	14	50	8	22
10	71.5	7	35	11	22
11	86.6	7	25	22	44
12	105	3.3	25	5.4	11
13	124	1.65	15	8	22
14	150	1.65	9.2	11	22
15	182	0.22	4.6	22	44

(1) All resistors are $\pm 1\%$

(2) Time to transition from 0 to 100% duty cycle.

(3) Time to transition from 100% to 0% duty cycle.

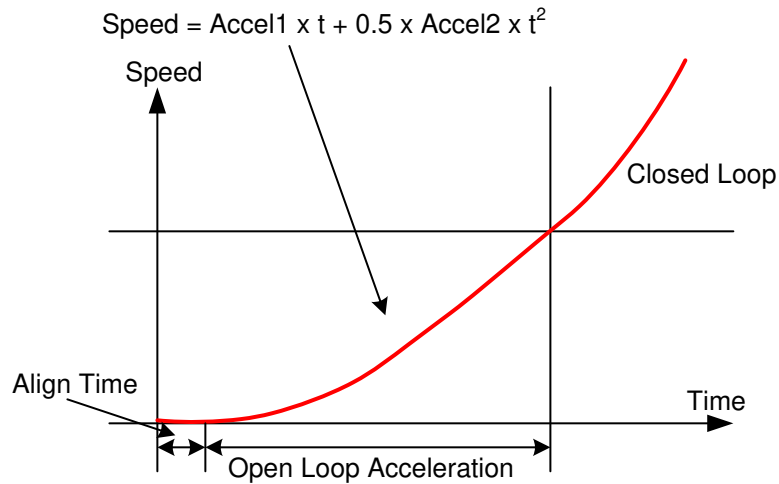


图 7-14. Start-Up Profile

7.4.3 Start-Up Current Sensing

The start-up peak current is controlled by the current-sense limit resistor, $R_{(CS)}$. The start current is set by selecting the $R_{(CS)}$ resistor based on 表 7-3. The current should be selected to allow the motor to accelerate reliably to the handoff threshold. Heavier loads may require a higher current setting, but the rate of acceleration is limited by the selected resistor, $R_{(RMP)}$.

表 7-3. Start-Up Current Limit

$R_{(CS)}$ [k Ω] ⁽¹⁾	$I_{(LIMIT)}$ [mA]
7.32	200
16.2	400
25.5	600
38.3	800
54.9	1000
80.6	1200
115	1400
182	1600 (1500 for align)

(1) All resistors are $\pm 1\%$.

7.4.4 Closed Loop

When the motor accelerates to the target BEMF threshold, commutation control transitions from open-loop mode to closed-loop mode. During this transition, the motor is allowed to coast for one electrical cycle to measure K_t . The commutation drive sequence and timing are determined by the internal control algorithm, and the applied voltage is determined by the PWM-commanded duty-cycle input. The closed-loop acceleration and deceleration values are provided in 表 7-2.

7.4.5 Control Advance Angle

To achieve the best efficiency, the drive state of the motor must be controlled such that the current is aligned with the BEMF voltage of the motor. 图 7-15 illustrates the operation when the drive angle has been optimized. For complete flexibility, the DRV10974 device offers a wide range of fixed lead times. The options for lead time are controlled by a resistor on the ADV pin. The values available are shown in 表 7-4.

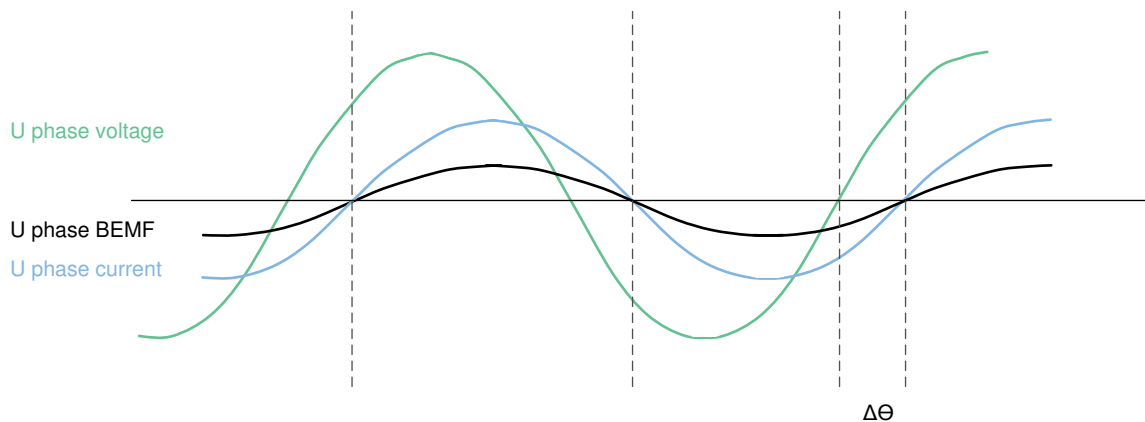


图 7-15. Drive Angle Adjustment

表 7-4. Lead Time Selection

R_{ADV} [kΩ]⁽¹⁾	LEAD TIME [μs]
10.7	10
14.3	25
17.8	50
22.1	100
28	150
34	200
41.2	250
49.9	300
59	400
71.5	500
86.6	600
105	700
124	800
150	900
182	1000

(1) All resistors are ±1%.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV10974 device is used in sensorless 3-phase BLDC motor control. The driver provides a high-performance, high-reliability, flexible, and simple solution for appliance fan, pump, and blower applications. The following design shows a common application of the DRV10974 device.

8.2 Typical Application

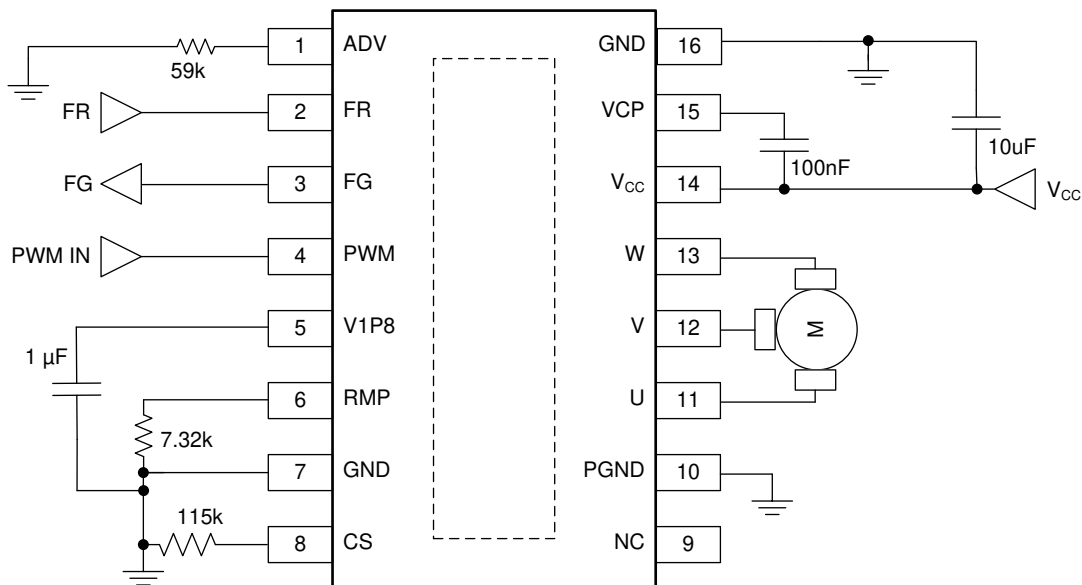


图 8-1. Typical Application Schematic

表 8-1. Recommended External Components

NODE 1	NODE 2	COMPONENT
V _{CC}	GND	10-µF, 25-V ceramic capacitor tied from V _{CC} to ground
VCP	V _{CC}	100-nF, 10-V ceramic capacitor tied from VCP to V _{CC}
V1P8	GND	1-µF ±30%, 6.3-V ceramic capacitor tied from V1P8 to ground
RMP	GND	1%, 1/8 watt resistor tied from RMP to ground to set the desired acceleration profile
CS	GND	1%, 1/8-watt resistor tied from CS to ground to set the desired current limit
ADV	GND	1%, 1/8-watt resistor tied from ADV to ground to set the desired lead angle (time)

8.2.1 Design Requirements

表 8-2 provides design input parameters and motor parameters for system design.

表 8-2. Recommended Application Range

		MIN	NOM	MAX	UNIT
Motor voltage		4.4	12	18	V
BEMF constant	Phase to center tap, measured while motor is coasting	5		150	mV/Hz
Motor phase resistance	Phase to center tap	1		20	Ω
Motor electrical constant	1 phase; inductance divided by resistance, measured phase to phase, yields the electrical constant for 1 phase.	100		5000	μ s
Motor winding current (rms)				1	A
Absolute maximum current	During locked condition			2.5	A

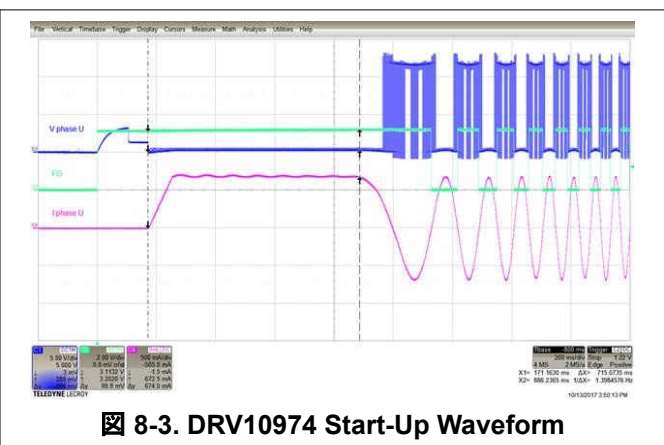
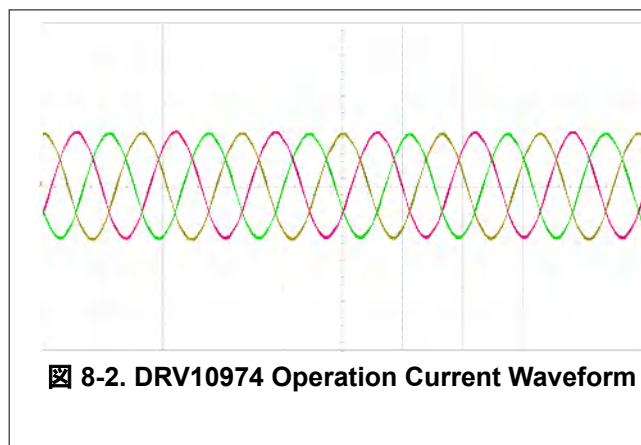
8.2.2 Detailed Design Procedure

Assuming the motor used in the application falls within the recommended application range shown in 表 8-2, the DRV10974 device is simple and intuitive to interface with. The DRV10974 device receives a PWM input that it uses to control the speed of the motor. The duty cycle of the PWM input is used to determine the magnitude of the voltage applied to the motor. The resulting motor speed can be monitored on the FG pin. The FR pin is used to control the direction of rotation for the motor. As a result, the only configuration and customization is dictated by the RMP, ADV, and CS pins.

The resistor on the CS pin is usually determined by the application specifications. Because the CS pin determines the current limit, specifications such as motor current or input power can determine what value the current limit can be set to. Then, the RMP and ADV resistors must be set experimentally through tuning. The RMP pin sets the acceleration profile of the motor. If the RMP pin is set to faster acceleration, the motor starts up faster but may be more likely to fail start-up. In addition, the ADV resistor controls the lead time so the applied current is aligned with the BEMF of the motor. If the ADV resistor is incorrectly selected, the motor may not run efficiently or at all.

As a result, the RMP pin is usually set to the slowest profile while ADV is correctly tuned. Then, the RMP can be set to a different value that allows for a faster acceleration with no impact to start-up reliability. This process, and other design considerations, are documented extensively in the [DRV10974 Technical Documents](#) tab on the DRV10974 product page.

8.2.3 Application Curves



9 Power Supply Recommendations

The DRV10974 device is designed to operate from an input voltage supply, V_{CC} , range between 4.4 V and 18 V. The user must place a minimum of a 10- μ F capacitor rated for V_{CC} between the V_{CC} and GND pins and as close as possible to the V_{CC} and GND pins.

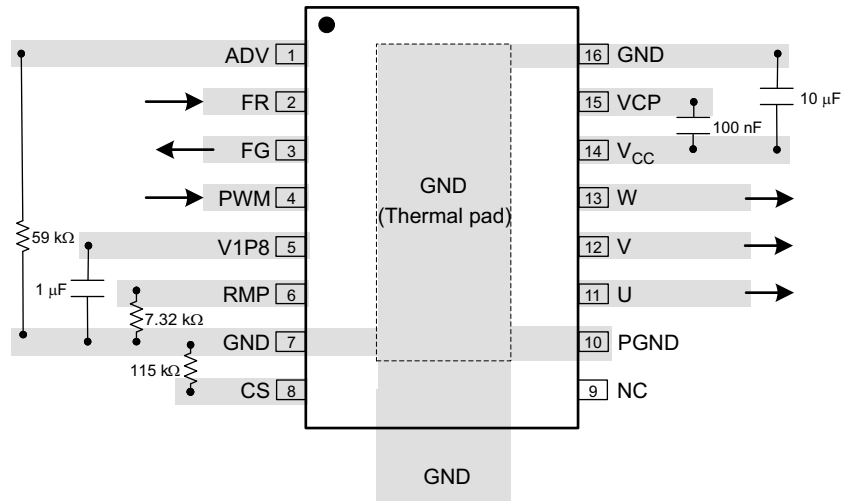
If the power supply ripple is more than 200 mV, in addition to the local decoupling capacitors, a bulk capacitance is required and must be sized according to the application requirements.

10 Layout

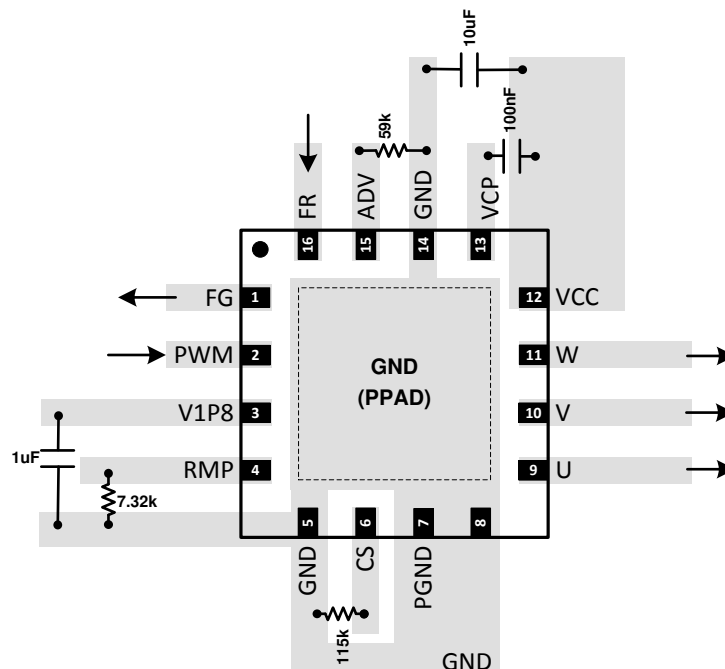
10.1 Layout Guidelines

- Use thick traces when routing to the V_{CC} , GND, U, V, and W pins, because high current passes through these traces.
- Place the 10- μF capacitor between V_{CC} and GND, and as close to the V_{CC} and GND pins as possible.
- Place the 100-nF capacitor between VCP and V_{CC} , and as close to the VCP and V_{CC} pins as possible.
- Connect GND and PGND under the thermal pad.
- Keep the thermal pad connection as large as possible. It should be one piece of copper without any gaps.

10.2 Layout Example



☒ 10-1. HTSSOP Layout Example



☒ 10-2. QFN Layout Example

11 Device and Documentation Support

11.1 Device Support

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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11.4 Trademarks

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11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV10974PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	10974	Samples
DRV10974RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 10974	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV10974PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV10974RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

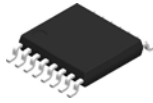

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV10974PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
DRV10974RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

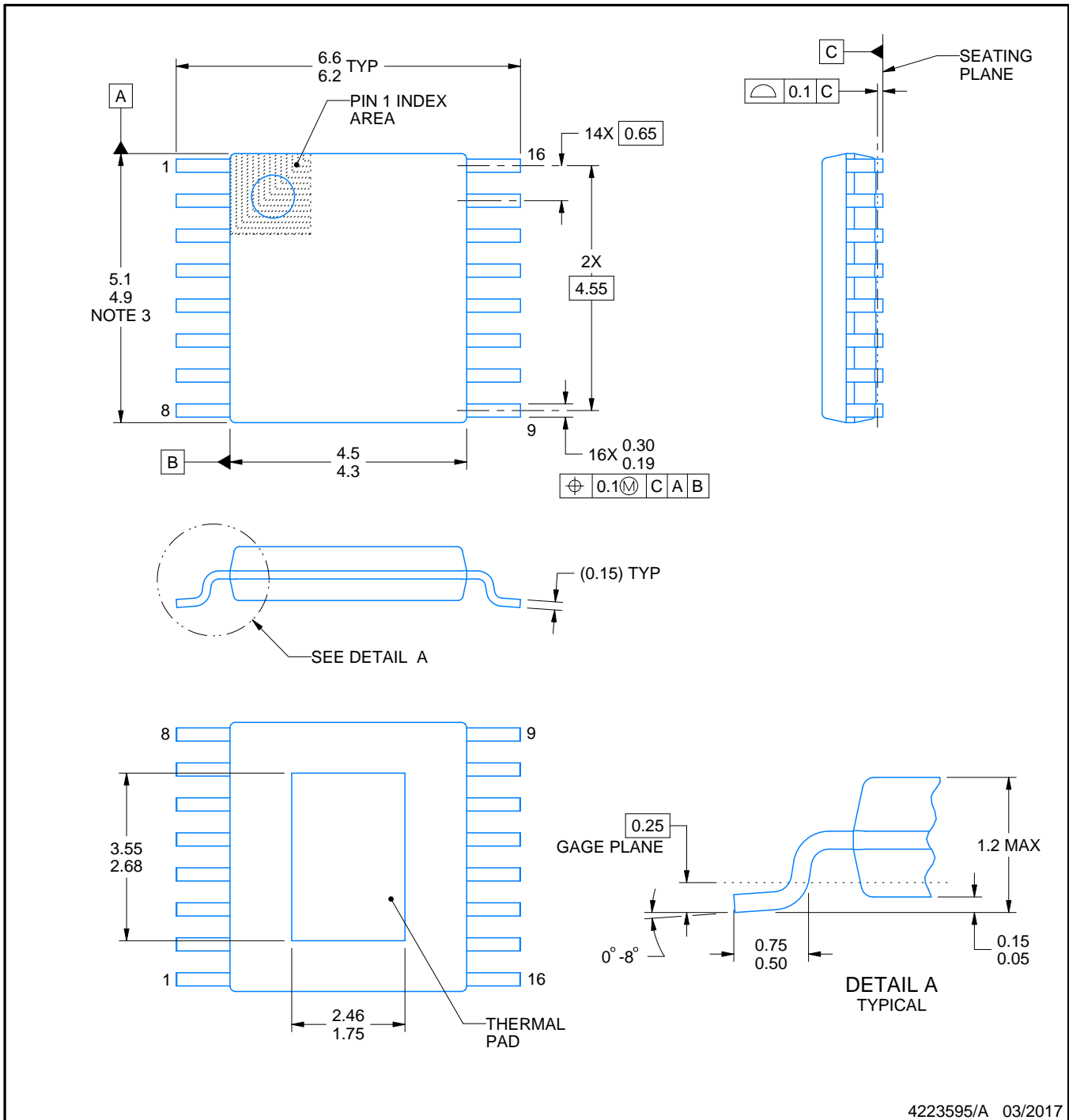
PWP0016J



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

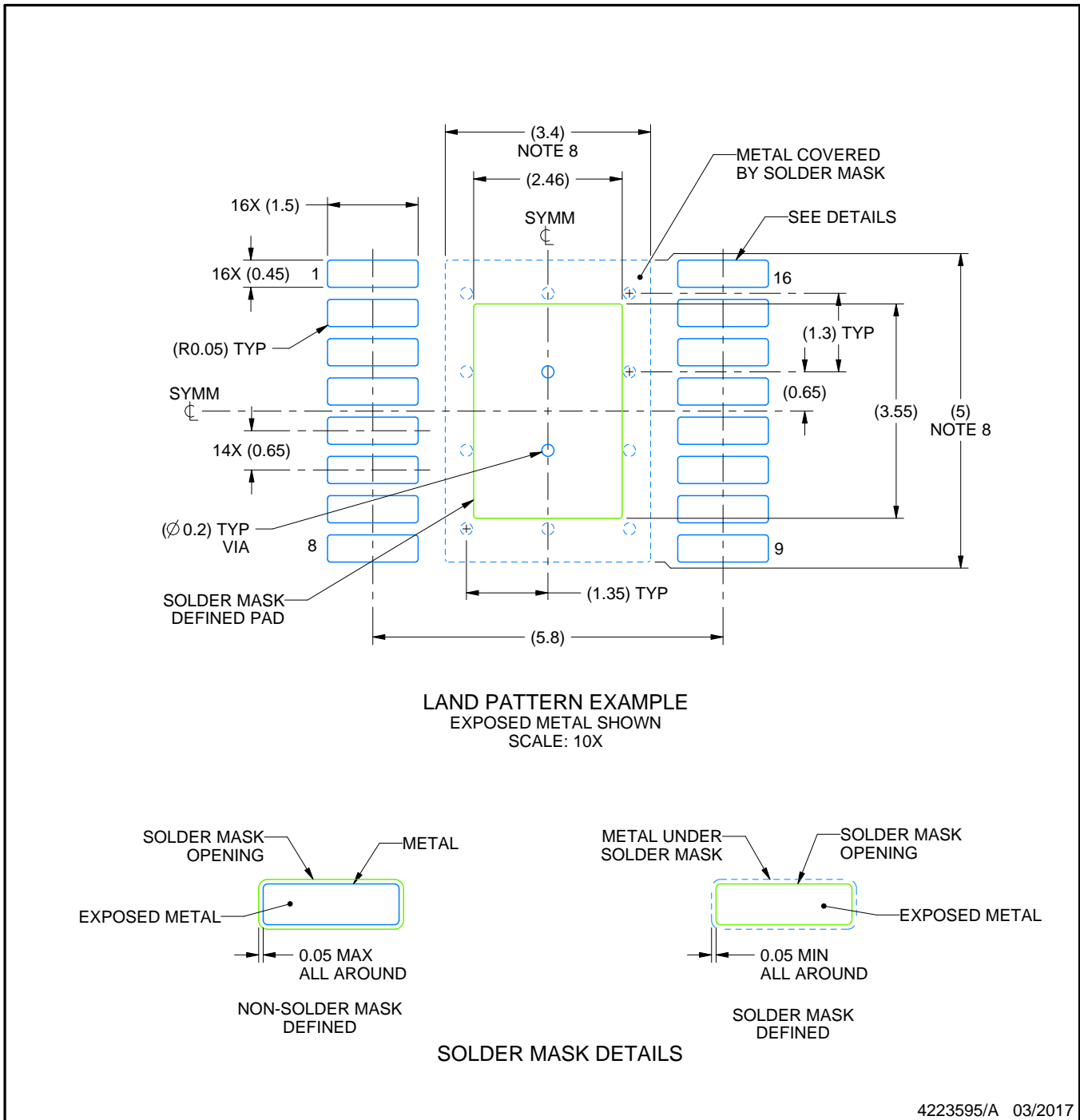
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

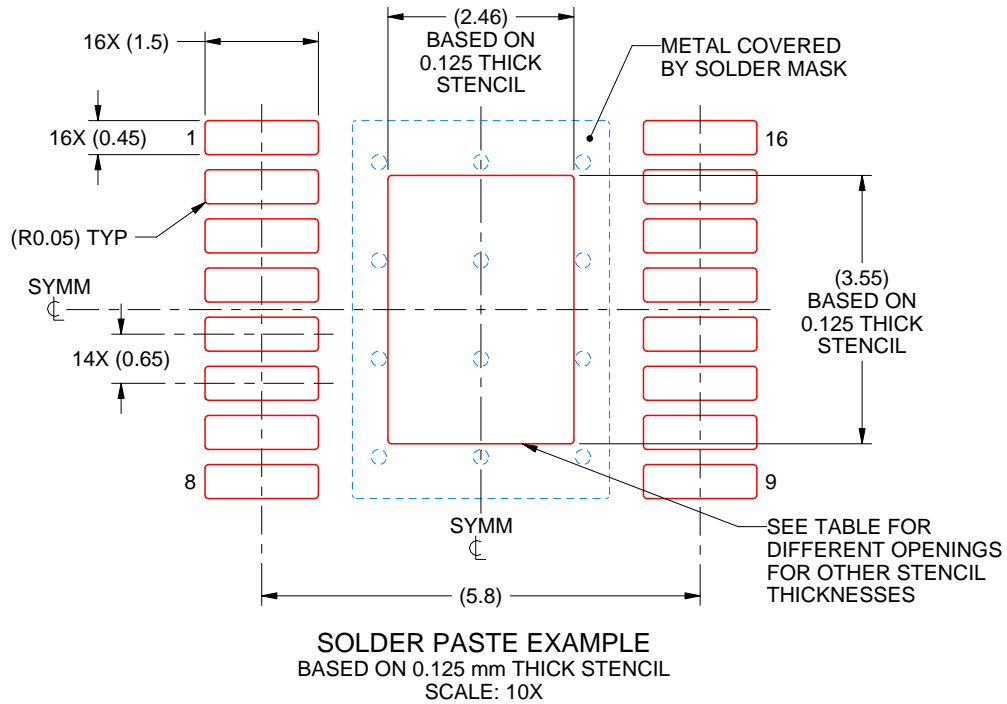
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

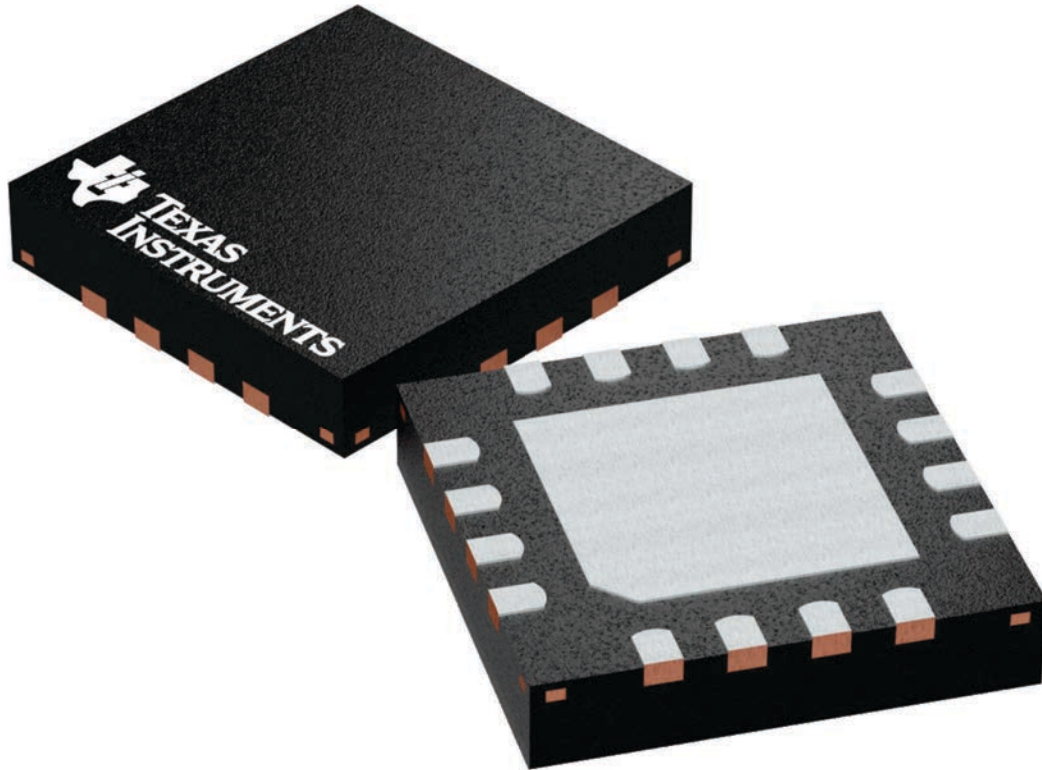
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

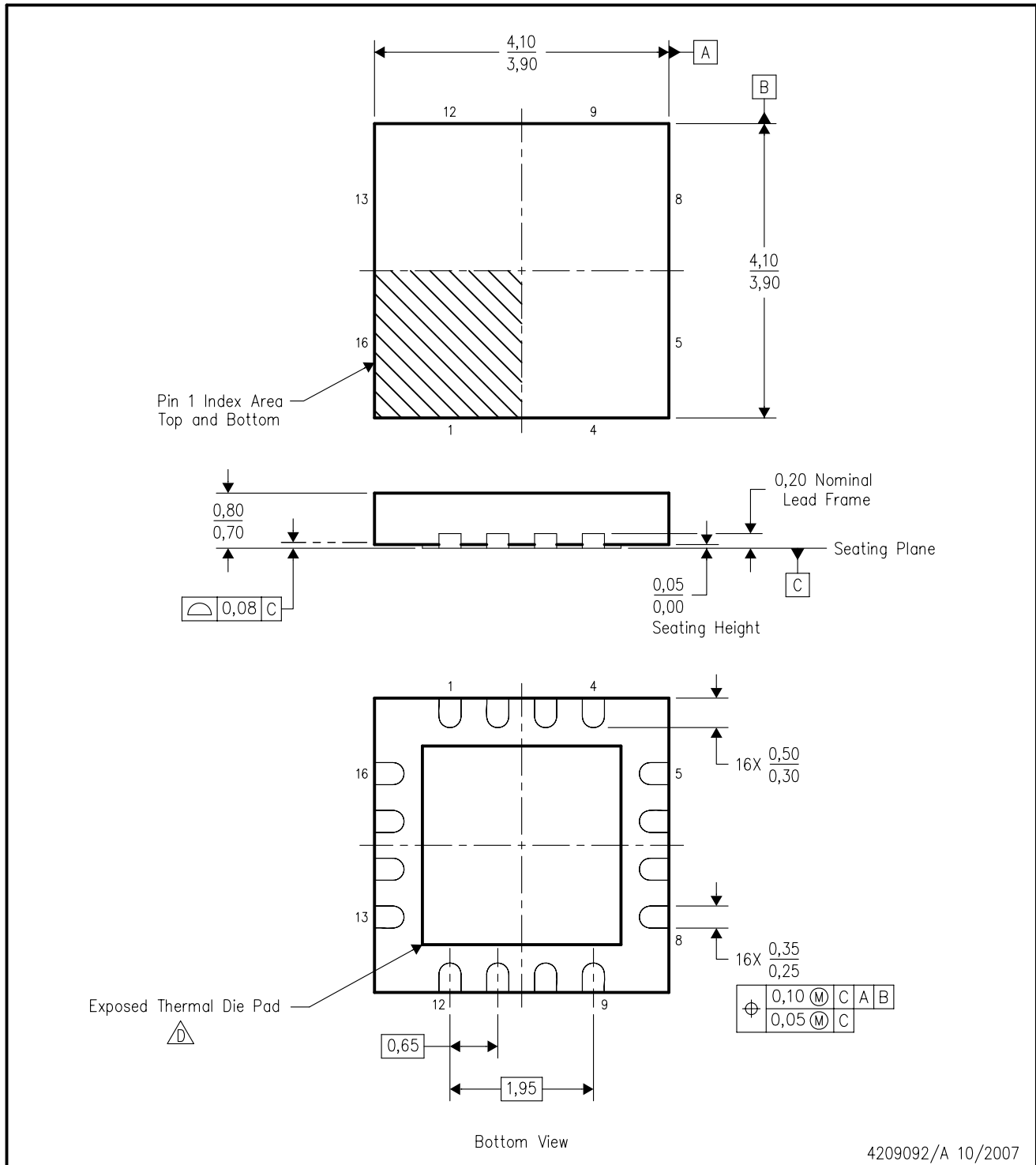
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224843/A

RUM (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4209092/A 10/2007

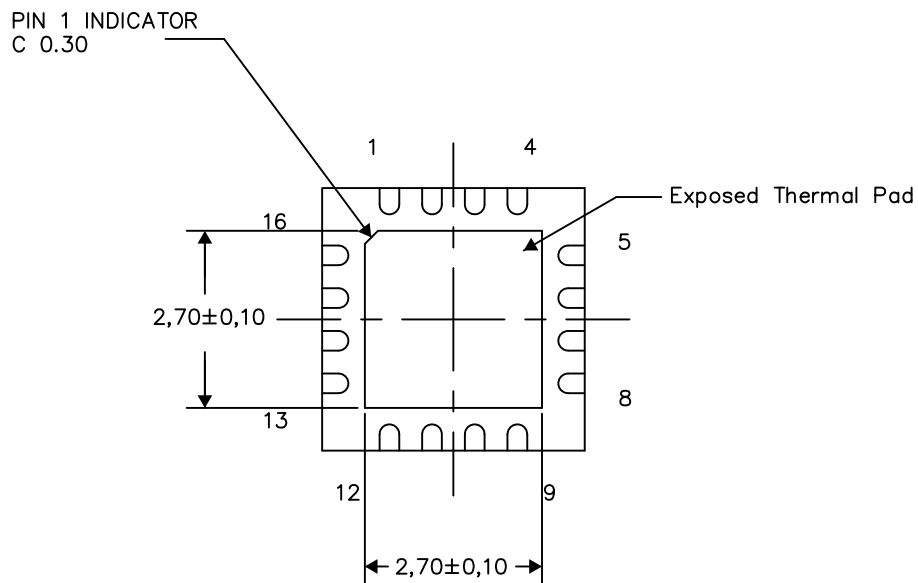
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Package complies to JEDEC MO-220 variation WGGC-3.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

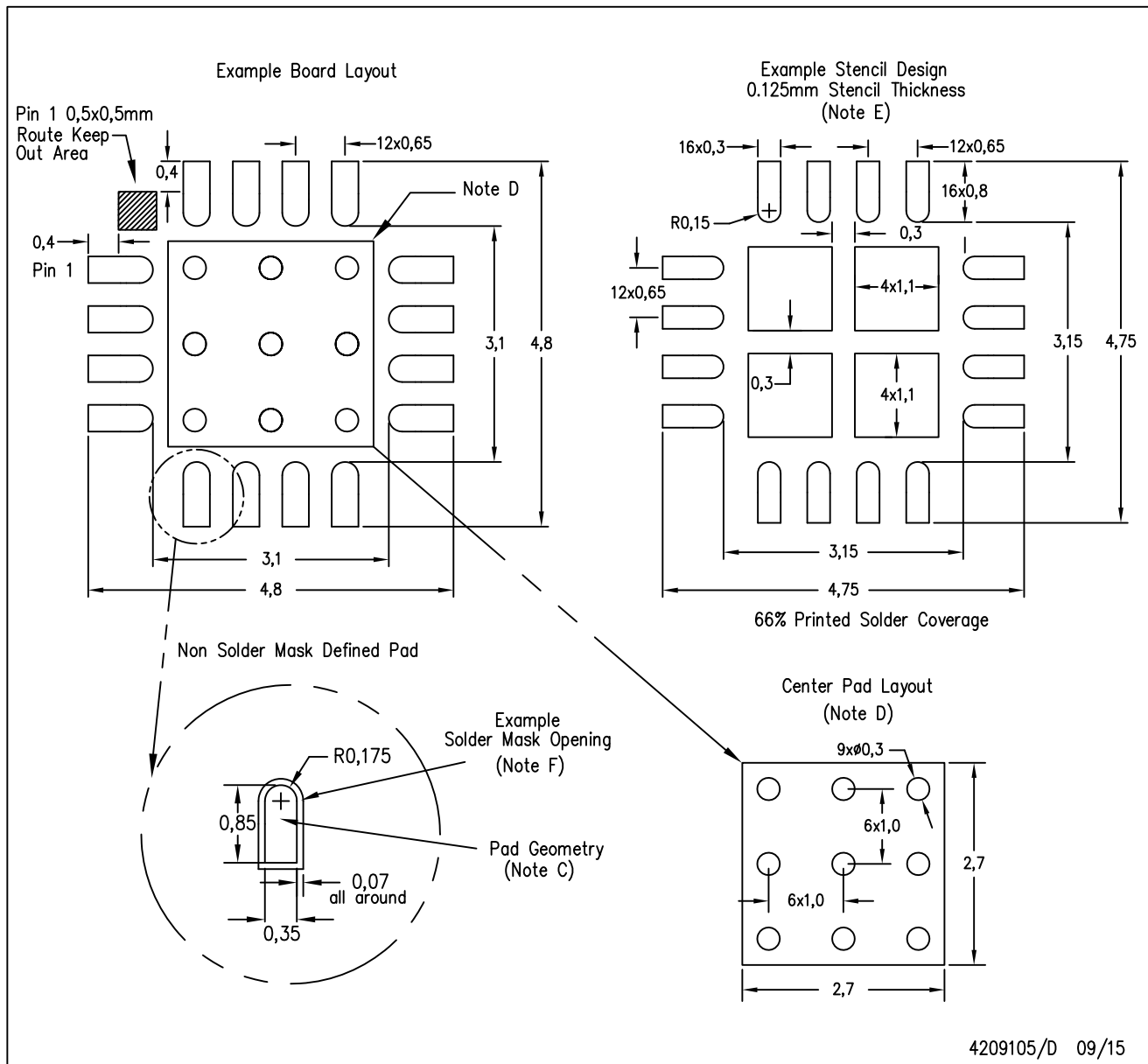
Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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