

DRV2510-Q1 3A 車載用、ソレノイドおよび音声コイル用ハプティックドライバ、診断機能内蔵

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: -40°C ~ 125°C, T_A
- 広い動作電圧範囲 (4.5V ~ 18V)
- 負荷ダンプ保護を内蔵 (40V)
- 高い電流ドライブ (3A ピーク)
- 低い R_{DS(on)}、完全な H ブリッジ出力
- 診断機能内蔵
- フォルト保護機能内蔵
 - ISO-7637-2 準拠の 40V 負荷ダンプ保護
 - 短絡保護
 - 過熱保護機能
 - 過電圧および低電圧保護
 - 障害通知
- アナログ入力
- I²C 通信
- 専用の割り込みピン
- ISO9000: 2002 TS16949 認定済み

2 アプリケーション

- 電磁気アクチュエータドライバ
 - 音声コイル
 - ソレノイド
- 機械式ボタンの置き換え
- 車載用ハプティックアプリケーション
 - インフォテインメント
 - 中央コンソール
 - ステアリング ホイール
 - ドア パネル
 - シート

3 概要

DRV2510-Q1 デバイスは、大電流のハプティックドライバで、ソレノイドや音声コイルなど誘導性の負荷に特化して設計されています。

出力段は、完全な H ブリッジで構成され、3A のピーク電流を供給できます。

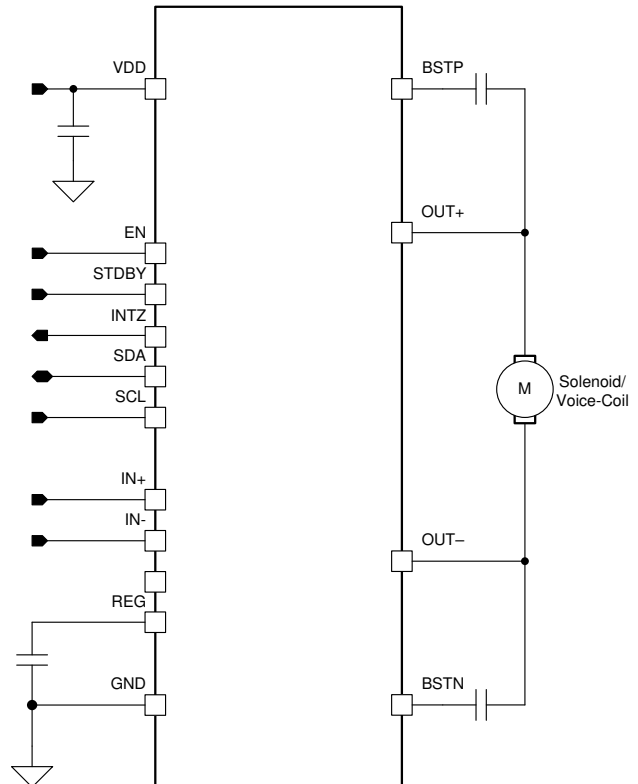
DRV2510-Q1 デバイスは、低電圧誤動作防止、過電流保護、過熱保護などの保護機能を備えています。

DRV2510-Q1 デバイスは車載用に認定済みです。負荷ダンプ保護が搭載されているため、外付け電圧クランプのコストとサイズを減らすことができ、オンボードの負荷診断機能によりデジタル インターフェイス経由でアクチュエータの状態が報告されます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
DRV2510-Q1	HTSSOP (16)	5.00 mm x 4.40 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図






Table of Contents

1 特長.....	1	7.5 Programming.....	14
2 アプリケーション.....	1	7.6 Register Map.....	17
3 概要.....	1	8 Application and Implementation.....	20
4 Revision History.....	2	8.1 Application Information.....	20
5 Pin Configuration and Functions.....	4	8.2 Typical Applications.....	20
6 Specifications.....	5	9 Power Supply Recommendations.....	24
6.1 Absolute Maximum Ratings.....	5	10 Layout.....	24
6.2 ESD Ratings.....	5	10.1 Layout Guidelines.....	24
6.3 Recommended Operating Conditions.....	5	10.2 Layout Example.....	24
6.4 Thermal Information.....	5	11 Device and Documentation Support.....	25
6.5 Electrical Characteristics.....	6	11.1 Device Support.....	25
6.6 Timing Requirements.....	7	11.2 ドキュメントの更新通知を受け取る方法.....	25
6.7 Switching Characteristics.....	7	11.3 サポート・リソース.....	25
6.8 Typical Characteristics.....	8	11.4 Trademarks.....	25
7 Detailed Description.....	9	11.5 静電気放電に関する注意事項.....	25
7.1 Overview.....	9	11.6 用語集.....	25
7.2 Functional Block Diagram.....	9	12 Mechanical, Packaging, and Orderable Information.....	25
7.3 Feature Description.....	10		
7.4 Device Functional Modes.....	13		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (May 2020) to Revision D (November 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1

Changes from Revision B (September 2016) to Revision C (May 2020)	Page
• 車載用の「特長」を「特長」リストの先頭に移動.....	1
• Added Junction temperature to the <i>Absolute Maximum Ratings</i>	5
• Changed the <i>ESD Ratings</i> table.....	5
• Added INTZ Report to the <i>Electrical Characteristics</i> table.....	6
• Changed  7-1.....	10
• Changed From: "The load diagnostic function runs on de-assertion" To: "The load diagnostic function runs on assertion" in the <i>Load Diagnostics</i> section.....	11
• Added the <i>Protection and Monitoring</i> section.....	12
• Changed From: "NRST pin..." To: "EN pin..." in the <i>Operation in Shutdown Mode</i> section.....	13
• Changed From: When EN is asserted (logic low) To: When EN is de-asserted (logic low) in the <i>Operation in Shutdown Mode</i> section.....	13
• Deleted register 0x00 from the <i>Register Map</i> section.....	17
• Changed register Address: 0x03.....	19
• Changed the <i>Single-Ended Source</i> section and  8-1.....	20
• Changed from: BSTA and BSTB to: BSTP and BSTN in the <i>Capacitor Selection</i> section.....	21
• Changed the <i>Differential Input Diagram</i> section and  8-6.....	23

Changes from Revision A (June 2016) to Revision B (September 2016) **Page**

- 「特長」の「車載用認定済み (Q100)」を「AEC-Q100 グレード 2 準拠を認定済み」に変更..... 1
 - 「特長」の「広い動作電圧範囲 (5V~18V)」を「広い動作電圧範囲 (4.5V~18V)」に変更..... 1
 - 「特長」に以下を追加: 「ISO9000: 2002 TS16949 認定済み」..... 1
 - Changed the VDD MIN value From: 5 V to: 4.5 V in the [セクション 6.3](#) 5
 - Changed From: operates from 5 V – 18 V To: operates from 4.5 V – 18 V in the [セクション 9](#) 24
-

Changes from Revision * (June 2016) to Revision A (June 2016) **Page**

- 量産データとしてリリース。 1
-

5 Pin Configuration and Functions

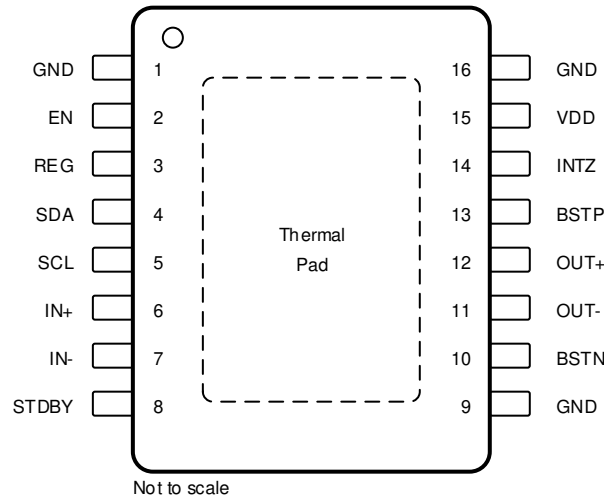


図 5-1. TWP Package HTSSOP 16-Pin With Thermal Pad Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 9, 16	P	Ground.
EN	2	I	Device enable pin.
REG	3	P	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 μ F X7R ceramic decoupling capacitor and the MODE resistor divider.
SDA	4	I	I ² C data.
SCL	5	I	I ² C clock.
IN+	6	I	Positive differential input.
IN-	7	I	Negative differential input.
STDBY	8	I	Standby pin.
BSTN	10	P	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUT-.
OUT-	11	O	Negative output.
OUT+	12	O	Positive output.
BSTP	13	P	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUT+.
INTZ	14	O	General fault reporting. Open drain. INTZ = High, normal operation INTZ = Low, fault condition
VDD	15	P	Power supply.
Thermal Pad		G	Connect to GND for best system performance. If not connected to GND, leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	VDD DC supply voltage range	-0.3	30	V
	VDD pulsed supply voltage range. t < 400 ms exposure	-1	40	
	VDD supply voltage ramp rate		15	V/ms
Input voltage, V _I	SCL, SDA, EN	-0.3	5	V
	IN+, IN-, STDBY	-0.3	6.5	
Current	DC current on VDD, GND, OUT+, OUT-	-4	4	A
	Maximum current in all input pins	-1	1	mA
	Maximum sink current for open-drain pins		7	
Operating free-air temperature, T _A		-40	125	°C
Junction temperature, T _J		-40	150	
Storage temperature range, T _{stg}		-55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level H2	±3500	V
	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage. VDD.	4.5		18	V
V _{IH}	High-level input voltage. SDA, SCL, STDBY, EN.	2.1			V
V _{IL}	Low-level input voltage. SDA, SCL, STDBY, EN			0.7	V
V _{OL}	Low-level output voltage			0.4	V
V _{OH}	High-level output voltage	2.4			V
I _{IH}	High-level input current. SDA, SCL, STDBY, EN			50	µA
R _L	Minimum load Impedance		1.5		Ω
C _B	Load capacitance for each bus line (SDA/SCL)			400	pF

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV2510-Q1	UNIT
		PWP (HTSSOP)	
		{16} PINS	
R _{θJA}	Junction-to-ambient thermal resistance	39.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	24.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	20	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19.8	°C/W

THERMAL METRIC ⁽¹⁾		DRV2510-Q1	UNIT
		PWP (HTSSOP)	
		{16} PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

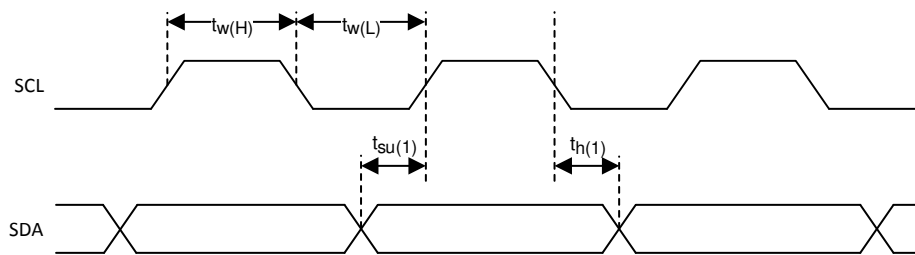
T_A = 25°C, AVCC = VDD = 12 V, R_L = 5 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Output offset voltage (measured differentially)	V _I = 0 V, Gain = 20 dB	-25		25	mV
I _{VDD}	Quiescent supply current	No load or filter		16		mA
I _{VDD(SD)}	Quiescent supply current in shutdown mode	No load or filter		5	20	μA
I _{VDD(STD BY)}	Quiescent supply current in standby mode	No load or filter		7		mA
r _{DS(on)}	Drain-source on-state resistance, measured pin to pin	T _J = 25°C		180		mΩ
G	Gain	P _(o) = 1 W	19	20	21	dB
			25	26	27	
			31	32	33	dB
			35	36	37	
V _{REG}	Regulator voltage		6.4	6.9	7.4	V
V _O	Output voltage (measured differentially)			20		V
PSRR	Power supply ripple rejection	VDD = 12 V + 1 Vrms at 1 kHz		75		dB
V _{ICMIN}	Input common-mode min			0.3		V
V _{ICMAX}	Input common-mode max			4.4		
CMRR	Common-mode rejection ratio	f = 1 kHz, 100 mVrms referenced to GND. Gain = 20 dB		63		dB
f _{OSC}	Oscillator frequency (with PWM duty cycle < 96%)			400		kHz
				500		
	Output resistance in shutdown			10		MΩ
	Resistance to detect a short from OUT pin(s) to VDD or GND				200	Ω
	Open-circuit detection threshold		75	95	120	Ω
	Short-circuit detection threshold		0.9	1.2	1.5	Ω
	Power-on threshold			4.1		V
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C
	Over-current trip point			3.5		A
	Over-voltage trip point			21		V
	Over-voltage hysteresis			0.6		V
	Under-voltage trip point			4		V
	Under-voltage hysteresis			0.25		V
INTZ Report						
	INTZ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V	2.4			V
	INTZ pin output voltage for logic-level low (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V			0.5	V

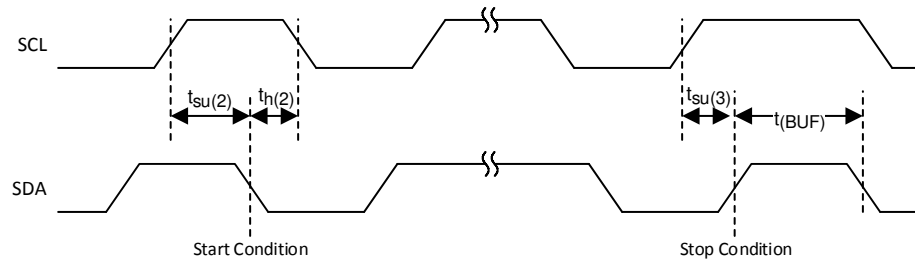
6.6 Timing Requirements

$T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = 3.6\text{ V}$ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Frequency at the SCL pin with no wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high	0.6			μs
$t_{w(L)}$	Pulse duration, SCL low	1.3			μs
$t_{su(1)}$	Setup time, SDA to SCL	100			ns
$t_{h(1)}$	Hold time, SCL to SDA	300			ns
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			μs
$t_{su(2)}$	Setup time, SCL to start condition	0.6			μs
$t_{h(2)}$	Hold time, start condition to SCL	0.6			μs
$t_{su(3)}$	Setup time, SCL to stop condition	0.6			μs



6-1. SCL and SDA Timing



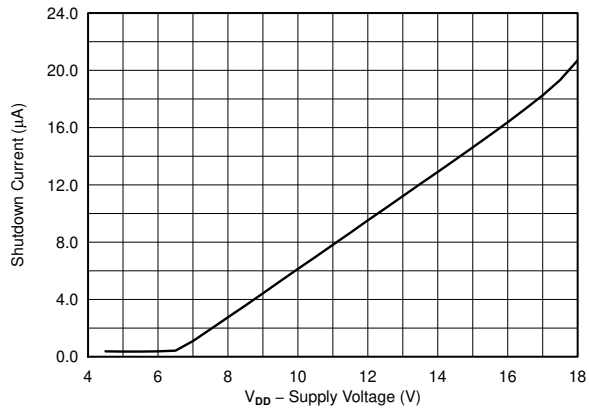
6-2. Timing for Start and Stop Conditions

6.7 Switching Characteristics

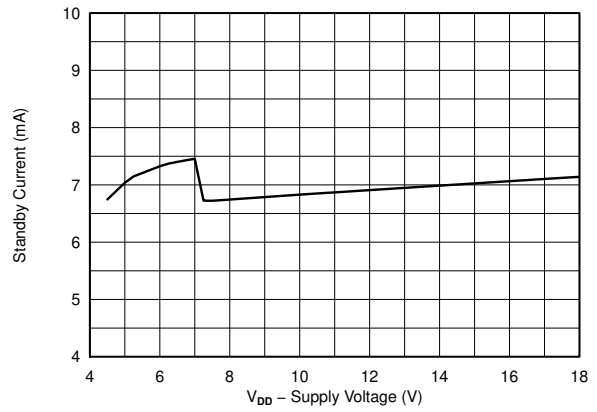
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on-sd}	Turn-on time from shutdown to waveform EN = Low to High, STBY = Low		229		ms
t_{OFF-sd}	Turn-off time EN = High to Low		47		μs
$t_{on-stdby}$	Turn-on time from standby to waveform EN = High, STBY = High to Low		32		μs

6.8 Typical Characteristics



6-3. Shutdown Current vs VDD Voltage



6-4. Standby Current vs VDD Voltage

7 Detailed Description

7.1 Overview

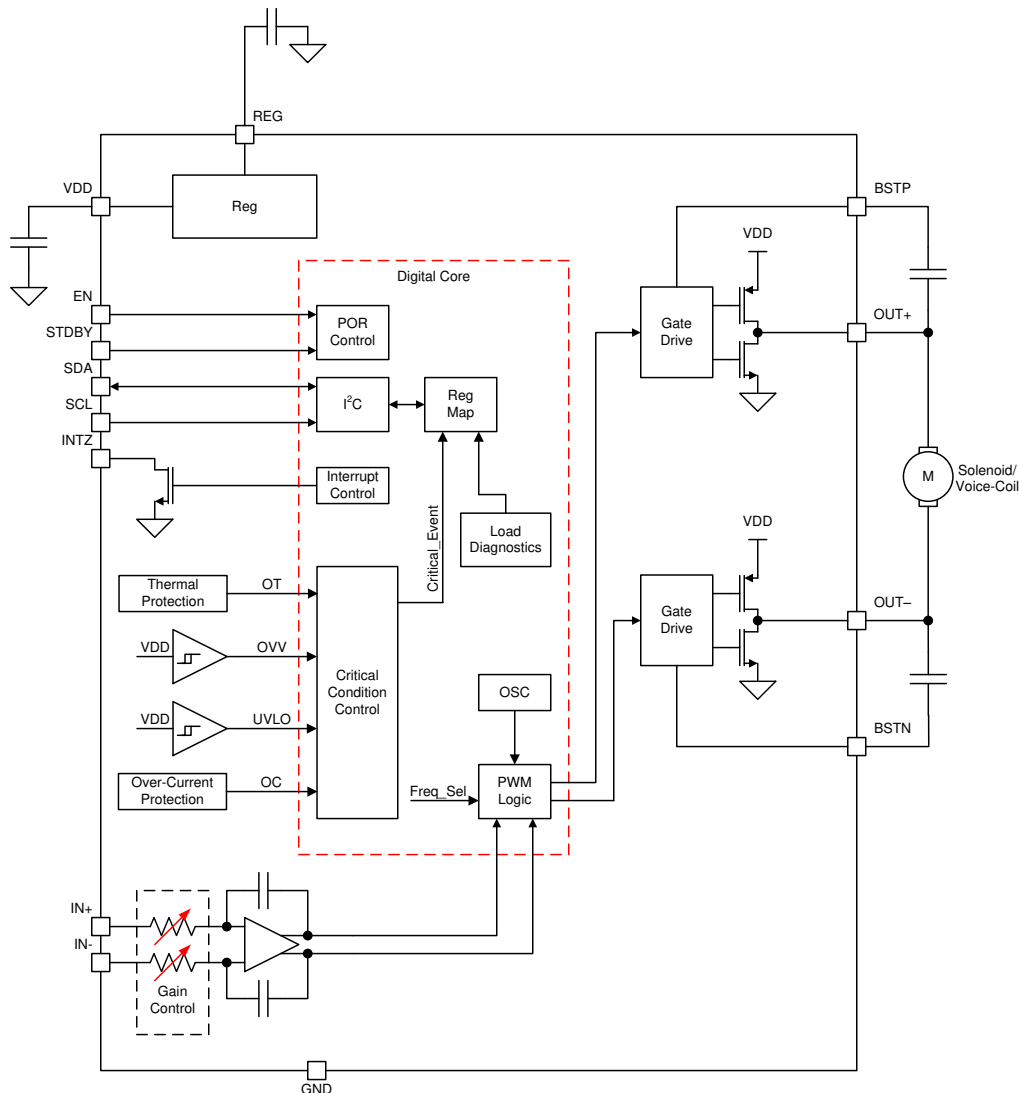
The DRV2510-Q1 device is a high current haptic driver specifically designed for inductive loads, such as solenoids and voice coils.

The output stage consists of a full H-bridge capable of delivering 3 A of peak current.

The design uses an ultra-efficient switching output technology developed by Texas Instruments, but with features added for the automotive industry. The DRV2510-Q1 device provides protection functions such as undervoltage lockout, over-current protection and over-temperature protection. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system.

The DRV2510-Q1 device is automotive qualified. The integrated load-dump protection reduces external voltage clamp cost and size, and the onboard load diagnostics report the status of the actuator through the digital interface.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Analog Input and Configurable Pre-amplifier

The DRV2510-Q1 device features a differential input stage that cancels common-mode noise that appears on the inputs. The DRV2510-Q1 device also features four gain settings that are configurable via I²C. Please see the Programming Sections for register locations.

表 7-1. Gain Configuration Table

GAIN	INPUT IMPEDANCE
20 dB	60 k Ω
26 dB	30 k Ω
32 dB	15 k Ω
36 dB	9 k Ω

7.3.2 Pulse-Width Modulator (PWM)

The DRV2510-Q1 device features BD modulation scheme with high bandwidth, low noise, low distortion, and excellent stability.

The BD modulation scheme allows for smaller ripple currents through the load. Each output switches from 0 V to the supply voltage. With no input, the OUT+ and OUT- pins are in phase with each other so that there is little or no current in the load. For positive differential inputs, the duty cycle of OUT+ is greater than 50% and the duty cycle of OUT- is lower than 50% for a positive differential output voltage. The opposite is true for negative differential inputs. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces the I²R losses in the load.

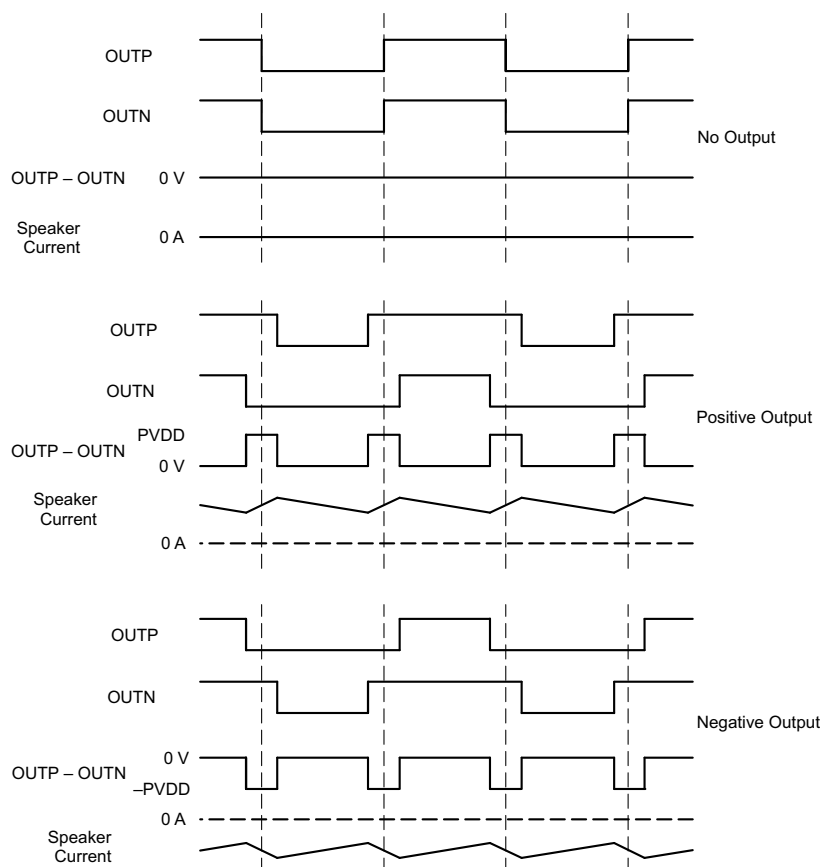


図 7-1. BD Mode Modulation

7.3.3 Designed for low EMI

The DRV2510-Q1 device design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that causes EMI. Follow the recommended design requirements in the [セクション 8.2.1.1](#) section.

7.3.4 Device Protection Systems

The DRV2510-Q1 device features a complete set of protection circuits carefully designed to protect the device against permanent failures due to shorts, over-temperature, over-voltage, and under-voltage scenarios. The INTZ pin signals if an error is detected.

Additionally, the DRV2510-Q1 device is not damaged by adjacent pin to pin shorts.

表 7-2. Fault Reporting Table

FAULT	TRIGGERING CONDITION	INTZ	ACTION
Over-current	Output short or short to VDD or GND	pulled low	output in high impedance. I ² updated.
Over-temperature	T _j > 150 °C	pulled low	output in high impedance. Recovery is automatic once the temperature returns to a safe level.
Under-voltage	VDD < 4 V	pulled low	output in high impedance. I ² reset.
Over-voltage	VDD > 21 V	pulled low	output in high impedance. I ² updated.

7.3.4.1 Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to VDD
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I²C register read.

7.3.4.1.1 Load Diagnostics

The load diagnostic function runs on assertion of EN or when the device is in a fault state (dc detect, overcurrent, overvoltage, undervoltage, and overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to VDD, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic test takes approximately 229 ms to run. Note that the *check* phase repeats up to five times if a fault is present or a large capacitor to GND is present on the output. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the output starts. The load diagnostics run after every other overvoltage (OV) event. The load diagnostic for open load only has I²C reporting. All other faults have I²C and INTZ pin assertion.

The device performs load diagnostic tests as shown in [図 7-2](#).

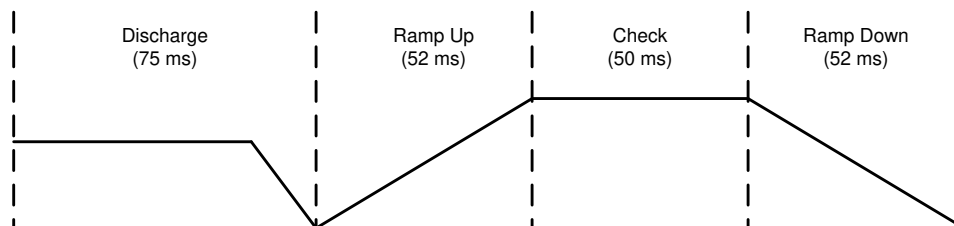


図 7-2. Load Diagnostics Sequence of Events

Figure 7-3 illustrates how the diagnostics determine the load based on output conditions.

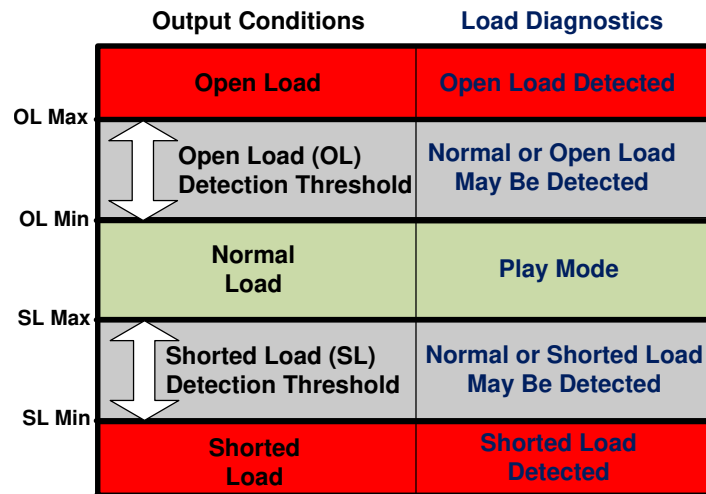


Figure 7-3. Load Diagnostic Reporting Thresholds

7.3.4.2 Faults During Load Diagnostics

If the device detects a fault (overtemperature, overvoltage, undervoltage) during the load diagnostics test, the device exits the load diagnostics, which may result in a small transient on the output.

7.3.4.3 Protection and Monitoring

- **Overcurrent Shutdown (OCS)**—The overcurrent shutdown forces the output into Hi-Z. The device asserts the INTZ pin and updates the I²C register.
- **DC Detect**—This circuit checks for a dc offset continuously during normal operation at the output of the amplifier. If a dc offset occurs, the device asserts the INTZ pin and updates the I²C register. Note that the dc detection threshold follows VDD changes.
- **Overtemperature Shutdown (OTSD)**—The device shuts down when the die junction temperature reaches the overtemperature threshold. The device asserts the INTZ pin and updates I²C register. Recovery is automatic when the temperature returns to a safe level.
- **Undervoltage (UV)**—The undervoltage (UV) protection detects low voltages on VDD. In the event of an undervoltage condition, the device asserts the INTZ pin and resets the I²C register.
- **Power-On Reset (POR)**—Power-on reset (POR) occurs when VDD drops below the POR threshold. A POR event causes the I²C bus to go into a high-impedance state. After recovery from the POR event, the device restarts automatically with default I²C register settings. The I²C is active as long as the device is not in POR.
- **Overvoltage (OV) and Load Dump**—OV protection detects high voltages on VDD. If VDD reaches the overvoltage threshold, the device asserts the INTZ pin and updates the I²C register. The device can withstand 40-V load-dump voltage spikes.
- **SpeakerGuard™**—This protection circuitry limits the output voltage to the value selected in I²C register 0x03. This value determines both the positive and negative limits. The user can use the SpeakerGuard feature to improve battery life or protect the actuator from exceeding its excursion limits.
- **Adjacent-Pin Shorts**—The device design is such that shorts between adjacent pins do not cause damage.

7.4 Device Functional Modes

The DRV2510-Q1 device has multiple power states to optimize power consumption.

7.4.1 Operation in Shutdown Mode

The EN pin of the DRV2510-Q1 device puts the device in a shutdown mode. When EN is de-asserted (logic low), all internal blocks of the device are off to achieve ultra low power. I²C is not operational in this mode and the output is in Hi-Z state.

7.4.2 Operation in Standby Mode

The STDBY pin of the DRV2510-Q1 device puts the device in a standby mode. When STDBY is asserted (logic high), some internal blocks of the device are off to achieve low power while preserving the ability to wake up quickly to achieve low latency waveform playback.

7.4.3 Operation in Active Mode

The DRV2510-Q1 device is in active mode when it has a valid supply, and it is not in either shutdown or standby modes. In this mode the DRV2510-Q1 device is fully on and reproducing at the output the input times the gain.

7.5 Programming

7.5.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. [Figure 7-4](#) shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When the acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. [Figure 7-4](#) shows a generic data-transfer sequence.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Pull-up resistors between 660 Ω and 4.7 k Ω are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2510-Q1 supply voltage, V_{DD} .

注

The DRV2510-Q1 slave address is 0x6C (7-bit), or 1101100 in binary.

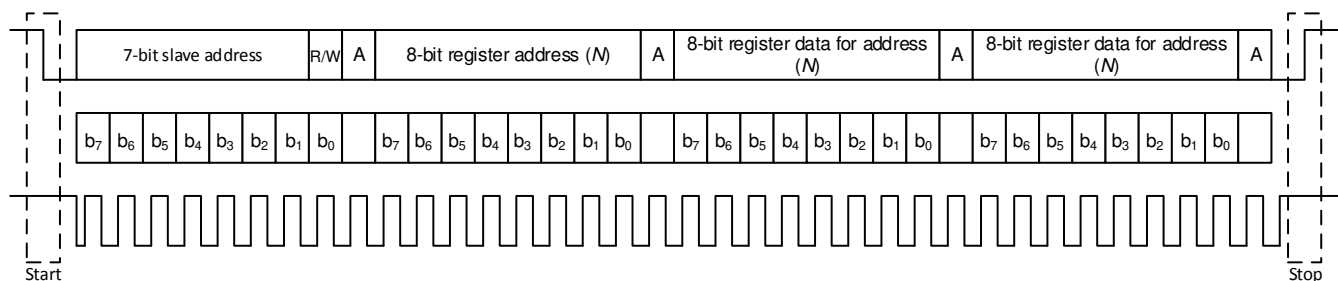


Figure 7-4. Typical I²C Sequence

The DRV2510-Q1 device operates as an I²C-slave 1.8-V logic thresholds, but can operate up to the V_{DD} voltage. The device address is 0x5A (7-bit), or 1011010 in binary which is equivalent to 0xB4 (8-bit) for writing and 0xB5 (8-bit) for reading.

7.5.2 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte R/W operations for all registers.

During multiple-byte read operations, the DRV2510-Q1 device responds with data one byte at a time and begins at the signed register. The device responds as long as the master device continues to respond with acknowledgements.

The DRV2510-Q1 supports sequential I²C addressing. For write transactions, a sequential I²C write transaction has taken place if a register is issued followed by data for that register as well as the remaining registers that follow. For I²C sequential-write transactions, the register issued then serves as the starting point and the amount of data transmitted subsequently before a stop or start is transmitted determines how many registers are written.

7.5.3 Single-Byte Write

As shown in [Figure 7-5](#), a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. The read-write bit determines the direction of the data transfer. For a write-data transfer, the read-write bit must be set to 0. After receiving the correct I²C device address and the read-write bit, the DRV2510-Q1 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the DRV2510-Q1 internal-memory address that is accessed. After receiving the register byte, the device responds again with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

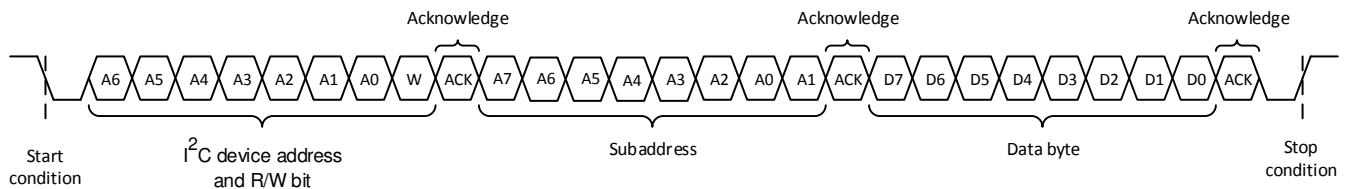


Figure 7-5. Single-Byte Write Transfer

7.5.4 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DRV2510-Q1 device as shown in [Figure 7-6](#). After receiving each data byte, the DRV2510-Q1 device responds with an acknowledge bit.

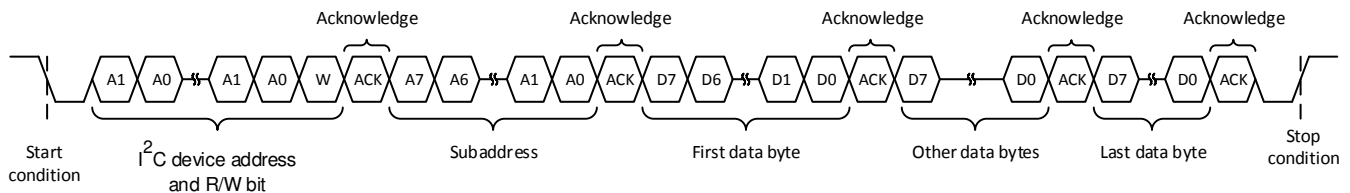


Figure 7-6. Multiple-Byte Write Transfer

7.5.5 Single-Byte Read

[Figure 7-7](#) shows that a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read-write bit. For the data-read transfer, both a write followed by a read actually occur. Initially, a write occurs to transfer the address byte of the internal memory address to be read. As a result, the read-write bit is set to 0.

After receiving the DRV2510-Q1 address and the read-write bit, the DRV2510-Q1 device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the DRV2510-Q1 address and the read-write bit again. On this occasion, the read-write bit is set to 1, indicating a read transfer. Next, the DRV2510-Q1 device transmits the data byte from the memory address that is read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer. See the note in the [セクション 7.5.1](#) section.

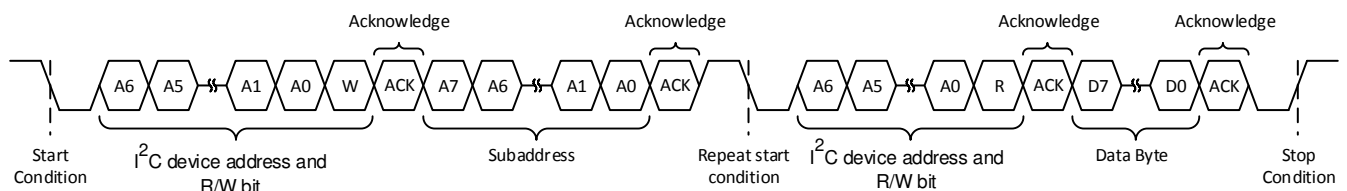


Figure 7-7. Single-Byte Read Transfer

7.5.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the DRV2510-Q1 device to the master device as shown in [Figure 7-8](#). With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

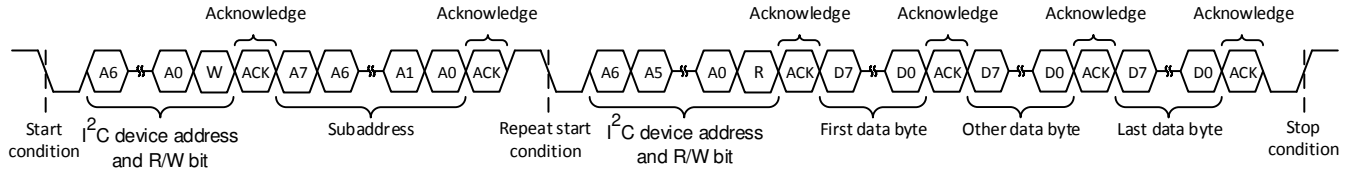


Figure 7-8. Multiple-Byte Read Transfer

7.6 Register Map

表 7-3. Register Map Overview

REG NO.	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x01	0x00	OVER_TEMP	DC_OFFSET	OVER_VOLT	UNDER_VOLT	OVER_CURR	LOAD_DIAG	Reserved	
0x02	0x00	DEV_ACTIVE	STDBY	DIAG_ACTIVE	FAULT	LOAD_SHORT	LOAD_OPEN	LOAD_SHORT_GND	LOAD_SHORT_VDD
0x03	0x00	GAIN[1:0]		PEAK_PROTECTION[1:2]			Reserved		FREQ_SEL

7.6.1 Address: 0x01

図 7-9. 0x01

7	6	5	4	3	2	1	0
OVER_TEMP[0]	DC_OFFSET[0]	OVER_VOLT[0]	UNDER_VOLT[0]	OVER_CURR[0]	LOAD_DIAG[0]	Reserved	
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0		

表 7-4. Address: 0x01

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	OVER_TEMP	RO	0	Shows the current status of the thermal protection	
				0	Temperature is below the over-temperature threshold.
				1	Temperature is above the over-temperature threshold.
6	DC_OFFSET	RO	0	Shows the status of DC offset protection	
				0	DC offset protection has not occurred.
				1	DC offset protection has occurred.
5	OVER_VOLT	RO	0	Shows the status of the over-voltage protection.	
				0	VDD voltage is below the over-voltage threshold.
				1	VDD voltage is above the over-voltage threshold.
4	UNDER_VOLT	RO	0	Shows the status of the under-voltage protection.	
				0	VDD voltage is above the under-voltage threshold.
				1	VDD voltage is below the under-voltage threshold.
3	OVER_CURR	RO	0	Shows the status of the over-current protection.	
				0	An over-current event has not occurred.
				1	Device shutdown due to over-current.
2	LOAD_DIAG	RO	0	Shows the status of the load diagnostics.	
				0	An open or short has not been detected.
				1	An open or short was detected.
1:0	Reserved				

7.6.2 Address: 0x02

図 7-10. 0x02

7	6	5	4	3	2	1	0
DEV_ACTIVE [0]	STDBY [0]	DIAG_ACTIVE [0]	FAULT [0]	LOAD_SHORT [0]	LOAD_OPEN [0]	LOAD_SHORT_GND [0]	LOAD_SHORT_VDD [0]
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0

表 7-5. Address: 0x02

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7	DEV_ACTIVE	RO	0	Shows the device status (active or shutdown).	
				0	Device is shutdown.
				1	Device is active.
6	STDBY	RO	0	Shows the device standby status.	
				0	Device is not on standby.
				1	Device is on standby.
5	DIAG_ACTIVE	RO	0	Shows the status of the diagnostics engine.	
				0	Not performing load diagnostics.
				1	Performing load diagnostics.
4	FAULT	RO	0	Shows if a fault has occurred on the system. Either over-voltage, under-voltage, over-current, over-temperature.	
				0	No fault has occurred.
				1	A fault has occurred.
3	LOAD_SHORT	RO	0	Shows whether the output is shorted.	
				0	OUT+ is not shorted to OUT-.
				1	OUT+ is shorted to OUT-.
2	LOAD_OPEN	RO	0	Shows whether the output has a proper load connected.	
				0	A proper load is connected between OUT+ and OUT-.
				1	There is an open connection between OUT+ and OUT-.
1	LOAD_SHORT_GND	RO	0	Shows whether the output is shorted to GND.	
				0	Output is not shorted to GND.
				1	Either OUT+ or OUT- is shorted to GND.
0	LOAD_SHORT_VDD	RO	0	Shows whether the output is shorted to VDD.	
				0	Output is not shorted to VDD.
				1	Either OUT+ or OUT- is shorted to VDD.

7.6.3 Address: 0x03

図 7-11. 0x03

7	6	5	4	3	2	1	0
GAIN[1:0]		PEAK_PROTECTION[2:0]			Reserved		FREQ_SEL[0]
R/W-0		R/W-0			R/W-0		R/W-0

表 7-6. Address: 0x03

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION	
7:6	GAIN[1:0]	R/W	01	Sets the gain.	
				0	20 dB.
				1	26 dB.
				2	32 dB.
				3	36 dB.
5:3	PEAK_PROTECTION[2:0]	R/W	111	Sets the peak output protection.	
				0	5V pk
				1	5.9 Vpk
				2	7 Vpk
				3	8.4 Vpk
				4	9.8 Vpk
				5	11.8 Vpk
				6	14 Vpk
7	Protection disabled				
2:1	Reserved		00	Always write default values	
0	FREQ_SEL	R/W	0	Sets the output frequency.	
				0	400 kHz.
				1	500 kHz.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The DRV2510-Q1 device is a high-efficiency driver for inductive loads, such as solenoids and voice-coils. The typical use of the device is on haptic applications where short, strong waveforms are desired to create a haptic event that will be coming from the application processor.

8.2 Typical Applications

8.2.1 Single-Ended Source

To use the DRV2510-Q1 with a single-ended source, apply either a voltage divider to bias IN- to 3 V, or use a 0.1- μ F cap from IN- to GND to have the device self bias. Apply the single-ended signal to the IN+ pin through an AC coupling capacitor.

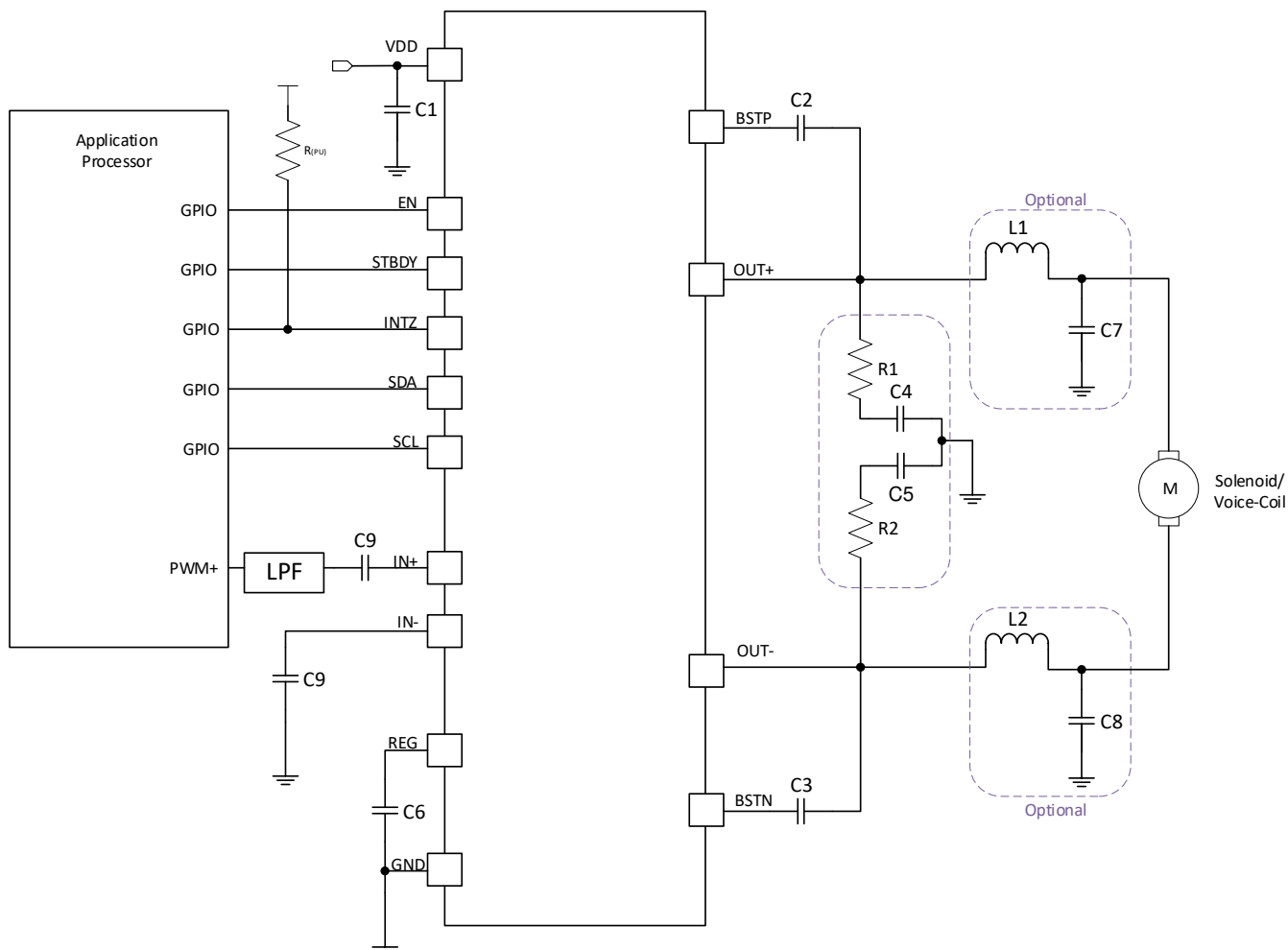


図 8-1. Typical Application Schematic

8.2.1.1 Design Requirements

For most applications the following component values found in 表 8-1 below can be used.

表 8-1. Component Requirements Table

COMPONENT	DESCRIPTION	SPECIFICATION	TYPICAL VALUE
C1	Supply capacitor	Capacitance	22 μF, 10 μF, and 0.1 μF
C2/C3	Boost capacitor	Capacitance	0.22 μF
C4/C5	Output snubber capacitor	Capacitance	470 pF
C6	Regulator capacitor	Capacitance	1 μF
C9	Input decoupling capacitor	Capacitance	0.1 μF
R1/R2	Output snubber resistor	Resistance	3.3 Ω
R _(PU)	Pull-up resistor	Resistance	100 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Optional Components

Note that in the diagrams, there are a few optional external components. These optional external components may be needed in the application to meet EMI/EMC standards and specifications by filters necessary frequency spectrums.

8.2.1.2.2 Capacitor Selection

A bulk bypass capacitor should be mounted between VBAT and GND. The capacitance needs to be >22 uF with a X5R or better rating on the power pins to GND. Also include two ceramic capacitors in the ranges of 220 pF to 1 uF and 100 nF to 1 uF. The bootstrap capacitors, BSTP and BSTN, should be 220-nF ceramic capacitors of quality X5R or better rated for at least the maximum rating of the pin.

8.2.1.2.3 Solenoid Selection

The DRV2510-Q1 solenoid driver can accommodate a variety of solenoids. Solenoids should have an equivalent resistance of 1.6 Ω or greater. Solenoids with lower resistances are prone to driving high currents. A maximum peak current of 3-A should not be exceeded.

8.2.1.2.4 Output Filter Considerations

The output filter is optional and is mainly for limiting peak currents. A second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See Equation 1, through Equation 4, for example filter design.

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \quad (1)$$

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_0} \quad (2)$$

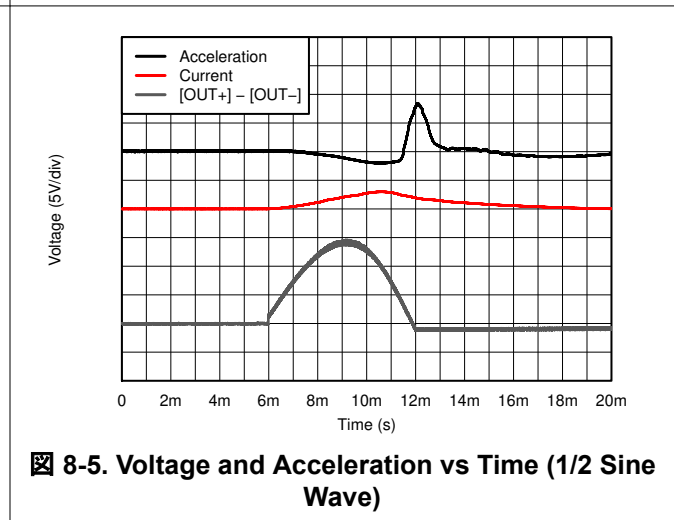
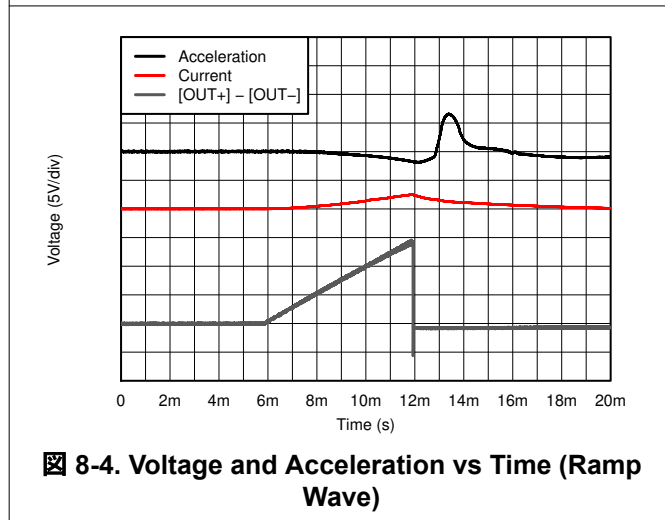
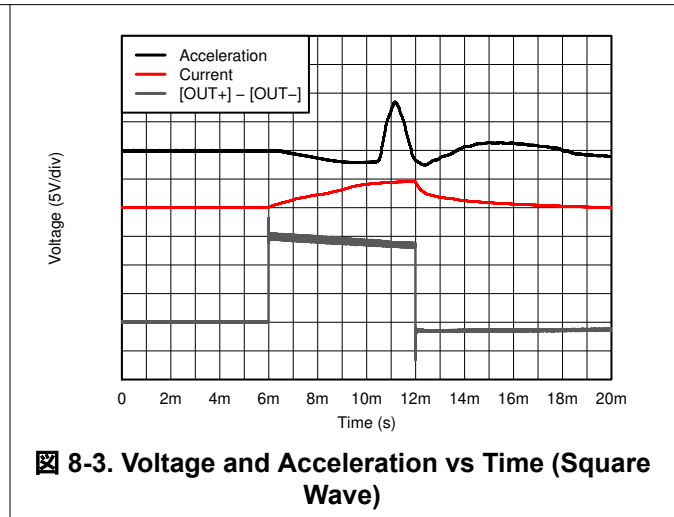
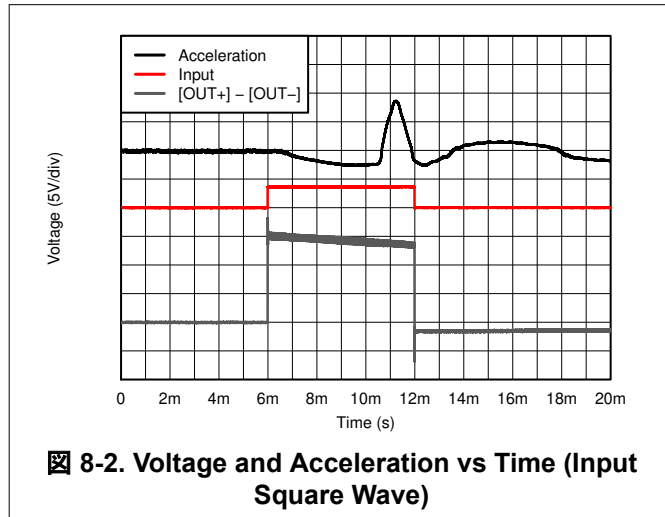
$$2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{2} \times \omega_0} \quad (3)$$

$$\omega_0 = 2\pi \times f \quad (4)$$

8.2.1.3 Application Curves

These application curves were taken using an HA200 solenoid with a 100-g mass, and the acceleration was measured using the DRV-AAC16-EVM accelerometer. The following scales apply to the graphs:

- Output Differential Voltage scale is shown on the plots at 5-V/div
- Acceleration scale is 5.85-G/div
- Current scale is 2-A/div



8.2.1.4 Differential Input Diagram

To use the DRV2510-Q1 with a differential input source, apply both inputs differentially through AC coupling capacitors from a control source (GPIO, DAC, etc...).

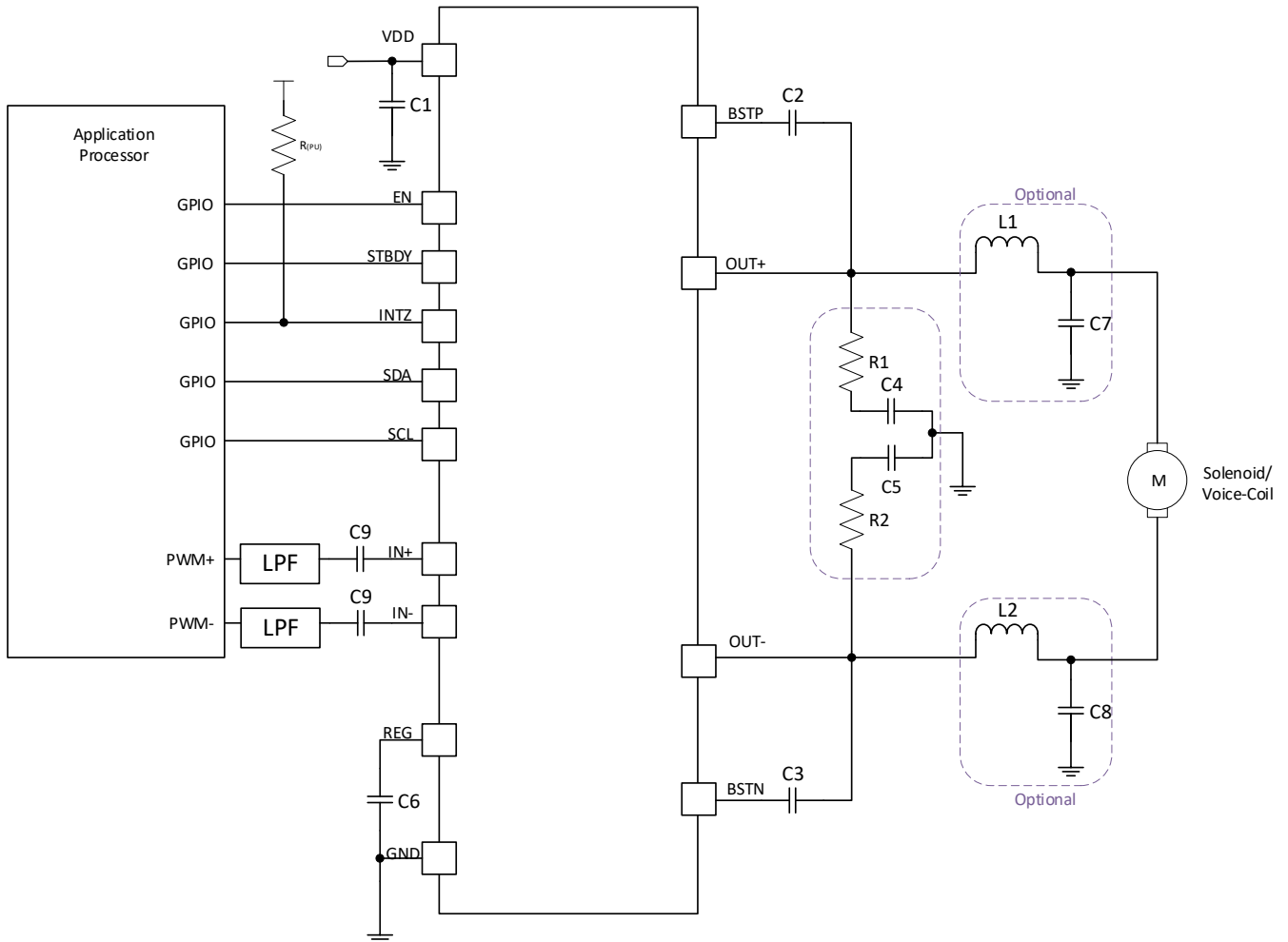


図 8-6. Typical Application Schematic

9 Power Supply Recommendations

The DRV2510-Q1 device operates from 4.5 V - 18 V and this supply should be able to handle high surge currents in order to meet the high current draws for haptics effects. Additionally the DRV2510-Q1 should have 22- μ F, 10- μ F and 0.1- μ F ceramic capacitors near the VDD pin for additional decoupling from trace routing.

10 Layout

10.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The DRV2510-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. It is best practice to use the same/similar layout as shown below in the DRV2510Q1EVM.

10.2 Layout Example

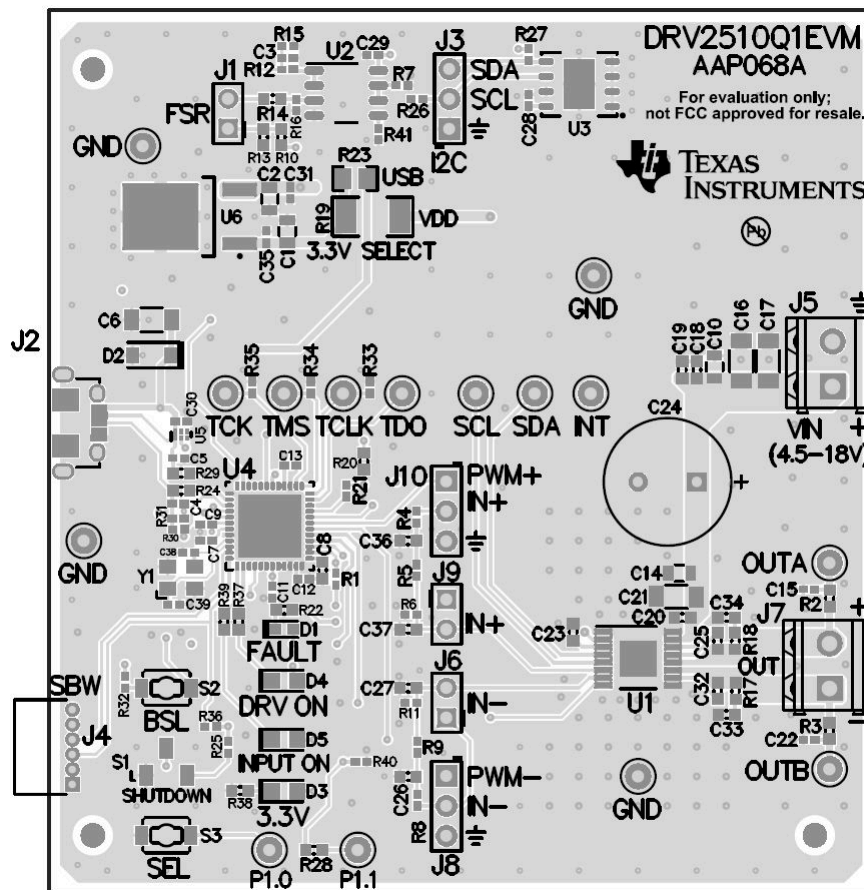


図 10-1. DRV2510-Q1 EVM

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

11.4 Trademarks

SpeakerGuard™ and TI E2E™ are trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV2510QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV2510	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

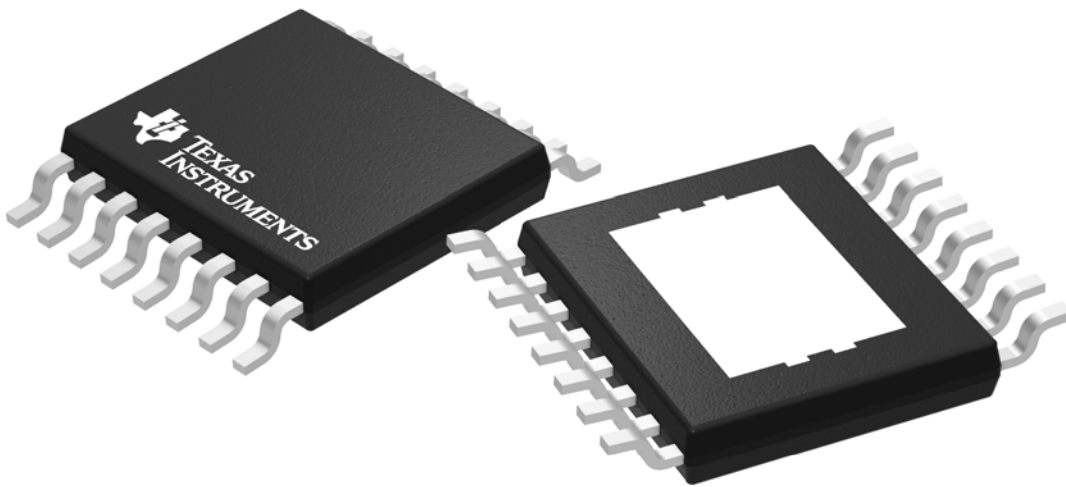

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV2510QPWRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV2510QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated