TEXAS INSTRUMENTS
DRV8161, DRV8162
JAJSUL1A – MAY 2024 – REVISED JULY 2024

DRV816x 保護機能および電流センス アンプ搭載、100V ハーフブリッジ スマート ゲート ドライバ

1 特長

- ハーフブリッジ構成の 2 つの N チャネル MOSFET を駆動
  - ハイサイド MOSFET ソース / ドレイン最大 102V (絶対最大定格)
  - 8V (5V DRV8162L)～20V のゲート ドライブ電源
  - ブートストラップ ダイオードを内蔵
- 16 レベルのゲート ドライブ ピーク電流
  - 16mA～1000mA ソース電流
  - 32mA～2000mA シンク電流
  - ソース - シンク電流比 1:1、1:2、1:3
- 可変 PWM デッド タイム挿入 20ns～400ns
- モーター位相 (SH) スイッチング向けの堅牢な設計
  - スルーレート 20V/µs
  - 負の過渡電圧 -20V
  - 2A の強力なゲート プルダウン
- 冗長シャットダウン用にゲート駆動電源入力を分割 (DRV8162、DRV8162L)
- 低オフセットの電流センス アンプ (DRV8161)
  - 可変ゲイン (5、10、20、40V/V)
- 柔軟な PWM 制御インターフェイス、2 ピン PWM、独立 PWM モード
- 13 レベル VDS 過電流スレッショルド
- 独立したシャットダウン ピン (nDRVOFF)
- ゲート ドライバ ソフト シャットダウン シーケンス
- 保護機能内蔵
  - GVDD 低電圧 (GVDDUV)
  - ブートストラップ低電圧 (BST_UV)
  - MOSFET 過電流保護 (VDS)
  - 貫通電流保護
  - サーマル シャットダウン (OTSD)
  - フォルト状態インジケータ (nFAULT)
- 3.3V および 5V のロジック入力をサポート

2 アプリケーション

- 産業用ロボット / 協力ロボット (コボット)
- 移動ロボット (AGV/AMR)
- リニア モーター輸送用システム
- サーボ ドライブ
- ドローン
- 電動アシスト自転車、電動スクーター、E-モビリティ

3 概要

DRV816x は、ハイサイドおよびローサイドの N チャネル パワー MOSFET を駆動できる、ハーフ ブリッジ ゲート ドライバです。ゲート駆動電圧は GVDD 電源ピンから生成され、内蔵ブートストラップ回路はハイサイド FET を最大 102V ドレインまで駆動するために使用されます。スマート ゲート ドライブ アーキテクチャは、最大でソース 1A、シンク 2A の 16 レベル (48 通りの組み合わせ) のゲート駆動ピーク電流をサポートし、ゲート駆動電流の内蔵タイミング制御機能も搭載しています。これらのデバイスを使用して、ブラシレス / ブラシ付き DC モータ、PMSM、ステッピング モータ、SRM、ソレノイドなど、各種の負荷を駆動できます。

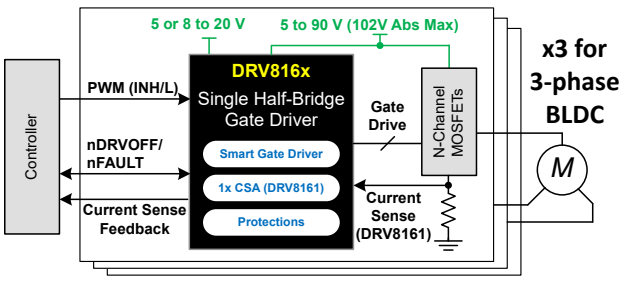
電源低電圧、FET 過電流、ダイ過熱に対する保護機能が内蔵されています。nFAULT ピンは、保護機能によって検出されたフォルト イベントを通知します。nDRVOFF ピンは、PWM 制御から独立して電力段のシャットダウンを開始します。DRV8162 および DRV8162L デバイスは、セーフ トルク オフ (STO) 機能を補助するために、分割電源アーキテクチャを採用しています。

ゲート駆動電流、デッドタイム、PWM 制御インターフェイス、過電流検出など、デバイスの多くのパラメータは、いくつかの受動部品をデバイスのピンに接続して構成できます。内蔵のローサイド電流センス アンプ (DRV8161) は、電流測定情報をコントローラに返します。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
DRV8161	VSSOP (20)	5.1mm × 3.0mm
DRV8162(2)	VSSOP (20)	5.1mm × 3.0mm

(1) 詳細については、セクション 12 を参照してください。
(2) DRV8162 (製品プレビュー) および DRV8162L (事前情報) のデバイス バリアントが含まれます。「Device Comparison Table」を参照してください。



DRV816x の概略回路図

Table of Contents

ADVANCE INFORMATION

4 Device Comparison Table

DEVICE	DEVICE VARIANT	PACKAGE PIN COUNT	CURRENT SENSE AMPLIFIER	GATE DRIVE POWER SUPPLY	MIN GVDD OPERATION	Control Mode
DRV8161	DRV8161(1)	20	YES	GVDD	8-V	2-pin, Independent FET
DRV8162	DRV8162(2)		No	GVDD and GVDD_LS	8-V	
	DRV8162L(1)				5-V	

(1) Advance Information. The products are in sampling and preproduction phase.
(2) Product Preview. The product is in the formative or design phase. Contact TI for more information.

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Pin Configuration and Functions

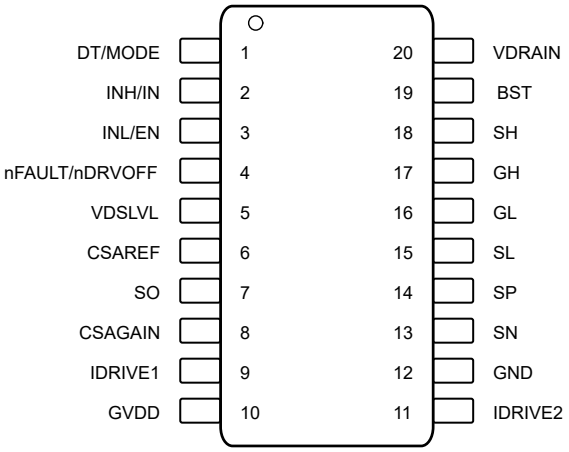


図 5-1. DRV8161 (Advance Information) DGS Package 20-pin VSSOP Top View

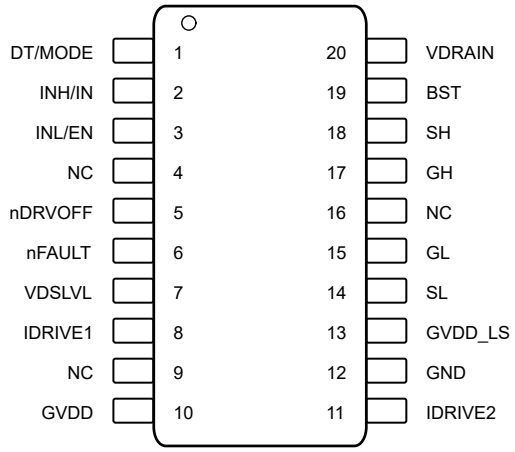


図 5-2. DRV8162 (Product Preview) and DRV8162L (Advance Information) DGS Package 20-pin VSSOP Top View

表 5-1. Pin Functions—DRV816x Devices

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DRV8161 20-pin	DRV8162, DRV8162L 20-pin		
DT/MODE	1	1	I	Selects input pin interface logic and gate drive dead time setting. Connect a resistor between DT and GND to adjust dead time between 20 ns to 1000 ns, and select a PWM mode.
INLH/IN	2	2	I	Gate driver control input. Gate driver control depends on DT/MODE pin setting.
INL/EN	3	3	I	Gate driver control input. Gate driver control depends on DT/MODE pin setting.
NC	—	4	N/A	No Connect. Leave open.
nDRVOFF	—	5	I	Gate driver shutdown control. Pulling nDRVOFF low turns off high-side and low-side external MOSFETs by putting the gate drivers into the pull-down state.
nFAULT/ nDRVOFF	4	—	I/OD	Shared fault indicator pin and gate driver shutdown pin. Connect this pin to an external pull-up resistor to the controller supply or a controller output pin. This pin is pulled logic low during a fault condition. To active gate drive shutdown, pull the pin low by external logic.
nFAULT	—	6	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor to controller I/O supply, 3.3V to 5.0V.
VDSLVL	5	7	I	VDS monitor threshold setting. This pin is a multilevel input pin set by an external resistor.
CSAREF	6	—	PWR	Current sense amplifier reference. Connect a capacitor between the CSAREF and GND pins.
SO	7	—	O	Current sense amplifier output.
CSAGAIN	8	—	I	Gain settings for current sense amplifier. This pin is a multilevel input pin set by an external resistor.
IDRIVE1	9	8	I	Gate drive source and sink current setting. This pin is a multilevel input pin set by an external resistor.
NC		9, 16		No Connect. Leave open.
GVDD	10	10	PWR	Gate driver power supply input. Connect a capacitor between the GVDD and GND pins.

表 5-1. Pin Functions—DRV816x Devices (続き)

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DRV8161 20-pin	DRV8162, DRV8162L 20-pin		
IDRIVE2	11	11	I	Gate drive source and sink current setting. This pin is a multilevel input pin set by an external resistor.
GND	12	12	PWR	Device ground.
GVDD_LS	—	13	PWR	Low-side gate driver power supply input (DRV8162 and DRV8162L only). Connect a capacitor between the GVDD_LS and GND pins.
SN	13	—	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SP	14	—	I	Current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SL	15	14	I	Low-side source pin. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor and the output for the low-side gate driver sink.
GL	16	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GH	17	17	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
SH	18	18	I	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
BST	19	19	O	Bootstrap output pin. Connect a capacitor between BST and SH.
VDRAIN	20	20	PWR	High-side MOSFET drain sense input for VDS monitor and charge pump reference. Connect to the high-side MOSFET drain.
THERMAL PAD			PWR	Leave open, or tied to GND

PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Specification

6.1 Absolute Maximum Ratings

Over recommended operating conditions (unless otherwise noted)(1)

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD, GVDD_LS	-0.3	20	V
High-side drain pin voltage	VDRAIN, T_J = 25℃	-0.3	102	V
Bootstrap pin voltage	BST, T_J = 25℃	-0.3	115	V
Bootstrap pin voltage	BST with respect to SH	-0.3	20	V
Logic pin voltage	nFAULT	-0.3	20	V
	INH(IN), INL(EN), nDRVOFF, VDSLVL	-0.3	20	
	DT/MODE, IDRIVE1, IDRIVE2, CSAGAIN	-0.3	6	
High-side gate drive pin voltage	GH, T_J = 25℃ GVDD >= 11V	-5	115	V
High-side gate drive pin voltage	GH with respect to SH	-0.3	20	V
High-side source pin voltage	SH, DC	-5	105	V
Transient high-side source pin negative voltage	SH, 1 µs	-20		V
High-side source pin slew rate	SH , V_{BST-SH} >3.5V		20	V/ns
Low-side gate drive pin voltage	GL with respect to SL	-0.3	20	V
Low-side source sense pin voltage	SL	-5	V_{GVDD}+0.3	V
Transient low-side source sense pin negative voltage	SL, 1 µs	-16		V
Current sense amplifier reference input pin voltage	CSAREF	-0.3	5.5	V
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP, 500ns	-16	20	V
Shunt amplifier output pin voltage	SO	-0.3	V_{CSAREF} + 0.3	V
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD, GVDD_LS	8		20	V
	Power supply voltage (DRV8162L only)	GVDD, GVDD_LS, DRV8162L device variant	5			V
$V_{GVDD-SL}$	Power supply voltage with respect to SL	GVDD(DRV8161), GVDD_LS (DRV8162x) for low-side Pre-Driver PWM operation	3.5			V
V_{VDRAIN}	High-side drain pin voltage	VDRAIN, low-side gate drive, and high-side gate drive switching with bootstrap	0		90	V
V_{BST-SH}	Bootstrap pin voltage with respect to SH	BST (V_{BST} - V_{SH}), high-side gate drive switching and no BST_UV detection, V_{BST-SH} min > V_{BST_UV} max (rising),	6.1		20	V
	Bootstrap pin voltage with respect to SH (DRV8162Lonly)	BST (V_{BST} - V_{SH}), DRV8162L device variant only, high-side gate drive switching and no BST_UV detection, V_{BST-SH} min > V_{BST_UV} max (rising)	4.6			V
V_{BST}	Bootstrap pin voltage	BST	0		105	V
V_{SH}	High-side source pin voltage	SH	-2		95	V
V_I	Digital / Pin detection input voltage	INH, INL, IDRIVE1, IDRIVE2, GAIN, VDSLVL	0		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT			5.5	V
I_{OD}	Open drain output current	nFAULT			–5	mA
V_{CSAREF}	Current sense amplifier reference voltage	CSAREF	3.0		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information 1pkg

THERMAL METRIC(1)		DRV8161/DRV8162 DGS(VSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics

V_{GVDD} = 12 V, V_{VDRAIN} = 48 V, CSAREF = 5V, T_J = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, BST)						
I_{VDRAIN_UNPWR}	VDRAIN leakage current under GVDD unpowered	GVDD = 0V, VDRAIN = 48V, V_{BST-SH} = 0V		3.5	5	µA
I_{GVDD}	GVDD active mode current	INH = INL = Switching @ 20kHz; V_{BST} = V_{GVDD}; No FETs connected, DT/MODE Pin open. VDS_LVL = 2V		2		mA
t_{WAKE}	Turnon time	GVDD = 0V to 12V V_{GVDD} = V_{GVDD_UV} to active mode (outputs ready : nFAULT = High)		0.4		ms
IL_{BS_TCPON}	Bootstrap pin leakage current during high-side pull-up	INH = high; TCP_ON		30		µA
LOGIC-LEVEL INPUTS (INH, INL, nDRVOFF)						
V_{IL}	Input logic low voltage	INL, INH, nDRVOFF			0.8	V
V_{IH}	Input logic high voltage	INL, INH, nDRVOFF	2.2			V
R_{PU}	Input pullup resistance	nDRVOFF to internal regulator, no external connection		250		kΩ
R_{PD}	Input pulldown resistance	INH, INL to GND		250		kΩ
$t_{nDRVOFF\_DEG}$	nDRVOFF input deglitch time	nDRVOFF falling and rising		2.1		µs
$t_{nDRVOFF\_DIAG}$	nDRVOFF diagnostic pulse valid input time	DRV8162 and DRV8162L only		0.5		µs
OPEN-DRAIN OUTPUT (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA, GVDD > 4V			0.4	V
BOOTSTRAP DIODE (BST)						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 10 mA		0.8		V
		I_{BOOT} = 100 mA		1.3		
R_{BOOTD}	Bootstrap dynamic resistance (ΔV_{BOOTD}/ΔI_{BOOT})	I_{BOOT} = 100 mA and 50 mA		4.8		Ω
CHARGE PUMP (BST)						
V_{TCP}	Trickle charge pump output voltage	V_{BST-SH} , INH = High, V_{SH} = V_{VDRAIN} = 20V, V_{BST} > V_{GVDD}, External load $I_{TRICKLE}$ = 2uA, T_J = 25℃		8.5		V
		V_{BST-SH} , INH = High, V_{SH} = V_{VDRAIN} = 20V, V_{BST} > V_{GVDD}, External load $I_{TRICKLE}$ = 2uA, T_J = 150℃		4.9		
GATE DRIVERS (GH, GL, SH, SL)						

ADVANCE INFORMATION

V_{GVDD} = 12 V, V_{VDRAIN} = 48 V, CSAREF = 5V, T_J = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVEP0}$	Peak source gate current	V_{BST}-V_{SH} = V_{GVDD} = 12V		16		mA
$I_{DRIVEP1}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		32		
$I_{DRIVEP2}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		64		
$I_{DRIVEP3}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		96		
$I_{DRIVEP4}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		128		
$I_{DRIVEP5}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		160		
$I_{DRIVEP6}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		192		
$I_{DRIVEP7}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		224		
$I_{DRIVEP8}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		256		
$I_{DRIVEP9}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		288		
$I_{DRIVEP10}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		320		
$I_{DRIVEP11}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		384		
$I_{DRIVEP12}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		448		
$I_{DRIVEP13}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		512		
$I_{DRIVEP14}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		768		
$I_{DRIVEP15}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		1024		
$I_{DRIVEN0}$	Peak sink gate current	V_{BST}-V_{SH} = V_{GVDD} = 12V		32		mA
$I_{DRIVEN1}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		64		
$I_{DRIVEN2}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		128		
$I_{DRIVEN3}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		192		
$I_{DRIVEN4}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		256		
$I_{DRIVEN5}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		320		
$I_{DRIVEN6}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		384		
$I_{DRIVEN7}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		448		
$I_{DRIVEN8}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		512		
$I_{DRIVEN9}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		576		
$I_{DRIVEN10}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		640		
$I_{DRIVEN11}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		768		
$I_{DRIVEN12}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		896		
$I_{DRIVEN13}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		1024		
$I_{DRIVEN14}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		1536		
$I_{DRIVEN15}$		V_{BST}-V_{SH} = V_{GVDD} = 12V		2048		
R_{PD_LS}	Low-side passive pull down	GL to SL, V_{GL} - V_{SL} = 2V		85		kΩ
R_{PDSA_HS}	High-side semi active pull down	V_{GVDD} < V_{GVDD_UV} GH to SH, V_{GH} - V_{SH} = 2V		4		kΩ
I_{PUHOLD_HS}	High-side pull-up hold current			512		mA
I_{PDHOLD_HS}	High-side pull-down hold current			2048		mA
$I_{PDSTRONG\_LS}$	Low-side pull-down strong current			2048		mA
$I_{PDSTRONG\_HS}$	High-side pull-down strong current			2048		mA
$I_{DRVIVENSD\_LS}$	Low-side peak sink gate shutdown current	$I_{DRIVENx}$ is set to $I_{DRIVEN13}$ (1024mA Typ) or smaller settings		32		mA
$I_{DRVIVENSD\_LS}$	Low-side peak sink gate shutdown current	$I_{DRIVENx}$ is set to $I_{DRIVEN14}$ (1536mA Typ) or $I_{DRIVEN15}$ (2048mA Typ)		64		mA
$I_{DRIVENSD\_HS}$	High-side peak sink gate shutdown current	$I_{DRIVENx}$ is set to $I_{DRIVEN13}$ (1024mA Typ) or smaller settings		32		mA

ADVANCE INFORMATION

V_{GVDD} = 12 V, V_{VDRAIN} = 48 V, CSAREF = 5V, T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRIVENSD\_HS}$	High-side peak sink gate shutdown current	$I_{DRIVENx}$ is set to $I_{DRIVEN14}$ (1536mA Typ) or $I_{DRIVEN15}$ (2048mA Typ)		64		mA
GATE DRIVERS TIMINGS						
t_{PDR_LS}	Low-side rising propagation delay	INL to GL rising, no load on GL		50		ns
t_{PDF_LS}	Low-side falling propagation delay	INL to GL falling, no load on GL		50		ns
t_{PDR_HS}	High-side rising propagation delay	INH to GH rising, no load on GH		50		ns
t_{PDF_HS}	High-side falling propagation delay	INH to GH falling, no load on GH		50		ns
t_{PD_MATCH}	Matching propagation delay of low-side gate driver	GL turning ON to GL turning OFF, From V_{GL-SL} = 1V to V_{GL-SL} = V_{GVDD} - 1V;, no load on GL		±4		ns
t_{PD_MATCH}	Matching propagation delay of high-side gate driver	GH turning ON to GH turning OFF, From V_{GH-SH} = 1V to V_{GH-SH} = V_{BST-SH} - 1V; no load on GH		±4		ns
$t_{PD\_MATCH\_PH}$	Matching propagation delay per phase from GL off to GH on	Deadtime disabled. GL turning OFF to GH turning ON, From V_{GL-SL} = V_{GVDD} - 1V to V_{GH-SH} = 1V		±4		ns
$t_{PD\_MATCH\_PH}$	Matching propagation delay per phase from GH off to GL on	Deadtime disabled. GH turning OFF to GL turning ON, From V_{GH-SH} = V_{BST-SH} - 1V to V_{GL-SL} = 1V		±4		ns
t_{DEAD}	Gate drive dead time	R_{DT} = 470 Ω 2-pin PWM mode; $I_{DRIVEN15}$		20		ns
		R_{DT} = 1.3 KΩ 2-pin PWM mode; $I_{DRIVEN15}$		100		
		R_{DT} = 3.3 KΩ 2-pin PWM mode; $I_{DRIVEN15}$		370		
$t_{MINDEAD\_VGS}$	Minimum gate drive dead time (shortest available) of VGS monitor mode	VGS monitor dead time insertion; t_{DEAD_CFG} < 130ns; HS falling to LS rising, LS falling to HS rising		280		ns
CURRENT SHUNT AMPLIFIERS (SN, SO, SP, CSAREF)						
A_{CSA}	Sense amplifier gain	CSAGAIN = Tied to GND (LEVEL0)		5		V/V
		CSAGAIN = 10kΩ typ tied to GND (LEVEL1)		10		V/V
		CSAGAIN = 30kΩ typ tied to GND (LEVEL2)		20		V/V
		CSAGAIN = open; (LEVEL3)		40		V/V
t_{SET}	Settling time to ±1%	V_{STEP} = 1.6 V, A_{CSA} = 5 V/V, C_{SO} = 500pF		0.6		µs
		V_{STEP} = 1.6 V, A_{CSA} = 40 V/V, C_{SO} = 500pF		0.8		µs
BW	Bandwidth	A_{CSA} = 5 V/V, C_{LOAD} = 60-pF, small signal -3 dB		5		MHz
V_{SWING}	Output voltage range	V_{CSAREF} = 3 to 5.5 V	0.25		V_{CSAREF} - 0.25	V
V_{COM}	Common-mode input range		-0.225		0.225	V
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 25°C, Gain A_{CSA} = 10, 20, 40 V/V	-1.3		1.3	mV
V_{OFF}	Input offset voltage	V_{SP} = V_{SN} = GND; T_J = 25°C, Gain A_{CSA} = 5 V/V	-2.6		2.6	mV
V_{OFF_DRIFT}	Input drift offset voltage	V_{SP} = V_{SN} = GND, ; –40°C ≤ T_J ≤ 150°C		8		µV/°C
I_{BIAS}	Input bias current	V_{SP} = V_{SN} = GND, V_{CSAREF} = 3V to 5.5V			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SP} – I_{SN}	-1		1	µA

ADVANCE INFORMATION

V_{GVDD} = 12 V, V_{VDRAIN} = 48 V, CSAREF = 5V, T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	DC		80		dB
		20 kHz		60		dB
I_{CSA_SUP}	Supply current for CSA	CSAREF, V_{CSAREF} = 3.V to 5.5V		1.5		mA
T_{CMREC}	Common mode recovery time			2		us
PROTECTION CIRCUITS						
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising		7.4		V
		V_{GVDD} falling		6.7		V
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising, DRV8162L		4.8		V
		V_{GVDD} falling, DRV8162L		4.7		
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BST} - V_{SH}; V_{BST} rising, GVDD = 12V		7.43		V
		V_{BST} - V_{SH}; V_{BST} falling, GVDD = 12V		7.25		
		V_{BST} - V_{SH}; V_{BST} rising, GVDD = 5V, DRV8162L		4.08		
		V_{BST} - V_{SH}; V_{BST} falling, GVDD = 5V, DRV8162L		3.94		
V_{DS_LVL0-0}	V_{DS} overcurrent protection threshold level (DC)	R_{VDSLVL} = 0.1 KΩ max (LEVEL0)		0.1		V
V_{DS_LVL1-1}		R_{VDSLVL} = 2 KΩ typ (LEVEL1); one pulse detected on VDSLVL pin		0.15		
V_{DS_LVL1-0}		R_{VDSLVL} = 2 KΩ typ (LEVEL1); DC		0.2		
V_{DS_LVL2-1}		R_{VDSLVL} = 5.6 KΩ typ (LEVEL2); one pulse detected on VDSLVL pin		0.3		
V_{DS_LVL2-0}		R_{VDSLVL} = 5.6 KΩ typ (LEVEL2)		0.4		
V_{DS_LVL3-1}		R_{VDSLVL} = 12 KΩ typ (LEVEL3); one pulse detected on VDSLVL pin		0.5		
V_{DS_LVL3-0}		R_{VDSLVL} = 12 KΩ typ (LEVEL3)		0.6		
V_{DS_LVL4-1}		R_{VDSLVL} = 26 KΩ typ (LEVEL4); one pulse detected on VDSLVL pin		0.7		
V_{DS_LVL4-0}		R_{VDSLVL} = 26 KΩ typ (LEVEL4)		0.8		
V_{DS_LVL5-1}		R_{VDSLVL} = 62 KΩ typ (LEVEL5); one pulse detected on VDSLVL pin		0.9		
V_{DS_LVL5-0}		R_{VDSLVL} = 62 KΩ typ (LEVEL5)		1.0		
V_{DS_LVL6-1}		R_{VDSLVL} = 130 KΩ typ (LEVEL6) ; one pulse detected on VDSLVL pin VDSLVL		1.5		
V_{DS_LVL6-0}		R_{VDSLVL} = 130 KΩ typ (LEVEL6);		2.0		
t_{DS_DG}	V_{DS} protection deglitch time			3		µs
t_{DS_BLK}	V_{DS} overcurrent protection blanking time			1		µs
$t_{VDSLVLFIL}$	VDSLVL pin digital input - one pulse filter time for LEVELx-1			4		µs
$V_{IHVDSLVL}$	VDSLVL pin digital input - one pulse high-level detection voltage for LEVELx-1			1		V
T_{OTSD}	Thermal shutdown temperature			170		°C

ADVANCE INFORMATION

6.6 Timing Diagrams

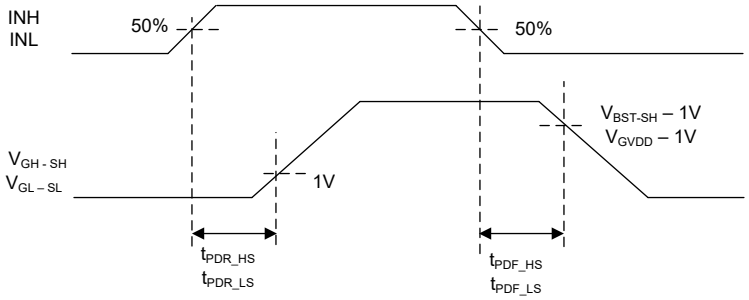


図 6-1. Gate Driver Propagation Delay Timing Diagram

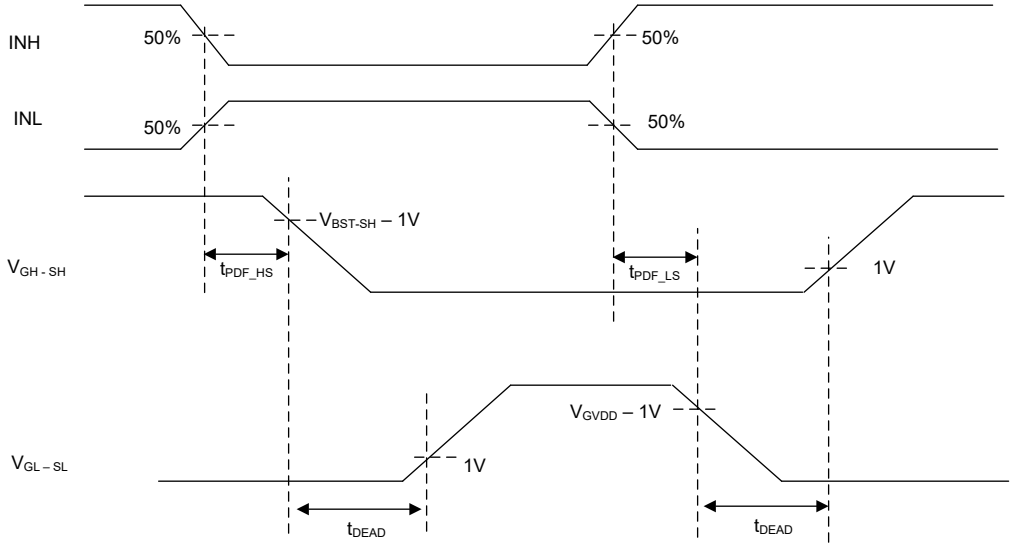


図 6-2. Gate Driver Dead Timing Insertion (INH and INL monitor mode)

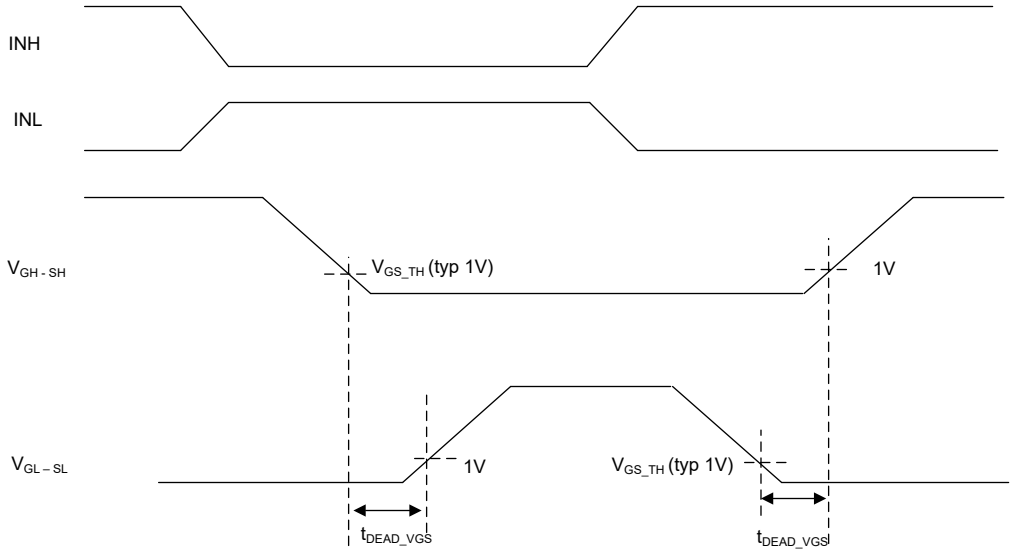


図 6-3. Gate Driver Dead Timing Insertion (VGS monitor mode)

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The DRV816x devices are integrated 100-V gate drivers for various electromechanical loads including brushless DC (BLDC) motors, brushed DC motors, stepper motors, switched reluctance motors, and solenoids. These devices reduce system component count, cost, and complexity by integrating half-bridge gate drivers with a trickle charge pump, bootstrap diode, and FET VDS monitoring. The FET VDS monitors protect the external FETs against shorts to the supply, to ground, or across motor terminals. The DRV8161 integrates a bidirectional low-side current sense amplifier for current feedback to the controller ADC. The half-bridge architecture allows for the gate driver to be placed near the power stage FETs to simplify signal routing, reduce radiated EMI, and reduce overall PCB area.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1-A source, 2-A sink peak currents. The integrated bootstrap diode, external bootstrap capacitor, and integrated trickle charge pump generate the high-side gate drive supply voltage from the GVDD pin. The GVDD pin directly supplies the low-side gate drive supply voltage. The DRV8162 and DRV8162L device variants offer separate GVDD and GVDD_LS pins to help the system design of safe torque off (STO).

A smart gate-drive architecture provides the ability to adjust the output gate-drive current strength allowing for the gate driver to control the power MOSFET VDS switching speed. This allows for the removal of external gate drive resistors and diodes reducing BOM component count, cost, and PCB area. The architecture also uses an internal state machine to protect against gate-drive short-circuit events, control the half-bridge dead time, and protect against dV/dt parasitic turn on of the external power MOSFET.

In addition to the high level of device integration, the DRV816x devices provide a wide range of integrated protection features. These features include power-supply under voltage lockout (UVLO), VDS over current monitoring (OCP), and over temperature shutdown (OTSD). The nFAULT pin indicates fault events detected by the protection features.

ADVANCE INFORMATION

7.2 Functional Block Diagram

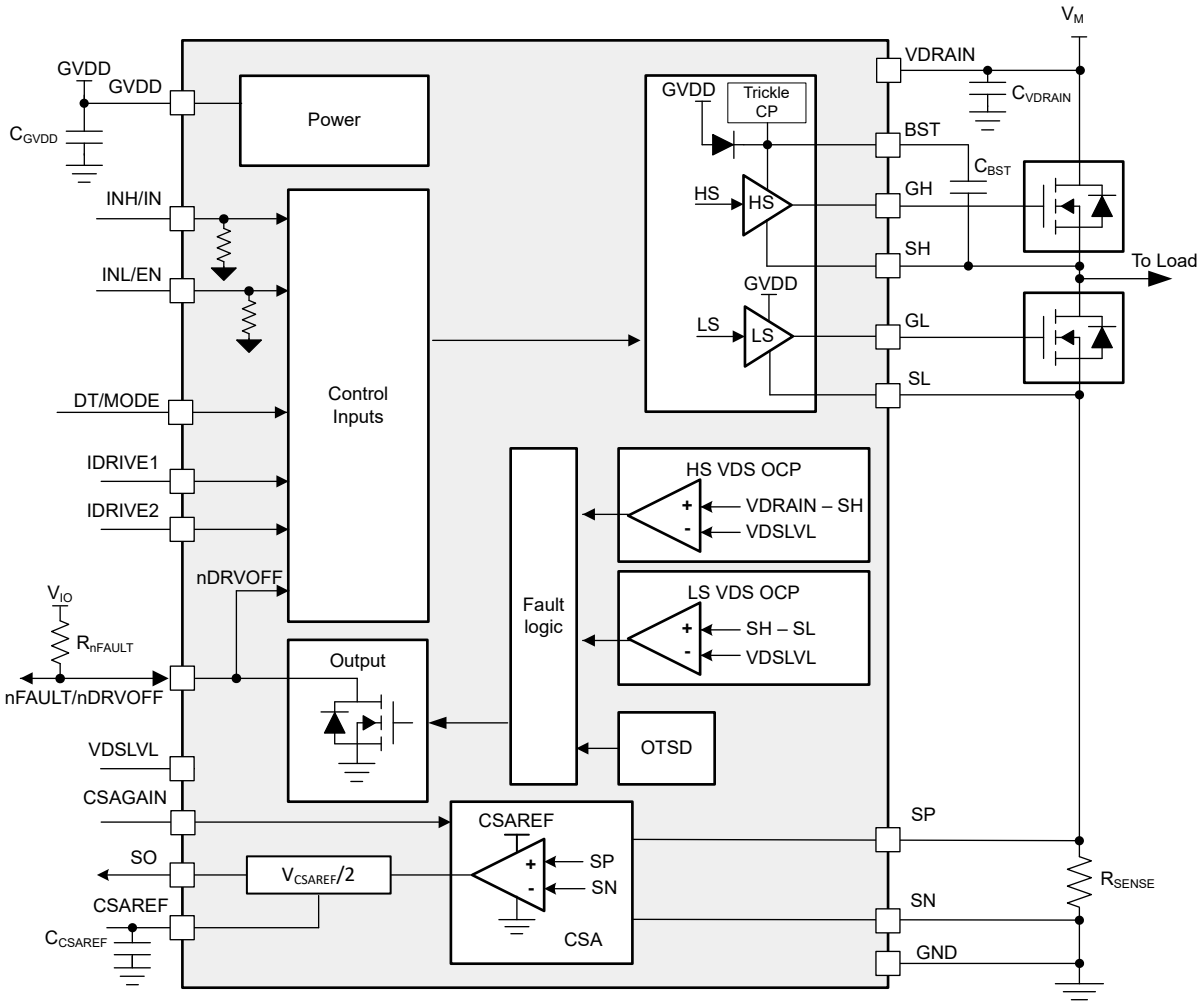


図 7-1. Block Diagram for DRV8161

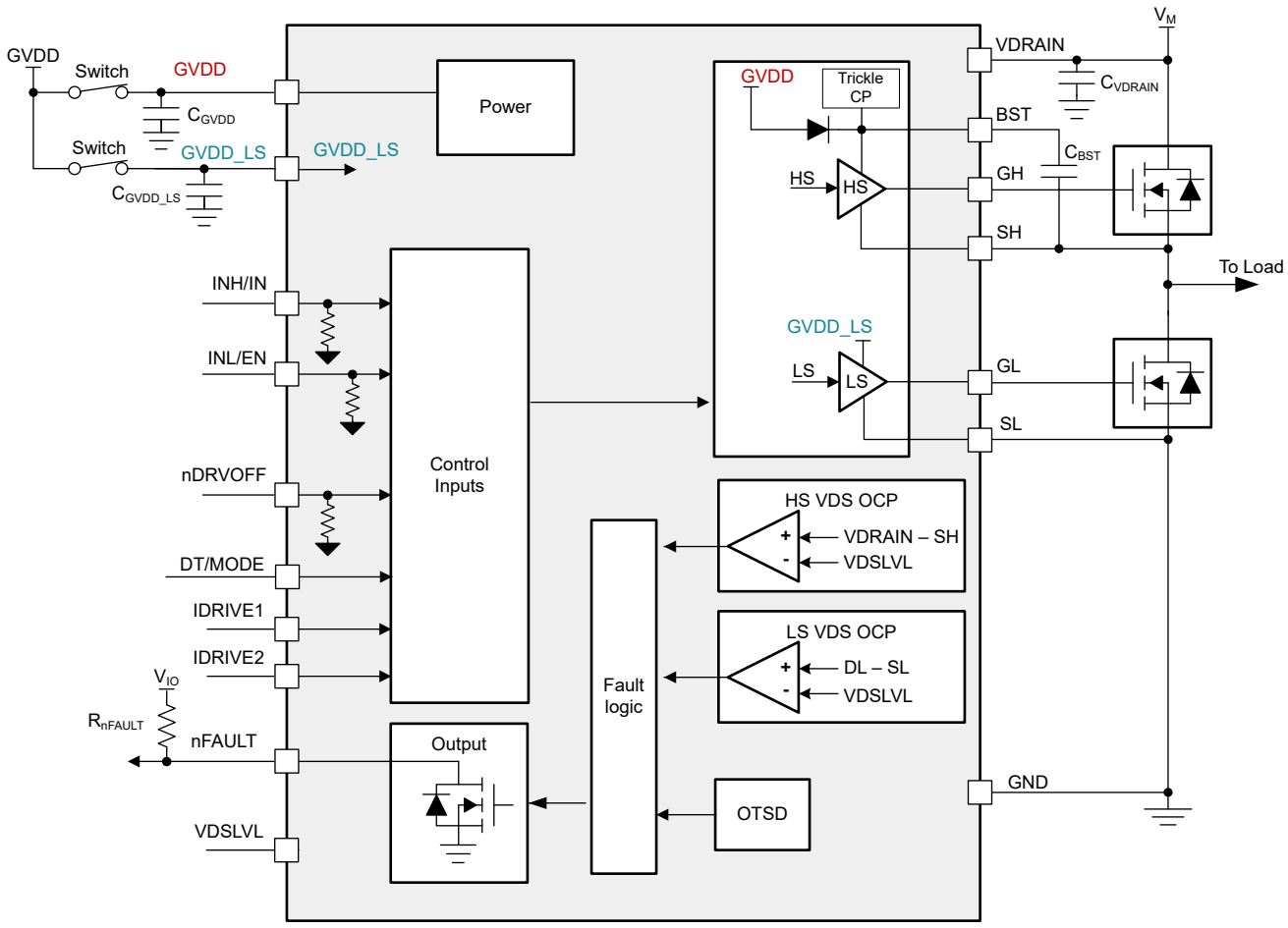


図 7-2. Block Diagram for DRV8162 and DRV8162L

ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Gate Drivers

The DRV816x family of devices integrates high-side and low-side FET gate drivers capable of driving N-channel power MOSFETs in half-bridge configuration. A bootstrap gate drive architecture generates the high-side gate driver voltage during PWM switching. The GVDD pin supplies both high-side and low-side gate drivers and sets the V_{GS} voltage for the FETs.

The DRV816x devices support half-bridge power stage architecture. In addition to the regular 2-pin PWM control interface, the device offers an independent PWM mode by disabling shoot through protection and allowing the high-side and low-side FETs to be controlled independently. Independent FET control is useful for driving solenoids and switched reluctance motors. The DRV8162 and DRV8162L have separate supply pins (GVDD and GVDD_LS) for high-side and low-side FET gate drive. This allows the system to support safe torque off (STO) function by adding external power switches to the gate drive supply pins.

7.3.1.1 PWM Control Modes

The DRV816x family of devices provides three different PWM control modes to support various commutation and control methods. The PWM control modes are 1-pin PWM, 2-pin PWM and independent PWM mode. The modes are configured by DT/MODE pin.

DT/MODE pin is latched at power up, so in order to change the PWM control mode the device needs to be reset through power supply. Refer to 表 7-6 for the configuration of PWM control mode using the DT/MODE pin.

7.3.1.1.1 2-pin PWM Mode

In 2-pin PWM mode, half-bridge driver supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INH and INL signals control the output state as listed in 表 7-1.

表 7-1. 2-pin PWM Mode Truth Table

INL	INH	GL	GH	SH
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

ADVANCE INFORMATION

7.3.1.1.2 1-pin PWM Mode (preview only)

> **警告**
> The DRV8161 prototype samples do not support 1-pin PWM Mode. This function is preview only. Please contact TI for more detailed information.

In 1-pin PWM mode, the IN pin controls half-bridge and supports two output states: low or high. The EN pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie INL/EN pin to logic high. The corresponding INH/IN and INL/EN signals control the output state as listed in 表 7-2.

表 7-2. 1-pin PWM Mode Truth Table (preview only)

INL/EN	INH/IN	GL	GH	SH
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

7.3.1.1.3 Independent PWM Mode

DRV816x supports independent PWM mode, the INH and INL pins control the outputs, GH and GL, respectively. This control mode lets the device drive separate high-side and low-side load. The independent PWM drive mode can be used for various type of loads including solenoids, Switched Reluctance Motor (SRM), unidirectional brushed DC motors, and low-side and high-side switches. In this mode, turning on both the high-side and low-side MOSFETs at the same time in a given half bridge gate driver is possible to use the device as a high-side or low-side driver. The shoot-through protection and dead time are bypassed in the mode.

表 7-3. Independent PWM Mode Truth Table

INL	INH	GL	GH
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

図 7-3 shows how the device can be used to connect an inductive load where both the high-side and low-side MOSFETs can be turned on at the same time to drive the load without causing shoot-through. The external diodes for current recirculation are recommended. This configuration helps the design of solenoids or applications. The trickle charge pump is enabled all the time regardless of low-side PWM activity.

> **注**
> The low-side VDS monitor of DRV816x is not available if independent PWM mode is configured. For DRV8161, the CSA output can be monitored by MCU to detect the over current condition.

ADVANCE INFORMATION

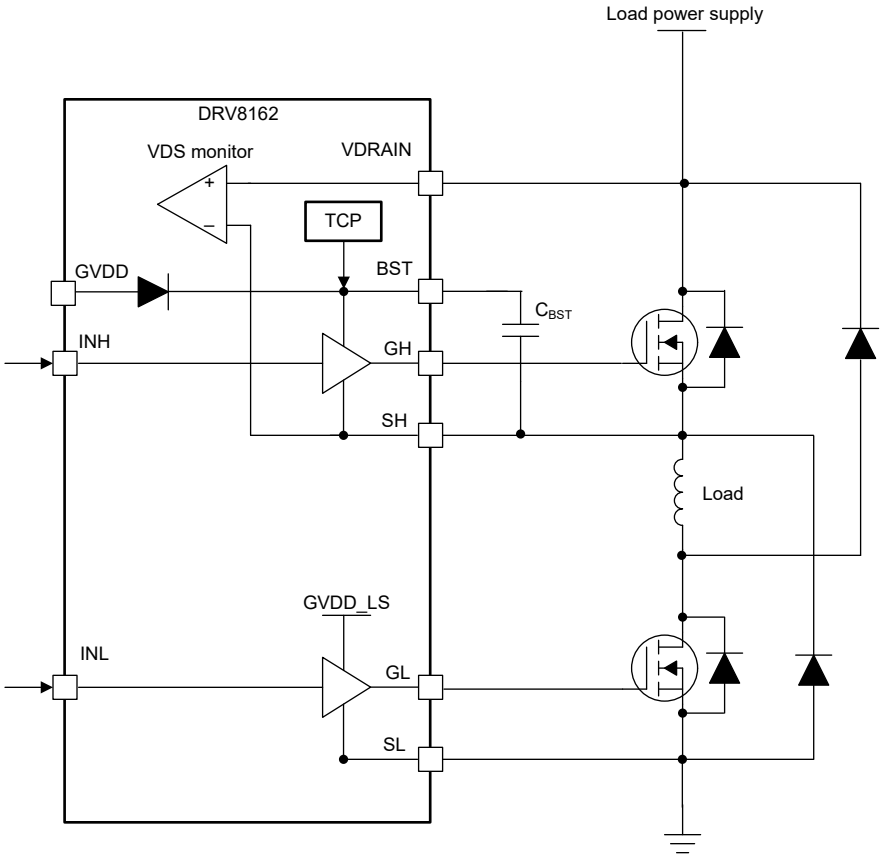


図 7-3. Independent PWM mode for single load between high-side and low-side

図 7-4shows how the device can be used to connect a high-side load and a low-side load at the same time with one half-bridge and drive the loads independently.

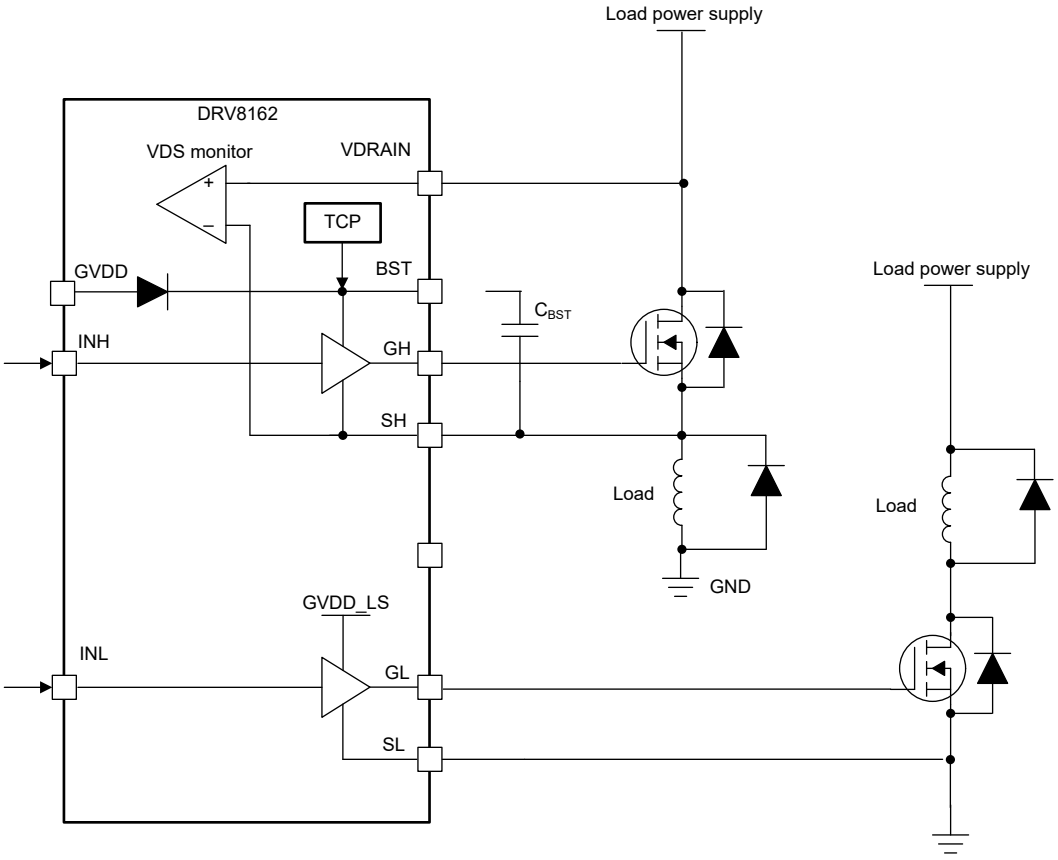


図 7-4. Independent PWM mode for high-side and low-side independent loads

7.3.1.2 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate driver is supplied directly from the GVDD regulator supply. For the high-side gate driver a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BST pin.

The high-side gate driver has semi-active pull down and low side gate has passive pull down to help prevent the external MOSFET from turning ON when power supply is disconnected.

ADVANCE INFORMATION

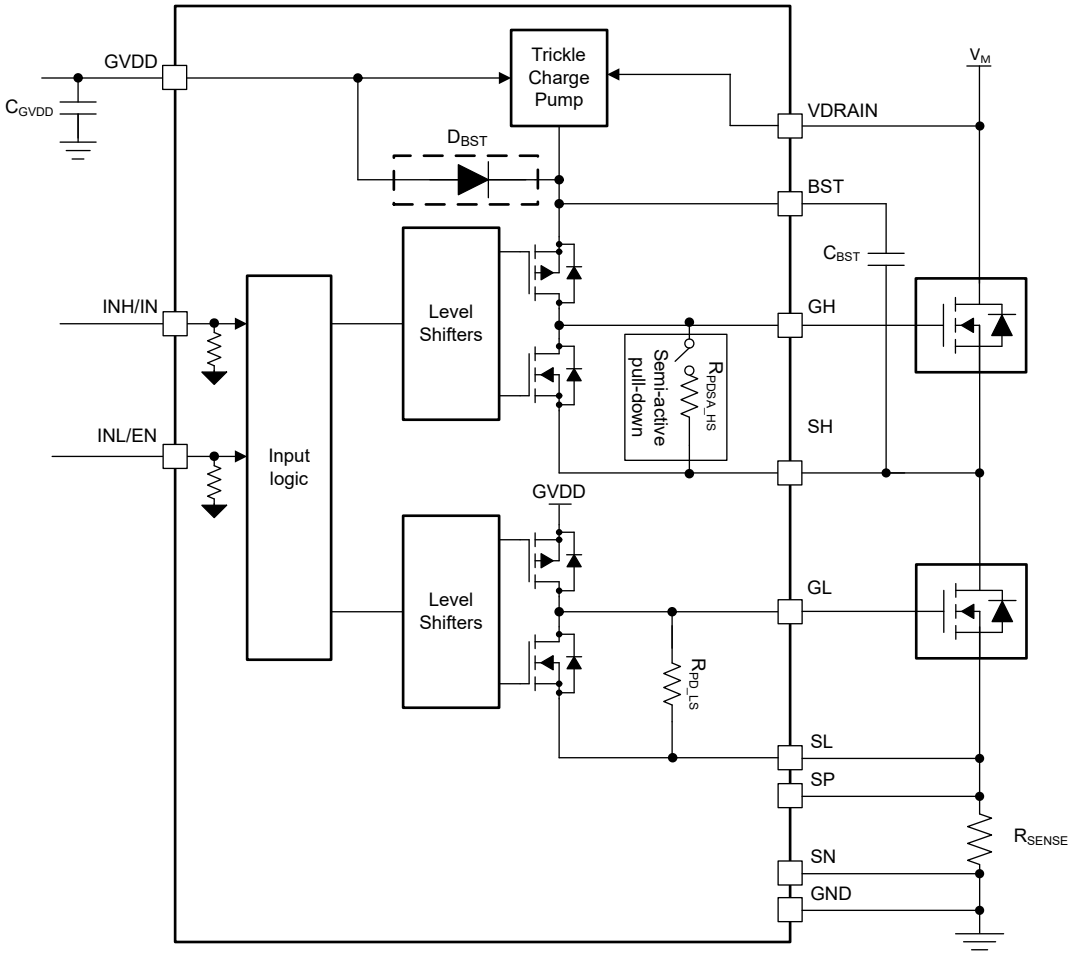


図 7-5. DRV8161 Gate Driver Block Diagram

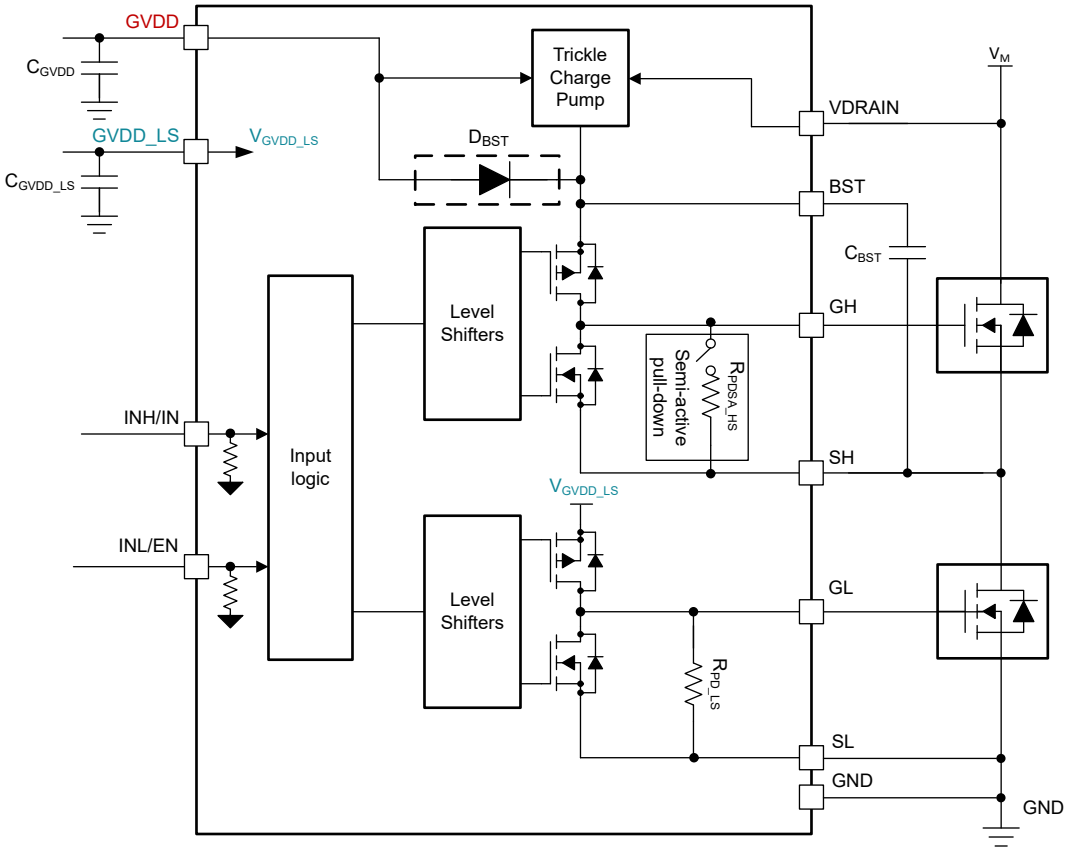


図 7-6. DRV8162 and DRV8162L Gate Driver Block Diagram

7.3.1.2.1 Tickle Charge Pump (TCP)

An internal trickle charge pump (TCP) is connected to BST node to reduce voltage drop due to the leakage currents of the driver and external components. The charge pump generates V_{TCP} voltage with respect to VDRAIN pin. For the independent PWM mode, the charge pump is active all the time. For the 2-pin PWM and 1-pin PWM mode, if the INL stays low for 250us (typ), the charge pump is activated.

警告

Depending on the system use case or the device condition, the output capability of TCP charge pump is not always sufficient to maintain the voltage on C_{BST} during 100% duty cycle. In particular at high temperature, the charge pump output voltage V_{TCP} can be lower than the bootstrap undervoltage threshold V_{BST_UV}, and hence the high-side gate driver output becomes shutdown. To avoid the shutdown, the length of 100% duty cycle time must be limited, or C_{BST} must be charged by system periodically to maintain the voltage.

7.3.1.2.2 Deadtime and Cross-Conduction Prevention (Shoot through protection)

In the DRV816x, if the device is configured to 2-pin PWM mode, high- and low-side inputs operate independently, with an exception to prevent cross conduction when the high and low side of the same half-bridge are turned ON at same time. The device turns OFF high- and low- side output to prevent shoot through when high- and low-side inputs are logic high at same time.

The DRV816x also provide dead time insertion to prevent both external MOSFETs of each half-bridge from switching on at the same time. The deadtime can be enabled and adjusted between 20 ns and 400 ns by connecting resistor between DT/MODE and ground. Refer to セクション 7.3.2.6.

ADVANCE INFORMATION

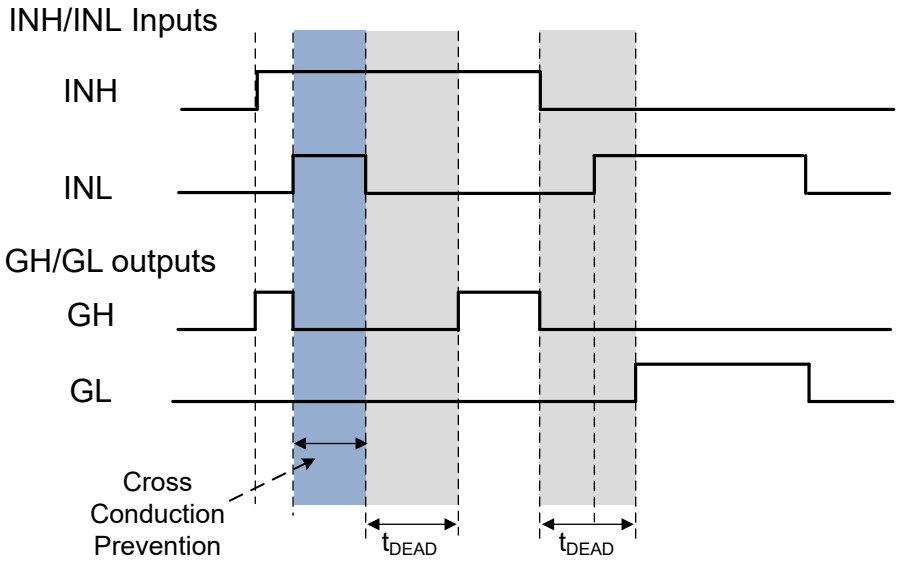


図 7-7. Cross Conduction Prevention and Dead time Insertion (2-pin PWM, dead time insertion enabled)

ADVANCE INFORMATION

7.3.2 Pin Diagrams

7.3.2.1 Four Level Input Pin (CSAGAIN)

図 7-8 shows the structure of the four level input pin, CSAGAIN, for hardware interface configuration. The input can be set with an external resistor. The $C_{CSAGAIN}$ is optional to help reduce the impact of GND noise. The CSA GAIN information is not latched at the device power up and may be updated during the device operation.

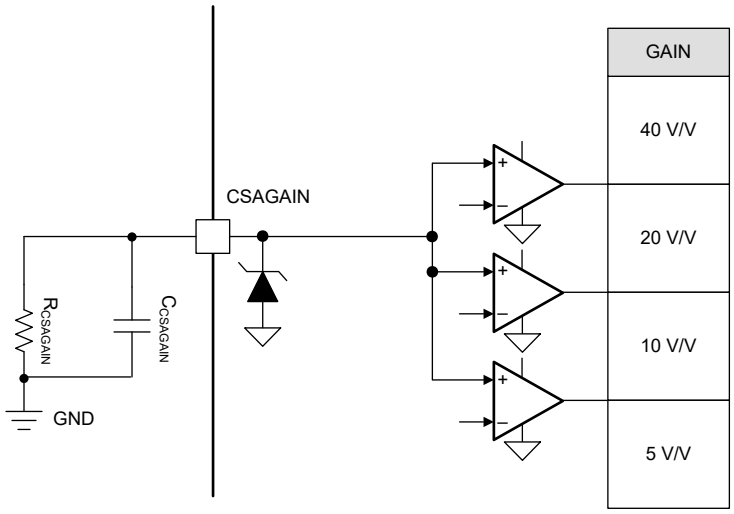


図 7-8. Four Level Input Pin Structure

7.3.2.2 Digital output nFAULT (DRV8162, DRV8162L)

図 7-9 shows the structure of the open-drain output pins, nFAULT. The open-drain output requires an external pullup resistor to function correctly. Refer to 表 7-7 for the device actions including nFAULT.

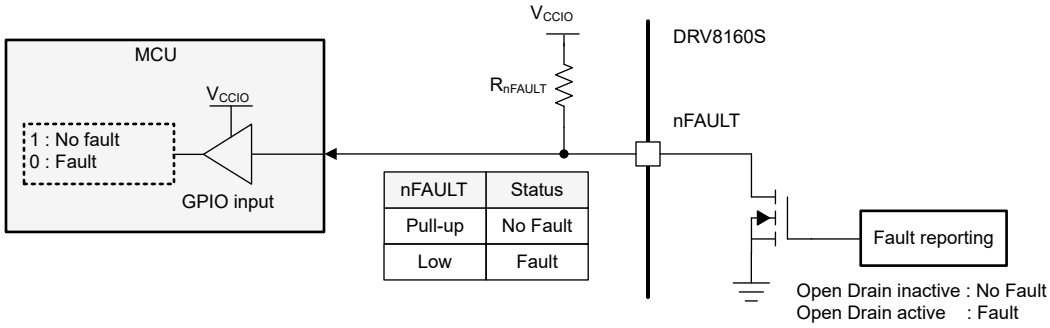
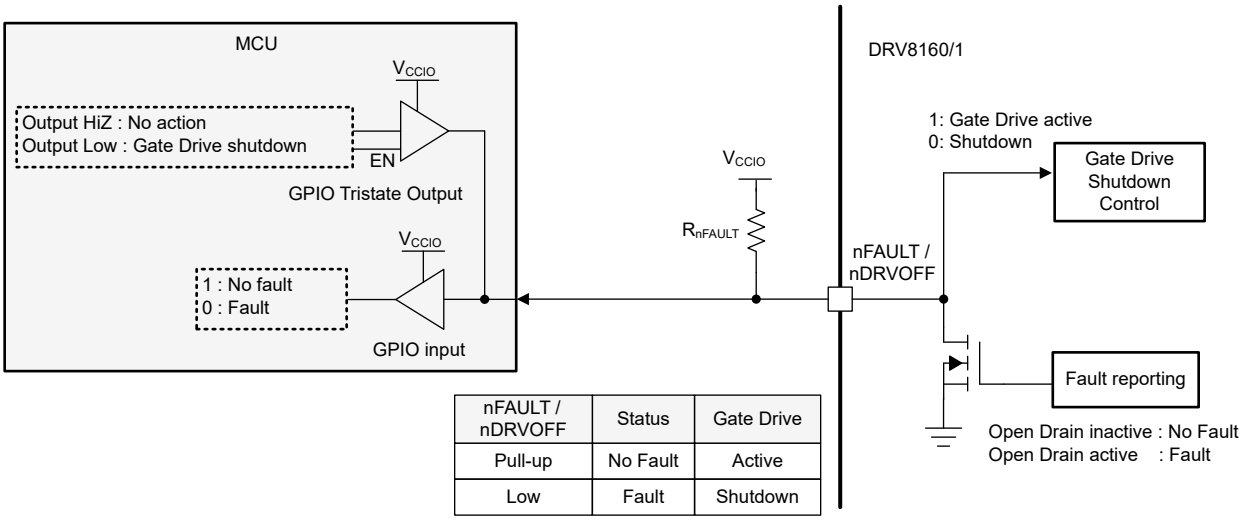


図 7-9. nFAULT Open Drain Output buffer

7.3.2.3 Digital InOut nFAULT/nDRVOFF (DRV8161)

図 7-10 shows the structure of the open-drain output and input pin. In the DRV8161 device variant, two functions nFAULT and nDRVOFF are achieved by sharing one device pin, nFAULT/nDRVOFF. The open-drain output requires an external pullup resistor to function correctly. If a fault condition is detected, the device activates Open Drain buffer, and nFAULT/nDRVOFF pin is driven low. The nFAULT/nDRVOFF pins is internally connected to Gate Drive Shutdown logic, and the gate drive outputs are shutdown (pull-down) if the nFAULT/nDRVOFF pin low. Refer to 表 7-7 for the device actions including nFAULT.

ADVANCE INFORMATION



nFAULT / nDRVOFF	Status	Gate Drive
Pull-up	No Fault	Active
Low	Fault	Shutdown

図 7-10. nFAULT/nDRVOFF Open Drain Output and Input buffer

7.3.2.4 Multi-level inputs (IDRIVE1 and IDRIVE2)

The DRV816x have IDRIVE1 and IDRIVE2 device pins for gate drive current configuration. Each pin can set 8 levels, LEVEL0 to LEVEL7, with an external resistor connected between the device pin and GND. The gate drive current I_{DRIVEN} and I_{DRIVEP} can be determined by 表 7-4. The (G) in the table indicates that VGS monitor dead time insertion is enabled. The IDRIVE1 and IDRIVE2 information are latched at the device power up.

ADVANCE INFORMATION

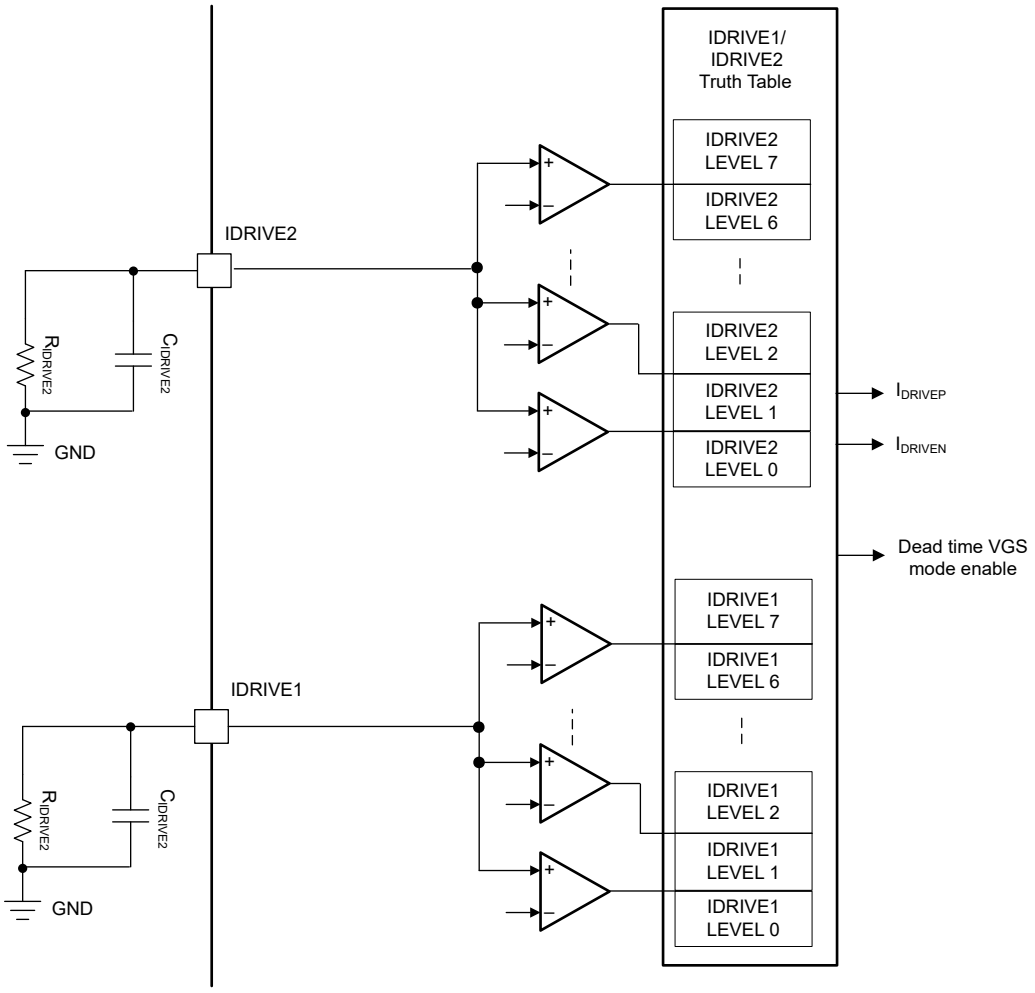


図 7-11. Multi-level digital inputs of IDRIVE1 and IDRIVE2

ADVANCE INFORMATION

表 7-4. IDRIVE1/IDRIVE2 Truth Table for Gate Drive Current configuration

		IDRIVE2															
		LEVEL0		LEVEL1		LEVEL2		LEVEL3		LEVEL4		LEVEL5		LEVEL6		LEVEL7	
		Source:Sink = 1:2		Source:Sink = 1:2		Source:Sink = 1:1.5		Source:Sink = 1:1.5		Source:Sink = 1:1		Source:Sink = 1:3		VGS dead time insertion enabled		IDRIVE2 open	
		I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]	I_{DRIVE_P}[mA]	I_{DRIVE_N}[mA]
IDRIVE1	LEVEL7	256	512	16	32	256	384	16	32	128	128	64	192	32 (G)	64 (G)	16 (G)	32 (G)
	LEVEL6	288	576	32	64	288	448	32	32	192	192	128	384	96 (G)	192 (G)	64 (G)	128 (G)
	LEVEL5	320	640	64	128	320	448	64	64	256	256	192	576	128 (G)	256 (G)	128	256
	LEVEL4	384	768	96	192	384	576	96	128	320	320	256	768	160 (G)	320 (G)	192	384
	LEVEL3	448	896	128	256	448	640	128	192	384	384	288	896	192 (G)	384 (G)	256	512
	LEVEL2	512	1024	160	320	512	768	160	256	448	448	384	1024	224 (G)	448 (G)	320	640
	LEVEL1	768	1536	192	384	768	1024	192	256	512	512	512	1536	512 (G)	1024 (G)	512	1024
	LEVEL0	1024	2048	224	448	1024	1536	224	384	1024	1024	768	2048	1024 (G)	2048 (G)	1024	2048

7.3.2.5 Multi-level digital input (VDSLVL)

The VDS monitor threshold level of DRV816x is configurable using VDSLVL pin. The pin can set 8 levels, LEVEL0 to LEVEL7, with an external resistor connected between VDSLVL and GND. The 7 threshold levels are determined by 表 7-5. As shown in 図 7-13, if one digital pulse is applied to VDSLVL pin, additional 6 threshold levels are available. If VDSLVL pin is open, VDS monitor function is disabled. The VDS monitor threshold infomration is latched at the device power up.

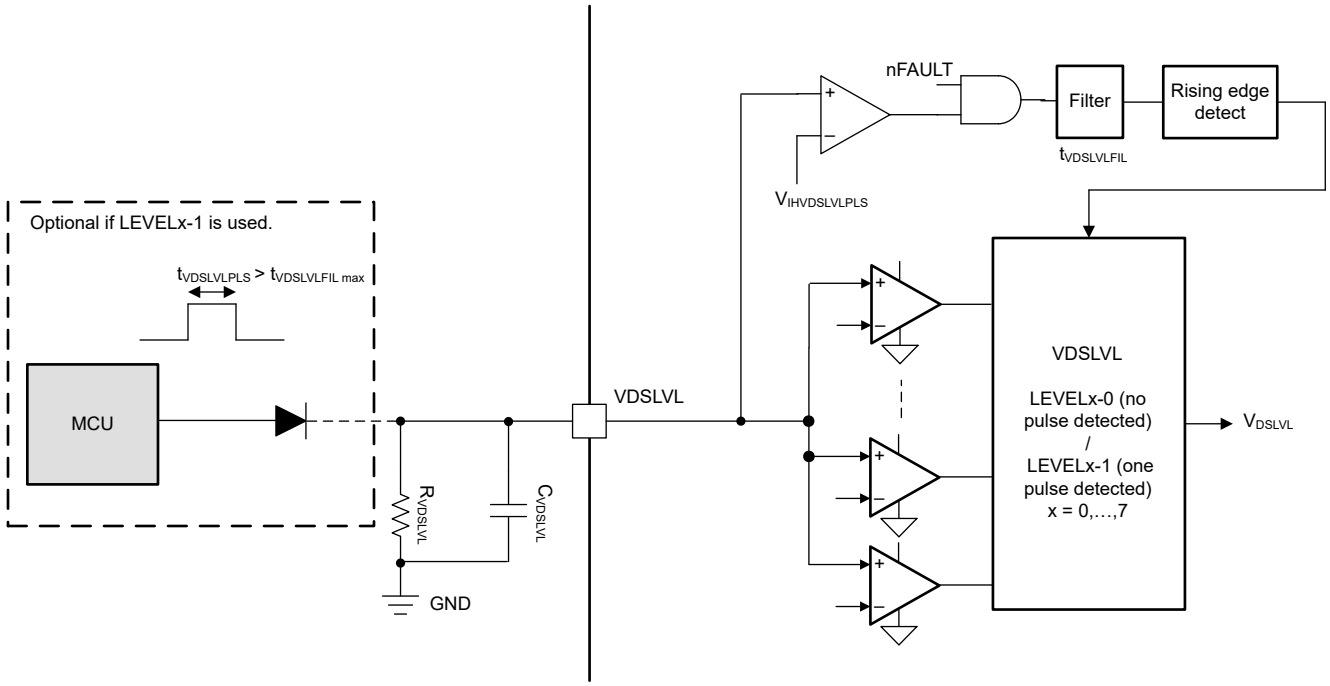


図 7-12. VDSLVL input pulse timing diagram

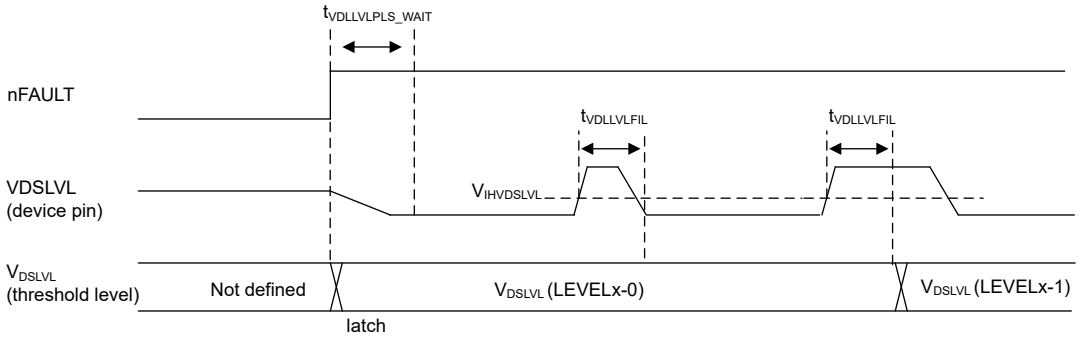


図 7-13. Multilevel digital input of VDSLVL

表 7-5. VDS threshold level selection table

VDSLVL input pin (R_{VDSLVL})	VDS monitor threshold	
	LEVELx-0 (no pulse detected)	LEVELx-1 (one pulse detected)
LEVEL7 (OPEN)	Disabled	Disabled
LEVEL6 (130KΩ typ)	2-V	1.5-V
LEVEL5 (62KΩ typ)	1-V	0.9-V
LEVEL4 (27KΩ typ)	0.8-V	0.7-V
LEVEL3 (12KΩ typ)	0.6-V	0.5-V
LEVEL2 (5.6KΩ typ)	0.4-V	0.3-V
LEVEL1 (2KΩ typ)	0.2-V	0.15-V
LEVEL0 (Short to GND)	0.1-V	Not available

7.3.2.6 Multi-level digital input DT/MODE

図 7-14 shows the structure of mutlelevel input pin DT/MODE for hardware interface configuration. The input can be set with an external resistor R_{DTMODE} connected to GND. The C_{DTMODE} is optional to help reduce the impact

ADVANCE INFORMATION

of GND noise. The shoot through function, dead time insertion, and PWM control mode are configured as shown in 表 7-6. The information of LEVEL0, 1, 2, 3, and LEVEL5 are latched at the device power up.

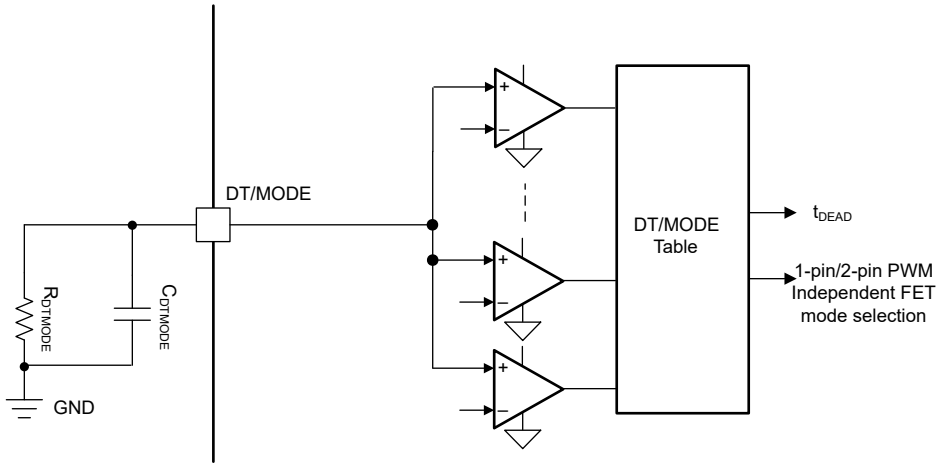


図 7-14. DT/MODE Pin Structure

表 7-6. DT/MODE Table

DT/MODE (R_{DTMODE})	Shoot Through protection	Dead Time Insertion (t_{DEAD})	PWM Control mode
LEVEL5 (pin floating)	enabled	disabled	2-pin PWM
LEVEL4 - Linear (10 KΩ - 1 MΩ)	Reserved.		
LEVEL3 (3.3 KΩ)	enabled	enabled (370-ns)	2-pin PWM
LEVEL2 (1.3 KΩ)	enabled	enabled (100-ns)	2-pin PWM
LEVEL1 (470 Ω)	enabled	enabled (20-ns)	2-pin PWM
LEVEL0 (short to GND)	disabled	disabled	Independent PWM

7.3.3 Low-Side Current Sense Amplifiers

The DRV8161 integrates high-performance low-side current sense amplifier for current measurements using low-side shunt resistor. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. Current sense amplifier can be used to sense the sum of the half-bridge current. The current sense amplifier includes features such as configurable gain, and a voltage reference pin (CSAREF). DRV8161 generates internally a common voltage of V_{CSAREF}/2.

The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). Gain settings can be configured through CSAGAIN pin.

ADVANCE INFORMATION

7.3.3.1 Bidirectional Current Sense Operation

DRV8161 internally generates common mode voltage to enable bidirectional for current measurement. The current sense amplifier operates as bidirectional mode and the SO pin outputs an analog voltage equal to the voltage across the SP and SN pins multiplied by the gain setting (G_{CSA}) plus the output bias voltage V_{VREF} / 2 .

Use 式 1 to calculate the current through the shunt resistor (CSAREF / 2 case) .

$$I = \frac{V_{SOx} - \frac{V_{VREF}}{2}}{G_{CSA} \times R_{SENSE}} \quad (1)$$

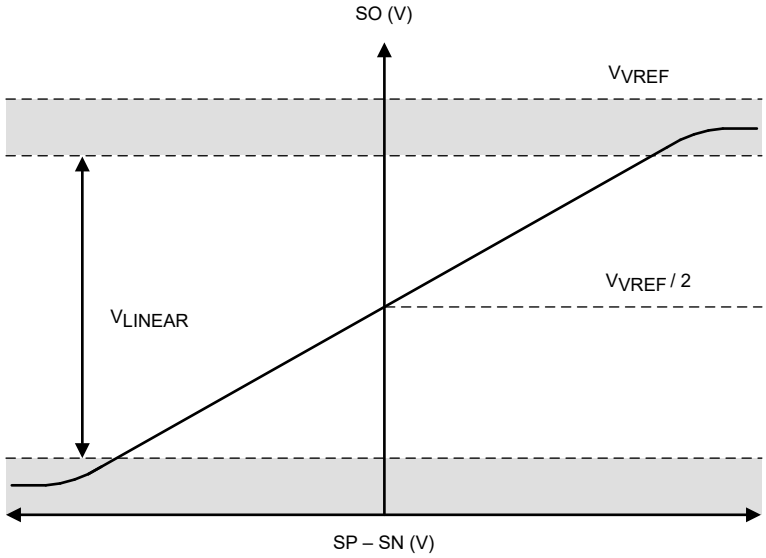


図 7-15. Bidirectional Current Sense Output

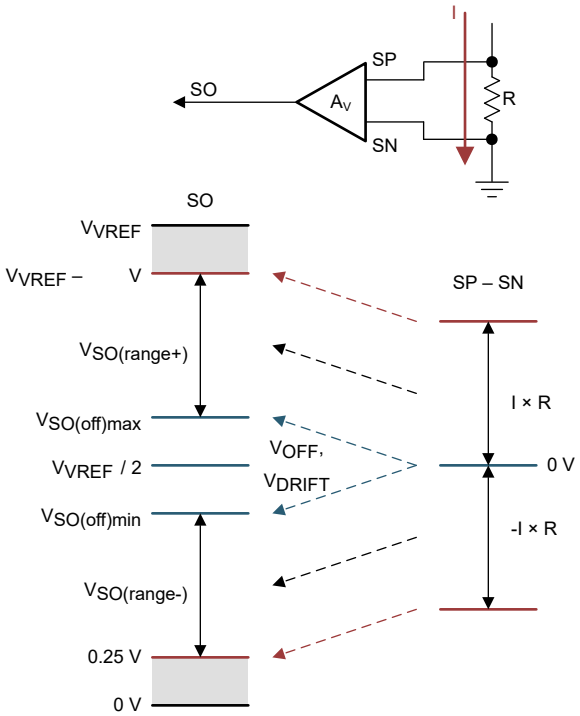


図 7-16. Bidirectional Current Sense Regions

ADVANCE INFORMATION

7.3.4 Gate Driver Shutdown Sequence (nDRVOFF)

When nDRVOFF is driven low, the gate driver goes into shutdown, overriding signals on inputs pins INH/IN and INL/EN. nDRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output. This pin provides a mechanism for externally monitored faults to disable gate driver by directly bypassing an external controller or the internal control logic. When DRV816x detect the nDRVOFF pin is driven low, the device disables the gate driver and puts it into pulldown mode. The gate driver shutdown sequence proceeds as shown in 図 7-17. When the gate driver initiates the shutdown sequence, the active driver pulldown is applied at I_{DRVN_SD} current for the t_{DRVN_SD} time.

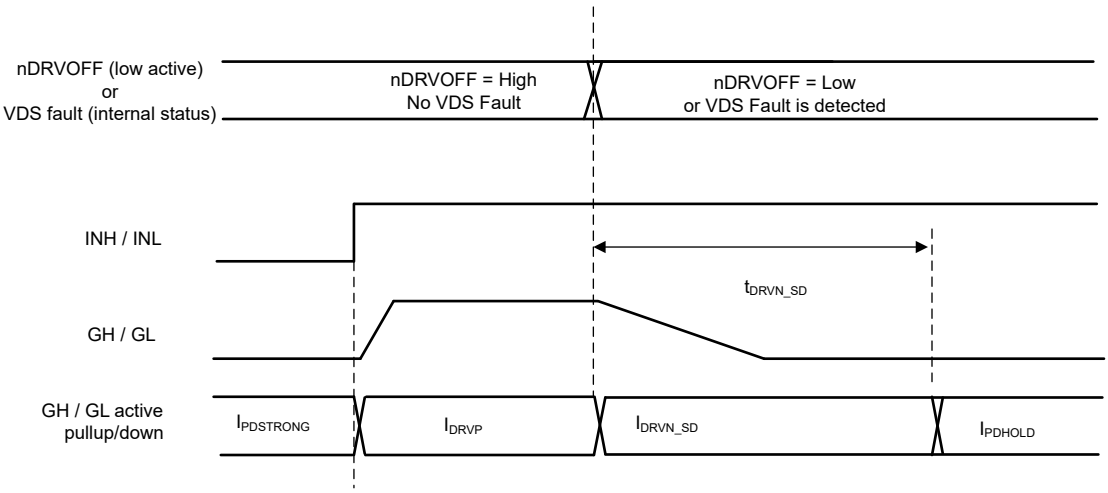


図 7-17. Gate Driver Shutdown Sequence

7.3.4.1 nDRVOFF Diagnostic

図 7-18 proposes a diagnostic of nDRVOFF of DRV8162 and DRV8162L. If a low active pulse $t_{nDRVOFF\_DIAG}$ (typ 0.5us) is applied to nDRVOFF pin, the device responds by driving nFAULT low without shutdown of the gate driver outputs. This device function is intended for a diagnostic of nDRVOFF function while continuing PWM operation. If nDRVOFF is driven low longer than $t_{nDRVOFF\_DEG}$, the device initiates the shutdown.

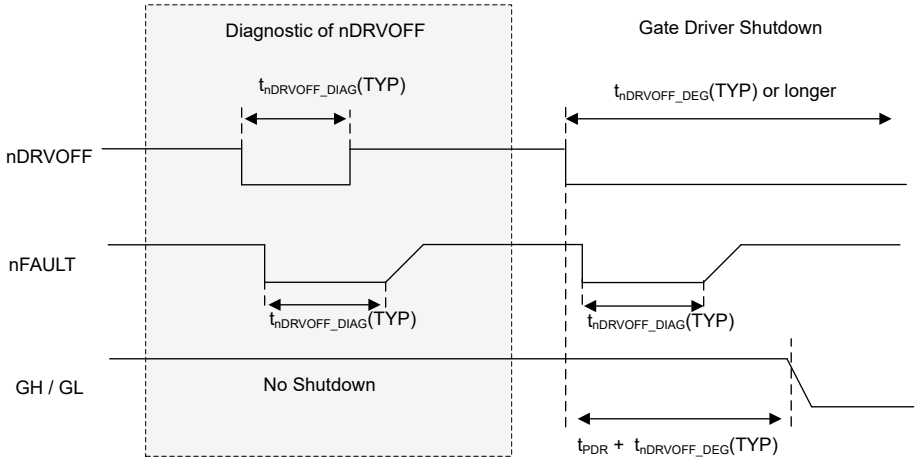


図 7-18. nDRVOFF Diagnostic

7.3.5 Gate Driver Protective Circuits

The DRV816x are protected against GVDD undervoltage and overvoltage, bootstrap undervoltage, MOSFET V_{DS} and Overtemperature (OTSD) events.

表 7-7. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER GH	GATE DRIVER GL	RECOVERY
GVDD undervoltage (GVDD_UV)	$V_{GVDD} < V_{GVDD\_UV}$	-	nFAULT	S-PD(1)	P-PD(2)	$V_{GVDD} > V_{GVDD\_UV}$
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{DSLVL}$	VDSLVL pin with R (LEVEL0 - LEVEL6)	nFAULT	S-PD (1)	P-PD(2)	Latched: INH(IN) = Low & INL(EN) = Low for > t_{CLKFLT}
		VDSLVL pin open (LEVEL7)	None	Active(3)	Active(3)	No action
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	-	nFAULT	S-PD (1)	P-PD(2)	$T_J < T_{OTSD}$
Bootstrap undervoltage	$V_{BST-SH} < V_{BST\_UV}$	-	None	S-PD(1)	Active(3)	$V_{BST-SH} > V_{BST\_UV}$

(1) S-PD : Semi-active Pull Down
(2) P-PD : Passive Pull Down
(3) Active : Gate Drivers are active for PWM

7.3.5.1 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD\_UV\_DG}$ deglitch time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is disabled, and the nFAULT pin pulls low. After the GVDD_UV condition is cleared, the nFAULT goes high.

7.3.5.2 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

The DRV816x devices have adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the VDRAIN and SH pins. The low-side VDS monitors measure between the SH and SL pins. If the voltage across external MOSFET exceeds the V_{VDSLVL} threshold for longer than the t_{DS_DG} deglitch time, a VDS_OCP event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The VDS threshold can be set between 0.1 V to 2.0 V by VDSLVL pin. The VDS deglitch time is fixed at t_{VDSDEG}. The VDS OCP can be disabled by leaving VDSLVL pin open. After the over current condition is cleared, the fault state remains latched and can be cleared when INH(IN) and INL(EN) stay low for t_{CLRFLT} time.

ADVANCE INFORMATION

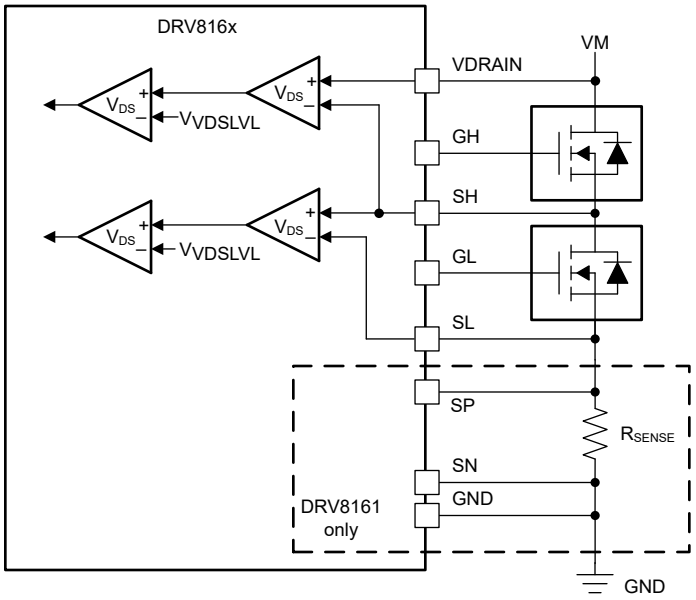


図 7-19. DRV816x MOSFET V_{DS} Overcurrent protection

7.3.5.3 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. After OTSD condition is cleared, the device returns to normal operation and nFAULT goes high.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV816x family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *セクション 8.2* section highlight how to use and configure the DRV816x family of devices.

8.2 Typical Application

8.2.1 Typical Application with DRV8161

Figure shows a typical application diagram of DRV8161.

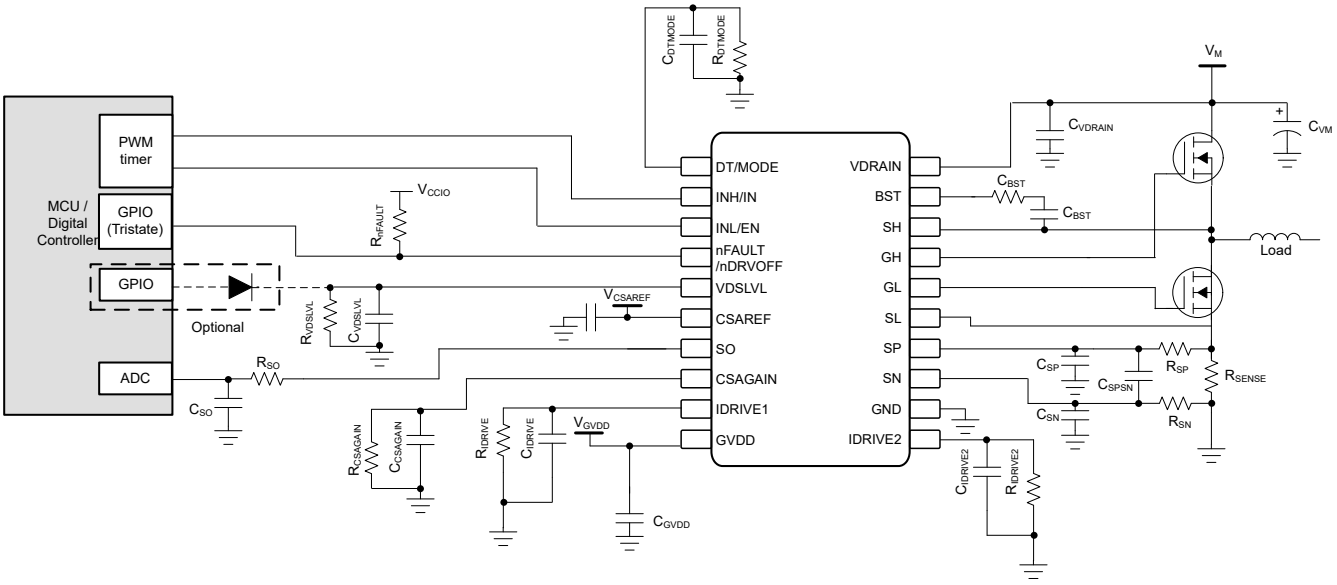


図 8-1. Typical application diagram of DRV8161

8.2.2 Typical Application with DRV8162 and DRV8162L

Figure shows a typical application diagram of DRV8162 and DRV8162L.

ADVANCE INFORMATION

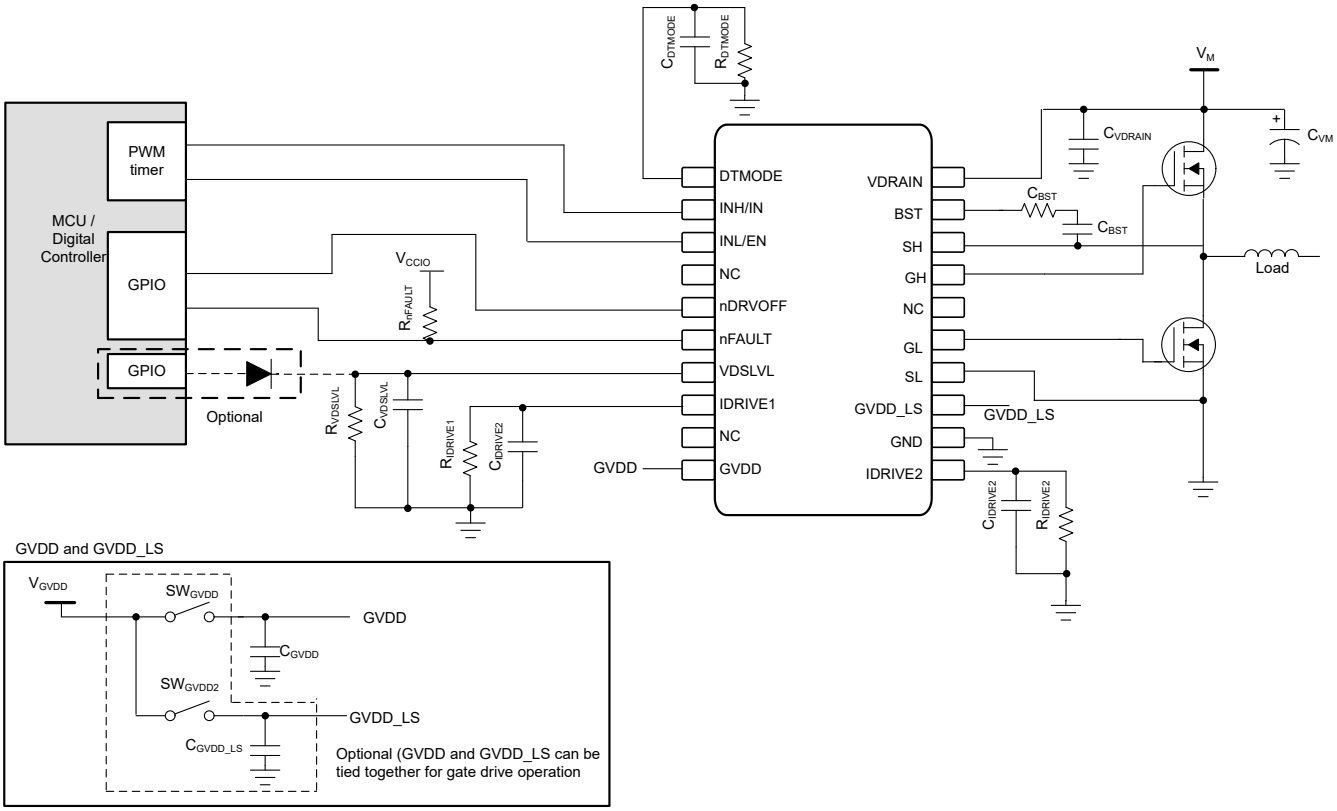


図 8-2. Typical application diagram of DRV8162 and DRV8162L

8.2.3 External Components

The table lists the recommended values of the external components for the gate driver.

表 8-1. DRV816x External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{BST}	BST	SH	1.0-µF, V_{BST-SH}-rated capacitor between BST and SH depending on the total gate charge of external MOSFET Qg. C_{BST} > 20 X Qg / (V_{GH}-V_{SH}). The maximum C_{BST} is 2.2-µF,
C_{GVDD}	GVDD	GND	10-µF, V_{GVDD}-rated capacitor. This capacitor can be shared with the other two DRV816x devices in 3-phase power stage design if the capacitor is placed sufficiently close to all the three devices. The voltage drop due to bootstrap operation at power up and during PWM switching must be reviewed by users.
C_{GVDD_LS}	GVDD_LS	GND	1-µF, V_{GVDD}-rated capacitor
C_{VDRAIN}	VDRAIN	GND	0.1-µF, V_{VDRAIN}-rated capacitor
R_{nFAULT}	V_{CCIO}	nFAULT	Pullup resistor 10K-Ω
$R_{IDRIVE1}$	IDRIVE1	GND	Hardware interface resistor See セクション 7.3.2.4
$C_{IDRIVE1}$	IDRIVE1	GND	OPTIONAL: 0.1-nF, 5-V -rated capacitor
$R_{IDRIVE2}$	IDRIVE2	GND	Hardware interface resistor See セクション 7.3.2.4
$C_{IDRIVE2}$	IDRIVE2	GND	OPTIONAL: 0.1-nF, 5-V -rated capacitor
R_{VDSLVL}	VDSLVL	GND	Hardware interface resistor See セクション 7.3.2.5
C_{VDSLVL}	VDSLVL	GND	OPTIONAL: 0.1-nF, 5-V -rated capacitor
D_{VDSLVL}	VDSLVL	MCU	OPTIONAL: Diode between VDSLVL pin and MCU GPIO.

ADVANCE INFORMATION

表 8-1. DRV816x External Components (続き)

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
R_{DTMODE}	DT/MODE	GND	Hardware interface resistor See セクション 7.3.2.6
C_{DTMODE}	DT/MODE	GND	OPTIONAL: 0.1-nF, 5-V -rated capacitor
$R_{CSAGAIN}$	CSAGAIN	GND	Hardware interface resistor See セクション 7.3.2.1
$C_{CSAGAIN}$	CSAGAIN	GND	OPTIONAL: 0.1-nF, 5-V -rated capacitor
C_{CSAREF}	CSAREF	GND	0.1-µF, V_{CSAREF}-rated capacitor
R_{SENSE}	SP	SN	Sense shunt resistor
R_{SP}, R_{SN}	SP/SN	R_{SENSE}	OPTIONAL: 10-Ω for current sense amplifier input filter.
C_{SPSN}	SP	SN	OPTIONAL: 1-nF ceramic capacitor for current sense amplifier input filter.
C_{SP}, C_{SN}	SP/SN	GND	OPTIONAL: 1-nF ceramic capacitor for current sense amplifier input filter.

ADVANCE INFORMATION

9 Layout

9.1 Layout Guidelines

- Minimize length and impedance of GH, SH, GL, and SL traces. Use as few vias as possible to minimize parasitic inductance. It is also recommended to increase these trace widths shortly after routing away from the device pin to minimize parasitic resistance.
- Keep bootstrap capacitor C_{BST} close to their respective pins
- Keep GVDD capacitors close to GVDD pin
- Keep VDRAIN capacitor close to VDRAIN pin to supply steady switching current for the charge pump.
- Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.
- Connect SL pin to MOSFET source, not directly to GND, for accurate VDS detection.
- DRV8161 only: Route SN/SP pins in parallel from the sense resistor to the device. Place filtering components close to the device pins to minimize post-filter noise coupling. Ensure that SN/SP stay separated from GND plane to achieve best CSA accuracy.
- The hardware interface resistors $R_{IDRIVE1}$, $R_{IDRIVE2}$, R_{VDSLVL}, R_{DTMODE}, and $R_{CSAGAIN}$ should be placed as close as possible to the device pins.
- Minimize parallel routing to reduce noise coupling from potential noise source into any noise-sensitive device signals. The noise-sensitive signals include the multilevel hardware interface pins IDRIVE1, IDRIVE2, VDSLVL, DTMODE and CSAGAIN as well as the current sense amplifier output SO.

10 Device and Documentation Support

10.1 Device Support

10.2 Documentation Support

10.2.1 Related Documentation

- Texas Instruments, *Understanding Smart Gate Drive (Rev. D)* application report
- Texas Instruments, *Brushless-DC Motor Driver Considerations and Selection Guide (Rev. A) application report*
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers (Rev. B)* application note
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle Using a BLDC Motor* application report
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430* application report

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

10.5 Trademarks

すべての商標は、それぞれの所有者に帰属します。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2024) to Revision A (July 2024)	Page
• 新しいデバイスの注文可能番号 DRV8328L を追加	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

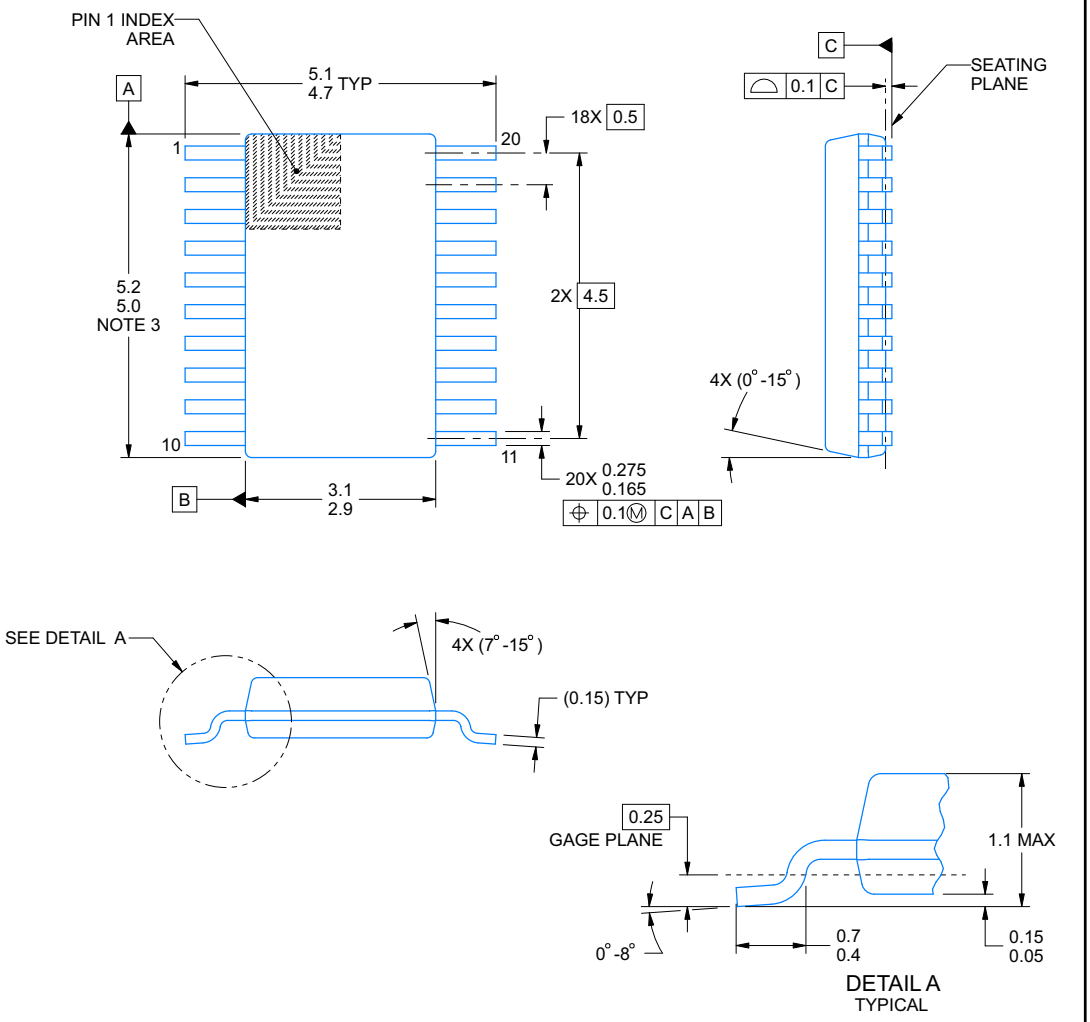
ADVANCE INFORMATION

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

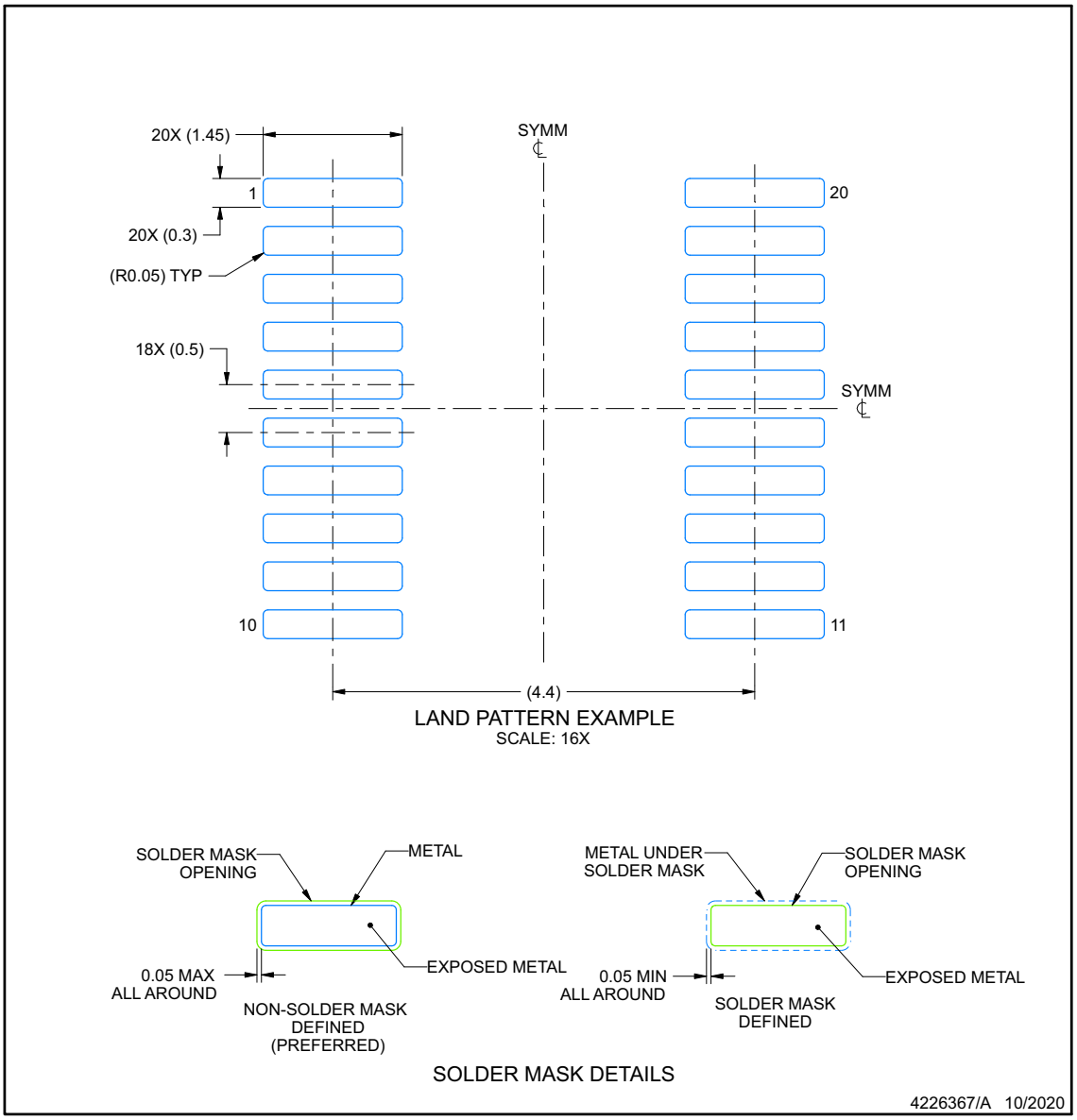
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

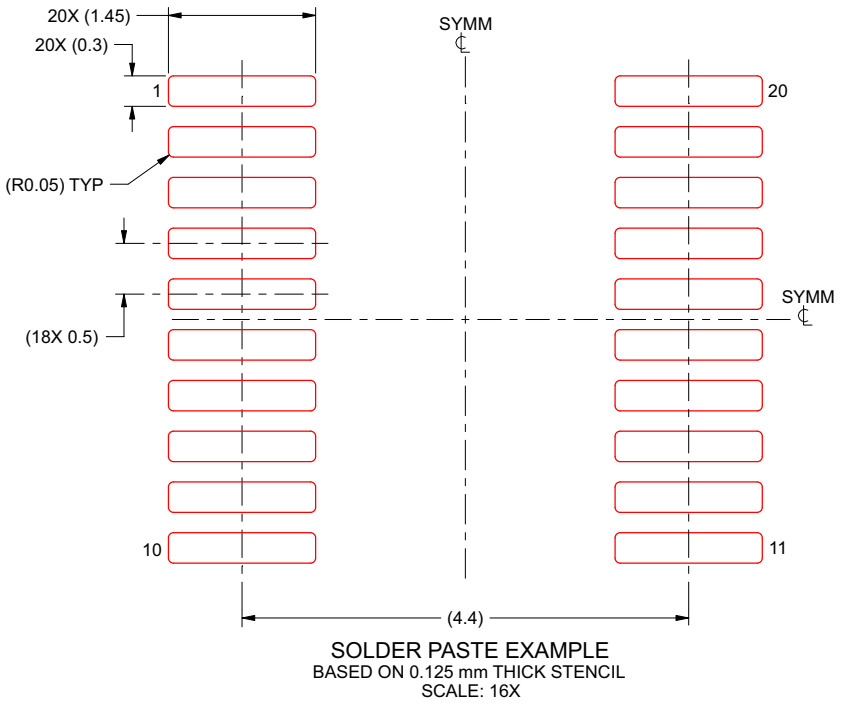
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DGS0020A — **VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

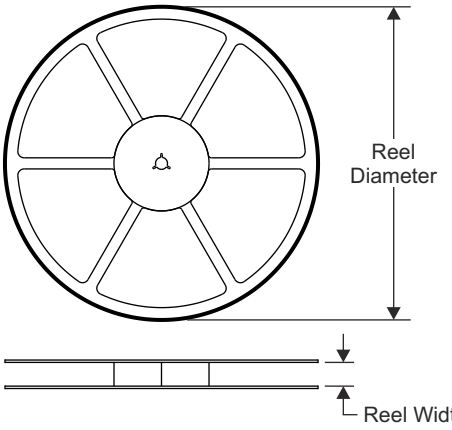
4226367/A 10/2020

NOTES: (continued)

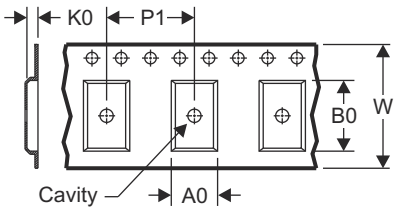
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

12.1 Tape and Reel Information

REEL DIMENSIONS

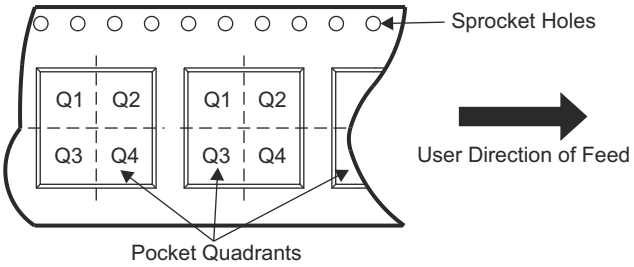


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

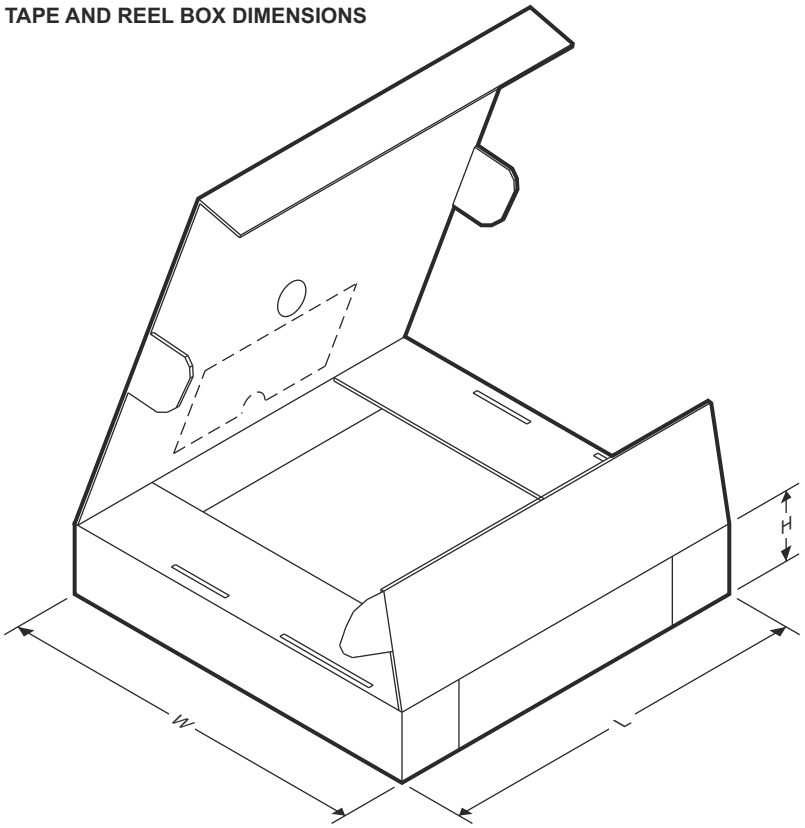


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDRV8161DGSR	VSSOP	DGS	20	3000	330.0	16.4	5.4	5.4	1.45	8.0	13.3	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDRV8161DGSR	VSSOP	DGS	20	3000	367.0	367.0	35.0

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV8161DGSR	ACTIVE	VSSOP	DGS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PDRV8162LDGSR	ACTIVE	VSSOP	DGS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265