TEXAS INSTRUMENTS
DRV8262-Q1
JAJST19 – FEBRUARY 2024

DRV8262-Q1：24V および 48V 車載アプリケーション向け、電流検出出力搭載、60V、シングルまたはデュアル H ブリッジ モータ ドライバ

1 特長

- 車載用 **AEC-Q100** 認定済み
  - 温度グレード 1：-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システム設計に役立つ資料を利用可能
- – シングルまたはデュアル H ブリッジ モータドライバ
  - 1 つまたは 2 つのブラシ付き DC モータを駆動
  - 1 つのステッパ モータ
  - 1 つまたは 2 つの熱電冷却器 (TEC)
- **4.5V～60V** の動作電源電圧範囲
- 低い $R_{DS(ON)}$：
  - **100mΩ** HS + LS (**デュアル** H ブリッジ)
  - **50mΩ** HS + LS (**シングル** H ブリッジ)
- 高い出力電流能力：
  - デュアル H ブリッジ (24V、25℃)：**ピーク 8A**
  - シングル H ブリッジ (24V、25℃)：**ピーク 16A**
- 動作インターフェイスをプログラム可能
  - 位相 / イネーブル (**PH/EN**)
  - PWM (**IN/IN**)
- 電流検出およびレギュレーション機能を内蔵
  - ハイサイド MOSFET の電流検出
  - 各 H ブリッジの検出出力 (**IPROPI**)
  - 最大電流時に **±4 %** の検出精度
- 独立したロジック電源電圧 (**VCC**)
- オフ時間 PWM チョッピングを構成可能
  - 7、16、24 または 32µs
- フォルトからの回復方法をプログラム可能
- 1.8V、3.3V、5.0V のロジック入力をサポート
- 低消費電流のスリープ モード (**3µA**)
- 保護機能
  - VM 低電圧誤動作防止 (UVLO)
  - チャージ ポンプ低電圧 (CPUV)
  - 過電流保護 (OCP)
  - サーマル シャットダウン (OTSD)
  - フォルト条件出力 (nFAULT)

2 アプリケーション

- **24V および 48V 車載ボディ・システム**
- 車載用 ブラシ付き DC モータ
- ドア・モジュール、ミラー、シフタ、シート
- トランク・リフト、ウィンドウ・リフト
- ステアリング・コラム、サンルーフ・シェード
- 電気自動車、トラック、バス、その他の商用車

3 概要

DRV8262-Q1 は、24V および 48V 車載アプリケーション向けの、電圧範囲の広い大電力の H ブリッジ モータ ドライバです。このデバイスは 2 個の H ブリッジを内蔵しており、1 個もしくは 2 個の DC モータまたは 1 個のバイポーラ ステッパ モータを駆動します。DRV8262-Q1 は、デュアル H ブリッジ モードで最大 8A、シングル H ブリッジ モードで最大 16A のピーク電流をサポートしています。このデバイスは、電流検出とレギュレーション、電流検出出力、保護回路も内蔵しています。

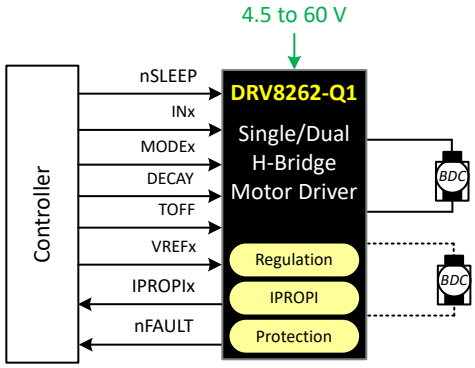
複数のハイサイド MOSFET 間にまたがる電流検出機能を内蔵しているため、ドライバは起動時や高負荷時にもモータの電流をレギュレートできます。可変の外部基準電圧により、電流制限を設定できます。また、このデバイスは、各 H ブリッジのモータ電流に比例した出力電流を供給します。センシング機能を内蔵しているので、シャント抵抗が不要になり、ボード面積の節減とシステムコストの削減につながります。

低消費電力のスリープ モードにより、非常に低い待機時消費電流を実現できます。保護機能として、電源低電圧誤動作防止 (UVLO)、チャージ ポンプ低電圧検出 (CPUV)、出力過電流検出 (OCP)、デバイス過熱検出 (OTSD) を内蔵しています。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ (2)	本体サイズ (公称)
DRV8262QDD WRQ1	HTSSOP-44	14mm × 8.1mm	14mm × 6.1mm

(1) 巻末の注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



DRV8262-Q1 の概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

The DRV8262-Q1 is available in thermally-enhanced, 44-Pin HTSSOP package.

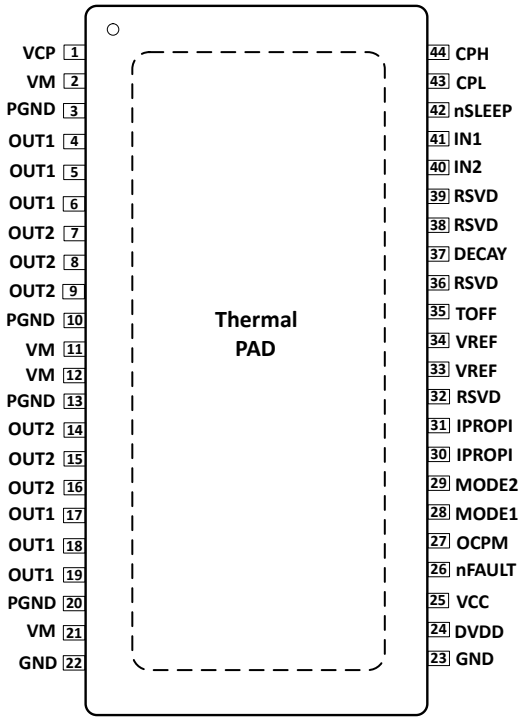

図 4-1. Single H-bridge Mode, Top View

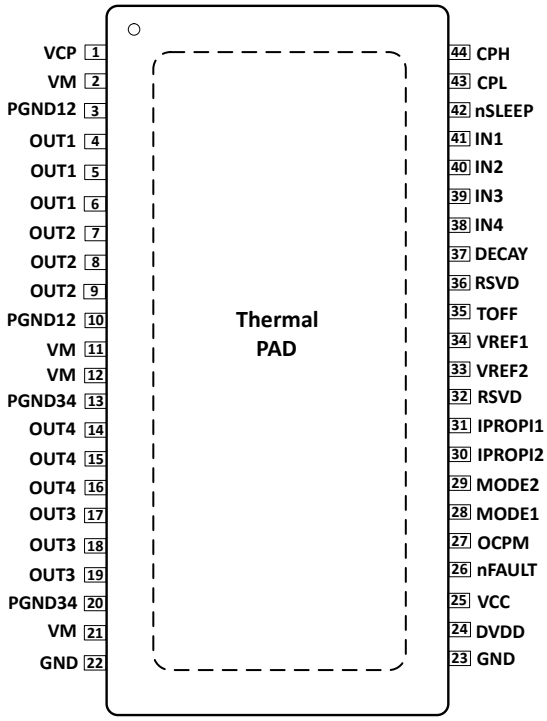

図 4-2. Dual H-bridge Mode, Top View

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表 4-1. Pin Configuration

PIN			TYPE	DESCRIPTION
NAME		DDW		
Single H-Bridge	Dual H-Bridge			
RSVD	IN4	38	Input	PWM input for H-bridge 2 in dual H-bridge mode. Leave this pin unconnected in single H-bridge mode.
RSVD	IN3	39	Input	PWM input for H-bridge 2 in dual H-bridge mode. Leave this pin unconnected in single H-bridge mode.
IPROPI	IPROPI2	30	Output	Analog current output for H-bridge 2 in dual H-bridge mode. Connect to the other IPROPI pin in single H-bridge mode.
IPROPI	IPROPI1	31	Output	Analog current output for H-bridge 1 in dual H-bridge mode. Connect to the other IPROPI pin in single H-bridge mode.
VREF	VREF2	33	Input	Reference input to set current for H-bridge 2 in dual H-bridge mode. Tie to the other VREF pin in single H-bridge mode. DVDD can be used to provide VREF through a resistor divider.
VREF	VREF1	34	Input	Reference input to set current for H-bridge 1 in dual H-bridge mode. Tie to the other VREF pin in single H-bridge mode. DVDD can be used to provide VREF through a resistor divider.
PGND	PGND12	3, 10	Power	Power ground for H-bridge. Connect to system ground.
PGND	PGND34	13, 20	Power	Power ground for H-bridge. Connect to system ground.
OUT1	OUT3	17, 18, 19	Output	Winding output. Connect to motor terminal.
OUT2	OUT4	14, 15, 16	Output	Winding output. Connect to motor terminal.
OUT1		4, 5, 6	Output	Winding output. Connect to motor terminal.
OUT2		7, 8, 9	Output	Winding output. Connect to motor terminal.
IN2		40	Input	PWM input for H-bridge 1.
IN1		41	Input	PWM input for H-bridge 1.
DECAY		37	Input	Decay setting pin.
TOFF		35	Input	PWM OFF time setting pin.
OCPM		27	Input	Determines the fault recovery method. Depending on the OCPM voltage, fault recovery can be either latch-off or auto-retry.
VCP		1	Power	Charge pump output. Connect a X7R, 1µF, 16V capacitor to VM.
VM		2, 11, 12, 21	Power	Power supply. Connect to supply voltage and bypass to PGND with two 0.01µF ceramic capacitors plus a bulk capacitor rated for VM.
GND		22, 23	Power	Device ground. Connect to system ground.
CPH		44	Power	Charge pump switching node. Connect a X7R, 0.022µF, VM rated ceramic capacitor from CPH to CPL.
CPL		43		
DVDD		24	Power	LDO output. Connect a X7R, 1µF, 10V ceramic capacitor to GND.
VCC		25	Power	Supply voltage for internal logic blocks. When no separate supply voltage is available, tie the VCC pin to the DVDD output.
nFAULT		26	Open Drain	Fault indication. Pulled logic low with fault condition; open drain output requires an external pullup resistor.
MODE1		28	Input	Selects between dual and single H-bridge modes of operation.
MODE2		29	Input	Selects the interface - between PH/EN and IN/IN.
nSLEEP		42	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode. An nSLEEP low pulse clears latched faults.
RSVD		32, 36	-	Reserved. Leave Unconnected.
PAD		-	-	Thermal pad.

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). [1] [2]

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	70	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 5.75	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
External logic supply (VCC)	-0.3	5.75	V
IPROPI pin voltage (IPROPI)	-0.3	DVDD + 0.3	V
Control pin voltage	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
PGNDx to GND voltage	-0.5	0.5	V
PGNDx to GND voltage, < 1 µs	-2.5	2.5	V
Continuous OUTx pin voltage	–1	V_{VM} + 1	V
Transient 100 ns OUTx pin voltage	–3	V_{VM} + 3	V
Peak drive current	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 [1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	60	V
V_I	Logic level input voltage	0	5.5	V
V_{VCC}	VCC pin voltage	3.05	5.5	V
V_{REF}	Reference voltage (VREF)	0.05	3.3	V
$I_{RMS,DUAL}$	RMS current, dual H-bridge mode	0	5	A
$I_{RMS.SINGLE}$	RMS current, single H-bridge mode	0	10	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC		DDW	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

5.4.1 Transient Thermal Impedance & Current Capability

Information based on thermal simulations

表 5-1. Transient Thermal Impedance ($R_{\theta JA}$) and Current Capability

$R_{\theta JA}$ [°C/W](1)				Configuration	Current (A)(2)					
					without PWM(3)				with PWM(4)	
0.1 sec	1 sec	10 sec	DC		0.1 sec	1 sec	10 sec	DC	10 sec	DC
1.8	4.7	8.4	23.3	Dual H-Bridge (both outputs loaded with same current)	8	5.7	4.2	2.5	4	2.2
				Dual H-Bridge (only one output loaded)	8	8	6	3.5	5.4	3
				Single H-Bridge	16	11.3	8.4	4.9	7.9	4.4

(1) Simulated using 114.3 mm x 76.2 mm x 1.6 mm 4 layer PCB – 2 oz Cu on top and bottom layers, 1 oz Cu on internal planes, 16 cm^2 top and bottom layer Cu area, with 13 x 5 thermal via array below thermal pad, 1.1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating.
(2) Estimated transient current capability at 85 °C ambient temperature for junction temperature rise up to 150°C.
(3) Only conduction losses (I^2R) and quiescent current loss at 48 V supply voltage are considered. Maximum ON resistance values at 150°C as per Electrical Characteristics table are considered to calculate conduction losses.
(4) Switching loss estimated by the equation: $P_{SW} = V_{VM} \times I_{Load} \times f_{PWM} \times t_{RF}$, where V_{VM} = 48 V, f_{PWM} = 20 KHz, t_{RF} = 110 ns

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5.5 Electrical Characteristics

Typical values are at T_A = 25°C. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No load, VCC = External 5V		5	8	mA
		nSLEEP = 1, No motor load, VCC = DVDD		8.5	13	
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		3	8	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.75	1	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.3	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 60 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5 V	4.3	4.45		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 60 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (IN1, IN2, IN3, IN4, OCPM, MODE1, MODE2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
V_{HYS_nSLEEP}	nSLEEP logic hysteresis			300		mV
I_{IL}	Input logic-low current (except MODE2)	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current (except MODE2)	V_{IN} = 5 V			50	µA
R_{PU}	MODE2 internal pull-up resistor			220		kΩ
t_{PDH} [1]	INx high to OUTx high propagation delay			600		ns
t_{PDL} [1]	INx low to OUTx low propagation delay			600		ns
TRI-LEVEL INPUTS (DECAY)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I3}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10.5		µA
QUAD-LEVEL INPUTS (TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V

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Typical values are at T_A = 25°C. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10.5		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.3	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2, OUT3, OUT4)						
$R_{DS(ONH\_DUAL)}$	Dual H-bridge, High-side FET on resistance	T_J = 25 °C, I_O = -5 A		50	60	mΩ
		T_J = 125 °C, I_O = -5 A		75	94	mΩ
		T_J = 150 °C, I_O = -5 A		85	107	mΩ
$R_{DS(ONL\_DUAL)}$	Dual H-bridge, Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		50	60	mΩ
		T_J = 125 °C, I_O = 5 A		72	90	mΩ
		T_J = 150 °C, I_O = 5 A		80	100	mΩ
$R_{DS(ONH\_SINGLE)}$	Single H-bridge, High-side FET on resistance	T_J = 25 °C, I_O = -5 A		25	30	mΩ
		T_J = 125 °C, I_O = -5 A		38	47	mΩ
		T_J = 150 °C, I_O = -5 A		43	54	mΩ
$R_{DS(ONL\_SINGLE)}$	Single H-bridge, Low-side FET on resistance	T_J = 25 °C, I_O = 5 A		25	30	mΩ
		T_J = 125 °C, I_O = 5 A		36	45	mΩ
		T_J = 150 °C, I_O = 5 A		40	50	mΩ
I_{LEAK}	Output leakage current to GND	Sleep-mode, H-bridges are Hi-Z, V_{VM} = 60 V			300	µA
t_{RF}	Output rise/fall time	I_O = 5 A, between 10% and 90%		110		ns
t_D	Output dead time	VM = 24V, I_O = 5 A		300		ns
CURRENT SENSE AND REGULATION (IPROPI, VREF)						
A_{IPROPI}	Current mirror gain			212		µA/A
A_{ERR}	Current mirror scaling error	10% to 20% rated current	-12		12	%
		20% to 40% rated current	-7		7	
		40% to 100% rated current	-4		4	
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			30	nA
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
t_{DEG}	Current regulation deglitch time			0.5		µs
t_{BLK}	Current Regulation Blanking time			1.5		µs
PROTECTION CIRCUITS						

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Typical values are at T_A = 25°C. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	VM UVLO lockout	VM falling	4.1	4.25	4.35	V
		VM rising	4.2	4.35	4.45	
VCC_{UVLO}	VCC UVLO lockout	VCC falling	2.7	2.8	2.9	V
		VCC rising	2.8	2.9	3.05	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Dual H-bridge, Current through any FET	8			A
		Single H-bridge, Current through any FET	16			A
t_{OCP}	Overcurrent detection delay			2.1		µs
t_{RETRY}	Overcurrent retry time			4.1		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

(1) Guaranteed by design.

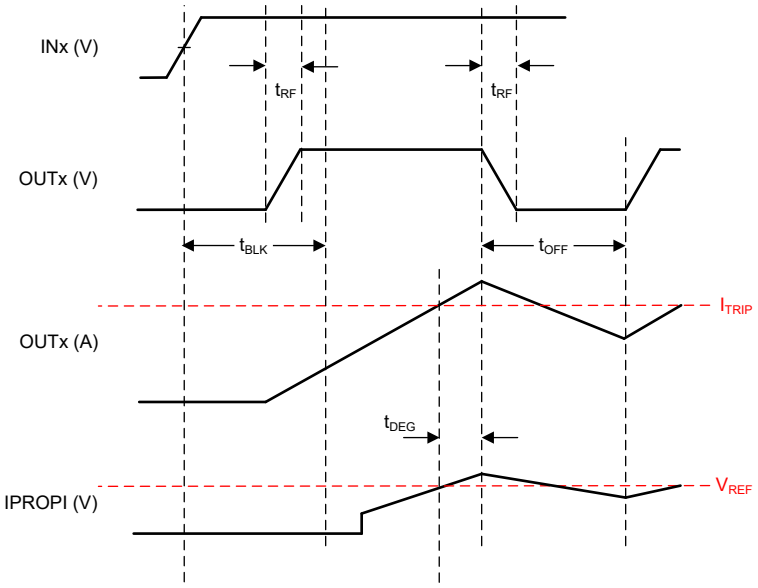

図 5-1. IPROPI Timing Diagram

5.6 Typical Characteristics

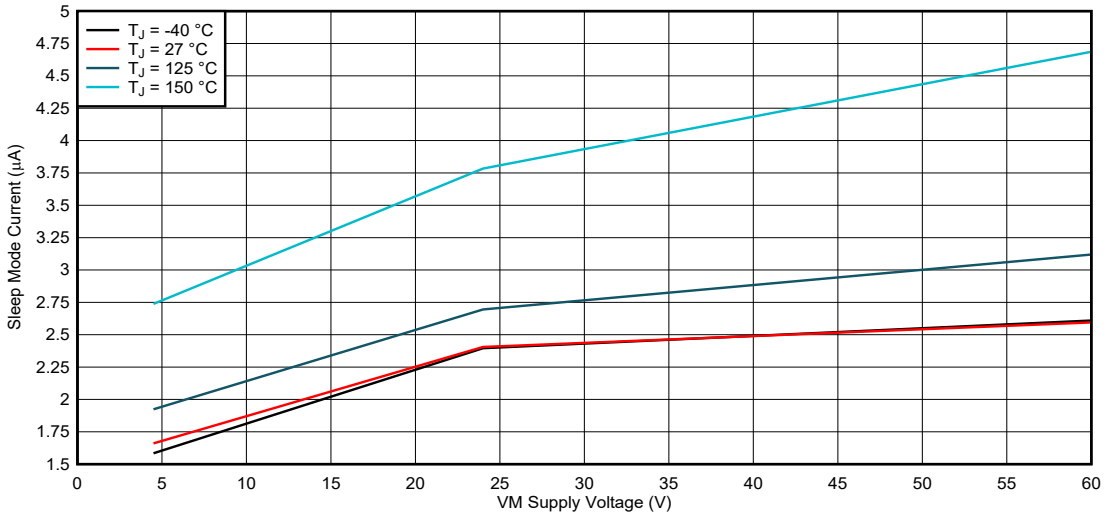

図 5-2. Sleep Mode Supply Current

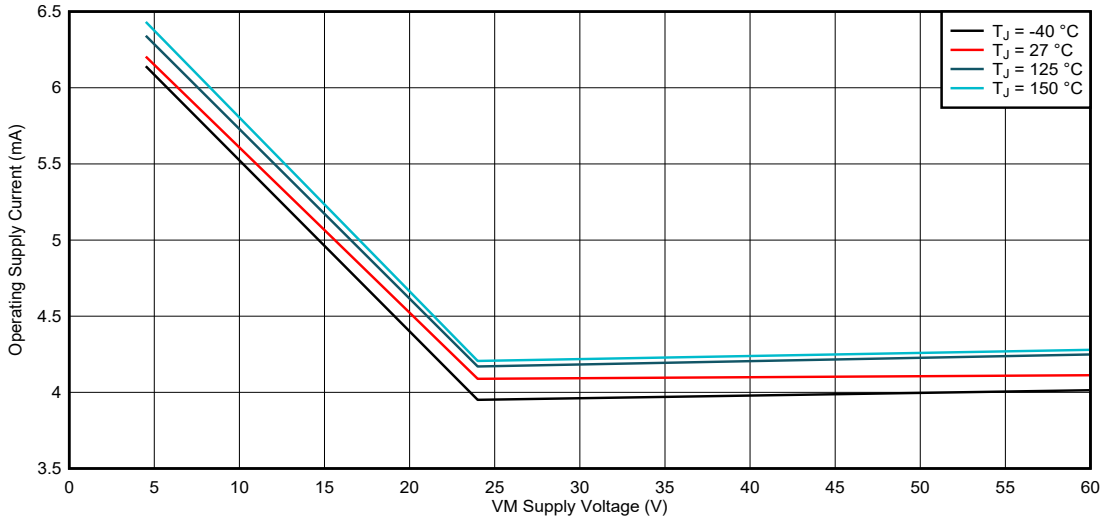

図 5-3. Operating Supply Current, VCC = External 5 V

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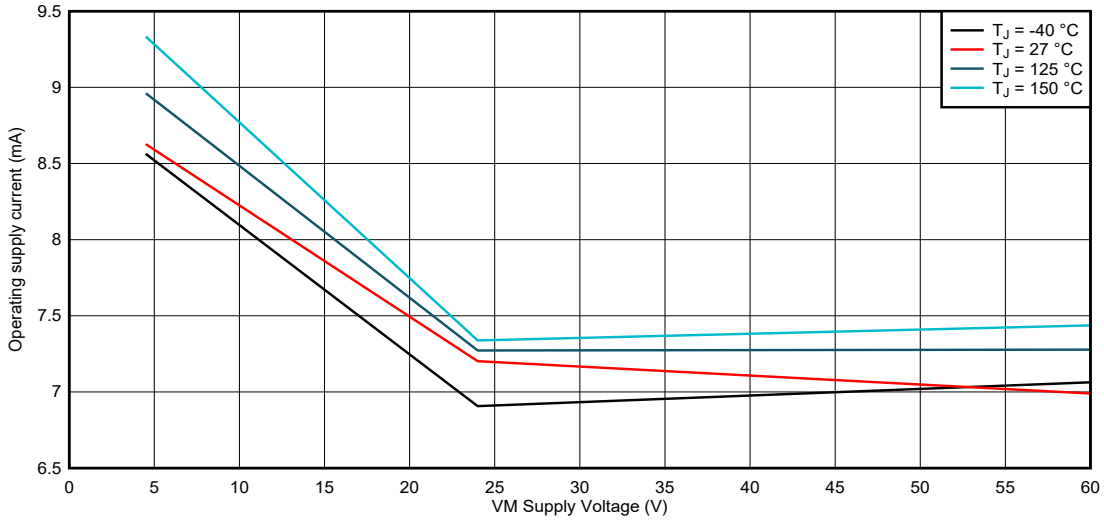

図 5-4. Operating Supply Current, VCC = DVDD

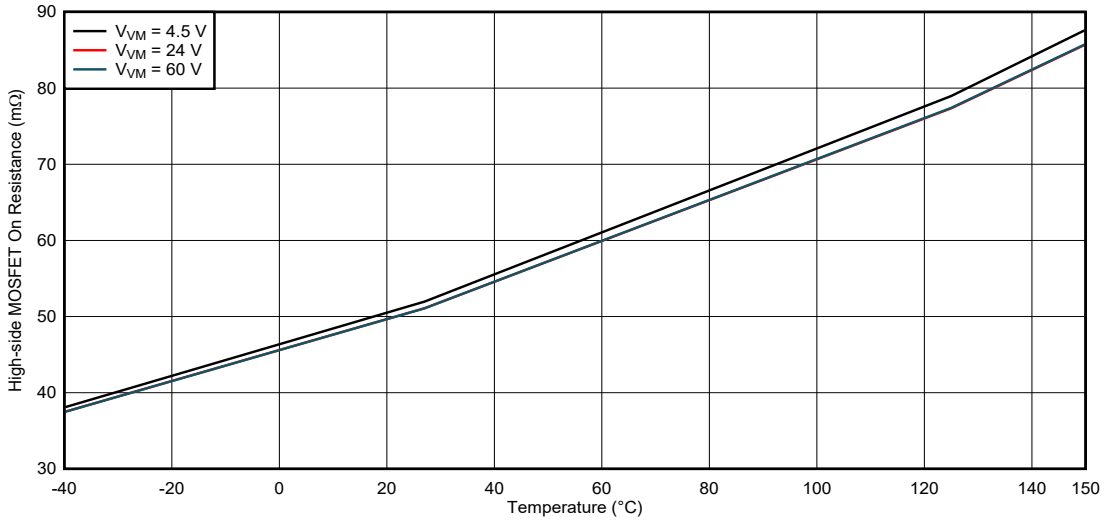

図 5-5. High-side FET on Resistance, Dual H-bridge Mode

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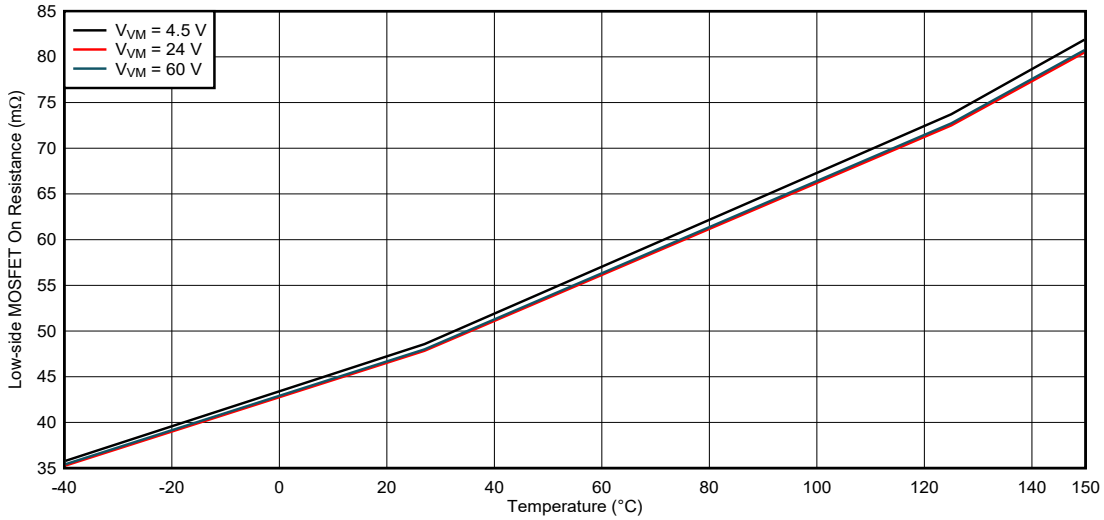

図 5-6. Low-side FET on Resistance, Dual H-bridge Mode

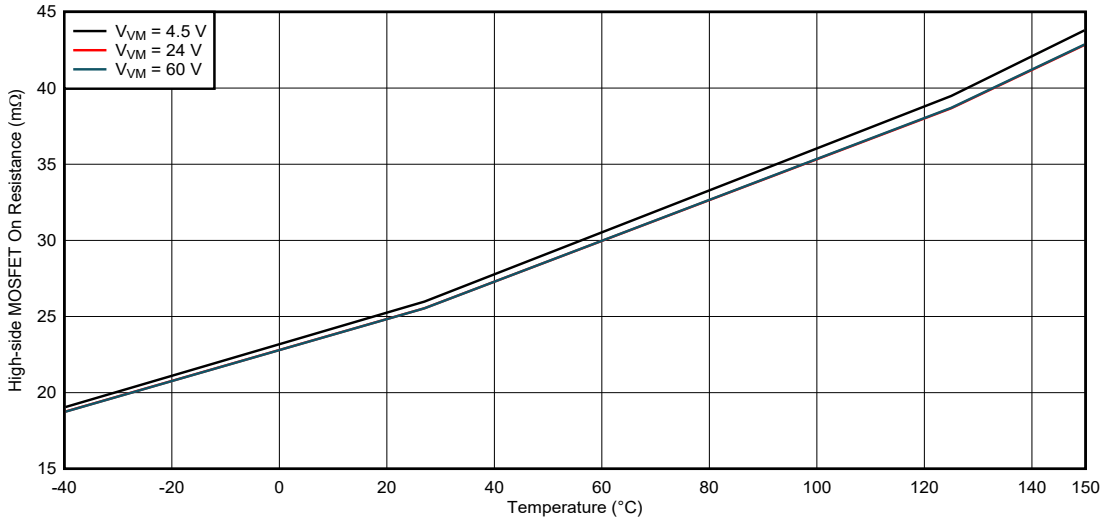

図 5-7. High-side FET on Resistance, Single H-bridge Mode

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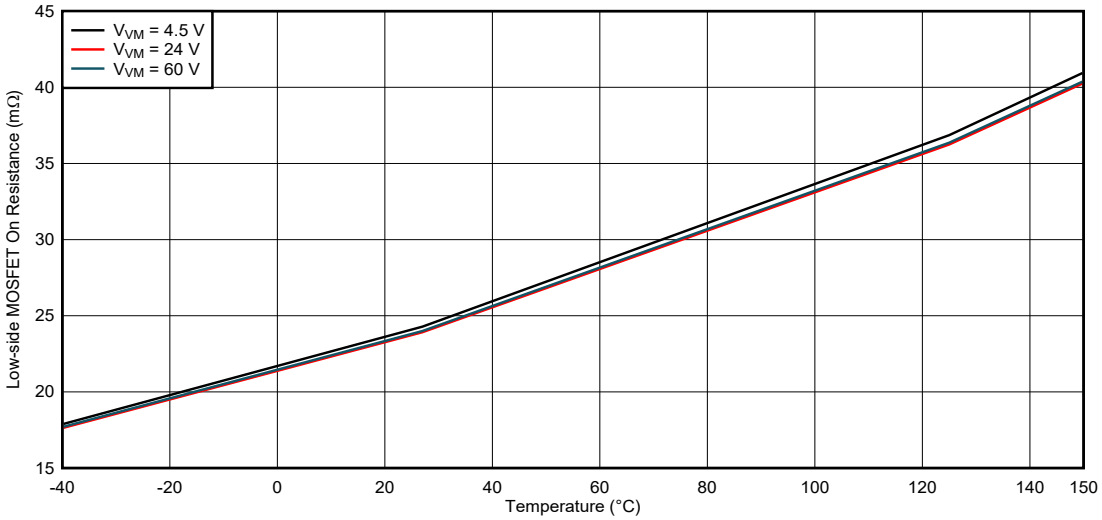

図 5-8. Low-side FET on Resistance, Single H-bridge Mode

6 Detailed Description

6.1 Overview

The DRV8262-Q1 is a H-Bridge motor driver that operates from 4.5V to 60V and supports up to 16A peak motor currents for various types of motors and loads. The device integrates two H-bridge output power stages to drive two brushed-DC motors. The H-bridges can be paralleled to provide a higher current to a single brushed-DC motor. The number of H-bridges and the interface of operation are selected by the MODE1 and MODE2 pin settings.

The device integrates a charge pump to efficiently drive high-side N-channel MOSFETs with 100% duty cycle. The device can operate from a single power supply input (VM). Alternatively, the VCC pin can be connected to a second power supply to provide power to the internal logic blocks. The nSLEEP pin provides an ultra-low power mode to minimize current drawn during system inactivity.

The device is available in a 44-pin HTSSOP (DDW) package with an exposed pad. In the dual H-bridge mode, the DDW package delivers up to 8A peak current per output. In single H-bridge mode, the DDW package delivers up to 16A peak current. The actual current that can be delivered depends on the ambient temperature, supply voltage, and PCB thermal design.

The device integrates current sense outputs. The IPROPI pins source a small current that is proportional to the current in the high-side MOSFETs. The current from the IPROPI pins can be converted to a proportional voltage using an external resistor (R_{IPROPI}). The integrated current sensing allows the DRV8262-Q1 to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect changes in load or stall conditions. The sensing accuracy of the IPROPI output is ± 4% for 40% to 100% of the rated current. External power sense resistors can also be connected if higher accuracy sensing is required. The current regulation level can be configured during operation through the VREF pin to limit the load current according to the system's demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), over current protection (OCP), and over temperature shutdown (OTSD). Fault conditions are indicated on the nFAULT pin.

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6.2 Functional Block Diagram

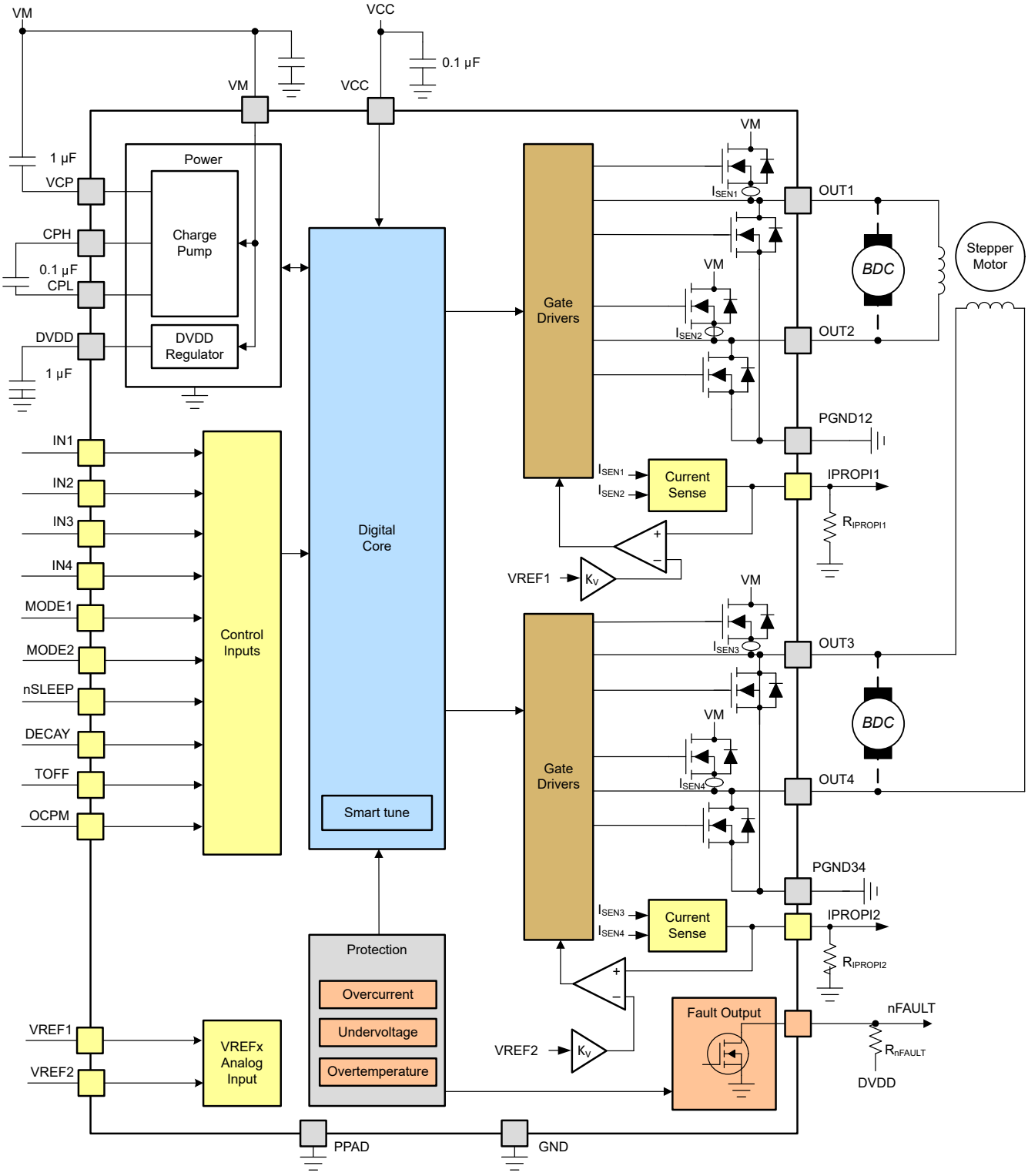

図 6-1. Dual H-Bridge Block Diagram

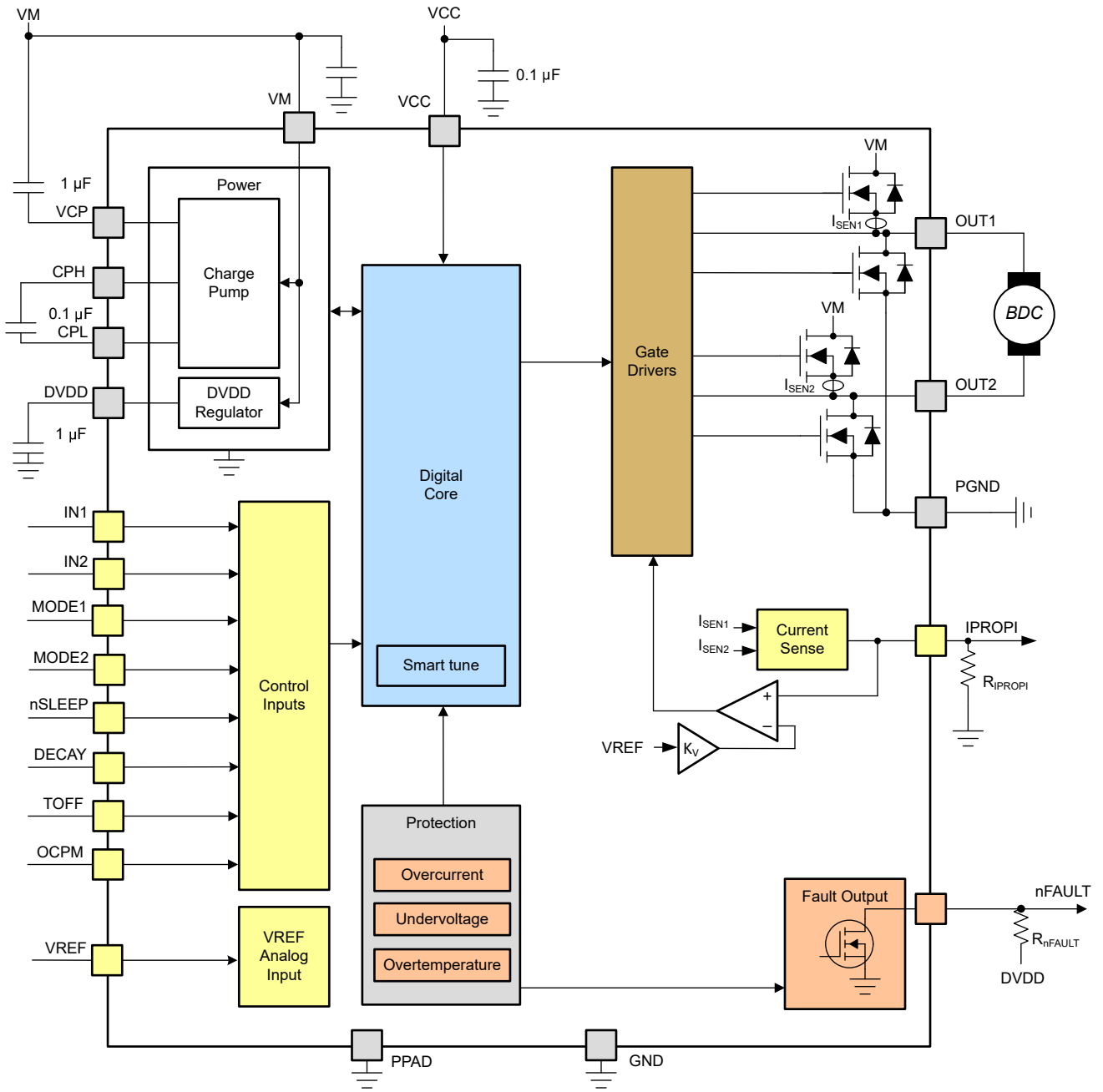

図 6-2. Single H-Bridge Block Diagram

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6.3 Feature Description

The following table shows the recommended values of the external components for the driver.

表 6-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND12	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM	PGND34	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM3}	VM	PGND12	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 1-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.1-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 1-µF, 10-V rated ceramic capacitor
C_{VCC}	VCC	GND	X7R, 0.1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	DVDD or VCC	nFAULT	10-kΩ resistor
R_{REF1}	VREFx	DVDD	Resistor to set current regulation threshold.
R_{REF2}	VREFx	GND	
$R_{IPROPIx}$	IPROPIx	GND	For details, see セクション 6.5.2

6.4 Device Operational Modes

The DRV8262-Q1 supports dual or single H-bridge with PH/EN or PWM interface. The mode of operation is selected by the MODE1 and MODE2 pins as shown in 表 6-2.

- The MODE1 and MODE2 pin states are latched when the device is enabled through the nSLEEP pin or at power-up.
- The MODE2 pin has to be grounded to select PH/EN interface.
- To select PWM interface, keep MODE2 pin floating or connect the MODE2 pin to DVDD.

表 6-2. Modes of Operation

MODE1	MODE2	Dual or Single H-bridge	Interface
0	0	Dual	PH/EN
	Floating or DVDD	Dual	PWM
1	0	Single	PH/EN
	Floating or DVDD	Single	PWM

The INx inputs can be set to static voltages for 100% duty cycle drive, or the INx inputs can be pulse-width modulated for variable motor speed. The input pins can be powered before VM supply is applied.

セクション 6.4.1 and セクション 6.4.2 show the truth tables for each interface. Note that the tables do not take into account the internal current regulation feature. Additionally, the DRV8262-Q1 automatically handles the dead time generation when switching between the high-side and low-side MOSFETs of a H-bridge.

6.4.1 Dual H-Bridge Mode (MODE1 = 0)

- If the MODE1 pin is logic low at power up, the device is latched into dual H-bridge mode.
  - Two brushed-DC motors or a stepper motor can be driven in this mode.
- The MODE2 pin configures the interface of operation between PH/EN and PWM.
  - PH/EN mode allows the H-bridge to be controlled with a speed and direction type of interface.
  - PWM interface allows the H-bridge outputs to become Hi-Z without making the nSLEEP pin logic low.

The truth tables for dual H-bridge mode are shown in 表 6-3 and 表 6-4.

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表 6-3. Dual H-Bridge with PH/EN Interface

nSLEEP	IN1/IN3	IN2/IN4	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	X	H	H	Brake (High-Side Slow Decay)
1	1	0	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	1	H	L	Forward (OUT1/3 -> OUT2/4)

表 6-4. Dual H-Bridge with PWM Interface

nSLEEP	IN1/IN3	IN2/IN4	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	0	Hi-Z	Hi-Z	Coast (H-Bridge outputs Hi-Z)
1	0	1	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	0	H	L	Forward (OUT1/3 -> OUT2/4)
1	1	1	H	H	Brake (High-Side Slow Decay)

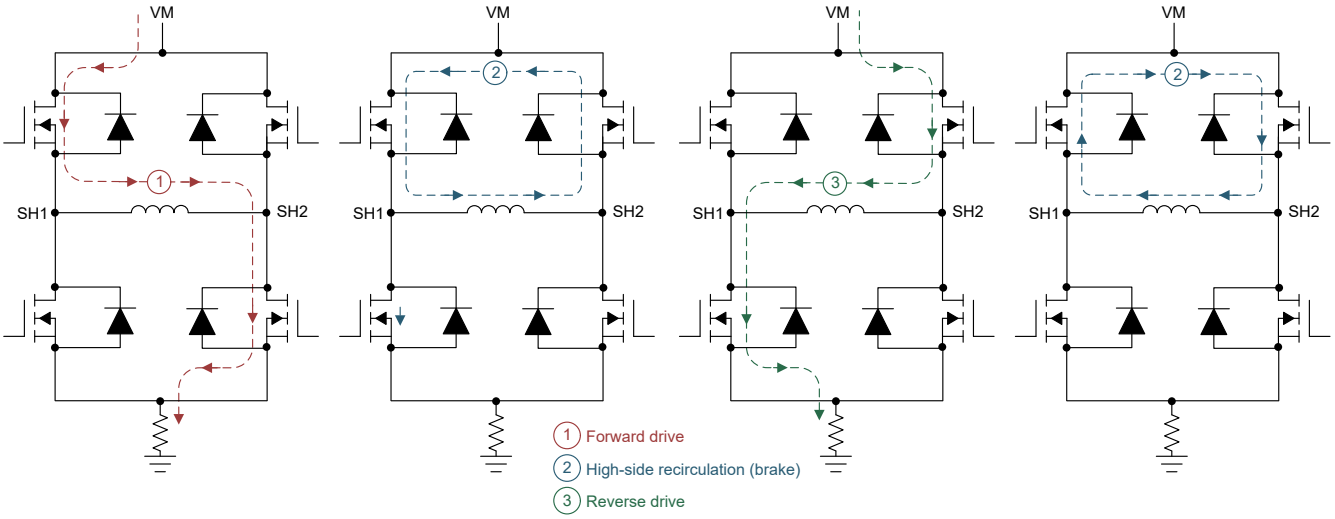

図 6-3. Current Paths

6.4.2 Single H-Bridge Mode (MODE1 = 1)

When the MODE1 pin is logic High on power up, the device is latched into single H-bridge mode. The device drives one brushed-DC motor in this mode. The truth table for single H-bridge mode is shown in 表 6-5 and 表 6-6.

表 6-5. Single H-Bridge with PH/EN Interface

nSLEEP	IN1	IN2	OUT1/3	OUT2/4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	X	H	H	Brake (High-Side Slow Decay)
1	1	0	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	1	H	L	Forward (OUT1/3 -> OUT2/4)

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表 6-6. Single H-Bridge with PWM Interface

nSLEEP	IN1	IN2	OUT1/OUT3	OUT2/OUT4	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep
1	0	0	Hi-Z	Hi-Z	Coast (H-bridge outputs Hi-Z)
1	0	1	L	H	Reverse (OUT2/4 -> OUT1/3)
1	1	0	H	L	Forward (OUT1/3 -> OUT2/4)
1	1	1	H	H	Brake (High-Side Slow Decay)

6.5 Current Sensing and Regulation

The device integrates current sensing across high-side MOSFETs, current regulation, and current sense feedback. These features allow the device to sense the motor current without an external sense resistor or current sense circuitry; reducing system size, cost, and complexity. This also allows the device to limit the motor current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through IPROPI outputs.

6.5.1 Current Sensing and Feedback

The device supports one IPROPI output when operating in the single H-bridge mode, and two IPROPI outputs when operating in the dual H-bridge mode.

The IPROPI pins output a current that is proportional to the current flowing in the high-side FETs of the H-bridge, scaled by the current mirror gain A_{IPROPI}. The IPROPI output current can be calculated by 式 1. The I_{HS1} and I_{HS2} in 式 1 are only valid when the current flows from drain to source in the high-side MOSFET. If current flows from source to drain, the value of I_{HS1} and I_{HS2} for that channel is zero. Because of this, the IPROPI pin does not represent the current when operating in a fast decay mode (coast mode) or low-side slow decay mode. The IPROPI pin represents the H-bridge current under forward drive, reverse drive, and high-side slow decay, thereby allowing for continuous current monitoring in typical brushed DC motor applications.

Even in coast mode, the current can be sampled by briefly re-enabling the driver in either drive or slow-decay modes and measuring the current before switching back to coast mode again.

$$I_{PROPI} = (I_{HS1} + I_{HS2}) \times A_{IPROPI} \quad (1)$$

Each IPROPI pin should be connected to an external resistor (R_{IPROPI}) to ground in order to generate a proportional voltage (V_{IPROPI}) on the IPROPI pin with the I_{IPROPI} analog current output. This allows for the load current to be measured as the voltage drop across the R_{IPROPI} resistor with a standard analog to digital converter (ADC). The R_{IPROPI} resistor can be sized based on the expected load current in the application so that the full range of the controller ADC is utilized. The device implements an internal clamp circuit to limit V_{IPROPI} with respect to V_{VREF} on the VREF pin and protect the external ADC in case of output overcurrent or unexpected high current events.

The corresponding IPROPI voltage to the output current can be calculated by 式 2.

$$V_{IPROPI}\ (V) = I_{PROPI}\ (A) \times R_{IPROPI}\ (\Omega) \quad (2)$$

The IPROPI voltage should be less than the maximum recommended value of VREF, which is 3.3V. For the R_{IPROPI} resistor, 10%, 5%, 1% and 0.1% are all valid tolerance values. The typical recommendation is 1% for best trade off between performance and cost.

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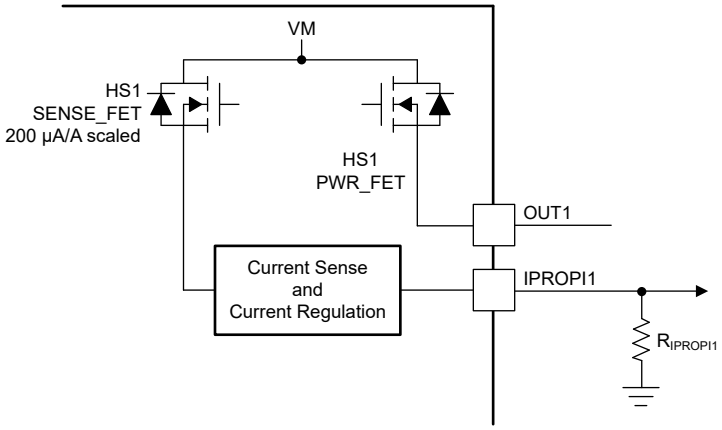

図 6-4. Integrated Current Sensing

The A_{ERR} parameter in the Electrical Characteristics table is the error of the A_{IPROPI} gain. It indicates the combined effect of offset error added to the I_{OUT} current and gain error.

6.5.2 Current Regulation

The current chopping threshold (I_{TRIP}) is set through a combination of the VREF voltage (V_{VREF}) and IPROPI output resistor (R_{IPROPI}). This is done by comparing the voltage drop across the external R_{IPROPI} resistor to V_{VREF} with an internal comparator.

$$I_{TRIP} \times A_{IPROPI} = V_{VREF}\ (V) / R_{IPROPI}\ (\Omega) \quad (3)$$

For example, in the dual H-bridge mode, to set I_{TRIP} at 5 A with V_{VREF} at 3.3V, R_{IPROPI} has to be -

$R_{IPROPI} = V_{VREF} / (I_{TRIP} \times A_{IPROPI}) = 3.3 / (5 \times 212 \times 10^{-6}) = 3.09k\Omega$

In the single H-bridge mode, connect the two IPROPI pins. In the dual H-bridge mode, there are two VREF pins, which allows setting separate current chopping thresholds for each brushed-DC motor.

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND (if current feedback is not required). If current feedback is required and current regulation is not required, set V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold.

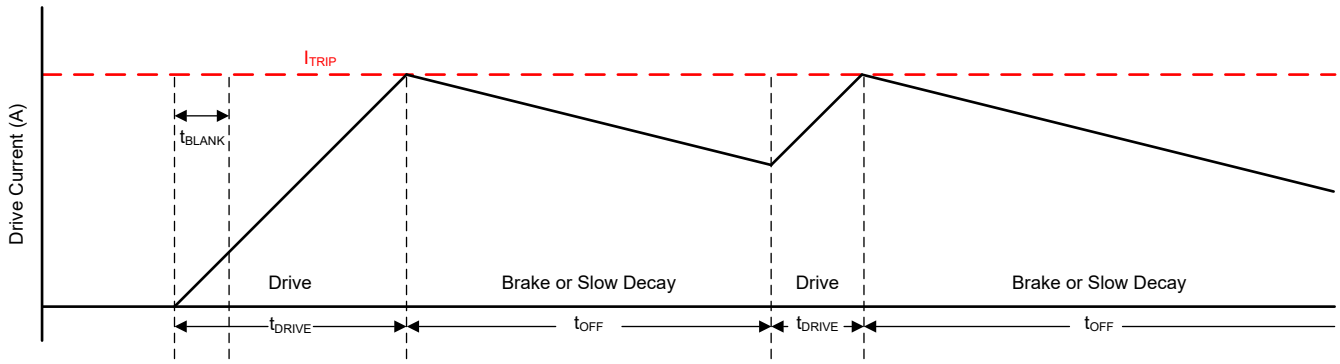

図 6-5. Current Regulation

The current through the motor windings is regulated by an adjustable off-time PWM current regulation circuit. During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached.

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When the I_{TRIP} current has been reached, for single BDC or dual BDC applications, with the DECAY pin grounded, the device enforces slow current decay by enabling both the high-side FETs for a time of t_{OFF}, programmed by the TOFF pin.

When the t_{OFF} time has elapsed and the current level falls below the current regulation (I_{TRIP}) level, the output is re-enabled according to the inputs. If, after the t_{OFF} time has elapsed, the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration. This "double t_{OFF}" time continues until the current is less than I_{TRIP} at the end of t_{OFF} time.

In current regulation, the inputs can be toggled to drive the load in the opposite direction to decay the current faster. For example, if the load was in forward drive before entering the current regulation it can only go into reverse drive when the driver enforces current regulation.

For single or dual-BDC applications, the DECAY pin should be kept grounded for high-side slow decay during t_{OFF}. For stepper applications, DECAY pin voltage should be according to the desired decay mode. The decay mode is selected by the DECAY pin as shown in 表 6-7.

表 6-7. Decay Mode Settings

DECAY	DECAY MODE
0	Slow decay (brake or high-side re-circulation)
1	Smart tune dynamic decay
Hi-Z	Mixed decay: 30% fast

If the state of the INx control pin inputs changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs. This is shown in 図 6-6.

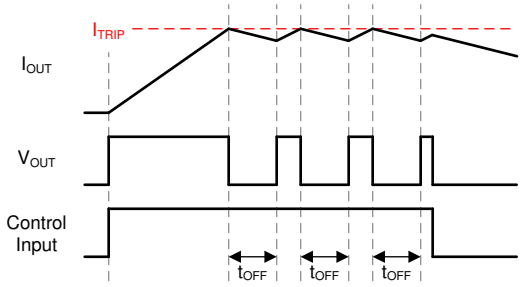

図 6-6. Current Regulation

As shown in 表 6-8, the TOFF pin configures the PWM OFF time. The OFF time settings can be changed on the fly.

表 6-8. Off-Time Settings

TOFF	OFF-TIME (t_{OFF})
0	7µs
1	16µs
Hi-Z	24µs
330 kΩ to GND	32µs

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6.5.2.1 Mixed Decay

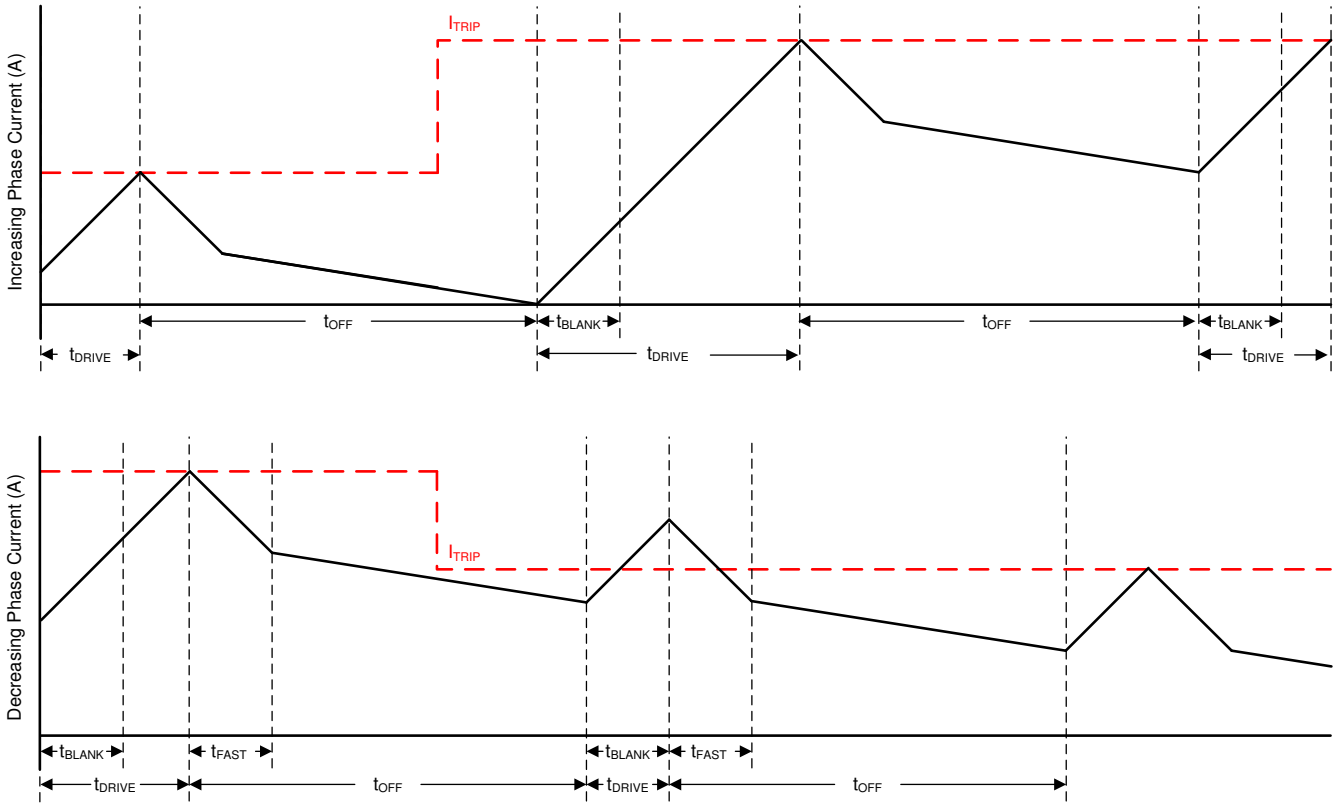

図 6-7. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

6.5.2.2 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

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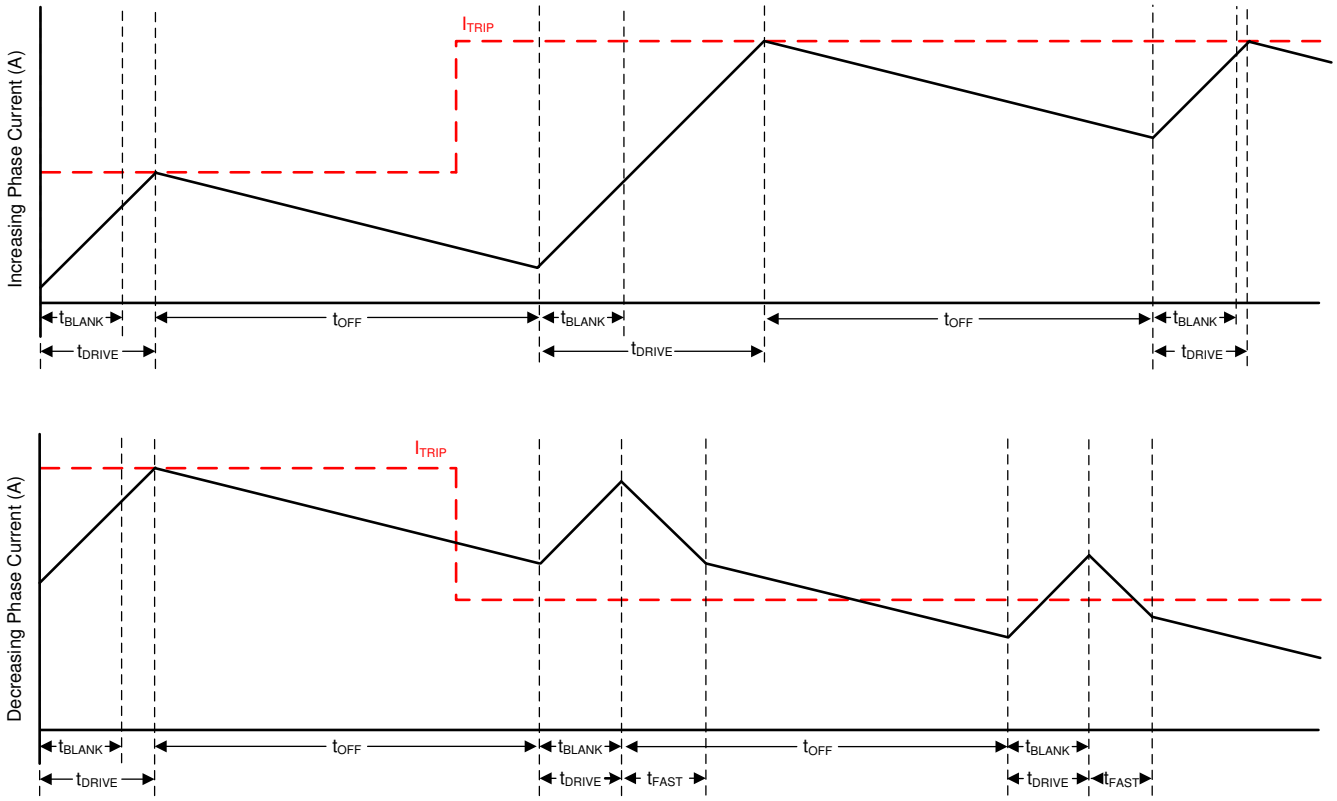

図 6-8. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

6.5.3 Current Sensing with External Resistor

The IPROPI output accuracy is ±4% for 40% to 100% of rated current. If more accurate current sensing is desired, external sense resistors can also be used between the PGND pins and the system ground to sense the load currents, as shown below.

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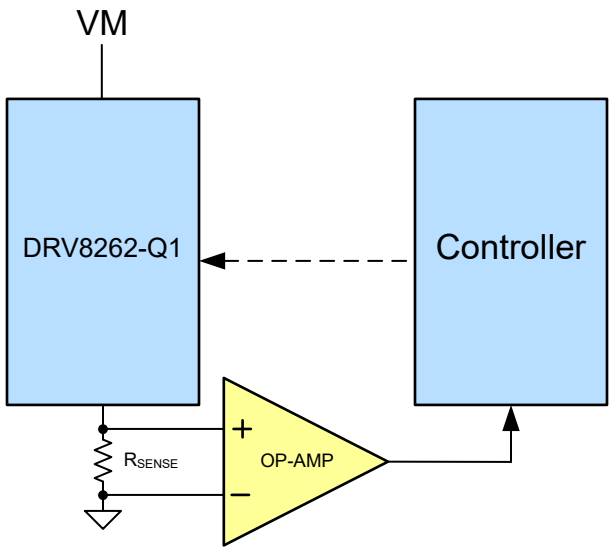

図 6-9. Current Sensing with External Resistor

The voltage drop across the external sense resistor should not exceed 300mV.

Place the sense resistors as close as possible to the corresponding IC pins. Use a symmetrical sense resistor layout to ensure good matching. Low-inductance sense resistors should be used to prevent voltage spikes and ringing. For optimal performance, the sense resistor should be a surface-mount resistor rated for high enough power. Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel. This distributes the current and heat dissipation.

6.6 Charge Pump

A charge pump is integrated to supply the high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

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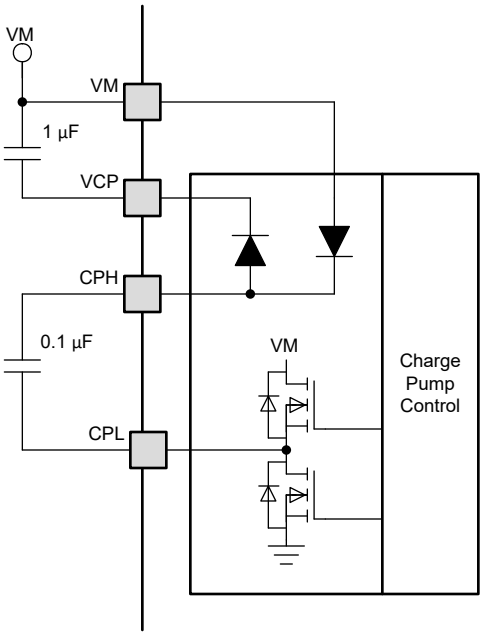

図 6-10. Charge Pump Block Diagram

6.7 Linear Voltage Regulator

A linear voltage regulator is integrated in the device. When the VCC pin is connected to DVDD, the DVDD regulator provides power to the low-side gate driver and all the internal circuits. For proper operation, bypass the DVDD pin to GND using a 1µF ceramic capacitor. The DVDD output is nominally 5V.

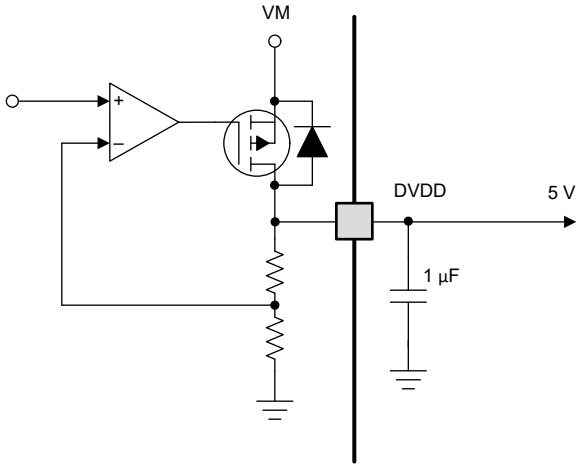

図 6-11. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

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6.8 VCC Voltage Supply

An external voltage can be applied to the VCC pin to power the internal logic circuitry. The voltage on the VCC pin should be between 3.05V and 5.5V and should be well regulated. When an external supply is not available, VCC must be connected to the DVDD pin of the device.

When powered by the VCC, the internal logic blocks do not consume power from the VM supply rail - thereby reducing the power loss in the DRV8262-Q1. This is beneficial in high voltage applications, and when ambient temperature is high. Bypass the VCC pin to ground using a 0.1µF ceramic capacitor.

6.9 Logic Level, Tri-Level and Quad-Level Pin Diagrams

図 6-12 shows the input structure for DECAY pin.

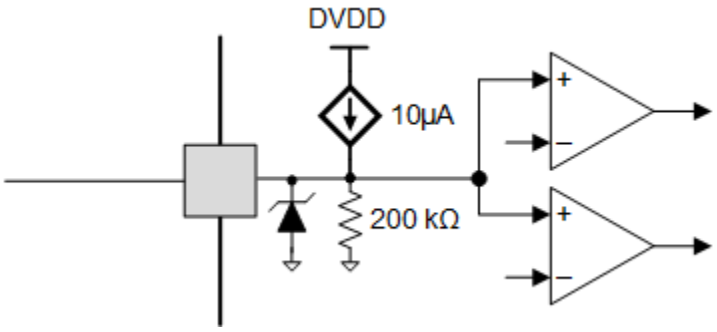

図 6-12. Tri-Level Input Pin Diagram

図 6-13 shows the input structure for TOFF pin.

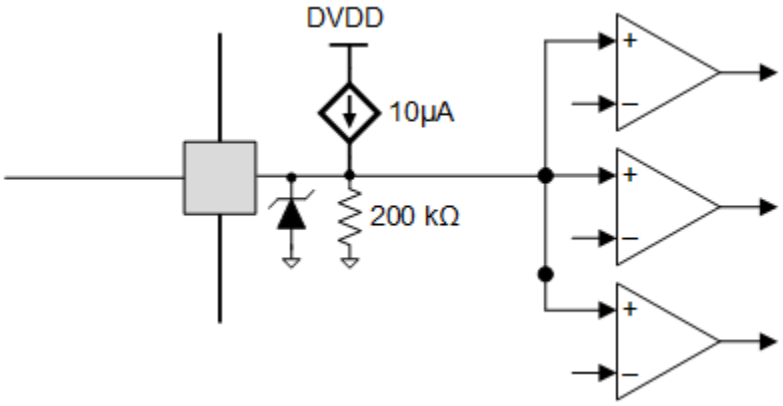

図 6-13. Quad-Level Input Pin Diagram

図 6-14 shows the input structure for IN1, IN2, IN3, IN4, MODE1, MODE2, OCPM and nSLEEP pins.

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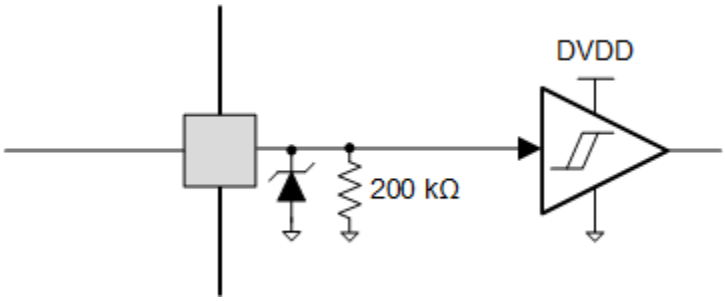

図 6-14. Logic-Level Input Pin Diagram

6.10 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

6.10.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO threshold voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump is disabled

Normal operation resumes (driver operation and nFAULT released) when the VM voltage recovers above the UVLO rising threshold voltage.

If the VM voltage falls below the internal digital reset voltage (3.9V maximum), then the internal logic circuits are disabled and the pull-down on nFAULT is also disabled. So, when VM drops below about 3.9V, nFAULT is pulled high again.

6.10.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage:

- All the outputs are disabled (High-Z)
- nFAULT pin is driven low
- The charge pump remains active

Normal operation resumes (driver operation and nFAULT released) when the VCP undervoltage condition is removed.

6.10.3 Logic Supply Power on Reset (POR)

If at any time the voltage on the VCC pin falls below the VCC_{UVLO} threshold:

- All the outputs are disabled (High-Z)
- Charge pump is disabled

VCC UVLO is not reported on the nFAULT pin. Normal motor-driver operation resumes when the VCC undervoltage condition is removed.

6.10.4 Overcurrent Protection (OCP)

Analog current-limit circuit on each MOSFET limits the current through that MOSFET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, an overcurrent fault is detected.

- The H-bridge will be disabled. For Dual H-bridge mode, only the H-bridge experiencing the overcurrent will be disabled.
- nFAULT is driven low

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- Charge pump remains active

Overcurrent conditions on both high and low side MOSFETs; meaning a short to ground or short to supply will result in an overcurrent fault detection.

Once the overcurrent condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically (driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

6.10.5 Thermal Shutdown (OTSD)

Thermal shutdown is detected if the die temperature exceeds the thermal shutdown limit (T_{OTSD}). When thermal shutdown is detected -

- All MOSFETs are disabled
- nFAULT is driven low
- Charge pump is disabled

Once the thermal shutdown condition is removed, the recovery mechanism depends on the OCPM pin setting. OCPM pin programs either latch-off or automatic retry type recovery.

- When the OCPM pin is logic low, the device has latch-off type recovery - which means after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.
- When the OCPM pin is logic high, normal operation resumes automatically after the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

6.10.6 nFAULT Output

The nFAULT pin has an open-drain output and should be pulled up to a 5V, 3.3V, or 1.8V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3V or 1.8V pullup, an external supply must be used.

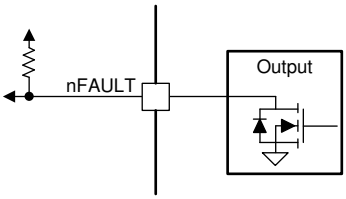

図 6-15. nFAULT Pin

6.10.7 Fault Condition Summary

表 6-9. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Reset	VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV}
Logic Supply POR	VCC < VCC_{UVLO}	-	Disabled	Disabled	Reset	VCC > VCC_{UVLO}

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表 6-9. Fault Condition Summary (続き)

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
Overcurrent (OCP)	I_{OUT} > I_{OCP}, OCPM = 0	nFAULT	Disabled	Operating	Operating	Latched: nSLEEP reset pulse
	I_{OUT} > I_{OCP}, OCPM = 1	nFAULT	Disabled	Operating	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (OTSD)	T_J > T_{TSD}, OCPM = 0	nFAULT	Disabled	Disabled	Operating	Latched: nSLEEP reset pulse
	T_J > T_{TSD}, OCPM = 1	nFAULT	Disabled	Disabled	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

6.11 Device Functional Modes

6.11.1 Sleep Mode

When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs, the DVDD regulator, SPI and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.2 Operating Mode

This mode is enabled when -

- nSLEEP is high
- VM > UVLO

The t_{WAKE} time must elapse before the device is ready for inputs.

6.11.3 nSLEEP Reset Pulse

A latched fault can be cleared by an nSLEEP reset pulse. This pulse width must be greater than 20 µs and smaller than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram below. This reset pulse does not affect the status of the charge pump or other functional blocks.

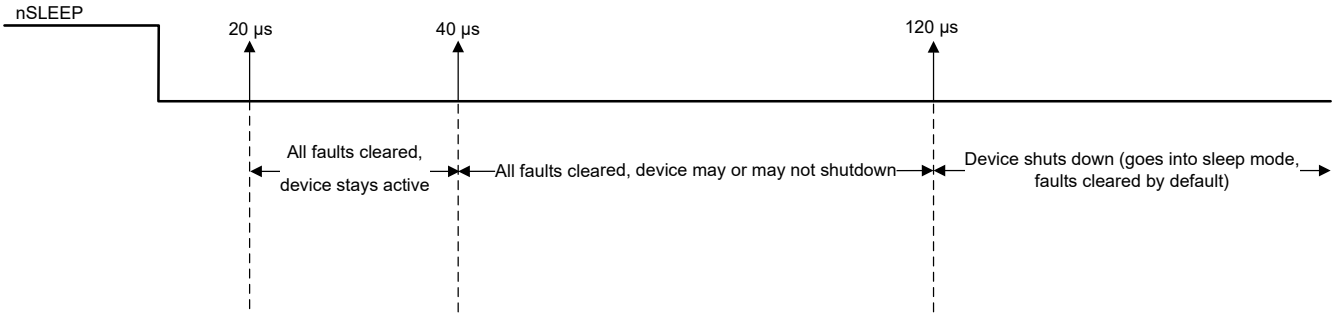

図 6-16. nSLEEP Reset Pulse

6.11.4 Functional Modes Summary

The table below lists a summary of the functional modes.

表 6-10. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 60 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled

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表 6-10. Functional Modes Summary (続き)

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Operating	4.5 V < VM < 60 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

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7 Application and Implementation

注

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7.1 Application Information

The DRV8262-Q1 can be used to drive the following types of loads -

- One or two brushed-DC motors
- One stepper motor
- One or two thermoelectric coolers (TEC)

7.1.1 Driving Brushed-DC Motors

In this application example, the device is configured to drive a bidirectional current through one or two brushed-DC motors. The H-bridge configuration, polarity, interface and duty cycle are controlled with PWM and IO resources from the external controller to the INx and MODEx pins. The current limit threshold (I_{TRIP}) is generated with a resistor divider from the VREF pin. The device is configured for the slow decay by tying the DECAY pin to ground.

7.1.1.1 Brushed-DC Motor Driver Typical Application

The following schematics show the DRV8262-Q1 driving one and two brushed-DC motors respectively.

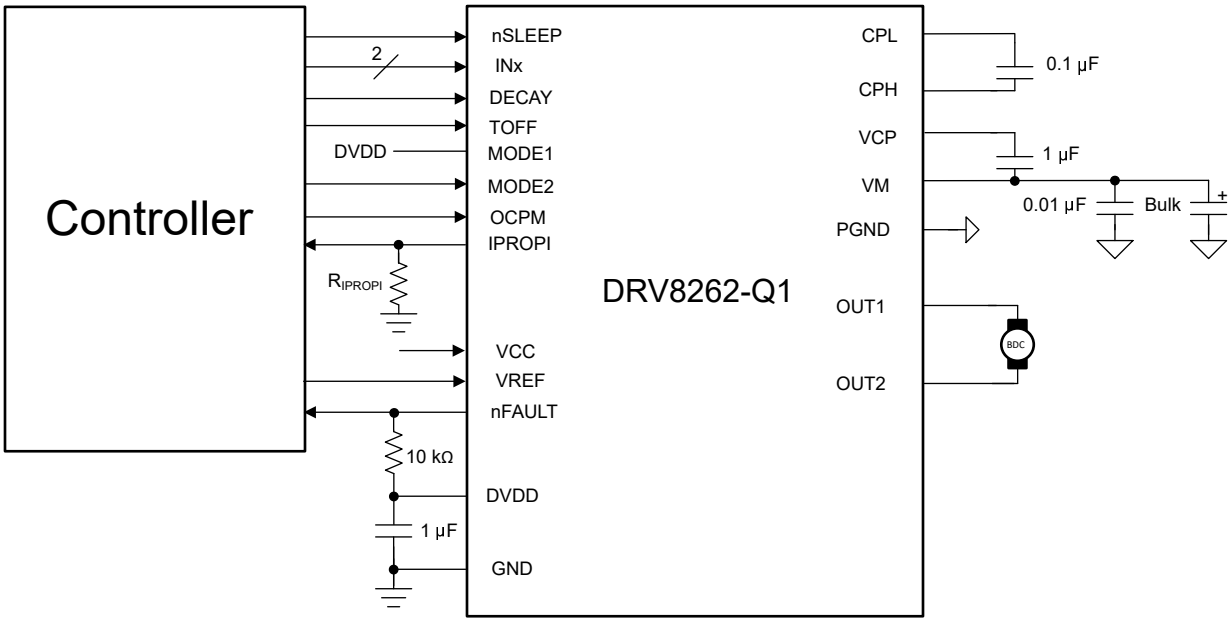

図 7-1. Driving One Brushed-DC Motor

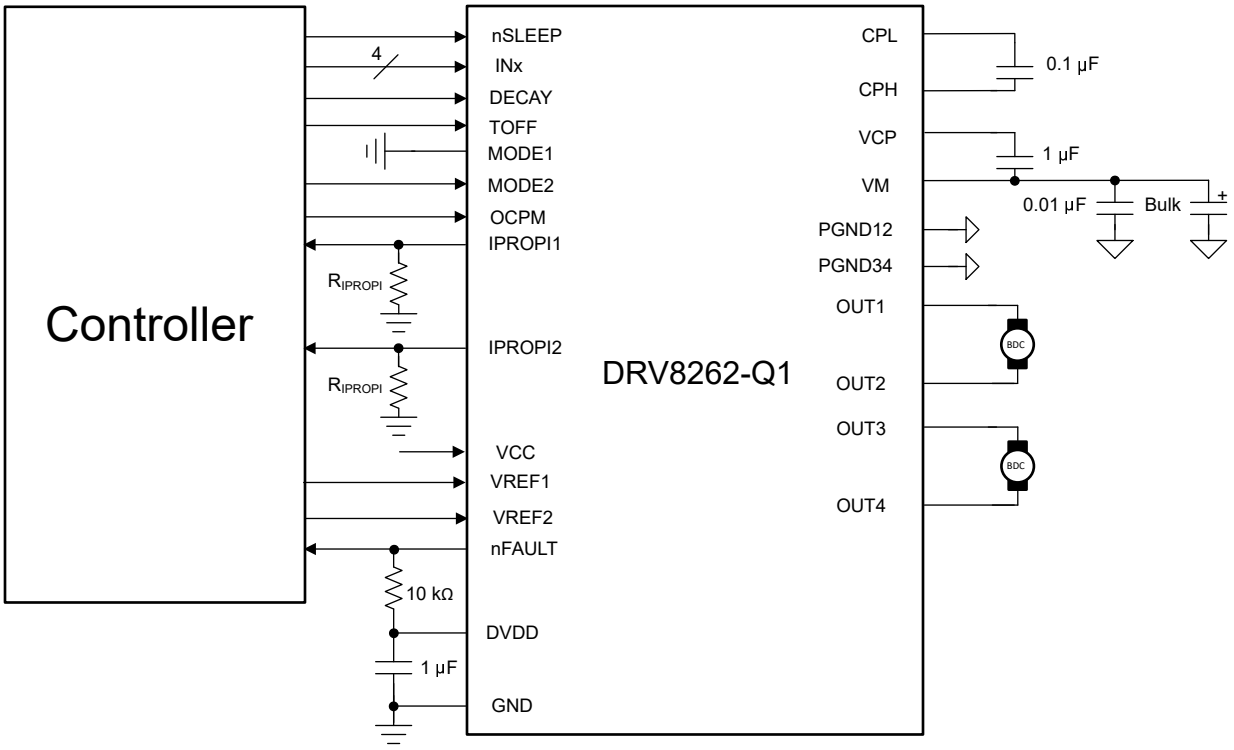

図 7-2. Driving Two Brushed-DC Motors

7.1.1.2 Power Loss Calculations - Dual H-bridge

For a H-bridge with high-side recirculation, power dissipation for each FET can be approximated as follows:

- $P_{HS1} = R_{DS(ON)} \times I_L^2$
- $P_{LS1} = 0$
- $P_{HS2} = [R_{DS(ON)} \times I_L^2 \times (1-D)] + [2 \times V_D \times I_L \times t_D \times f_{PWM}]$
- $P_{LS2} = [R_{DS(ON)} \times I_L^2 \times D] + [VM \times I_L \times t_{RF} \times f_{PWM}]$

Where,

- $R_{DS(ON)}$ = ON resistance of each FET
  - For DRV8262-Q1 in dual H-bridge mode, it is typically 50 mΩ at 25 °C, and 85 mΩ at 150 °C.
- f_{PWM} = PWM switching frequency
- VM = Supply voltage to the driver
- I_L = Motor RMS current
- D = PWM duty cycle (between 0 and 1)
- t_{RF} = Output voltage rise/ fall time
  - For DRV8262-Q1, the rise/fall time is 110 ns
- V_D = FET body diode forward bias voltage
  - For DRV8262-Q1, it is 1 V
- t_D = dead time
  - For DRV8262-Q1, it is 300 ns

For estimating power dissipation for load current flow in the reverse direction, identical equations apply, with only swapping of HS1 with HS2 and LS1 with LS2.

Substituting the following values in the equations above -

- VM = 24 V

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- I_L = 4 A
- $R_{DS(ON)}$ = 50 mΩ
- D = 0.5
- V_D = 1 V
- t_D = 300 ns
- t_{RF} = 110 ns
- f_{PWM} = 20 kHz

The losses in each FET can be calculated as follows -

P_{HS1} = 50 mΩ × 4^2 = 0.8 W

P_{LS1} = 0

P_{HS2} = [50 mΩ × 4^2 x (1-0.5)] + [2 x 1 V x 4 A x 300 ns x 20 KHz] = 0.448 W

P_{LS2} = [50 mΩ × 4^2 x 0.5] + [24 x 4 A x 110 ns x 20 kHz] = 0.611 W

Quiescent Current Loss P_Q = 24 V × 5 mA = 0.12 W

P_{TOT} = 2 x (P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2}) + P_Q = 2 x (0.8 + 0 + 0.448 + 0.611) + 0.12 = 3.84 W

7.1.1.3 Power Loss Calculations - Single H-bridge

In single H-bridge mode, on-resistance of each FET is typically 25 mΩ at 25 °C, and 43 mΩ at 150 °C.

Substituting the following values in the power loss equations -

- VM = 24 V
- I_L = 8 A
- $R_{DS(ON)}$ = 25 mΩ
- D = 0.5
- V_D = 1 V
- t_D = 300 ns
- t_{RF} = 110 ns
- f_{PWM} = 20 kHz

The losses in each FET can be calculated as follows -

P_{HS1} = 25 mΩ × 8^2 = 1.6 W

P_{LS1} = 0

P_{HS2} = [25 mΩ × 8^2 x (1-0.5)] + [2 x 1 V x 8 A x 300 ns x 20 KHz] = 0.896 W

P_{LS2} = [25 mΩ × 8^2 x 0.5] + [24 x 8 A x 110 ns x 20 kHz] = 1.223 W

Quiescent Current Loss P_Q = 24 V × 5 mA = 0.12 W

P_{TOT} = P_{HS1} + P_{LS1} + P_{HS2} + P_{LS2} + P_Q = 1.6 + 0 + 0.896 + 1.223 + 0.12 = 3.84 W

7.1.1.4 Junction Temperature Estimation

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as -

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 22.2 °C/W .

Assuming 25°C ambient temperature, the junction temperature is calculated as shown below -

$$T_J = 25°C + (3.84\ W \times 22.2\ °C/W) = 110.2\ °C \quad (4)$$

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For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature shown in the Typical Operating Characteristics section.

For example,

- At 110.2 °C junction temperature, the on-resistance will likely increase by a factor of 1.4 compared to the on-resistance at 25 °C.
- The initial estimate of conduction loss was 3.2 W.
- New estimate of conduction loss will therefore be 3.2 W x 1.4 = 4.48 W.
- New estimate of the total power loss will accordingly be 5.12 W.
- New estimate of junction temperature for the DDW package will be 138.7 °C.
- Further iterations are unlikely to increase the junction temperature estimate by significant amount.

7.1.1.5 Application Performance Plots

Traces from top to bottom: I_{OUT2}, $V_{IPROPI2}$, I_{OUT1}, $V_{IPROPI1}$, OUT2, OUT3, OUT1, OUT4

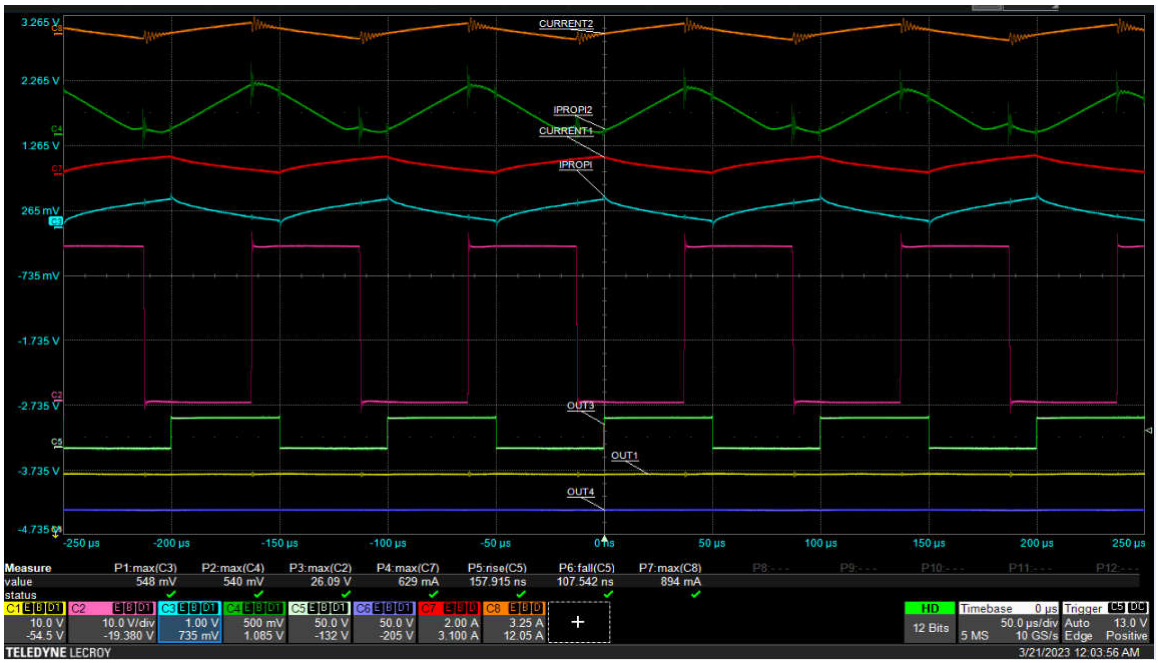

図 7-3. Dual H-bridge Operation, VM = 24 V

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7.1.2 Driving Stepper Motors

When configured in the dual H-bridge mode, the device can drive one stepper motor.

7.1.2.1 Stepper Driver Typical Application

The following schematic shows the DRV8262-Q1 driving a stepper motor.

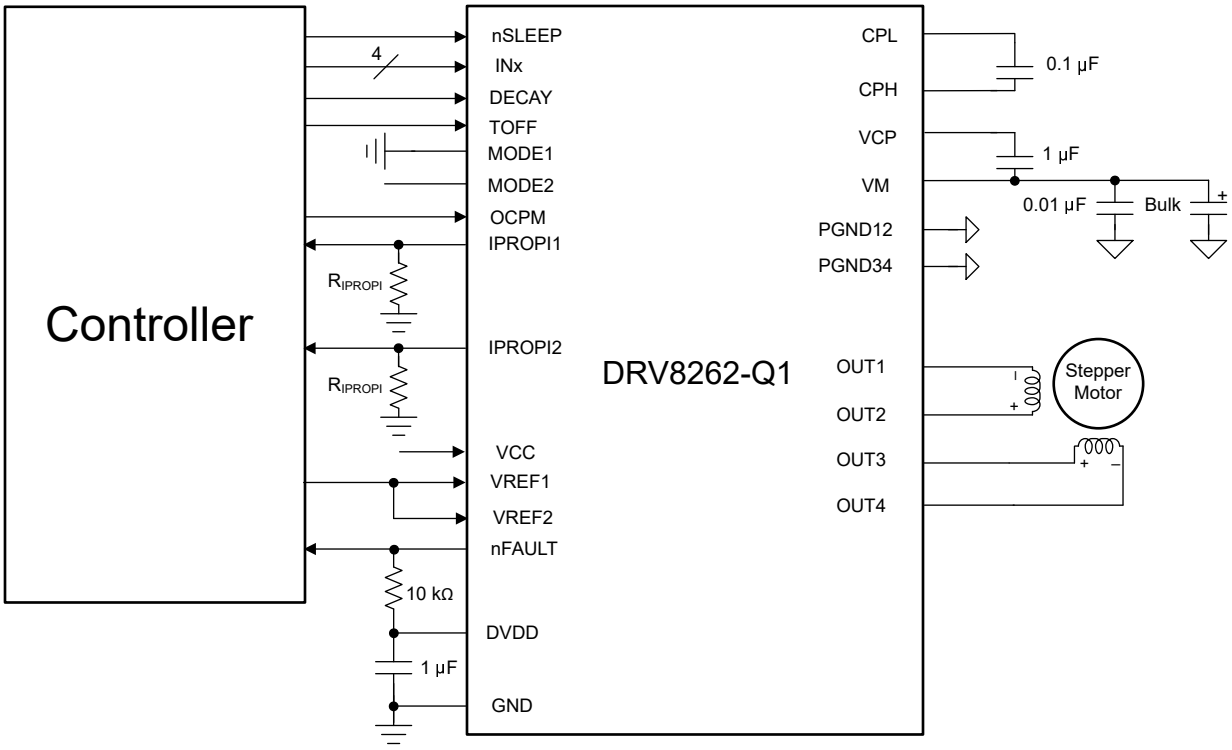

図 7-4. Driving One Stepper Motor

The full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the VREF voltage and the resistor connected from IPROPI pin to ground.

$I_{FS} \times A_{IPROPI} = V_{VREF} / R_{IPROPI}$

The maximum allowable voltage on the VREF pins is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

注

The I_{FS} current must also follow 式 5 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{5}$$

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}), determine the frequency of the input waveform as follows -

$$f_{step}\,(\text{steps}/\text{s}) = \frac{\text{v}\,(\text{rpm}) \times 360\,(^\circ/\text{rot})}{\theta_{step}\,(^\circ/\text{step}) \times n_m\,(\text{steps}/\text{microstep}) \times 60\,(\text{s}/\text{min})} \quad (6)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the DRV8262-Q1. 1/ f_{step} = t_{STEP} on the diagram below. 式 7 shows an example calculation for a 120 rpm target speed and 1/2 step.

$$f_{step}\,(\text{steps}/\text{s}) = \frac{120\ \text{rpm} \times 360^\circ/\text{rot}}{1.8^\circ/\text{step} \times 1/2\ \text{steps}/\text{microstep} \times 60\ \text{s}/\text{min}} = 800\,\text{Hz} \quad (7)$$

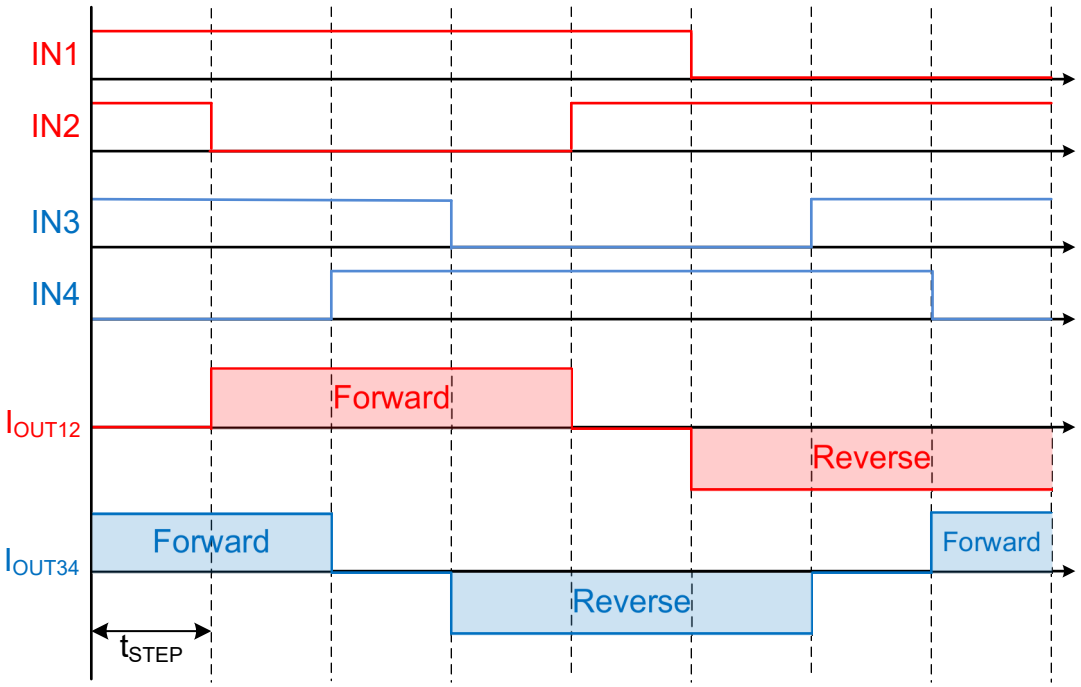

図 7-5. Example 1/2 Stepping Operation

The IPROPI pins output the current of each H-bridge, corresponding to current of coil A and coil B of the stepper motor during drive and slow-decay (high-side recirculation) modes.

7.1.2.2 Power Loss Calculations

The following calculations assume a use case where the supply voltage is 24 V, full-scale current is 5 A, and input PWM frequency is 30-kHz.

The total power dissipation constitutes of three main components - conduction loss (P_{COND}), switching loss (P_{SW}) and power loss due to quiescent current consumption (P_Q).

The conduction loss (P_{COND}) depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ONH)}$) and low-side ($R_{DS(ONL)}$) on-state resistances as shown in 式 8.

$$P_{COND} = 2 \text{ x } (I_{RMS})^2 \text{ x } (R_{DS(ONH)} + R_{DS(ONL)}) \quad (8)$$

The conduction loss for the typical application shown in セクション 7.1.2.1 is calculated in 式 9.

$$P_{COND} = 2 \text{ x } (I_{RMS})^2 \text{ x } (R_{DS(ONH)} + R_{DS(ONL)}) = 2 \text{ x } (5\text{-A} / \sqrt{2})^2 \text{ x } (0.1\text{-}\Omega) = 2.5\text{-W} \quad (9)$$

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The power loss due to the PWM switching frequency depends on the output voltage rise/fall time (t_{RF}), supply voltage, motor RMS current and the PWM switching frequency. The switching losses in each H-bridge during rise-time and fall-time are calculated as shown in 式 10 and 式 11.

$$P_{SW\_RISE} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (10)$$

$$P_{SW\_FALL} = 0.5 \times V_{VM} \times I_{RMS} \times t_{RF} \times f_{PWM} \quad (11)$$

After substituting the values of various parameters, the switching losses in each H-bridge are calculated as shown below -

$$P_{SW\_RISE} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (110\ \text{ns}) \times 30\text{-kHz} = 0.14\text{-W} \quad (12)$$

$$P_{SW\_FALL} = 0.5 \times 24\text{-V} \times (5\text{-A} / \sqrt{2}) \times (110\ \text{ns}) \times 30\text{-kHz} = 0.14\text{-W} \quad (13)$$

The total switching loss for the stepper motor driver (P_{SW}) is calculated as twice the sum of rise-time (P_{SW_RISE}) switching loss and fall-time (P_{SW_FALL}) switching loss as shown below -

$$P_{SW} = 2 \times (P_{SW\_RISE} + P_{SW\_FALL}) = 2 \times (0.14\text{-W} + 0.14\text{-W}) = 0.56\text{-W} \quad (14)$$

注

The output rise/fall time (t_{RF}) is expected to change based on the supply-voltage, temperature and device to device variation.

When the VCC pin is connected to an external voltage, the quiescent current is typically 5 mA. The power dissipation due to the quiescent current consumed by the power supply is calculated as shown below -

$$P_Q = V_{VM} \times I_{VM} \quad (15)$$

Substituting the values, quiescent power loss can be calculated as shown below -

$$P_Q = 24\text{-V} \times 5\text{-mA} = 0.12\text{-W} \quad (16)$$

注

The quiescent power loss is calculated using the typical operating supply current (I_{VM}) which is dependent on supply-voltage, temperature and device to device variations.

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss as shown in 式 17.

$$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.5\text{-W} + 0.56\text{-W} + 0.12\text{-W} = 3.18\text{-W} \quad (17)$$

7.1.2.3 Junction Temperature Estimation

Assuming 25°C ambient temperature, the junction temperature is calculated as shown below -

$$T_J = 25°C + (3.18\text{-W} \times 22.2\ °C/W) = 95.6\ °C \quad (18)$$

For more accurate calculation, consider the dependency of on-resistance of FETs with device junction temperature, as explained in セクション 7.1.1.4.

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7.1.3 Driving Thermoelectric Coolers (TEC)

Thermoelectric coolers (TEC) work according to the Peltier effect. When a voltage is applied across the TEC, a DC current flows through the junction of the semiconductors, causing a temperature difference. Heat is transferred from one side of the TEC to the other. This creates a “hot” and a “cold” side of the TEC element. If the DC current is reversed, the hot and cold sides reverse as well.

A common way of modulating the current through the TEC is to use PWM driving and make the average current change by varying the ON and OFF duty cycles. To allow both heating and cooling from a single supply, a H-bridge topology is required. In the dual H-bridge mode, the device can drive two H-bridges to drive two TECs bi-directionally with up to 5-A current. In the single H-bridge mode, the device can drive a single TEC with up to 10-A current.

The DRV8262-Q1 also features integrated current sensing and current sense output (IPROPI) with ± 4% accuracy to eliminate the need for two external shunt resistors in a closed-loop control topology, saving bill-of-materials cost and space. The following schematic shows the DRV8262-Q1 driving two TECs.

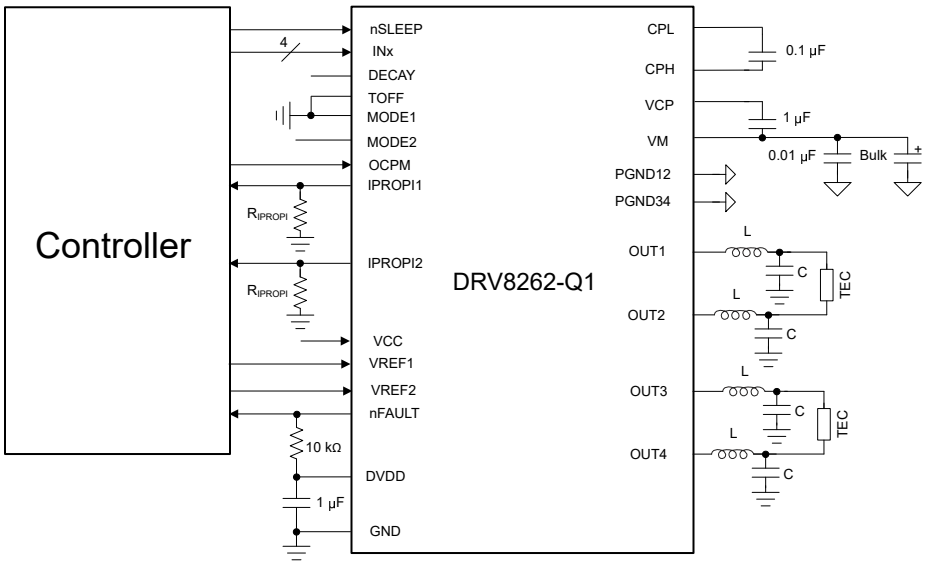

図 7-6. Driving two TECs

The following schematuic shows the DRV8262-Q1 driving one TEC with higher current.

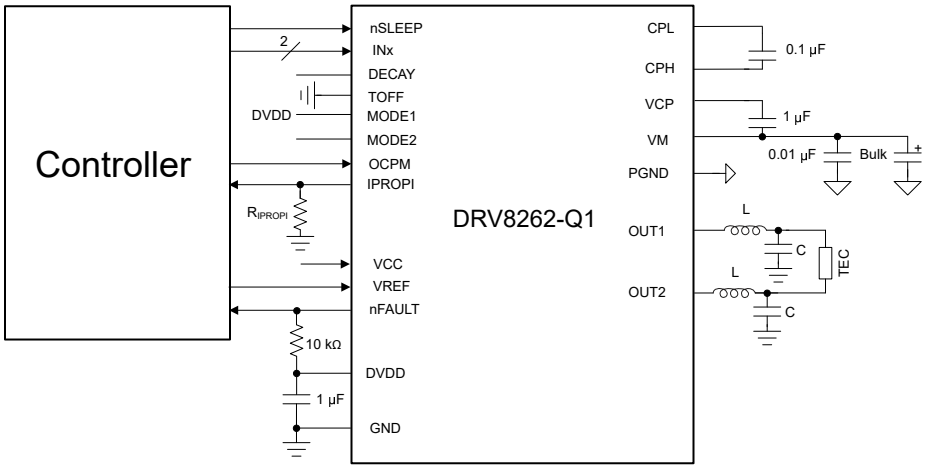

図 7-7. Driving one TEC with higher current

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The LC filters connected to the output nodes convert the PWM output from the DRV8262-Q1 into a low-ripple DC voltage across the TEC. The filters are required to minimize the ripple current, because fast transients (e.g., square wave power) can shorten the life of the TEC. The maximum ripple current is recommended to be less than 10% of maximum current. The maximum temperature differential across the TEC, which decreases as ripple current increases, is calculated with the following equation:

$$\Delta T = \Delta T_{MAX} / (1 + N^2) \quad (19)$$

Where ΔT is actual temperature differential, ΔT_{MAX} is maximum possible temperature differential specified in the TEC datasheet, N is the ratio between ripple and maximum current. N should not be greater than 0.1.

The choice of the input PWM frequency is a trade-off between switching loss and use of smaller inductors and capacitors. High PWM frequency also means that the voltage across the TEC can be tightly controlled, and the LC components can potentially be cheaper.

The transfer function of a second order low-pass filter is shown below:

$$H(j\omega) = 1 / (1 - (\omega / \omega_0)^2 + j\omega / Q\omega_0) \quad (20)$$

Where,

$\omega_0 = 1 / \sqrt{(LC)}$, resonant frequency of the filter

Q = quality factor

ω = DRV8262-Q1 input PWM frequency

The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the PWM frequency. With this assumption, 式 19 may be simplified to -

$H \text{ in dB} = -40 \log (f_S/f_0)$

Where $f_0 = 1/ 2\pi\sqrt{(LC)}$ and f_S is the input PWM switching frequency.

- If L = 10 µH and C = 22 µF, the resonant frequency is 10.7 kHz.
- This resonant frequency corresponds to 39 dB of attenuation at 100 kHz switching frequency.
- For VM = 48 V, 39 dB attenuation means that the amount of ripple voltage across the TEC element will be approximately 550 mV.
- For a TEC element with a resistance of 1.5 Ω, the ripple current through the TEC will therefore be 366 mA.
- At 5 A current, 366 mA corresponds to 7.32% ripple current.
- This will cause about 0.5% reduction of the maximum temperature differential of the TEC element, as per 式 19.

Adjust the LC values according to the supply voltage and DC current through the TEC element. The DRV8262-Q1 supports up to 200 kHz input PWM frequency. The power loss in the device at any given ambient temperature must be carefully considered before selecting the input PWM frequency.

Closing the loop on current is important in some TEC based heating and cooling systems. The DRV8262-Q1 can achieve this without the need for external current shunt resistors. Internal current mirrors are used to monitor the currents in each half-bridge and this information is available on IPROPI pins. A microcontroller can monitor and adjust the PWM duty based on the IPROPI pin voltage.

Additionally, the DRV8262-Q1 can regulate the current internally by providing an external voltage reference (VREF) to the device to adjust the current regulation trip point. The current loop would then be closed within the H-bridge itself.

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8 Package Thermal Considerations

8.1 DDW Package

Thermal pad of the DDW package is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. Refer to the セクション 10.1 section for more details.

8.1.1 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

HTSSOP (DDW package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the thermal pad for the driver. Bottom layer copper area varies with top copper area.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the thermal pad (13 x 5 thermal via array, 1.1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Mid layer 1: GND plane thermally connected to thermal pad through vias. The area of the ground plane varies with top copper area.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane varies with top copper area.
  - Bottom layer: signal layer thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is the same size as the top layer copper area.

図 8-1 shows an example of the simulated board for the DDW package. 表 8-1 shows the dimensions of the board that were varied for each simulation.

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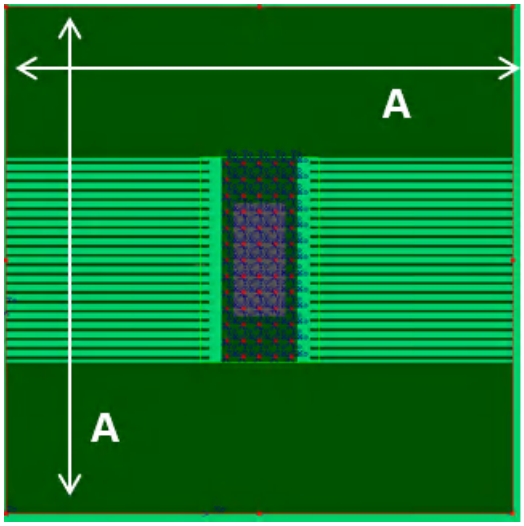

図 8-1. DDW PCB model top layer

表 8-1. Dimension A for DDW package

Cu area (cm^2)	Dimension A (mm)
2	19.79
4	26.07
8	34.63
16	46.54
32	63.25

8.1.1.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

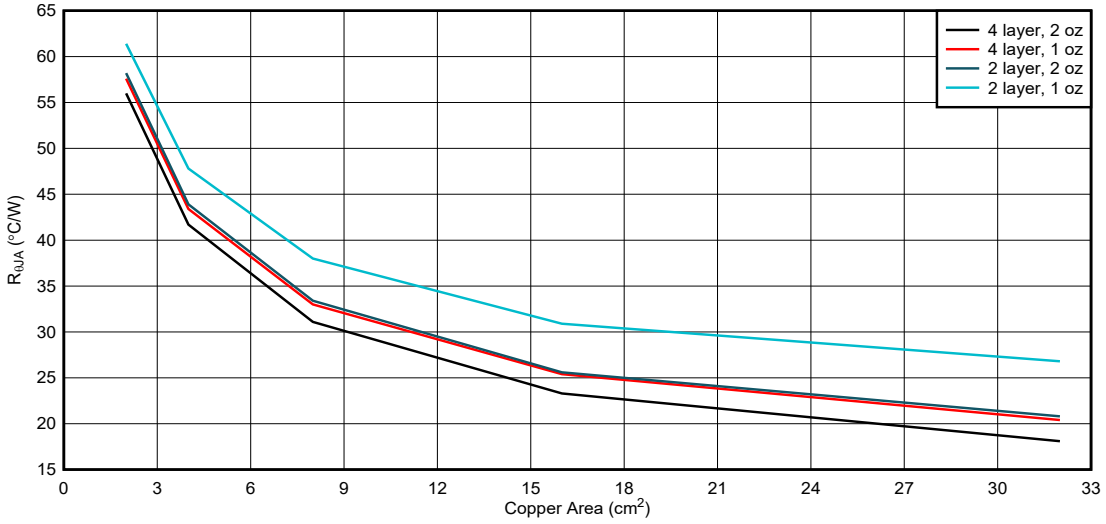

図 8-2. DDW Package, PCB junction-to-ambient thermal resistance vs copper area

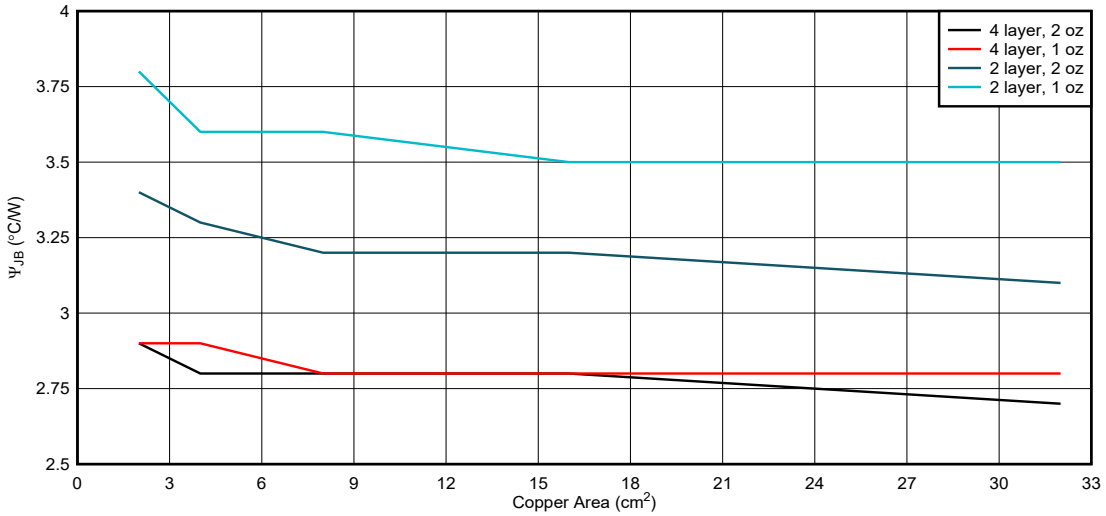

図 8-3. DDW Package, junction-to-board characterization parameter vs copper area

8.1.1.2 Transient Thermal Performance

The driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include -

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the DDW package. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

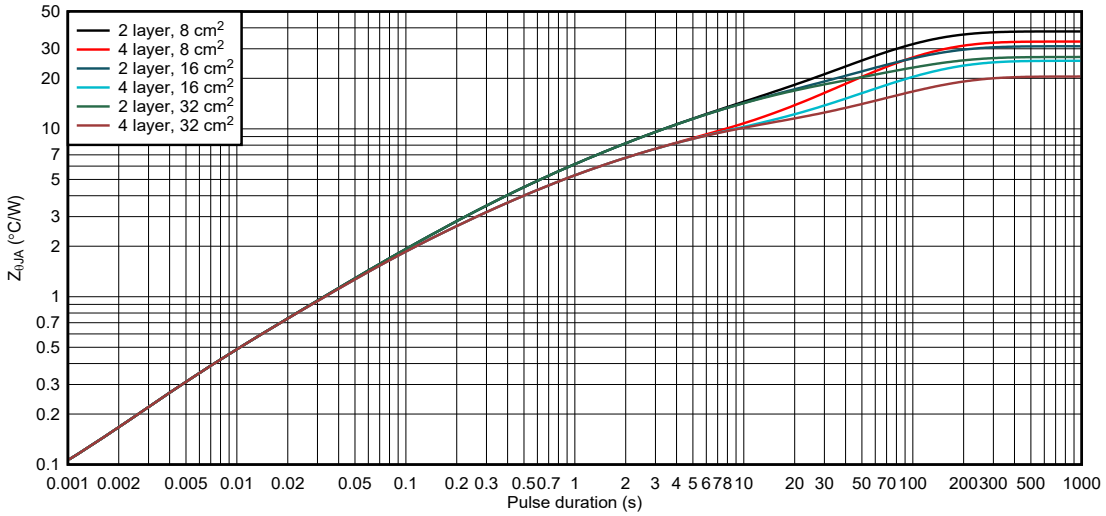

図 8-4. DDW package junction-to-ambient thermal impedance for 1-oz copper layouts

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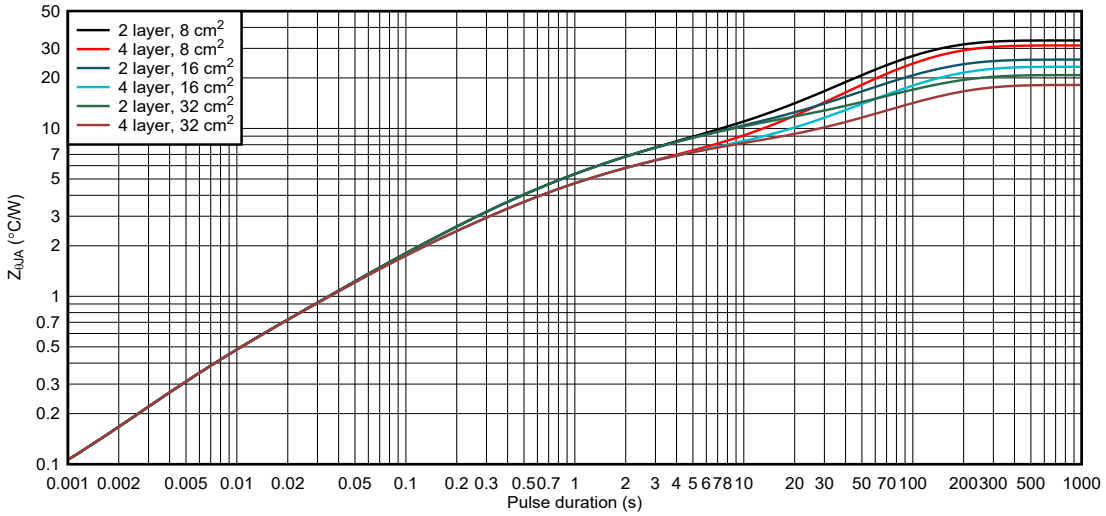

図 8-5. DDW package junction-to-ambient thermal impedance for 2-oz copper layouts

8.2 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper on both top and bottom layer is recommended for improved thermal performance and better EMI margin (due to lower PCB trace inductance).

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 60 V. A 0.01-µF ceramic capacitor rated for VM must be placed close to the VM pins of the device. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

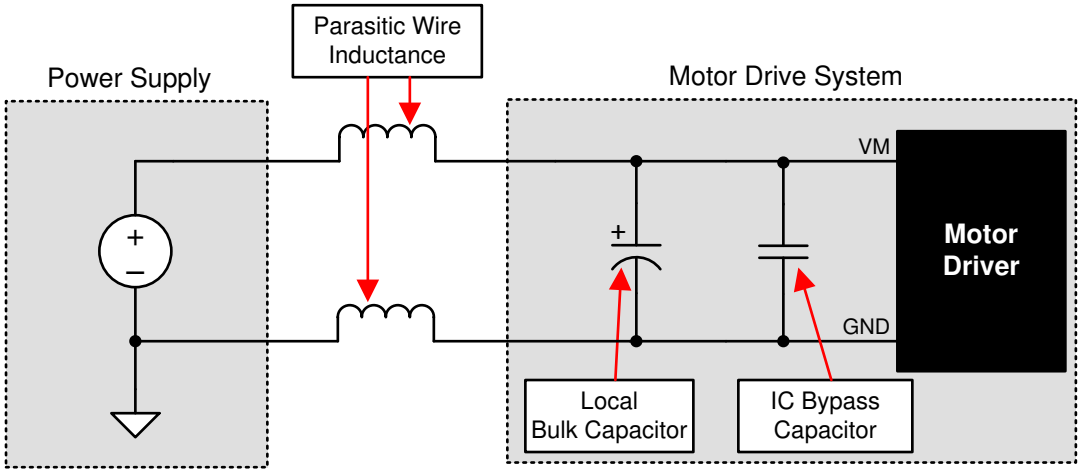

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図 9-1. Example Setup of Motor Drive System With External Power Supply

9.2 Power Supplies

The device needs only a single supply voltage connected to the VM pins.

- The VM pin provides the power supply to the H-Bridges.
- An internal voltage regulator provides a 5V supply (DVDD) for the digital and low-voltage analog circuitry. The DVDD pin is not recommended to be used as a voltage source for external circuitry.
- An external low-voltage supply can be connected to the VCC pin to power the internal circuitry. A 0.1-µF decoupling capacitor should be placed close to the VCC pin to provide a constant voltage during transient.

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- Additionally, the high-side gate drive requires a higher voltage supply, which is generated by built-in charge pump requiring external capacitors.

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10 Layout

10.1 Layout Guidelines

- The VM pins should be bypassed to PGND pins using low-ESR ceramic bypass capacitors with a recommended value of 0.01 µF rated for VM. The capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device PGND pins.
- The VM pins must be bypassed to PGND using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.
- A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 1 µF rated for 16 V is recommended. Place this component as close to the pins as possible.
- Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- Bypass the VCC pin to ground with a low-ESR ceramic capacitor. A value of 0.1 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the DDW package must be connected to system ground.
  - It is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer.
  - In order to minimize the impedance and inductance, the traces from ground pins should be as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD will also help spreading the heat and reduce the thermal resistance.

10.2 Layout Example

Follow the layout example of the DRV8262-Q1 EVM. The design files can be downloaded from the DRV8262Q1EVM product folder.

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Motor Drives Layout Guide* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *What Motor Drivers should be considered for driving TEC*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2024	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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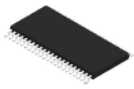
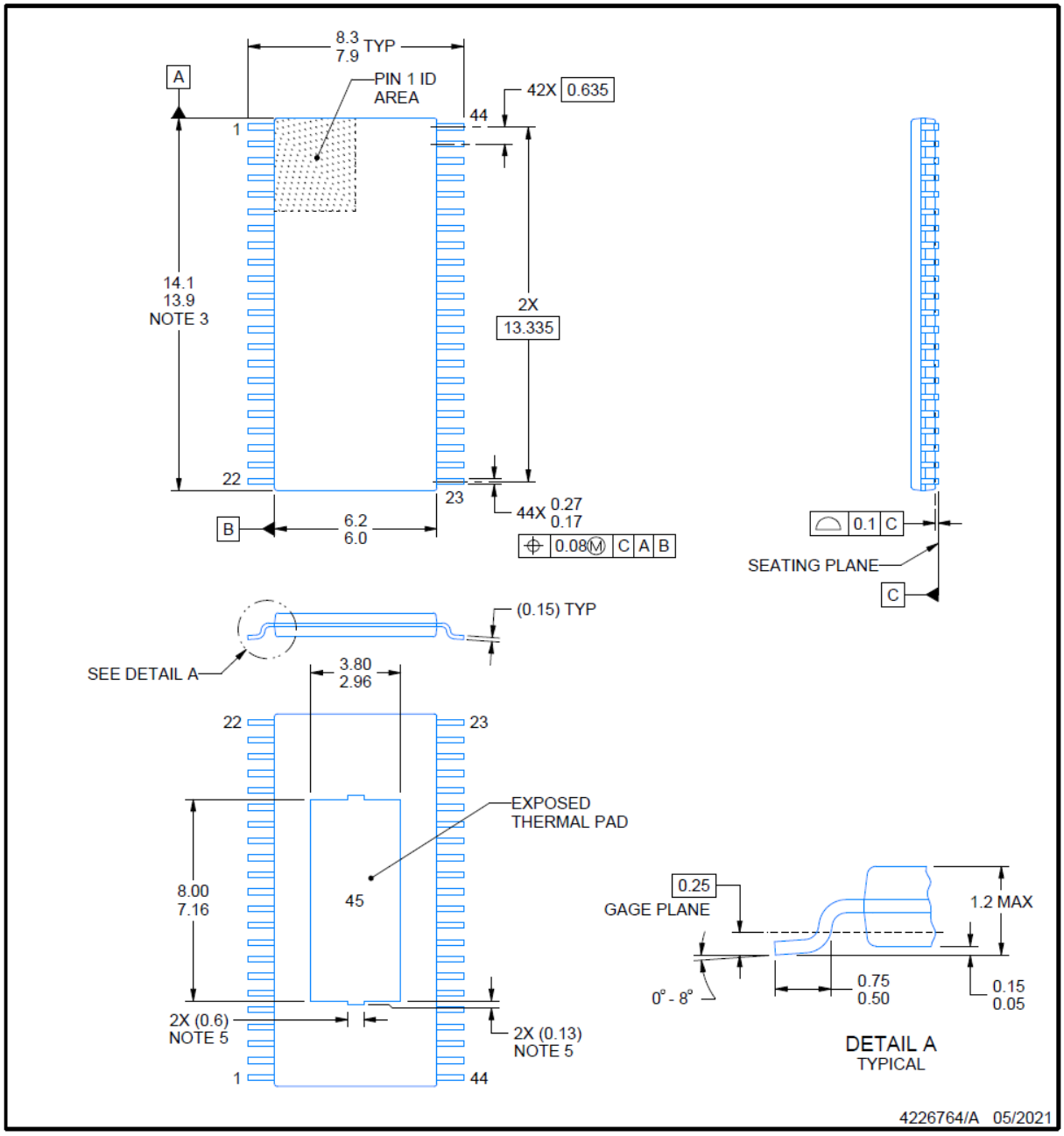
PACKAGE OUTLINE

DDW0044E



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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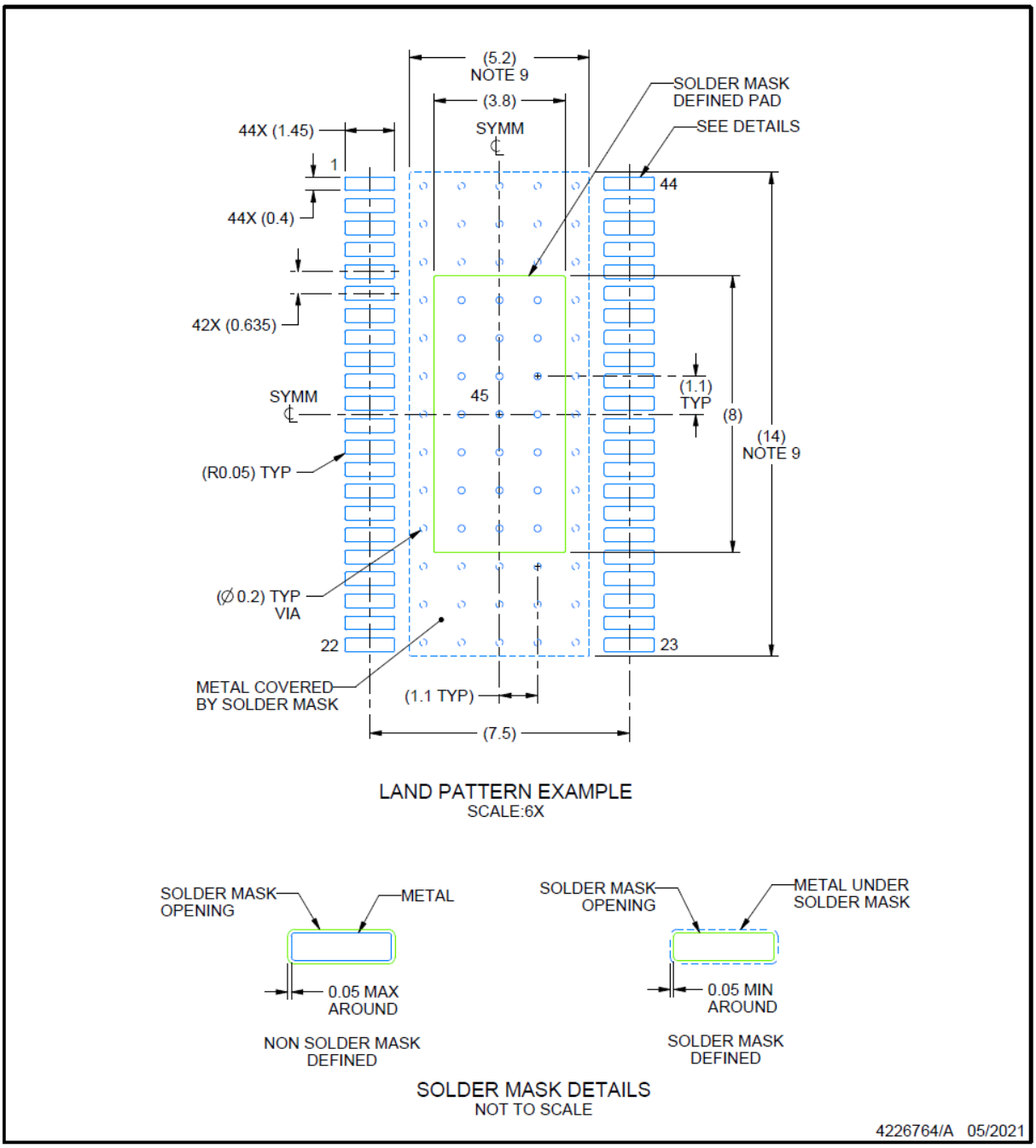
EXAMPLE BOARD LAYOUT

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

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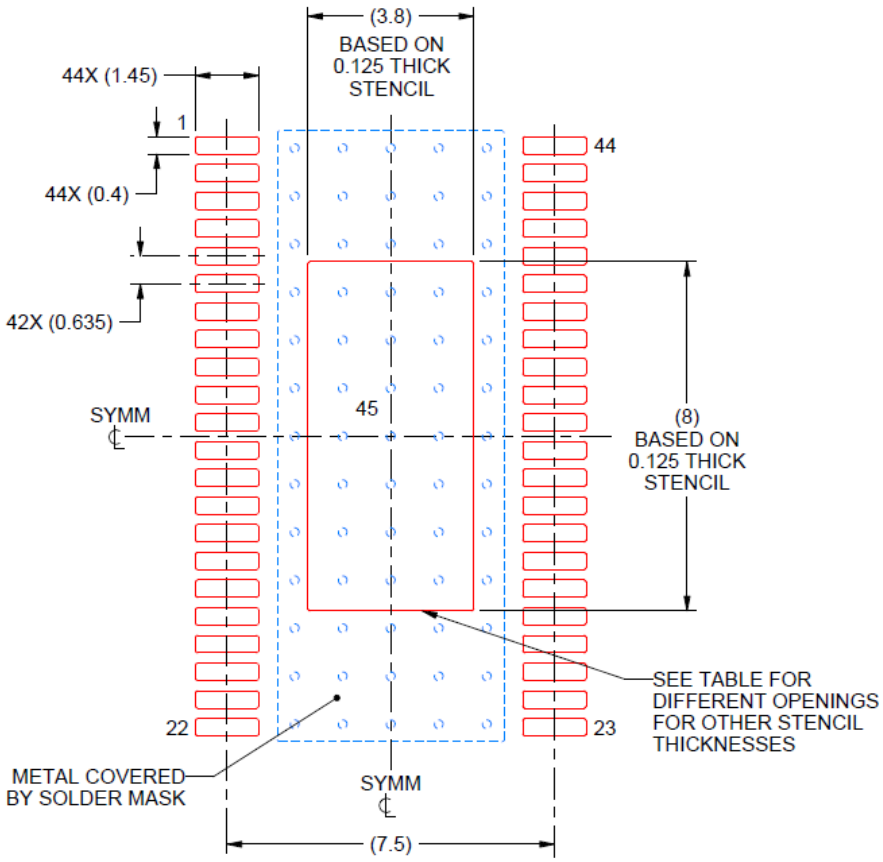
EXAMPLE STENCIL DESIGN

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

4226764/A 05/2021

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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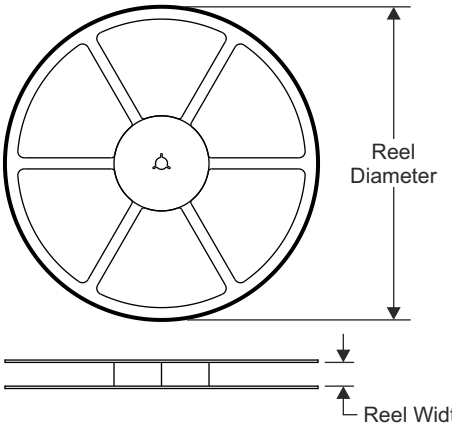
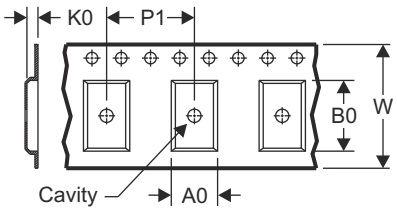
13.1 Tape and Reel Information

REEL DIMENSIONS

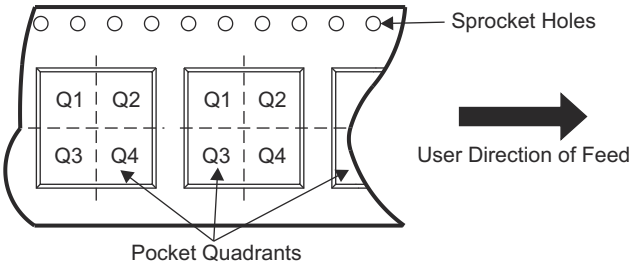


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8262QDDWRQ1	HTSSOP	DDW	44	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

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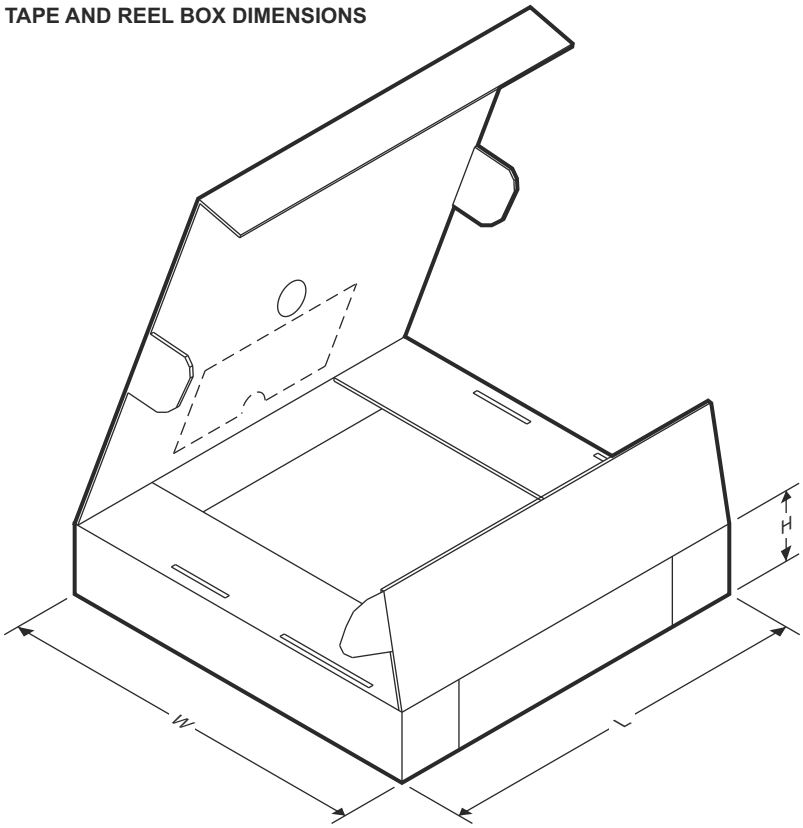
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8262QDDWRQ1	HTSSOP	DDW	44	2500	367.0	367.0	45.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8262QDDWRQ1	ACTIVE	HTSSOP	DDW	44	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8262Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DRV8262-Q1 :

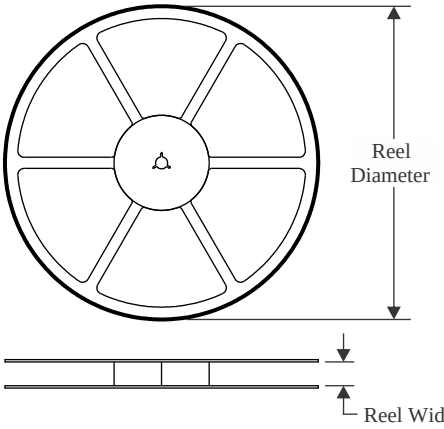
- Catalog : DRV8262

NOTE: Qualified Version Definitions:

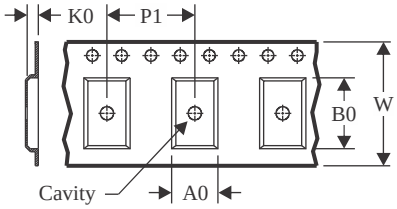
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

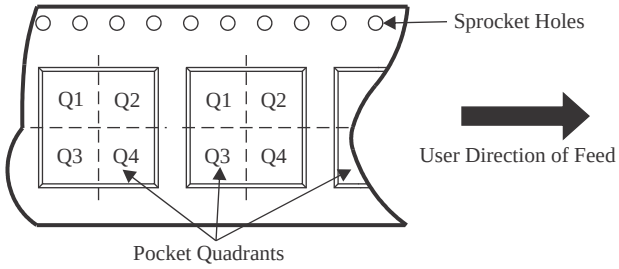


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

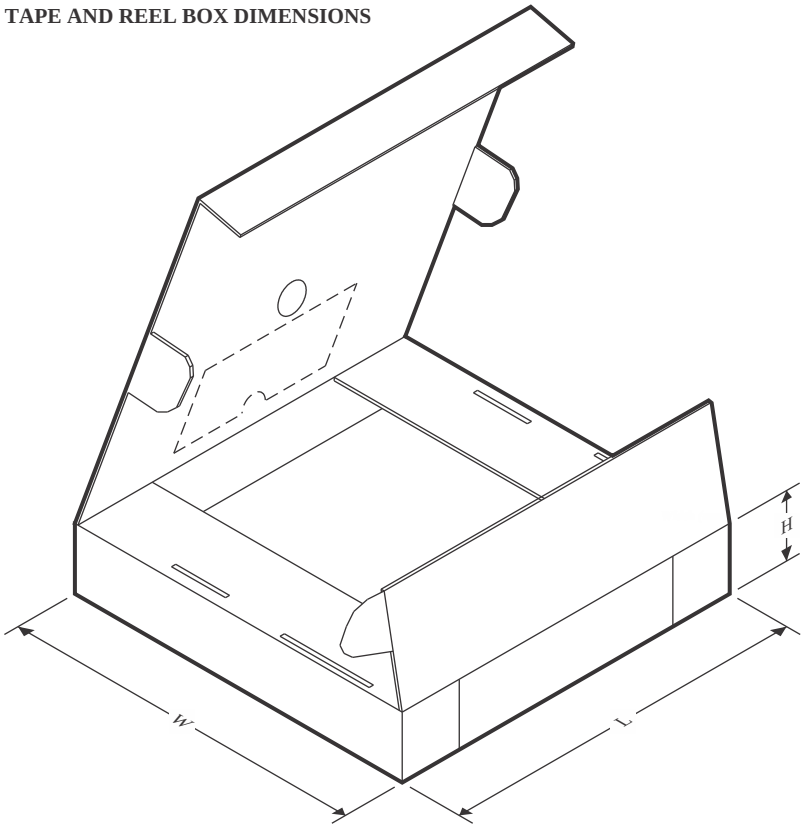
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8262QDDWRQ1	HTSSOP	DDW	44	2500	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8262QDDWRQ1	HTSSOP	DDW	44	2500	356.0	356.0	41.0

GENERIC PACKAGE VIEW

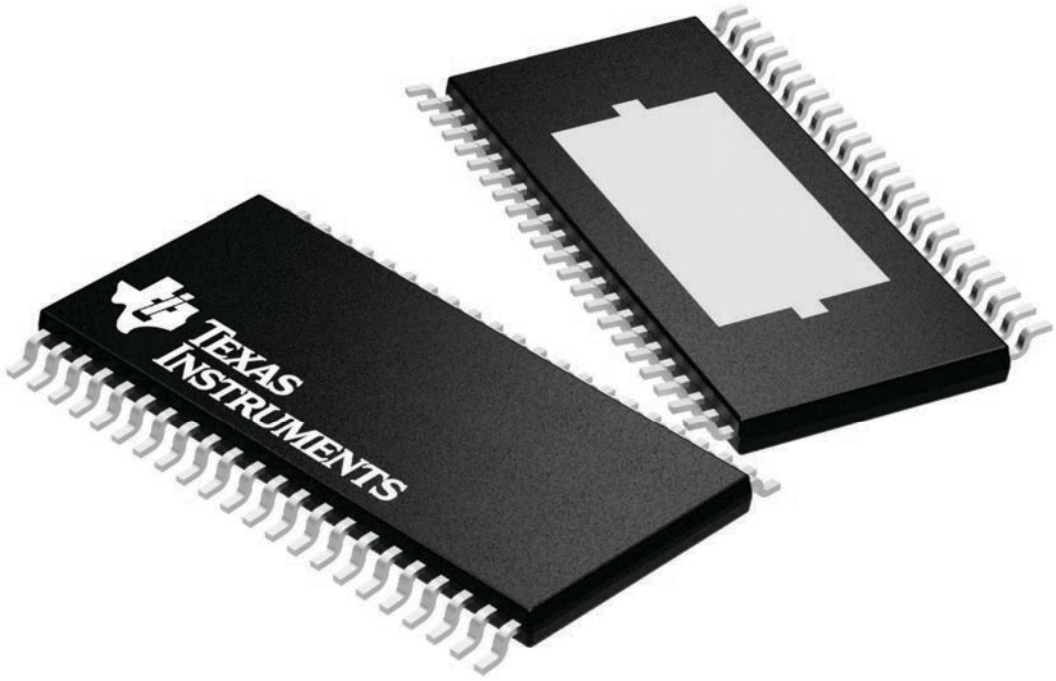
DDW 44

PowerPAD TSSOP - 1.2 mm max height

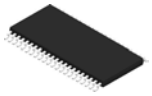
6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224876/A

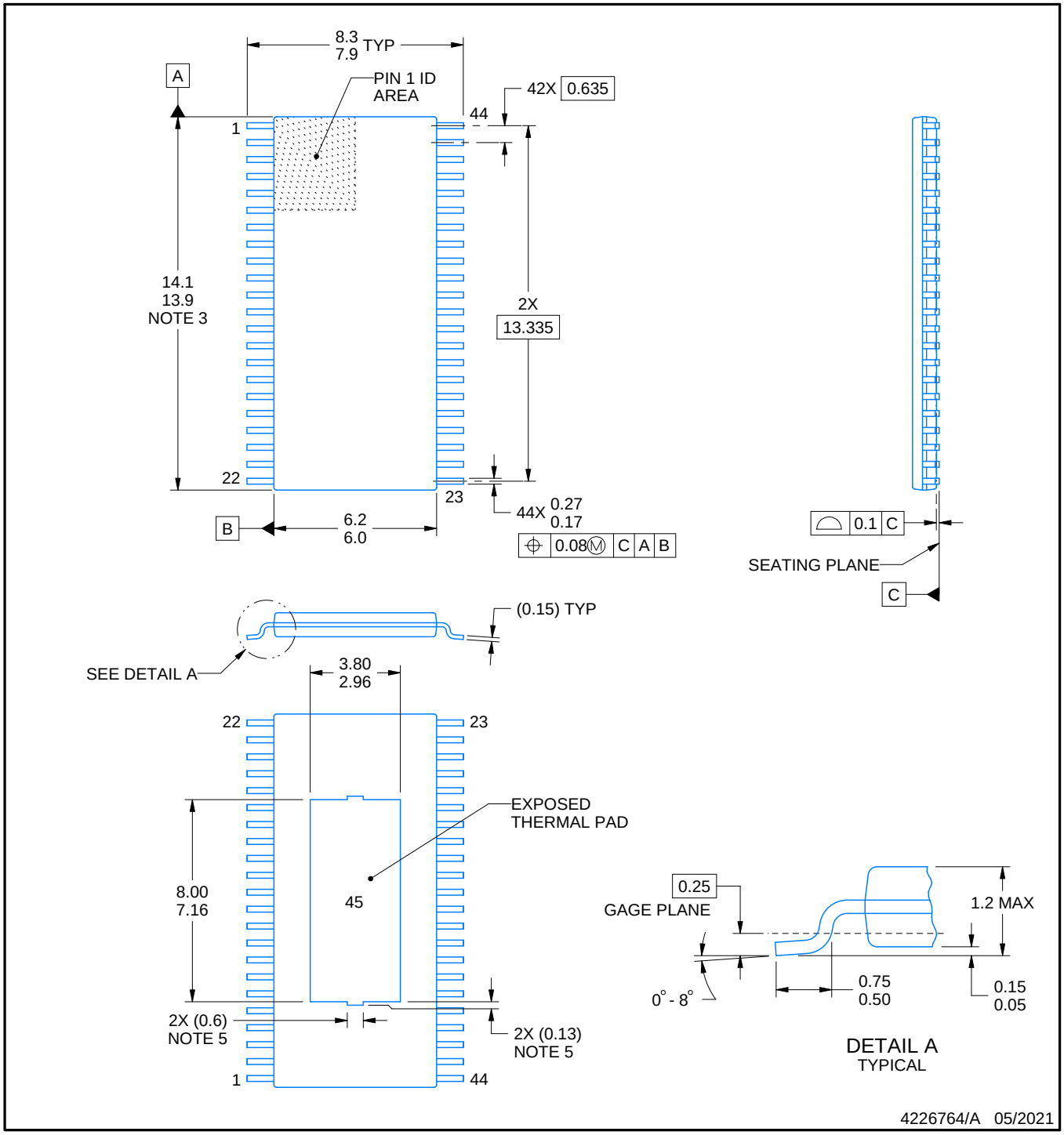


PACKAGE OUTLINE

DDW0044E

PowerPAD™ TSSOP - 1.2 mm max height

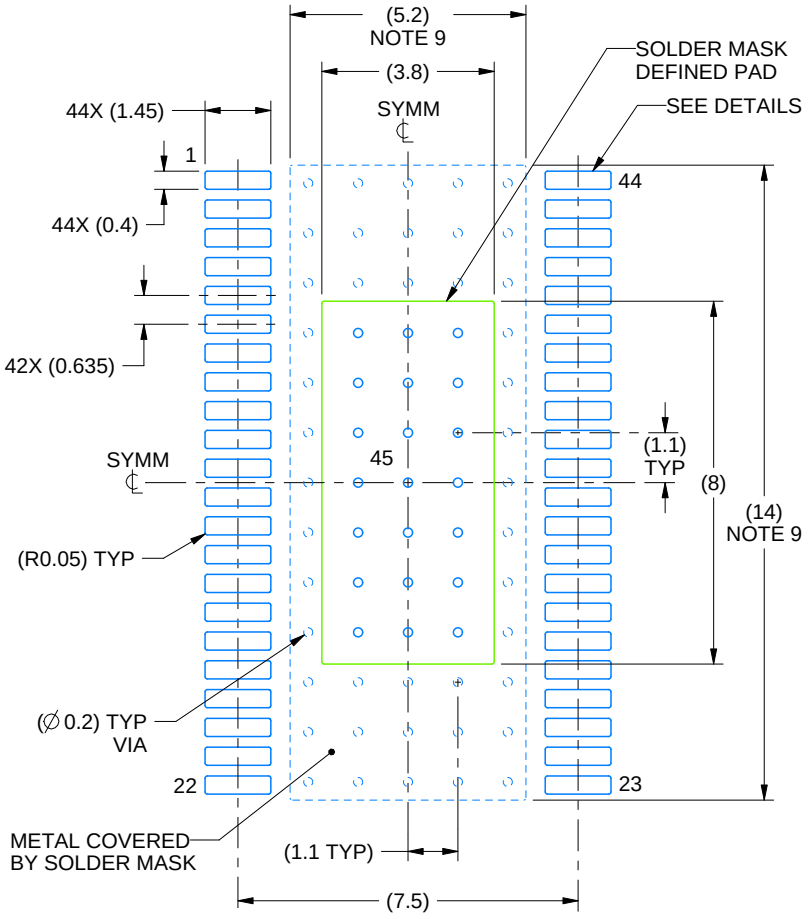
PLASTIC SMALL OUTLINE



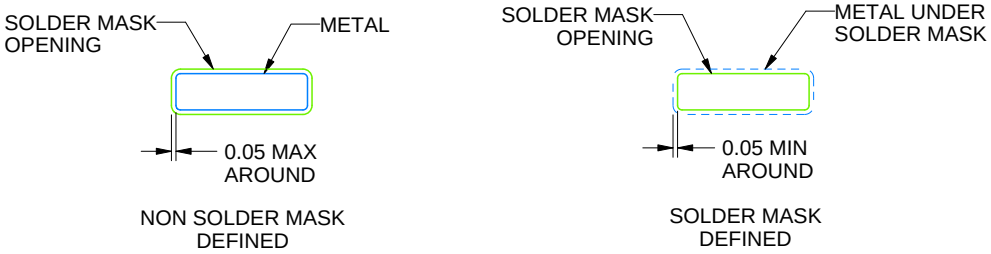
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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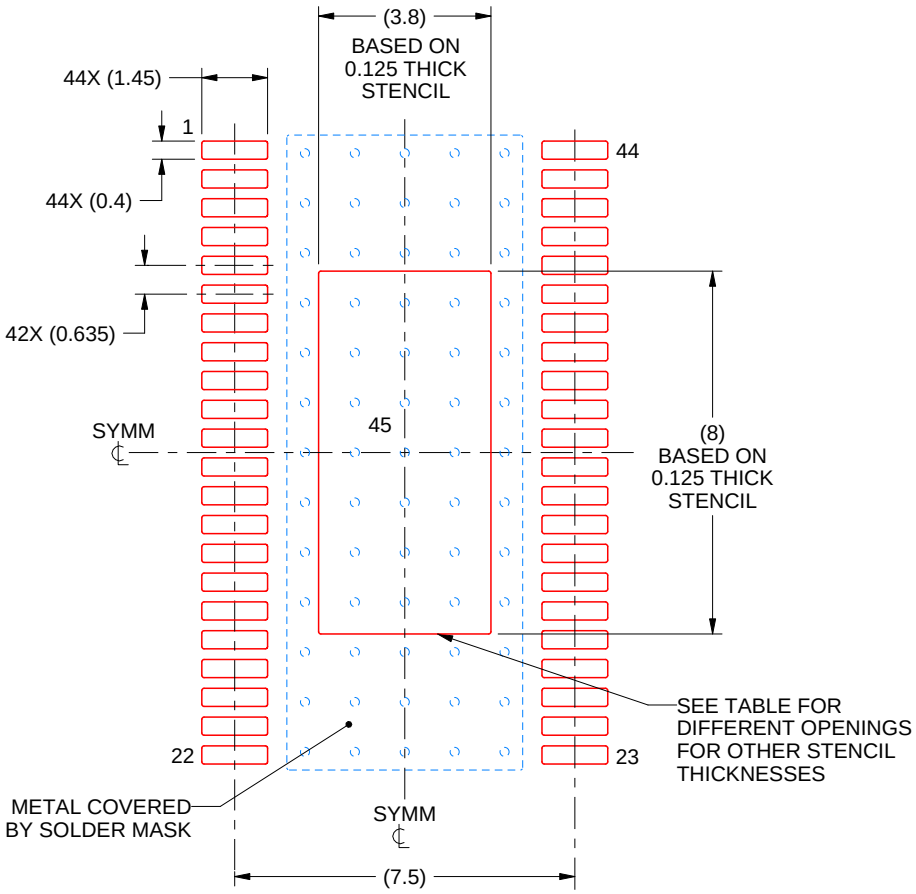
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 8.94
0.125	3.80 X 8.00 (SHOWN)
0.15	3.47 X 7.30
0.175	3.21 X 6.76

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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