DRV8376 3 相 FET 内蔵モーター ドライバ

1 特長

- 三相 BLDC モータードライバ
  - 48V システムをサポート
  - 最大 100kHz の PWM 周波数をサポート
  - アクティブ消磁により電力損失を低減
  - サイクル単位の電流制限により位相電流を制限
- 動作電圧:4.5V～65V (絶対最大定格 70V)
- 高い出力電流能力:ピーク 4.5A
- 低い MOSFET オンステート抵抗
  - T_A = 25℃で 400mΩ の $R_{DS(ON)}$ (HS + LS)
- 1.1V/ns のスルーレートと逆方向回復損失の最小化手法により、スイッチング損失を低減します
  - 調整可能なスルー レート オプション
- 200ns 未満の非常に短いデッドタイムと、100ns 未満の伝搬遅延により、小さい可聴ノイズとモーター制御が容易
- 低消費電力スリープ モード
  - 1.5μA (標準値) (V_{VM} = 24V、T_A = 25°C)
- 複数の制御インターフェイス オプション
  - 6x PWM 制御インターフェイス
  - 3x PWM 制御インターフェイス
- 電流センス機能内蔵、外付け電流センス抵抗不要
- 柔軟なデバイス構成オプション
  - DRV8376S:デバイスの構成とフォルト ステータスのための 5MHz、16 ビット SPI インターフェイス
  - DRV8376H:ハードウェア ピンベースの構成
- 1.8V、3.3V、5V のロジック入力をサポート
- 3.3V (5%)、30mA LDO レギュレータ内蔵
- 5V (5%)、30mA LDO レギュレータ内蔵
- 各種保護機能を内蔵
  - 電源低電圧誤動作防止 (UVLO)
  - チャージ ポンプ低電圧 (CPUV)
  - 過電流保護 (OCP)
  - 熱警告およびシャットダウン (OTW/OTSD)
  - フォルト状況表示ピン (nFAULT)
  - SPI インターフェイスによるフォルト診断 (オプション)

2 アプリケーション

- ブラシレス DC (BLDC) モーター モジュール
- HVAC モーター
- OA 機器
- ファクトリ オートメーションおよびロボティクス
- ワイヤレス アンテナ モーター
- ATM (現金自動預け払い機)
- ドローン

3 概要

DRV8376 は、4.5V から 65V のブラシレス DC モーターを駆動するためのシングルチップ電力段ソリューションを提供します。DRV8376 は、大電力駆動能力を実現するため、70V の絶対最大定格と 400mΩ (ハイサイドとローサイドの合計) という非常に小さい $R_{DS(ON)}$ を持つ 3 つのハーフ H ブリッジを内蔵しています。内蔵の電流検出機能を使用して電流を検出するので、外付けの検出抵抗は不要です。内蔵 LDO による電源管理機能が、デバイスに必要な電圧レールを生成します。また、外部回路に電力を供給するためにも使用できます。

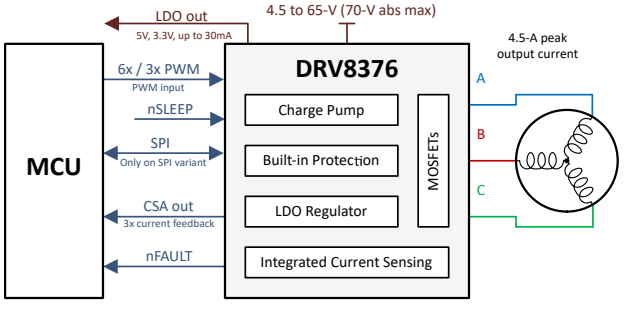
DRV8376 には 6x または 3x の PWM 制御方式が実装されており、センサ付きまたはセンサレスのフィールド オリエンテッド制御 (FOC)、正弦波制御、または外付けマイコンを使用した台形制御を実現できます。DRV8376 は、最大 100kHz の PWM 周波数で駆動できます。制御方式は、モーター電流制限動作からフォルト応答まで、ハードウェア ピンまたはレジスタ設定を使って詳細に設定できます。

DRV8376 は、本デバイス自身、モーター、システムをフォルト イベントから保護するための多くの保護機能を内蔵しています。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (公称)
DRV8376H	VQFN (28)	6.00 mm × 5.00mm	6.00 mm × 5.00mm
DRV8376S (3)	VQFN (28)	6.00 mm × 5.00mm	6.00 mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) このデバイスはプレビュー版としてのみ供給されます。



概略回路図

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4 Device Comparison Table

DEVICE	PACKAGES	INTERFACE
DRV8376S	28-pin VQFN (6x5mm)	SPI
DRV8376H		Hardware

表 4-1. DRV8376S (SPI variant) vs. DRV8376H (Hardware variant) configuration comparison

Parameters	DRV8376S (SPI variant)	DRV8376H (Hardware variant)
PWM mode settings	PWM_MODE (4 settings)	MODE_SR pin (4 settings)
Slew rate settings	SLEW_RATE (4 settings)	SLEW pin (4 settings)
CSA gain settings	CSA_GAIN (4 settings)	GAIN pin (4 settings)
SDO pin configuration: mode, voltage	SDO_ODEN (2 settings), SDO_VSEL (2 settings), SDO_MD (2 settings)	
Current Limit configuration: Mode, reporting on nFAULT, Blanking time, 100% duty PWM frequency	ILIMFLT_MODE (2 settings), ILIM_MODE (2 settings), ILIM_BLANK_SEL (4 settings), PWM_100_FREQ_SEL (4 settings)	Current limit reporting on nFAULT is enabled, fixed to coast mode, blanking time set to 5.5µs for slew rate of 50 and 1.8µs for all other slew rates, the 100% duty input PWM cycle is fixed to 20kHz
Over voltage protection mode	OVP_MODE (2 settings), OVP_SEL (2 settings)	Over voltage protection is disabled
OCP configuration: Mode, level, deglitch	OCP_MODE (4 settings) , OCP_LVL (2 settings) ,OCP_DEG (4 settings) and OCP_RETRY (2 settings)	Enabled with automatic retry mode, level is fixed to 4.5A with 1.25µs deglitch time, 5ms retry time
Active demagnetization: Enable, comparator threshold, comparator mask time, behaviour during fault	EN_ASR (2 settings), EN_AAR (2 settings), AD_COMP_TH (2 settings)	MODE_SR (2 settings), active demag comparator threshold set to 100mA, comparator mask time set to 5.5µs for slew rate of 50 and 1.8µs for all other slew rates. ADMAG_TMARGIN set to 1.6µs, active demag is disabled during OCP.
Over temperature warning	OTW_MODE (2 settings)	Reported on nFAULT

5 Pin Configuration and Functions

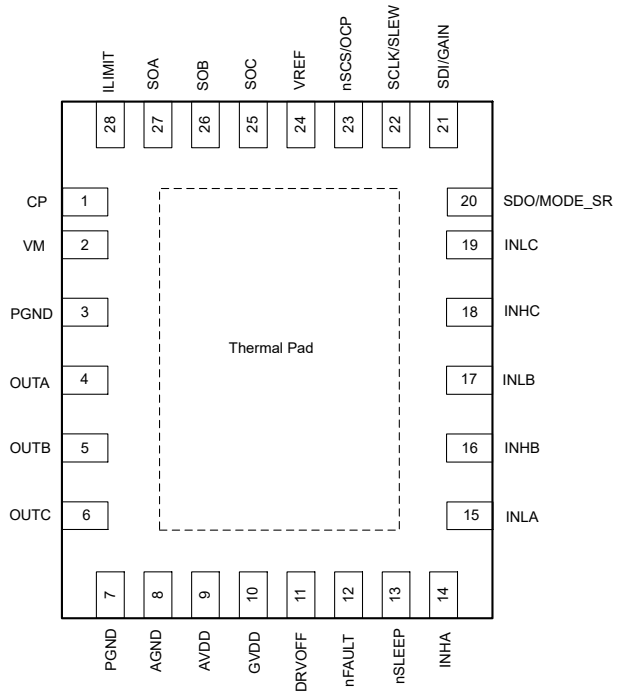

図 5-1. DRV8376 28-Pin VQFN With Exposed Thermal Pad Top View

表 5-1. DRV8376 Pin Functions

PIN	28-pin VQFN Package		TYPE(1)	DESCRIPTION
NAME	DRV8376H	DRV8376S		
AGND	8	8	GND	Device analog ground. Refer セクション 8.3.1 for connections recommendation.
AVDD	9	9	PWR O	3.3V internal regulator output. Connect an X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30mA externally.
CP	1	1	PWR O	Charge pump output. Connect a X5R or X7R, 0.1µF, 16V ceramic capacitor between the CP and VM pins.
DRVOFF	11	11	I	When this pin is pulled high the six MOSFETs in the power stage are turned OFF making all outputs Hi-Z.
GAIN	21	-	I	Current sense amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GVDD	10	10	PWR O	5V internal regulator output. Connect an X5R or X7R, 1µF, 10V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30 mA externally.
ILIMIT	28	28		Sets the threshold for phase current used in cycle by cycle current limit.
INHA	14	14	I	High-side driver control input for OUTA. This pin controls the output of the high-side MOSFET.
INHB	16	16	I	High-side driver control input for OUTB. This pin controls the output of the high-side MOSFET.
INHC	18	18	I	High-side driver control input for OUTC. This pin controls the output of the high-side MOSFET.
INLA	15	15	I	Low-side driver control input for OUTA. This pin controls the output of the low-side MOSFET.
INLB	17	17	I	Low-side driver control input for OUTB. This pin controls the output of the low-side MOSFET.

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表 5-1. DRV8376 Pin Functions (続き)

PIN	28-pin VQFN Package		TYPE(1)	DESCRIPTION
NAME	DRV8376H	DRV8376S		
INLC	19	19	I	Low-side driver control input for OUTC. This pin controls the output of the low-side MOSFET.
MODE_SR	20	-	I	PWM input mode setting. This pin is a 4-level input pin set by an external resistor.
nFAULT	12	12	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V. If an external supply is used to pull up nFAULT, ensure that it is pulled to >2.2V on power up.
nSCS	-	23	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	13	13	I	Driver nSLEEP. When this pin is logic-low, the device goes into a low-power sleep mode. A 20 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
OCP	23	-	I	OCP level setting. This pin is a 2 level input pin set by an external resistor (Hardware devices).
OUTA	4	4	PWR O	Half bridge output A
OUTB	5	5	PWR O	Half bridge output B
OUTC	6	6	PWR O	Half bridge output C
PGND	3, 7	3, 7	GND	Device power ground. Refer セクション 8.3.1 for connections recommendation.
SCLK	-	22	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	-	21	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	-	20	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SLEW	22	-	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor.
SOA	27	27	O	Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to GND)
SOB	26	26	O	Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to GND)
SOC	25	25	O	Current sense amplifier output. Supports capacitive load or low pass filter (resistor in series and capacitor to GND)
VM	2	2	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with a 0.1-µF capacitor plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
VREF	24	24	PWR/I	Current sense amplifier reference. Connect a X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the VREF and AGND pins.
Thermal pad			AGND	Must be connected to analog ground.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	70	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (PGND, AGND)	–0.6	0.6	V
Charge pump voltage (CP)	–0.3	V_M + 6	V
Analog regulators pin voltage (GVDD)	–0.3	5.75	V
Analog regulators pin voltage (AVDD)	-0.3	5.75	V
Analog pin input voltage (VREF, ILIMIT)	-0.3	5.75	V
Analog pin output voltage (SOx)	-0.3	5.75	V
Logic pin input voltage (DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO,)	–0.3	5.75	V
Multi-level pin input voltage (GAIN, MODE_SR, OCP, SLEW)	-0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	65	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			100	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			4	A
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI, OCP	–0.1		5.5	V
V_{IN}	Multilevel input voltage	GAIN, MODE_SR, SLEW	-0.1		GVDD	
V_{OD}	Open drain pullup voltage	nFAULT, SDO, FG	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		AVDD	V
I_{OD}	Open drain output current	nFAULT, SDO, FG			5	mA
V_{VREF}	Voltage reference pin voltage	VREF		2.8	5.5	V
ILIMIT	Voltage reference for current limit	ILIMIT	-0.1		5.5	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

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6.4 Thermal Information

THERMAL METRIC(1)		DRV8376H, DRV8376S VQFN (NLG) 28 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6V, nSLEEP = 0, T_A = 25 °C		1.5		µA
		nSLEEP = 0		2.5		µA
I_{VMS}	VM standby mode current	V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C		6.6		mA
		nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF'		6.6		mA
I_{VM}	VM operating mode current	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 20 kHz		8.5		mA
		nSLEEP =1, f_{PWM} = 20 kHz		8.5		mA
		nSLEEP =1, f_{PWM} =100 kHz		11		mA
V_{GVDD}	Analog regulator voltage	0 mA ≤ I_{GVDD} ≤ 30 mA; (External Load); VM > 6V	4.75	5	5.25	V
V_{GVDD}	Analog regulator voltage	0 mA ≤ I_{GVDD} ≤ 30 mA; (External Load); VM = 4.5V	3.7		4.5	V
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA; (External Load)	3.1	3.3	3.465	V
I_{GVDD}	External analog regulator load	I_{AVDD} = 0 mA			30	mA
I_{AVDD}	External analog regulator load	I_{GVDD} = 0 mA			30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	4	5	6	V
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			5.5	ms
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
LOGIC-LEVEL INPUTS (DRVOFF, INHx, INLx, nSLEEP, SCLK, SDI, OCP)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	nSLEEP	1.6		5.5	V
		Other Pins	1.5		5.5	V
V_{HYS}	Input logic hysteresis	nSLEEP		250		mV
		Other PIns		300		mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 5 V	15		35	µA
I_{IH}	Input logic high current	Other pins, V_{PIN} (Pin Voltage) = 5 V	30		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	300	kΩ
		Other pins	70	100	130	kΩ

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{GED}	Deglitch time	DRVOFF pin	0.8	1	1.2	µs
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			300		mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–1		25	µA
R_{PU}	Input pullup resistance		80	100	130	kΩ
C_{ID}	Input capacitance			30		pF
FOUR-LEVEL INPUTS (GAIN, MODE_SR, SLEW)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.2*GVDD	V
V_{L2}	Input mode 2 voltage	Hi-Z	0.27*GVDD	0.5*GVDD	0.55*GVDD	V
V_{L3}	Input mode 3 voltage	47 kΩ +/- 5% tied to GVDD	0.6*GVDD	0.76*GVDD	0.9*GVDD	V
V_{L4}	Input mode 4 voltage	Tied to GVDD	0.94*GVDD		GVDD	V
R_{PU}	Input pullup resistance	To GVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA, SDO_VSEL = 0	2.6		AVDD	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA, SDO_VSEL = 1, V_{VM} > 6V	4		GVDD	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		400	505	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		407		mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		690		mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		705		mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 1 A		1100		V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 1 A		500		V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to GVDD, I_{OUTx} = 1 A		250		V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 1 A		50		V/us

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, I_{OUTx} = 1 A		1100		V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, I_{OUTx} = 1 A		500		V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to GVDD, I_{OUTx} = 1 A		250		V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, I_{OUTx} = 1 A		50		V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			2	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND, HS driver ON to LS driver OFF		65		ns
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z, HS driver ON to LS driver OFF		100		ns
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to GVDD, HS driver ON to LS driver OFF		100		ns
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to GVDD, HS driver ON to LS driver OFF		250		ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24 V, INHx = 1 to OUTx transisition, SLEW = 00b or SLEW pin tied to AGND		35		ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SLEW = 01b or SLEW pin to Hi-Z		40		ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to GVDD		45		ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SLEW = 11b or SLEW pin tied to GVDD		1200		ns
t_{MIN_PULSE}	Minimum output pulse width	SLEW = 00b or SLEW pin tied to AGND	100			ns
CURRENT SENSE AMPLIFIER						
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 00		0.4		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 01		1		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 02		2.5		V/A
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 03		5		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin tied to AGND		0.4		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin to Hi-Z		1		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin to 47 kΩ ± 5% to GVDD		2.5		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin tied to GVDD		5		V/A
G_{CSA_ERR}	Current sense gain error	T_J = 25°C, LS FET Current < 2A		±5		%
		T_J = 25°C, LS FET Current > 2A (Current direction from OUTx to PGND)		±5		%
		LS FET Current < 2A		±5		%
		2A < LS FET Current < 4A; (Current direction from OUTx to PGND)		±5		%
I_{MATCH}	Current sense gain error matching between phases A, B and C	T_A = 25°C		±5		%
				±5		%

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FS_{POS}	Full scale positive current measurement	Current direction from PGND to OUTx in the LS FET, VREF = 3.3 V	2			A
FS_{NEG}	Full scale negative current measurement	Current direction from OUTx to PGND in the LS FET, VREF = 3.3 V			–3.5	A
V_{LINEAR}	SOX output voltage linear range		0.25		VREF-0.25	V
I_{OFFSET}	Current sense offset	T_J = 25°C, Phase current = 0 A		±10		mA
t_{SET}	Settling time to ±1%, 30 pF	Step on SOX = 1.2 V			1	µs
$t_{CSA\_ON\_DELAY}$	Delay from INLx turn on to current sense amplifier turn on	SR = 1000 V/µs or 500 V/µs or 250 V/µs		500		ns
$t_{CSA\_ON\_DELAY}$	Delay from INLx turn on to current sense amplifier turn on	SR = 50 V/µs		4300		ns
V_{DRIFT}	Drift offset	Phase current = 0 A	–160		160	µA/℃
I_{VREF}	VREF input current	VREF = 3.0 V, nSLEEP = 0 or 1			25	µA
PULSE-BY-PULSE CURRENT LIMIT						
V_{LIM}	Voltage on ILIMIT pin for cycle by cycle current limit		VREF/2		VREF - 0.25	V
V_{LIM_DIS}	Voltage on ILIMIT pin for disabling cycle by cycle current limit		VREF		GVDD	V
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range		0		4	A
I_{LIM_AC}	Current limit accuracy	VREF = 3.3V, ILIMIT > 1A		±6		%
I_{LIM_AC}	Current limit accuracy	VREF = 3.3V, 0.5 A < ILIMIT < 1A		±10		%
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 00b, HW variant		1.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 01b		2.25		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 10b		2.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 00b or 01b or 10b, ILIM_BLANK_SEL = 11b		3.75		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 00b, HW variant		5.5		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 01b		6		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 10b		6.5		µs
t_{BLANK}	Cycle by cycle current limit blank time	SLEW = 11b, ILIM_BLANK_SEL = 11b		7.5		µs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.2	4.35	4.5	V
		VM falling	4.0	4.15	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold		200		mV
t_{UVLO}	Supply undervoltage deglitch time		3	6	10	µs
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	60	62.5	65	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	58	61	63.5	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	32	33	34	V

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 4.5 to 65 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 1		0.8		V
		Rising to falling threshold, OVP_SEL = 0		1.45		V
t_{OVP}	Supply overvoltage deglitch time		2.5	6.5	12	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.1	2.7	3.2	V
		Supply falling	1.8	2.45	2.95	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold		250		mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold		200		mV
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply rising	3.1	3.3	3.5	V
V_{GVDD_UV}	GVDD regulator undervoltage lockout	Supply falling	2.9	3.1	3.3	V
$V_{GVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold		190		mV
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 00b or 01b	4.5			A
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 10b or 11b	2			A
I_{OCP}	Overcurrent protection trip point (HW Device)	OCP pin tied to AGND or OCP pin HiZ	4.5			A
I_{OCP}	Overcurrent protection trip point (HW Device)	OCP tied to GVDD	2			A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.2	0.6	1.2	µs
		OCP_DEG = 01b	0.6	1.25	1.8	µs
		OCP_DEG = 10b	1	1.6	2.5	µs
		OCP_DEG = 11b	1.4	2	3	µs
	Overcurrent protection deglitch time (HW Device)		0.6	1.25	1.8	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
t_{RETRY}	Overcurrent protection retry time (HW Device)		4	5	6	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	160	170	180	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	175	185	195	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	25	30	35	°C

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns

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		MIN	NOM	MAX	UNIT
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

6.7 SPI Slave Mode Timings

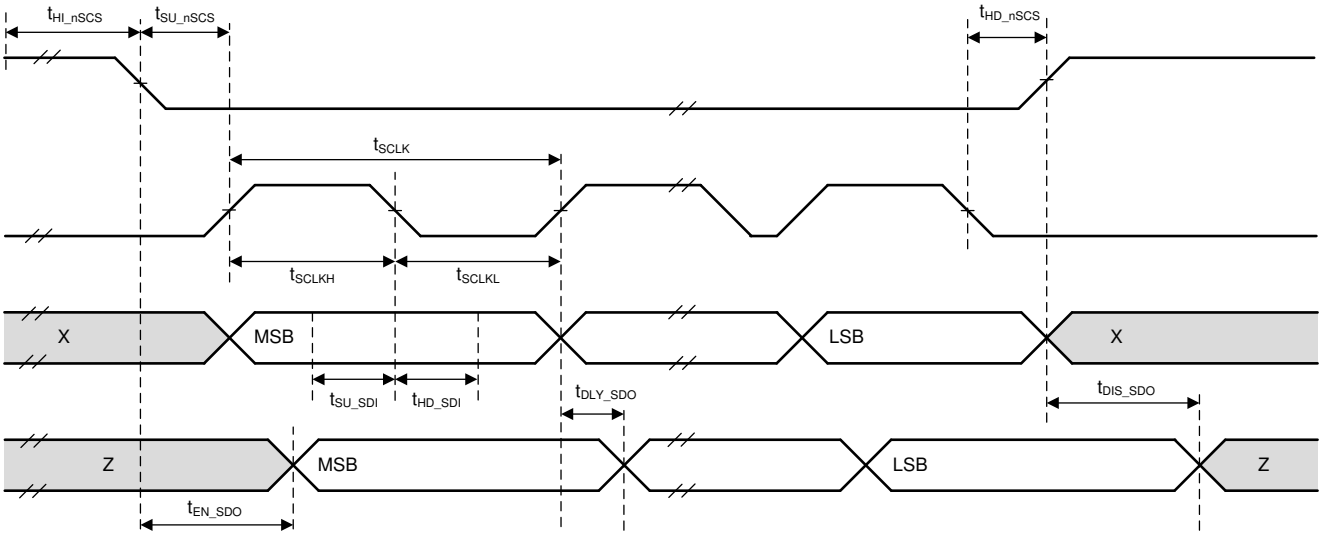


図 6-1. SPI Secondary Mode Timings

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The DRV8376 device is an integrated 400mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, current sense amplifiers, and linear regulator for the external load. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET.

The DRV8376 device integrates three, bidirectional current-sense amplifiers for monitoring the current through each of the low side MOSFET using a built-in current sense. The gain setting of the amplifier can be adjusted through the SPI or hardware interface.

In addition to the high level of device integration, the DRV8376 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD and GVDD undervoltage lockout (AVDD_UV, GVDD_UV), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV8376 device in a VQFN surface-mount package. The VQFN package size is 6 mm × 5 mm.

7.2 Functional Block Diagram

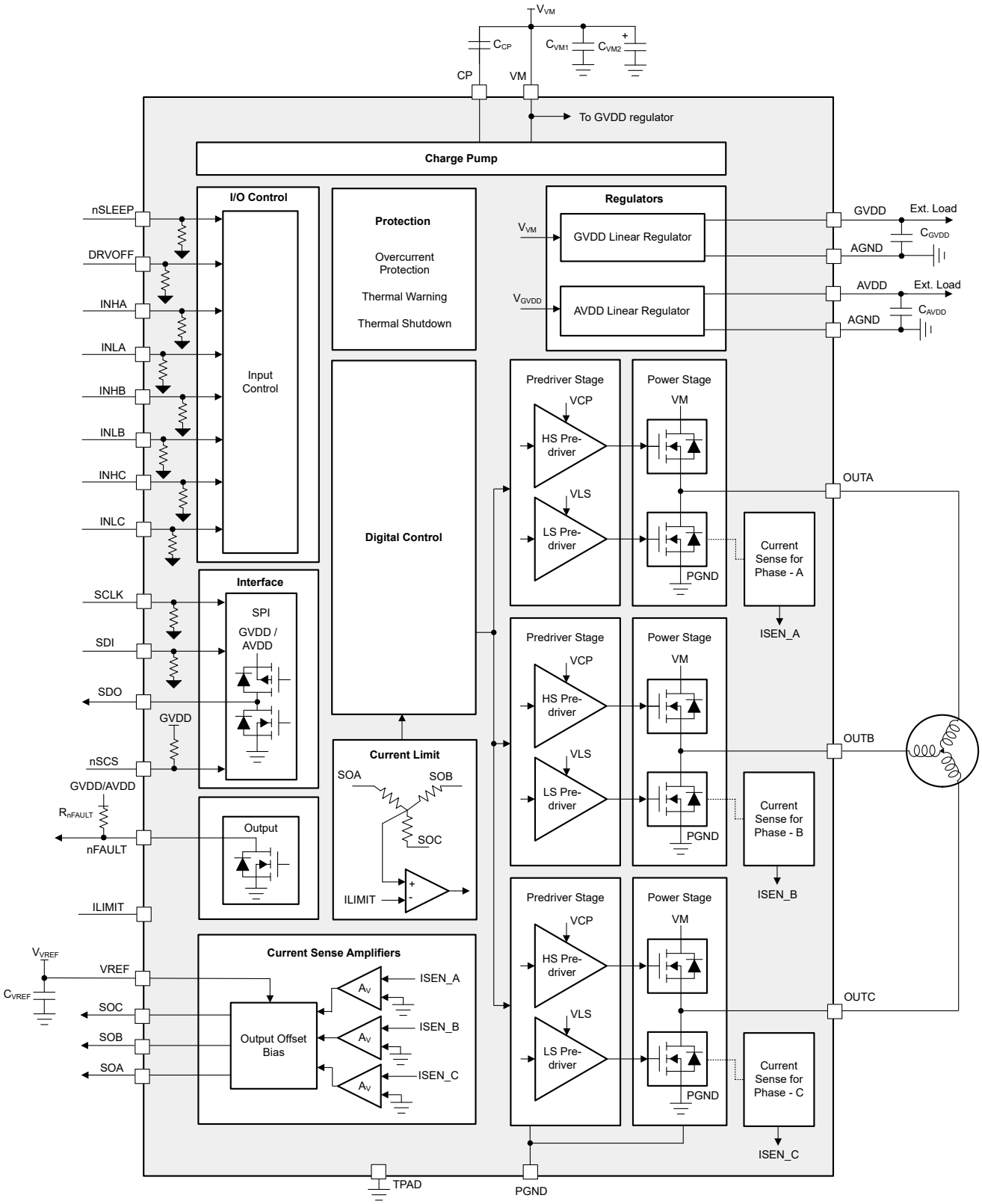


図 7-1. DRV8376S Block Diagram

ADVANCE INFORMATION

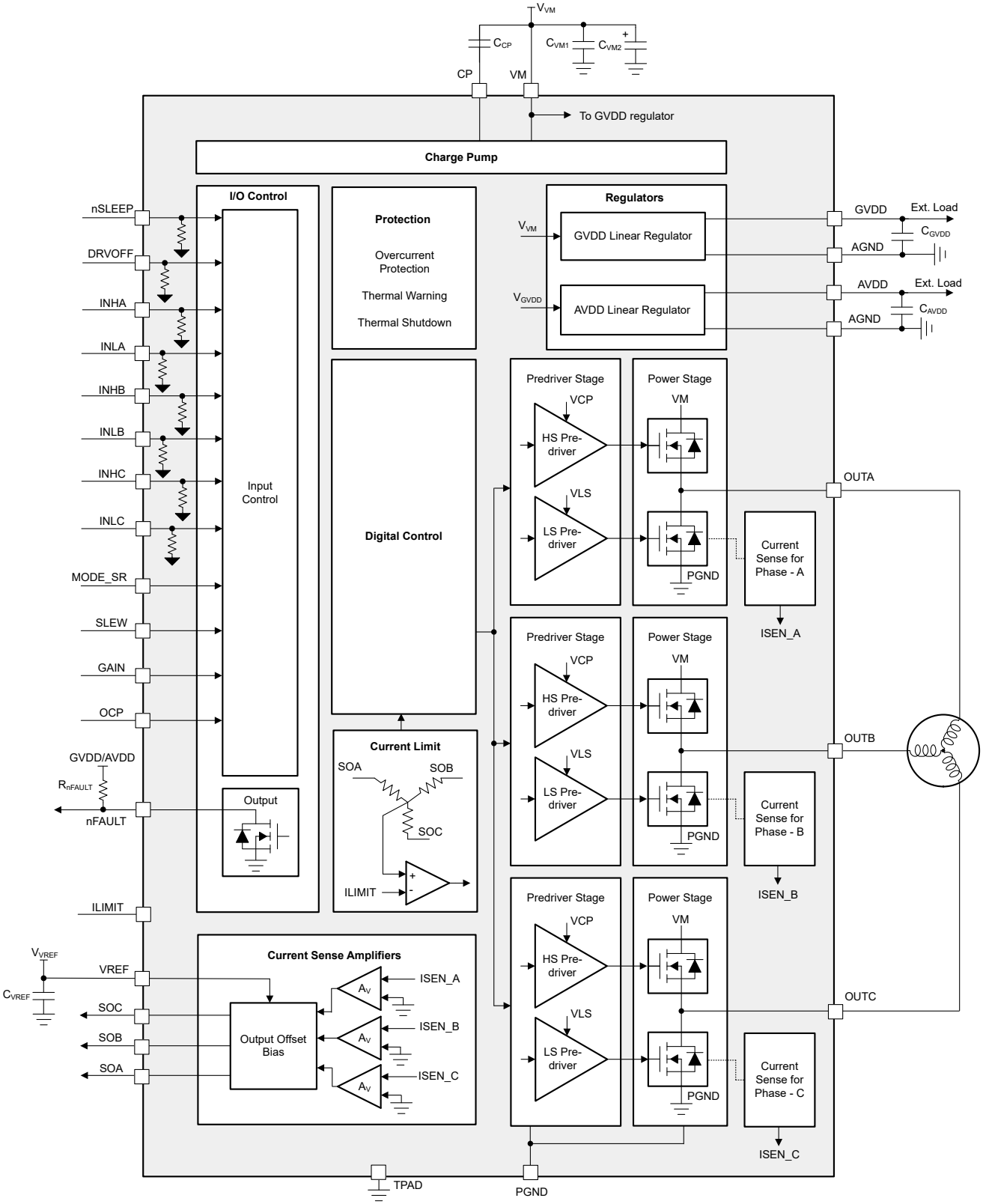


図 7-2. DRV8376H Block Diagram

7.3 Feature Description

表 7-1 lists the recommended values of the external components for the driver.

表 7-1. DRV8376 External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, 16-V, 0.1-µF capacitor
C_{GVDD}	GVDD	AGND	X5R or X7R, 1-µF, ≥ 10-V
C_{AVDD}	AVDD	AGND	X5R or X7R, 0.1-µF, ≥ 6.3-V
R_{nFAULT}	AVDD/GVDD	nFAULT	5.1-kΩ, Pullup resistor
R_{MODE_SR}	MODE_SR	AGND or GVDD	DRV8376H hardware interface
R_{SLEW}	SLEW	AGND or GVDD	DRV8376H hardware interface
R_{OCP}	OCP	AGND or GVDD	DRV8376H hardware interface
R_{GAIN}	GAIN	AGND or GVDD	DRV8376H hardware interface
C_{VREF}	VREF	AGND	X5R or X7R, 0.1-µF, VREF-rated capacitor (Optional)

注

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, ensure that it is pulled to >2.2V on power up.

7.3.1 Output Stage

The DRV8376 device consists of an integrated 400mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FET's across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

ADVANCE INFORMATION

7.3.2 Control Modes

The DRV8376 family of devices provides four different control modes to support various commutation and control methods. 表 7-2 shows the various modes of the DRV8376 device.

表 7-2. PWM Control Modes

MODE Type	MODE_SR Pin (Hardware Variant)	PWM_MODE Bits (SPI Variant)	SR Bits (SPI Variant)	PWM MODE	ASR and AAR Mode
Mode 1	Connected to AGND	PWM_MODE = 00b	EN_ASR = 0, EN_AAR = 0	6x Mode	ASR and AAR Disabled
Mode 2	Hi-Z	PWM_MODE = 01b	EN_ASR = 1, EN_AAR = 1	6x Mode	ASR and AAR Enabled
Mode 3	Connected to GVDD with R_{MODE}	PWM_MODE = 10b	EN_ASR = 0, EN_AAR = 0	3x Mode	ASR and AAR Disabled
Mode 4	Connected to GVDD	PWM_MODE = 11b	EN_ASR = 1, EN_AAR = 1	3x Mode	ASR and AAR Enabled

注

The MODE_SR pin is sensed or PWM_MODE register is read only during power up and the device doesn't support MODE_SR / PWM_MODE change during operation.

7.3.2.1 6x PWM Mode (PWM_MODE = 00b or 01b or MODE_SR Pin Tied to AGND or in Hi-Z)

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in 表 7-3.

表 7-3. 6x PWM Mode Truth Table

INLx	INHx	PHASEx
0	0	Hi-Z
0	1	H
1	0	L
1	1	Hi-Z

図 7-3 shows the application diagram of DRV8376 configured in 6x PWM mode.

ADVANCE INFORMATION

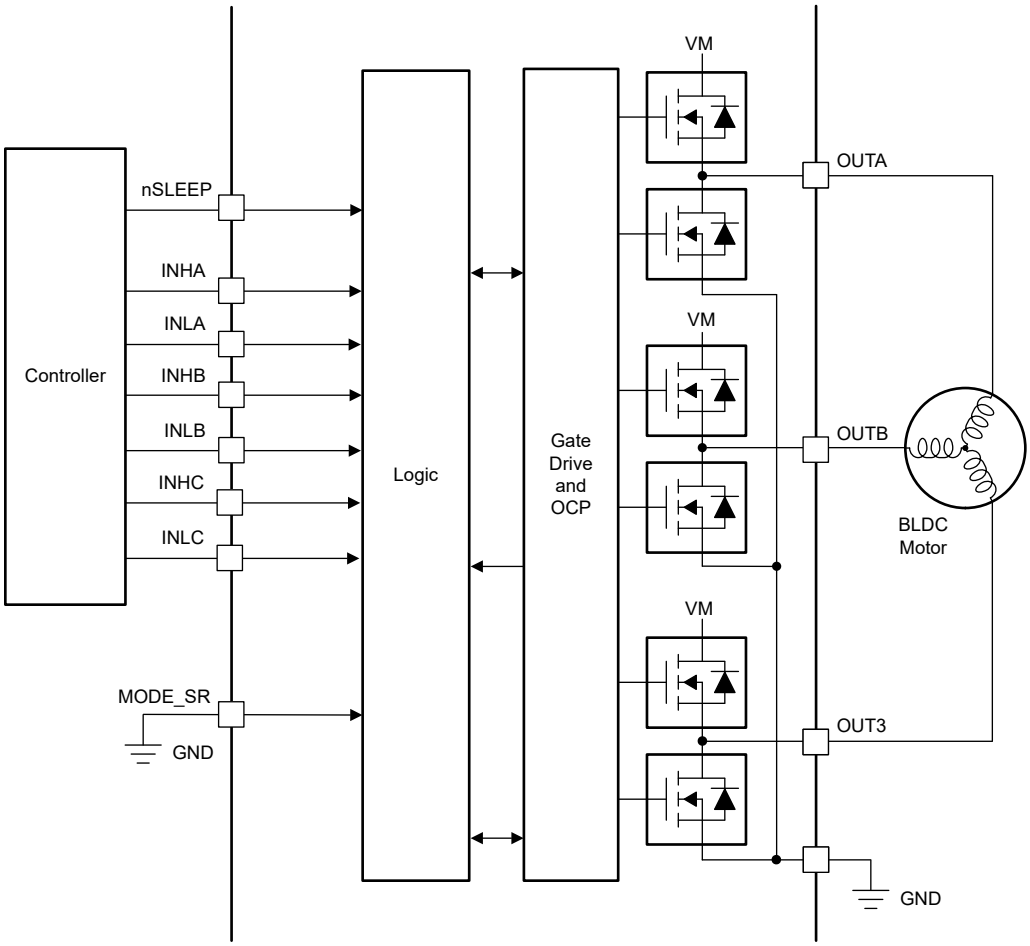


図 7-3. 6x PWM Mode

ADVANCE INFORMATION

7.3.2.2 3x PWM Mode (xPWM_MODE = 10b or 11b or MODE_SR Pin is Connected to GVDD or to GVDD with R_{MODE})

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in 表 7-4.

表 7-4. 3x PWM Mode Truth Table

INLx	INHx	PHASEx
0	X	Hi-Z
1	0	L
1	1	H

図 7-4 shows the application diagram of DRV8376 configured in 3x PWM mode.

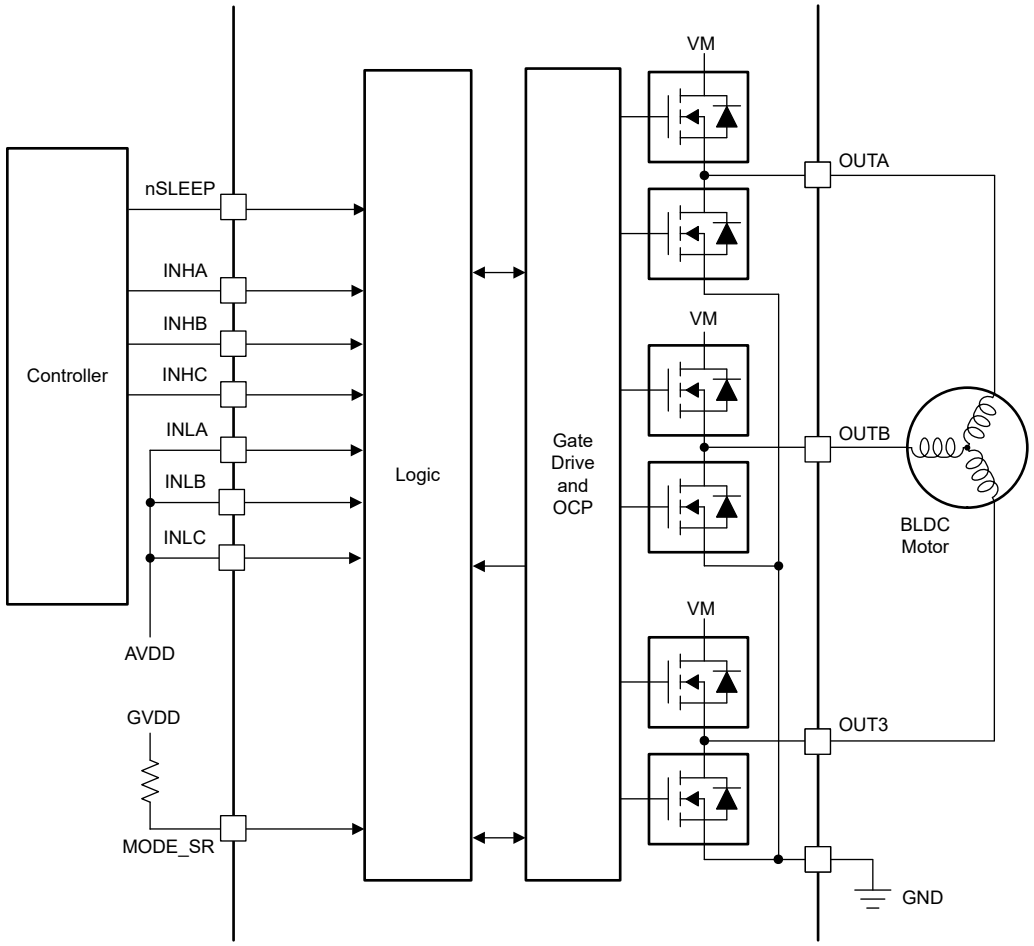


図 7-4. 3x PWM Mode

ADVANCE INFORMATION

7.3.3 Device Interface Modes

The DRV8376 family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate one interface version and potentially switch to another with minimal modifications to their design.

7.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the DRV8376. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin can be configured to either open-drain or push-pull through SDO_MODE.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8376.

For more information on the SPI, see the *セクション 7.5* section.

7.3.3.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are GAIN, SLEW, MODE_SR, and OCP.

The hardware interface lets the application designer to configure the most common device by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the gain of the current sense amplifier.
- The SLEW pin configures the slew rate of the output voltage.
- The MODE_SR pin configures the PWM control mode.
- The OCP pin is used to configures the OCP level.

For more information on the hardware interface, see the *セクション 7.3.9* section.

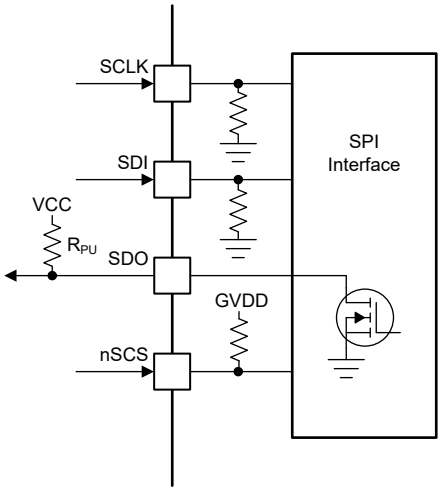


図 7-5. DRV8376S SPI Interface

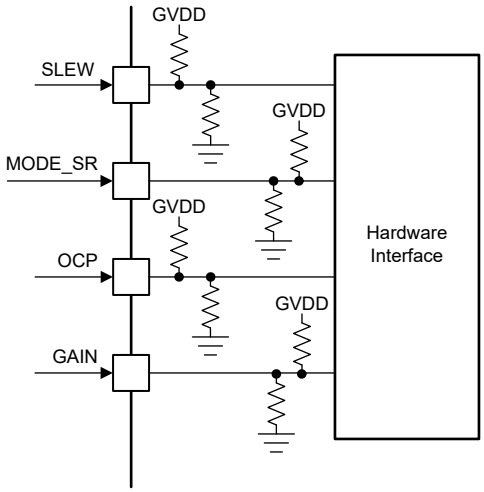


図 7-6. DRV8376H Hardware Interface

ADVANCE INFORMATION

7.3.4 AVDD and GVDD Linear Voltage Regulator

3.3V and 5V linear regulators are integrated into the DRV8376 family of devices and is available for use by external circuitry. The AVDD and GVDD regulators are used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30mA). The output of the AVDD regulator should be bypassed near the AVDD pin with an X5R or X7R, 0.1µF, 6.3V ceramic capacitor routed directly back to the adjacent AGND ground pin. The output of the GVDD regulator should be bypassed near the GVDD pin with an X5R or X7R, 1µF, 10V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

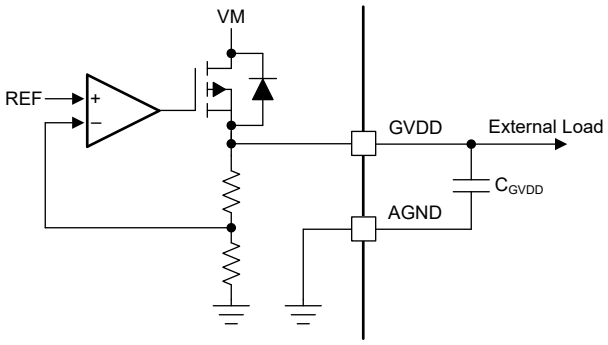


図 7-7. GVDD Linear Regulator Block Diagram

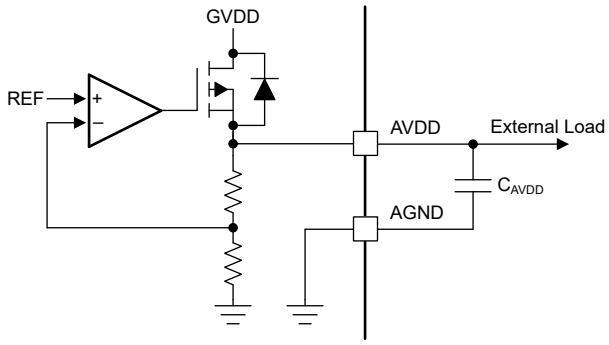


図 7-8. AVDD Linear Regulator Block Diagram

Use 式 1 and 式 2 to calculate the power dissipated in the device by the AVDD and GVDD linear regulator with VM as supply.

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

$$P = (V_{VM} - V_{GVDD}) \times I_{GVDD} \quad (2)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in power dissipation as shown in 式 3.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (3)$$

注

The combined external current support from both the linear regulators AVDD and GVDD is limited to 30mA. If 30mA of external load is connected to AVDD, then do not connect any external load to GVDD and vice versa.

ADVANCE INFORMATION

7.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The DRV8376 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires one external capacitors for operation. See the block diagram, pin descriptions and see section (セクション 7.3) for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low or duing an over temperature shutdown.

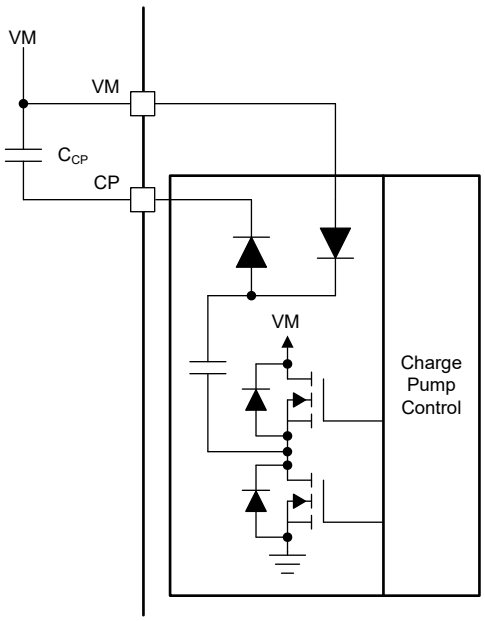


図 7-9. DRV8376 Charge Pump

7.3.6 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in 図 7-10.

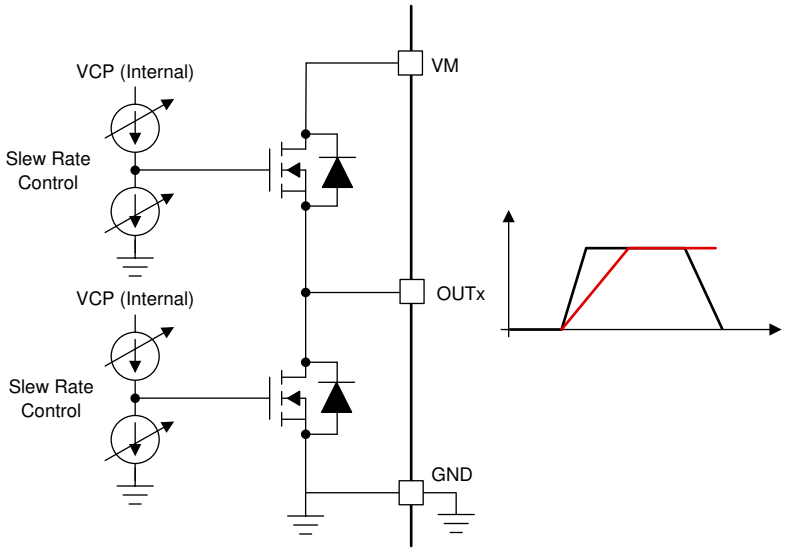


図 7-10. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted by the SLEW pin in the hardware device variant or by using the SLEW bits in the SPI device variant. Each half-bridge can be selected to either of a slew rate setting of 1.1V/ns, 0.5V/ns, 0.25V/ns, or 0.05V/ns. The slew rate is calculated by the rise time and fall time of the voltage on the OUTx pin as shown in 図 7-11.

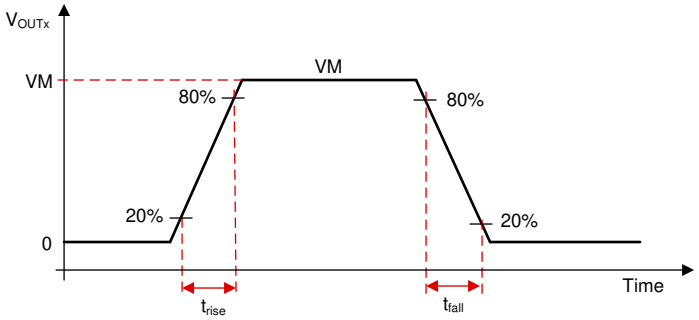


図 7-11. Slew Rate Timings

注

The SLEW pin is sensed only during power up and the DRV8376H device doesn't support slew rate change during operation. Slew rate can be changed during operation through register write in DRV8376S device. TI recommends not to change the slew rate during operation.

7.3.7 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in 図 7-12 and 図 7-13.

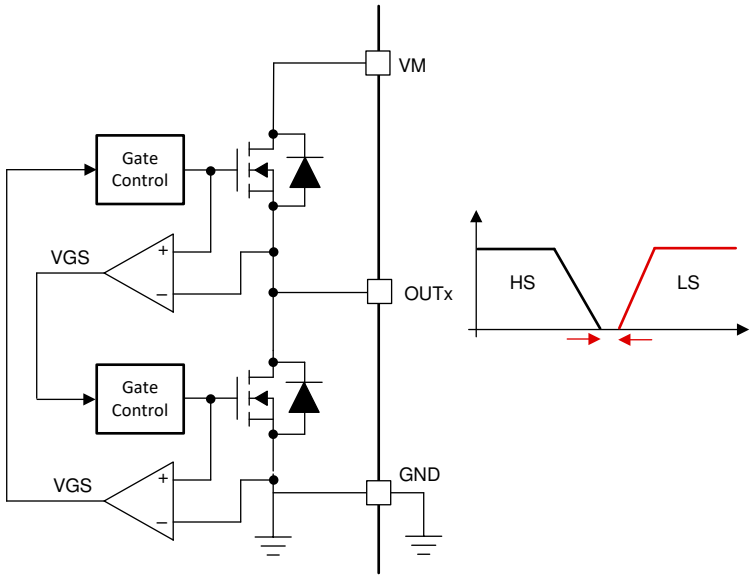


図 7-12. Cross Conduction Protection

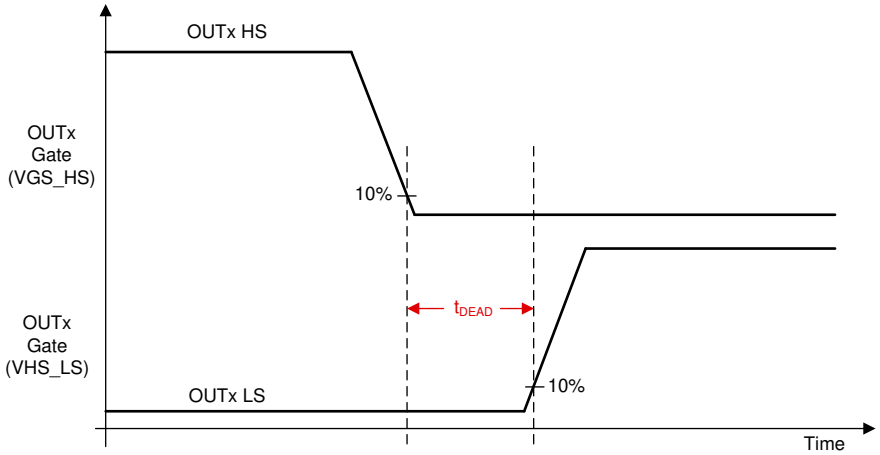


図 7-13. Dead Time

7.3.8 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage.

注

During current limit mode or active demag mode a small digital delay is added as the input command propagates through the device, and user may see upto 300ns more delay during these modes.

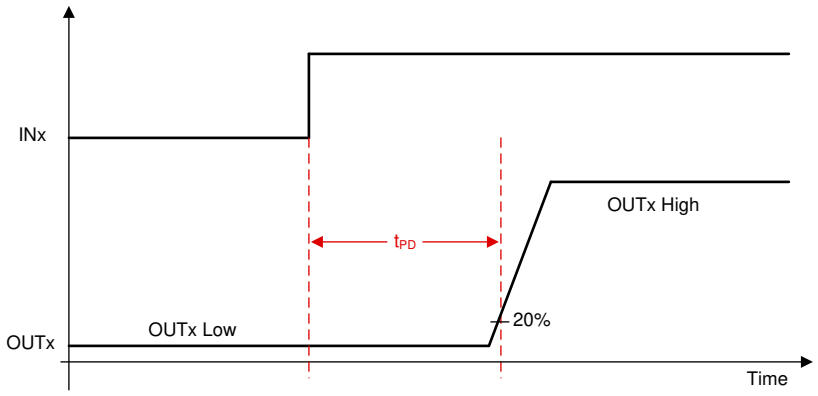


図 7-14. Propagation Delay Timing

7.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

7.3.9.1 Logic Level Input Pin (Internal Pulldown)

図 7-15 shows the input structure for the logic level pins, DRVOFF, INHx, INLx, nSLEEP, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

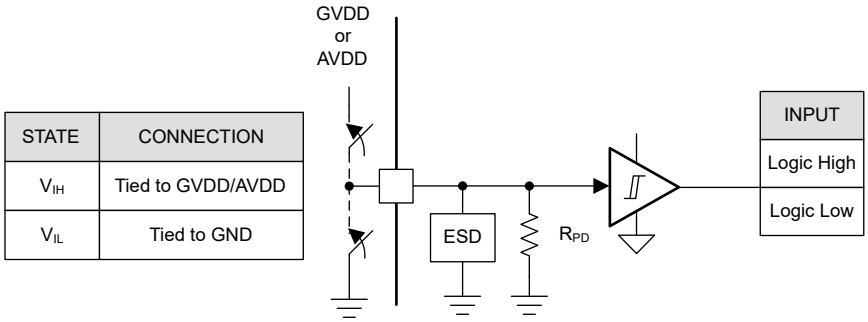
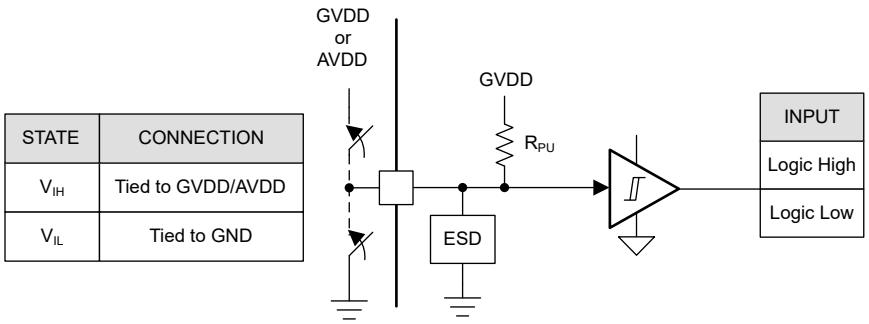


図 7-15. Logic-Level Input Pin Structure

7.3.9.2 Logic Level Input Pin (Internal Pullup)

図 7-16 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

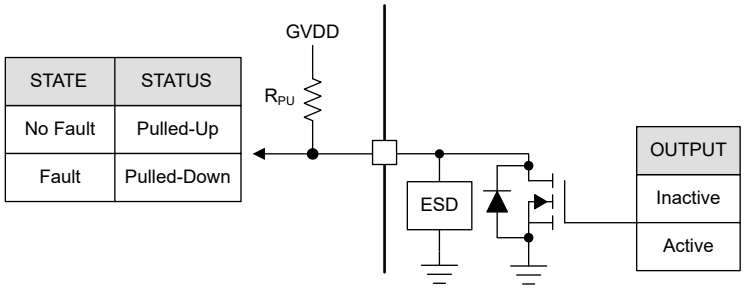


STATE	CONNECTION
V_{IH}	Tied to GVDD/AVDD
V_{IL}	Tied to GND

図 7-16. Logic nSCS

7.3.9.3 Open Drain Pin

図 7-17 shows the structure of the open-drain output pin, nFAULT and SDO in open drain mode. The open-drain output requires an external pullup resistor to function properly.

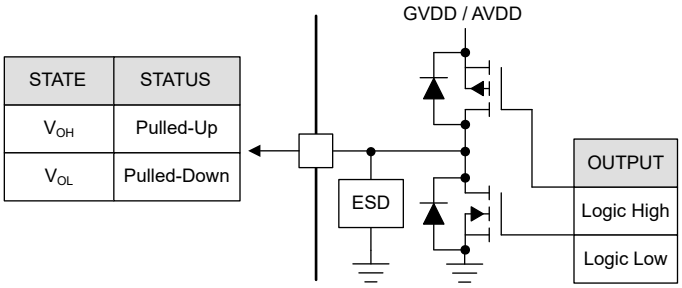


STATE	STATUS
No Fault	Pulled-Up
Fault	Pulled-Down

図 7-17. Open Drain

7.3.9.4 Push Pull Pin

図 7-18 shows the structure of SDO in push-pull mode. The SDO power supply in push pull mode can be selected to GVDD or AVDD by configuring SDO_VSEL.



STATE	STATUS
V_{OH}	Pulled-Up
V_{OL}	Pulled-Down

図 7-18. Push Pull

7.3.9.5 Four Level Input Pin

図 7-19 shows the structure of the four level input pins, GAIN, MODE,_SR, SLEW, and OCP on hardware interface devices. The input can be set with an external resistor.

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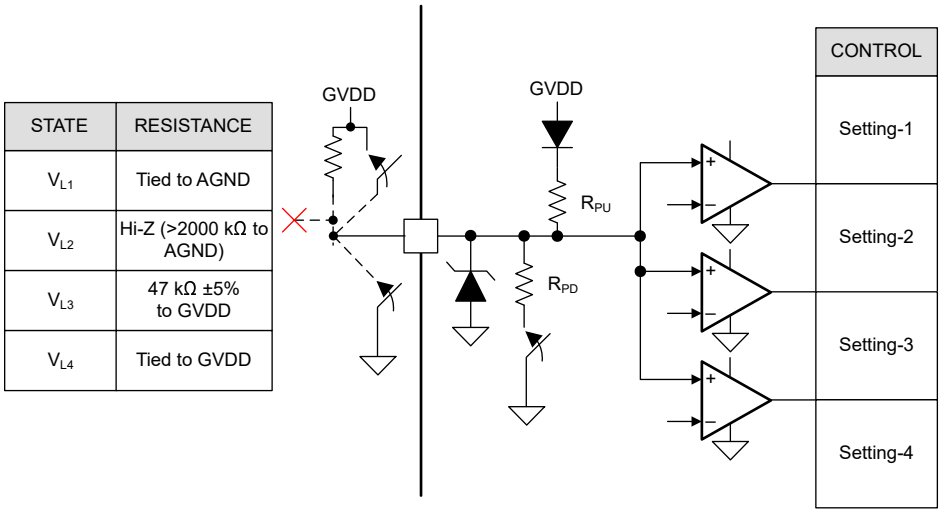

図 7-19. Four Level Input Pin Structure

7.3.10 Current Sense Amplifiers

The DRV8376 integrates three, high-performance low-side current sense amplifiers for current measurements using built-in current sensing. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless-DC commutation with an external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs (low-side FETs). The current sense amplifiers include features such as programmable gain and external reference is provided on a voltage reference pin (VREF).

7.3.10.1 Current Sense Amplifier Operation

The SOx pin on the DRV8376 outputs an analog voltage proportional to the current flowing in the low-side FETs multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels which can be set by the GAIN pin (in the hardware device variant) or the GAIN bits (in the SPI device variant).

図 7-20 shows the internal architecture of the current sense amplifiers. The current sense is implemented with the sense FET on each low-side FET of the DRV8376 device. This current information is fed to the internal I/V converter, which generates the CSA output voltage on the SOX pin based on the voltage on the VREF pin and the Gain setting. The CSA output voltage can be calculated as :

$$SOX = \left({}^{V_{REF}}/_{2}\right) \pm GAIN \times I_{OUTX} \quad (4)$$

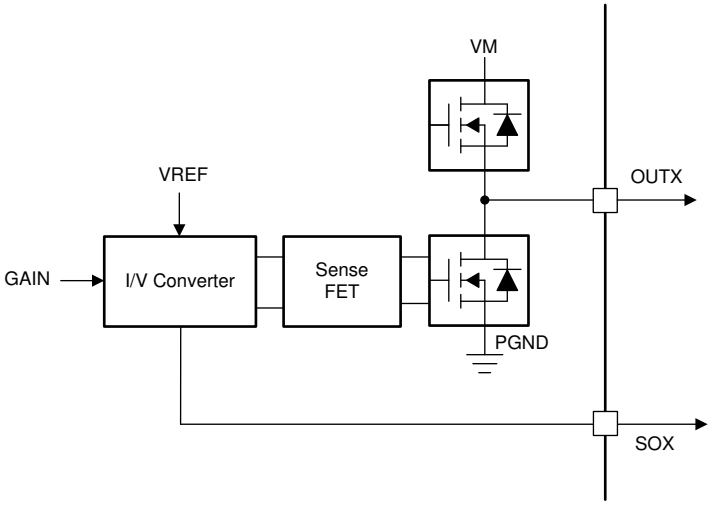

図 7-20. Integrated Current Sense Amplifier

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図 7-21 and 図 7-22 show the detail of the amplifier operational range. In bi-directional operation, the amplifier output for 0V input is set at VREF/2. Any change in the differential input results in a corresponding change in the output times the CSA_GAIN factor. The amplifier has a defined linear region in which it can maintain operation.

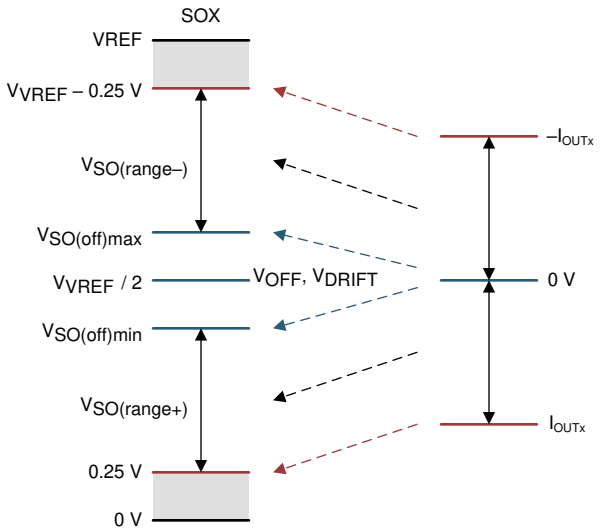

図 7-21. Bidirectional Current Sense Output

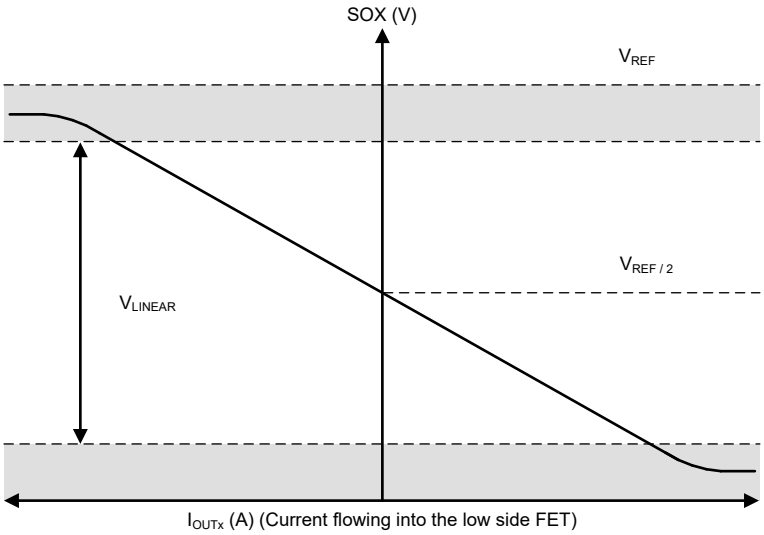

図 7-22. Bidirectional Current Sense Regions

注

The current sense amplifier supports only capacitive load at the output. TI recommends connecting the low pass filter with the resistor and capacitor on the output of the current sense amplifier.

注

The current sense amplifier supports dynamic gain change. The GAIN is sampled every 1ms through pin sensing in the HW variant and any GAIN change through SPI write (in the SPI variant). After receiving the GAIN change command, the new GAIN will be applied to all three current sense amplifiers on the next falling edge of any INLx signal.

7.3.11 Active Demagnetization

DRV8376 family of devices has smart rectification features (active demagnetization) which decreases power losses in the device by reducing diode conduction losses. When this feature is enabled, the device automatically turns ON the corresponding MOSFET whenever it detects diode conduction. This feature can be configured with the MODE_SR pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in the sections below.

注

In SPI device variants both bits, EN_ASR and EN_AAR need to be set to 1 to enable active demagnetization.

The DRV8376 device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS comparator compares with the ground (0V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization features.

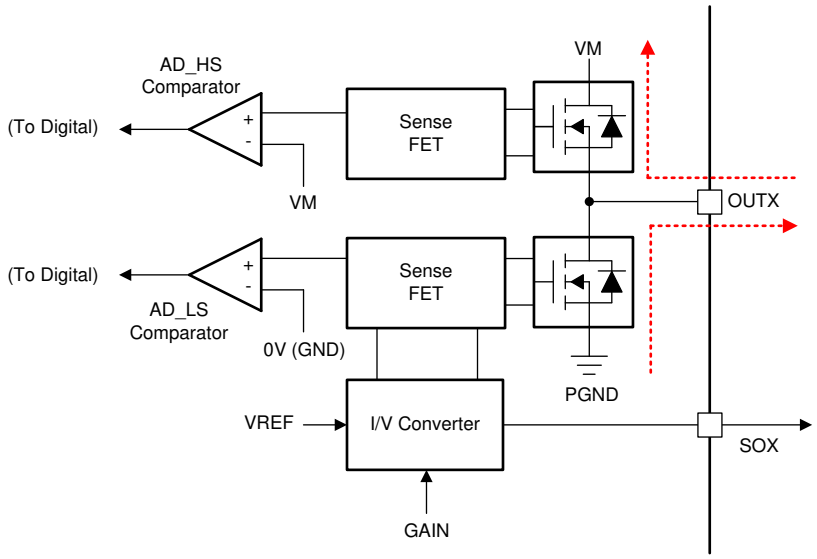

図 7-23. Active Demagnetization Operation

表 7-2 shows the configuration of ASR and AAR mode in the DRV8376 device.

注

Active demagnetization disabled on an OCP event .

7.3.11.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

7.3.11.1.1 Automatic Synchronous Rectification in Commutation

図 7-24 shows the operation of active demagnetization during the BLDC motor commutation. As shown in 図 7-24 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in 図 7-24 (b), the HB switch is turned on, whereas the commutation current (due to motor inductance) in

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OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in 図 7-24 (c).

Similarly the operation of high-side FET is realized in 図 7-24 (d), (e) and (f).

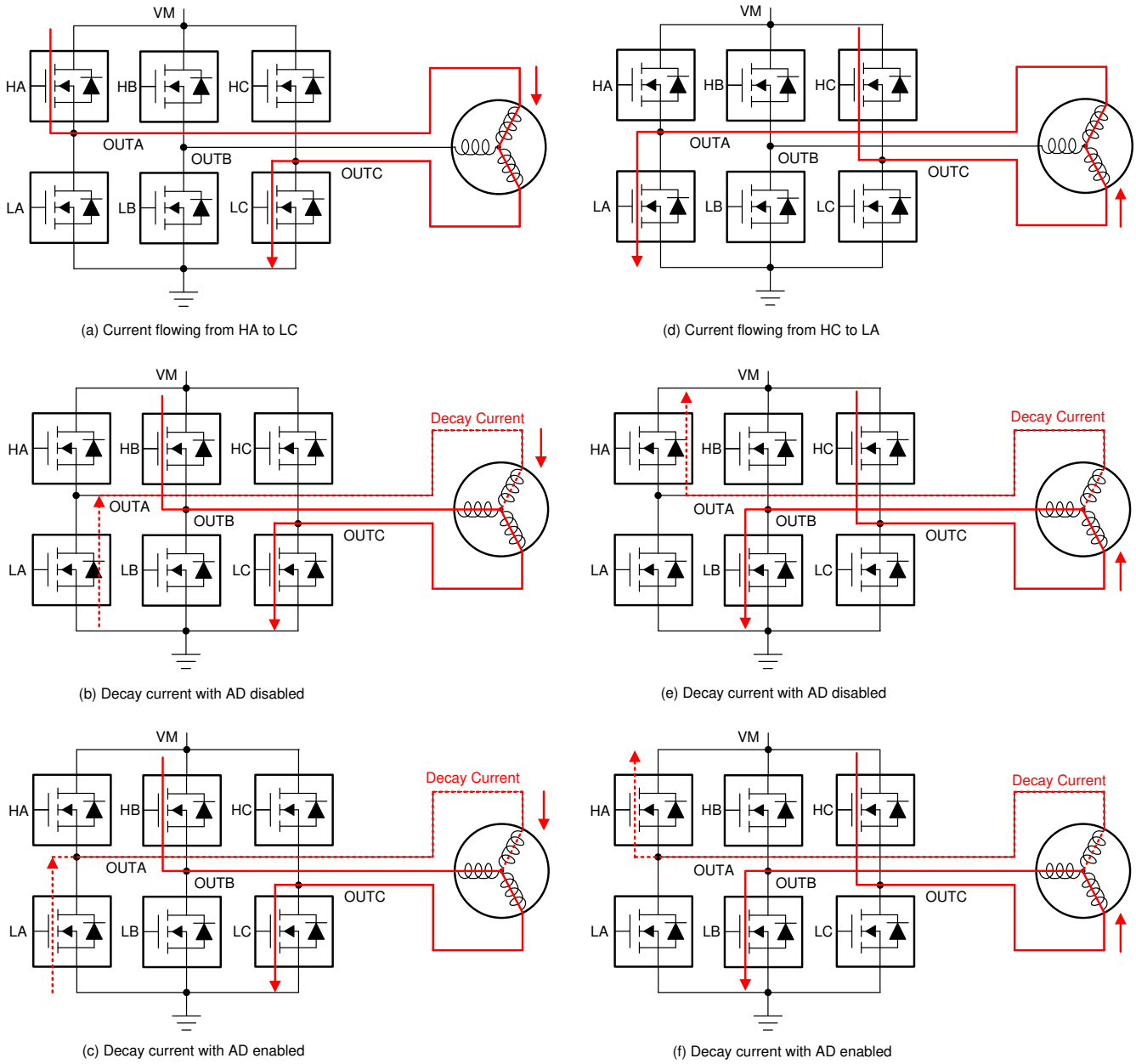
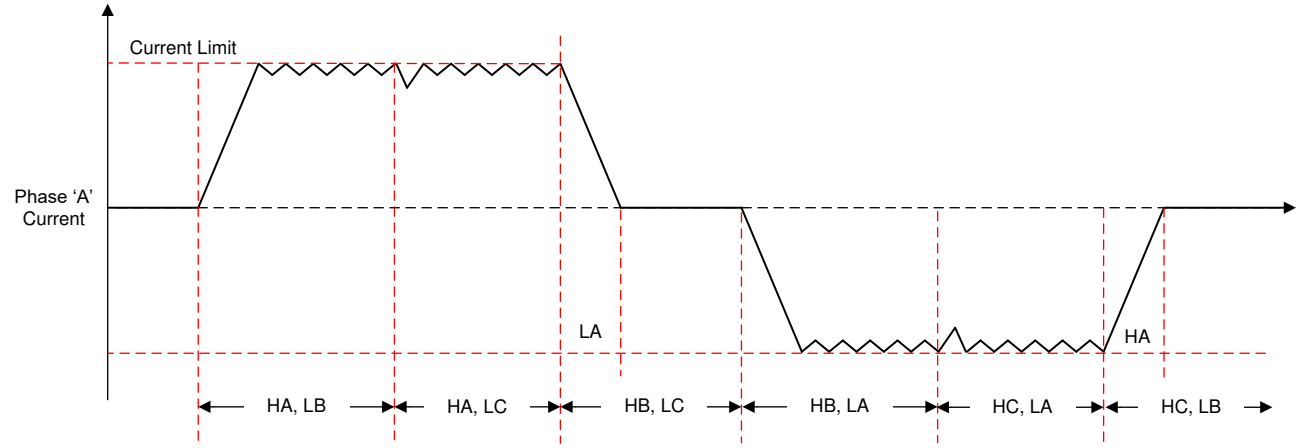


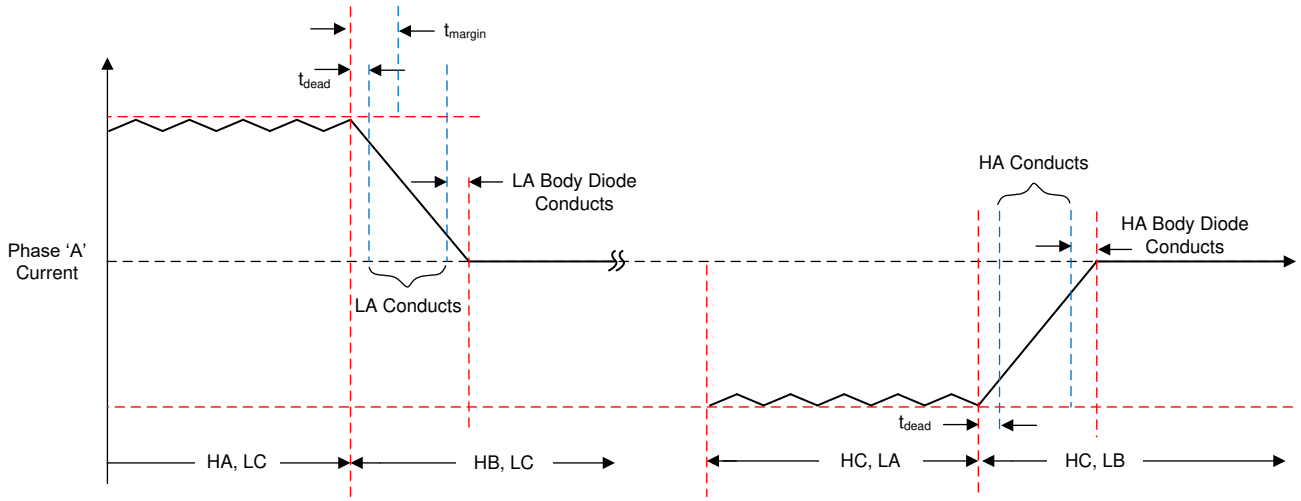
図 7-24. ASR in BLDC Motor Commutation

図 7-25 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

図 7-25 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demag. comparator threshold and delays.



(a) Commutation current of Phase "A"



(b) Zoomed waveform of Active Demagnetization

図 7-25. Current Waveforms for ASR in BLDC Motor Commutation

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7.3.11.1.2 Automatic Synchronous Rectification in PWM Mode

図 7-26 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

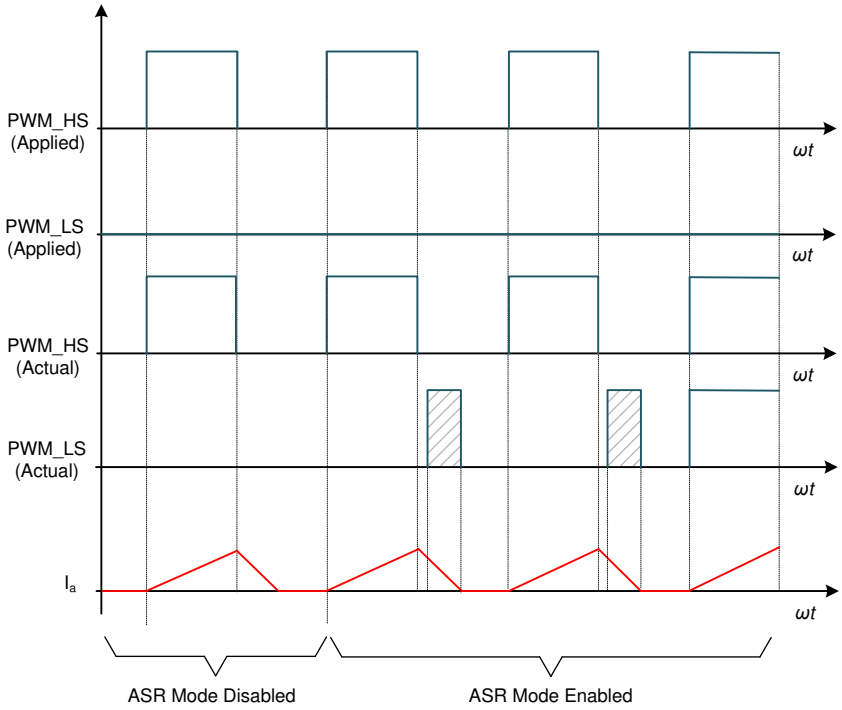

図 7-26. ASR in PWM Mode

7.3.11.2 Automatic Asynchronous Rectification Mode (AAR Mode)

図 7-27 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

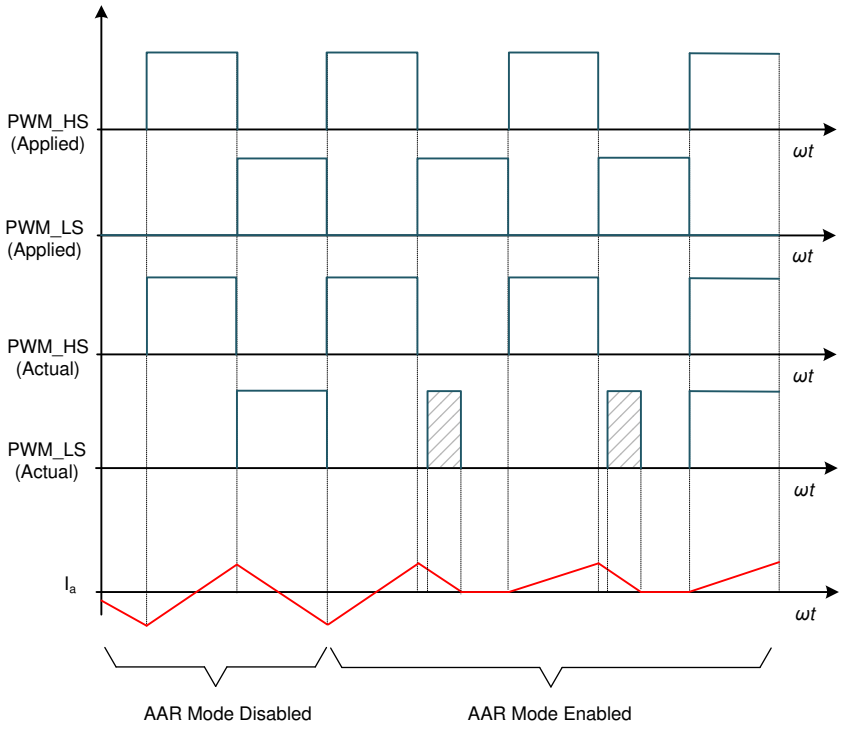

図 7-27. AAR in PWM Mode

7.3.12 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFET exceeds the I_{LIMIT} current. This feature restricts motor current to less than the I_{LIMIT}.

The current-limit circuitry utilizes the current sense amplifier output of the three phases compared with the voltage at ILIMIT pin. 図 7-28 shows the implementation of current limit circuitry, the output of current sense amplifiers are combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage V_{ILIMIT} pin to realize the current limit implementation. The relation between current sensed on OUTX pin and V_{MEAS} threshold is given as:

$$V_{MEAS} = \left({}^{V_{VREF}}/_{2}\right) - ((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3) \quad (5)$$

where

- $V_{VREF}$is the current sense amplifier supply
- I_{OUTX} is current flowing into the low-side MOSFET
- CSA_GAIN is the current sense amplifier gain

The I_{LIMIT} threshold can be adjusted by configuring the voltage at ILIMIT pin. ILIMIT varies linearly between 0A to 4A, as the voltage at ILIMIT pin varies from V_{REF}/2 to V_{MEAS}. A voltage more than V_{REF}/2 can be applied to disable ILIMIT.

Current limit comparator output is blanked for a blanking time, on every rising edge of high side and low side switch control input (INHx and INLx) and the DRV8376 output state depends on the INHx and INLx status during blanking time. The blanking time is configured through ILIM_BLANK_SEL in SPI device and the blanking time is fixed to 5.5 us for slew rate of 50 and 1.8us for all other slew rates in hardware variant.

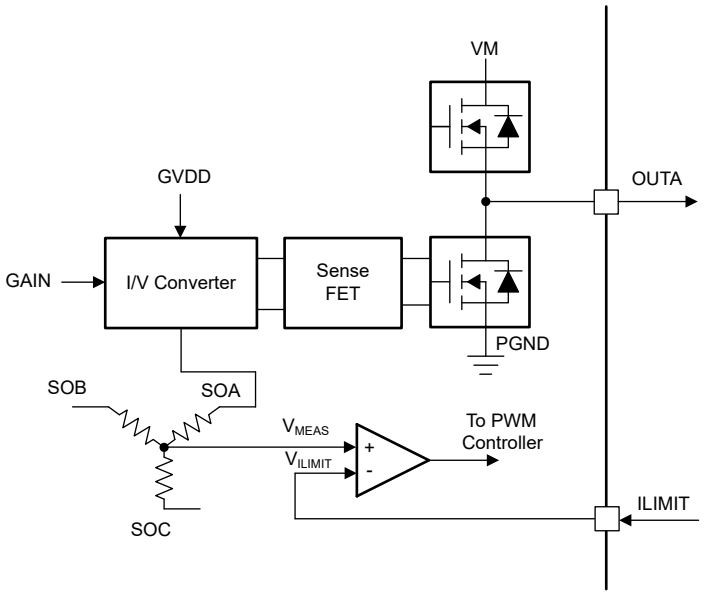

図 7-28. Current Limit Implementation

When then the current limit activates, the high-side FET of each half bride is disabled until the rising edge of the high side (INHx) of that half bridge as shown in 図 7-29. The low-side FETs can operate in brake mode or Coast (high-Z) mode by configuring the ILIM_MODE bit in the SPI device variant. The low-side FETs operate in Coast (high-Z) mode in the hardware variant.

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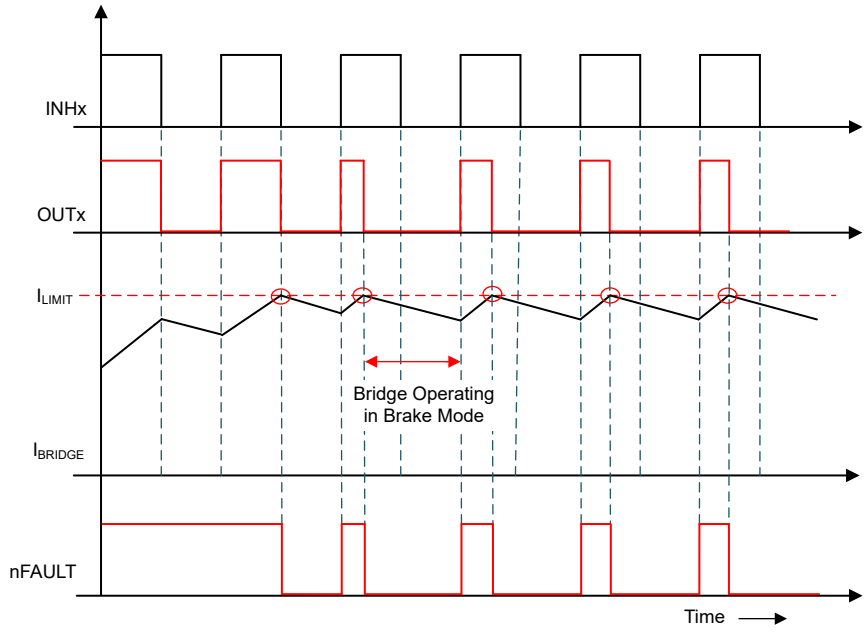

図 7-29. Cycle-by-Cycle Current-Limit Operation

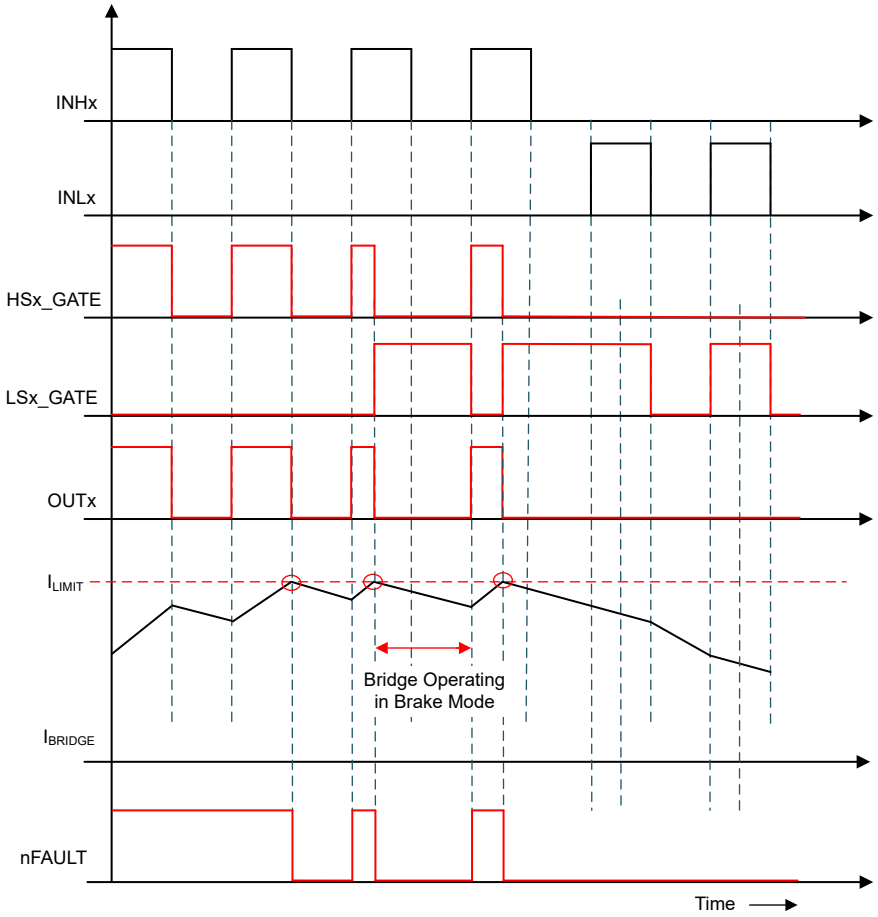

図 7-30. Cycle-by-Cycle Current-Limit Operation with Low Side Switching in Brake Mode

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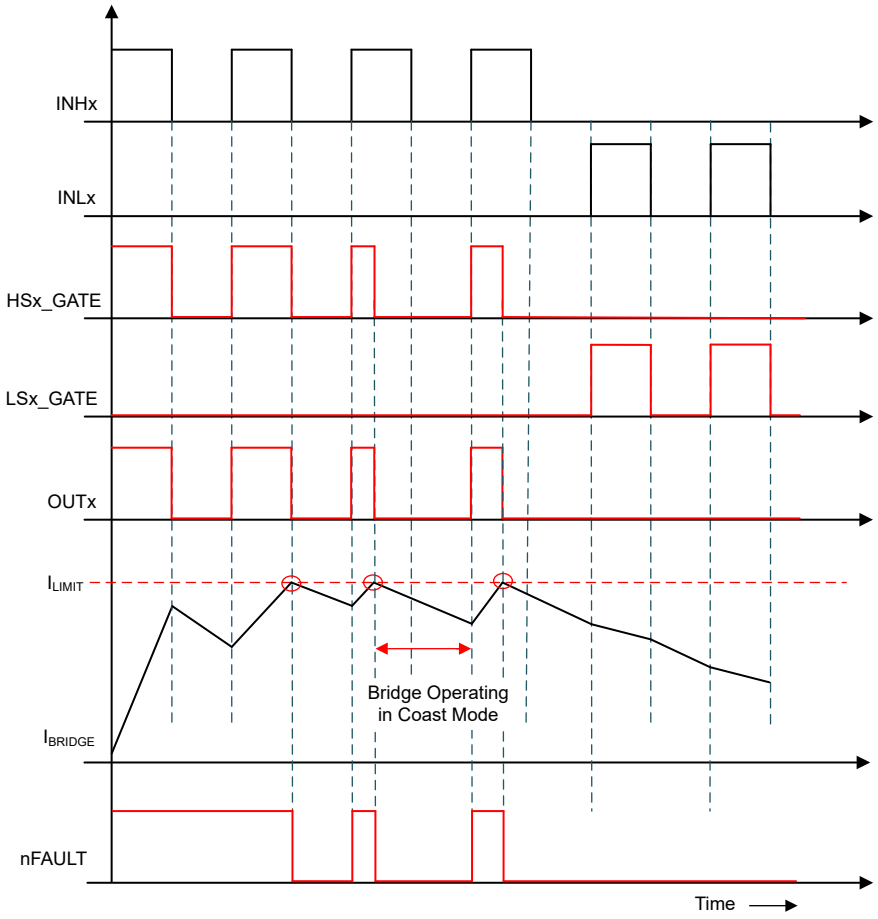

図 7-31. Cycle-by-Cycle Current-Limit Operation with Low Side Switching in Coast Mode

図 7-32 shows the operation of driver in brake mode, where the current recirculates through low-side FETs while the high-side FETs are disabled.

図 7-33 shows the operation of driver in hi-Z mode, where the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled.

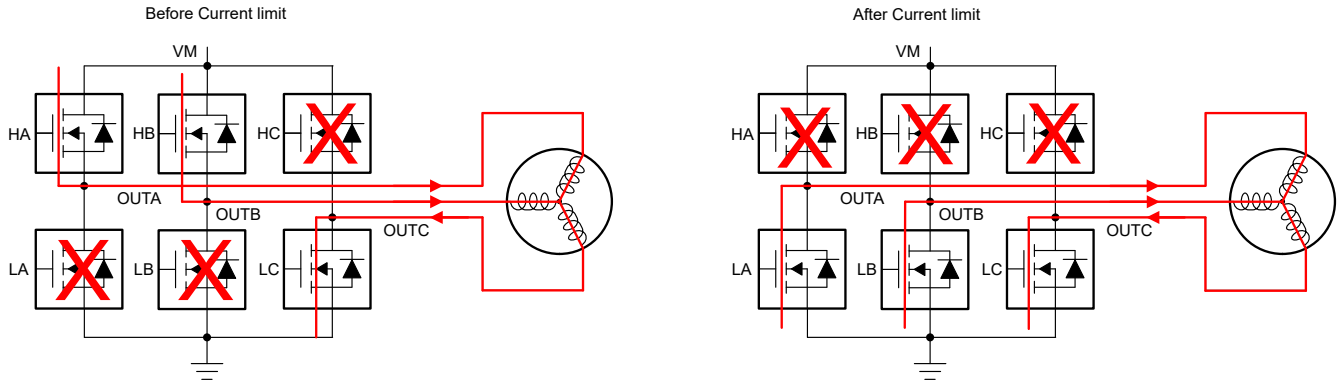

図 7-32. Brake State

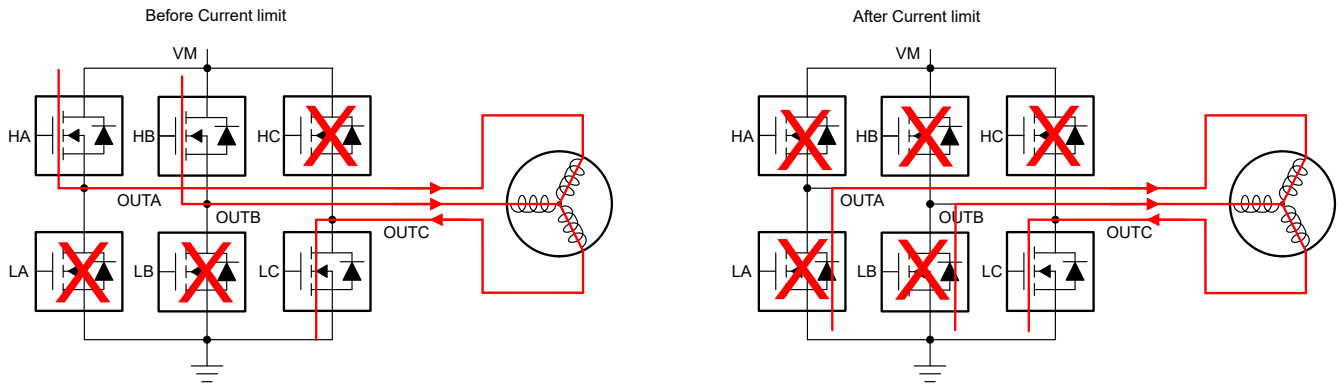

図 7-33. Coast State

注

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

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7.3.12.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, DRV8376 has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant DRV8376, this internal PWM clock can be configured to either 10 kHz or 20 kHz or 40 kHz through PWM_100_DUTY_SEL. In H/W variant DRV8376 PWM internal clock is set to 20 kHz. 図 7-34 shows operation with 100 % duty cycle.

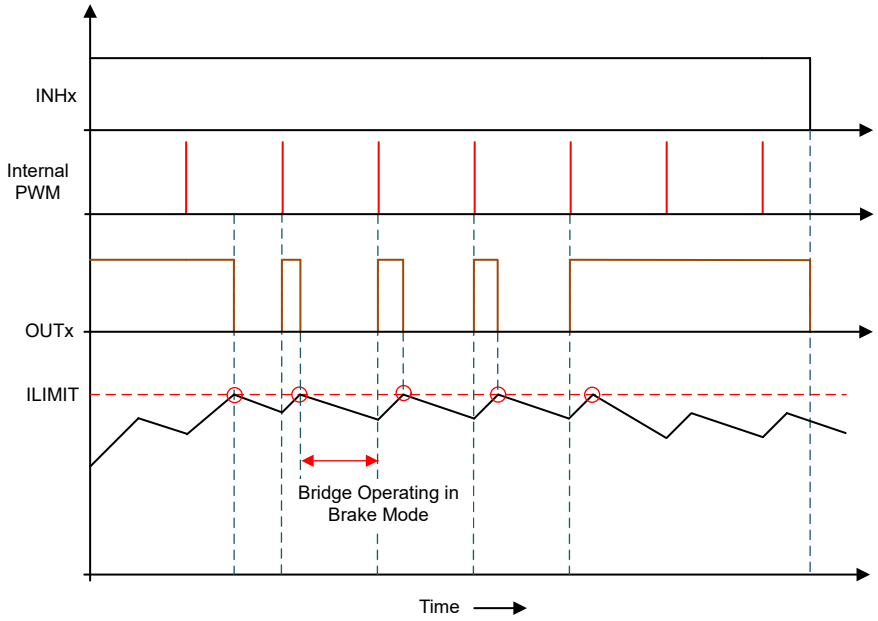

図 7-34. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

7.3.13 Protections

The DRV8376 family of devices is protected against VM undervoltage, charge pump undervoltage, and overcurrent events. 表 7-5 summarizes various faults details.

表 7-5. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (RESET)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
GVDD undervoltage (RESET)	$V_{GVDD} < V_{GVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{GVDD} > V_{GVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
AVDD undervoltage (RESET)	$V_{AVDD} < V_{AVDD\_UV}$	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (RESET bit)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_MODE = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_MODE = 1b	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY} CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 10b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
ILIMIT	$V_{ILIMIT} > V_{SO}$	ILIMFLT_MODE = 0b	None	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
		ILIMFLT_MODE = 1b	nFAULT	ILIMIT Mode	Active	Automatic: High side on the next rising edge of INHx Low side on the next rising edge of INLx
SPI Error (SPI_FLT)	SCLK, Parity and ADDR fault	SPIFLT_MODE = 0b	None	Active	Active	No action
		SPIFLT_MODE = 1b	nFAULT	Active	Active	Report only: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, CLR_FLT
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_MODE = 0b	None	Active	Active	No action
		OTW_MODE = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD)	$T_J > T_{TSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$

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7.3.13.1 VM Supply Undervoltage Lockout (RESET)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in 図 7-35. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

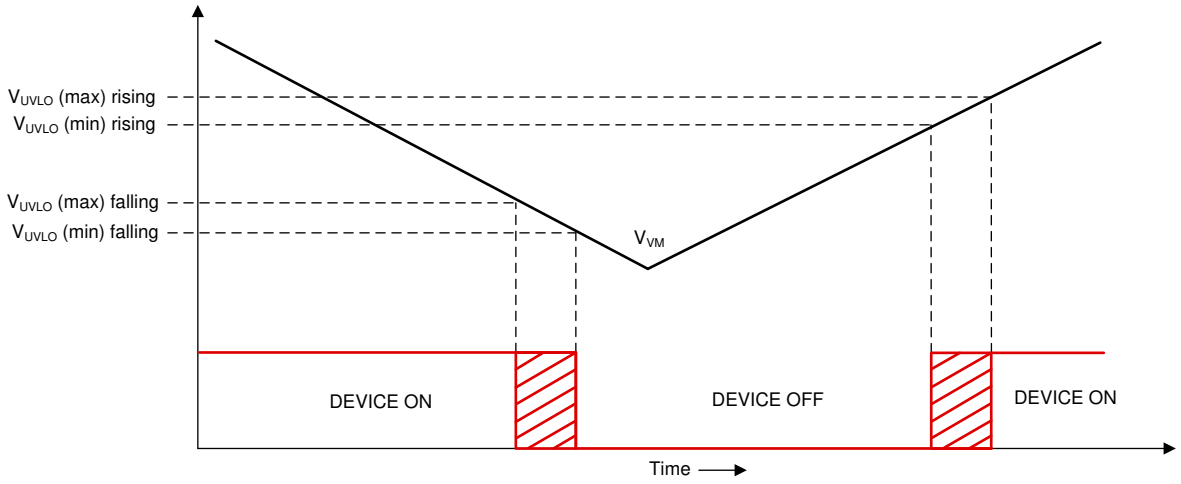

図 7-35. VM Supply Undervoltage Lockout

7.3.13.2 AVDD Undervoltage Protection (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

7.3.13.3 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on GVDD pin falls lower than the V_{GVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the GVDD undervoltage condition is removed. The RESET bit is latched high in the device status (DEV_STS) register once the device presumes VM. The RESET bit remains high until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

7.3.13.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The charge pump undervoltage is reported on FAULT and CPUV bits. FAULT bit will be autocleared when charge pump undervoltage condition is removed. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

7.3.13.5 Overvoltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The undervoltage is reported on FAULT and OVP bits. FAULT bit will be autocleared when over voltage condition is removed. The OVP bit stays set until

cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). Setting the OVP_MODE bit high on the SPI devices enables this protection feature. On hardware interface devices, the OVP protection is disabled.

The OVP threshold is also programmable on the SPI device variant. The OVP threshold can be set to 35-V or 65-V based on the OVP_SEL bit.

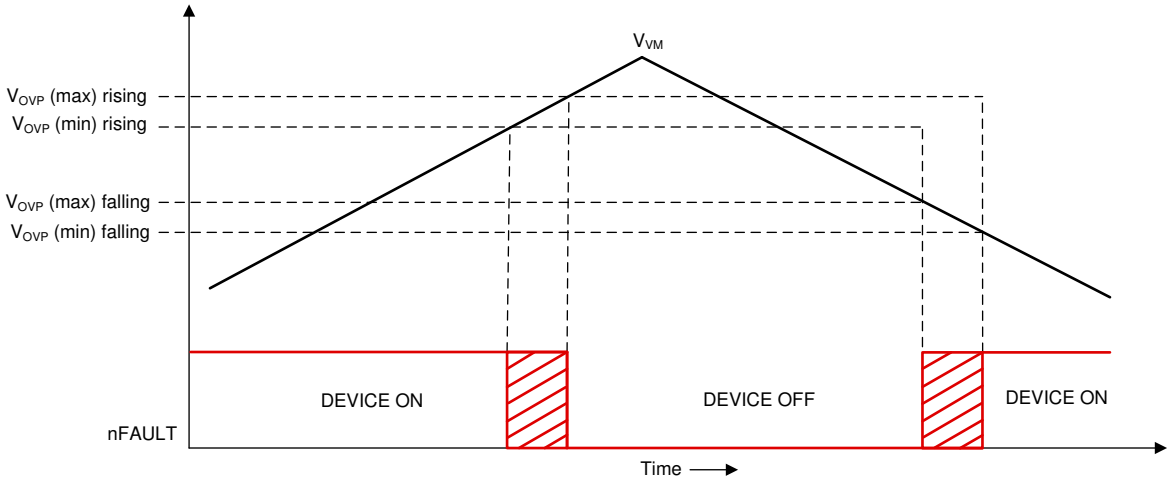

図 7-36. Over Voltage Protection

7.3.13.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current through a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is set via OCP pin, the t_{OCP_DEG} is fixed at 1.2-µs, and the OCP_MODE bit is configured for latched shutdown. On SPI devices, the I_{OCP} threshold is set through the OCP_LVL bits, the t_{OCP_DEG} is set through the OCP_DEG bits.

表 7-6 shows the configuration of OCP level and deglitch time in the DRV8376 device.

表 7-6. OCP Configuration

OCP Setting	OCP Pin (Hardware Variant)	OCP_LVL bits (SPI variant)	Minimum OCP Level
OCP 1	Connected to AGND	OCP_LVL= 0b	4.5-A
OCP 2	Connected to GVDD	OCP_LVL= 1b	2-A

The OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

7.3.13.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

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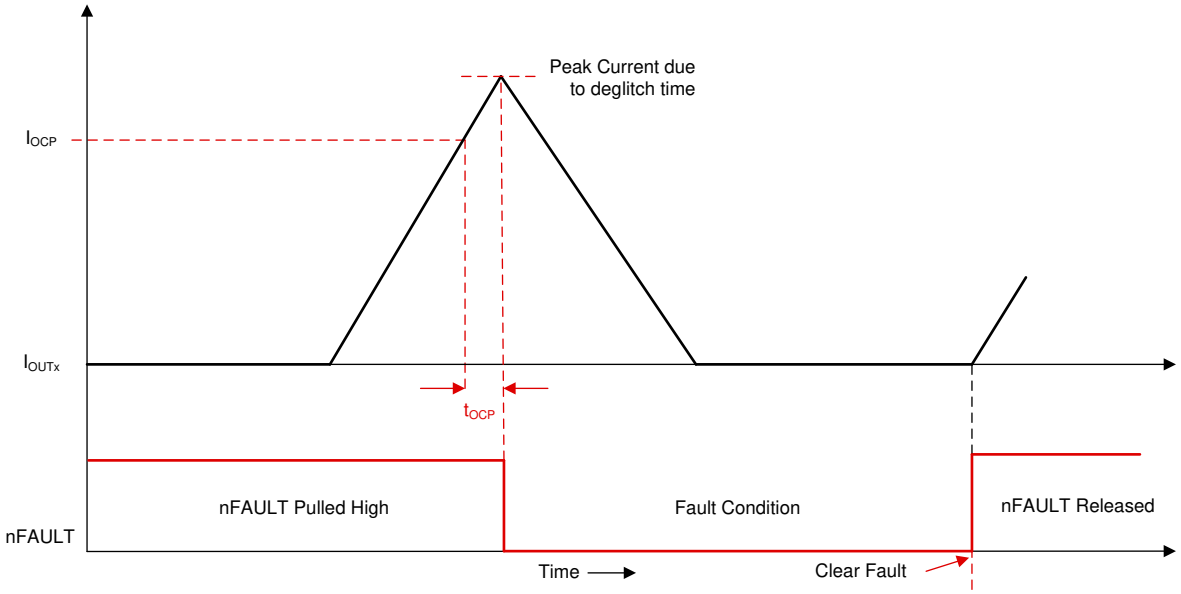

図 7-37. Overcurrent Protection - Latched Shutdown Mode

7.3.13.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

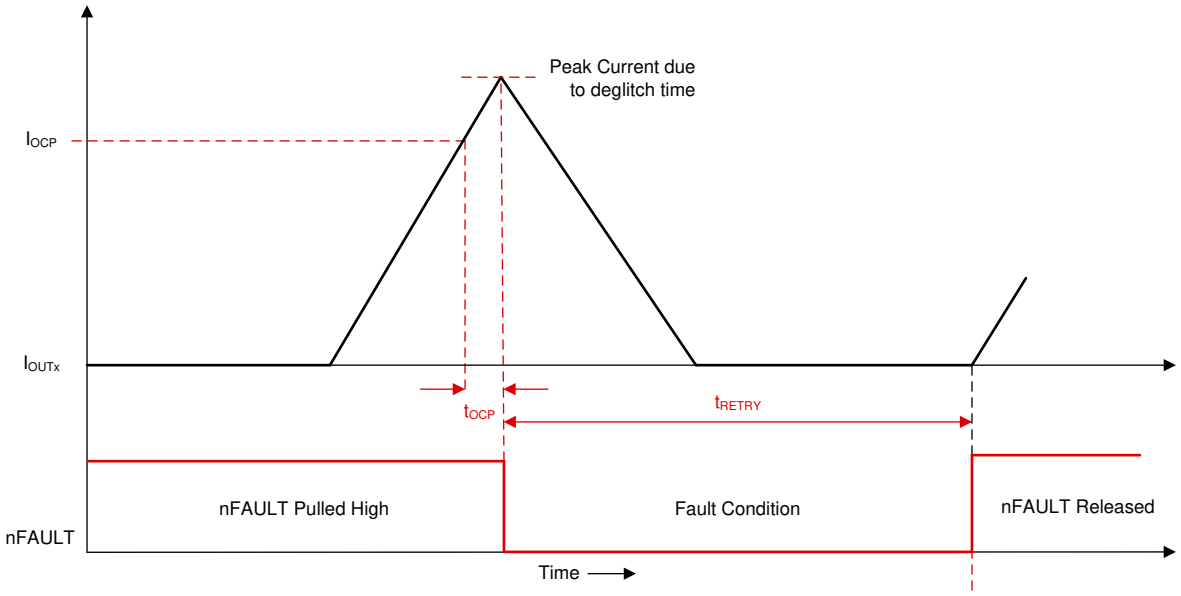

図 7-38. Overcurrent Protection - Automatic Retry Mode

7.3.13.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The

DRV8376 continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.13.6.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

7.3.13.7 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the OT status (OT_STS) register and and OTF bit in the status register (DEV_STS) is set.. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_MODE) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}). In hardware variant the over temperature warning is reported on nFAULT pin by default.

7.3.13.8 Thermal Shutdown (OTS)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OTSD bit in the OT status (OT_STS) register and OTF bit in the status register (DEV_STS) is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8376 family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, the charge pump is disabled, the GVDD and AVDD regulators are disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

注

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin in low does not exceed the t_{SLEEP} or t_{WAKE} time.

7.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, GVDD and AVDD regulator, and SPI bus are active.

7.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the DRV8376 family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

7.4.2 DRVOFF functionality

DRV8376 has capability to disable predriver and MOSFETs bypassing the digital through DRVOFF pin. When DRVOFF pin is pulled high, all six MOSFETs are disabled. If nSLEEP is high when the DRVOFF pin is high, the charge pump, AVDD regulator, GVDD regulator, and SPI bus are active and any driver-related faults such as OCP will be inactive. DRVOFF pin independently disables MOSFETs which will stop motor commutation irrespective of status of INHx and INLx input pins.

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7.5 SPI Communication

7.5.1 Programming

On DRV8376 SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in secondary mode and connects to a controller. The SPI input data (SDI) word consists of a 24-bit word, with one read or write bit, a parity bit, 6-bit address and 15 bits of data with a parity bit. The SPI output consists of 24 bit word, with a 8 bits of status information (STS register) and 16-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 24 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 24 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

7.5.1.1 SPI Format

SPI Format - with Parity

The SDI input data word is 24 bits long and consists of the following format:

- 1 read or write bit, W (bit B16)
- 6 address bits, A (bits B22 through B17)
- Parity bit, P (bit B23)
- 15 data bits with 1 parity bit, D (bits B15 through B0)

The SDO output data word is 24 bits long. The most significant bits are status bits and the least significant 16 bits are the data content of the register being accessed.

表 7-7. SDI Input Data Word Format for SPI

PARITY	ADDRESS							RW	PARITY	DATA														
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
P	A5	A4	A3	A2	A1	A0	W0	P	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

表 7-8. SDO Output Data Word Format

STATUS								DATA															
B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

The details of the bits used in SPI frame format are detailed below.

Read/Write Bit (R/W): R/W (W0) bit set to 0b indicates a SPI write transaction. For a SPI read operation, R/W bit needs to be set to 1b.

Address Bits (A): A SPI secondary device takes a 6-bit register address.

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Parity Bit (P): Both header and data fields of a SPI input data frame include a parity bit for single bit error detection - in 表 7-7, B23 is parity bit for the header field, while B15 is the parity bit for the data field. The parity scheme used is even parity - the number of ones in a block of 16-bits (including the parity bit) is even. Data will be written to the internal registers only if the parity check is successful. Parity checks can be enabled or disabled by configuring the SPI_PEN bit of SYS_CTRL register. Parity checks are disabled by default.

注

Though parity checks are disabled by default, TI recommends enabling parity checks to safeguard against single-bit errors.

7.6 Register Map

7.6.1 STATUS Registers

表 7-9 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in 表 7-9 should be considered as reserved locations and the register contents should not be modified.

表 7-9. STATUS Registers

Offset	Acronym	Register Name	Section
0h	Device Status Register	Device Status Register	セクション 7.6.1.1
2h	Device Raw Status Register	Device Raw Status Register	セクション 7.6.1.2
4h	Over Temperature Status Register	Over Temperature Status Register	セクション 7.6.1.3
5h	Supply Status Register	Supply Status Register	セクション 7.6.1.4
6h	Driver Status Register	Driver Status Register	セクション 7.6.1.5
7h	System Interface Status Register	System Interface Status Register	セクション 7.6.1.6

Complex bit access types are encoded to fit into small table cells. 表 7-10 shows the codes that are used for access types in this section.

表 7-10. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1.1 Device Status Register (Offset = 0h) [Reset = 0280h]

Device Status Register is shown in 表 7-11.

Return to the Summary Table.

表 7-11. Device Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-11	RESERVED	R-0	0h	Reserved
10	RESERVED	R	0h	Reserved
9	DNRDY_STS	R	1h	Device Not Ready Status. Will be cleared automatically after completion of Power Up. 0h = Device is Ready 1h = Device is NOT Ready
8	SYSFLT	R	0h	OTP Read fault occurred. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No OTP read fault is detected 1h = OTP read fault detected
7	RESET	R	1h	Device Reset status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = Cleared by FW after read 1h = Device has undergone power on reset
6	SPIFLT	R	0h	SPI Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No SPI fault is detected 1h = SPI fault is detected
5	OCP	R	0h	Overcurrent Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
4	RESERVED	R-0	0h	Reserved
3	OVP	R	0h	Over Voltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No over voltage condition is detected 1h = Over voltage condition is detected
2	UVP	R	0h	Supply Undervoltage Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No undervoltage voltage condition is detected on CP 1h = Undervoltage voltage condition is detected on CP
1	OTF	R	0h	Overtemperature Fault Status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No fault condition is detected 1h = Fault condition is detected

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7.6.1.2 Device Raw Status Register (Offset = 2h) [Reset = 0280h]

Device Raw Status Register is shown in 表 7-12.

Return to the Summary Table.

表 7-12. Device Raw Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-13	RESERVED	R-0	0h	Reserved
12	DRVOFF_RSTS	R	0h	Status of DRV_OFF pin 0h = DRV_OFF is not active 1h = DRV_OFF is active
11	OTW_RSTS	R	0h	OT Warning Raw Status 0h = OTW not active 1h = OTW is active
10	RESERVED	R	0h	Reserved
9	DNRDY_RSTS	R	1h	Device Not Ready Status 0h = Device is Ready 1h = Device is NOT Ready
8	SYSFLT_RSTS	R	0h	OTP Read fault occurred. Status remains latched until cleared by write to FLT_CLR 0h = No OTP read fault is detected 1h = OTP read fault detected
7	RESET	R	1h	Device power on status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = Cleared by FW after read 1h = Device has undergone power on reset
6	SPIFLT_RSTS	R	0h	SPI Fault status. Status remains latched until cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No SPI fault is detected 1h = SPI fault is detected
5	OCP_RSTS	R	0h	Overcurrent Fault Raw Status. Status remains latched until completion of Auto Retry or write to FLT_CLR or reset pulse on nSLEEP. 0h = Overcurrent condition is not active 1h = Overcurrent condition is active
4	RESERVED	R-0	0h	Reserved
3	OVP_RSTS	R	0h	Over Voltage Raw Fault Status. 0h = Over Voltage condition is not active. 1h = Over Voltage condition is active.
2	UVP_RSTS	R	0h	CP Undervoltage Raw Fault Status. 0h = Chare Pump Under voltage condition is not active. 1h = Chare Pump Under voltage condition is active.
1	OTF_RSTS	R	0h	Overtemperature Shutdown Raw Fault Status. 0h = Overtemperature shutdown is not active. 1h = Overtemperature shutdown is active.
0	RESERVED	R-0	0h	Reserved

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7.6.1.3 Over Temperature Status Register (Offset = 4h) [Reset = 0000h]

Over Temperature Status Register is shown in 表 7-13.

Return to the Summary Table.

表 7-13. Over Temperature Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1	OTW	R	0h	Overtemperature Warning Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
0	OTSD	R	0h	Overtemperature Shutdown Fault status. Can be cleared by write to FLT_CLR or reset pulse on nSLEEP 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected

7.6.1.4 Supply Status Register (Offset = 5h) [Reset = 0000h]

Supply Status Register is shown in 表 7-14.

Return to the Summary Table.

表 7-14. Supply Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-7	RESERVED	R-0	0h	Reserved
6	VM_OV	R	0h	Vm Over Voltage Fault Status 0h = No Vm over voltage is detected 1h = Vm over voltage is detected
5	RESERVED	R-0	0h	Reserved
4	CP_UV	R	0h	Charge Pump Undervoltage fault status 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
3-0	RESERVED	R-0	0h	Reserved

7.6.1.5 Driver Status Register (Offset = 6h) [Reset = 0000h]

Driver Status Register is shown in 表 7-15.

Return to the Summary Table.

表 7-15. Driver Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-7	RESERVED	R-0	0h	Reserved
6	OCPC_HS	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side MOSFET of OUTC 1h = Overcurrent detected on high-side MOSFET of OUTC
5	OCPB_HS	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side MOSFET of OUTB 1h = Overcurrent detected on high-side MOSFET of OUTB
4	OCPA_HS	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side MOSFET of OUTA 1h = Overcurrent detected on high-side MOSFET of OUTA
3	RESERVED	R-0	0h	Reserved
2	OCPC_LS	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side MOSFET of OUTC 1h = Overcurrent detected on low-side MOSFET of OUTC
1	OCPB_LS	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side MOSFET of OUTB 1h = Overcurrent detected on low-side MOSFET of OUTB
0	OCPA_LS	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side MOSFET of OUTA 1h = Overcurrent detected on low-side MOSFET of OUTA

7.6.1.6 System Interface Status Register (Offset = 7h) [Reset = 0000h]

System Interface Status Register is shown in 表 7-16.

Return to the Summary Table.

表 7-16. System Interface Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-5	RESERVED	R-0	0h	Reserved
4	OTPLD_ERR	R	0h	OTP CRC error during load 0h = No OTP read error is detected 1h = OTP read error is detected
3	RESERVED	R-0	0h	Reserved
2	SPI_PARITY	R	0h	SPI Parity Error 0h = No SPI Parity Error is detected 1h = SPI Parity Error is detected
1	RESERVED	R-0	0h	Reserved
0	FRM_ERR	R	0h	SPI Frame Error 0h = No SPI Frame Error is detected 1h = SPI Frame Error is detected

7.6.2 CONTROL Registers

表 7-17 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in 表 7-17 should be considered as reserved locations and the register contents should not be modified.

表 7-17. CONTROL Registers

Offset	Acronym	Register Name	Section
10h	Fault Mode Register	Fault Mode Register	セクション 7.6.2.1
13h	Drviver Fault Control Register	Drviver Fault Control Register	セクション 7.6.2.2
17h	Fault Clear Register	Fault Clear Register	セクション 7.6.2.3
20h	PWM Control Register 1	PWM Control Register 1	セクション 7.6.2.4
22h	Predriver control Register	Predriver control Register	セクション 7.6.2.5
23h	CSA Control Register	CSA Control Register	セクション 7.6.2.6
3Fh	System Control Register	System Control Register	セクション 7.6.2.7

Complex bit access types are encoded to fit into small table cells. 表 7-18 shows the codes that are used for access types in this section.

表 7-18. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

7.6.2.1 Fault Mode Register (Offset = 10h) [Reset = 2811h]

Fault Mode Register is shown in 表 7-19.

Return to the Summary Table.

表 7-19. Fault Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	RESERVED	R-0	0h	Reserved
13	ILIMFLT_MODE	R/W	1h	ILIMIT Fault mode 0h = ILIMIT reporting on nFAULT pin is disabled 1h = ILIMIT reporting on nFAULT pin is enabled
12-11	RESERVED	R/W	0h	Reserved
10	RESERVED	R-0	0h	Reserved
9	OVP_MODE	R/W	0h	Over Voltage Protection Fault mode 0h = Over Voltage protection is disabled 1h = Over Voltage protection is enabled
8	RESERVED	R-0	0h	Reserved
7	SPIFLT_MODE	R/W	0h	SPI Fault mode 0h = SPI fault reporting on nFAULT pin is disabled 1h = SPI fault reporting on nFAULT pin is enabled
6	RESERVED	R-0	0h	Reserved
5-4	OCP_MODE	R/W	1h	Overcurrent Protection Fault mode 0h = Over Current causes a latched fault 1h = Over Current causes an automatic retrying fault 2h = Over Current is report only but no action is taken 3h = Over Current is not reported and no action is taken
3-1	RESERVED	R-0	0h	Reserved
0	OTW_MODE	R/W	1h	Overtemperature Warning Fault mode 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

7.6.2.2 Drviver Fault Control Register (Offset = 13h) [Reset = 1010h]

Drviver Fault Control Register is shown in 表 7-20.

Return to the Summary Table.

表 7-20. Drviver Fault Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14	RESERVED	R-0	0h	Reserved
13-12	RESERVED	R/W	0h	Reserved
11	RESERVED	R-0	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R-0	0h	Reserved
8	OVP_SEL	R/W	0h	Overvoltage level setting 0h = VM overvoltage level is 65V 1h = VM overvoltage level is 35V
7-6	RESERVED	R-0	0h	Reserved
5-4	OCP_DEG	R/W	1h	OCP Deglitch time 0h = OCP Deglitch time is 0.6 µs 1h = OCP Deglitch time is 1.25 µs 2h = OCP Deglitch time is 1.6 µs 3h = OCP Deglitch time is 2 µs
3	RESERVED	R-0	0h	Reserved
2	OCP_TRETRY	R/W	0h	OCP Retry Time 0h = 5ms 1h = 500ms
1	RESERVED	R-0	0h	Reserved
0	OCP_LVL	R/W	0h	OCP Level 0h = 4.5A 1h = 2A

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7.6.2.3 Fault Clear Register (Offset = 17h) [Reset = 0000h]

Fault Clear Register is shown in 表 7-21.

Return to the Summary Table.

表 7-21. Fault Clear Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-1	RESERVED	R-0	0h	Reserved
0	FLT_CLR	R-0/W1C	0h	Clear latched faults 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

7.6.2.4 PWM Control Register 1 (Offset = 20h) [Reset = 0020h]

PWM Control Register 1 is shown in 表 7-22.

Return to the Summary Table.

表 7-22. PWM Control Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9-8	RESERVED	R/W	0h	Reserved
7-6	PWM_100_FREQ_SEL	R/W	0h	Frequency of PWM at 100% Duty cycle 0h = 20KHz 1h = 40KHz 2h = 10KHz 3h = None
5	ILIM_MODE	R/W	1h	Current limit recirculation settings 0h = Current recirculation through FETs (Brake mode) 1h = Current recirculation through diodes (coast mode)
4	RESERVED	R/W	0h	Reserved
3	EN_AAR	R/W	0h	Enable AAR where LS FET gets turned off when current goes negative. 0h = Active Demagnetization AAR is Disabled 1h = Active Demagnetization AAR is Enabled
2	EN_ASR	R/W	0h	Actie Demag Enable 0h = Active Demagnetization is Disabled 1h = Active Demagnetization is Enabled
1-0	PWM_MODE	R/W	0h	PWM mode selection 0h = 6x mode 1h = 6x mode 2h = 3x mode 3h = 3x mode

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7.6.2.5 Predriver control Register (Offset = 22h) [Reset = 0080h]

Predriver control Register is shown in 表 7-23.

Return to the Summary Table.

表 7-23. Predriver control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-11	RESERVED	R-0	0h	Reserved
10-8	ILIM_BLANK_SEL	R/W	0h	Current Limit Blanking Time Selection 0h = 5.5us for slew rate of 50 and 1.8us for all other slew rates. 1h = 6.0us for slew rate of 50 and 2.3us for all other slew rates. 2h = 6.5us for slew rate of 50 and 2.8us for all other slew rates. 3h = 7.5us for slew rate of 50 and 3.8us for all other slew rates.
7-4	ADMAG_TMARGIN	R/W	8h	Wait time before determining HiZ N * 4 Clock Cycles => N*4*50ns
3	AD_COMP_TH_HS	R/W	0h	Active demag high side comparator threshold 0h = active demag comparator threshold is 100mA 1h = active demag comparator threshold is 150mA
2	AD_COMP_TH_LS	R/W	0h	Active demag low side comparator threshold 0h = active demag comparator threshold is 100mA 1h = active demag comparator threshold is 150mA
1-0	SLEW_RATE	R/W	0h	Slew rate settings 0h = Slew rate is 1000 V/µs 1h = Slew rate is 500 V/µs 2h = Slew rate is 250 V/µs 3h = Slew rate is 50 V/µs

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7.6.2.6 CSA Control Register (Offset = 23h) [Reset = 0000h]

CSA Control Register is shown in 表 7-24.

Return to the Summary Table.

表 7-24. CSA Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-2	RESERVED	R-0	0h	Reserved
1-0	CSA_GAIN	R/W	0h	CSA Gain settings 0h = CSA gain is 0.4 V/A 1h = CSA gain is 1.0 V/A 2h = CSA gain is 2.5 V/A 3h = CSA gain is 5.0 V/A

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7.6.2.7 System Control Register (Offset = 3Fh) [Reset = 0008h]

System Control Register is shown in 表 7-25.

Return to the Summary Table.

表 7-25. System Control Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PARITY	R	0h	Parity Bit if SPI_PEN is set to '1' otherwise reserved
14-12	WRITE_KEY	R-0/W	0h	0x5 Write Key Specific to this register.
11	SDO_VSEL	R/W	0h	SDO Output Voltage Select 0h = AVDD 1h = GVDD
10	SDO_ODEN	R/W	0h	SDO in Open Drain Mode 0h = SDO in Push Pull Mode 1h = SDO in Open Drain Mode
9-8	RESERVED	R-0	0h	Reserved
7	REG_LOCK	R/W	0h	Register Lock Bit 0h = Registers Unlocked 1h = Registers Locked
6	SPI_PEN	R/W	0h	Parity Enable for SPI 0h = Parity Disabled 1h = Parity Enabled
5-4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2-0	RESERVED	R-0	0h	Reserved

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV8376 can be used to drive Brushless-DC motors. A primary application schematic is shown in 図 8-1.

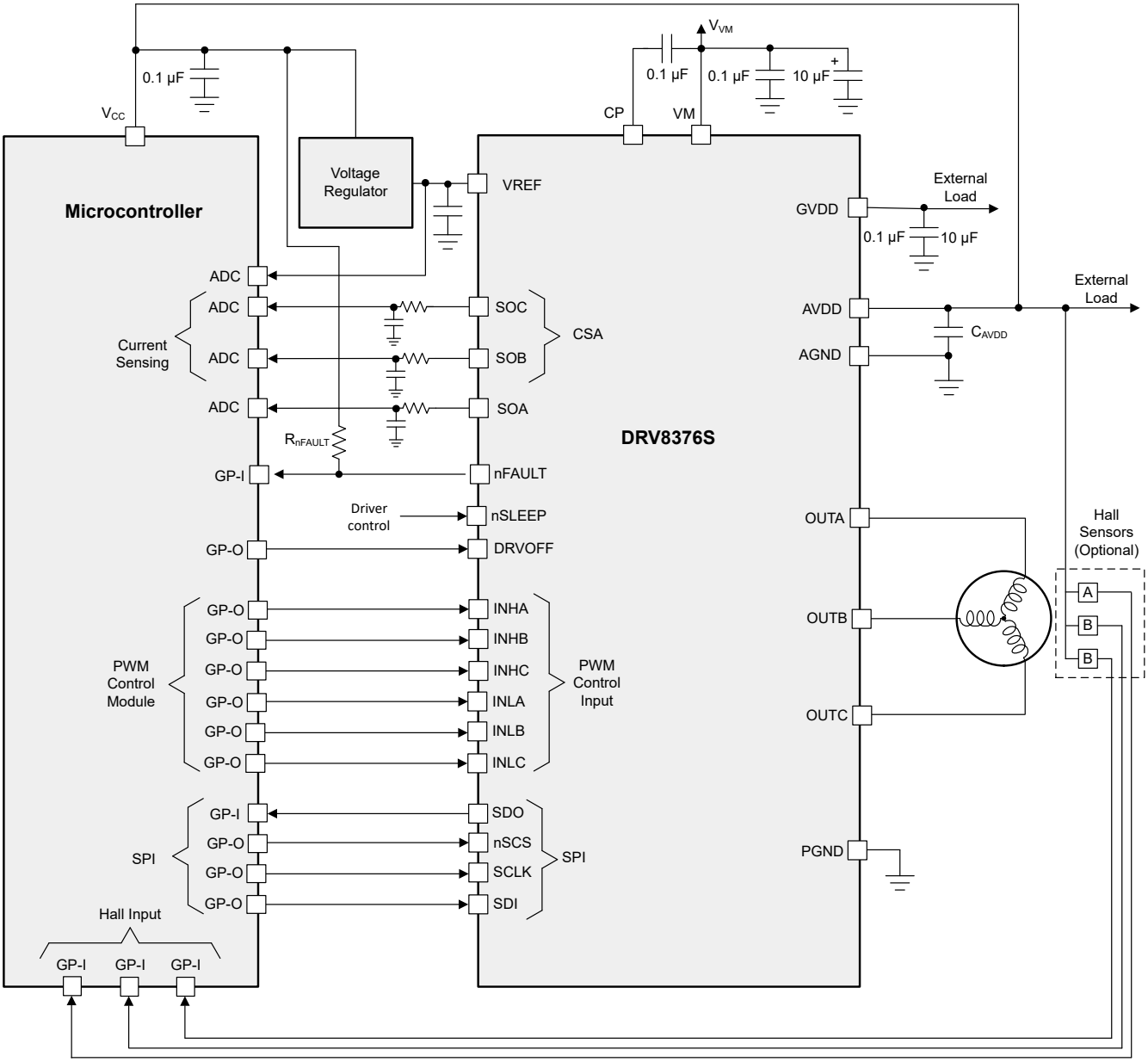

図 8-1. Primary Application Schematics

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8.2 Power Supply Recommendations

8.2.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

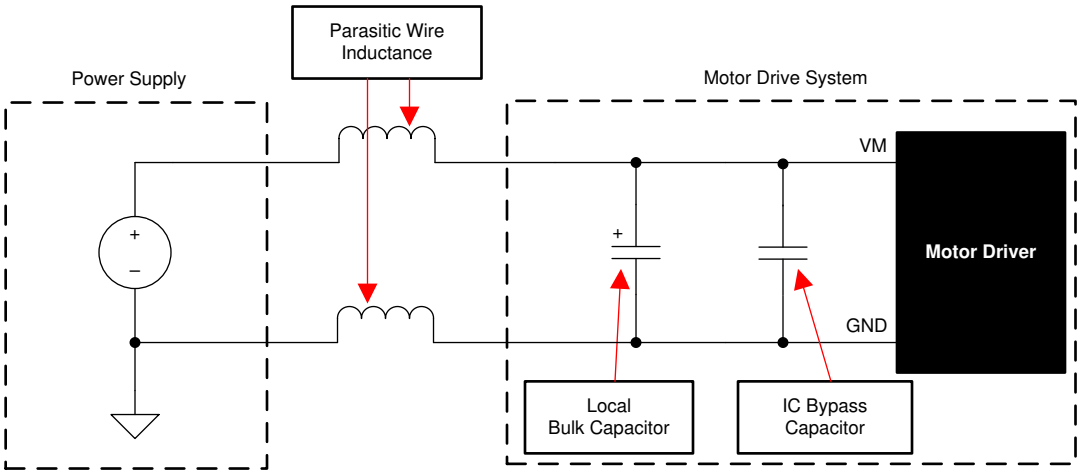

図 8-2. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

8.3 Layout

8.3.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump, GVDD, AVDD, and VREF capacitors should be ceramic and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage

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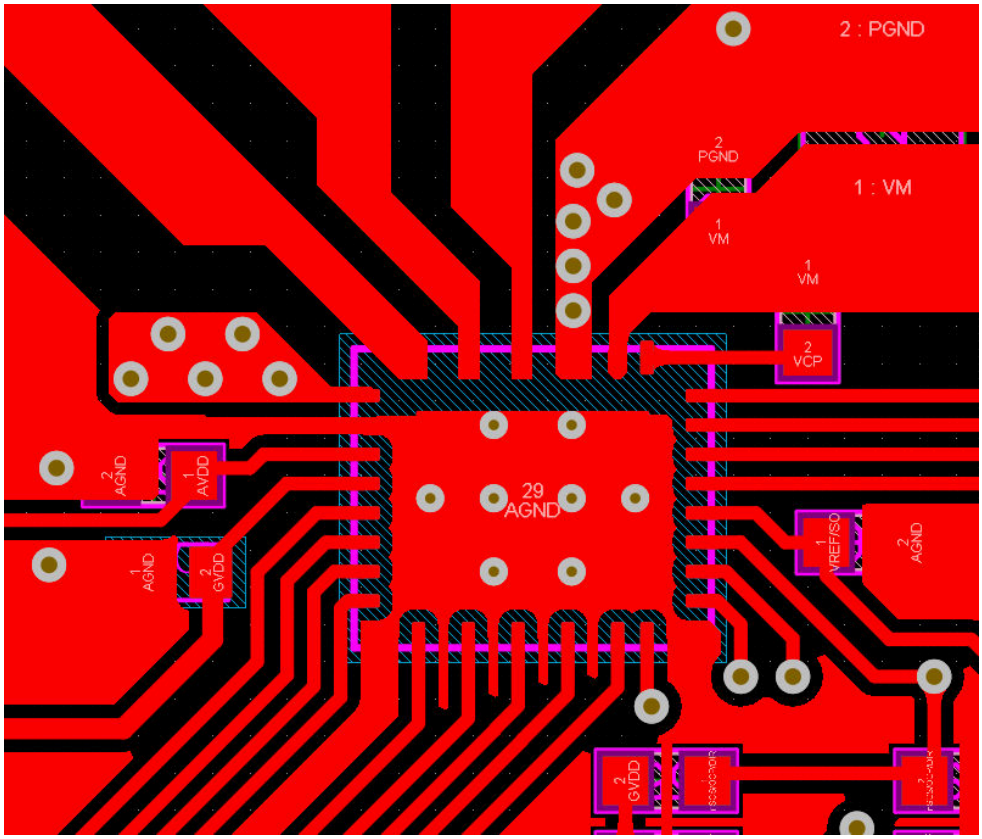
circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

8.3.2 Layout Example

Recommended Layout Example for VQFN Package



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8.3.3 Thermal Considerations

The DRV8376 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.3.3.1 Power Dissipation

The power loss in DRV8376 include standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in DRV8376. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and their duration into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that RDS,ON increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

9 Device and Documentation Support

9.1 Documentation Support

9.2 サポート・リソース

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
October 2024	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PDRV8376HNLGR		HTSSOP	DDW	44	2500					

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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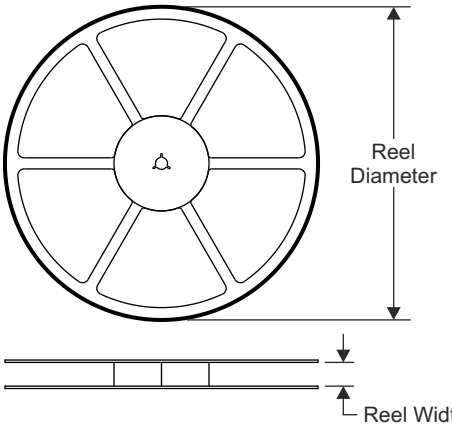
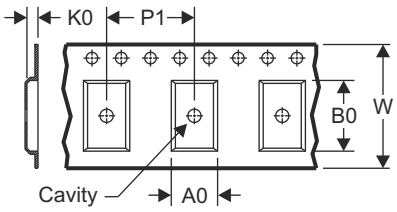
11.2 Tape and Reel Information

REEL DIMENSIONS

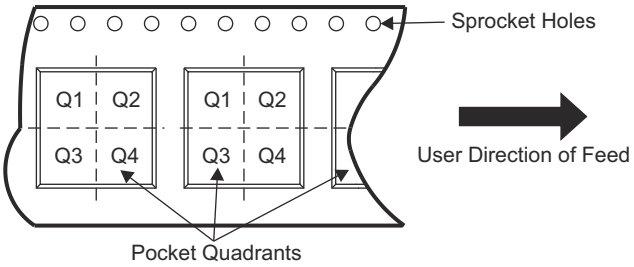


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

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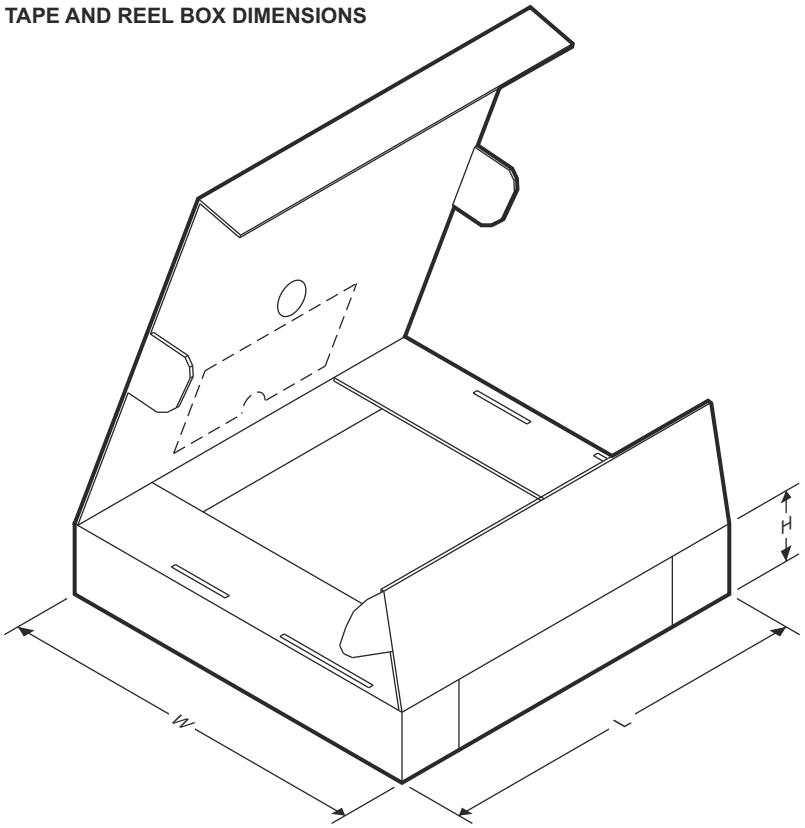
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV8376HNLGR	ACTIVE	VQFN	NLG	28	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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