DRV8801A-Q1　DMOS フルブリッジ・モータ・ドライバ

1 特長

- 車載アプリケーション向けに認定済み
- 低オン抵抗出力:0.83Ω
- 低消費電力スリープ・モード
- 100% の PWM デューティ・サイクルをサポート
- 6.5～36V の電源動作電圧範囲
- 放熱性を高めた表面実装パッケージ
- 設定可能な過電流制限値
- **保護機能**
  - V_{BB} 低電圧誤動作防止 (UVLO)
  - 過電流保護 (OCP)
  - 電源短絡保護
  - グランド短絡保護
  - 過熱警告 (OTW)
  - 過熱シャットダウン (OTS)
  - 過電流および過熱フォルト状態をピン (nFAULT) で表示

2 アプリケーション

- 車載ボディ・システム
- ドア・ロック
- HVAC アクチュエータ
- ピエゾ・アラーム

3 概要

DRV8801A-Q1 デバイスは、フル H ブリッジ・ドライバを備えた多用途モータ・ドライバ・ソリューションです。本デバイスは、ブラシ付き DC モータ、ステッパ・モータの 1 つの巻線、ソレノイドなどのその他のデバイスを駆動できます。単純な PHASE/ENABLE インターフェイスにより、簡単に制御回路と接続できます。

出力段は、H ブリッジとして構成された N チャネル・パワー MOSFET を使用しています。DRV8801A-Q1 デバイスは最大 ±2.8A のピーク出力電流と最大 36V の動作電圧に対応しています。必要なゲート駆動電圧は、内蔵チャージ・ポンプによって生成されます。

低消費電力スリープ・モードが用意されており、内部回路をシャットダウンして静止消費電流を非常に小さく抑えられます。このスリープ・モードは、専用の nSLEEP ピンを使用して設定できます。

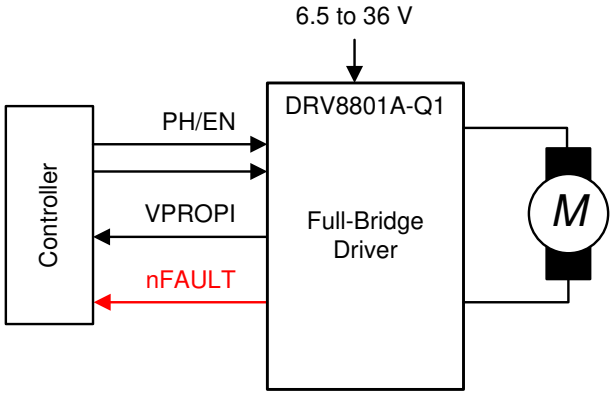
低電圧誤動作防止、過電流保護、電源短絡保護、グランド短絡保護、過熱警告、過熱シャットダウンなどの保護機能が内蔵されています。過電流 (グランドとの短絡、電源との短絡を含む) および過熱フォルト状態は nFAULT ピンによって示されます。

DRV8801A-Q1 デバイスは、ウェッタブル・フランクと露出サーマル・パッドを備えた 16 ピン WQFN パッケージ (環境配慮型パッケージ:RoHS 準拠、Sb/Br 非含有) で供給されます。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)
DRV8801A-Q1	WQFN (16)	4.00mm × 4.00mm

(1)　利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2016) to Revision D (June 2020) — **Page**

- Improved description for pins CP1, CP2,nFAULT, nSLEEP, VBB and VCP in *Pin Functions* table ... 3
- Added entries for VCP and CP2 pins in *Absolute Maximum Ratings* table ... 4
- Removed incorrect duplicate input logic current entry for ENABLE pin in *Electrical Characteristics* table ... 5
- Added additional information on SENSE pin behavior ... 10
- Added equation for VPROPI to help when connecting pin's output to ADC in *Feature Description* ... 11
- Added die temperature estimation equation utilizing junction to ambient thermal impedance in Application and Implementation section ... 14
- Added information on using motor driver's pulse width modulating modes in *Application and Implementation* section ... 14
- Added information on connecting multiple DRV8801-Q1 together to support higher current in *Application and Implementation* section ... 15

Changes from Revision B (June 2016) to Revision C (July 2016) — **Page**

- Changed the T_J value for some test conditions for the output ON resistance parameter in the *Electrical Characteristics* ... 5
- Added the *Documentation Support*, *Receiving Notification of Documentation Updates*, and *Community Resources* sections ... 21

Changes from Revision A (September 2014) to Revision B (June 2016) — **Page**

- Changed the value of T_J from 125°C to 25°C in the test condition (source driver, I_O = –2.8 A, V_{BB} = 8 to 36 V) for the output ON resistance parameter ... 5
- Added the UVLO hysteresis parameter in the *Electrical Characteristics* table ... 5
- Added MIN and MAX values for the overcurrent retry time parameter in the *Electrical Characteristics* table ... 5
- Updated the *Functional Block Diagram* ... 8
- Added t_{pd} to the *Overcurrent Control Timing* image ... 10

Changes from Revision * (June 2014) to Revision A (September 2014) **Page**

- Added TYPE column to the *Pin Functions* table 3
- Updated the *Overcurrent Control Timing* image..... 10

5 Pin Configuration and Functions

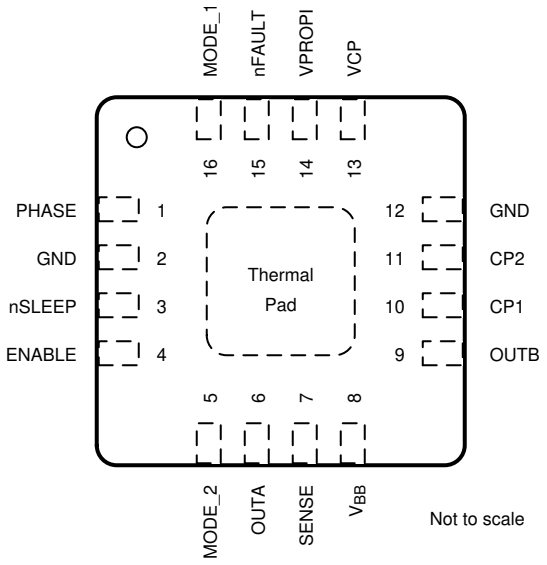


図 5-1. RMJ Package 16-Pin WQFN With Thermal Pad Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CP1	10	—	Charge pump switching node. Connect a X7R, 0.1-µF, V_{BB}-rated ceramic capacitor from CP1 to CP2.
CP2	11	—	
ENABLE	4	I	Enables OUTA and OUTB drivers
GND	2	PWR	Ground
	12		
MODE 1	16	I	Mode logic input
MODE 2	5	I	Mode 2 logic input
nFAULT	15	OD	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	3	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
OUTA	6	O	DMOS full-bridge output positive. H-Bridge output A
OUTB	9	O	DMOS full-bridge output negative. H-Bridge output B
PHASE	1	I	Phase logic input for direction control
SENSE	7	IO	Sense power return
V_{BB}	8	PWR	Driver supply voltage. Bypass to GND with 0.1-µF ceramic capacitors plus a bulk capacitor rated for V_{BB}.
VCP	13	—	Charge pump reservoir capacitor pin. Connect a X7R, 0.1-µF, 16-V ceramic capacitor to V_{BB}.
VPROPI	14	O	Winding current proportional voltage output
Thermal pad		—	Exposed pad for thermal dissipation; connect to GND pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage(2)	V_{BB}	–0.3	40	V
Charge pump voltage	VCP and CP2	–0.3	V_{BB} +17	V
Digital pin voltage	PHASE, ENABLE, MODE1, MODE2, nSLEEP, nFAULT	–0.3	7	V
V_{BB} to OUTx voltage	OUTA and OUTB	–0.3	36	V
OUTx to GND voltage	OUTA and OUTB	–0.3	36	V
Sense pin voltage	SENSE	–0.5	0.5	V
H-bridge output current	OUTA, OUTB, and SENSE		2.8	A
VPROPI pin voltage	VPROPI	–0.3	3.6	V
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{BB}	Power supply voltage	6.5	36	V
V_{CC}	Logic supply voltage	0	5.5	V
$f_{(PWM)}$	Applied PWM signal (PHASE and ENABLE)	0	100	kHz
I_O	H-bridge peak output current	0	2.8	A
T_A	Ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DRV8801A-Q1 RMJ (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.7	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{BB})							
V_{BB}	V_{BB} operating supply voltage			6.5		36	V
I_{BB}	V_{BB} operating supply current	f_{PWM} < 50 kHz			6		mA
		Charge pump on, Outputs disabled			3.2		
$I_{BB(Q)}$	V_{BB} sleep-mode supply current	nSLEEP = 0, T_J = 25°C				10	µA
CONTROL INPUTS (PHASE, ENABLE, MODE1, MODE2, nSLEEP)							
V_{IL}	Input logic low voltage	PHASE, ENABLE MODE1, MODE2				0.8	V
V_{IH}	Input logic high voltage			2			
I_{IL}	Input logic low current	PHASE, MODE1, MODE2	V_I = 0.8 V	–20	≤ –2	20	µA
I_{IH}	Input logic high current		V_I = 2 V		< 1	20	
I_{IL}	Input logic low current	ENABLE	V_I = 0.8 V		16	40	µA
I_{IH}	Input logic high current		V_I = 2 V		40	100	
V_{IL}	Input logic low voltage	nSLEEP				0.8	V
V_{IH}	Input logic high voltage			2.7			
I_{IL}	Input logic low current		V_I = 0.8 V		< 1	10	µA
I_{IH}	Input logic high current		V_I = 2 V		27	50	
CONTROL OUTPUTS (nFAULT)							
V_{OL}	Output logic low voltage	I_O = 1 mA				0.4	V
DMOS DRIVERS (OUTA, OUTB, SENSE, VPROPI)							
$r_{DS(on)}$	Output ON resistance	Source driver, I_O = –2.8 A, T_J = 25°C , V_{BB} = 6.5 to 36 V			0.48		Ω
		Source driver, I_O = –2.8 A, T_J = 125°C, V_{BB} = 8 to 36 V			0.74	0.85	
		Source driver, I_O = –2.8 A, T_J = 125°C, V_{BB} = 6.5 to 8 V			0.74	0.9	
		Sink driver, I_O = 2.8 A, T_J = 25°C, V_{BB} = 6.5 to 36 V			0.35		
		Sink driver, I_O = 2.8 A, T_J = 125°C, V_{BB} = 8 to 36 V			0.52	0.7	
		Sink driver, I_O = 2.8 A, T_J = 125°C, V_{BB} = 6.5 to 8 V			0.52	0.75	
$V_{(TRIP)}$	SENSE trip voltage	$R_{(SENSE)}$ between SENSE and GND		450	500	550	mV
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A				1.4	V
		Sink diode, I_f = 2.8 A				1.4	
t_{pd}	Propagation delay time	Input edge to source or sink ON			600		ns
		Input edge to source or sink OFF			100		
t_{COD}	Crossover delay				500		ns

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$G_{D(a)}$	Differential amplifier gain	V_{BB} = 8 to 36 V; SENSE = 0.1 to 0.4 V	4.8	5	5.2	V/V
		V_{BB} = 6.5 to 8 V; SENSE = 0.1 to 0.3 V	4.8		5.2	V/V
PROTECTION CIRCUITS						
VUV	UVLO threshold	V_{BB} increasing		5.5	6.4	V
		V_{BB} decreasing			5.7	
	UVLO hysteresis		500		850	mV
$I_{(OCP)}$	Overcurrent protection trip level	V_{BB} = 8 to 36 V	3			A
		V_{BB} = 6.5 to 8 V	2.8			A
$t_{(DEG)}$	Overcurrent deglitch time			3		µs
$t_{(OCP)}$	Overcurrent retry time		0.5	1.2	3	ms
$T_{(OTW)}$	Thermal warning temperature	Die temperature T_J		160		°C
$T_{hys(OTW)}$	Thermal warning hysteresis	Die temperature T_J		15		°C
$T_{(OTS)}$	Thermal shutdown temperature	Die temperature T_J		175		°C
$T_{hys(OTS)}$	Thermal shutdown hysteresis	Die temperature T_J		15		°C

6.6 Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
RMJ	36.8	3 W	27 mW/C

6.7 Typical Characteristics

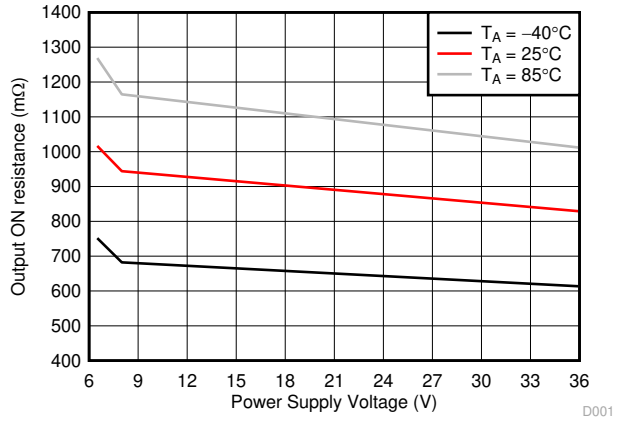


図 6-1. $r_{DS(on)}$ Over Voltage

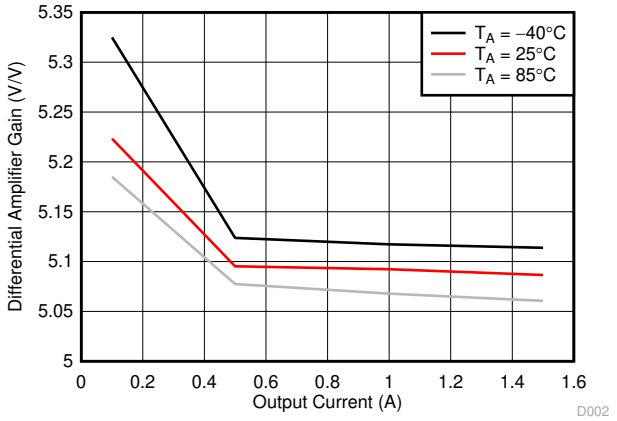


図 6-2. VPROPI Over Output Current

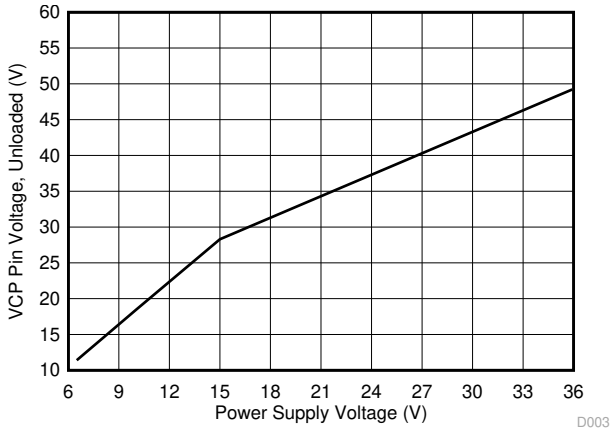


図 6-3. VCP Voltage vs V_{BB}

7 Detailed Description

7.1 Overview

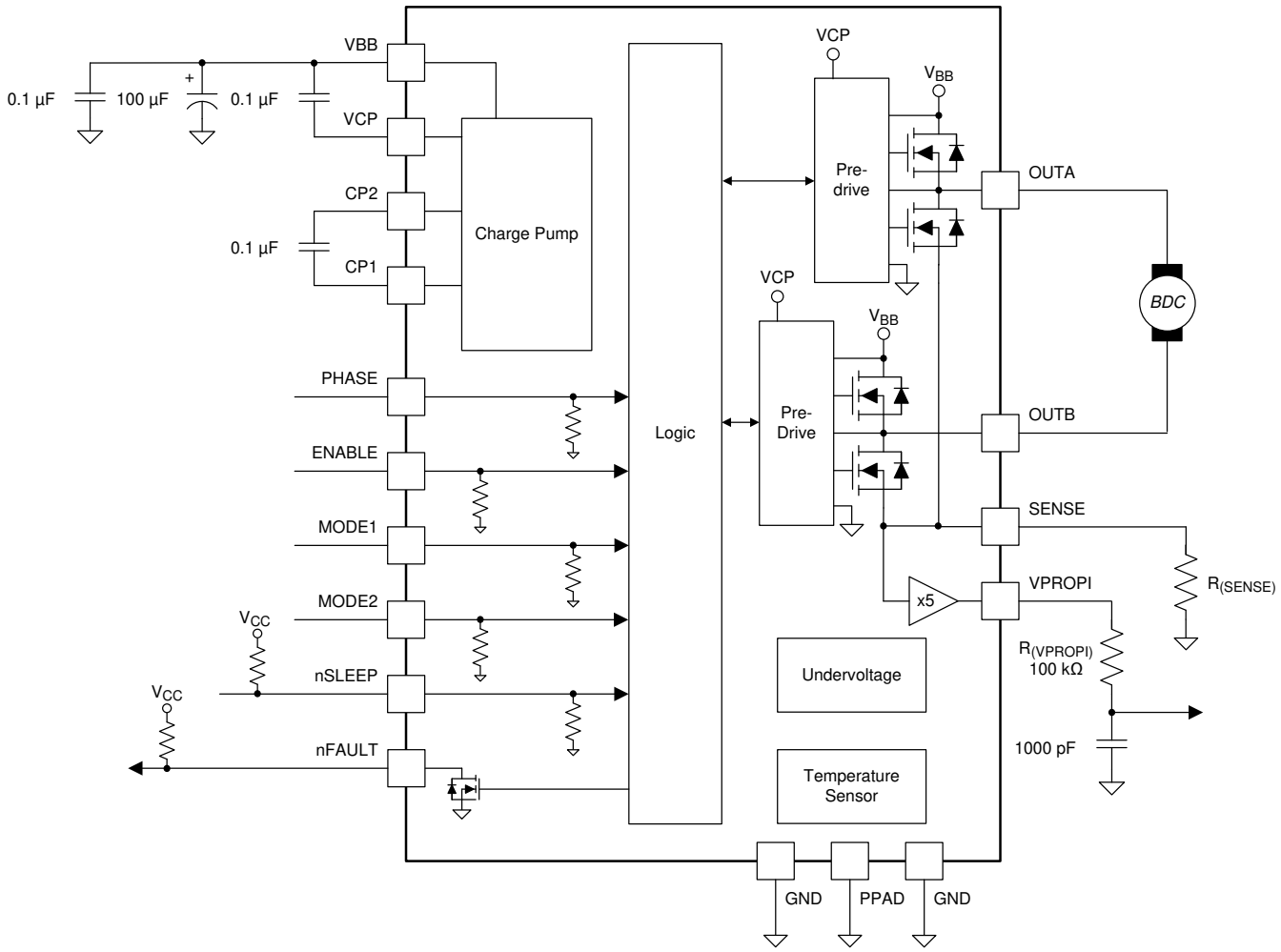
The DRV8801A-Q1 device is an integrated motor driver solutions for brushed-DC motors. The device integrates a DMOS H-bridge and current sense and protection circuitry. The device can be powered with a supply voltage between 6.5 V and 36 V, and is capable of providing an output current up to 2.8-A peak.

A simple PHASE and ENABLE interface allows control of the motor speed and direction.

A shunt amplifier output is provided for accurate current measurements by the system controller. The VPROPI pin outputs a voltage that is five-times the voltage seen at the SENSE pin.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supervisor

The control input, nSLEEP, is used to minimize power consumption when the DRV8801A-Q1 device is not in use. A logic low on the nSLEEP input disables much of the internal circuitry, including the internal voltage rails and charge pump. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

7.3.2 Bridge Control

The following table shows the logic for the DRV8801A-Q1:

nSLEEP	PHASE	ENABLE	MODE1	MODE2	OUTA	OUTB	OPERATION
0	X	X	X	X	Z	Z	Sleep mode
1	0	1	X	X	L	H	Reverse
1	1	1	X	X	H	L	Forward
1	0	0	0	X	H	L	Fast decay
1	1	0	0	X	L	H	Fast decay
1	X	0	1	0	L	L	Low-side Slow decay
1	X	0	1	1	H	H	High-side Slow decay

To prevent reversal of current during fast-decay synchronous rectification, outputs go to the high impedance state as the current approaches 0 A.

The path of current flow for each of the states in the above logic table is shown in 図 7-1.

7.3.2.1 MODE 1

Input MODE 1 is used to toggle between fast-decay mode and slow-decay mode. A logic high puts the device in slow-decay mode.

7.3.2.2 MODE 2

MODE 2 is used to select which set of drivers (high side versus low side) is used during the slow-decay recirculation. MODE 2 is meaningful only when MODE 1 is asserted high. A logic high on MODE 2 has current recirculation through the high-side drivers. A logic low has current recirculation through the low-side drivers.

7.3.3 Fast Decay with Synchronous Rectification

This decay mode is equivalent to a phase change where the FETs opposite of the driving FETs are switched on (2 in 図 7-1). When in fast decay, the motor current is not allowed to go negative because this would cause a change in direction. Instead, as the current approaches zero, the drivers turn off. See the *セクション 10.3* section for an equation to calculate power.

7.3.4 Slow Decay with Synchronous Rectification (Brake Mode)

In slow-decay mode, both low-side and high-side drivers turn on, allowing the current to circulate through the low-side and high-side body diodes of the H-bridge and the load (3 and 4 in 図 7-1). See the *セクション 10.3* section for equations to calculate power for both high-side and low-side slow decay.

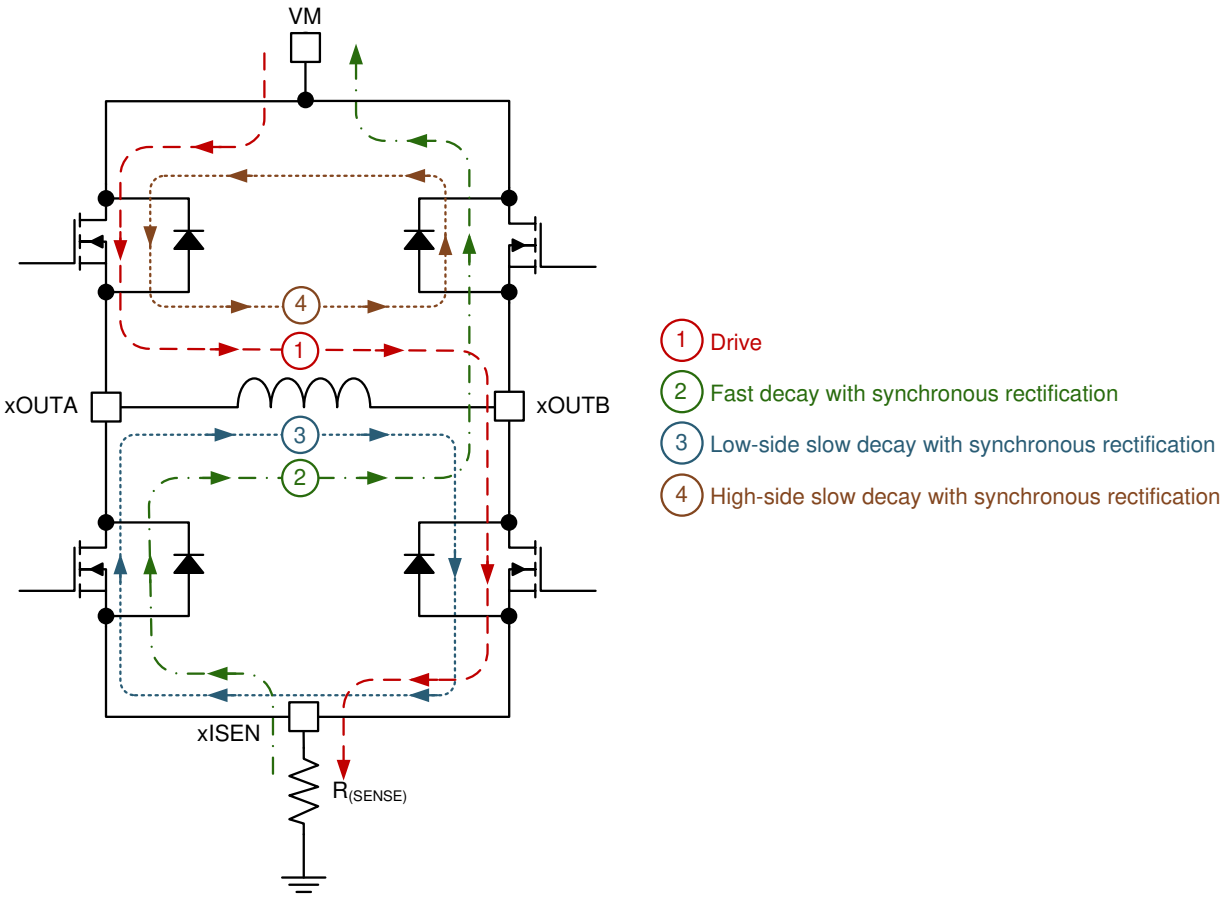


図 7-1. H-Bridge Operation Modes

7.3.5 Charge Pump

The charge pump is used to generate a supply above V_{BB} to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor should be connected between VCP and V_{BB} to act as a reservoir to run the high-side DMOS devices.

7.3.6 SENSE

A low-value SENSE resistor is used to set an overcurrent threshold lower than the default maximum value of 2.8 A and to provide a voltage for VPROPI. This SENSE resistor must be connected between the SENSE pin and ground. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

A direct connection to ground yields a SENSE voltage equal to zero. In that case, maximum current is 2.8 A and VPROPI outputs 0 V. A resistor connected as explained before, will yield a VPROPI output as detailed in section セクション 7.3.7. Size the sense resistor such that voltage drop across the sense resistor is less than 500 mV under normal loading conditions. Any voltage equal or larger to 500 mV will signal the device to hi-Z the H-bridge output as overcurrent trip threshold has been reached. In this case, device will enter recirculation as stipulated by the MODE input pin. The device automatically retries with a period of $t_{(OCP)}$.

式 1 shows the value of the resistor to a particular current setting.

$$R_{sense} = \frac{500\ mV}{I_{trip}} \quad (1)$$

The overcurrent trip level selected cannot be greater than $I_{(OCP)}$.

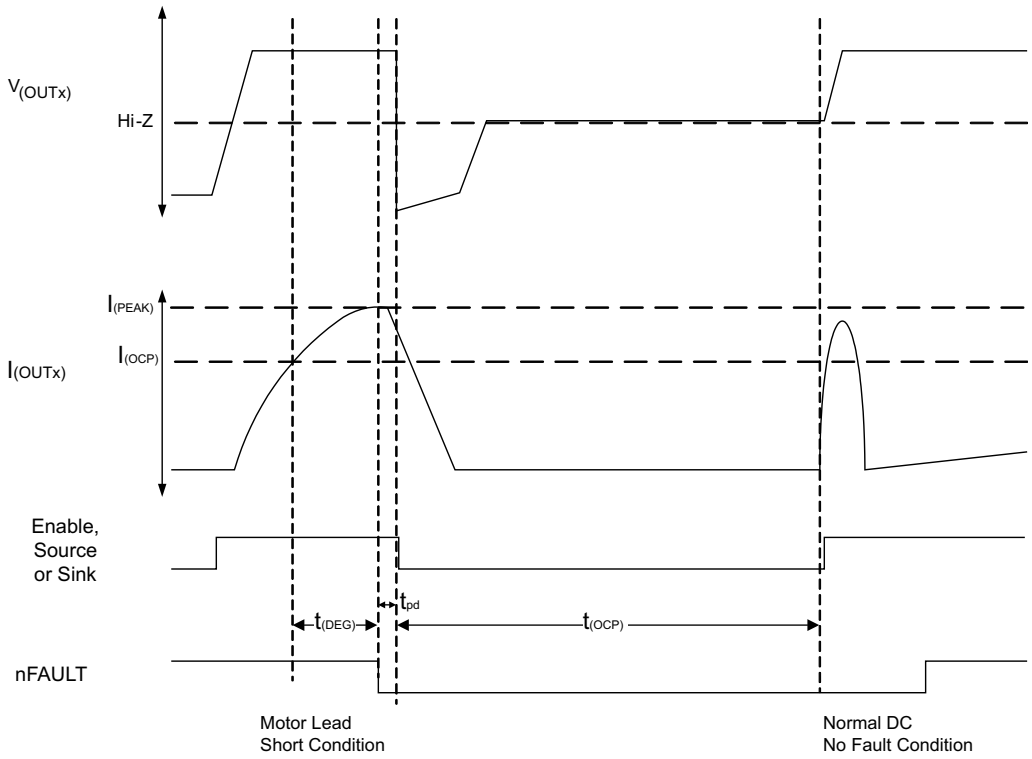


図 7-2. Overcurrent Control Timing

7.3.7 VPROPI

The analog output VPROPI offers SENSE current information as an analog voltage proportional to the current flowing through the DC motor winding. This voltage can be used by an analog to digital converter and microcontroller to accurately determine how much current is flowing through the controlled DC motor. See セクション 7.3.6 for guidance on selecting a SENSE resistor value.

7.3.7.1 Connecting VPROPI Output to ADC

The analog output VPROPI varies proportionally with the SENSE voltage according to 式 2. It's important to note even if V_{SENSE} is negative VPROPI will remain at 0 V.

$$VPROPI = 5 \times V_{SENSE} \quad (2)$$

An RC network in series with the VPROPI output is recommended, if this voltage is to be sampled by an analog to digital converter.

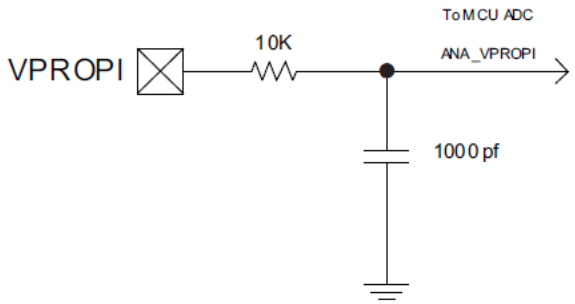


図 7-3. RC Network in Series With the VPROPI Output

It is imperative to realize that VPROPI will decrease to 0 V while the H-Bridge enters slow decay recirculation.

7.3.8 Protection Circuits

The DRV8801A-Q1 device is fully protected against V_{BB} undervoltage, overcurrent, and overtemperature events.

FAULT	ERROR REPORT	H-BRIDGE	CHARGE PUMP	RECOVERY
V_{BB} undervoltage (UVLO)	No error report – nFAULT is hi-Z	Disabled	Shut Down	V_{BB} > VUVLO RISING
Overcurrent (OCP)	nFAULT pulled low	Disabled	Operating	Retry time, $t_{(OCP)}$
Overtemperature Warning (OTW)	nFAULT pulled low	Enabled	Operating	$T_J < T_{(OTW)} – T_{hys(OTW)}$
Overtemperature Shutdown (OTS)	nFAULT remains pulled low (set during OTW)	Disabled	Shut Down	$T_J < T_{(OTS)} – T_{hys(OTS)}$

7.3.8.1 V_{BB} Undervoltage Lockout (UVLO)

If at any time the voltage on the V_{BB} pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled and the charge pump is disabled. The nFAULT pin does not report the UVLO fault condition and remains hi-Z. Operation resumes when V_{BB} rises above the UVLO threshold.

7.3.8.2 Overcurrent Protection (OCP)

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge are disabled, nFAULT is driven low, and a $t_{(OCP)}$ fault timer is started. After this period, $t_{(OCP)}$, the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT releases during this attempt). If there is still a fault condition, the cycle repeats. If the short condition is not present after $t_{(OCP)}$ expires, normal operation resumes and nFAULT is released.

7.3.8.3 Overtemperature Warning (OTW)

If the die temperature increases past the thermal warning threshold the nFAULT pin is driven low. When the die temperature has fallen below the hysteresis level, the nFAULT pin is released. If the die temperature continues to increase, the device enters overtemperature shutdown as described in the *セクション 7.3.8.4* section.

7.3.8.4 Overtemperature Shutdown (OTS)

If the die temperature exceeds the thermal shutdown temperature, all FETs in the H-bridge are disabled and the charge pump shuts down. The nFAULT pin remains pulled low during this fault condition. When the die temperature falls below the hysteresis threshold, operation automatically resumes.

7.4 Device Functional Modes

The DRV8801A-Q1 device is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled and the H-bridge FETs are disabled hi-Z. The DRV8801A-Q1 device is brought out of sleep mode automatically if nSLEEP is brought logic high.

8 Application and Implementation

8.1 Application Information

The DRV8801A-Q1 device is used in medium voltage brushed-DC motor control applications.

8.2 Typical Application

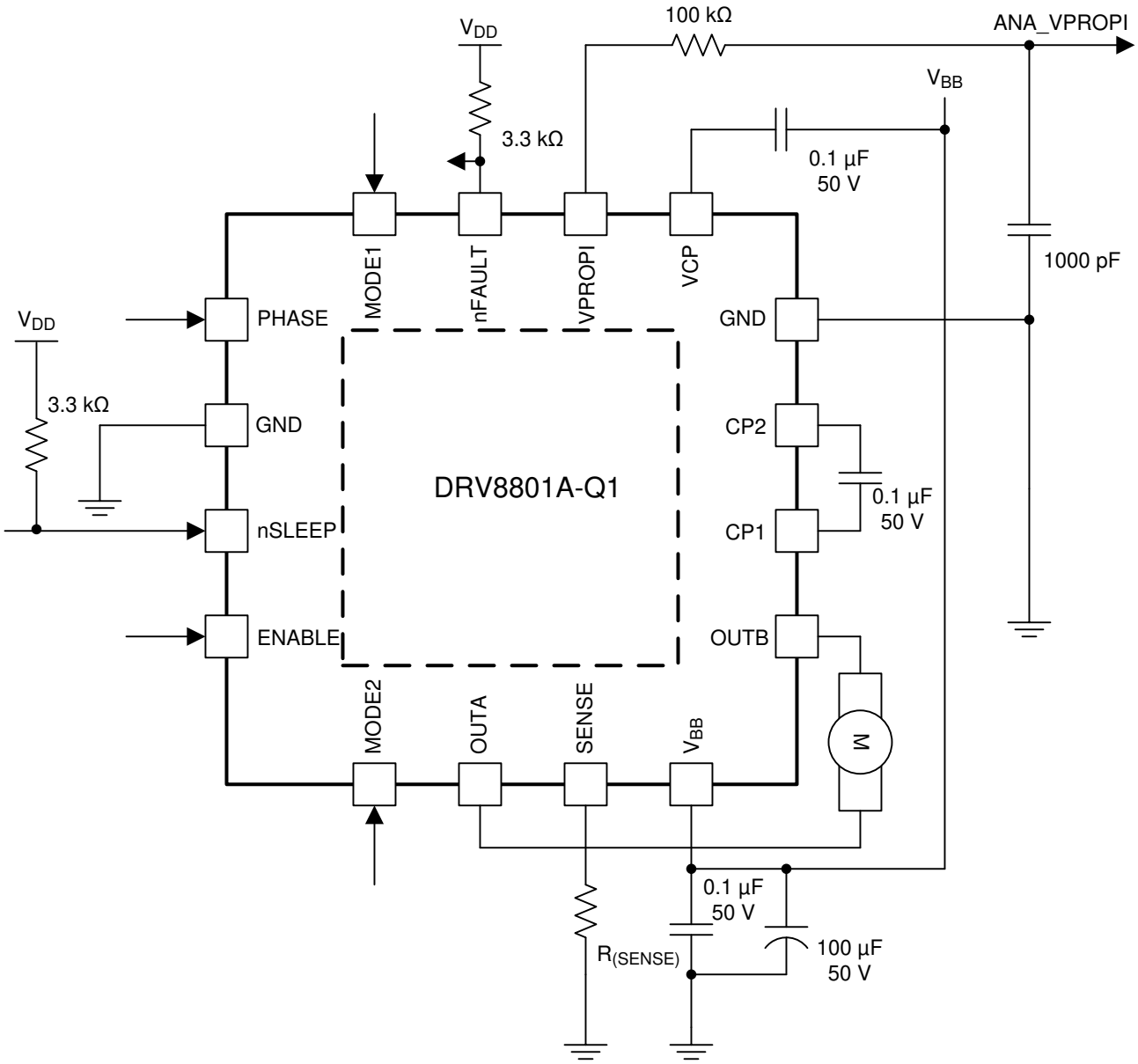


図 8-1. Typical Application Diagram

8.2.1 Design Requirements

The example supply voltage for this design is V_{BB} = 18 V.

8.2.2 Detailed Design Procedure

8.2.2.1 Drive Current

This current path is through the high-side sourcing DMOS driver, motor winding, and low-side sinking DMOS driver. Power dissipation I^2R losses in one source and one sink DMOS driver, as shown in 式 3.

8.2.2.2

$$P_D = I^2(r_{DS(on)Source} + r_{DS(on)Sink}) \quad (3)$$

8.2.2.3 Slow-Decay SR (Brake Mode)

In slow-decay mode, both low-side sinking drivers turn on, allowing the current to circulate through the low side of the H-bridge (two sink drivers) and the load. Power dissipation I^2R loses in the two sink DMOS drivers as shown in 式 4

$$P_D = I^2(2 \times r_{DS(on)Sink}) \quad (4)$$

8.2.3 Thermal Considerations

Although DRV8801A-Q1 is rated at 2.8-A of current handling, the previous only holds true as long as the internal temperature does not exceed 170°C. In order to operate at this rate, the following measures must be taken under consideration.

8.2.3.1 Junction-to-Ambiant Thermal Impedance (ϴJA)

At any given time during the steady state portion of the cycle, two FETs are enabled: A high side sourcing FET and a low side sinking FET. The increase in die temperature above ambient can be estimated by 式 5

$$T_{die} = \theta_{JA} \frac{^{o}C}{W} \times I_{winding}{}^{2} \times RDS_{ON} + T_A \quad (5)$$

8.2.4 Pulse-Width Modulating

8.2.4.1 Pulse-Width Modulating ENABLE

The most common H-Bridge direction/speed control scheme is to use a conventional GPIO output for the PHASE (selects direction) and pulse-width modulate ENABLE for speed control.

8.2.4.2 Pulse-Width Modulating PHASE

A technique that uses a speed/direction control scheme where ENABLE is connected to a GPIO output and the PHASE is pulse-width modulated. In this case, both direction and speed are controlled with a single signal. ENABLE is only used to disable the motor and stop all current flow.

When pulse-width modulating PHASE, a 50% duty cycle will stop the motor. Duty cycles above 50% will have the motor moving on the clockwise direction with proportional control; 100% duty cycle represents full speed.

Duty cycles below 50% will have the motor rotating with a counter clockwise direction; 0% duty cycle represents full speed.

8.2.5 Application Curves

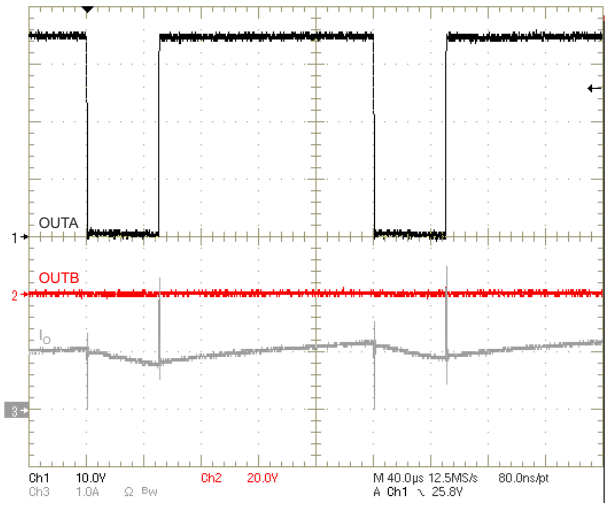


図 8-2. 75% Drive, 25% Slow Decay; $f_{(PWM)}$ = 5 kHz

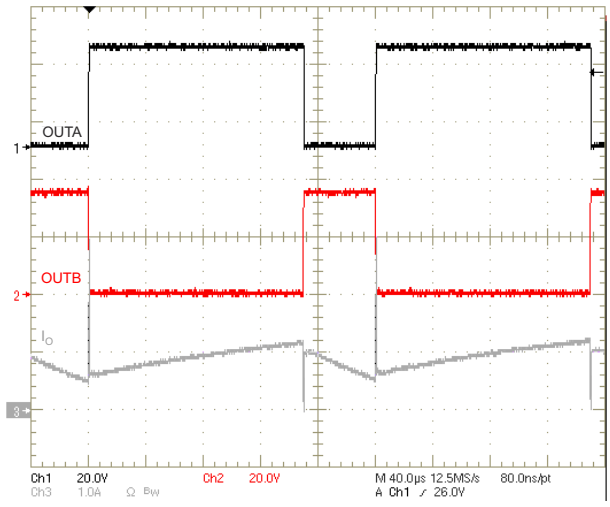


図 8-3. 75% Drive, 25% Fast Decay; $f_{(PWM)}$ = 5 kHz

8.3 Parallel Configuration

It is possible to drive higher than the 2.8 A of current by connecting more than one devices in parallel. To properly use this option the guidelines documented below must be followed.

8.3.1 Parallel Connections

図 8-4 shows the signals that need to be connected together. ENABLE, PHASE, MODE 1, MODE 2, nSLEEP, OUTA, OUTB, SENSE, VBB and GND.

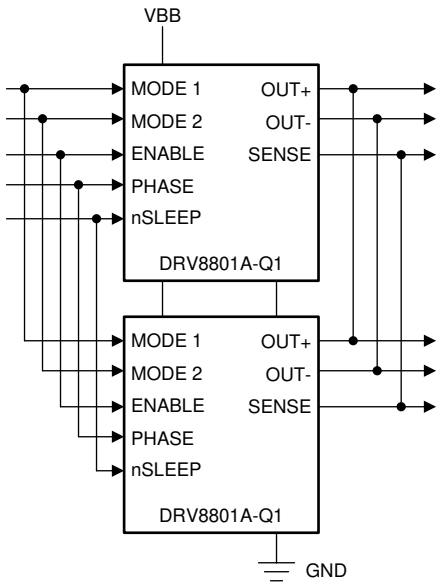


図 8-4. Functional Block Diagram (Connected Signals)

8.3.2 Non – Parallel Connections

図 8-5 shows the signals that should not be connected together and will be driven on an individual basis. These are: VCP, CP1, CP2, and VPROPI.

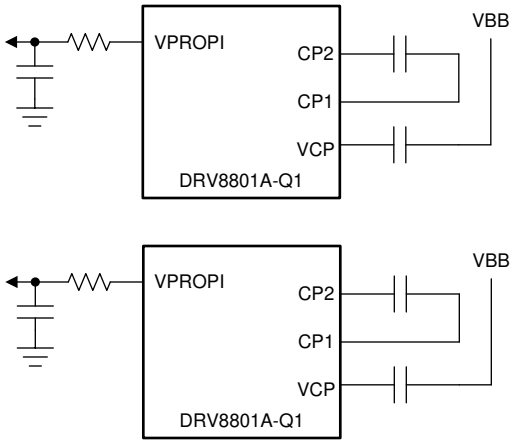


図 8-5. Functional Block Diagram (Individual Signals)

8.3.3 Wiring nFAULT as Wired OR

Since nFAULT is an open drain output, multiple nFAULT outputs can be paralleled with a single resistor. The end result is a wired OR configuration. When any individual nFAULT output goes to a logic low, the wired OR output will go to the same logic low. There is no need to determine which device signaled the fault condition, as once they are connected in parallel they function as a single device.

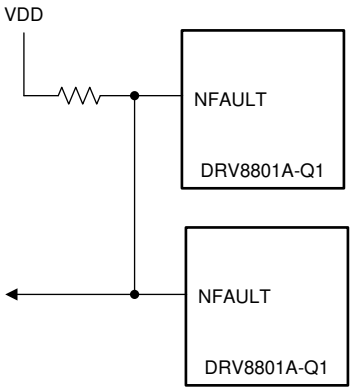


図 8-6. nFAULT as Wired OR

8.3.4 Electrical Considerations

8.3.4.1 Device Spacing

It is recommended that devices be connected as close as possible and with trace lengths as short as possible. Doing this minimizes the potential of generating timing differences between devices. Although it may seem like a harmful situation for the power stage, DRV8801A-Q1 contains enough protection to effectively deal with enable time skews from device to device. This consideration focuses on motion quality, as total current needed for acceleration and proper speed control will only be available when all power stages are brought online.

8.3.4.2 Recirculation Current Handling

During recirculation, it is not possible to synchronize all devices connected in parallel so that the current is equally distributed. Also, during the asynchronous portion of the current decay, the body diode with the lowest forward voltage will start conducting and sink all of the current. Said body diode is not meant to handle the new increased current capacity and will be severely affected if allowed to sink current of said magnitude.

In order to assure proper operation when devices are connected in parallel, it is imperative that external schottky diodes be used. These schottky diodes will conduct during the asynchronous portion of the recirculation mode and will sink the inductive load current until the respective FET switches are brought online.

Schottky diodes should be connected as shown in 図 8-7.

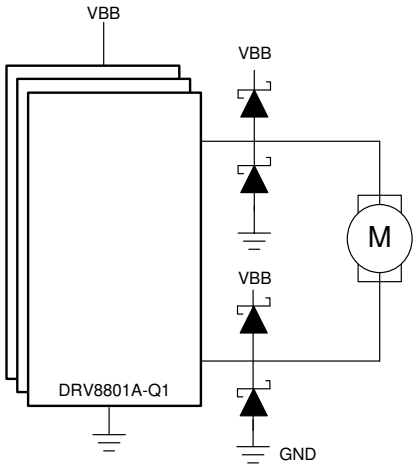


図 8-7. Schottky Diodes Connection

8.3.4.3 Sense Resistor Selection

The guideline for the SENSE resistor chosen doesn't change in parallel mode. As the goal of this configuration is to evenly distribute the current load across multiple devices, each device should be configured with the same I_{TRIP} setting. Therefore, the same SENSE resistor should be used for all devices connected in parallel.

Connection of the SENSE resistors should be as shown in 図 8-8.

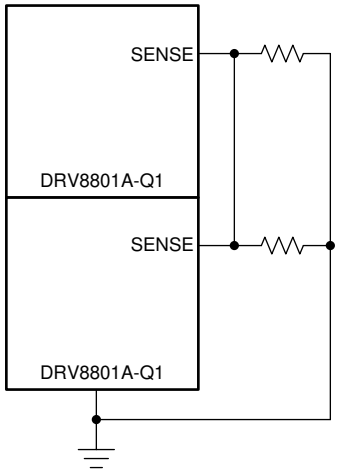


図 8-8. SENSE Resistors Connection

8.3.4.4 Maximum System Current

The idea behind placing multiple devices in parallel is to increase maximum drive current. At first glance, it may seem that the new increased I_{TRIP} setting is given by 式 6.

$$\text{System}I_{TRIP} = \left(I_{TRIP} \times N\right) \tag{6}$$

Where:

N is the number of devices connected in parallel.

I_{TRIP} is the individual I_{TRIP} value per device.

However, although in theory accurate, due to tolerances in internal SENSE amplifier/comparator circuitry, the system I_{TRIP} should be expected to be less than the addition of all the individual I_{TRIP}. The reason for this is that as soon as one of the devices senses a current for which the H Bridge should be disabled, the remaining devices will end up having to conduct the same current but with less capacity. Therefore, remaining devices are expected to get disabled shortly after.

A good rule of thumb is to expect 90% of the theoretical maximum.

By way of example, if the system level requirements indicate that 6 A of current are required to meet the motion control requirements, then:

6 A = (2.8 A x 0.9)N

N = (6 A) / (2.8 A x 0.9)

N = 2.38

In this example, three devices would be required to safely meet the needs of the system.

9 Power Supply Recommendations

The DRV8801A-Q1 device is designed to operate from an input-voltage supply (V_{BB}) range between 6.5 V and 36 V. One 0.1-µF ceramic capacitor rated for V_{BB} must be placed as close as possible to the V_{BB} pin. In addition to the local decoupling caps, additional bulk capacitance is required and must be sized accordingly to the application requirements.

9.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. This sizing is dependent on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value but system-level testing is required to determine the appropriate sized bulk capacitor.

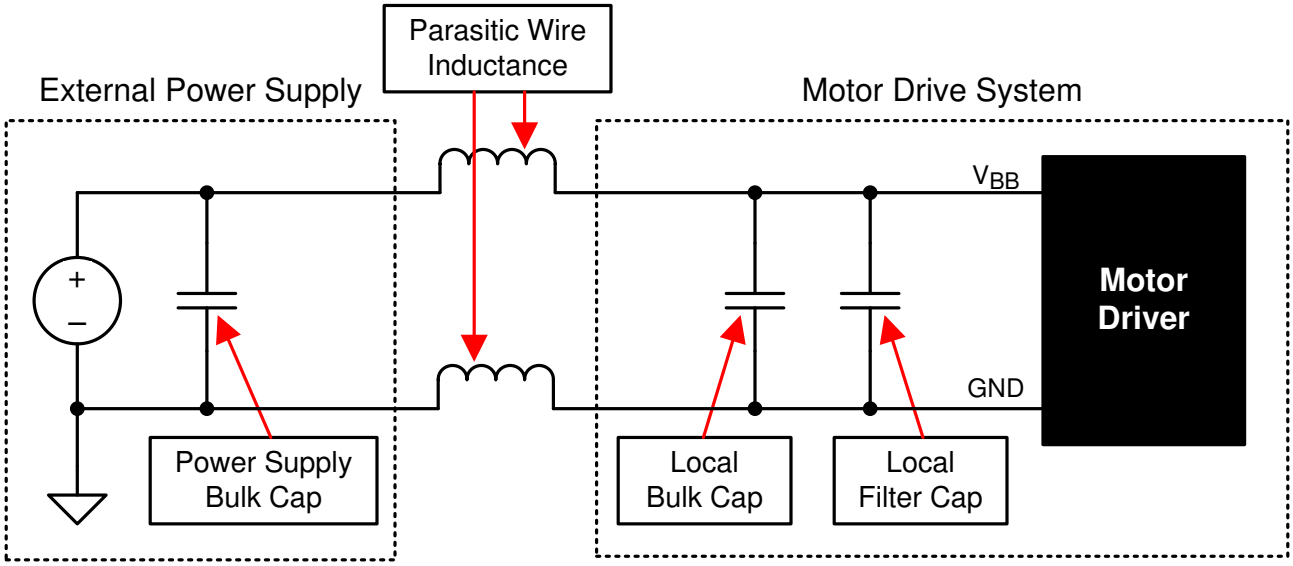


図 9-1. Bulk Capacitance

10 Layout

10.1 Layout Guidelines

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8801A-Q1 device must be soldered directly onto the board. On the bottom side of the DRV8801A-Q1 device is a thermal pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB. For more information on this technique, refer to *QFN/SON PCB Attachment*.

The load supply pin, V_{BB}, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a ceramic capacitor placed as close as possible to the device. In order to minimize lead inductance, the ceramic capacitors between the VCP and V_{BB} pins, connected to the REG pin, and the capacitors between the CP1 and CP2 pins should be as close to the pins of the device as possible.

10.2 Layout Example

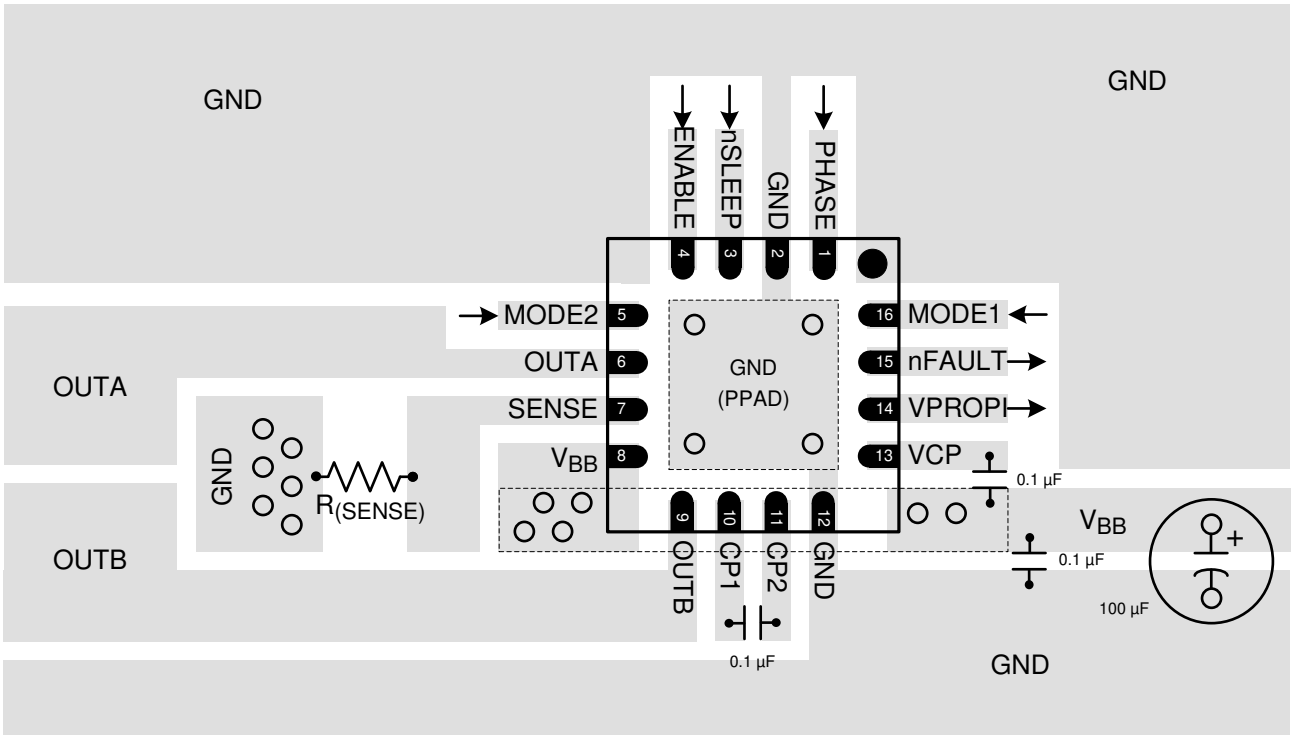


図 10-1. DRV8801A-Q1 Layout

10.3 Power Dissipation

First-order approximation of power dissipation in the DRV8801A-Q1 device can be calculated by examining the power dissipation in the full-bridge during each of the operation modes. The DRV8801A-Q1 device uses synchronous rectification. During the decay cycle, the body diode is shorted by the low-$r_{DS(on)}$ driver, which in turn reduces power dissipation in the full-bridge. In order to prevent shoot through (high-side and low-side drivers on the same side are ON at the same time), the DRV8801A-Q1 device implements a 500-ns typical crossover delay time. During this period, the body diode in the decay current path conducts the current until the DMOS driver turns on. High-current and high-ambient-temperature applications should take this into consideration. In addition, motor parameters and switching losses can add power dissipation that could affect critical applications.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

QFN/SON PCB Attachment

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Community Resources

11.5 Trademarks

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11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8801AQRMJRQ1	ACTIVE	WQFN	RMJ	16	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8801 ARMJQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

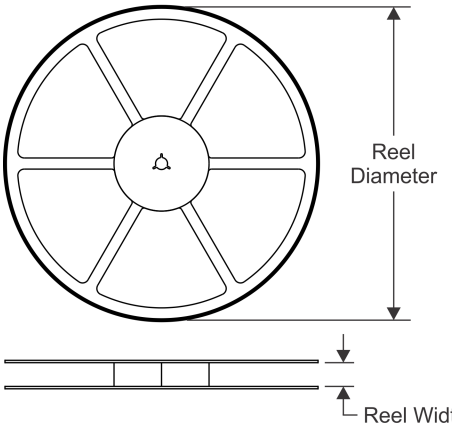
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

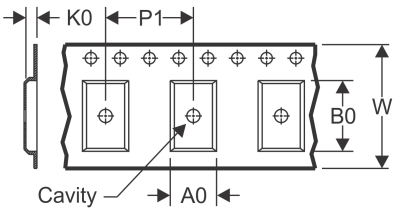
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

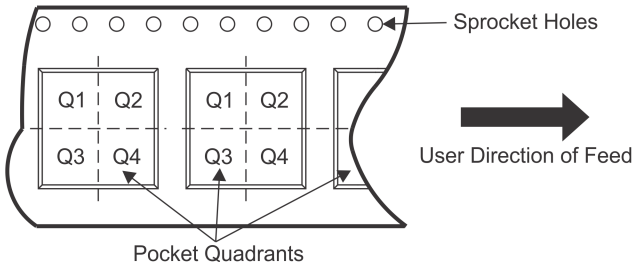


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

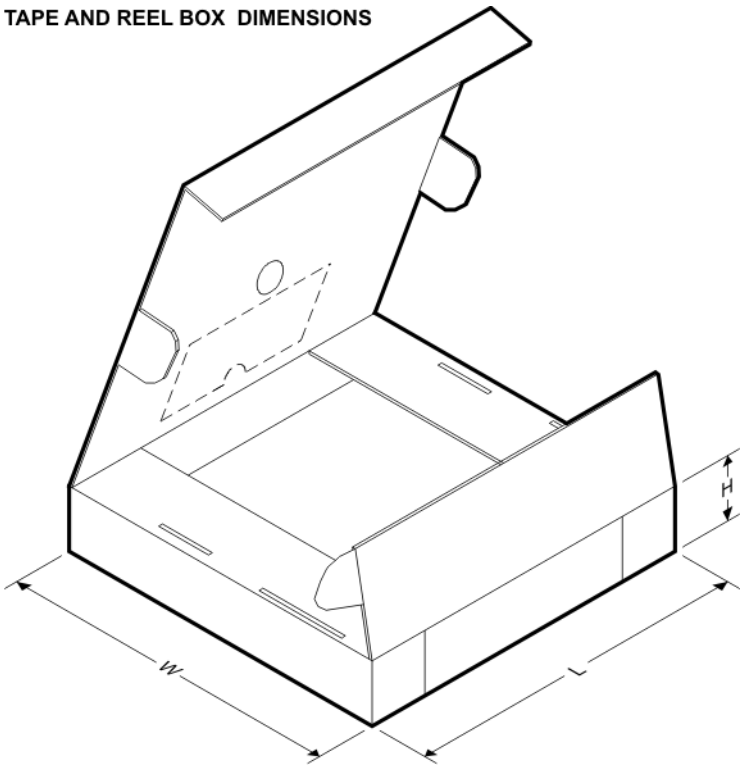
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8801AQRMJRQ1	WQFN	RMJ	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

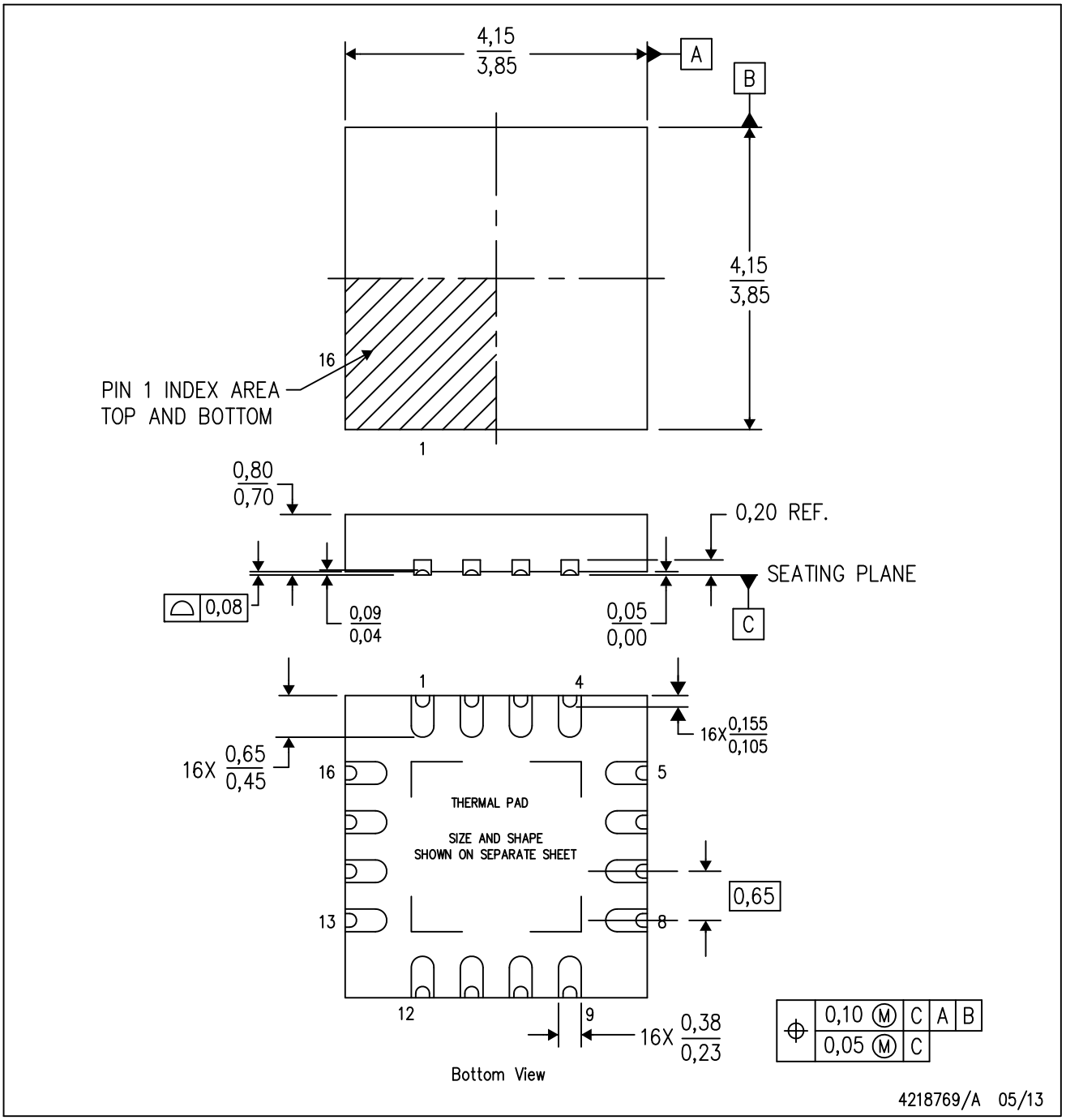
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8801AQRMJRQ1	WQFN	RMJ	16	3000	367.0	367.0	35.0

RMJ (S–PWQFN–N16) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

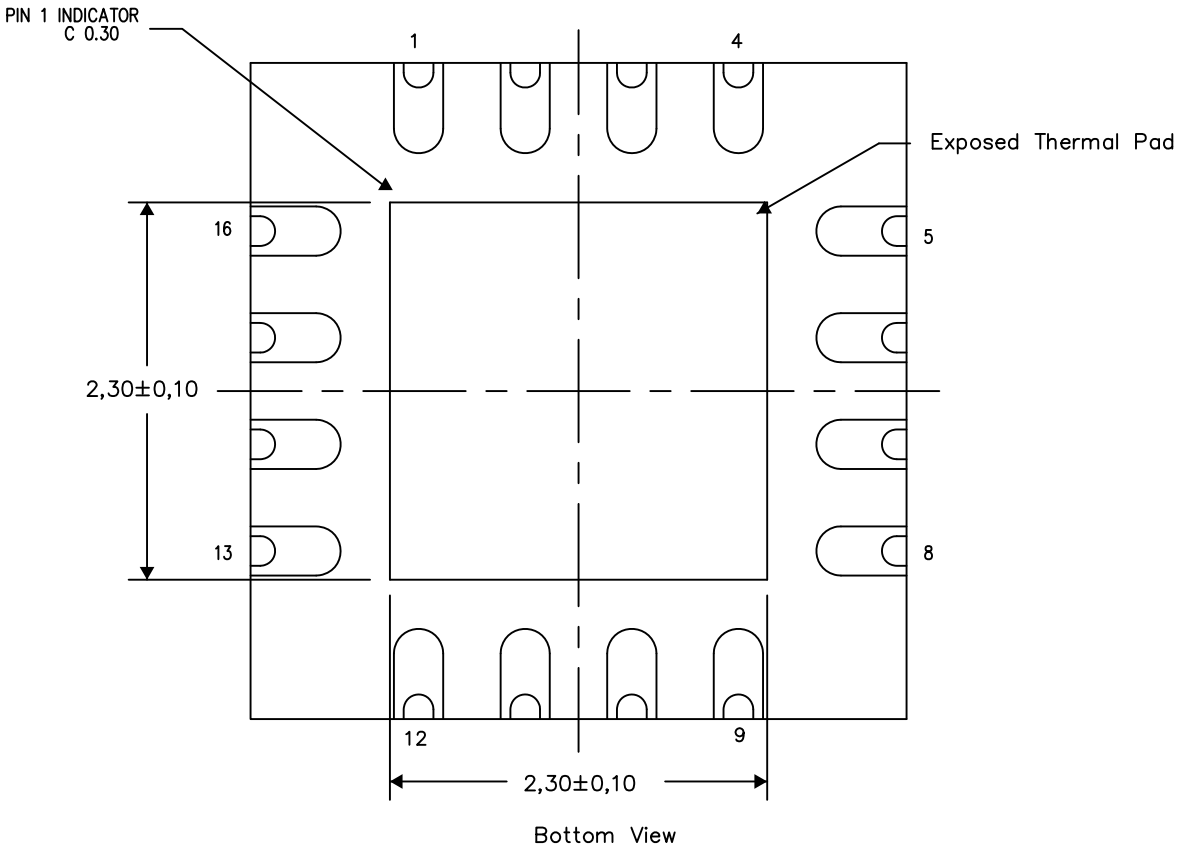
RMJ (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4219300/A 07/13

NOTE: All linear dimensions are in millimeters

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