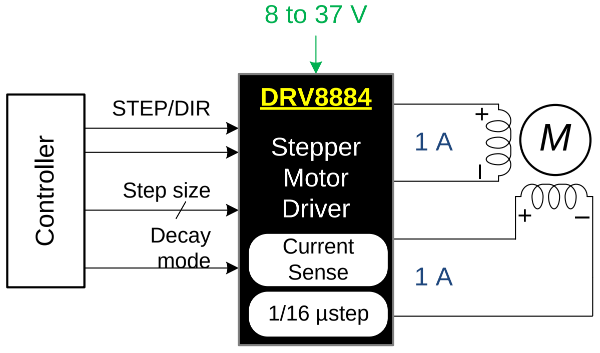
DRV8884 電流検出機能搭載の1.0Aステッピング・モータ・ドライバ

1 特長

- PWMマイクロステッピングのステッピング・モータ・ドライバ
  - 最高1/16のマイクロステッピング
  - 非循環および標準の½ステップ・モード
- 電流検出機能を搭載
  - 検出抵抗が不要
  - ±6.25%のフルスケール電流精度
- 低速および混合減衰オプション
- 8.0～37Vの電源電圧範囲で動作
- 低い$R_{DS(ON)}$: 24V、25℃で1.4Ω HS + LS
- 高い電流容量
  - ブリッジごとにフルスケールで1.0A
  - ブリッジごとにrms 0.7A
- 固定オフ時間のPWMチョッピング
- シンプルなSTEP/DIRインターフェイス
- 低消費電流のスリープ・モード(20µA)
- 小さなパッケージと占有面積
  - 24 HTSSOP PowerPAD™パッケージ
  - 28 WQFNパッケージ
- 保護機能
  - VM低電圧誤動作防止(UVLO)
  - チャージ・ポンプ低電圧(CPUV)
  - 過電流保護(OCP)
  - サーマル・シャットダウン(TSD)
  - フォルト状況表示ピン(nFAULT)

概略回路図



2 アプリケーション

- 多機能プリンタおよびスキャナ
- レーザー・ビーム・プリンタ
- 3Dプリンタ
- 現金自動預払機および金銭処理機
- 防犯カメラ
- OA機器
- ファクトリ・オートメーションおよびロボティクス

3 概要

DRV8884は、産業用機器アプリケーション向けのステッピング・モータ・ドライバです。このデバイスには2つのNチャネル・パワーMOSFET Hブリッジ・ドライバ、マイクロステッピング・インデクサ、および電流検出機能が組み込まれています。DRV8884は、フルスケールで1.0A、rmsで0.7Aまでの出力電流を供給できます(24VおよびT_A = 25℃の場合。放熱のため適切なPCBグランド・プレーンが必要です)。

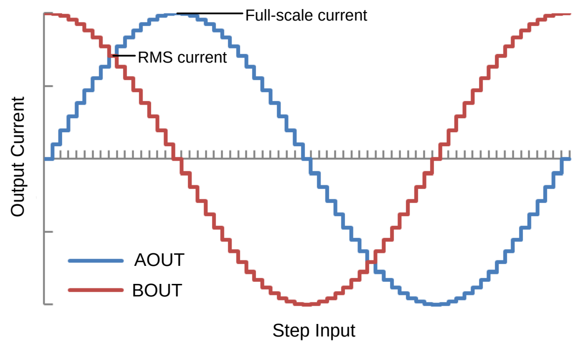
DRV8884には電流検出機能が組み込まれているため、2つの外部検出抵抗が必要ありません。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DRV8884	HTSSOP (24)	7.80mm×4.40mm
	WQFN (28)	5.50mm×3.5mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

マイクロステッピング電流の波形



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (July 2018) から Revision D に変更 — Page

- デバイスのステータスを「事前情報」から「量産データ」に 変更 1

Revision B (April 2016) から Revision C に変更 — Page

- WQFNパッケージ・オプション 追加 1
- Deleted *and internal indexer* from the description of the ENABLE pin in the *Pin Functions* table 4
- Changed *until ENABLE is deasserted* to *until ENABLE is asserted* in the *Device Functional Modes* section 27
- 追加 「*ドキュメントの更新通知を受け取る方法*」セクション 33

Revision A (March 2016) から Revision B に変更 — Page

- Updated R_{PD} and R_{PU} values 7
- Fixed chopping current equation 19
- Added "Controlling RREF with a PWM Resource" 19
- Fixed resistance values in tri-level input pin diagram 25

2016年1月発行のものから更新 — Page

- デバイスのステータスを製品プレビューから量産データへ 変更 3

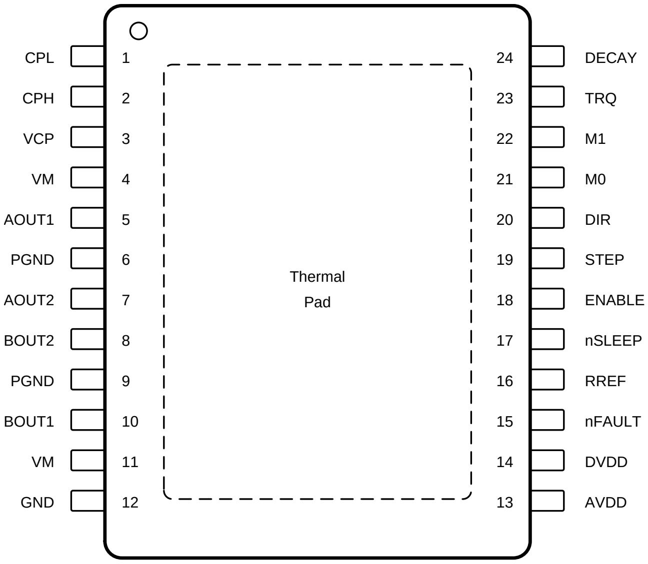
5 概要（続き）

STEP/DIRピンは、シンプルな制御インターフェイスとして使用できます。デバイスは、フルステップから1/16ステップまでのモードに構成可能です。低消費電力のスリープ・モードが用意されており、専用のnSLEEPピンを使用することで、静止電流の非常に低いスタンバイ・モードに移行できます。

低電圧、チャージ・ポンプ障害、過電流、短絡、過熱への保護機能が内蔵されています。フォルト状況は、nFAULTピンにより示されます。

6 Pin Configuration and Functions

PWP PowerPAD™ Package
24-Pin HTSSOP
Top View



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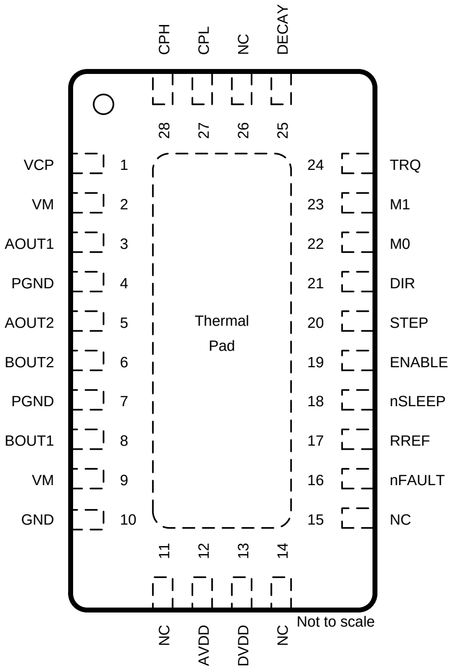
RHR Package
28-Pin WQFN With Exposed Thermal Pad
Top View



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Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	HTSSOP	WQFN		
AOUT1	5	3	O	Winding A output. Connect to stepper motor winding.
AOUT2	7	5		
AVDD	13	12	PWR	Internal regulator. Bypass to GND with a X5R or X7R, 0.47-μF, 6.3-V ceramic capacitor.
BOUT1	10	8	O	Winding B output. Connect to stepper motor winding.
BOUT2	8	6		
CPH	2	28	PWR	Charge pump switching node. Connect a X5R or X7R, 0.022-μF, VM-rated ceramic capacitor from CPH to CPL.
CPL	1	27		
DECAY	24	25	I	Decay-mode setting. Sets the decay mode (see the *Decay Modes* section). Decay mode can be adjusted during operation.
DIR	20	21	I	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
DVDD	14	13	PWR	Internal regulator. Bypass to GND with a X5R or X7R, 0.47-μF, 6.3-V ceramic capacitor.
ENABLE	18	19	I	Enable driver input. Logic high to enable device outputs; logic low to disable; internal pulldown resistor.
GND	12	10	PWR	Device ground. Connect to system ground.
M0	21	22	I	Microstepping mode-setting. Sets the step mode; tri-level pins; sets the step mode; internal pulldown resistor.
M1	22	23		
NC	—	11	—	No connect. No internal connection
		14		
		15		
		26		
PGND	6	4	PWR	Power ground. Connect to system ground.
	9	7		
RREF	16	17	I	Current-limit analog input. Connect a resistor to ground to set full-scale regulation current.

(1) I = input, O = output, PWR = power, OD = open-drain

Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	HTSSOP	WQFN		
STEP	19	20	I	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.
TRQ	23	24	I	Current-scaling control. Scales the output current; tri-level pin.
VCP	3	1	PWR	Charge pump output. Connect a X5R or X7R, 0.22-μF, 16-V ceramic capacitor to VM.
VM	4	2	PWR	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-μF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
	11	9		
nFAULT	15	16	OD	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	17	18	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	40	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (VCP, CPH)	–0.3	VM + 7	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal regulator voltage (DVDD)	–0.3	3.8	V
Internal regulator current output (DVDD)	0	1	mA
Internal regulator voltage (AVDD)	–0.3	5.7	V
Control pin voltage (STEP, DIR, ENABLE, nFAULT, M0, M1, DECAY, TRQ, nSLEEP)	–0.3	5.7	V
Open drain output current (nFAULT)	0	10	mA
Current limit input pin voltage (RREF)	–0.3	6.0	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.7	VM + 0.7	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)		1.7	A
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Power supply voltage	8	37	V
VCC	Logic level input voltage	0	5.3	V
f_{PWM}	Applied STEP signal (STEP)	0	100 (1)	kHz
I_{DVDD}	DVDD external load current	0	1 (2)	mA
I_{FS}	Motor full scale current	0	1.0	A
I_{rms}	Motor rms current	0	0.7	A
T_A	Operating ambient temperature	–40	125	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC (1)		DRV8884		UNIT
		PWP (HTSSOP)	RHR (WQFN)	
		24 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.1	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.3	23.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	12.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	12.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD, AVDD)						
VVM	VM operating voltage		8		37	V
I_{VM}	VM operating supply current	VM ≈ 8 to 35 V, ENABLE = 1, nSLEEP = 1, No motor load		5	8	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0; T_A = 25°C			20	μA
		nSLEEP = 0; T_A = 125°C (1)			40	
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode		50	200	μs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.85	1.5	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.85	1.5	ms
V_{DVDD}	Internal regulator voltage	0- to 1-mA external load	2.9	3.3	3.6	V
V_{AVDD}	Internal regulator voltage	No external load	4.5	5.0	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	VM > 8 V		VM + 5.5		V
LOGIC-LEVEL INPUTS (STEP, DIR, ENABLE, nSLEEP, M1)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.6		5.3	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	VIN = 0 V	–1		1	μA
I_{IH}	Input logic high current	VIN = 5.0 V			100	μA
R_{PD}	Pulldown resistance	To GND		100		kΩ
t_{PD}	Propagation delay	STEP to current change			1.2	μs
TRI-LEVEL INPUT (M0, TRQ)						
V_{IL}	Tri-level input logic low voltage		0		0.65	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.5		5.3	V
I_{IL}	Tri-level input logic low current	VIN = 0 V	–80			μA
I_{IZ}	Tri-level input Hi-Z current	VIN = 1.3 V	–5		5	μA
I_{IH}	Tri-level input logic high current	VIN = 5.0 V			155	μA
R_{PD}	Tri-level pulldown resistance	To GND	18	32	50	kΩ
R_{PU}	Tri-level pullup resistance	To DVDD	30	60	90	kΩ
QUAD-LEVEL INPUT (DECAY)						
V_{I1}	Quad-level input voltage 1	5% resistor 5 kΩ to GND	0.07	0.11	0.13	V
V_{I2}	Quad-level input voltage 2	5% resistor 15 kΩ to GND	0.24	0.32	0.40	V
V_{I3}	Quad-level input voltage 3	5% resistor 45 kΩ to GND	0.71	0.97	1.20	V
V_{I4}	Quad-level input voltage 4	5% resistor 135 kΩ to GND	2.12	2.90	3.76	V
I_O	Output current	To GND	14	22	30	μA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 1 mA, R_{PULLUP} = 4.7 kΩ			0.5	V
I_{OH}	Output logic high leakage	V_O = 5.0 V, R_{PULLUP} = 4.7 kΩ	–1		+1	μA

(1) Not tested in production; limits are based on characterization data

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 24 V, I = 1 A, T_A = 25°C		716	798	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 24 V, I = 1 A, T_A = 25°C		684	749	mΩ
t_{RISE} (2)	Output rise time			100		ns
t_{FALL} (2)	Output fall time			100		ns
t_{DEAD} (2)	Output dead time			200		ns
V_d (2)	Body diode forward voltage	I_{OUT} = 0.5 A		0.7	1.0	V
PWM CURRENT CONTROL (RREF)						
A_{RREF}	RREF transimpedance gain		28.1	30	31.9	kAΩ
V_{RREF}	RREF voltage	RREF = 27 to 132 kΩ	1.18	1.232	1.28	V
t_{OFF}	PWM off-time			20		µs
C_{RREF}	Equivalent capacitance on RREF				10	pF
t_{BLANK}	PWM blanking time	I_{RREF} = 1.0 A, 63% to 100% current setting		1.5		µs
		I_{RREF} = 1.0 A, 0% to 63% current setting		1.0		
ΔI_{TRIP}	Current trip accuracy	I_{RREF} = 1.0 A, 10% to 20% current setting, 1% reference resistor	–25%		25%	
		I_{RREF} = 1.0 A, 20% to 63% current setting, 1% reference resistor	–12.5%		12.5%	
		I_{RREF} = 1.0 A, 71% to 100% current setting, 1% reference resistor	–6.25%		6.25%	
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO	VM falling; UVLO report			7.8	V
		VM rising; UVLO recovery			8.0	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 2.0		V
I_{OCP}	Overcurrent protection trip level	Current through any FET	1.7			A
t_{OCP}	Overcurrent deglitch time		1.3	1.9	2.8	µs
t_{RETRY}	Overcurrent retry time		1		1.6	ms
T_{TSD} (2)	Thermal shutdown temperature	Die temperature T_J	150			°C
T_{HYS} (2)	Thermal shutdown hysteresis	Die temperature T_J		20		°C

(2) Not tested in production; limits are based on characterization data

7.6 Indexer Timing Requirements

T_A = 25°C, over recommended operating conditions unless otherwise noted

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500 (1)	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR or USMx to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR or USMx to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load

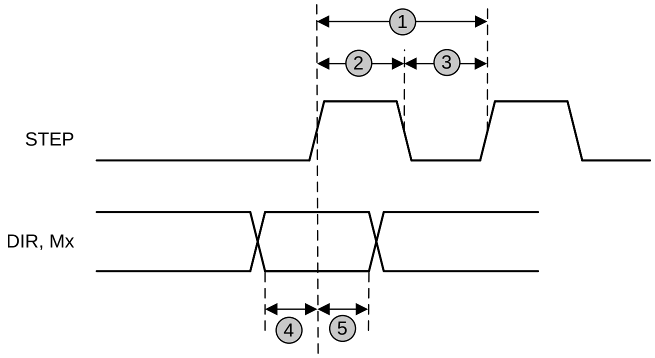


Figure 1. Timing Diagram

7.7 Typical Characteristics

Over recommended operating conditions (unless otherwise noted)

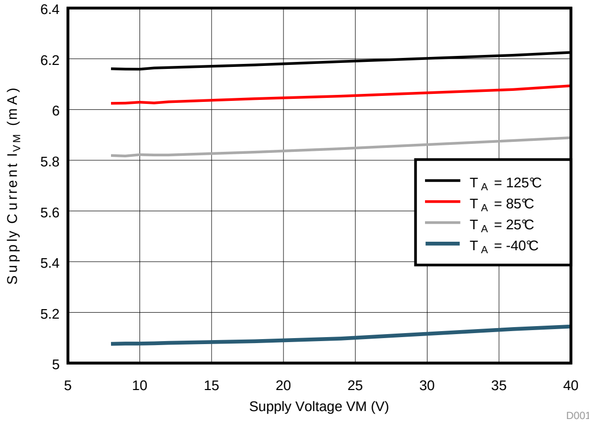


Figure 2. Supply Current over VM

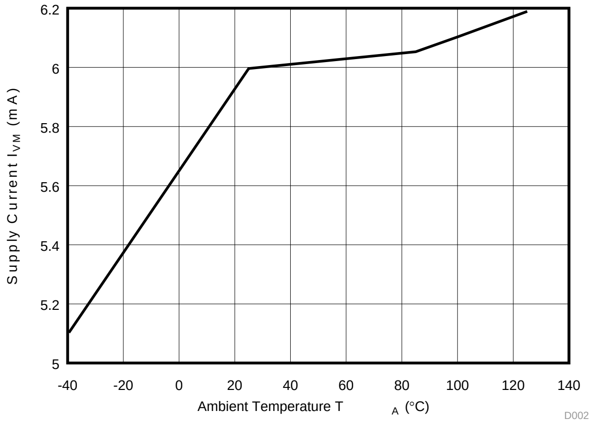


Figure 3. Supply Current over Temperature (VM = 24 V)

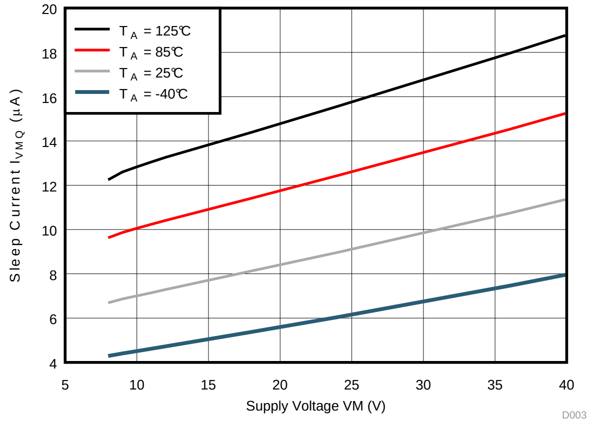


Figure 4. Sleep Current over VM

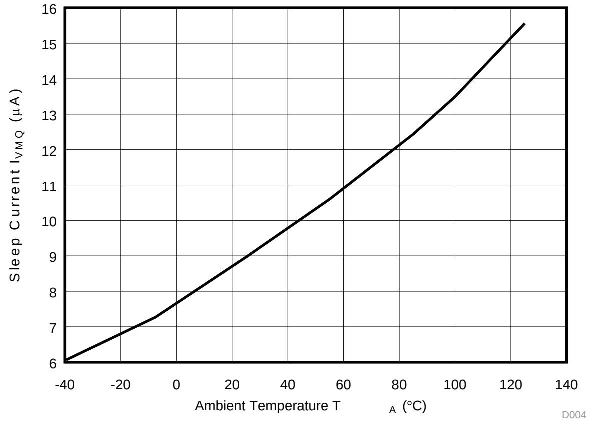


Figure 5. Sleep Current over Temperature (VM = 24 V)

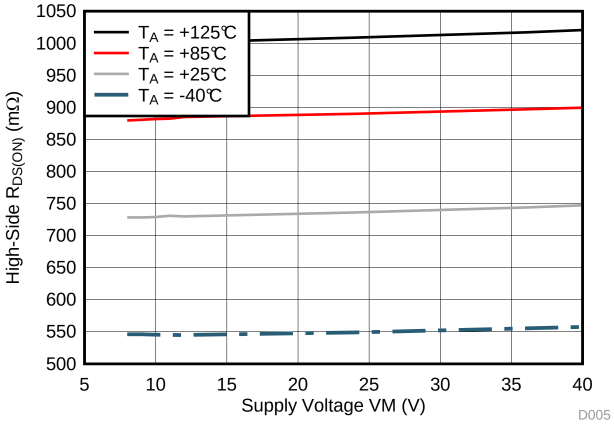


Figure 6. High-Side $R_{DS(ON)}$ over VM

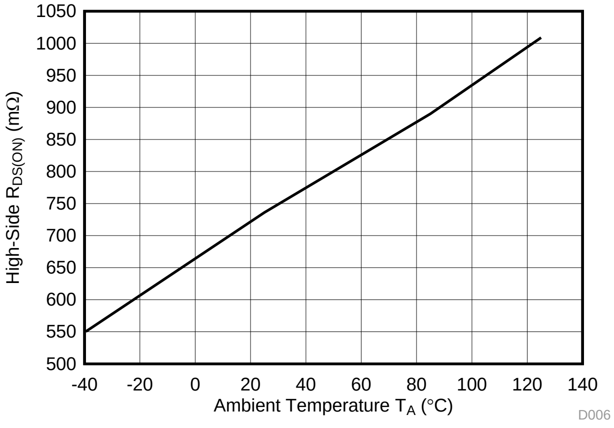


Figure 7. High-Side $R_{DS(ON)}$ over Temperature (VM = 24 V)

Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)

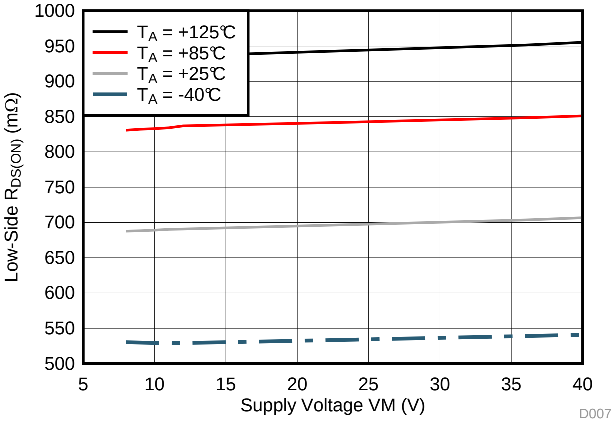


Figure 8. Low-Side $R_{DS(ON)}$ over VM

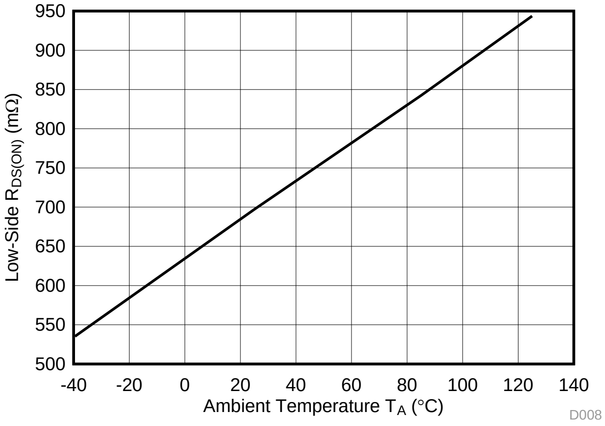


Figure 9. Low-Side $R_{DS(ON)}$ over Temperature (VM = 24 V)

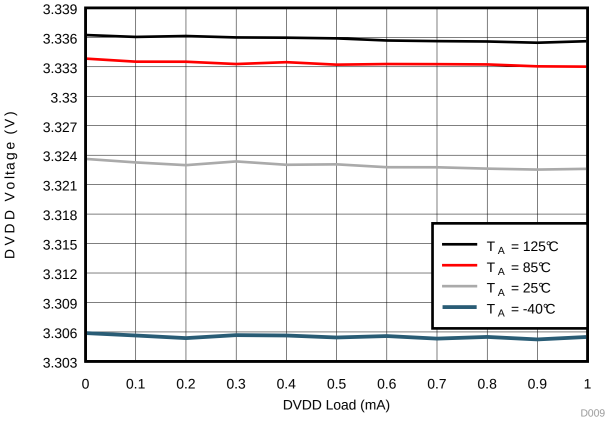


Figure 10. DVDD Regulator over Load (VM = 24 V)

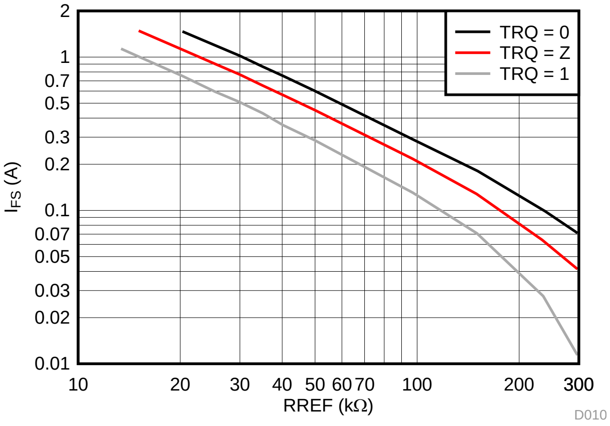


Figure 11. Full-Scale Current over RREF Selection

8 Detailed Description

8.1 Overview

The DRV8884 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8884 can be powered with a supply voltage between 8 and 37 V, and is capable of providing an output current with up to 1.7-A peak, 1.0-A full-scale, or 0.7-A rms. Actual full-scale and rms current depends on ambient temperature, supply voltage, and PCB ground plane size.

The DRV8884 integrates current sense functionality, which eliminates the need for high-power external sense resistors. This integration does not dissipate the external sense resistor power, because the current sense functionality is not implemented using a resistor-based architecture. This functionality helps improve component cost, board size, PCB layout, and system power consumption.

A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level. The indexer is capable of full step and half step as well as microstepping to 1/4, 1/8, and 1/16. In addition to the standard half-stepping mode, a non-circular 1/2-stepping mode is available for increased torque output at higher motor rpm.

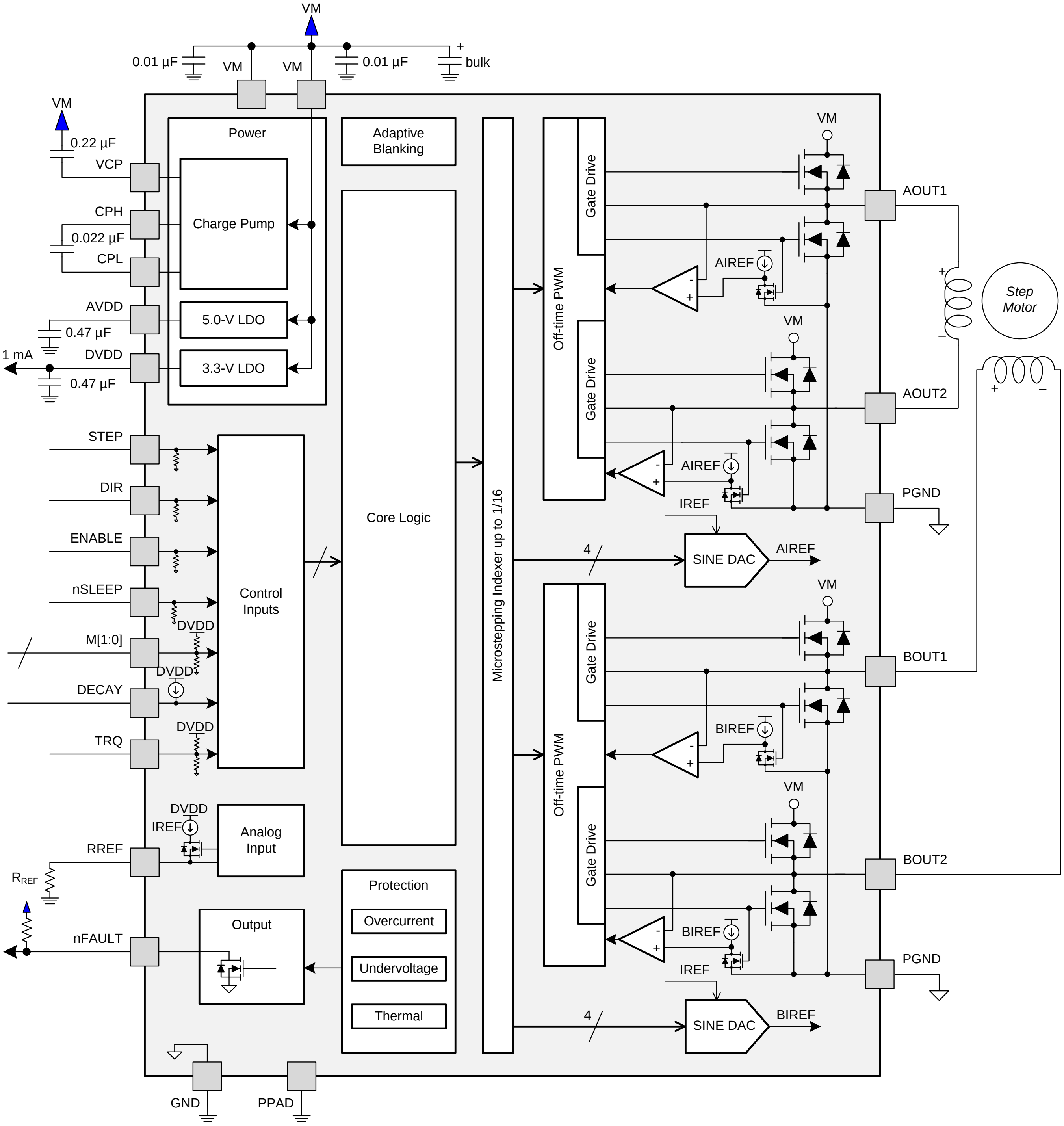
The current regulation is configurable with several decay modes of operation. The decay mode can be selected as a fixed slow, slow/mixed, or mixed decay. The slow/mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps.

An adaptive blanking time feature automatically scales the minimum drive time with output current. This helps alleviate zero-crossing distortion by limiting the drive time at low-current steps.

A torque DAC feature allows the controller to scale the output current without needing to scale the reference resistor. The torque DAC is accessed using a digital input pin. This allows the controller to save power by decreasing the current consumption when not high current is not required.

A low-power sleep mode is included that allows the system to save power when not driving the motor.

8.2 Functional Block Diagram



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8.3 Feature Description

Table 1 lists the recommended external components for the DRV8884 device.

Table 1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	Two 0.01-µF ceramic capacitors rated for VM
C_{VM}	VM	GND	Bulk electrolytic capacitor rated for VM
C_{VCP}	VCP	VM	16-V, 0.22-µF ceramic capacitor
C_{SW}	CPH	CPL	0.022-µF X7R capacitor rated for VM
C_{AVDD}	AVDD	GND	6.3-V, 0.47-µF ceramic capacitor
C_{DVDD}	DVDD	GND	6.3-V, 0.47-µF ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	>4.7 kΩ
R_{REF}	RREF	GND	Resistor to limit chopping current must be installed. See the *Typical Application* section for value selection.

(1) VCC is not a pin on the DRV8884, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

8.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

8.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold, I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general, the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver. For the DRV8884, the peak current rating is 1.7 A per bridge.

8.3.1.2 RMS Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The real operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8884, the rms current rating is 0.7 A per bridge.

8.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the IC. The full-scale current rating is approximately $\sqrt{2} \times I_{rms}$. The full-scale current is set by VREF, the sense resistor, and torque DAC when configuring the DRV8884 (see *Current Regulation* for details). For the DRV8884, the full-scale current rating is 1.0 A per bridge.

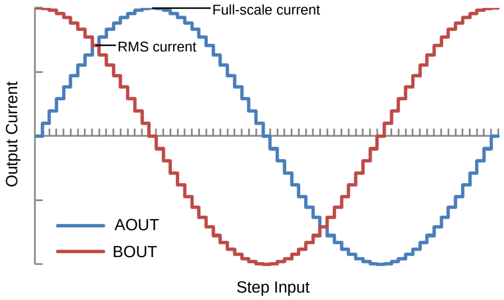

Figure 12. Full-Scale and rms Current

8.3.2 PWM Motor Drivers

The DRV8884 contains drivers for two full H-bridges. Figure 13 shows a block diagram of the circuitry.

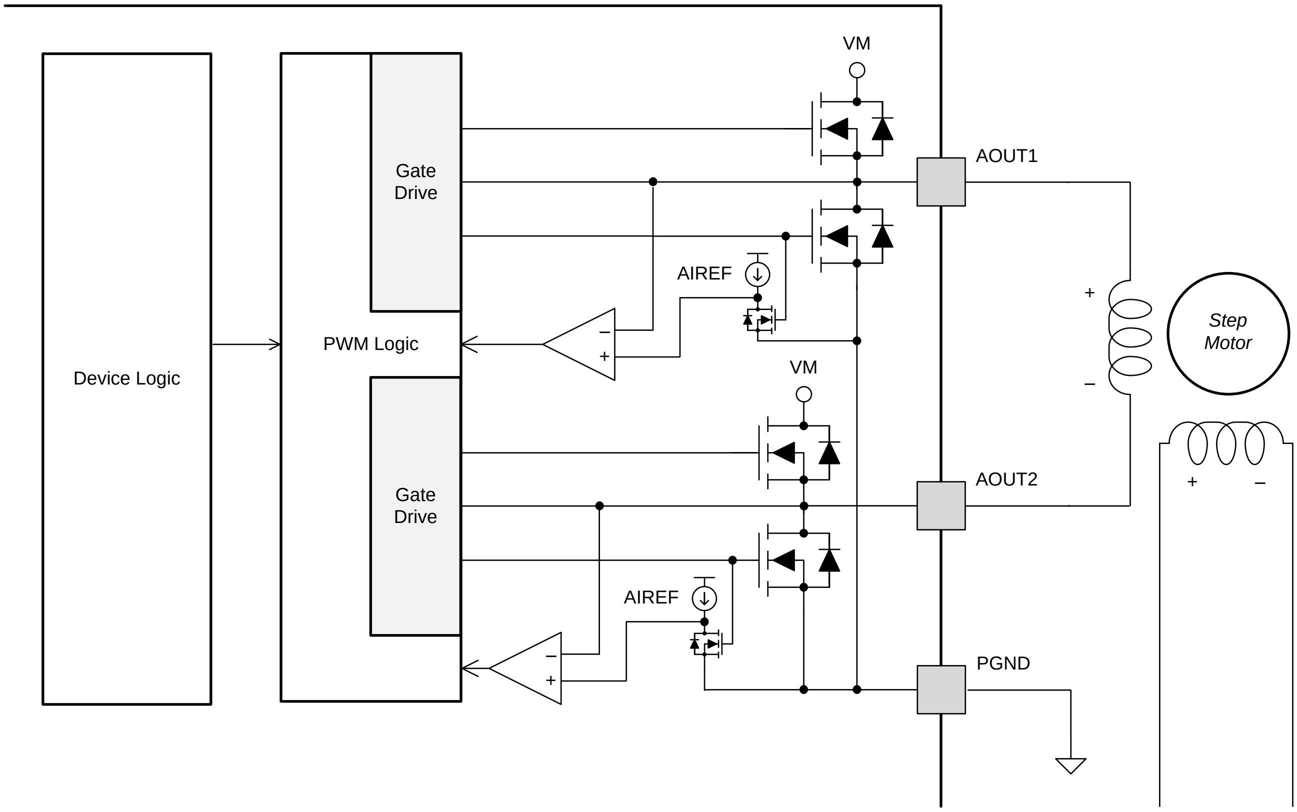

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Figure 13. PWM Motor Driver Block Diagram

8.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8884 allows a number of different stepping configurations. The Mx pins are used to configure the stepping format as shown in Table 2.

Table 2. Microstepping Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

Table 3 shows the relative current and step directions for full-step through 1/16-step operation. The AOUT current is the sine of the electrical angle; BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from xOUT1 to xOUT2 while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table (see Table 3). The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

On power-up or when exiting sleep mode, keep the STEP pin logic low, otherwise the indexer will advance one step.

Note that if the step mode is changed from full, 1/2, 1/4, 1/8, or 1/16 to full, 1/2, 1/4, 1/8, or 1/16 while stepping, the indexer will advance to the next valid state for the new MODE setting at the rising edge of STEP. If the step mode is changed from or to non-circular 1/2 step, the indexer will immediately go to the valid state for that mode.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout (UVLO), or after exiting sleep mode. Table 3 shows this state with the cells outlined in red.

Table 3. Microstepping Relative Current per Step (DIR = 1)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
	1	1	1	1	0.000°	0%	100%
				2	5.625°	10%	100%
			2	3	11.250°	20%	98%
				4	16.875°	29%	96%
		2	3	5	22.500°	38%	92%
				6	28.125°	47%	88%
			4	7	33.750°	56%	83%
				8	39.375°	63%	77%
1	2	3	5	9	45.000°	71%	71%
				10	50.625°	77%	63%
			6	11	56.250°	83%	56%
				12	61.875°	88%	47%
		4	7	13	67.500°	92%	38%
				14	73.125°	96%	29%
			8	15	78.750°	98%	20%
				16	84.375°	100%	10%
	3	5	9	17	90.000°	100%	0%
				18	95.625°	100%	–10%
			10	19	101.250°	98%	–20%
				20	106.875°	96%	–29%
		6	11	21	112.500°	92%	–38%
				22	118.125°	88%	–47%
			12	23	123.750°	83%	–56%
				24	129.375°	77%	–63%
2	4	7	13	25	135.000°	71%	–71%
				26	140.625°	63%	–77%
			14	27	146.250°	56%	–83%
				28	151.875°	47%	–88%
		8	15	29	157.500°	38%	–92%
				30	163.125°	29%	–96%
			16	31	168.750°	20%	–98%
				32	174.375°	10%	–100%
	5	9	17	33	180.000°	0%	–100%
				34	185.625°	–10%	–100%
			18	35	191.250°	–20%	–98%
				36	196.875°	–29%	–96%
		10	19	37	202.500°	–38%	–92%
				38	208.125°	–47%	–88%
			20	39	213.750°	–56%	–83%
				40	219.375°	–63%	–77%

Table 3. Microstepping Relative Current per Step (DIR = 1) (continued)

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	1/16 STEP	ELECTRICAL ANGLE (DEGREES)	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)
3	6	11	21	41	225.000°	–71%	–71%
				42	230.625°	–77%	–63%
			22	43	236.250°	–83%	–56%
				44	241.875°	–88%	–47%
		12	23	45	247.500°	–92%	–38%
				46	253.125°	–96%	–29%
			24	47	258.750°	–98%	–20%
				48	264.375°	–100%	–10%
	7	13	25	49	270.000°	–100%	0%
				50	275.625°	–100%	10%
			26	51	281.250°	–98%	20%
				52	286.875°	–96%	29%
		14	27	53	292.500°	–92%	38%
				54	298.125°	–88%	47%
			28	55	303.750°	–83%	56%
				56	309.375°	–77%	63%
4	8	15	29	57	315.000°	–71%	71%
				58	320.625°	–63%	77%
			30	59	326.250°	–56%	83%
				60	331.875°	–47%	88%
		16	31	61	337.500°	–38%	92%
				62	343.125°	–29%	96%
			32	63	348.750°	–20%	98%
				64	354.375°	–10%	100%
	1	1	1	1	360.000°	0%	100%

Non-circular 1/2–step operation is shown in Table 4. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor rpm.

Table 4. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2 STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (°)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

8.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. After the current hits the current chopping threshold, the bridge enters a decay mode for a fixed 20-µs period of time to decrease the current. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

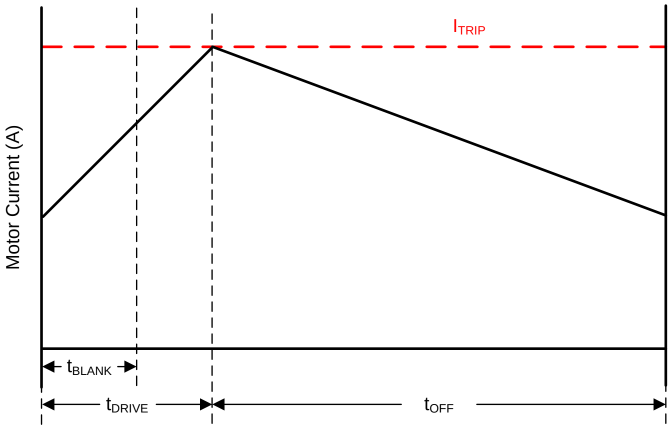

Figure 14. Current Chopping Waveform

The PWM chopping current is set by a comparator which looks at the voltage across current sense FETs in parallel with the low-side drivers. The current sense FETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the current through the RREF pin. An external resistor is placed from the RREF pin to GND in order to set the reference current. In addition, the TRQ pin can further scale the reference current.

The chopping current is calculated as shown in Equation 1.

$$I_{FS}\ (A) = \frac{A_{RREF}\ (k A \Omega)}{RREF\ (k\Omega)} \times TRQ\ (\%) = \frac{30\ (k A \Omega)}{RREF\ (k\Omega)} \times TRQ\ (\%) \tag{1}$$

Example: If a 30-kΩ resistor is connected to the RREF pin, the chopping current will be 1 A (TRQ at 100%).

The TRQ pin is the input to a DAC used to scale the output current. The current scalar value for different inputs is shown in Table 5.

Table 5. Torque DAC Settings

TRQ	CURRENT SCALAR (TRQ)
0	100%
Z	75%
1	50%

8.3.5 Controlling RREF With an MCU DAC

In some cases, the full-scale output current may need to be changed on the fly between many different values, depending on motor speed and loading. The RREF pin reference current can be adjusted in system by tying the RREF resistor to a DAC output instead of GND.

In this mode of operation, as the DAC voltage increases, the reference current will decrease, and therefore, the full-scale current will decrease as well. For proper operation, the output of the DAC should not rise above V_{RREF}.

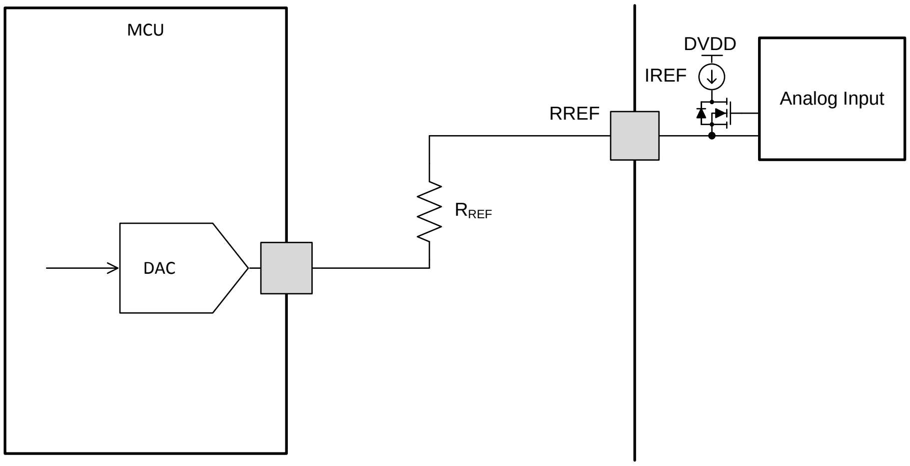

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Figure 15. Controlling RREF With a DAC

The chopping current as controlled by a DAC is calculated as in Equation 2.

$$I_{FS}\ (A) = \frac{A_{RREF}\ (k A\Omega) \times \left[V_{RREF}\ (V) - V_{DAC}\ (V)\right]}{V_{RREF}\ (V) \times RREF\ (k\Omega)} \times TRQ\ (\%) \tag{2}$$

Example: If a 20-kΩ resistor is connected from the RREF pin to the DAC, and the DAC is outputting 0.74 V, the chopping current will be 600 mA (TRQ at 100%).

RREF can also be adjusted using a PWM signal and low-pass filter.

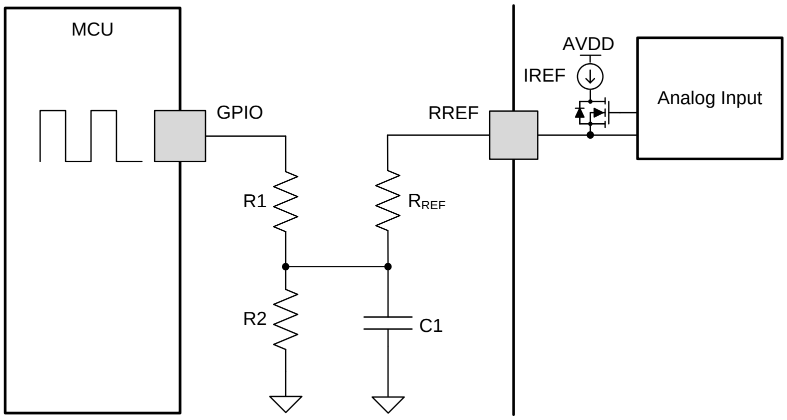

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Figure 16. Controlling RREF with a PWM Resource

8.3.6 Decay Modes

The DRV8884 decay mode is selected by setting the quad-level DECAY pin to the voltage range in Table 6.

Table 6. Decay Mode Settings

DECAY	INCREASING STEPS	DECREASING STEPS
100 mV Can be tied to ground	Slow decay	Mixed decay: 30% fast
300 mV, 15 kΩ to GND	Mixed decay: 30% fast	Mixed decay: 30% fast
1.0 V, 45 kΩ to GND	Mixed decay: 60% fast	Mixed decay: 60% fast
2.9 V Can be tied to DVDD	Slow decay	Slow decay

Increasing and decreasing current are defined in Figure 17. For the slow/mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full-step mode, the decreasing steps decay mode is always used.

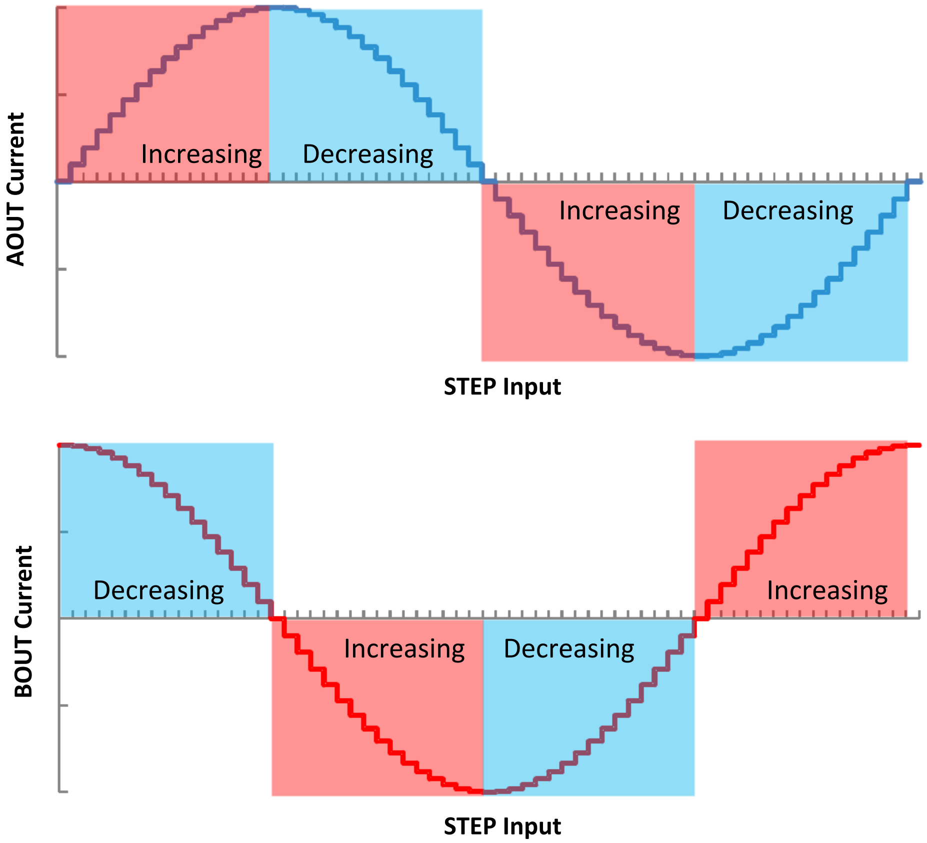

Figure 17. Definition of Increasing and Decreasing Steps

8.3.6.1 Mode 1: Slow Decay for Increasing and Decreasing Current

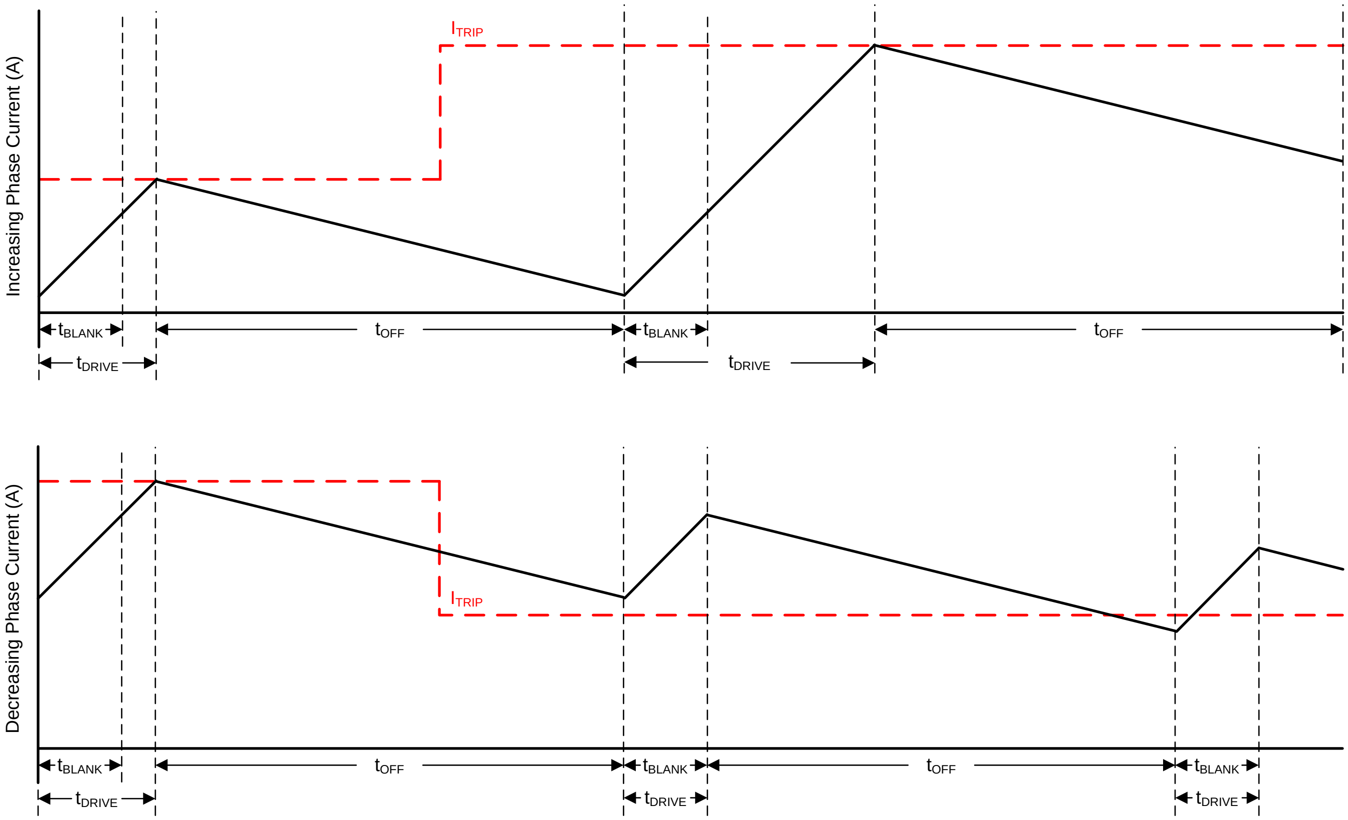

Figure 18. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However, on decreasing current steps, slow decay takes a long time to settle to the new I_{TRIP} level because the current decreases very slowly.

8.3.6.2 Mode 2: Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

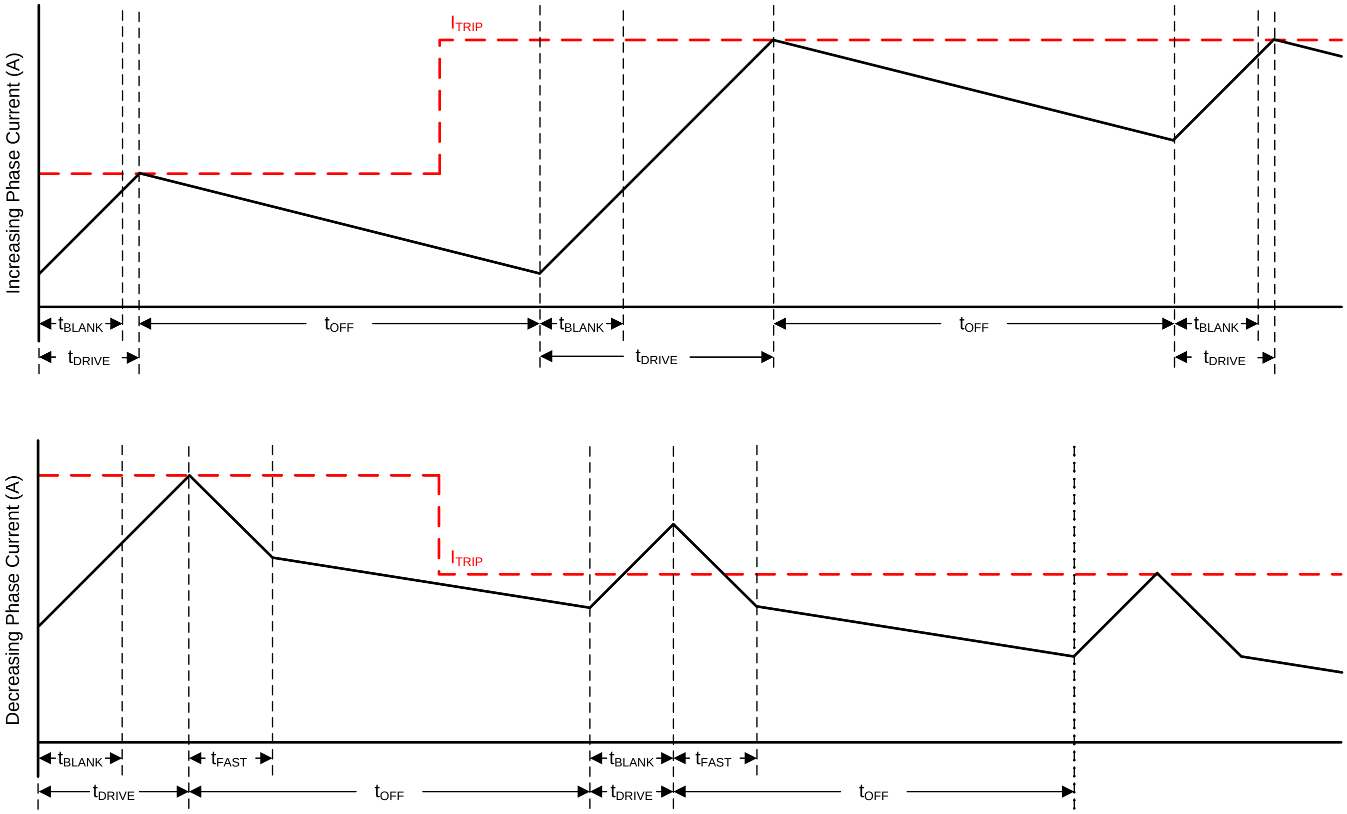

Figure 19. Slow/Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, since for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

8.3.6.3 Mode 3: Mixed Decay for Increasing and Decreasing Current

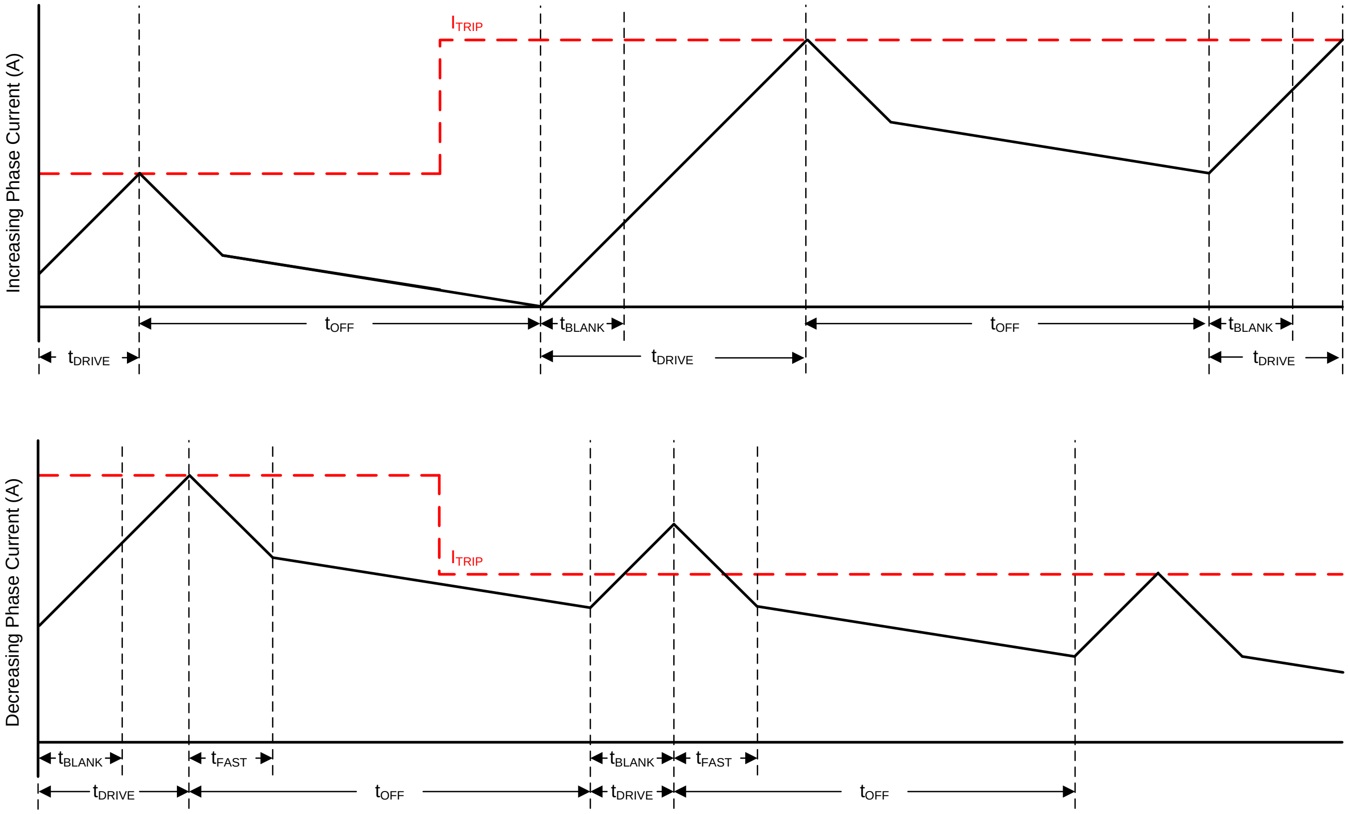

Figure 20. Mixed/Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing/decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

8.3.7 Blanking Time

After the current is enabled in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. Note that the blanking time also sets the minimum drive time of the PWM. Table 7 shows the blanking time based on the sine table index and the torque DAC setting. Note that the torque DAC index is not the same as one step as given in Table 3.

Table 7. Adaptive Blanking Time over Torque DAC and Microsteps

🟧 t_{blank} = 1.5 µs	🟦 t_{blank} = 1.0 µs

SINE INDEX	TORQUE DAC (TRQ)		
	100%	75%	50%
16	🟧 100%	🟧 75%	🟦 50%
15	🟧 98%	🟧 73.5	🟦 49%
14	🟧 96%	🟧 72%	🟦 48%
13	🟧 92%	🟧 69%	🟦 46%
12	🟧 88%	🟧 66%	🟦 44%
11	🟧 83%	🟧 62.3%	🟦 41.5%
10	🟧 77%	🟦 57.8%	🟦 38.5%
9	🟧 71%	🟦 53.3%	🟦 35.5%
8	🟧 63%	🟦 47.3%	🟦 31.5%
7	🟦 56%	🟦 42%	🟦 28%
6	🟦 47%	🟦 35.3	🟦 23.5%
5	🟦 38%	🟦 28.5	🟦 19%
4	🟦 29%	🟦 21.8%	🟦 14.5%
3	🟦 20%	🟦 15%	🟦 10%
2	🟦 10%	🟦 7.5%	🟦 5%
1	🟦 0%	🟦 0%	🟦 0%

8.3.8 Charge Pump

A charge pump is integrated in order to supply a high-side NMOS gate drive voltage. The charge pump requires a capacitor between the VM and VCP pins. Additionally, a low-ESR ceramic capacitor is required between pins CPH and CPL.

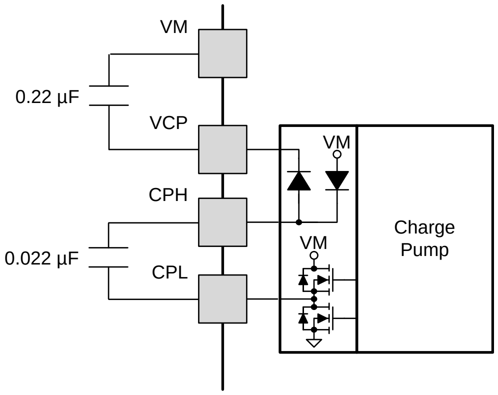

Figure 21. Charge Pump Diagram

8.3.9 LDO Voltage Regulator

An LDO regulator is integrated into the DRV8884. DVDD can be used to provide a reference voltage. For proper operation, bypass DVDD to GND using a ceramic capacitor.

The DVDD output is nominally 3.3 V. When the DVDD LDO current load exceeds 1 mA, the output voltage drops significantly.

The AVDD pin also requires a bypass capacitor to GND. This LDO is for DRV8884 internal use only.

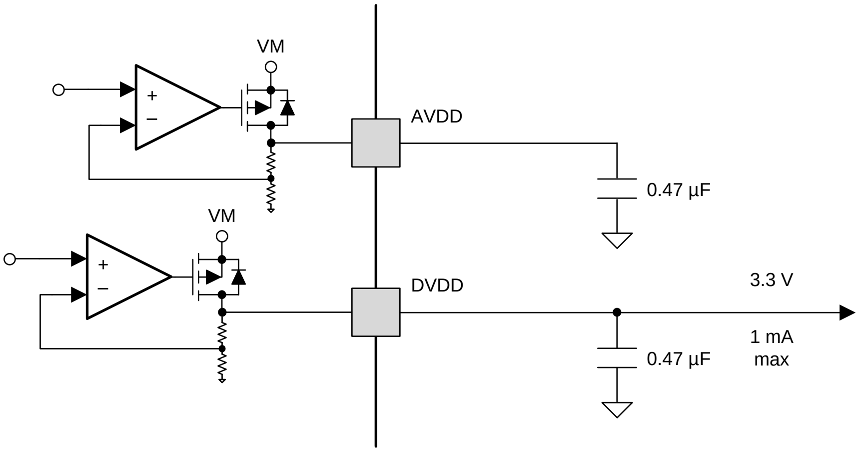

Figure 22. LDO Diagram

If a digital input needs to be tied permanently high (that is, Mx, DECAY, or TRQ), it is preferable to tie the input to DVDD instead of an external regulator. This saves power when VM is not applied or in sleep mode; DVDD is disabled and current will not be flowing through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 100 kΩ, and tri-level inputs have a typical pulldown of 60 kΩ.

8.3.10 Logic and Multi-Level Pin Diagrams

Figure 23 gives the input structure for logic-level pins STEP, DIR, ENABLE, nSLEEP, and M1.

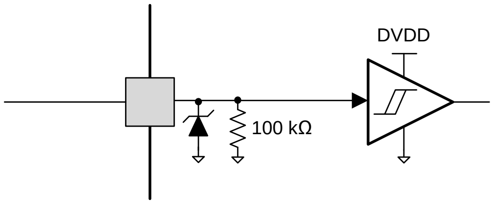

Figure 23. Logic-level Input Pin Diagram

Tri-level logic pins M0 and TRQ have the following structure shown in Figure 24.

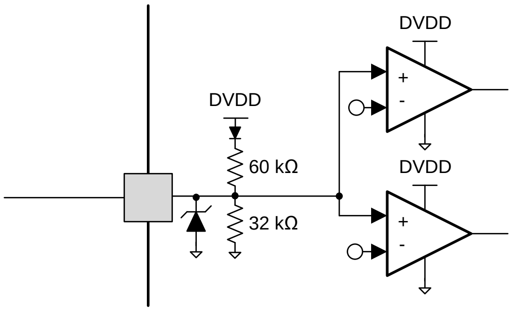

Figure 24. Tri-level Input Pin Diagram

Quad-level logic pin DECAY has the following structure shown in Figure 25.

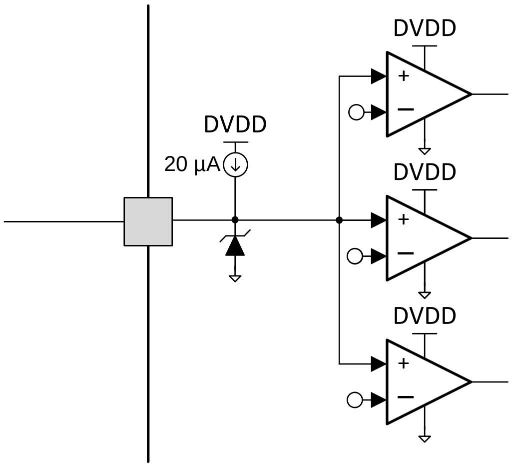

Figure 25. Quad-level Input Pin Diagram

8.3.11 Protection Circuits

The DRV8884 is fully protected against undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

8.3.11.1 VM UVLO

If at any time the voltage on the VM pin falls below the VM UVLO threshold voltage (V_{UVLO}), all FETs in the H-bridge will be disabled, the charge pump will be disabled, the logic will be reset, the DVDD regulator is disabled, and the nFAULT pin will be driven low. Operation resumes when VM rises above the UVLO threshold. The nFAULT pin is released after operation has resumed. Decreasing VM below this undervoltage threshold will reset the indexer position.

8.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the charge pump UVLO threshold voltage, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Operation resumes when VCP rises above the CPUV threshold. The nFAULT pin is released after operation has resumed.

8.3.11.3 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, all FETs in the H-bridge will be disabled and nFAULT will be driven low.

The driver is re-enabled after the OCP retry period (t_{RETRY}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted.

8.3.11.4 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

Table 8. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	DVDD	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO} (max 7.8 V)	nFAULT	Disabled	Disabled	Disabled	Disabled	VM > V_{UVLO} (max 8.0 V)

Table 8. Fault Condition Summary (continued)

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	DVDD	RECOVERY
VCP undervoltage (CPUV)	VCP < V_{CPUV} (typ VM + 2.0 V)	nFAULT	Disabled	Operating	Operating	Operating	VCP > V_{CPUV} (typ VM + 2.7 V)
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$ (min 1.7 A)	nFAULT	Disabled	Operating	Operating	Operating	t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$ (min 150°C)	nFAULT	Disabled	Operating	Operating	Operating	$T_J < T_{TSD} – T_{HYS}$ (T_{HYS} typ 20°C)

8.4 Device Functional Modes

The DRV8884 is active unless the nSLEEP pin is brought logic low. In sleep mode, the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the V3P3 regulator is disabled. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8884 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up.

TI recommends to keep the STEP pin logic low when coming out of nSLEEP or when applying power.

If the ENABLE pin is brought logic low, the H-bridge outputs are disabled, but the internal logic will still be active. A rising edge on STEP will advance the indexer, but the outputs will not change state until ENABLE is asserted.

Table 9. Functional Modes Summary

CONDITION		H-BRIDGE	CHARGE PUMP	INDEXER	V3P3
Operating	8 V < VM < 40 V nSLEEP pin = 1 ENABLE pin = 1	Operating	Operating	Operating	Operating
Disabled	8 V < VM < 40 V nSLEEP pin = 1 ENABLE pin = 0	Disabled	Operating	Operating	Operating
Sleep mode	8 V < VM < 40 nSLEEP pin = 0	Disabled	Disabled	Disabled	Disabled
Fault encountered	VM undervoltage (UVLO)	Disabled	Disabled	Disabled	Disabled
	VCP undervoltage (CPUV)	Disabled	Operating	Operating	Operating
	Overcurrent (OCP)	Disabled	Operating	Operating	Operating
	Thermal shutdown (TSD)	Disabled	Operating	Operating	Operating

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8884 is used in bipolar stepper control.

9.2 Typical Application

The following design procedure can be used to configure the DRV8884.

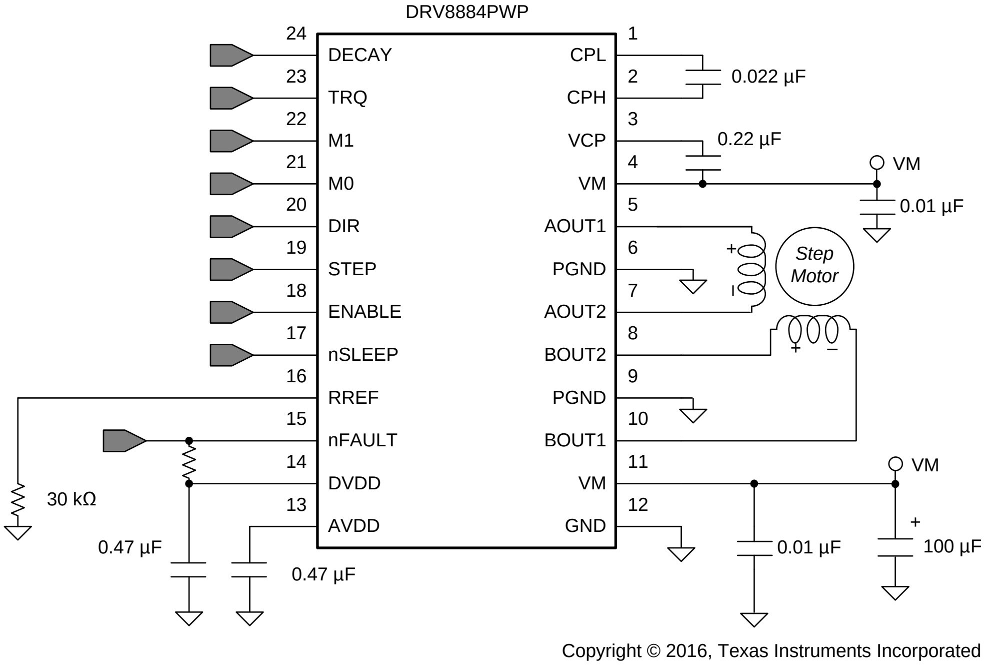

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Figure 26. Typical Application Schematic

9.2.1 Design Requirements

Table 10 gives design input parameters for system design.

Table 10. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	2.6 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	1.0 A

9.2.2 Detailed Design Procedure

9.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8884 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\ (\text{steps / s}) = \frac{\text{v (rpm)} \times 360\ (° / \text{rot})}{\theta_{step}\ (° / \text{step}) \times n_m\ (\text{steps / microstep}) \times 60\ (\text{s / min})} \tag{3}$$

θ_{step} can be found in the stepper motor data sheet, or written on the motor itself.

For the DRV8884, the microstepping level is set by the Mx pins and can be any of the settings in Table 11. Higher microstepping will mean a smother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

Table 11. Microstepping Indexer Settings

M1	M0	STEP MODE
0	0	Full step (2-phase excitation) with 71% current
0	1	1/16 step
1	0	1/2 step
1	1	1/4 step
0	Z	1/8 step
1	Z	Non-circular 1/2 step

Example: Target 120 rpm at 1/8 microstep mode. The motor is 1.8°/step

$$f_{step}\ (\text{steps / s}) = \frac{120\ \text{rpm} \times 360° / \text{rot}}{1.8° / \text{step} \times 1/8\ \text{steps / microstep} \times 60\ \text{s / min}} = 3.2\ \text{kHz} \tag{4}$$

9.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity will depend on the RREF resistor and the TRQ setting. During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}\ (\text{A}) = \frac{A_{RREF}\ (\text{k}A\Omega)}{\text{RREF}\ (\text{k}\Omega)} = \frac{30\ (\text{k}A\Omega) \times \text{TRQ}\%}{\text{RREF}\ (\text{k}\Omega)} \tag{5}$$

Note that I_{FS} must also follow Equation 6 in order to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (\text{A}) < \frac{\text{VM (V)}}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{6}$$

9.2.2.3 Decay Modes

The DRV8884 supports three different decay modes: slow decay, slow/mixed and all mixed decay. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8884 will place the winding in one of the three decay modes for t_{OFF}. After t_{OFF}, a new drive phase starts.

The blanking time t_{BLANK} defines the minimum drive time for the PWM current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

9.2.3 Application Curves

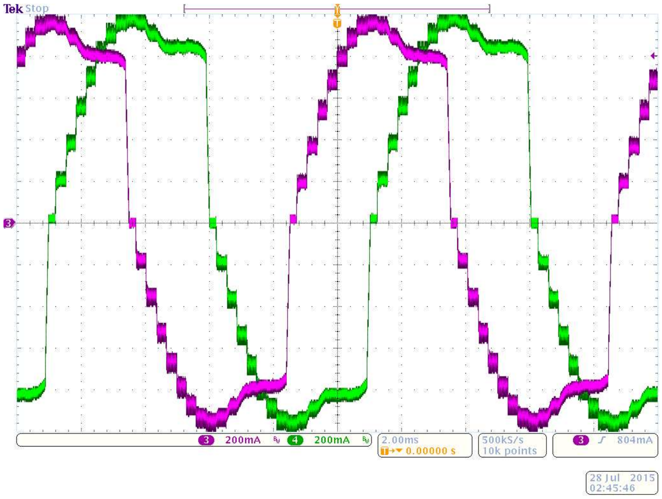

Figure 27. Microstepping Using Slow Decay on Increasing and Decreasing Steps; Current Loses Regulation on Falling Steps

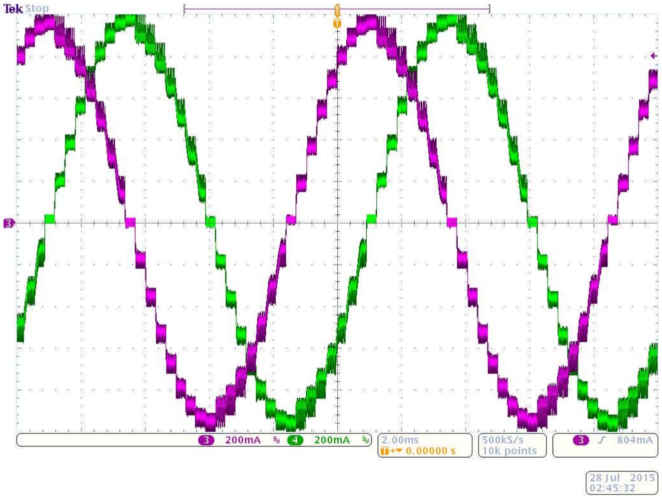

Figure 28. Microstepping Using Slow Decay on Increasing Steps and Mixed 30% Fast Decay on Decreasing Steps

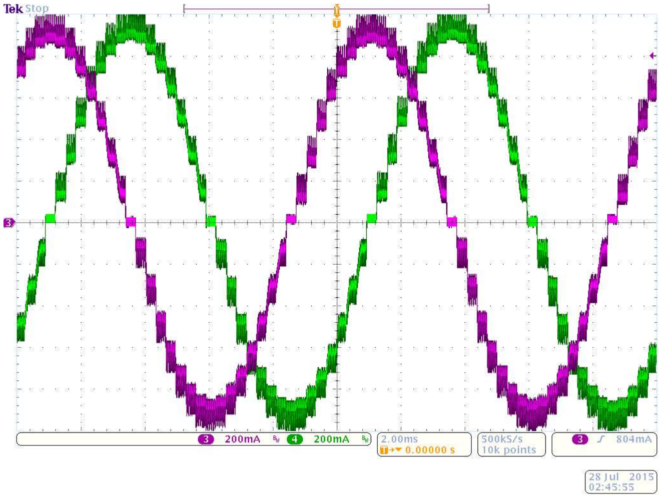

Figure 29. Microstepping Using Mixed 30% Fast Decay on Increasing and Decreasing Steps

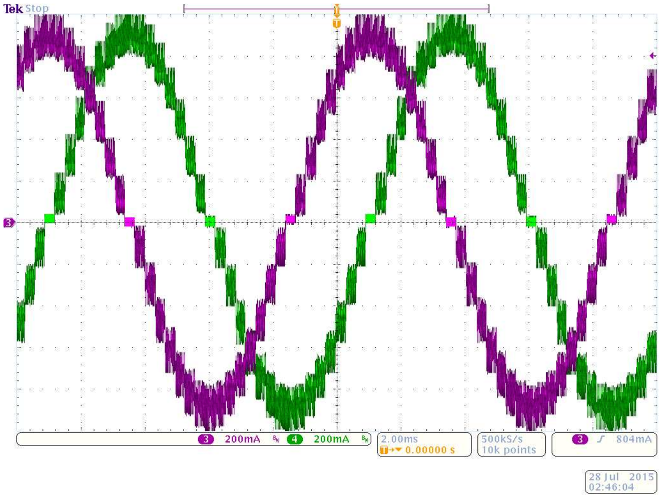

Figure 30. Microstepping Using Mixed 60% Fast Decay on Increasing and Decreasing Steps

10 Power Supply Recommendations

The DRV8884 is designed to operate from an input voltage supply (VM) range between 8 and 35 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8884 as possible. In addition, a bulk capacitor must be included on VM.

10.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply’s capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

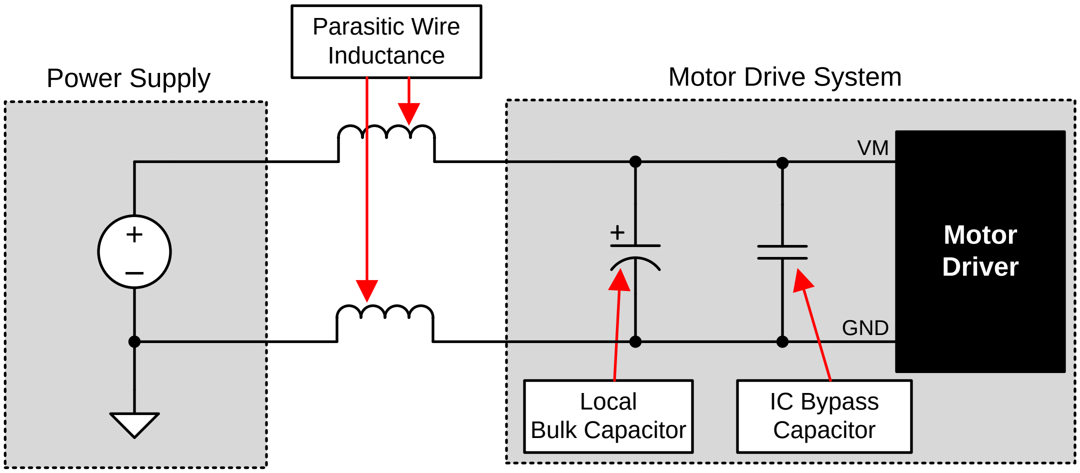

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Figure 31. Example Setup of Motor Drive System With External Power Supply

11 Layout

11.1 Layout Guidelines

The VM terminal should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.022 µF rated for VM. Place this component as close as possible to the pins.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.22 µF rated for 16 V. Place this component as close as possible to the pins.

Bypass AVDD and DVDD to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close as possible to the pin.

11.2 Layout Example

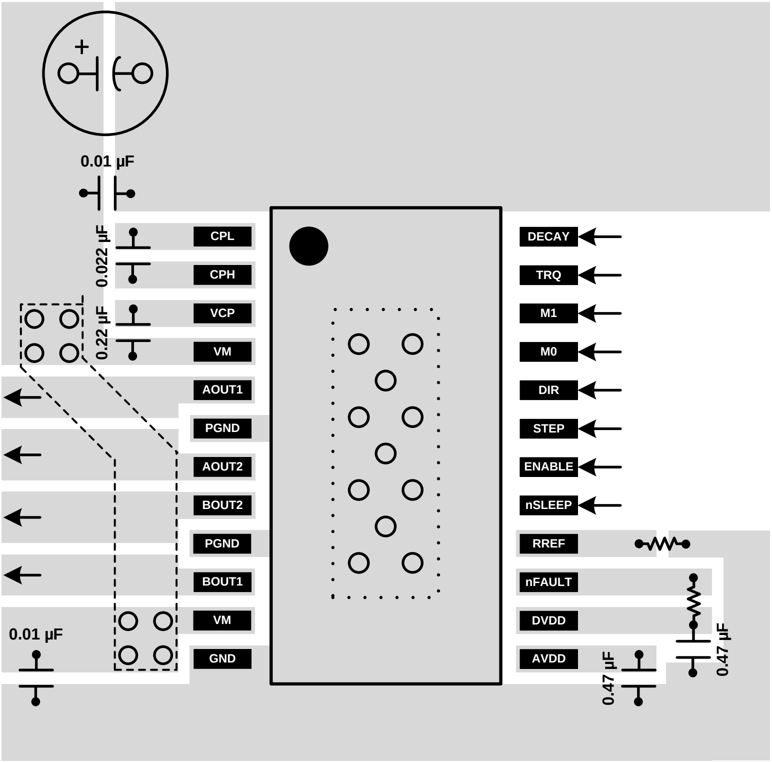

Figure 32. Layout Recommendation

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

- テキサス・インスツルメンツ、*『電流再循環および減衰モード』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『モータ・ドライバの消費電力計算』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『デジタル/アナログ・コンバータ(DAC)を使用するフルスケール電流調整』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『DRV8884評価モジュール(EVM)ユーザー・ガイド』*
- テキサス・インスツルメンツ、*『放熱特性に優れたPowerPAD™パッケージ』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『PowerPAD™の簡単な使用法』*アプリケーション・レポート
- テキサス・インスツルメンツ、*『モータ・ドライバの電流定格について』*アプリケーション・レポート

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

PowerPAD, E2E are trademarks of Texas Instruments.
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12.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8884PWP	LIFEBUY	HTSSOP	PWP	24	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8884	
DRV8884PWPR	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8884	Samples
DRV8884RHRR	ACTIVE	WQFN	RHR	28	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8884	Samples
DRV8884RHRT	LIFEBUY	WQFN	RHR	28	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8884	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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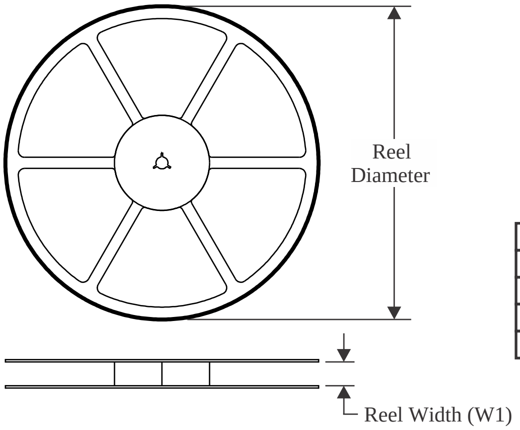
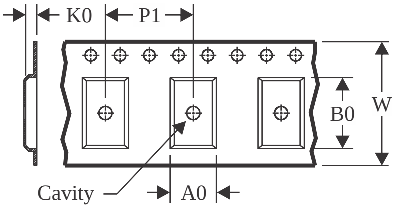
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

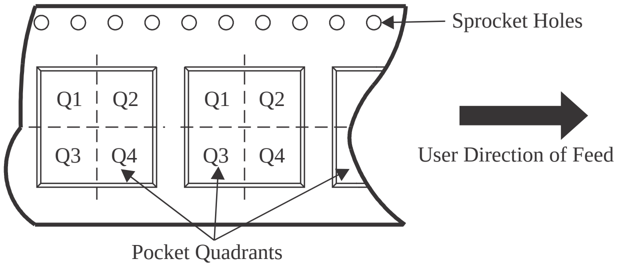


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

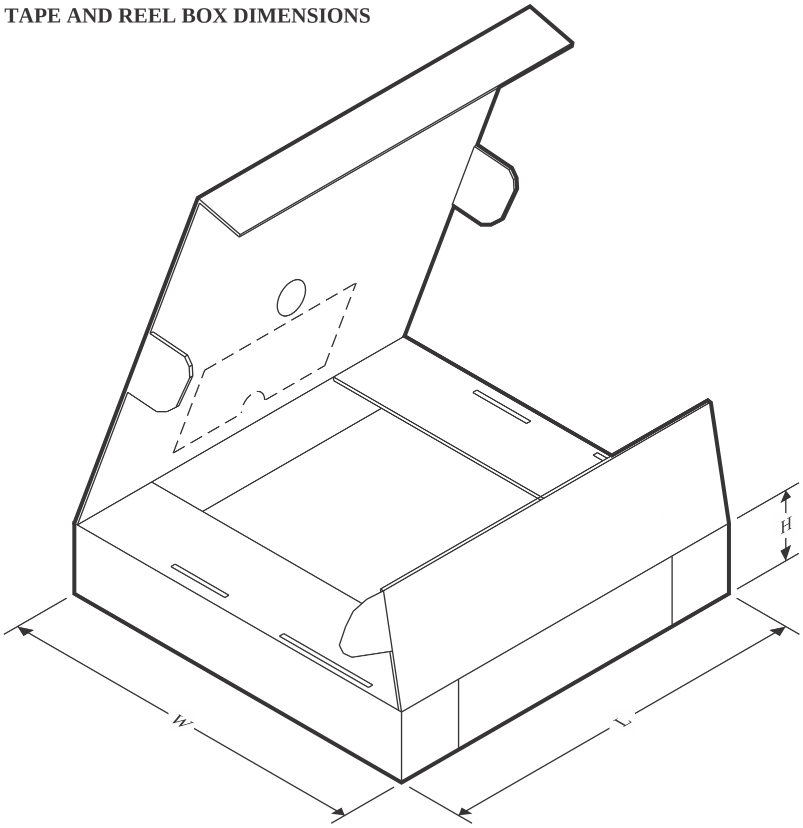
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8884PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8884RHRR	WQFN	RHR	28	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
DRV8884RHRT	WQFN	RHR	28	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

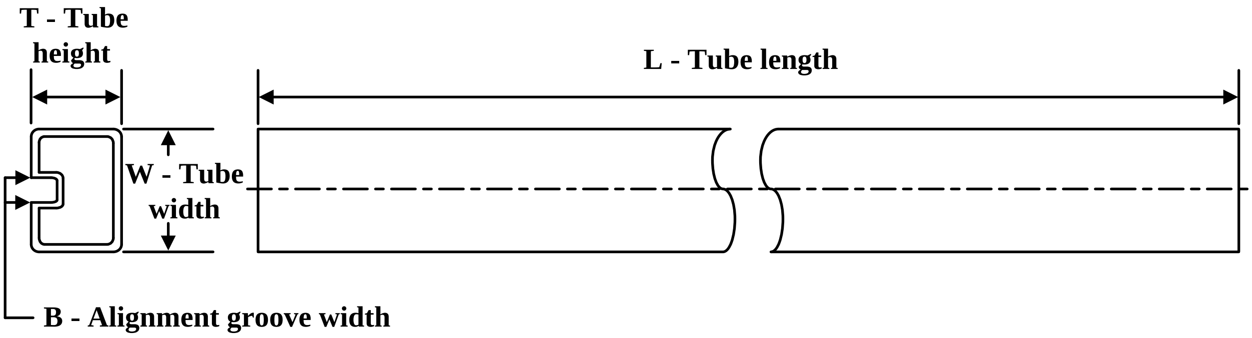
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8884PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV8884RHRR	WQFN	RHR	28	3000	367.0	367.0	35.0
DRV8884RHRT	WQFN	RHR	28	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8884PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

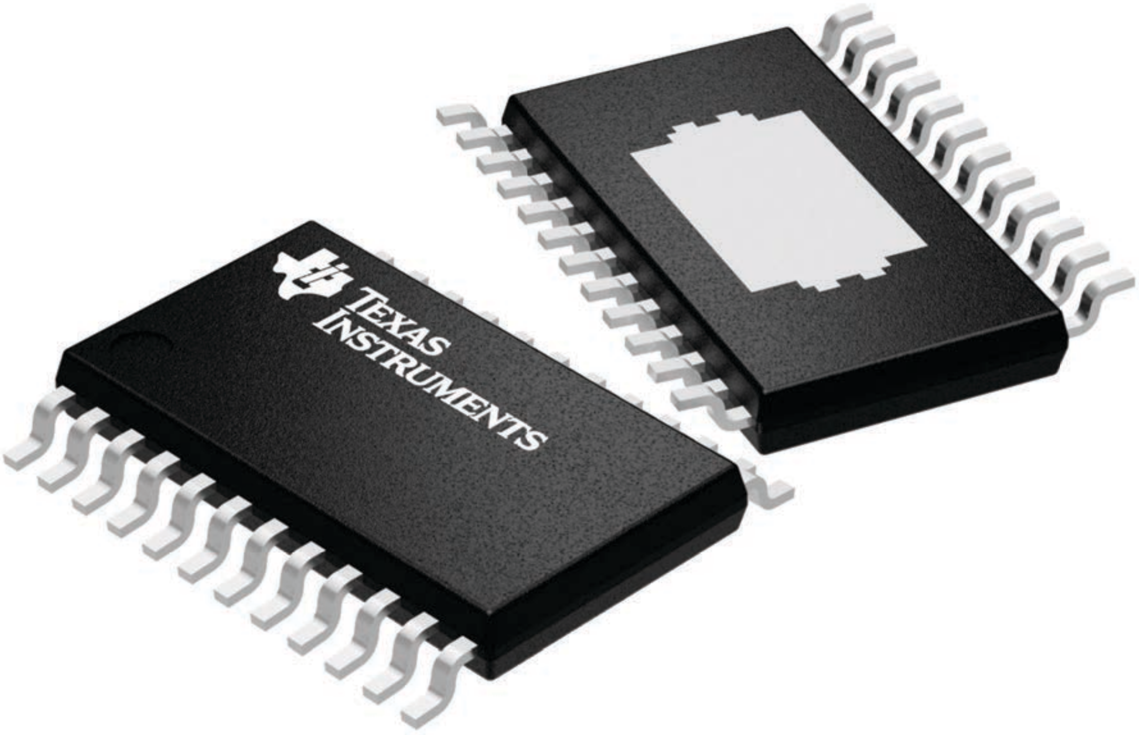
PWP 24

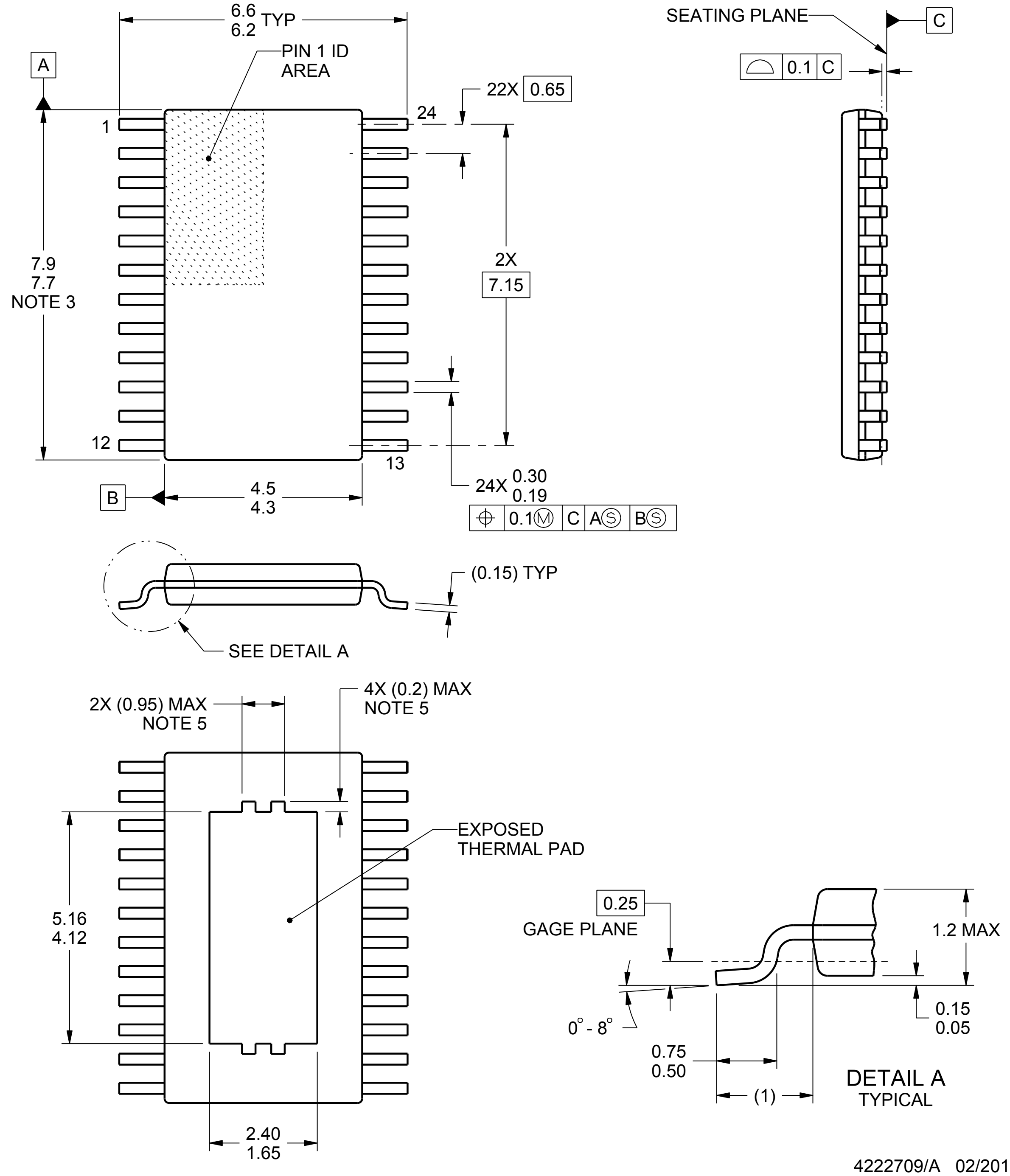
PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



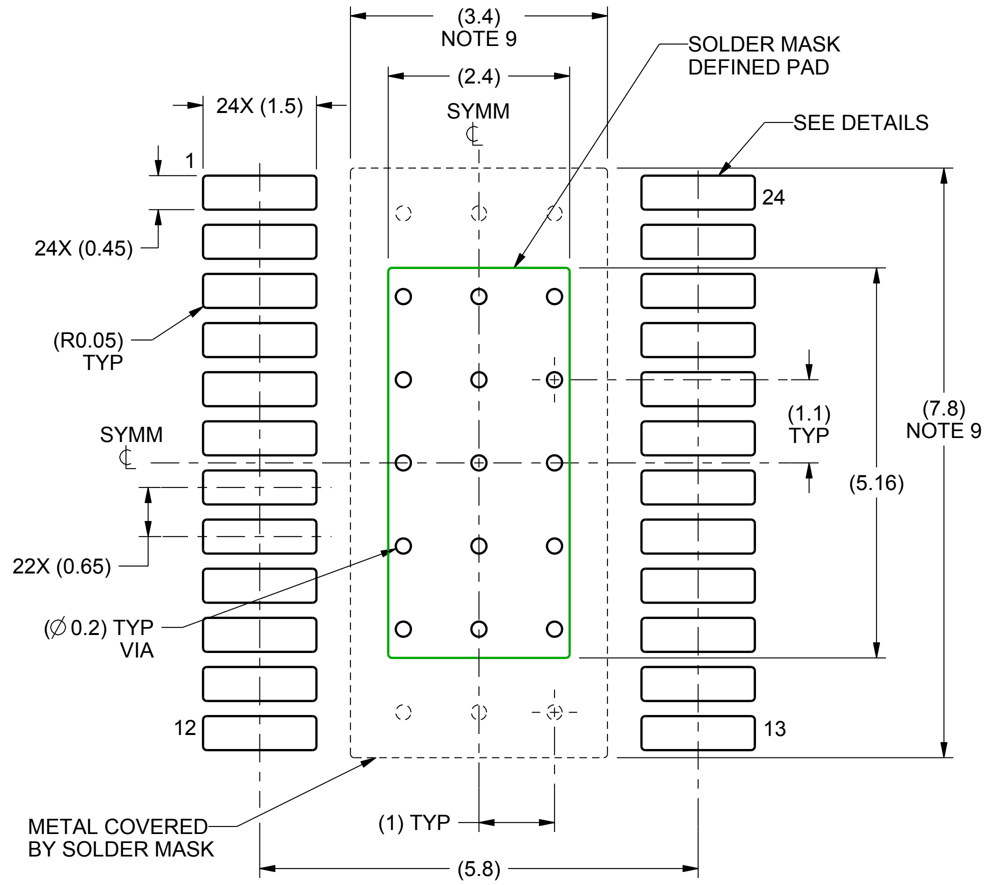


4222709/A 02/2016

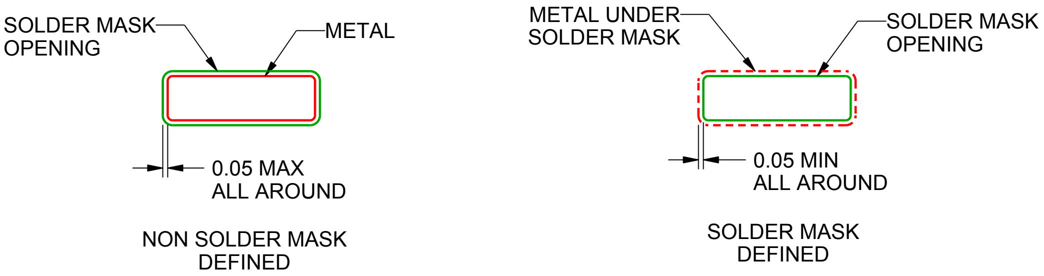
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

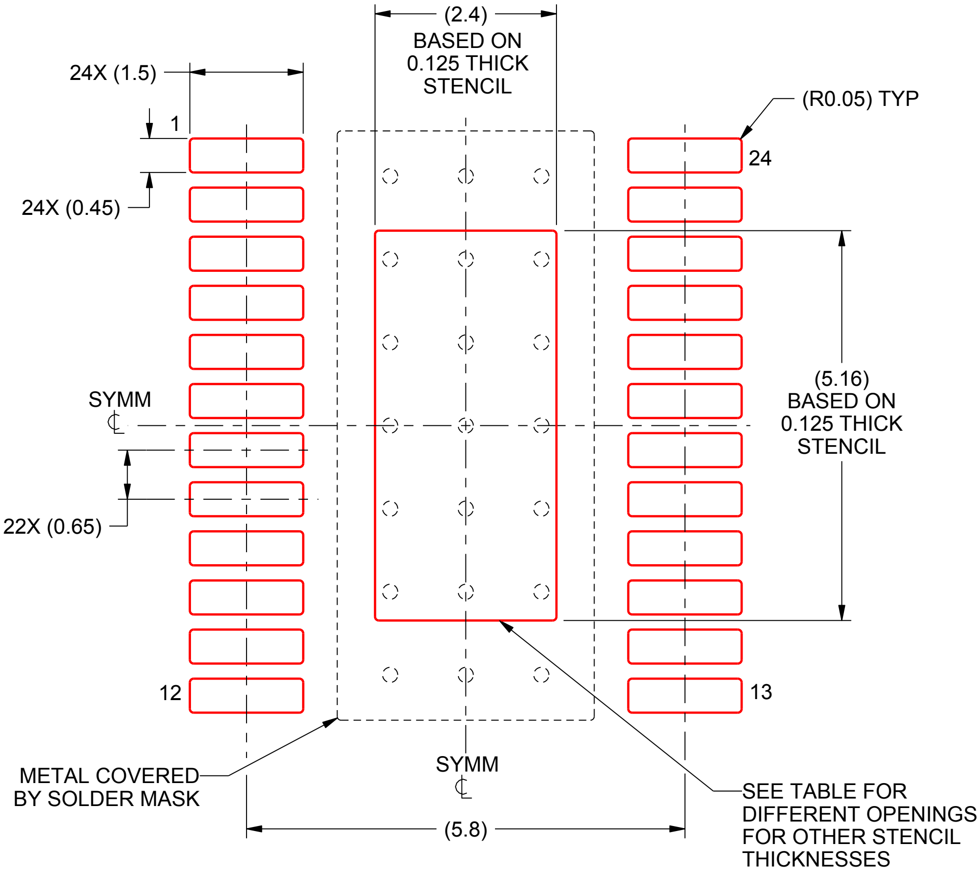


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

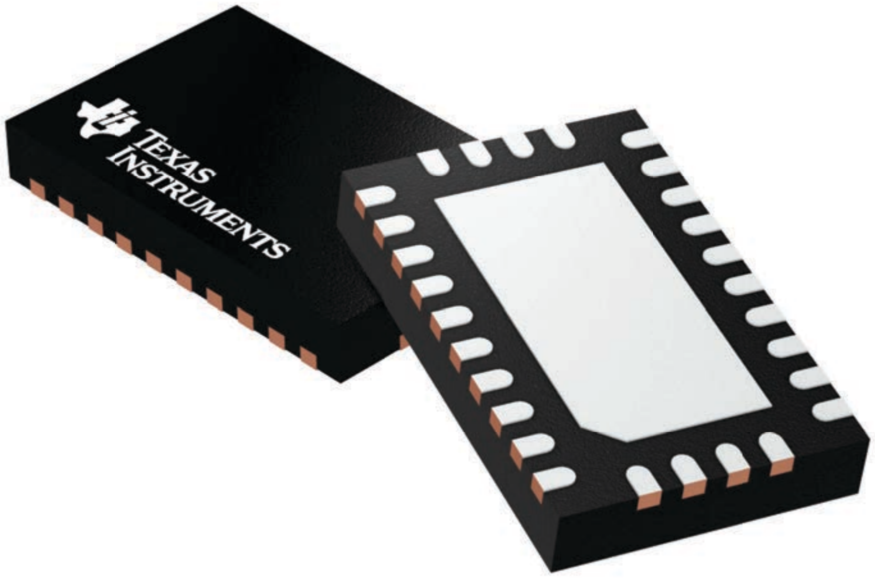
GENERIC PACKAGE VIEW

RHR 28

WQFN - 0.8 mm max height

3.5 x 5.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

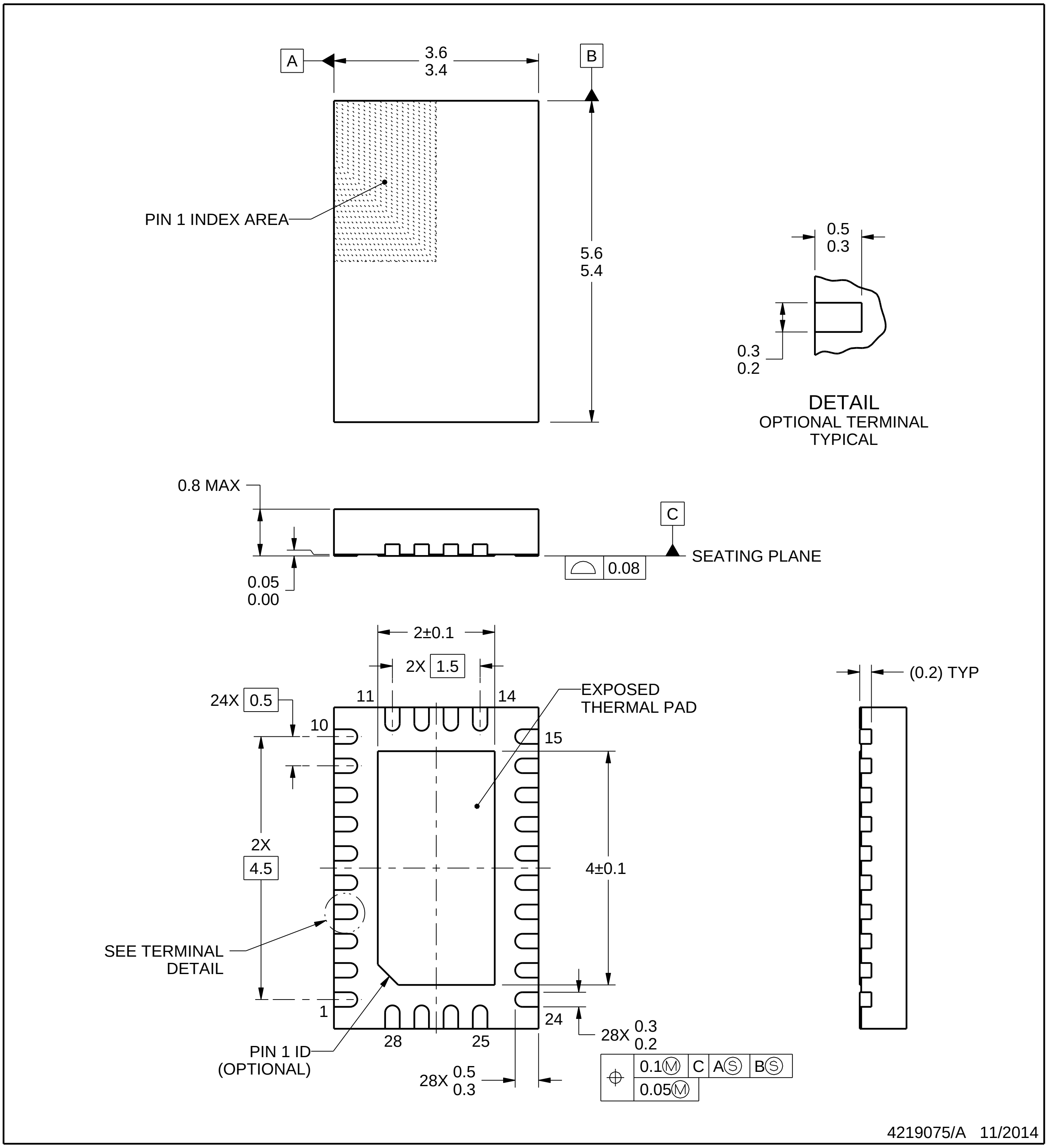
4210249/B

PACKAGE OUTLINE

RHR0028A

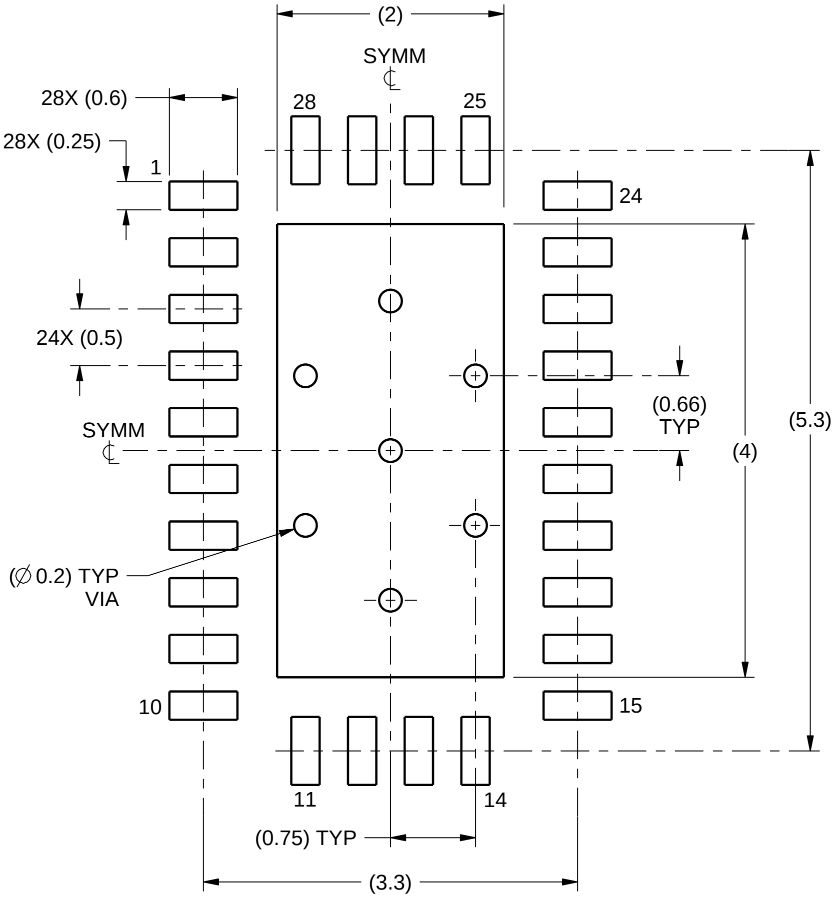
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

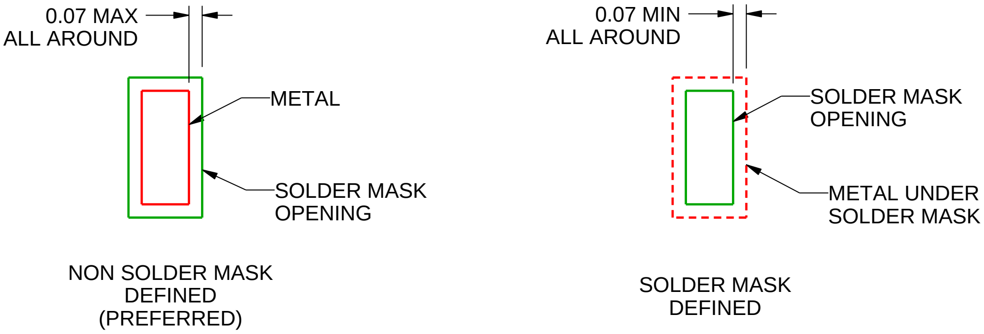


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

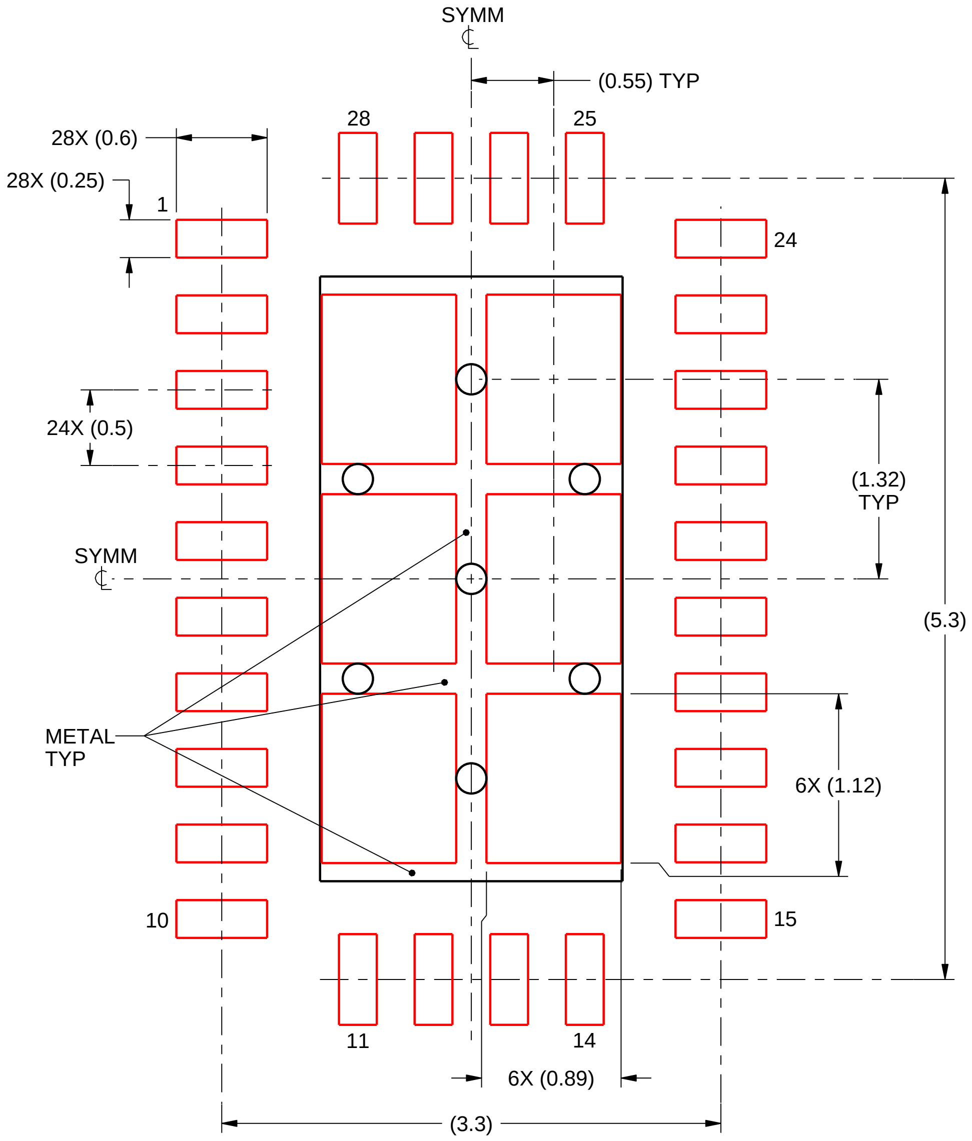


SOLDER MASK DETAILS

4219075/A 11/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265