

DS250DF210 25Gbps、マルチレート2チャンネル・リタイマ

1 特長

- 信号コンディショニングを内蔵した2チャンネル、マルチレートのリタイマ
- すべてのチャンネルは独立に 20.6~25.8Gbps でロック (10.3125Gbps、12.5Gbps などのサブレートを含む)
- 非常に短いレイテンシ : 25.78125Gbps のデータ速度で標準値 500ps 未満
- 単一電源で、低ジッタの基準クロックを必要とせず、電源デカップリングが最小限であるため、基板の配線の複雑性と BOM コストを低減
- アダプティブ連続時間リニア・イコライザ(CTLE)
- アダプティブ・デジション・フィードバック・イコライザ(DFE)
- 2×2 のクロス・ポイントを内蔵
- 3 タップ FIR フィルタ付きの低ジッタ・トランスミッタ
- 結合イコライゼーションにより、12.9GHz で 35dB を超えるチャンネル損失をサポート
- 伝送振幅を変更可能 : 205mVppd~1225mVppd (標準値)
- オンチップのアイ・オープニング・モニタ (EOM)、PRBS パターン・チェッカおよびジェネレータ
- フロースルー配線が簡単な小型の 6mm × 6mm BGA パッケージ

2 アプリケーション

- フロント・ポート光学系のジッタ・クリーニング
- アクティブ・ケーブル・アセンブリ
- バックプレーンおよびミッドプレーンの範囲拡張
- IEEE802.3bj 100GbE、Infiniband EDR、および OIF-CEI-25G-LR/MR/SR/VSR 電氣的インターフェイス
- SFP28、QSFP28、CFP2/CFP4、CDFP

3 概要

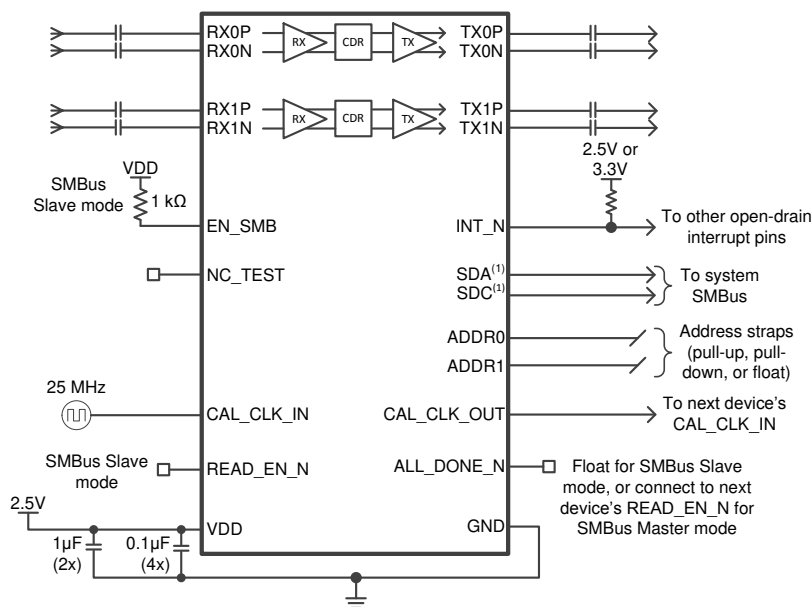
DS250DF210 デバイスは2チャンネル、マルチレートのリタイマで、信号コンディショニング機能が内蔵されています。長距離で損失が大きく、クロストークを受ける高速なシリアル・リンクの到達距離と堅牢性を拡張し、ビット・エラー・レート(BER)を 10^{-15} 以下に抑えるために使用されます。

製品情報⁽¹⁾

| 型番 | パッケージ | 本体サイズ(公称) |
|------------|-----------|---------------|
| DS250DF210 | ABM (101) | 6.00mm×6.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



(1) SMBus signals need to be pulled up elsewhere in the system.



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4 改訂履歴

Revision A (February 2019) から Revision B に変更

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| | | |
|---|-----------------|----------|
| • | 最初の公開リリース | 1 |
|---|-----------------|----------|

5 概要(続き)

DS250DF210の各チャンネルは、20.6Gbps～25.8Gbpsの連続した範囲のシリアル・データ・レート、またはサポートされている任意のサブレート($\div 2$ および $\div 4$) (10.3125Gbpsや12.5Gbpsなどの主要データ・レートを含む)へ独立にロックされるため、DS250DF210は個別レーンの前方誤り訂正(FEC)パススルーをサポートできます。

DS250DF210は単一電源で、必要な外部コンポーネントも最小限です。これらの特長により、PCB配線の複雑性とBOMコストが低減されます。

DS250DF210の高度なイコライゼーション機能には、低ジッタの3タップ送信有限インパルス応答(FIR)フィルタ、アダプティブ連続時間リニア・イコライザ(CTLE)、アダプティブ・デジジョン・フィードバック・イコライザ(DFE)が含まれています。これにより、複数のコネクタやクロストークが存在する、損失の多い相互接続およびバックプレーンにおいて、到達距離を拡張できます。内蔵のCDR機能は、フロントポート光学モジュール・アプリケーションで、ジッタ・バジェットをリセットし、高速シリアル・データをリタイムするために最適です。DS250DF210には2x2のクロス・ポイントが実装されており、ホストでレーン交差、ファンアウト、多重化オプションを使用できます。







DS250DF210はSMBus経由、または外付けのEEPROMにより構成可能です。最大16個のデバイスが、共通のチャンネル・フォーマットを使用して単一のEEPROMを共有できます。非破壊的なオンチップ・アイ・モニタと PRBS ジェネレータ/チェッカにより、インシステム診断が可能です。

6 Pin Configuration and Functions

ABM Package
101-Pin fcBGA, 0.5mm BGA pitch
Top View

| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|-------------|----------|-----|------|------|-----|-----|-----|-----|----------|------------|---|
| L | TX0P | TX0N | GND | TX1P | TX1N | GND | NC | NC | GND | NC | NC | L |
| K | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | K |
| J | GND | | VDD | | | GND | | | VDD | | GND | J |
| H | SDC | NC_TEST4 | VDD | VDD | VDD | GND | VDD | VDD | VDD | NC_TEST5 | INT_N | H |
| G | SDA | GND | GND | | GND | | GND | | GND | GND | EN_SMB | G |
| F | CAL_CLK_OUT | | GND | GND | GND | GND | GND | GND | GND | | CAL_CLK_IN | F |
| E | READ_EN_N | NC_TEST2 | GND | | GND | | GND | | GND | NC_TEST3 | ALL_DONE_N | E |
| D | ADDR0 | NC_TEST0 | VDD | VDD | VDD | GND | VDD | VDD | VDD | NC_TEST1 | ADDR1 | D |
| C | GND | | VDD | | | GND | | | VDD | | GND | C |
| B | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | B |
| A | RX0P | RX0N | GND | RX1P | RX1N | GND | NC | NC | GND | NC | NC | A |
| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |

Legend

| | |
|---|-------------------------------------|
|  | Control/ status |
|  | High-Speed |
|  | TI test or No Connect (CN on board) |
|  | Ground |
|  | Power |
|  | De-populated BGA |

Pin Functions

| PIN | | TYPE | INTERNAL PULLUP/ PULLDOWN | DESCRIPTION |
|-------------------------------------|-----|--------|---------------------------|---|
| NAME | NO. | | | |
| HIGH-SPEED DIFFERENTIAL I/Os | | | | |
| RX0N | A10 | Input | None | Inverting and noninverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs must be AC-coupled. ⁽¹⁾ |
| RX0P | A11 | Input | None | |
| RX1N | A7 | Input | None | |
| RX1P | A8 | Input | None | |
| TX0N | L10 | Output | None | Inverting and noninverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs must be AC-coupled. ⁽¹⁾ |
| TX0P | L11 | Output | None | |
| TX1N | L7 | Output | None | Inverting and noninverting 50-Ω driver outputs. Compatible with AC-coupled differential inputs. These outputs must be AC-coupled. ⁽¹⁾ |
| TX1P | L8 | Output | None | |

(1) High-speed pins do not have short-circuit protection. High-speed pins must be AC-coupled.

Pin Functions (continued)

| PIN | | TYPE | INTERNAL PULLUP/ PULLDOWN | DESCRIPTION |
|---|--------------------------------|--------------------------------|------------------------------|--|
| NAME | NO. | | | |
| CALIBRATION CLOCK PINS | | | | |
| CAL_CLK_IN | F1 | Input, 2.5-V CMOS | Weak pulldown | 25-MHz (± 100 PPM) 2.5-V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. Used to calibrate VCO frequency range. |
| CAL_CLK_OUT | F11 | Output, 2.5-V CMOS | None | 2.5-V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion. |
| SYSTEM MANAGEMENT BUS (SMBus) PINS | | | | |
| ADDR0 | D11 | Input, 4-level | None | 4-level strap pins used to set the SMBus address of the device. The pin state is read on power up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 k Ω to GND R: 20 k Ω to GND F: Float 1: 1 k Ω to VDD Refer to Device SMBus Address for more details. |
| ADDR1 | D1 | Input, 4-level | None | |
| EN_SMB | G1 | Input, 4-level | None | Four-level, 2.5-V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 k Ω to GND - RESERVED R: 20 k Ω to GND - RESERVED, TI test mode F: Float - SMBus Master Mode 1: 1 k Ω to VDD - SMBus Slave Mode |
| SDA | G11 | I/O, 3.3-V LVC MOS, Open-Drain | None | SMBus data input / open-drain output. External 2-k Ω to 5-k Ω pullup resistor is required as per SMBus interface standard. This pin is 3.3-V LVC MOS tolerant. |
| SDC | H11 | I/O, 3.3-V LVC MOS, Open-Drain | None | SMBus clock input / open-drain clock output. External 2-k Ω to 5-k Ω pullup resistor is required as per SMBus interface standard. This pin is 3.3-V LVC MOS tolerant. |
| SMBus MASTER MODE PINS | | | | |
| ALL_DONE_N | E1 | Output, LVC MOS | None | Indicates the completion of a valid EEPROM register load operation when in SMBus Master Mode (EN_SMB=Float): High = External EEPROM load failed or incomplete Low = External EEPROM load successful and complete When in SMBus slave mode (EN_SMB=1), this output reflects the status of the READ_EN_N input. |
| READ_EN_N | E11 | Input, LVC MOS | Weak pullup | SMBus Master Mode (EN_SMB=Float): When asserted low, initiates the SMBus master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. SMBus Slave Mode (EN_SMB=1): When asserted low, this causes the device to be held in reset (I ² C state machine reset and register reset). This pin must be pulled high or left floating for normal operation in SMBus Slave Mode. |
| MISCELLANEOUS PINS | | | | |
| INT_N | H1 | Output, LVC MOS, Open-Drain | None | Open-drain 3.3-V tolerant active-low interrupt output. It pulls low when an interrupt occurs. The events which trigger an interrupt are programmable through SMBus registers. INT_N can be connected in a wired-OR fashion with other device's interrupt pin. A single pullup resistor in the 2-k Ω to 5-k Ω range is adequate for the entire INT_N net. |
| NC | A1, A2, A4, A5, L1, L2, L4, L5 | No connect on board | None | Unused pins. No connect on the PCB. |

Pin Functions (continued)

| PIN | | TYPE | INTERNAL PULLUP/ PULLDOWN | DESCRIPTION |
|--------------|---|---------------|------------------------------|---|
| NAME | NO. | | | |
| TEST0 | D10 | Input, LVCMOS | Weak pullup | Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5-V (maximum) output. |
| TEST1 | D2 | Input, LVCMOS | Weak pullup | |
| TEST2 | E10 | Input, LVCMOS | Weak pullup | |
| TEST3 | E2 | Input, LVCMOS | Weak pullup | |
| TEST4 | H10 | Input, LVCMOS | Weak pullup | |
| TEST5 | H2 | Input, LVCMOS | Weak pullup | |
| POWER | | | | |
| GND | A3, A6, A9, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, C1, C6, C11, D6, E3, E5, E7, E9, F3, F4, F5, F6, F7, F8, F9, G2, G3, G5, G7, G9, G10, H6, J1, J6, J11, K1, K2, K3, K4, K5, K6, K7, K8, K9, K10, K11, L3, L6, L9 | Power | None | Ground reference. The GND pins on this device must be connected through a low-resistance path to the board GND plane. |
| VDD | C3, C9, D3, D4, D5, D7, D8, D9, H3, H4, H5, H7, H8, H9, J3, J9 | Power | None | Power supply, VDD = 2.5 V ±5%. TI recommends connecting at least six de-coupling capacitors between the DS250DF210's VDD plane and GND as close to the DS250DF210 as possible. For example, four 0.1-μF capacitors and two 1-μF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device must be connected through a low-resistance path to the board VDD plane. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------------------|---|------|------|------|
| VDD_ABSMAX | Supply voltage (VDD) | -0.5 | 2.75 | V |
| VIO _{2.5V,ABS} MAX | 2.5-V I/O voltage (LVCMOS, CMOS and Analog) | -0.5 | 2.75 | V |
| VIO _{3.3V,ABS} MAX | Open-drain voltage (SDA, SDC, INT_N) and LVCMOS input voltage (READ_EN_N) | -0.5 | 4.0 | V |
| VIN_ABSMAX | Signal input voltage (RXnP, RXnN) | -0.5 | 2.75 | V |
| VOUT_ABSMAX | Signal output voltage (TXnP, TXnN) | -0.5 | 2.75 | V |
| TJ_ABSMAX | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT | |
|--------------------|-------------------------|--|-------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------|--|-------|-------------------|------|
| VDD | Supply voltage, VDD to GND. DC plus AC power must not exceed these limits. | 2.375 | 2.625 | V |
| NVDD | Supply noise, DC to < 50 Hz, sinusoidal ⁽¹⁾ | | 250 | mVpp |
| NVDD | Supply noise, 50 Hz to 10 MHz, sinusoidal ⁽¹⁾ | | 20 | mVpp |
| NVDD | Supply noise, > 10 MHz, sinusoidal ⁽¹⁾ | | 10 | mVpp |
| T _{rampVDD} | VDD supply ramp time, from 0 V to 2.375 V | 150 | | µs |
| T _J | Operating junction temperature | -40 | 110 | °C |
| T _A | Operating ambient temperature | -40 | 85 ⁽²⁾ | °C |
| VIO _{2.5V} | 2.5 V I/O voltage (LVCMOS, CMOS and Analog) | 2.375 | 2.625 | V |
| VIO _{3.3V,INT_N} | Open Drain LVCMOS I/O voltage (INT_N) | | 3.6 | V |
| VIO _{3.3V} | Open Drain LVCMOS I/O voltage (SDA, SDC) | 2.375 | 3.6 | V |

- (1) Take steps to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.
- (2) Take steps to ensure the operating junction temperature range and ambient temperature stay-in-lock range (TEMP_{LOCK+}, TEMP_{LOCK-}) are met. Refer to *Electrical Characteristics* for more details concerning TEMP_{LOCK+} and TEMP_{LOCK-}.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | CONDITIONS/ASSUMPTIONS ⁽²⁾ | DS250DF210 | UNIT |
|---|---------------------------------------|--------------|------|
| | | ABM (FC/CSP) | |
| | | 101 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 4-Layer JEDEC Board | 34.2 | °C/W |
| | 10-Layer 8-in x 6-in Board | 16.7 | |
| | 20-Layer 8-in x 6-in Board | 15.6 | |
| | 30-Layer 8-in x 6-in Board | 14.6 | |
| R _{θJC(top)} Junction-to-case (top) thermal resistance | 4-Layer JEDEC Board | 7.8 | °C/W |
| R _{θJB} Junction-to-board thermal resistance | 4-Layer JEDEC Board | 13.7 | °C/W |
| Ψ _{JT} Junction-to-top characterization parameter | 4-Layer JEDEC Board | 0.004 | °C/W |
| | 10-Layer 8-in x 6-in Board | 0.004 | |
| | 20-Layer 8-in x 6-in Board | 0.004 | |
| | 30-Layer 8-in x 6-in Board | 0.004 | |
| Ψ _{JB} Junction-to-board characterization parameter | 4-Layer JEDEC Board | 13.0 | °C/W |
| | 10-Layer 8-in x 6-in Board | 11.7 | |
| | 20-Layer 8-in x 6-in Board | 11.5 | |
| | 30-Layer 8-in x 6-in Board | 11.3 | |

(1) For more information about traditional and new thermal metrics, see the [IC Package-Thermal Metrics](#) application report.

(2) No heat sink or airflow was assumed for these estimations. Depending on the application, a heat sink, faster airflow, and/or reduced ambient temperature (<85°C) may be required in order to meet the maximum junction temperature specification per the [Recommended Operating Conditions](#) section.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|-----|-------------------|------|
| R _{baud} Input data rate | Full-rate | 20.6 | | 25.8 | Gbps |
| | Half-rate | 10.3 | | 12.9 | |
| | Quarter-rate | 5.15 | | 6.45 | |
| t _{EEPROM} EEPROM configuration load time | Single device reading its configuration from an EEPROM. Common channel configuration. This time scales with the number of devices reading from the same EEPROM. | | | 15 ⁽¹⁾ | ms |
| t _{EEPROM} EEPROM configuration load time | Single device reading its configuration from an EEPROM. Unique channel configuration. This time scales with the number of devices reading from the same EEPROM. | | | 40 ⁽¹⁾ | ms |
| t _{POR} Power-on reset assertion time | Internal power-on reset (PoR) stretch between stable power supply and de-assertion of internal PoR. The SMBus address is latched on the completion of the PoR stretch, and SMBus accesses are permitted. | | | 50 | ms |

(1) From low assertion of READ_EN_N to low assertion of ALL_DONE_N. Does not include Power-On Reset time.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|--|-----|------|-----|------|
| POWER SUPPLY | | | | | | |
| W_{channel} | Power consumption per active channel | With CTLE, full DFE, Tx FIR, Driver and Crosspoint enabled. Idle power consumption not included. | | 241 | 305 | mW |
| | | With CTLE, full DFE, Tx FIR, and Driver enabled. Crosspoint disabled. Idle power consumption not included. | | 233 | | |
| | | With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; Crosspoint and DFE taps 3-5 disabled. Idle power consumption not included. | | 220 | | |
| | | With CTLE, Tx FIR, and Driver enabled; DFE disabled. Idle power consumption not included. | | 211 | 290 | |
| | | Assuming CDR acquiring lock with CTLE, full DFE, Tx FIR, Driver and Crosspoint enabled. Idle power consumption not included. | | 365 | 430 | |
| | | Assuming CDR acquiring lock with CTLE, Tx FIR, Driver and Crosspoint enabled; DFE disabled. Idle power consumption not included. | | 318 | 393 | |
| | | PRBS checker power consumption only ⁽²⁾ | | 220 | 302 | |
| | | PRBS generator power power consumption only ⁽²⁾ | | 230 | 315 | |
| $W_{\text{static_total}}$ | Total idle power consumption | Idle and static mode, power supplied, no high-speed data present at inputs, all channels automatically powered down. | | 329 | 525 | mW |
| I_{total} | Active mode total device supply current consumption | With CTLE, full DFE, Tx FIR, and Driver enabled. | | 318 | 432 | mA |
| | | With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; DFE taps 3-5 disabled. | | 308 | | |
| | | With CTLE, Tx FIR, and Driver enabled. DFE disabled. | | 300 | 421 | |
| $I_{\text{static_total}}$ | Idle mode total device supply current consumption | Idle and static mode. Power supplied, no high-speed data present at inputs, all channels automatically powered down. | | 132 | 200 | mA |
| LVC MOS DC SPECIFICATIONS | | | | | | |
| V_{IH} | Input high-level voltage | 2.5-V LVC MOS pins | | 1.75 | VDD | V |
| | | 3.3-V LVC MOS pin (READ_EN_N) | | 1.75 | 3.6 | V |
| V_{IL} | Input low-level voltage | 2.5-V LVC MOS pins | | GND | 0.7 | V |
| | | 3.3-V LVC MOS pin (READ_EN_N) | | GND | 0.8 | V |

(2) To ensure optimal performance, it is recommended to not enable more than two PRBS blocks (checker and/or generator) per device.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--|------|------------|-----|-------|
| V _{TH} | High level (1) input voltage | 4-level pins ADDR0, ADDR1, and EN_SMB | | 0.95 × VDD | | V |
| | Float level input voltage | 4-level pins ADDR0, ADDR1, and EN_SMB | | 0.67 × VDD | | V |
| | 10K to GND input voltage | 4-level pins ADDR0, ADDR1, and EN_SMB | | 0.33 × VDD | | V |
| | Low-level (0) input voltage | 4-level pins ADDR0, ADDR1, and EN_SMB | | 0.1 | | V |
| V _{OH} | High-level output voltage | I _{OH} = 4 mA | 2 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = -4 mA | | | 0.4 | V |
| I _{IH} | Input high leakage current | V _{input} = VDD, Open-drain pins | | | 70 | μA |
| I _{IH} | Input high leakage current | V _{input} = VDD and CAL_CLK_IN pin | | | 65 | μA |
| I _{IH} | Input high leakage current | V _{input} = VDD, ADDR[1:0] and EN_SMB pins | | | 120 | μA |
| I _{IH} | Input high leakage current | V _{input} = VDD, READ_EN_N | | | 75 | μA |
| I _{IL} | Input low leakage current | V _{input} = 0 V, Open-drain pins | -15 | | | μA |
| I _{IL} | Input low leakage current | V _{input} = 0 V, CAL_CLK_IN pins | -45 | | | μA |
| I _{IL} | Input low leakage current | V _{input} = 0 V, ADDR[1:0], READ_EN_N, and EN_SMB pins | -230 | | | μA |
| RECEIVER INPUTS (RXnP, RXnN) | | | | | | |
| V _{IDMax} | Maximum input differential voltage | For normal operation | | 1225 | | mVppd |
| RL _{SDD11} | Differential input return loss, SDD11 | Between 50 MHz and 3.69 GHz | | <-16 | | dB |
| RL _{SDD11} | Differential input return loss, SDD11 | Between 3.69 GHz and 12.9 GHz | | <-12 | | dB |
| RL _{SDC11} | Differential to common-mode input return loss, SDC11 | Between 50 MHz and 12.9 GHz | | <-23 | | dB |
| RL _{SCD11} | Differential to common-mode input return loss, SCD11 | Between 50 MHz and 12.9 GHz | | <-24 | | dB |
| RL _{SCC11} | Common-mode input return loss, SCC11 | Between 150 MHz and 10 GHz | | <-10 | | dB |
| RL _{SCC11} | Common-mode input return loss, SCC11 | Between 10 GHz and 12.9 GHz | | <-10 | | dB |
| V _{SDAT} | AC signal detect assert (ON) threshold level | Minimum input peak-to-peak amplitude level at device pins required to assert signal detect. 25.78125 Gbps with PRBS7 pattern and 20-dB loss channel | | 196 | | mVppd |
| V _{SDDT} | AC signal detect de-assert (OFF) threshold level | Maximum input peak-to-peak amplitude level at device pins which causes signal detect to de-assert. 25.78125 Gbps with PRBS7 pattern and 20-dB loss channel | | 147 | | mVppd |

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|------|------|-----|---------|
| TRANSMITTER OUTPUTS (TXnP, TXnN) | | | | | | |
| VOD | Output differential voltage amplitude | Measured with c(0)=7 setting (Reg_0x3D[6:0]=0x07, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1s followed by eight 0s) at 25.78125 Gbps with TXPn and TXNn terminated by 50 Ω to GND. | | 525 | | mVppd |
| VOD | Output differential voltage amplitude | Measured with c(0)=31 setting (Reg_0x3D[6:0]=0x1F, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1s followed by eight 0s) at 25.78125 Gbps with TXPn and TXNn terminated by 50 Ω to GND. | | 1225 | | mVppd |
| VOD _{idle} | Differential output amplitude with TX disabled | | | < 11 | | mVppd |
| VOD _{res} | Output VOD resolution | Difference in VOD between two adjacent c(0) settings. Applies to VOD in the 525 mVppd to 1225 mVppd range [c(0)>4]. | | < 50 | | mVppd |
| V _{cm-TX-AC} | Common-mode AC output noise | With respect to signal ground. Measured with PRBS9 data pattern. Measured with a 33 GHz (–3 dB) low-pass filter. | | 6.5 | | mV, RMS |
| t _r , t _f | Output transition time | 20%-to-80% rise time and 80%-to-20% fall time on a clock-like {1111100000} data pattern at 25.78125 Gbps. Measured for ~800 mVppd output amplitude and no equalization: Reg_0x3D=+13, Reg_0x3E=0, REG_0x3F=0 | | 17 | | ps |
| RL _{SDD22} | Differential output return loss, SDD22 | Between 50 MHz and 5 GHz | | <–12 | | dB |
| RL _{SDD22} | Differential output return loss, SDD22 | Between 5 GHz and 12.9 GHz | | <–9 | | dB |
| RL _{SCD22} | Common-mode to differential output return loss, SCD22 | Between 50 MHz and 12.9 GHz | | <–22 | | dB |
| RL _{SDC22} | Differential-to-common-mode output return loss, SDC22 | Between 50 MHz and 12.9 GHz | | <–22 | | dB |
| RL _{SCC22} | Common-mode output return loss, SCC22 | Between 50 MHz and 10 GHz | | <–9 | | dB |
| RL _{SCC22} | Common-mode output return loss, SCC22 | Between 10 GHz and 12.9 GHz | | <–9 | | dB |
| SMBus ELECTRICAL CHARACTERISTICS (SLAVE MODE) | | | | | | |
| V _{IH} | Input high level voltage | SDA and SDC | 1.75 | | 3.6 | V |
| V _{IL} | Input low level voltage | SDA and SDC | GND | | 0.8 | V |
| C _{IN} | Input pin capacitance | | | 15 | | pF |
| V _{OL} | Low level output voltage | SDA or SDC, IOL = 1.25 mA | | | 0.4 | V |
| I _{IN} | Input current | SDA or SDC, VINUT = VIN, VDD, GND | –15 | | 15 | μA |
| T _R | SDA rise time, read operation | Pullup resistor = 1 kΩ, Cb = 50 pF | | 150 | | ns |
| T _F | SDA fall time, read operation | Pullup resistor = 1 kΩ, Cb = 50 pF | | 4.5 | | ns |

7.6 Timing Requirements, Retimer Jitter Specifications

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----|------|-----|---------------------------|
| J _{TJ} | Output total jitter (TJ) | Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded. | | 0.17 | | U _{Ipp} at 1E-12 |
| J _{RJ} | Output random jitter (RJ) | Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded | | 6 | | mUI RMS |
| J _{DCD} | Output duty cycle distortion (DCD) | Measured at 25.78125 Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded | | 4 | | mUI _{pp} |
| J _{PEAK} | Jitter peaking | Measured at 10.3125 Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 6 MHz. | | 0.8 | | dB |
| J _{PEAK} | Jitter peaking | Measured at 25.78125 Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 17 MHz. | | 0.4 | | dB |
| BW _{PLL} | PLL bandwidth | Data rate of 10.3125 Gbps with PRBS7 pattern | | 5.3 | | MHz |
| BW _{PLL} | PLL bandwidth | Data rate of 25.78125 Gbps with PRBS7 pattern | | 5.5 | | MHz |
| J _{TOL} | Input jitter tolerance | Measured at 25.78125 Gbps with SJ frequency = 190 KHz, 30-dB input channel loss, PRBS31 data pattern, 800 mVppd launch amplitude, and 0.078 U _{Ipp} total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12. | | 9 | | U _{Ipp} |
| J _{TOL} | Input jitter tolerance | Measured at 25.78125 Gbps with SJ frequency = 940 KHz, 30-dB input channel loss, PRBS31 data pattern, 800 mVppd launch amplitude, and 0.078 U _{Ipp} total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12. | | 1 | | U _{Ipp} |
| J _{TOL} | Input jitter tolerance | Measured at 25.78125 Gbps with SJ frequency > 15 MHz, 30-dB input channel loss, PRBS31 data pattern, 800-mVppd launch amplitude, and 0.078 U _{Ipp} total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12. | | 0.3 | | U _{Ipp} |
| TEMP _{LOCK-} | CDR stay-in-lock ambient temperature range, negative ramp. Maximum temperature <i>change</i> below initial CDR lock acquisition temperature. | 85°C starting ambient temperature, ramp rate -3°C/minute, 1.7 liters/sec airflow, 12-layer PCB. | | 115 | | °C |
| TEMP _{LOCK+} | CDR stay-in-lock ambient temperature range, positive ramp. Maximum temperature <i>change</i> above initial CDR lock acquisition temperature. | -40°C starting ambient temperature, ramp rate +3°C/minute, 1.7 liters/sec airflow, 12-layer PCB. | | 125 | | °C |

7.7 Timing Requirements, Retimer Specifications

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|---|-----|-----------------|-----|------|
| t_D | Input-to-output latency (propagation delay) through a channel | | 3.5 UI + 125 ps | | ps |
| | CDR in raw (bypass) mode. | | < 145 | | ps |
| t_{SK} | Channel-to-channel interpair skew | | < 30 | | ps |
| t_{lock} | CDR lock acquisition time | | < 100 | | ms |
| t_{lock} | CDR lock acquisition time | | < 100 | | ms |

7.8 Timing Requirements, Recommended Calibration Clock Specifications

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|------|-----|-----|------|
| CLK_f | Calibration clock frequency | | 25 | | MHz |
| CLK_{PPM} | Calibration clock PPM tolerance | -100 | | 100 | PPM |
| CLK_{IDC} | Recommended/tolerable input duty cycle | 40% | 50% | 60% | |
| CLK_{ODC} | Intrinsic calibration clock duty cycle distortion | 45% | | 55% | |
| CLK_{num} | Number of devices which can be cascaded from CAL_CLK_OUT to CAL_CLK_IN | | 20 | | N/A |

7.9 Recommended SMBus Switching Characteristics (Slave Mode)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---------------------|-----|------|-----|------|
| f_{SDC} | SDC clock frequency | 10 | 100 | 400 | kHz |
| t_{HD-DAT} | Data hold time | | 0.75 | | ns |
| t_{SU-DAT} | Data setup time | | 100 | | ns |

7.10 Recommended SMBus Switching Characteristics (Master Mode)

over operating free-air temperature range (unless otherwise noted)

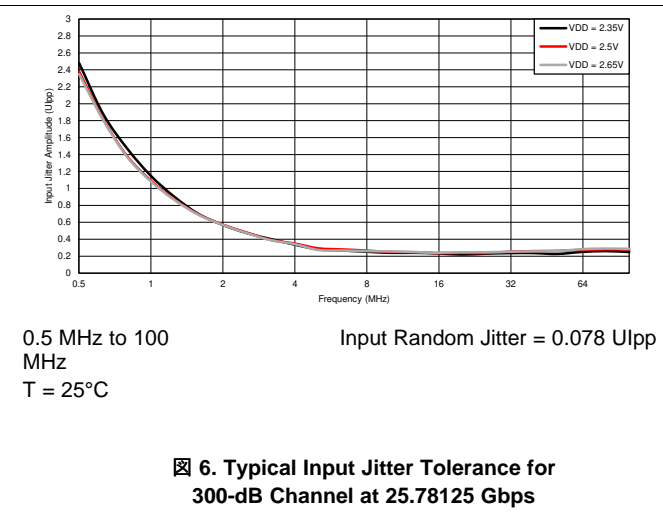
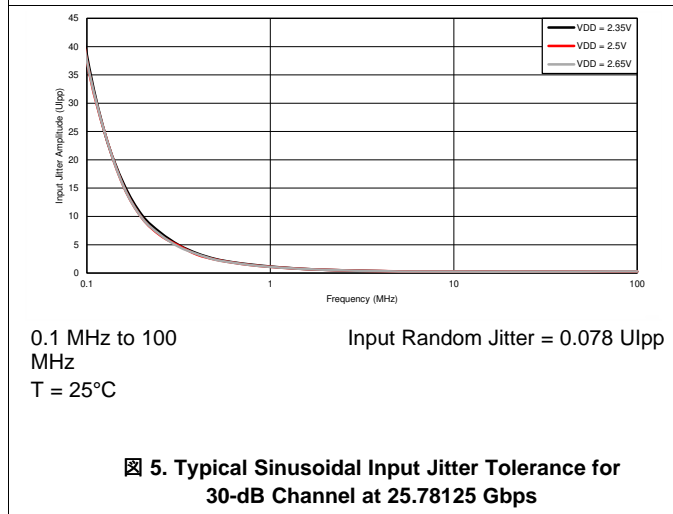
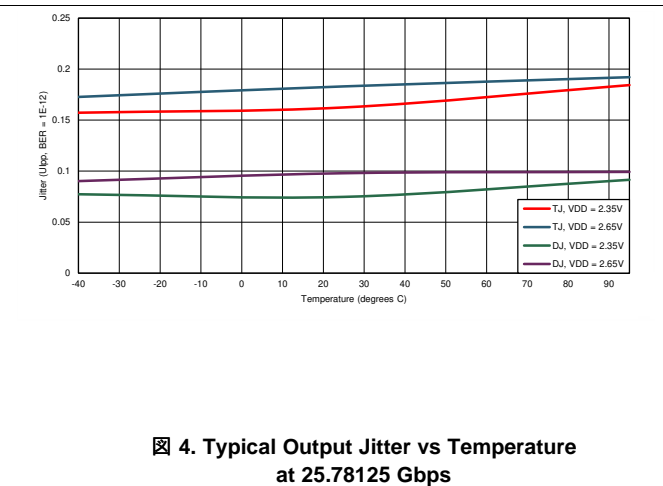
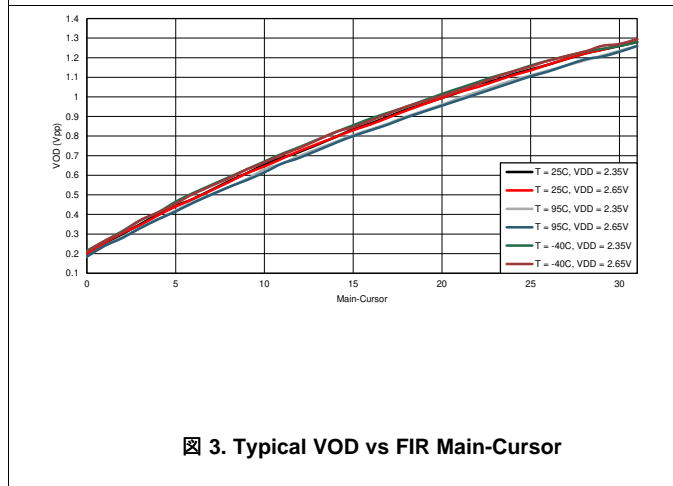
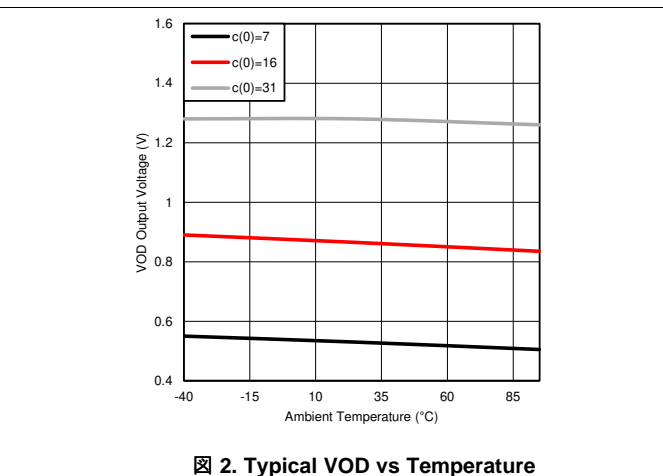
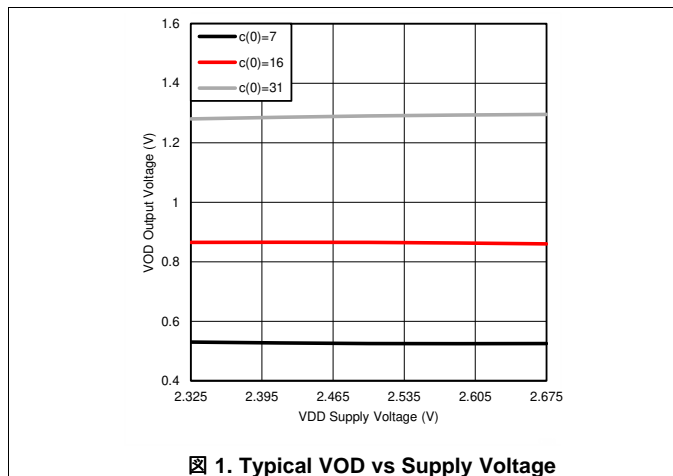
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|----------------------------------|------|------|------|---------|
| f_{SDC} | SDC clock frequency | 260 | 303 | 346 | kHz |
| T_{LOW} | SDC low period | 1.66 | 1.90 | 2.21 | μ s |
| T_{HIGH} | SDC high period | 1.22 | 1.40 | 1.63 | μ s |
| T_{HD-STA} | Hold time start operation | | 0.6 | | μ s |
| T_{SU-STA} | Setup time start operation | | 0.6 | | μ s |
| T_{HD-DAT} | Data hold time | | 0.6 | | μ s |
| T_{SD-DAT} | Data setup time | | 0.1 | | μ s |
| T_{SU-STO} | Stop condition setup time | | 0.6 | | μ s |
| T_{BUF} | Bus free time between Stop-Start | | 1.3 | | μ s |

Recommended SMBus Switching Characteristics (Master Mode) (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------|------------------------|-----|-----|-----|------|
| T _R | SDC rise time | Pullup resistor = 1 kΩ | | 300 | | ns |
| T _F | SDC fall time | Pullup resistor = 1 kΩ | | 300 | | ns |

7.11 Typical Characteristics



8 Detailed Description

8.1 Overview

The DS250DF210 is a two-channel multi-rate retimer with integrated signal conditioning. Each of the two channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS250DF210 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

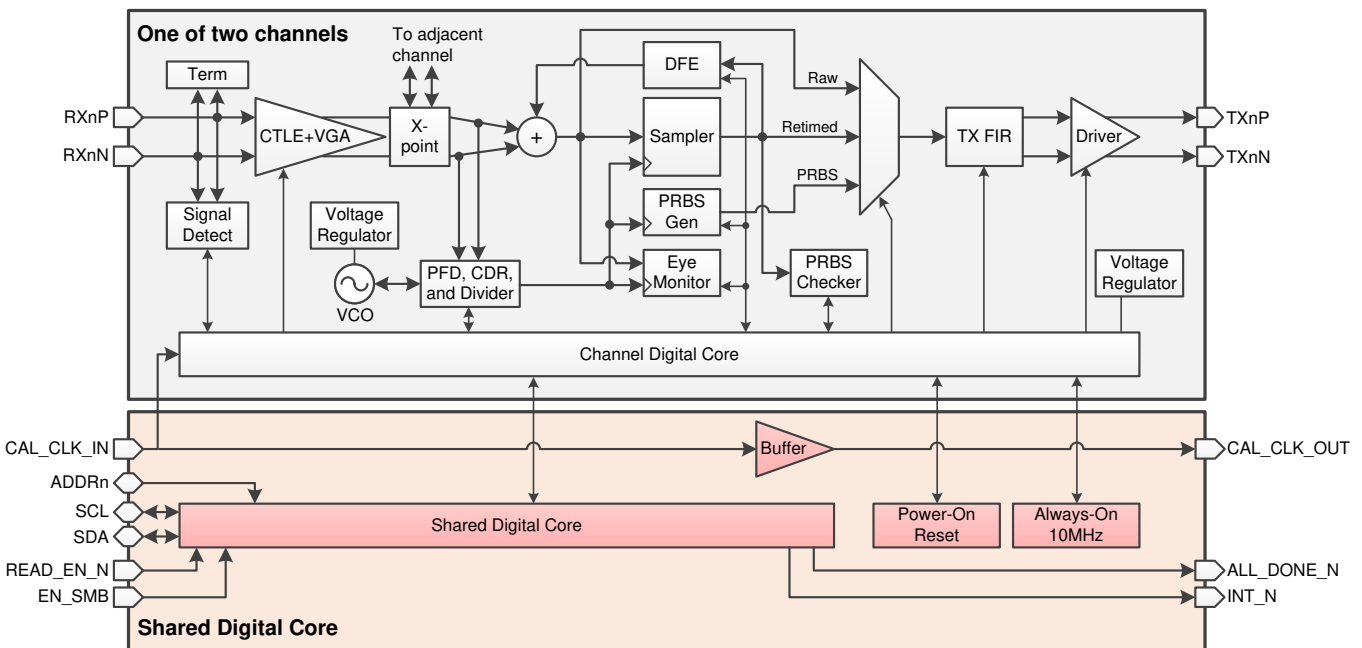
Each channel of the DS250DF210 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS250DF210. Between the two channels is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing/fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

The DS250DF210 is configurable through a single SMBus port. The DS250DF210 can also act as an SMBus master to configure itself from an EEPROM. Up to sixteen DS250DF210 devices can share a single SMBus.

The following sections describe the functionality of various circuits and features within the DS250DF210. For more information about how to program or operate these features, consult the [DS250DF210 Programming Guide](#) (SNLU202).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Data Path Operation

The DS250DF210 data path consists of several key blocks as shown in the functional block diagram. These key circuits are:

- [Signal Detect](#)
- [Continuous Time Linear Equalizer \(CTLE\)](#)
- [Variable Gain Amplifier \(VGA\)](#)
- [Decision Feedback Equalizer \(DFE\)](#)
- [Clock and Data Recovery \(CDR\)](#)
- [Calibration Clock](#)
- [Differential Driver With FIR Filter](#)

8.3.2 Signal Detect

The DS250DF210 receiver contains a signal detect circuit. The signal detect circuit monitors the energy level on the receiver inputs and powers on or off the rest of the high-speed data path if a signal is detected or not. By default, each channel allows the signal detect circuit to automatically power on or off the rest of the high speed data path depending on the presence of an input signal. The signal detect block can be manually controlled in the SMBus channel registers. This can be useful if it is desired to manually force channels to be disabled. For information on how to manually operate the signal detect circuit refer to the [DS250DF210 Programming Guide](#) (SNLU202).

8.3.3 Continuous Time Linear Equalizer (CTLE)

The CTLE in the DS250DF210 is a fully-adaptive equalizer. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. The FOM calculation is based upon the horizontal eye opening (HEO) and vertical eye opening (VEO). Once the CDR locks and the CTLE adapts, the CTLE boost level is frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE can be re-adapted by resetting the CDR.

The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 16 of these boost combinations. These 16 boost combinations comprise the EQ Table in the channel registers. See channel registers 0x40 through 0x4F in [表 6](#). This EQ Table can be reprogrammed to support up to 16 of the 256 boost settings.

The boost levels can be set between 8 dB and 25 dB (at 12.89 GHz.)

8.3.4 Variable Gain Amplifier (VGA)

The DS250DF210 receiver implements a VGA. The VGA assists in the recovery of extremely small signals, working in conjunction with the CTLE to equalize and scale amplitude. The VGA has 1-bit control via Register 0x8E[0], and the VGA is enabled by default. In addition to the VGA, the CTLE implements its own gain control via register 0x13[5] to adjust the DC amplitude similar to the VGA. For more information on how to configure the VGA refer to the [DS250DF210 Programming Guide](#) (SNLU202).

8.3.5 Cross-Point Switch

The channels in the DS250DF210 have a 2x2 cross-point that may be enabled to implement a 2-to-1 mux, a 1-to-2 fanout, or an A-to-B/B-to-A lane cross.

8.3.6 Decision Feedback Equalizer (DFE)

A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of crosstalk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. Once the DFE has been enabled it can be configured to adapt only during lock acquisition or to adapt continuously. The DFE can also be manually configured to specified tap polarities and tap weights. However, when the DFE is configured manually the DFE auto-adaption must be disabled. For many applications with lower insertion loss (that is, < 30 dB) lower crosstalk, or lower reflections, part or all of the DFE can be disabled to reduce power consumption. The DFE can either be fully enabled (taps 1-5), partially enabled (taps 1-2 only), or fully disabled (no taps).

Feature Description (continued)

The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit.

表 1. DFE Tap Weights

| DFE PARAMETER | DECIMAL (REGISTER VALUE) | VALUE (mV) (TYP) |
|----------------------|--|------------------|
| Tap 1 Weight Range | 0 - 31 | 0 – 217 |
| Tap 2-5 Weight Range | 0 - 15 | 0 – 105 |
| Tap Weight Step Size | NA | 7 |
| Polarity | 0: (+) positive; feedback value creates a low-pass filter response, thus providing attenuation to correct for negative-sign postcursor ISI 1: (-) negative; Feedback value creates a high-pass filter response, thus providing boost to correct for positive-sign postcursor ISI. | |

8.3.7 Clock and Data Recovery (CDR)

The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator, and output muted modes.

By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5 MHz (typical) in full-rate (divide-by-1) mode and 5.3 MHz (typical) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the [DS250DF210 Programming Guide](#) (SNLU202) for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.

The CDR requires the following in order to be properly configured:

- 25-MHz calibration clock to run the PPM counter (CAL_CLK_IN).
- Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the [DS250DF210 Programming Guide](#) (SNLU202) for more information on configuring the CDR for different data rates.

8.3.8 Calibration Clock

The calibration clock is not part of the CDR's PLL and thus is not used for clock and data recovery. The calibration clock is connected only to the PPM counter for each CDR. The PPM counter constrains the allowable lock ranges of the CDR according to the programmed values in the rate table or the manually entered data rates. The host should provide an input calibration clock signal of 25-MHz frequency. Because this clock is not used for clock and data recovery, there are no stringent jitter requirements placed on this 25 MHz calibration clock.

8.3.9 Differential Driver With FIR Filter

The DS250DF210 output driver has a three-tap finite impulse response (FIR) filter which allows for precursor and postcursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].

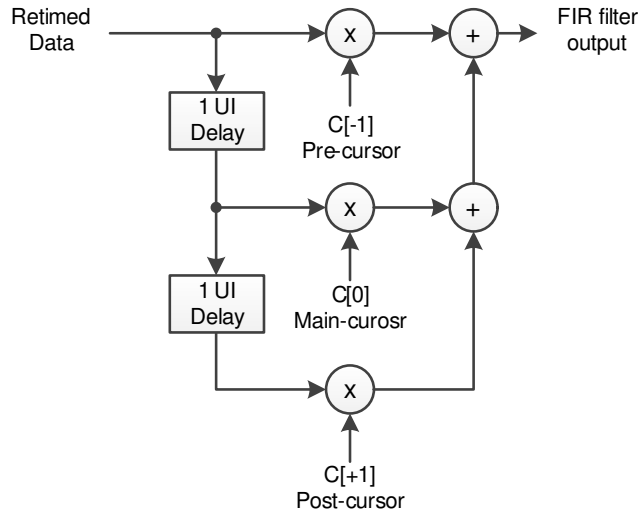


Fig 7. FIR Filter Functional Model

When using the FIR filter, it is important to abide by the following general rules:

- $|C[-1]| + |C[0]| + |C[+1]| \leq 31$; the FIR tap coefficients absolute sum must be less or equal to 31
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) \neq \text{sgn}(C[0])$, for high-pass filter effect; the sign for the precursor or postcursor tap must be different from main-cursor tap to realize boost effect
- $\text{sgn}(C[-1]) = \text{sgn}(C[+1]) = \text{sgn}(C[0])$, for low-pass filter effect; the sign for the precursor or postcursor tap must be equal to the main-cursor tap to realize attenuation effect

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the precursor tap, and the bit after the transition is accentuated through the postcursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

- $VOD_{pk-pk} = V_7 - V_8$
- $VOD_{low-frequency} = V_2 - V_5$
- $Rpre_{dB} = 20 * \log_{10} (v_3/v_2)$
- $Rpst_{dB} = 20 * \log_{10} (v_1/v_2)$

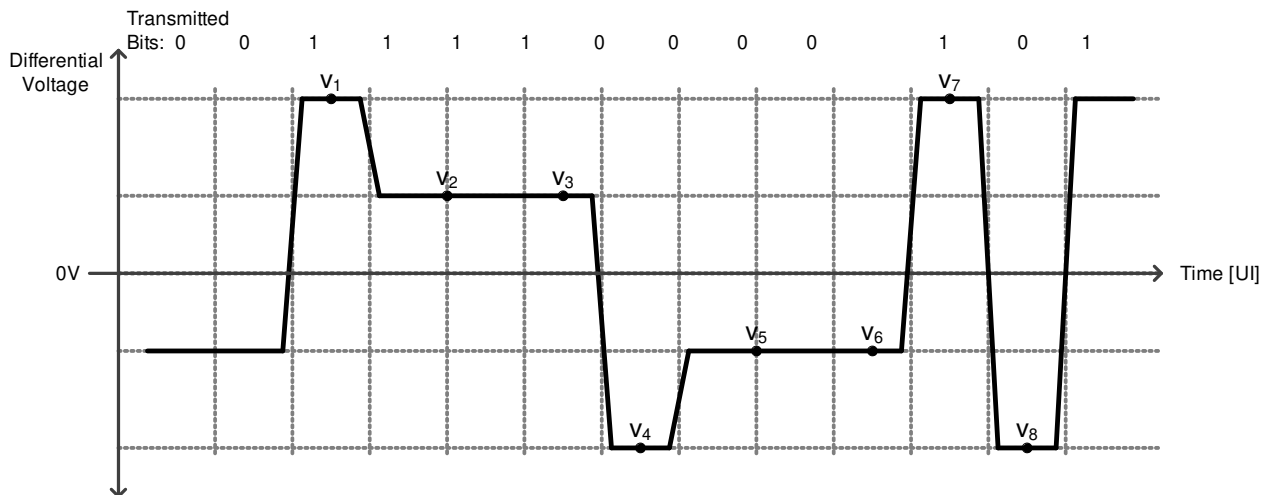


Fig 8. Conceptual FIR Waveform With Postcursor Only

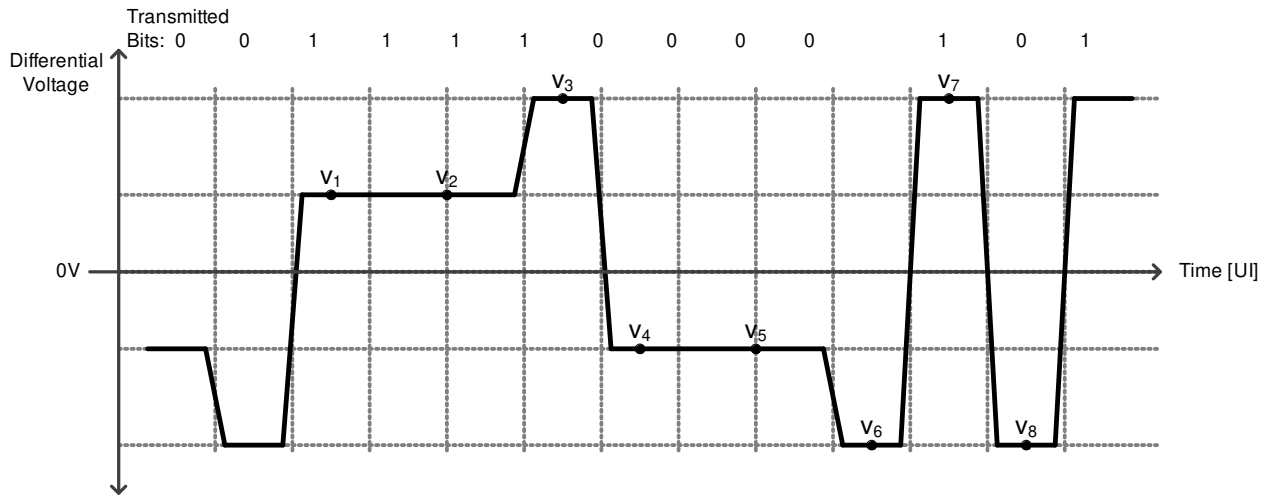


图 9. Conceptual FIR Waveform With Precursor Only

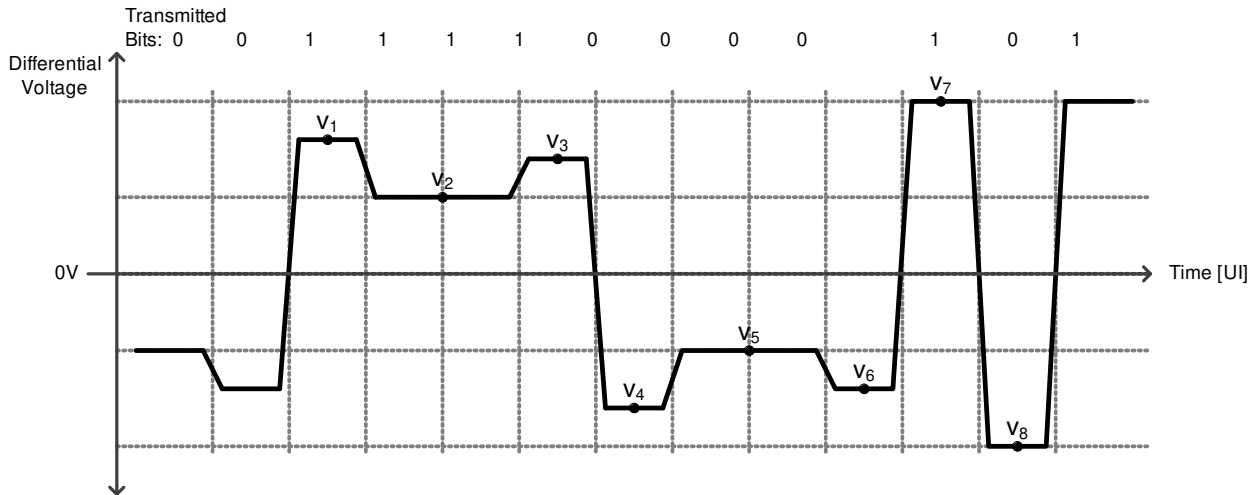


图 10. Conceptual FIR Waveform With Both Precursor and Postcursor

8.3.9.1 Setting the Output V_{OD} , Precursor, and Postcursor Equalization

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak V_{OD} , the user should adjust the main cursor tap value relative to the pre and post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

表 2. Typical VOD and FIR Values

| FIR SETTINGS | | | PEAK-TO-PEAK VOD(V) | RPRE (dB) | RPST (dB) |
|-----------------------------|-------------------------------|------------------------------|---------------------|-----------|-----------|
| PRECURSOR: REG_0x3E[6:0] | MAIN CURSOR: REG_0x3D[6:0] | POSTCURSOR: REG_0x3F[6:0] | | | |
| 0 | 0 | 0 | 0.205 | NA | NA |
| 0 | +1 | 0 | 0.260 | NA | NA |
| 0 | +2 | 0 | 0.305 | NA | NA |

表 2. Typical VOD and FIR Values (continued)

| FIR SETTINGS | | | PEAK-TO-PEAK VOD(V) | RPRE (dB) | RPST (dB) |
|-----------------------------|-------------------------------|------------------------------|------------------------|-----------|-----------|
| PRECURSOR: REG_0x3E[6:0] | MAIN CURSOR: REG_0x3D[6:0] | POSTCURSOR: REG_0x3F[6:0] | | | |
| 0 | +3 | 0 | 0.355 | NA | NA |
| 0 | +4 | 0 | 0.395 | NA | NA |
| 0 | +5 | 0 | 0.440 | NA | NA |
| 0 | +6 | 0 | 0.490 | NA | NA |
| 0 | +7 | 0 | 0.525 | NA | NA |
| 0 | +8 | 0 | 0.565 | NA | NA |
| 0 | +9 | 0 | 0.610 | NA | NA |
| 0 | +10 | 0 | 0.650 | NA | NA |
| 0 | +11 | 0 | 0.685 | NA | NA |
| 0 | +12 | 0 | 0.720 | NA | NA |
| 0 | +13 | 0 | 0.760 | NA | NA |
| 0 | +14 | 0 | 0.790 | NA | NA |
| 0 | +15 | 0 | 0.825 | NA | NA |
| 0 | +16 | 0 | 0.860 | NA | NA |
| 0 | +17 | 0 | 0.890 | NA | NA |
| 0 | +18 | 0 | 0.925 | NA | NA |
| 0 | +19 | 0 | 0.960 | NA | NA |
| 0 | +20 | 0 | 0.985 | NA | NA |
| 0 | +21 | 0 | 1.010 | NA | NA |
| 0 | +22 | 0 | 1.040 | NA | NA |
| 0 | +23 | 0 | 1.075 | NA | NA |
| 0 | +24 | 0 | 1.095 | NA | NA |
| 0 | +25 | 0 | 1.125 | NA | NA |
| 0 | +26 | 0 | 1.150 | NA | NA |
| 0 | +27 | 0 | 1.165 | NA | NA |
| 0 | +28 | 0 | 1.190 | NA | NA |
| 0 | +29 | 0 | 1.205 | NA | NA |
| 0 | +30 | 0 | 1.220 | NA | NA |
| 0 | +31 | 0 | 1.225 | NA | NA |
| 0 | +18 | -1 | 0.960 | NA | 2.1 |
| 0 | +17 | -2 | 0.960 | NA | 2.5 |
| 0 | +16 | -3 | 0.960 | NA | 3.1 |
| 0 | +15 | -4 | 0.960 | NA | 3.8 |
| 0 | +14 | -5 | 0.960 | NA | 4.7 |
| 0 | +13 | -6 | 0.960 | NA | 5.8 |
| 0 | +12 | -7 | 0.960 | NA | 7.2 |
| 0 | +11 | -8 | 0.960 | NA | 9.0 |
| 0 | +10 | -9 | 0.960 | NA | 11.6 |
| -1 | 18 | 0 | 0.960 | 1.0 | NA |
| -2 | 17 | 0 | 0.960 | 1.6 | NA |
| -3 | 16 | 0 | 0.960 | 2.4 | NA |
| -4 | 15 | 0 | 0.960 | 3.3 | NA |
| 0 | 26 | -1 | 1.165 | NA | 1.1 |
| 0 | 25 | -2 | 1.165 | NA | 1.3 |
| 0 | 24 | -3 | 1.165 | NA | 1.8 |
| 0 | 23 | -4 | 1.165 | NA | 2.2 |

表 2. Typical VOD and FIR Values (continued)

| FIR SETTINGS | | | PEAK-TO-PEAK VOD(V) | RPRE (dB) | RPST (dB) |
|--------------------------|----------------------------|---------------------------|---------------------|-----------|-----------|
| PRECURSOR: REG_0x3E[6:0] | MAIN CURSOR: REG_0x3D[6:0] | POSTCURSOR: REG_0x3F[6:0] | | | |
| 0 | 22 | -5 | 1.165 | NA | 2.7 |
| 0 | 21 | -6 | 1.165 | NA | 3.3 |
| 0 | 20 | -7 | 1.165 | NA | 3.9 |
| 0 | 19 | -8 | 1.165 | NA | 4.7 |
| 0 | 18 | -9 | 1.165 | NA | 5.7 |
| 0 | 17 | -10 | 1.165 | NA | 6.9 |
| 0 | 16 | -11 | 1.165 | NA | 8.4 |
| 0 | 15 | -12 | 1.165 | NA | 10.1 |
| -1 | 26 | 0 | 1.165 | 0.7 | NA |
| -2 | 25 | 0 | 1.165 | 1.2 | NA |
| -3 | 24 | 0 | 1.165 | 1.5 | NA |
| -4 | 23 | 0 | 1.165 | 2.0 | NA |
| -5 | 22 | 0 | 1.165 | 2.6 | NA |
| -6 | 21 | 0 | 1.165 | 3.2 | NA |
| -7 | 20 | 0 | 1.165 | 4.0 | NA |

The recommended precursor and postcursor settings for a given channel depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS250DF210 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of precursor or postcursor. The figures below give general recommendations for precursor and postcursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS250DF210 receiver.

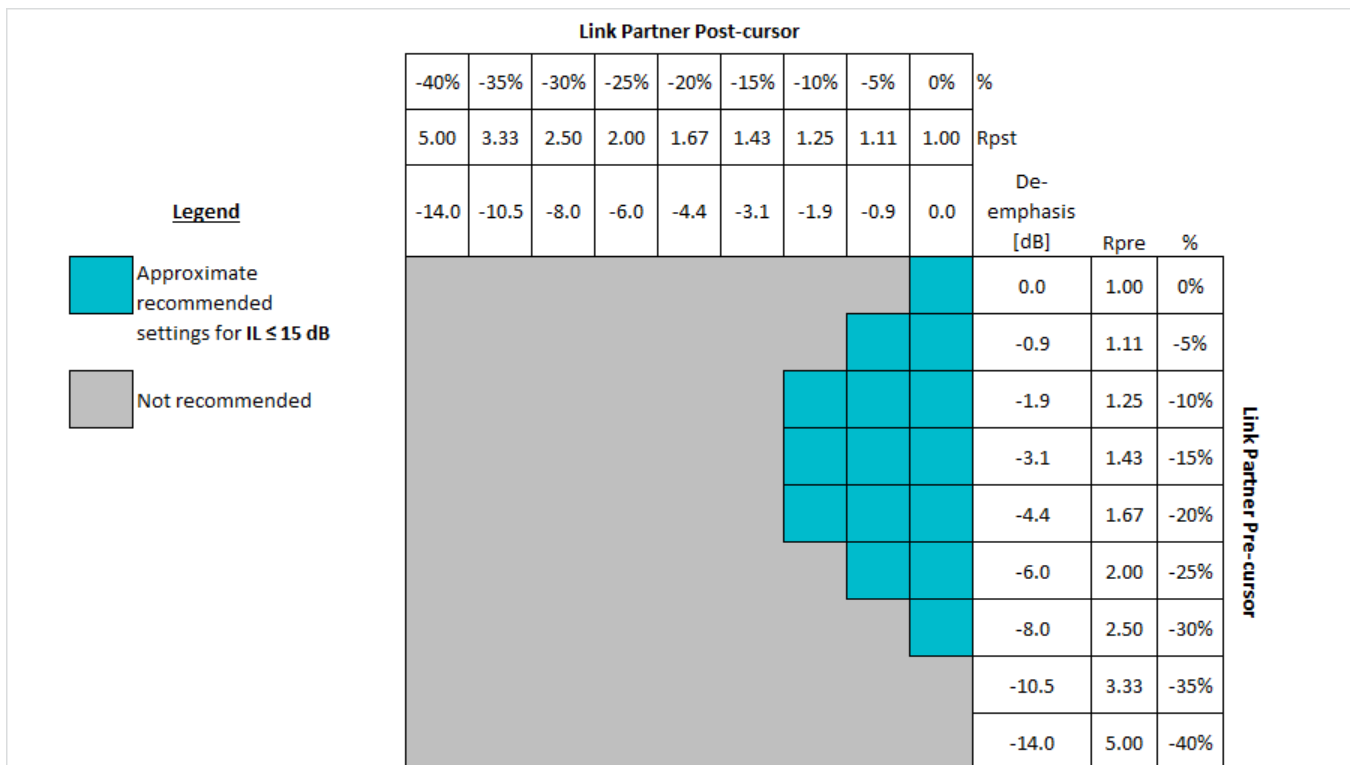
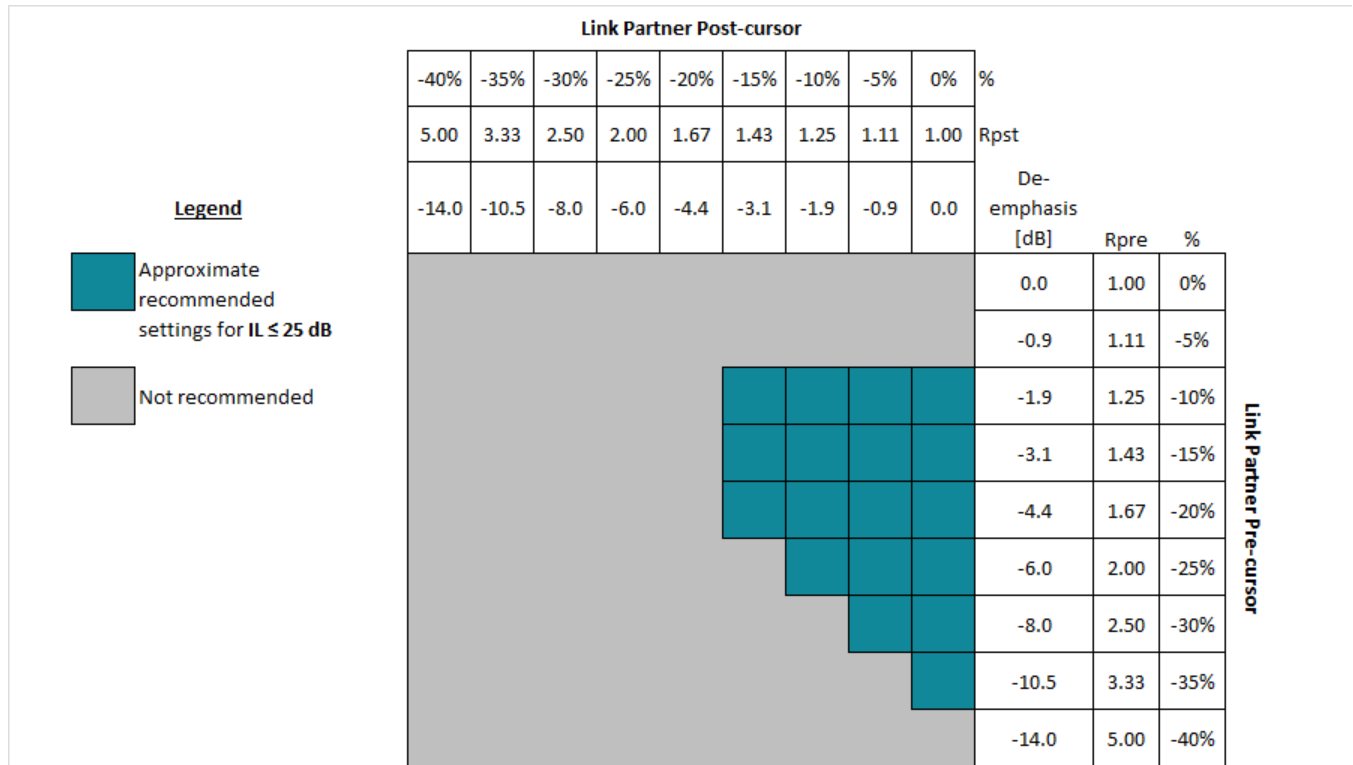
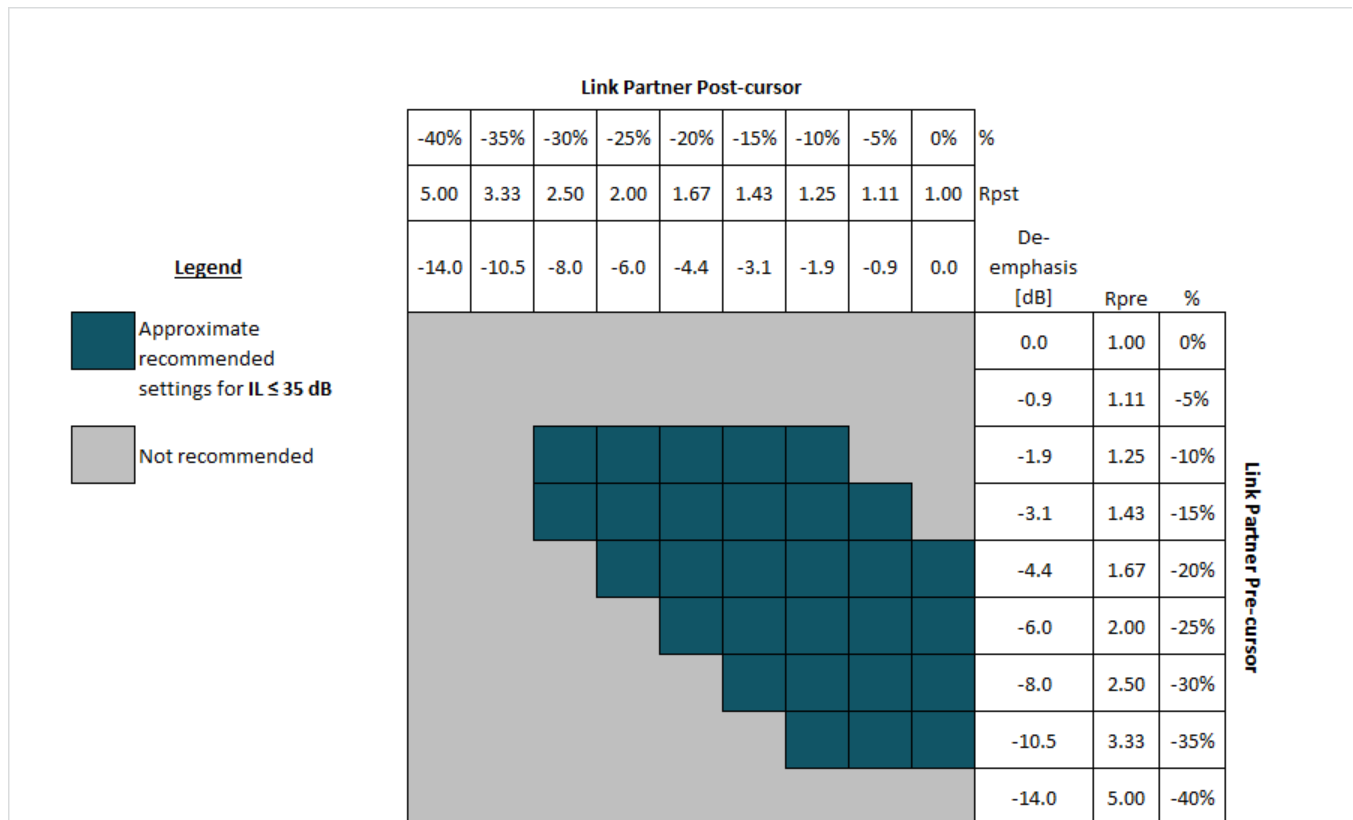


图 11. Guideline for Link Partner FIR Settings When IL ≤ 15 dB



☒ 12. Guideline for Link Partner FIR Settings When IL ≤ 25 dB



☒ 13. Guideline for Link Partner FIR Settings When IL ≤ 35 dB

8.3.9.2 Output Driver Polarity Inversion

In some applications, it may be necessary to invert the polarity of the data transmitted from the retimer. To invert the polarity of the data, read back the FIR polarity settings for the pre, main and post cursor taps and then invert these bits.

8.3.10 Debug Features

8.3.10.1 Pattern Generator

Each channel in the DS250DF210 can be configured to generate a 16-bit user-defined data pattern or a pseudo random bit sequence (PRBS). The user defined pattern can also be set to automatically invert every other 16-bit symbol for DC balancing purposes. The DS250DF210 pattern generator supports the following PRBS sequences:

- PRBS – $2^7 - 1$
- PRBS – $2^9 - 1$
- PRBS – $2^{11} - 1$
- PRBS – $2^{15} - 1$
- PRBS – $2^{23} - 1$
- PRBS – $2^{31} - 1$
- PRBS – $2^{58} - 1$
- PRBS – $2^{63} - 1$

8.3.10.2 Pattern Checker

The pattern checker can be manually set to look for specific PRBS sequences and polarities or it can be set to automatically detect the incoming pattern and polarity. The PRBS checker supports the same set of PRBS patterns as the PRBS generator.

The pattern checker consists of an 11-bit error counter. The pattern checker uses 32-bit words, but every bit in the word is checked for error, so the error count represents the count of single bit errors.

In order to read out the bit and error counters, the pattern checker must first be frozen. Continuous operation with simultaneous read out of the bit and error counters is not supported in this implementation. Once the bit and error counter is read, they can be un-frozen to continue counting.

8.3.10.3 Eye Opening Monitor

The DS250DF210's Eye Opening Monitor (EOM) measures the internal data eye at the input of the decision slicer and can be used for 2 functions:

1. Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) measurement
2. Full Eye Diagram Capture

The HEO measurement is made at the 0V crossing and is read in channel register 0x27. The VEO measurement is made at the 0.5 UI mark and is read in channel register 0x28. The HEO and VEO registers can be read from channel registers 0x27 and 0x28 at any time while the CDR is locked. The following equations are used to convert the contents of channel registers 0x27 and 0x28 into their appropriate units:

- $\text{HEO [UI]} = \text{Reg_0x27} \div 32$
- $\text{VEO [mV]} = \text{Reg_0x28} \times 3.125$

A full eye diagram capture can be performed when the CDR is locked. The eye diagram is constructed within a 64 x 64 array, where each cell in the matrix consists of an 16-bit word representing the total number of hits recorded at that particular phase and voltage offset. Users can manually adjust the vertical scaling of the EOM or allow the state machine to control the scaling which is the default option. The horizontal scaling controlled by the state machine and is always directly proportional to the data rate.

When a full eye diagram plot is captured, the retimer shifts out four 16-bit words of junk data that must be discarded followed by 4096 16-bit words that make up the 64 × 64 eye plot. The first actual word of the eye plot from the retimer is for (X, Y) position (0,0), which is the earliest position in time and the most negative position in voltage. Each time the eye plot data is read out the voltage position is incremented. Once the voltage position has incremented to position 63 (the most positive voltage), the next read causes the voltage position to reset to 0 (the most negative voltage) and the phase position to increment. This process continues until the entire 64 × 64 matrix is read out. Figure 14 below shows the EOM read out sequence overlaid on top of a simple eye opening plot. In this plot any hits are shown in green. This type of plot is helpful for quickly visualizing the HEO and VEO. Users can apply different algorithms to the output data to plot density or color gradients to the output data.

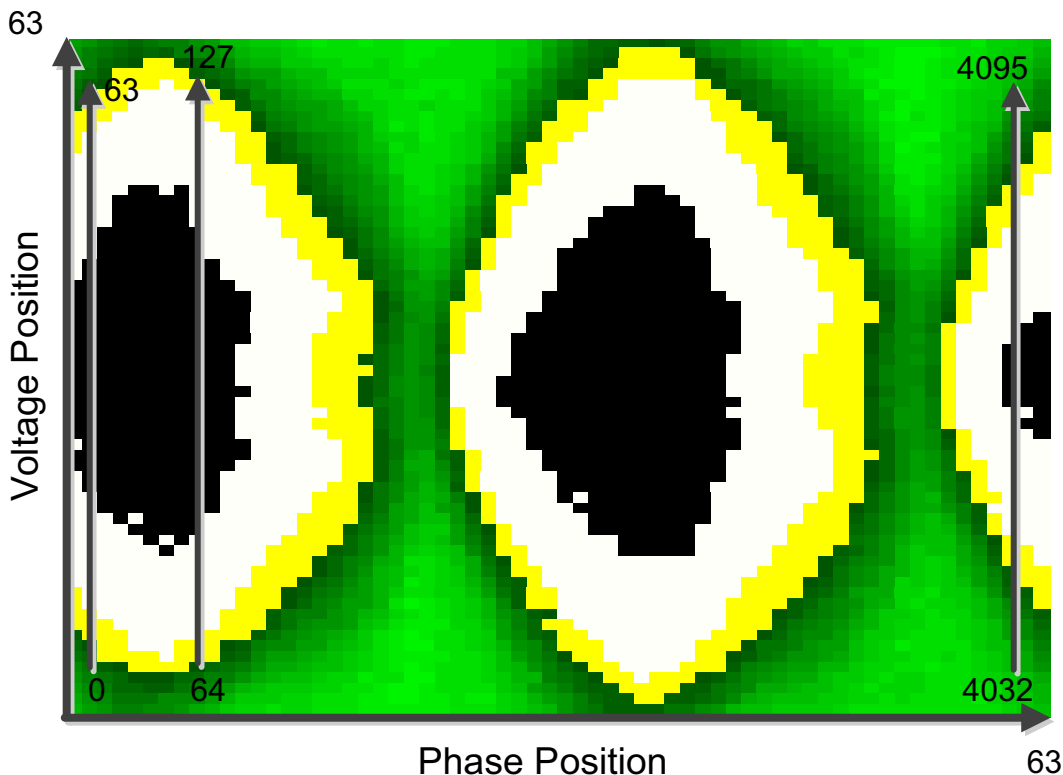


图 14. EOM Full Eye Capture Readout

To manually control the EOM vertical range, remove scaling control from the state machine then select the desired range:

Channel Reg 0x2C[6] → 0 (see 表 3).

表 3. Eye Opening Monitor Vertical Range Settings

| CH REG 0x11[7:6] VALUE | EOM VERTICAL RANGE [mV] |
|------------------------|-------------------------|
| 2'b00 | ±100 |
| 2'b01 | ±200 |
| 2'b10 | ±300 |
| 2'b11 | ±400 |

The EOM operates as an under-sampled circuit. This allows the EOM to be useful in identifying over equalization, ringing and other gross signal conditioning issues. However, the EOM cannot be correlated to a bit error rate.

The EOM can be accessed in two ways to read out the entire eye plot:

- Multi-byte reads can be used such that data is repeatedly latched out from channel register 0x25.
- With single byte reads, the MSB are located in register 0x25 and the LSB are located in register 0x26. In this mode, the device must be addressed each time a new byte is read.

To perform a full eye capture with the EOM, follow these steps below within the desired channel register set:

表 4. Eye Opening Monitor Full Eye Capture Instructions

| STEP | REGISTER [bits] | Operation | VALUE | DESCRIPTION |
|------|-----------------|-----------|-------|--|
| 1 | 0x67[5] | Write | 0 | Disable lock EOM lock monitoring |
| 2 | 0x2C[6] | Write | 0 | Set the desired EOM vertical range |
| | 0x11[7:6] | Write | 2'b-- | |
| 3 | 0x11[5] | Write | 0 | Power on the EOM |
| 4 | 0x24[7] | Write | 1 | Enable fast EOM |
| 5 | 0x24[0] | Read | 1 | Begin read out of the 64 x 64 array, discard first 4 words Ch reg 0x24[0] is self-clearing. |
| | 0x25 | | | 0x25 is the MSB of the 16-bit word |
| | 0x26 | | | 0x26 is the LSB of the 16-bit word |
| 6 | 0x25 | Read | | Continue reading information until the 64 x 64 array is complete. |
| | 0x26 | | | |
| 7 | 0x67[5] | Write | 1 | Return the EOM to its original state. Undo steps 1-4 |
| | 0x2C[6] | Write | 1 | |
| | 0x11[5] | Write | 1 | |
| | 0x24[7] | Write | 0 | |

8.3.11 Interrupt Signals

The DS250DF210 can be configured to report different events as interrupt signals. These interrupt signals do not impact the operation of the device, but merely report that the selected event has occurred. The interrupt bits in the register sets are all sticky bits. This means that when an event triggers an interrupt the status bit for that interrupt is set to logic HIGH. This interrupt status bit remains at logic HIGH until the bit has been read. Once the bit has been read, it is automatically cleared, which allows for new interrupts to be detected. The DS250DF210 reports the occurrence of an interrupt through the INT_N pin. The INT_N pin is an open-drain output that pulls the line low when an interrupt signal is triggered.

Note that all available interrupts are disabled by default. Users must activate the various interrupts before they can be used.

The interrupts available in the DS250DF210 are:

- CDR loss of lock
- CDR locked
- Signal detect loss
- Signal detected
- PRBS pattern checker bit error detected
- HEO/VEO threshold violation

When an interrupt occurs, share register 0x08 reports which channel generated the interrupt request. Users can then select the channel(s) that generated the interrupt request and service the interrupt by reading the appropriate interrupt status bits in the corresponding channel registers. For more information on reading interrupt status, refer to the [DS250DF210 Programming Guide](#) (SNLU202).

8.4 Device Functional Modes

8.4.1 Supported Data Rates

The DS250DF210 supports a wide range of input data rates, including divide-by-2 and divide-by-4 sub-rates. The supported data rates are listed in 表 5. Refer to the *DS250DF210 Programming Guide* (SNLU202) for information on configuring the DS250DF210 for different data rates.

表 5. Supported Data Rates

| DATA RATE RANGE | | DIVIDER | CDR MODE | COMMENT |
|-----------------|-------------|---------|----------|--|
| MIN | MAX | | | |
| ≥ 20.6 Gbps | ≤ 25.8 Gbps | 1 | Enabled | |
| ≥ 10.3 Gbps | ≤ 12.9 Gbps | 2 | Enabled | |
| > 6.45 Gbps | < 10.3 Gbps | N/A | Disabled | Output jitter is higher with CDR disabled. |
| ≥ 5.15 Gbps | ≤ 6.45 Gbps | 4 | Enabled | |
| ≥ 1.25 Gbps | < 5.15 Gbps | N/A | Disabled | Output jitter is higher with CDR disabled. |

8.4.2 SMBus Master Mode

SMBus master mode allows the DS250DF210 to program itself by reading directly from an external EEPROM. When using the SMBus master mode, the DS250DF210 reads directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- Maximum EEPROM size is 2048 Bytes
- Minimum EEPROM size for a single DS250DF210 with individual channel configuration is 305 Bytes (3 base header bytes + 12 address map bytes + 4 x 72 channel register bytes + 2 share register bytes; bytes are defined to be 8-bits)
- Set ENSMB = Float, for SMBus master mode
- The external EEPROM device address byte must be 0xA0
- The external EEPROM device must support 400kHz operation at 2.5V or 3.3V supply
- Set the SMBus address of the DS250DF210 by configuring the ADDR0 and ADDR1 pins

When loading multiple DS250DF210 devices from the same EEPROM, use these guidelines to configure the devices:

- Configure the SMBus addresses for each DS250DF210 to be sequential. The first device in the sequence must have an address of 0x30
- Daisy chain READ_EN_N and ALL_DONE_N from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
- If all of the DS250DF210 devices share the same EEPROM channel and share register settings, configure the common channel bit in the base header to 1. With common channel configuration enabled, each DS250DF210 device configures all channels with the same settings.

When loading a single DS250DF210 from an EEPROM, use these guidelines to configure the device:

- Set the common channel bit to 0 to allow for individual channel configuration, or set the common channel bit to 1 to load the same configuration settings to all channels.
- When configuring individual channels, a 1024 or 2048 Byte EEPROM must be used.
- If there are more than three DS250DF210 devices on a PCB that require individual channel configuration, then each device must have its own EEPROM.

8.4.3 Device SMBus Address

The DS250DF210's SMBus slave address is strapped at power up using the ADDR[1:0] pins. The pin state is read on power up, after the internal power-on reset signal is de-asserted. The ADDR[1:0] pins are four-level LVCMOS IOs, which provides for 16 unique SMBus addresses. The four levels are achieved by pin strap options as follows:

- 0: 1 kΩ to GND
- R: 10 kΩ to GND (20 kΩ also acceptable)
- F: Float
- 1: 1 kΩ to VDD

表 6. SMBus Address Map

| 8-BIT WRITE ADDRESS [HEX] | REQUIRED ADDRESS PIN STRAP VALUE | |
|---------------------------|----------------------------------|-------|
| | ADDR1 | ADDR0 |
| 0x30 | 0 | 0 |
| 0x32 | 0 | R |
| 0x34 | 0 | F |
| 0x36 | 0 | 1 |
| 0x38 | R | 0 |
| 0x3A | R | R |
| 0x3C | R | F |
| 0x3E | R | 1 |
| 0x40 | F | 0 |
| 0x42 | F | R |
| 0x44 | F | F |
| 0x46 | F | 1 |
| 0x48 | 1 | 0 |
| 0x4A | 1 | R |
| 0x4C | 1 | F |
| 0x4E | 1 | 1 |

8.5 Programming

8.5.1 Bit Fields in the Register Set

Many of the registers in the DS250DF210 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS250DF210 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, keep this procedure in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, use the procedure described above.

Most register bits can be read or written to. However, some register bits are constrained to specific interface instructions.

Register bits can have the following interface constraints:

- R - Read only
- RW - Read/Write
- RWSC - Read/Write, self-clearing

8.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS250DF210 has 3 types of registers:

- 1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.
- 2) Shared Registers – These registers are used for device-level configuration, status read back or control.
- 3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS250DF210 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved/unused registers – all other addresses

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device returns 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters/retimers have a vendor ID register (0xFE) which always reads back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus master and the DS250DF210.

8.6 Register Maps

Table 7. Global Registers

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-------------------|---|
| EF | 7 | 0 | R | N | SPARE | |
| | 6 | 0 | R | N | SPARE | |
| | 5 | 0 | R | N | SPARE | |
| | 4 | 0 | R | N | SPARE | |
| | 3 | 1 | R | N | CHAN_CONFIG_ID[3] | TI device ID (Quad count). DS250DF810: 0x0C DS250DF410 and DS250DF210: 0x0E |
| | 2 | 1 | R | N | CHAN_CONFIG_ID[2] | |
| | 1 | 1 | R | N | CHAN_CONFIG_ID[1] | |
| | 0 | 0 | R | N | CHAN_CONFIG_ID[0] | |
| F0 | 7 | 0 | R | N | VERSION[7] | Version ID |
| | 6 | 0 | R | N | VERSION[6] | |
| | 5 | 1 | R | N | VERSION[5] | |
| | 4 | 1 | R | N | VERSION[4] | |
| | 3 | 0 | R | N | VERSION[3] | |
| | 2 | 0 | R | N | VERSION[2] | |
| | 1 | 1 | R | N | VERSION[1] | |
| | 0 | 0 | R | N | VERSION[0] | |
| F1 | 7 | 0 | R | N | DEVICE_ID[7] | Full device ID |
| | 6 | 0 | R | N | DEVICE_ID[6] | |
| | 5 | 0 | R | N | DEVICE_ID[5] | |
| | 4 | 1 | R | N | DEVICE_ID[4] | |
| | 3 | 0 | R | N | DEVICE_ID[3] | |
| | 2 | 0 | R | N | DEVICE_ID[2] | |
| | 1 | 0 | R | N | DEVICE_ID[1] | |
| | 0 | 0 | R | N | DEVICE_ID[0] | |
| F3 | 7 | 0 | R | N | CHAN_VERSION[3] | Digital Channel Version |
| | 6 | 0 | R | N | CHAN_VERSION[2] | |
| | 5 | 0 | R | N | CHAN_VERSION[1] | |
| | 4 | 0 | R | N | CHAN_VERSION[0] | |
| | 3 | 0 | R | N | SHARE_VERSION[3] | Digital Share Version |
| | 2 | 0 | R | N | SHARE_VERSION[2] | |
| | 1 | 0 | R | N | SHARE_VERSION[1] | |
| | 0 | 0 | R | N | SHARE_VERSION[0] | |
| FB | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| FC | 7 | 0 | RW | N | EN_CH7 | Select channel 7 (DS250DF810 only) |
| | 6 | 0 | RW | N | EN_CH6 | Select channel 6 (DS250DF810 only) |
| | 5 | 0 | RW | N | EN_CH5 | Select channel 5 (DS250DF810 only) |
| | 4 | 0 | RW | N | EN_CH4 | Select channel 4 (DS250DF810 only) |

Register Maps (continued)
Table 7. Global Registers (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--------------|--|
| | 3 | 0 | RW | N | EN_CH3 | Select channel 3 (DS250DF810 and DS250DF410 only) |
| | 2 | 0 | RW | N | EN_CH2 | Select channel 2 (DS250DF810 and DS250DF410 only) |
| | 1 | 0 | RW | N | EN_CH1 | Select channel 1 |
| | 0 | 0 | RW | N | EN_CH0 | Select channel 0 |
| FD | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| FE | 7 | 0 | R | N | VENDOR_ID[7] | TI vendor ID |
| | 6 | 0 | R | N | VENDOR_ID[6] | |
| | 5 | 0 | R | N | VENDOR_ID[5] | |
| | 4 | 0 | R | N | VENDOR_ID[4] | |
| | 3 | 0 | R | N | VENDOR_ID[3] | |
| | 2 | 0 | R | N | VENDOR_ID[2] | |
| | 1 | 1 | R | N | VENDOR_ID[1] | |
| | 0 | 1 | R | N | VENDOR_ID[0] | |
| FF | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | EN_SHARE_Q1 | Select shared registers for quad 1 (DS250DF810 only) |
| | 4 | 0 | RW | N | EN_SHARE_Q0 | Select shared registers for quad 0 |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | WRITE_ALL_CH | Allows user to write to all channels as if they are the same, but only allows read back from the channel specified in 0xFC. Note: EN_CH_SMB must be = 1 or else this function is invalid. |
| | 0 | 0 | RW | N | EN_CH_SMB | 1: Enables SMBUS access to the channels specified in Reg_0xFC 0: The shared registers are selected |

Table 8. Shared Registers

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|----------|---------------------|---|
| 00 | 7 | 1 | R | N | SMBUS_ADDR[3] | SMBus Address Strapped 7-bit address is 0x18 + SMBus_Addr[3:0] |
| | 6 | 1 | R | N | SMBUS_ADDR[2] | |
| | 5 | 0 | R | N | SMBUS_ADDR[1] | |
| | 4 | 0 | R | N | SMBUS_ADDR[0] | |
| | 3:0 | 0 | R | N | RESERVED | RESERVED |
| 01 | 7 | 1 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 1 | R | N | RESERVED | RESERVED |
| | 4 | 1 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| 0 | 1 | R | N | RESERVED | RESERVED | |
| 02 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 03 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 04 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RWSC | N | RST_I2C_REGS | 1: Reset shared registers. This bit is self-clearing. 0: Normal operation |
| | 5 | 0 | RWSC | N | RST_I2C_MAS | 1: Reset for SMBus/I2C Master. This bit is self-clearing. 0: Normal operation |
| | 4 | 0 | RW | N | FRC_EEPRM_RD | 1: Force EEPROM Configuration 0: Normal operation |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 05 | 7 | 0 | RW | N | DISAB_EEPRM_CFG | 1: Disable Master Mode EEPROM configuration (if not started; this bit is not effective if EEPROM configuration is already started) 0: Normal operation |
| | 6:5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | R | N | EEPROM_READ_DONE | 1: SMBus Master mode EEPROM read complete 0: SMBus Master mode EEPROM read not started or not complete |
| | 3 | 0 | RW | N | TEST0_AS_CAL_CLK_IN | 1: Use TEST0 as the input for the 25MHz CAL_CLK instead of CAL_CLK_IN. This must be configured for quad0 only. 0: Normal operation. Use CAL_CLK_IN as the input for the 25MHz CAL_CLK. |
| | 2 | 0 | RW | Y | CAL_CLK_INV_DIS | 1: Disable the inversion of CAL_CLK_OUT 0: Normal operation. CAL_CLK_OUT is inverted with respect to CAL_CLK_IN. |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| 0 | 1 | RW | Y | RESERVED | RESERVED | |

Table 8. Shared Registers (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-------------------|---|
| 06 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 08 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | INT_Q0C3 | Interrupt from channel 3. For DS250DF810 only, this applies to the quad selected by Reg_0xFF[5:4]. Not applicable for DS250DF210. |
| | 2 | 0 | R | N | INT_Q0C2 | Interrupt from channel 2. For DS250DF810 only, this applies to the quad selected by Reg_0xFF[5:4]. Not applicable for DS250DF210. |
| | 1 | 0 | R | N | INT_Q0C1 | Interrupt from channel 1. For DS250DF810 only, this applies to the quad selected by Reg_0xFF[5:4]. |
| | 0 | 0 | R | N | INT_Q0C0 | Interrupt from channel 0. For DS250DF810 only, this applies to the quad selected by Reg_0xFF[5:4]. |
| 0A | 7:1 | 0 | R | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | DIS_REFCLK_OUT | 1: Disable CAL_CLK_OUT (high-Z) 0: Normal operation. Enable CAL_CLK_OUT |
| 0B | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | REFCLK_DET | 1: 25MHz clock detected on CAL_CLK_IN 0: No clock detected on CAL_CLK_IN |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | MR_REFCLK_DET_DIS | 0: CAL_CLK_IN detection and status reporting enabled (default) 1: CAL_CLK_IN detection disabled |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 0C | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 0D | 7:0 | 0 | R | N | RESERVED | RESERVED |
| 0E | 7:2 | 0 | RW | N | RESERVED | RESERVED |
| | 1:0 | 0 | R | N | RESERVED | RESERVED |
| 0F | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 10 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |

Table 8. Shared Registers (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|----------------|--|
| 11 | 7 | 0 | R | N | EECFG_CMPLT | 11: Not valid 10: EEPROM load completed successfully 01: EEPROM load failed after 64 attempts 00: EEPROM load in progress |
| | 6 | 0 | R | N | EECFG_FAIL | |
| | 5 | 0 | R | N | EECFG_ATMPT[5] | Number of attempts made to load EEPROM image |
| | 4 | 0 | R | N | EECFG_ATMPT[4] | |
| | 3 | 0 | R | N | EECFG_ATMPT[3] | |
| | 2 | 0 | R | N | EECFG_ATMPT[2] | |
| | 1 | 0 | R | N | EECFG_ATMPT[1] | |
| | 0 | 0 | R | N | EECFG_ATMPT[0] | |
| 12 | 7 | 1 | RW | N | REG_I2C_FAST | 1: EEPROM load uses Fast I2C Mode (400 kHz) 0: EEPROM load uses Standard I2C Mode (100 kHz) |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-------------------|---|
| 00 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RST_CORE | 1: Reset the 10M core clock domain. This is the main clock domain for all the state machines 0: Normal operation |
| | 2 | 0 | RW | N | RST_REGS | 1: Reset channel registers to power-up defaults. 0: Normal operation |
| | 1 | 0 | RW | N | RST_VCO | 1: Resets the CDR S2P clock domain, includes PPM counter, EOM counter. 0: Normal operation |
| | 0 | 0 | RW | N | RST_REFCLK | 1: Resets the 25MHz reference clock domain, includes PPM counter. Does not work if 25MHz clock is not present. 0: Normal operation |
| 01 | 7 | 0 | R | N | SIGDET | Raw Signal Detect observation |
| | 6 | 0 | R | N | POL_INV_DET | Indicates PRBS checker detected polarity inversion in the locked data sequence. |
| | 5 | 0 | R | N | CDR_LOCK_LOSS_INT | 1: Indicates loss of CDR lock after having acquired it. Bit clears on read. Feature must be enabled with Reg_0x31[1] |
| | 4 | 0 | R | N | PRBS_SEQ_DET[3] | Indicates the pattern detected on the input serial stream |
| | 3 | 0 | R | N | PRBS_SEQ_DET[2] | 0xxx: No detect 1000: 7 bits PRBS sequence 1001: 9 bits PRBS sequence 1010: 11 bits PRBS sequence 1011: 15 bits PRBS sequence 1100: 23 bits PRBS sequence 1101: 31 bits PRBS sequence 1110: 58 bits PRBS sequence 1111: 63 bits PRBS sequence |
| | 2 | 0 | R | N | PRBS_SEQ_DET[1] | |
| | 1 | 0 | R | N | PRBS_SEQ_DET[0] | |
| | 0 | 0 | R | N | SIG_DET_LOSS_INT | |
| 02 | 7 | 0 | R | N | CDR_STATUS[7] | This register is used to read the status of internal signal. Select what is observable on this bus using Reg_0x0C[7:4] |
| | 6 | 0 | R | N | CDR_STATUS[6] | |
| | 5 | 0 | R | N | CDR_STATUS[5] | |
| | 4 | 0 | R | N | CDR_STATUS[4] | |
| | 3 | 0 | R | N | CDR_STATUS[3] | |
| | 2 | 0 | R | N | CDR_STATUS[2] | |
| | 1 | 0 | R | N | CDR_STATUS[1] | |
| | 0 | 0 | R | N | CDR_STATUS[0] | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------|---|
| 03 | 7 | 0 | RW | Y | EQ_BST0[1] | This register can be used to force an EQ boost setting if used in conjunction with channel Reg_0x2D[3]. |
| | 6 | 0 | RW | Y | EQ_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_BST3[0] | |
| 04 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 05 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 06 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 07 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--|--|
| 08 | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |
| 09 | 7 | 0 | RW | Y | REG_VCO_CAP_OV | Enable bit to override cap_cnt with value in Reg_0x0B[4:0] |
| | 6 | 0 | RW | Y | REG_SET_CP_LVL_LPF_OV | Enable bit to override lpf_dac_val with value in Reg_0x1F[4:0] |
| | 5 | 0 | RW | Y | REG_BYPASS_PFD_OV | 0: Normal operation. |
| | 4 | 0 | RW | Y | REG_EN_FD_PD_VCO_PDIQ_OV | Enable bit to override en_fd, pd_pd, pd_vco, pd_pdiq with Reg_0x1E[0], Reg_0x1E[2], Reg_0x1C[0], Reg_0x1C[1] |
| | 3 | 0 | RW | Y | REG_EN_PD_CP_OV | Enable bit to override pd_fd_cp and pd_pd_cp with value in Reg_0x1B[1:0] |
| | 2 | 0 | RW | Y | REG_DIVSEL_OV | Enable bit to override divsel with value in Reg_0x18[6:4] |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 0A | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 0 | RW | Y | REG_EN_IDAC_PD_CP_OV_AND_REG_EN_IDAC_FD_CP_OV | Enable bit to override phase detector charge pump settings with Reg_0x1C[7:5] Enable bit to override frequency detector charge pump settings with Reg_0x1C[4:2] |
| | 5 | 0 | RW | Y | REG_DAC_LPF_HIGH_PHASE_OV_AND_REG_DAC_LPF_LOW_PHASE_OV | Enable bit to loop filter comparator trip voltages with Reg_0x16[7:0] |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | N | REG_CDR_RESET_OV | Enable CDR Reset override with Reg_0x0A[2] |
| | 2 | 0 | RW | N | REG_CDR_RESET_SM | CDR Reset override bit |
| | 1 | 0 | RW | N | REG_CDR_LOCK_OV | Enable CDR lock signal override with Reg_0x0A[0] |
| | 0 | 0 | RW | N | REG_CDR_LOCK | CDR lock signal override bit |
| 0B | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------|---|
| 0C | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 0D | 7 | 1 | RW | N | DES_PD | 1: De-serializer (for PRBS checker) is powered down 0: De-serializer (for PRBS checker) is enabled |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 0E | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 0F | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 10 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-------------------|--|
| 11 | 7 | 0 | RW | Y | EOM_SEL_VRANGE[1] | Manually set the EOM vertical range, used with channel Reg_0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV |
| | 6 | 0 | RW | Y | EOM_SEL_VRANGE[0] | |
| | 5 | 1 | RW | Y | EOM_PD | 1: Normal operation. Eye opening monitor (EOM) is automatically duty-cycled. 0: EOM is force-enabled |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | DFE_TAP2_POL | Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight |
| | 2 | 0 | RW | Y | DFE_TAP3_POL | Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight |
| | 1 | 0 | RW | Y | DFE_TAP4_POL | Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight |
| | 0 | 0 | RW | Y | DFE_TAP5_POL | Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight |
| 12 | 7 | 1 | RW | Y | DFE_TAP1_POL | Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | DFE_WT1[4] | These bits force DFE tap 1 weight. Manual DFE operation is required for this to take effect by setting Reg_0x15[7]=1. If Reg_0x15[7]=0, the value defined here is used as the initial DFE tap 1 weight during adaptation. |
| | 3 | 0 | RW | Y | DFE_WT1[3] | |
| | 2 | 0 | RW | Y | DFE_WT1[2] | |
| | 1 | 1 | RW | Y | DFE_WT1[1] | |
| | 0 | 1 | RW | Y | DFE_WT1[0] | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------|---|
| 13 | 7 | 1 | RW | N | EQ_PD_PEAKDETECT | 1: Normal operation. Power down test mode. 0: Test mode. |
| | 6 | 0 | RW | Y | EQ_PD_SD | 1: Power down signal detect. 0: Normal operation. Enable signal detect. |
| | 5 | 1 | RW | Y | EQ_HI_GAIN | 1: Enable high DC gain mode in the equalizer 0: Enable low DC gain mode in the equalizer (Refer to the Programming Guide for more details) |
| | 4 | 1 | RW | Y | EQ_EN_DC_OFF | 1: Normal operation. 0: Disable DC offset compensation. |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | EQ_LIMIT_EN | 1: Configures the final stage of the equalizer to be a limiting stage. 0: Normal operation, final stage of the equalizer is configured to be a non-limiting stage. |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 14 | 7 | 0 | RW | Y | EQ_SD_PRESET | 1: Forces signal detect HIGH, and force enables the channel. Should not be set if bit 6 is set. 0: Normal Operation. |
| | 6 | 0 | RW | Y | EQ_SD_RESET | 1: Forces signal detect LOW and force disables the channel. Should not be set if bit 7 is set. 0: Normal Operation. |
| | 5 | 0 | RW | Y | EQ_REFA_SEL1 | Controls the signal detect assert levels. (Refer to the Programming Guide for more details) |
| | 4 | 0 | RW | Y | EQ_REFA_SEL0 | |
| | 3 | 0 | RW | Y | EQ_REFD_SEL1 | Controls the signal detect de-assert levels. (Refer to the Programming Guide for more details) |
| | 2 | 1 | RW | Y | EQ_REFD_SEL0 | |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 15 | 7 | 0 | RW | Y | DFE_FORCE_EN | 1: Enables manual DFE tap settings 0: Normal operation |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | DRV_PD | 1: Powers down the high speed driver 0: Normal operation |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------|---|
| 16 | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 17 | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 0 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 18 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | PDIQ_SEL_DIV[2] | These bits will force the divider setting if 0x09[2] is set. 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 All other values are reserved. |
| | 5 | 0 | RW | Y | PDIQ_SEL_DIV[1] | |
| | 4 | 0 | RW | Y | PDIQ_SEL_DIV[0] | |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 19 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 1A | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RESERVED | RESERVED |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------|--|
| 1B | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | CP_EN_CP_PD | 1: Normal operation, phase detector charge pump enabled |
| | 0 | 1 | RW | Y | CP_EN_CP_FD | 1: Normal operation, frequency detector charge pump enabled |
| 1C | 7 | 1 | RW | Y | EN_IDAC_PD_CP2 | Phase detector charge pump setting. Override bit required for these bits to take effect |
| | 6 | 0 | RW | Y | EN_IDAC_PD_CP1 | |
| | 5 | 0 | RW | Y | EN_IDAC_PD_CP0 | |
| | 4 | 1 | RW | Y | EN_IDAC_FD_CP2 | Frequency detector charge pump setting. Override bit required for these bits to take effect |
| | 3 | 0 | RW | Y | EN_IDAC_FD_CP1 | |
| | 2 | 0 | RW | Y | EN_IDAC_FD_CP0 | |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 1D | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 1E | 7 | 1 | RW | Y | PFD_SEL_DATA_PRELCK[2] | Output mode for when the CDR is not locked. For these values to take effect, Reg_0x09[5] must be set to 0, which is the default. 000: Raw Data 111: Mute (Default) All other values are reserved. (Refer to the Programming Guide for more details) |
| | 6 | 1 | RW | Y | PFD_SEL_DATA_PRELCK[1] | |
| | 5 | 1 | RW | Y | PFD_SEL_DATA_PRELCK[0] | |
| | 4 | 0 | RW | N | SER_EN | 1: Enable serializer (used for PRBS Generator) 0: Normal operation. Disable serializer. |
| | 3 | 1 | RW | Y | DFE_PD | This bit must be cleared for the DFE to be functional in any adapt mode. 1: (Default) DFE disabled. 0: DFE enabled |
| | 2 | 0 | RW | Y | PFD_PD_PD | 1: Power down PFD phase detector. 0: Normal operation. Enable PFD phase detector. |
| | 1 | 0 | RW | Y | EN_PARTIAL_DFE | 1: Enable DFE taps 3-5. DFE_PD must also be set to 0. 0: (Default) Disable DFE taps 3-5. |
| | 0 | 1 | RW | Y | PFD_EN_FD | 1: Normal operation. Enable PFD frequency detector. 0: Disable PFD frequency detector. |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------------|--|
| 1F | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | MR_LPF_AUTO_ADJUST_EN | 1: Normal operation. Allow LPF to tune to optimum value during fast-cap search routine. 0: Otherwise LPF value is determined by the Reg_0x9D. |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |
| 20 | 7 | 0 | RW | Y | DFE_WT5[3] | Bits force DFE tap 5 weight, manual DFE operation required to take effect by setting 0x15[7]=1. |
| | 6 | 0 | RW | Y | DFE_WT5[2] | |
| | 5 | 0 | RW | Y | DFE_WT5[1] | |
| | 4 | 0 | RW | Y | DFE_WT5[0] | |
| | 3 | 0 | RW | Y | DFE_WT4[3] | Bits force DFE tap 4 weight, manual DFE operation required to take effect by setting 0x15[7]=1. |
| | 2 | 0 | RW | Y | DFE_WT4[2] | |
| | 1 | 0 | RW | Y | DFE_WT4[1] | |
| | 0 | 0 | RW | Y | DFE_WT4[0] | |
| 21 | 7 | 0 | RW | Y | DFE_WT3[3] | Bits force DFE tap 3 weight, manual DFE operation required to take effect by setting 0x15[7]=1. |
| | 6 | 0 | RW | Y | DFE_WT3[2] | |
| | 5 | 0 | RW | Y | DFE_WT3[1] | |
| | 4 | 0 | RW | Y | DFE_WT3[0] | |
| | 3 | 0 | RW | Y | DFE_WT2[3] | Bits force DFE tap 2 weight, manual DFE operation required to take effect by setting 0x15[7]=1. |
| | 2 | 0 | RW | Y | DFE_WT2[2] | |
| | 1 | 0 | RW | Y | DFE_WT2[1] | |
| | 0 | 0 | RW | Y | DFE_WT2[0] | |
| 22 | 7 | 0 | RW | N | EOM_OV | 1: Override enable for EOM manual control 0: Normal operation |
| | 6 | 0 | RW | N | EOM_SEL_RATE_OV | 1: Override enable for EOM rate selection 0: Normal operation |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------------|--|
| 23 | 7 | 0 | RW | N | EOM_GET_HEO_VEO_OV | 1: Override enable for manual control of the HEO/VEO trigger 0: Normal operation |
| | 6 | 1 | RW | Y | DFE_OV | 1: Normal operation; DFE must be enabled in Reg_0x1E[3]. |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| 24 | 7 | 0 | RW | N | FAST_EOM | 1: Enables fast EOM for full eye capture. In this mode the phase DAC and voltage DAC or the EOM are automatically incremented through a 64 x 64 matrix. Values for each point are stored in Reg_0x25 and Reg_0x26. 0: Normal operation. |
| | 6 | 0 | R | N | DFE_EQ_ERROR_NO_LOCK | DFE/CTLE SM quit due to loss of lock |
| | 5 | 0 | R | N | GET_HEO_VEO_ERROR_NO_HITS | get_heo_veo sees no hits at zero crossing |
| | 4 | 0 | R | N | GET_HEO_VEO_ERROR_NO_OPENING | get_heo_veo cannot see a vertical eye opening |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RWSC | N | DFE_ADAPT | 1: Manually start DFE adaption (self-clearing). 0: Normal operation. |
| | 1 | 0 | R | N | EOM_GET_HEO_VEO | 1: Manually triggers HEO/VEO measurement; feature must be enabled with Reg_0x23[7]; the HEO/VEO values are read from Reg_0x27, Reg_0x28 |
| 25 | 7 | 0 | R | N | EOM_COUNT15 | MSBs of EOM counter |
| | 6 | 0 | R | N | EOM_COUNT14 | |
| | 5 | 0 | R | N | EOM_COUNT13 | |
| | 4 | 0 | R | N | EOM_COUNT12 | |
| | 3 | 0 | R | N | EOM_COUNT11 | |
| | 2 | 0 | R | N | EOM_COUNT10 | |
| | 1 | 0 | R | N | EOM_COUNT9 | |
| 26 | 7 | 0 | R | N | EOM_COUNT7 | LSBs of EOM counter |
| | 6 | 0 | R | N | EOM_COUNT6 | |
| | 5 | 0 | R | N | EOM_COUNT5 | |
| | 4 | 0 | R | N | EOM_COUNT4 | |
| | 3 | 0 | R | N | EOM_COUNT3 | |
| | 2 | 0 | R | N | EOM_COUNT2 | |
| | 1 | 0 | R | N | EOM_COUNT1 | |
| 26 | 0 | 0 | R | N | EOM_COUNT0 | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------------|--|
| 27 | 7 | 0 | R | N | HEO7 | HEO value, requires CDR to be locked for valid measurement |
| | 6 | 0 | R | N | HEO6 | |
| | 5 | 0 | R | N | HEO5 | |
| | 4 | 0 | R | N | HEO4 | |
| | 3 | 0 | R | N | HEO3 | |
| | 2 | 0 | R | N | HEO2 | |
| | 1 | 0 | R | N | HEO1 | |
| | 0 | 0 | R | N | HEO0 | |
| 28 | 7 | 0 | R | N | VEO7 | VEO value, requires CDR to be locked for valid measurement |
| | 6 | 0 | R | N | VEO6 | |
| | 5 | 0 | R | N | VEO5 | |
| | 4 | 0 | R | N | VEO4 | |
| | 3 | 0 | R | N | VEO3 | |
| | 2 | 0 | R | N | VEO2 | |
| | 1 | 0 | R | N | VEO1 | |
| | 0 | 0 | R | N | VEO0 | |
| 29 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | EOM_VRANGE_SETTING[1] | Read the currently set Eye Monitor Voltage Range: 11 - +/-400mV 10 - +/- 300mV 01 - +/- 200mV 00 - +/- 100mV" |
| | 5 | 0 | R | N | EOM_VRANGE_SETTING[0] | |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | VEO[8] | VEO MSB value |
| | 0 | 0 | R | N | HEO[8] | HEO MSB value |
| 2A | 7 | 0 | RW | Y | EOM_TIMER_THR[3] | The value of EOM_TIMER_THR[7:4] controls the amount of time the Eye Monitor samples each point in the eye. (Refer to the Programming Guide for more details) |
| | 6 | 1 | RW | Y | EOM_TIMER_THR[2] | |
| | 5 | 0 | RW | Y | EOM_TIMER_THR[1] | |
| | 4 | 1 | RW | Y | EOM_TIMER_THR[0] | |
| | 3 | 1 | RW | Y | VEO_MIN_REQ_HITS[3] | Whenever the Eye Monitor is used to measure HEO and VEO, the data is sampled for some number of bits, set by Reg_0x2A[7:4]. This register sets the number of hits within that sample size that is required before the EOM will indicate a hit has occurred. This filtering only affects the VEO measurement. |
| | 2 | 0 | RW | Y | VEO_MIN_REQ_HITS[2] | |
| | 1 | 1 | RW | Y | VEO_MIN_REQ_HITS[1] | |
| | 0 | 0 | RW | Y | VEO_MIN_REQ_HITS[0] | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION | |
|---------------|------|---------------------|------|---------------------|----------------------|--|------------------------|
| 2B | 7 | 0 | RW | N | RESERVED | RESERVED | |
| | 6 | 0 | RW | N | RESERVED | RESERVED | |
| | 5 | 0 | RW | Y | RESERVED | RESERVED | |
| | 4 | 0 | RW | Y | RESERVED | RESERVED | |
| | 3 | 1 | RW | Y | EOM_MIN_REQ_HITS[3] | Whenever the Eye Monitor is used to measure HEO and VEO, the data is sampled for some number of bits, set by Reg_0x2A[7:4]. This register sets the number of hits within that sample size that is required before the EOM will indicate a hit has occurred. This filtering only affects the HEO measurement. | |
| | 2 | 0 | RW | Y | EOM_MIN_REQ_HITS[2] | | |
| | 1 | 1 | RW | Y | EOM_MIN_REQ_HITS[1] | | |
| 0 | 0 | RW | Y | EOM_MIN_REQ_HITS[0] | | | |
| 2C | 7 | 1 | RW | N | RELOAD_DFE_TAPS | Causes DFE taps to load from last adapted values | |
| | 6 | 1 | RW | Y | VEO_SCALE | 1: Normal operation. Scale VEO based on EOM vrange. | |
| | 5 | 1 | RW | Y | DFE_SM_FOM1 | This register defines the Figure of Merit used when adapting the DFE: 00: not valid 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO Additionally, if Reg_0x6E[6] is set to '1', the Alternate FOM is used. This bit takes precedence over DFE_SM_FOM | |
| | 4 | 1 | RW | Y | DFE_SM_FOM0 | | |
| | 3 | 0 | RW | Y | DFE_ADAPT_COUNTER[3] | | DFE look-beyond count. |
| | 2 | 1 | RW | Y | DFE_ADAPT_COUNTER[2] | | |
| | 1 | 1 | RW | Y | DFE_ADAPT_COUNTER[1] | | |
| | 0 | 0 | RW | Y | DFE_ADAPT_COUNTER[0] | | |
| 2D | 7 | 0 | RW | Y | RESERVED | RESERVED | |
| | 6 | 0 | RW | Y | RESERVED | RESERVED | |
| | 5 | 1 | RW | Y | RESERVED | RESERVED | |
| | 4 | 1 | RW | Y | RESERVED | RESERVED | |
| | 3 | 0 | RW | Y | REG_EQ_BST_OV | 1: Allow override control of the EQ setting by writing to Reg_0x03 0: Normal operation. | |
| | 2 | 0 | RW | Y | RESERVED | RESERVED | |
| | 1 | 0 | RW | Y | RESERVED | RESERVED | |
| | 0 | 0 | RW | Y | RESERVED | RESERVED | |
| 2E | 7 | 0 | RW | N | RESERVED | RESERVED | |
| | 6 | 0 | RW | N | RESERVED | RESERVED | |
| | 5 | 0 | R | N | EQ_BST3_BIT2_TO_EQ | Read-back of eq_BST3[2] driving the EQ | |
| | 4 | 0 | RW | N | RESERVED | RESERVED | |
| | 3 | 0 | RW | N | RESERVED | RESERVED | |
| | 2 | 0 | RW | N | PRBS_PATTERN_SEL[2] | MSB for the PRBS_PATTERN_SEL field. Lower bits are found on Reg_0x30[1:0]. Refer to the Reg_0x30 description on this table. | |
| | 1 | 0 | RW | N | RESERVED | RESERVED | |
| | 0 | 0 | RW | N | RESERVED | RESERVED | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|---------------------|--|
| 2F | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RATE[2] | Configure PPM register and divider for a standard data rate. (Refer to the Programming Guide for more details) |
| | 5 | 0 | RW | Y | RATE[1] | |
| | 4 | 1 | RW | Y | RATE[0] | |
| | 3 | 0 | RW | Y | INDEX_OV | If this bit is 1, then Reg_0x39 is to be used as 4-bit index to the [15:0] array of EQ settings. The EQ setting at that index is loaded to the EQ boost registers going to the analog and is used as the starting point for adaption. |
| | 2 | 1 | RW | Y | EN_PPM_CHECK | 1: (Default) Enable the PPM to be used as a qualifier when performing Lock Detect 0: Remove the PPM check as a lock qualifier. |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RWSC | N | CTLE_ADAPT | 1: Re-starts CTLE adaptation, self-clearing |
| 30 | 7 | 0 | RW | N | FREEZE_PPM_CNT | 1: Freeze the PPM counter to allow safe read asynchronously |
| | 6 | 0 | RW | Y | EQ_SEARCH_OV_EN | 1: Enables the EQ "search" bit to be forced by Reg_0x13[2] |
| | 5 | 0 | RW | N | EN_PATT_INV | 1: Enable automatic pattern inversion of successive 16 bit words when using the "Fixed Pattern" generator option. |
| | 4 | 0 | RW | N | RELOAD_PRBS_CHKR | 1: Force reload of seed into PRBS checker LFSR without holding the checker in reset. |
| | 3 | 0 | RW | N | PRBS_EN_DIG_CLK | This bit enables the clock to operate the PRBS generator and/or the PRBS checker. Toggling this bit is the primary method to reset the PRBS pattern generator and PRBS checker. |
| | 2 | 0 | RW | N | PRBS_PROGPATT_EN | Enable a fixed data pattern output. Requires that serializer is enabled with Reg_0x1E[4]. PRBS generator and checker should be disabled, Reg_0x30[3]. The fixed data pattern is set by Reg_0x7C and Reg_0x97. Enable inversion of the pattern every 16 bits with Reg_0x30[5]. |
| | 1 | 0 | RW | N | PRBS_PATTERN_SEL[1] | Selects the pattern output when using the PRBS generator. Requires the pattern generator to be configured properly. The MSB for the PRBS_PATTERN_SEL field is in Reg_0x2E[2]. Use Reg_0x30[3] to enable the PRBS generator. 000: 2 ⁷ -1 bits PRBS sequence 001: 2 ⁹ -1 bits PRBS sequence 010: 2 ¹¹ -1 bits PRBS sequence 011: 2 ¹⁵ -1 bits PRBS sequence 100: 2 ²³ -1 bits PRBS sequence 101: 2 ³¹ -1 bits PRBS sequence 110: 2 ⁵⁸ -1 bits PRBS sequence 111: 2 ⁶³ -1 bits PRBS sequence |
| | 0 | 0 | RW | N | PRBS_PATTERN_SEL[0] | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------|---|
| 31 | 7 | 0 | RW | N | PRBS_INT_EN | 1: Enables interrupt for detection of PRBS errors. The PRBS checker must be properly configured for this feature to work. |
| | 6 | 0 | RW | Y | ADAPT_MODE[1] | 00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal Note: for ADAPT_MODE=2 or 3, the DFE must be enabled by setting Reg_0x1E[3]=0 and Reg_0x1E[1]=1. (Refer to the Programming Guide for more details) |
| | 5 | 1 | RW | Y | ADAPT_MODE[0] | |
| | 4 | 0 | RW | Y | EQ_SM_FOM[1] | CTLE (EQ) adaption state machine figure of merit. 00: (Default) SM uses both HEO and VEO 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO Additionally, if Reg_0x6E[7]=1, the Alternate FOM is used. Reg_0x6E[7] takes precedence over EQ_SM_FOM. |
| | 3 | 0 | RW | Y | EQ_SM_FOM[0] | |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | CDR_LOCK_LOSS_INT_EN | Enable for CDR Lock Loss Interrupt. Observable in Reg_0x01[5] |
| | 0 | 0 | RW | Y | SIGNAL_DET_LOSS_INT_EN | Enable for Signal Detect Loss Interrupt. Observable in Reg_0x01[0] |
| 32 | 7 | 0 | RW | Y | HEO_INT_THRESH[3] | These bits set the threshold for the HEO and VEO interrupt. Each threshold bit represents 8 counts of HEO or VEO. |
| | 6 | 0 | RW | Y | HEO_INT_THRESH[2] | |
| | 5 | 0 | RW | Y | HEO_INT_THRESH[1] | |
| | 4 | 1 | RW | Y | HEO_INT_THRESH[0] | |
| | 3 | 0 | RW | Y | VEO_INT_THRESH[3] | |
| | 2 | 0 | RW | Y | VEO_INT_THRESH[2] | |
| | 1 | 0 | RW | Y | VEO_INT_THRESH[1] | |
| | 0 | 1 | RW | Y | VEO_INT_THRESH[0] | |
| 33 | 7 | 1 | RW | Y | HEO_THRESH[3] | In adapt mode 3, the register sets the minimum HEO and VEO required for CTLE adaption, before starting DFE adaption. This can be a max of 15. |
| | 6 | 0 | RW | Y | HEO_THRESH[2] | |
| | 5 | 0 | RW | Y | HEO_THRESH[1] | |
| | 4 | 0 | RW | Y | HEO_THRESH[0] | |
| | 3 | 1 | RW | Y | VEO_THRESH[3] | |
| | 2 | 0 | RW | Y | VEO_THRESH[2] | |
| | 1 | 0 | RW | Y | VEO_THRESH[1] | |
| | 0 | 0 | RW | Y | VEO_THRESH[0] | |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------|---|
| 34 | 7 | 0 | R | N | PPM_ERR_RDY | 1: Indicates that a PPM error count is read to be read from channel Reg_0x3B and Reg_0x3C |
| | 6 | 0 | RW | Y | LOW_POWER_MODE_DISABLE | By default, all blocks (except signal detect) power down after 100 ms after signal detect goes low. If set high, all blocks get powered on after the signal detect initially goes high. |
| | 5 | 1 | RW | Y | LOCK_COUNTER[1] | After achieving lock, the CDR continues to monitor the lock criteria. If the lock criteria fail, the lock is checked for a total of N number of times before declaring an out of lock condition, where N is set by this the value in these registers, with a max value of +3, for a total of 4. If during the N lock checks, lock is regained, then the lock condition is left HI, and the counter is reset back to zero. |
| | 4 | 1 | RW | Y | LOCK_COUNTER[0] | |
| | 3 | 1 | RW | Y | DFE_MAX_TAP2_5[3] | These four bits are used to set the maximum value by which DFE taps 2-5 are able to adapt with each subsequent adaptation. Same used for both polarities. |
| | 2 | 1 | RW | Y | DFE_MAX_TAP2_5[2] | |
| | 1 | 1 | RW | Y | DFE_MAX_TAP2_5[1] | |
| | 0 | 1 | RW | Y | DFE_MAX_TAP2_5[0] | |
| 35 | 7 | 0 | RW | Y | DATA_LOCK_PPM[1] | Modifies the value of the PPM delta tolerance from channel Reg_0x64: 00 - ppm_delta[7:0] = 1 x ppm_delta[7:0] 01 - ppm_delta[7:0] = 1 x ppm_delta[7:0] + ppm_delta[3:1] 10 - ppm_delta[7:0] = 2 x ppm_delta[7:0] 11 - ppm_delta[7:0] = 2 x ppm_delta[7:0] + ppm_delta[3:1] |
| | 6 | 0 | RW | Y | DATA_LOCK_PPM[0] | |
| | 5 | 0 | RW | N | GET_PPM_ERROR | Get PPM error from PPM_COUNT - clears when done. Normally updates continuously, but can be manually triggered with read value from Reg_0x3B and Reg_0x3C |
| | 4 | 0 | RW | Y | DFE_MAX_TAP1[4] | Limits DFE tap 1 maximum magnitude. |
| | 3 | 1 | RW | Y | DFE_MAX_TAP1[3] | |
| | 2 | 1 | RW | Y | DFE_MAX_TAP1[2] | |
| | 1 | 1 | RW | Y | DFE_MAX_TAP1[1] | |
| | 0 | 1 | RW | Y | DFE_MAX_TAP1[0] | |
| 36 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | Y | HEO_VEO_INT_EN | 1: Enable HEO/VEO interrupt capability |
| | 5 | 1 | RW | Y | REF_MODE[1] | 11: Normal Operation. Reference mode 3. |
| | 4 | 1 | RW | Y | REF_MODE[0] | |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 9. Channel Registers, 0 to 39 (continued)

| ADDRESS (HEX) | BITS | DEFAULT VALUE (HEX) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|----------------|--|
| 37 | 7 | 0 | R | N | CTLE_STATUS[7] | Feature is reserved for future use |
| | 6 | 0 | R | N | CTLE_STATUS[6] | |
| | 5 | 0 | R | N | CTLE_STATUS[5] | |
| | 4 | 0 | R | N | CTLE_STATUS[4] | |
| | 3 | 0 | R | N | CTLE_STATUS[3] | |
| | 2 | 0 | R | N | CTLE_STATUS[2] | |
| | 1 | 0 | R | N | CTLE_STATUS[1] | |
| | 0 | 0 | R | N | CTLE_STATUS[0] | |
| 38 | 7 | 0 | R | N | DFE_STATUS[7] | Feature is reserved for future use |
| | 6 | 0 | R | N | DFE_STATUS[6] | |
| | 5 | 0 | R | N | DFE_STATUS[5] | |
| | 4 | 0 | R | N | DFE_STATUS[4] | |
| | 3 | 0 | R | N | DFE_STATUS[3] | |
| | 2 | 0 | R | N | DFE_STATUS[2] | |
| | 1 | 0 | R | N | DFE_STATUS[1] | |
| | 0 | 0 | R | N | DFE_STATUS[0] | |
| 39 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | MR_EOM_RATE[1] | With eom_ov = 1, these bits control the Eye Monitor Rate: 11: Use for full rate, fastest 10: Use for 1/2 Rate All other values are reserved |
| | 5 | 1 | RW | Y | MR_EOM_RATE[0] | |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | START_INDEX[3] | Start index for EQ adaptation |
| | 2 | 0 | RW | Y | START_INDEX[2] | |
| | 1 | 0 | RW | Y | START_INDEX[1] | |
| | 0 | 0 | RW | Y | START_INDEX[0] | |

Table 10. Channel Registers, 3A to A9

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------|---|
| 3A | 7 | 0 | RW | Y | FIXED_EQ_BST0[1] | During adaptation, if the divider setting is >2, then a fixed EQ setting from this register will be used. However, if channel Reg_0x6F[7] is enabled, then an EQ adaptation will be performed instead |
| | 6 | 0 | RW | Y | FIXED_EQ_BST0[0] | |
| | 5 | 0 | RW | Y | FIXED_EQ_BST1[1] | |
| | 4 | 0 | RW | Y | FIXED_EQ_BST1[0] | |
| | 3 | 0 | RW | Y | FIXED_EQ_BST2[1] | |
| | 2 | 0 | RW | Y | FIXED_EQ_BST2[0] | |
| | 1 | 0 | RW | Y | FIXED_EQ_BST3[1] | |
| | 0 | 0 | RW | Y | FIXED_EQ_BST3[0] | |
| 3B | 7 | 0 | R | N | PPM_COUNT[15] | PPM count MSB |
| | 6 | 0 | R | N | PPM_COUNT[14] | |
| | 5 | 0 | R | N | PPM_COUNT[13] | |
| | 4 | 0 | R | N | PPM_COUNT[12] | |
| | 3 | 0 | R | N | PPM_COUNT[11] | |
| | 2 | 0 | R | N | PPM_COUNT[10] | |
| | 1 | 0 | R | N | PPM_COUNT[9] | |
| | 0 | 0 | R | N | PPM_COUNT[8] | |
| 3C | 7 | 0 | R | N | PPM_COUNT[7] | PPM count LSB |
| | 6 | 0 | R | N | PPM_COUNT[6] | |
| | 5 | 0 | R | N | PPM_COUNT[5] | |
| | 4 | 0 | R | N | PPM_COUNT[4] | |
| | 3 | 0 | R | N | PPM_COUNT[3] | |
| | 2 | 0 | R | N | PPM_COUNT[2] | |
| | 1 | 0 | R | N | PPM_COUNT[1] | |
| | 0 | 0 | R | N | PPM_COUNT[0] | |
| 3D | 7 | 0 | RW | Y | EN_FIR_CURSOR | 1: Enable Pre- and Post-cursor FIR 0: Disable Pre- and Post-cursor FIR (lower power) |
| | 6 | 0 | RW | Y | FIR_C0_SGN | Main-cursor sign bit 0: positive 1: negative |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | FIR_C0[4] | Main-cursor magnitude (Refer to the Programming Guide for more details) |
| | 3 | 1 | RW | Y | FIR_C0[3] | |
| | 2 | 0 | RW | Y | FIR_C0[2] | |
| | 1 | 1 | RW | Y | FIR_C0[1] | |
| | 0 | 0 | RW | Y | FIR_C0[0] | |
| 3E | 7 | 0 | RW | Y | FIR_PD_TX | |
| | 6 | 1 | RW | Y | FIR_CN1_SGN | Pre-cursor sign bit 1: negative 0: positive |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | FIR_CN1[3] | Pre-cursor magnitude (Refer to the Programming Guide for more details) |
| | 2 | 0 | RW | Y | FIR_CN1[2] | |
| | 1 | 0 | RW | Y | FIR_CN1[1] | |
| | 0 | 0 | RW | Y | FIR_CN1[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--------------------------|--|
| 3F | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | FIR_CP1_SGN | Post-cursor sign bit 1: negative 0: positive |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | FIR_CP1[3] | Post-cursor magnitude (Refer to the Programming Guide for more details) |
| | 2 | 0 | RW | Y | FIR_CP1[2] | |
| | 1 | 0 | RW | Y | FIR_CP1[1] | |
| | 0 | 0 | RW | Y | FIR_CP1[0] | |
| 40 | 7 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST0[1] | |
| | 6 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_0_BST3[0] | |
| 41 | 7 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_1_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_1_BST3[0] | |
| 42 | 7 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_2_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_2_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_2_BST3[0] | |
| 43 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_3_BST0[1] | |
| | 6 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_3_BST3[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--------------------------|-------------|
| 44 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_4_BST0[1] | |
| | 6 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_4_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_4_BST3[0] | |
| 45 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_5_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_5_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_5_BST3[0] | |
| 46 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_6_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_6_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_6_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_6_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_6_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_6_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_6_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_6_BST3[0] | |
| 47 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_7_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_7_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_7_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_7_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_7_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_7_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_7_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_7_BST3[0] | |
| 48 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_8_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_8_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_8_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_8_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_8_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_8_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_8_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_8_BST3[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|---------------------------|-------------|
| 49 | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_9_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_9_BST0[0] | |
| | 5 | 0 | RW | Y | EQ_ARRAY_INDEX_9_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_9_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_9_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_9_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_9_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_9_BST3[0] | |
| 4A | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_10_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_10_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_10_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_10_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_10_BST2[1] | |
| | 2 | 0 | RW | Y | EQ_ARRAY_INDEX_10_BST2[0] | |
| | 1 | 1 | RW | Y | EQ_ARRAY_INDEX_10_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_10_BST3[0] | |
| 4B | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST1[0] | |
| | 3 | 0 | RW | Y | EQ_ARRAY_INDEX_11_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST2[0] | |
| | 1 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_11_BST3[0] | |
| 4C | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST2[0] | |
| | 1 | 0 | RW | Y | EQ_ARRAY_INDEX_12_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_12_BST3[0] | |
| 4D | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_13_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST2[0] | |
| | 1 | 1 | RW | Y | EQ_ARRAY_INDEX_13_BST3[1] | |
| | 0 | 0 | RW | Y | EQ_ARRAY_INDEX_13_BST3[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|---------------------------|-------------|
| 4E | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST1[1] | |
| | 4 | 0 | RW | Y | EQ_ARRAY_INDEX_14_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST2[0] | |
| | 1 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_14_BST3[0] | |
| 4F | 7 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST0[1] | |
| | 6 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST0[0] | |
| | 5 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST1[1] | |
| | 4 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST1[0] | |
| | 3 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST2[1] | |
| | 2 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST2[0] | |
| | 1 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST3[1] | |
| | 0 | 1 | RW | Y | EQ_ARRAY_INDEX_15_BST3[0] | |
| 50 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 51 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 52 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------|-------------|
| 53 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 54 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 55 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 56 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 57 | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------|-------------|
| 58 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 59 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 5A | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 5B | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 5C | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 1 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------|--|
| 5D | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 5E | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 5F | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 60 | 7 | 0 | RW | Y | GRP0_OV_CNT[7] | Group 0 count LSB |
| | 6 | 0 | RW | Y | GRP0_OV_CNT[6] | |
| | 5 | 0 | RW | Y | GRP0_OV_CNT[5] | |
| | 4 | 0 | RW | Y | GRP0_OV_CNT[4] | |
| | 3 | 0 | RW | Y | GRP0_OV_CNT[3] | |
| | 2 | 0 | RW | Y | GRP0_OV_CNT[2] | |
| | 1 | 0 | RW | Y | GRP0_OV_CNT[1] | |
| | 0 | 0 | RW | Y | GRP0_OV_CNT[0] | |
| 61 | 7 | 0 | RW | Y | CNT_DLTA_OV_0 | Override enable for group 0 manual data rate selection |
| | 6 | 0 | RW | Y | GRP0_OV_CNT[14] | Group 0 count MSB |
| | 5 | 0 | RW | Y | GRP0_OV_CNT[13] | |
| | 4 | 0 | RW | Y | GRP0_OV_CNT[12] | |
| | 3 | 0 | RW | Y | GRP0_OV_CNT[11] | |
| | 2 | 0 | RW | Y | GRP0_OV_CNT[10] | |
| | 1 | 0 | RW | Y | GRP0_OV_CNT[9] | |
| | 0 | 0 | RW | Y | GRP0_OV_CNT[8] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------|---|
| 62 | 7 | 0 | RW | Y | GRP1_OV_CNT[7] | Group 1 count LSB |
| | 6 | 0 | RW | Y | GRP1_OV_CNT[6] | |
| | 5 | 0 | RW | Y | GRP1_OV_CNT[5] | |
| | 4 | 0 | RW | Y | GRP1_OV_CNT[4] | |
| | 3 | 0 | RW | Y | GRP1_OV_CNT[3] | |
| | 2 | 0 | RW | Y | GRP1_OV_CNT[2] | |
| | 1 | 0 | RW | Y | GRP1_OV_CNT[1] | |
| | 0 | 0 | RW | Y | GRP1_OV_CNT[0] | |
| 63 | 7 | 0 | RW | Y | CNT_DLTA_OV_1 | Override enable for group 1 manual data rate selection |
| | 6 | 0 | RW | Y | GRP1_OV_CNT[14] | Group 1 count MSB |
| | 5 | 0 | RW | Y | GRP1_OV_CNT[13] | |
| | 4 | 0 | RW | Y | GRP1_OV_CNT[12] | |
| | 3 | 0 | RW | Y | GRP1_OV_CNT[11] | |
| | 2 | 0 | RW | Y | GRP1_OV_CNT[10] | |
| | 1 | 0 | RW | Y | GRP1_OV_CNT[9] | |
| | 0 | 0 | RW | Y | GRP1_OV_CNT[8] | |
| 64 | 7 | 0 | RW | Y | GRP0_OV_DLTA[3] | Sets the PPM delta tolerance for the PPM counter lock check for group 0. Must also program channel Reg_0x67[7]. |
| | 6 | 0 | RW | Y | GRP0_OV_DLTA[2] | |
| | 5 | 0 | RW | Y | GRP0_OV_DLTA[1] | |
| | 4 | 0 | RW | Y | GRP0_OV_DLTA[0] | |
| | 3 | 0 | RW | Y | GRP1_OV_DLTA[3] | Sets the PPM delta tolerance for the PPM counter lock check for group 1. Must also program channel Reg_0x67[6]. |
| | 2 | 0 | RW | Y | GRP1_OV_DLTA[2] | |
| | 1 | 0 | RW | Y | GRP1_OV_DLTA[1] | |
| | 0 | 0 | RW | Y | GRP1_OV_DLTA[0] | |
| 65 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 66 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------|--|
| 67 | 7 | 0 | RW | Y | GRP0_OV_DLTA[4] | |
| | 6 | 0 | RW | Y | GRP1_OV_DLTA[4] | |
| | 5 | 1 | RW | Y | HV_LOCKMON_EN | 1: Enable periodic monitoring of HEO/VEO for lock qualification. 0: Disable periodic HEO/VEO monitoring for lock qualification. |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 68 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 69 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 6A | 7 | 0 | RW | Y | VEO_LCK_THRSH[3] | VEO threshold to meet before lock is established. The LSB step size is 4 counts of VEO. |
| | 6 | 0 | RW | Y | VEO_LCK_THRSH[2] | |
| | 5 | 1 | RW | Y | VEO_LCK_THRSH[1] | |
| | 4 | 0 | RW | Y | VEO_LCK_THRSH[0] | |
| | 3 | 0 | RW | Y | HEO_LCK_THRSH[3] | HEO threshold to meet before lock is established. The LSB step size is 4 counts of HEO. |
| | 2 | 0 | RW | Y | HEO_LCK_THRSH[2] | |
| | 1 | 0 | RW | Y | HEO_LCK_THRSH[1] | |
| | 0 | 1 | RW | Y | HEO_LCK_THRSH[0] | |
| 6B | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | FOM_A[6] | Alternate Figure of Merit variable A. Max value for this register is 128. |
| | 5 | 0 | RW | Y | FOM_A[5] | |
| | 4 | 0 | RW | Y | FOM_A[4] | |
| | 3 | 0 | RW | Y | FOM_A[3] | |
| | 2 | 0 | RW | Y | FOM_A[2] | |
| | 1 | 0 | RW | Y | FOM_A[1] | |
| | 0 | 0 | RW | Y | FOM_A[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|----------------|--|
| 6C | 7 | 0 | RW | Y | FOM_B[7] | HEO adjustment for Alternate FoM, variable B |
| | 6 | 0 | RW | Y | FOM_B[6] | |
| | 5 | 0 | RW | Y | FOM_B[5] | |
| | 4 | 0 | RW | Y | FOM_B[4] | |
| | 3 | 0 | RW | Y | FOM_B[3] | |
| | 2 | 0 | RW | Y | FOM_B[2] | |
| | 1 | 0 | RW | Y | FOM_B[1] | |
| | 0 | 0 | RW | Y | FOM_B[0] | |
| 6D | 7 | 0 | RW | Y | FOM_C[7] | VEO adjustment for Alternate FoM, variable C |
| | 6 | 0 | RW | Y | FOM_C[6] | |
| | 5 | 0 | RW | Y | FOM_C[5] | |
| | 4 | 0 | RW | Y | FOM_C[4] | |
| | 3 | 0 | RW | Y | FOM_C[3] | |
| | 2 | 0 | RW | Y | FOM_C[2] | |
| | 1 | 0 | RW | Y | FOM_C[1] | |
| | 0 | 0 | RW | Y | FOM_C[0] | |
| 6E | 7 | 0 | RW | Y | EN_NEW_FOM_CTL | 1: CTLE adaption state machine will use the alternate FoM $HEO_ALT = (HEO-B)*A*2VEO_ALT = (VEO-C)*(1-A)*2$ The values of A,B,C are set in channel Reg_0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128. The Alternate FoM = $(HEOB)*A*2 + (VEO-C)*(1-A)*2$ |
| | 6 | 0 | RW | Y | EN_NEW_FOM_DFE | 1: DFE adaption state machine will use the alternate FoM. $HEO_ALT = (HEO-B)*A*2VEO_ALT = (VEO-C)*(1-A)*2$ The values of A,B,C are set in channel Reg_0x6B, 0x6C, and 0x6D. The value of A is equal to the register value divided by 128. The Alternate FoM = $(HEOB)*A*2 + (VEO-C)*(1-A)*2$ |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|----------------|---------------------|--|
| 6F | 7 | 0 | RW | Y | MR_EN_LOW_DIVSEL_EQ | Normally, during adaptation, if the divider setting is >2, then a fixed EQ setting, from Reg_0x3A will be used. However, if Reg_0x6F[7]=1, then an EQ adaptation will be performed instead. |
| | 6 | 0 | RW | Y | RESERVED | RESERVED |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 70 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | EQ_LB_CNT[3] | CTLE look-beyond count for adaptation |
| | 2 | 1 | RW | Y | EQ_LB_CNT[2] | |
| | 1 | 0 | RW | Y | EQ_LB_CNT[1] | |
| 0 | 1 | RW | Y | EQ_LB_CNT[0] | | |
| 71 | 7 | 0 | R | N | PRBS_INT | When enabled by Reg_0x31[7], goes HI if a PRBS stream is detected. Clears on reading. PRBS checker must be enabled with Reg_0x30[3]. Once cleared, if a PRBS error occurs, then the interrupt will again go HI. Clears on reading. If signal detect is lost, this is considered a PRBS error, and the interrupt will go HI. Clears on reading. |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | DFE_POL_1_OBS | DFE tap 1 polarity observation |
| | 4 | 0 | R | N | DFE_WT1_OBS[4] | DFE tap 1 weight observation |
| | 3 | 0 | R | N | DFE_WT1_OBS[3] | |
| | 2 | 0 | R | N | DFE_WT1_OBS[2] | |
| | 1 | 0 | R | N | DFE_WT1_OBS[1] | |
| | 0 | 0 | R | N | DFE_WT1_OBS[0] | |
| 72 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | DFE_POL_2_OBS | Primary observation point for DFE tap 2 polarity |
| | 3 | 0 | R | N | DFE_WT2_OBS[3] | Primary observation point for DFE tap 2 weight |
| | 2 | 0 | R | N | DFE_WT2_OBS[2] | |
| | 1 | 0 | R | N | DFE_WT2_OBS[1] | |
| 0 | 0 | R | N | DFE_WT2_OBS[0] | | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|----------------------|--|
| 73 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | DFE_POL_3_OBS | Primary observation point for DFE tap 3 polarity |
| | 3 | 0 | R | N | DFE_WT3_OBS[3] | Primary observation point for DFE tap 3 weight |
| | 2 | 0 | R | N | DFE_WT3_OBS[2] | |
| | 1 | 0 | R | N | DFE_WT3_OBS[1] | |
| | 0 | 0 | R | N | DFE_WT3_OBS[0] | |
| 74 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | DFE_POL_4_OBS | Primary observation point for DFE tap 4 polarity |
| | 3 | 0 | R | N | DFE_WT4_OBS[3] | Primary observation point for DFE tap 4 weight |
| | 2 | 0 | R | N | DFE_WT4_OBS[2] | |
| | 1 | 0 | R | N | DFE_WT4_OBS[1] | |
| | 0 | 0 | R | N | DFE_WT4_OBS[0] | |
| 75 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | DFE_POL_5_OBS | Primary observation point for DFE tap 5 polarity |
| | 3 | 0 | R | N | DFE_WT5_OBS[3] | Primary observation point for DFE tap 5 weight |
| | 2 | 0 | R | N | DFE_WT5_OBS[2] | |
| | 1 | 0 | R | N | DFE_WT5_OBS[1] | |
| | 0 | 0 | R | N | DFE_WT5_OBS[0] | |
| 76 | 7 | 0 | RW | Y | POST_LOCK_VEO_THR[3] | VEO threshold after LOCK is established |
| | 6 | 0 | RW | Y | POST_LOCK_VEO_THR[2] | |
| | 5 | 1 | RW | Y | POST_LOCK_VEO_THR[1] | |
| | 4 | 0 | RW | Y | POST_LOCK_VEO_THR[0] | |
| | 3 | 0 | RW | Y | POST_LOCK_HEO_THR[3] | HEO threshold after LOCK is established |
| | 2 | 0 | RW | Y | POST_LOCK_HEO_THR[2] | |
| | 1 | 0 | RW | Y | POST_LOCK_HEO_THR[1] | |
| | 0 | 1 | RW | Y | POST_LOCK_HEO_THR[0] | |
| 77 | 7 | 0 | RW | N | PRBS_GEN_POL_EN | 1: Force polarity inversion on generated PRBS data |
| | 6 | 0 | RW | Y | RESERVED | RESERVED |
| | 5 | 0 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------|--|
| 78 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | SD_STATUS | Primary observation point for signal detect status |
| | 4 | 0 | R | N | CDR_LOCK_STATUS | Primary observation point for CDR lock status |
| | 3 | 0 | R | N | CDR_LOCK_INT | Requires that channel Reg_0x79[1] be set. 1: Indicates CDR has achieved lock, lock goes from LOW to HIGH. This bit is cleared after reading. This bit will stay set until it has been cleared by reading. |
| | 2 | 0 | R | N | SD_INT | Requires that channel Reg_0x79[0] be set. 1: Indicates signal detect status has changed. This will trigger when signal detect goes from LOW to HIGH or HIGH to LOW. This bit is cleared after reading. This bit will stay set until it has been cleared by reading. |
| | 1 | 0 | R | N | EOM_VRANGE_LIMIT_ERROR | Goes high if GET_HEO_VEO indicates high during adaptation |
| | 0 | 0 | R | N | HEO_VEO_INT | Requires that channel Reg_0x36[6] be set. 1: Indicates that HEO/VEO dropped below the limits set in channel Reg_0x76 This bit is cleared after reading. This bit will stay set until it has been cleared by reading. |
| 79 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | PRBS_CHK_EN | 1: Enable the PRBS checker. 0: Disable the PRBS checker |
| | 5 | 0 | RW | N | PRBS_GEN_EN | 1: Enable the pattern generator 0: Disable the pattern generator |
| | 4 | 1 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | CDR_LOCK_INT_EN | 1: Enable CDR lock interrupt, observable in channel Reg_0x78[3] 0: Disable CDR lock interrupt |
| | 0 | 0 | RW | Y | SD_INT_EN | 1: Enable signal detect interrupt, observable in channel Reg_0x78[3] 0: Disable signal detect interrupt |
| 7A | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------------------|---|
| 7B | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 7C | 7 | 0 | R | N | PRBS_FIXED[7] | Pattern generator user defined pattern LSB. MSB located at channel Reg_0x97. |
| | 6 | 0 | R | N | PRBS_FIXED[6] | |
| | 5 | 0 | R | N | PRBS_FIXED[5] | |
| | 4 | 0 | R | N | PRBS_FIXED[4] | |
| | 3 | 0 | R | N | PRBS_FIXED[3] | |
| | 2 | 0 | R | N | PRBS_FIXED[2] | |
| | 1 | 0 | R | N | PRBS_FIXED[1] | |
| | 0 | 0 | R | N | PRBS_FIXED[0] | |
| 7D | 7 | 0 | RW | Y | CONT_ADAPT_HEO_CHNG_THRS[3] | Limit for HEO change before triggering a DFE adaption while continuous DFE adaption is enabled. |
| | 6 | 1 | RW | Y | CONT_ADAPT_HEO_CHNG_THRS[2] | |
| | 5 | 0 | RW | Y | CONT_ADAPT_HEO_CHNG_THRS[1] | |
| | 4 | 0 | RW | Y | CONT_ADAPT_HEO_CHNG_THRS[0] | |
| | 3 | 1 | RW | Y | CONT_ADAPT_VEO_CHNG_THRS[3] | Limit for VEO change before triggering a DFE adaption while continuous DFE adaption is enabled. (Refer to the Programming Guide for more details) |
| | 2 | 0 | RW | Y | CONT_ADAPT_VEO_CHNG_THRS[2] | |
| | 1 | 0 | RW | Y | CONT_ADAPT_VEO_CHNG_THRS[1] | |
| | 0 | 0 | RW | Y | CONT_ADAPT_VEO_CHNG_THRS[0] | |
| 7E | 7 | 0 | RW | Y | CONT_ADPT_TAP_INCR[3] | Limit for allowable tap increase from the previous base point |
| | 6 | 0 | RW | Y | CONT_ADPT_TAP_INCR[2] | |
| | 5 | 0 | RW | Y | CONT_ADPT_TAP_INCR[1] | |
| | 4 | 1 | RW | Y | CONT_ADPT_TAP_INCR[0] | |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--------------------|---|
| 7F | 7 | 0 | RW | N | EN_OBS_ALT_FOM | 1: Allows for alternate FoM calculation to be shown in channel registers Reg_0x27, Reg_0x28 and Reg_0x29 instead of HEO and VEO |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | EN_DFE_CONT_ADAPT | 1: Continuous DFE adaption is enabled 0: DFE adapts only during lock and then freezes (Refer to the Programming Guide for more details) |
| | 3 | 1 | RW | Y | CONT_ADPT_CMP_BOTH | 1: If continuous DFE adaption is enabled, a DFE adaption will trigger if either HEO or VEO degrades |
| | 2 | 0 | RW | Y | CONT_ADPT_COUNT[2] | Limit for number of weights the DFE can look ahead in continuous adaption. (Refer to the Programming Guide for more details) |
| | 1 | 1 | RW | Y | CONT_ADPT_COUNT[1] | |
| | 0 | 0 | RW | Y | CONT_ADPT_COUNT[0] | |
| 80 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 81 | 7 | 1 | R | N | RESERVED | RESERVED |
| | 6 | 1 | R | N | RESERVED | RESERVED |
| | 5 | 1 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 1 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------|--|
| 82 | 7 | 0 | RW | N | FREEZE_PRBS_CNTR | 1: Freeze the PRBS error count to allow for readback. 0: Normal operation. Error counters is allowed to increment if the PRBS checker is properly configured |
| | 6 | 0 | RW | N | RST_PRBS_CNTR | 1: Reset the PRBS error counter. 0: Normal operation. Error counter is released from reset. |
| | 5 | 0 | RW | N | PRBS_PATT_OV | 1: Override PRBS pattern auto-detection. Forces the pattern checker to only lock onto the pattern defined in Reg_0x82[4:2]. 0: Normal operation. Pattern checker will automatically detect the PRBS pattern |
| | 4 | 0 | RW | N | PRBS_PATT[2] | Used with the PRBS checker. Usage is enabled with Reg_0x82[5]. Select PRBS pattern to be checked: 000 - PRBS7 001 - PRBS9 010 - PRBS11 011 - PRBS15 100 - PRBS23 101 - PRBS31 110 - PRBS58 111 - PRBS63 |
| | 3 | 0 | RW | N | PRBS_PATT[1] | |
| | 2 | 0 | RW | N | PRBS_PATT[0] | |
| | 1 | 0 | RW | N | PRBS_POL_OV | 1: Override PRBS pattern auto polarity detection. Forces the pattern checker to only lock onto the polarity defined in bit 0 of this register. 0: Normal operation, pattern checker will automatically detect the PRBS pattern polarity |
| | 0 | 0 | RW | N | PRBS_POL | Usage is enabled with Reg_0x82[1]=1 0: Forced polarity = true 1: Forced polarity = inverted |
| 83 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | PRBS_ERR_CNT[10] | PRBS checker error count |
| | 1 | 0 | R | N | PRBS_ERR_CNT[9] | |
| | 0 | 0 | R | N | PRBS_ERR_CNT[8] | |
| 84 | 7 | 0 | R | N | PRBS_ERR_CNT[7] | PRBS checker error count |
| | 6 | 0 | R | N | PRBS_ERR_CNT[6] | |
| | 5 | 0 | R | N | PRBS_ERR_CNT[5] | |
| | 4 | 0 | R | N | PRBS_ERR_CNT[4] | |
| | 3 | 0 | R | N | PRBS_ERR_CNT[3] | |
| | 2 | 0 | R | N | PRBS_ERR_CNT[2] | |
| | 1 | 0 | R | N | PRBS_ERR_CNT[1] | |
| | 0 | 0 | R | N | PRBS_ERR_CNT[0] | |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------|-------------|
| 85 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 86 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 87 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 88 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 89 | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|--------------|---|
| 8A | 7 | 0 | R | N | RESERVED | RESERVED |
| | 6 | 0 | R | N | RESERVED | RESERVED |
| | 5 | 0 | R | N | RESERVED | RESERVED |
| | 4 | 0 | R | N | RESERVED | RESERVED |
| | 3 | 0 | R | N | RESERVED | RESERVED |
| | 2 | 0 | R | N | RESERVED | RESERVED |
| | 1 | 0 | R | N | RESERVED | RESERVED |
| | 0 | 0 | R | N | RESERVED | RESERVED |
| 8B | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 8C | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 8D | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 1 | RW | N | RESERVED | RESERVED |
| | 1 | 1 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 8E | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | VGA_SEL_GAIN | VGA selection bit : 1: VGA high-gain mode 0: VGA low-gain mode (Refer to the Programming Guide for more details) |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|-----------------|--|
| 8F | 7 | 0 | R | N | EQ_BST_TO_EQ[7] | Primary observation point for the EQ boost setting. |
| | 6 | 0 | R | N | EQ_BST_TO_EQ[6] | |
| | 5 | 0 | R | N | EQ_BST_TO_EQ[5] | |
| | 4 | 0 | R | N | EQ_BST_TO_EQ[4] | |
| | 3 | 0 | R | N | EQ_BST_TO_EQ[3] | |
| | 2 | 0 | R | N | EQ_BST_TO_EQ[2] | |
| | 1 | 0 | R | N | EQ_BST_TO_EQ[1] | |
| | 0 | 0 | R | N | EQ_BST_TO_EQ[0] | |
| 90 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 91 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 92 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 93 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 94 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| 95 | 7 | 0 | RW | N | SD_ENABLE | 1: Force enable signal detect 0: Normal operation |
| | 6 | 0 | RW | N | SD_DISABLE | 1: Force disable signal detect 0: Normal operation |
| | 5 | 0 | RW | N | DC_OFF_ENABLE | 1: Force enable DC offset compensation 0: Normal operation |
| | 4 | 0 | RW | N | DC_OFF_DISABLE | 1: Force disable DC offset compensation 0: Normal operation |
| | 3 | 1 | RW | N | EQ_ENABLE | 1: Force enable the CTLE 0: Normal operation |
| | 2 | 0 | RW | N | EQ_DISABLE | 1: Force disable the CTLE 0: Normal operation |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|----------------|--|
| 96 | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 0 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 97 | 7 | 0 | R | N | PRBS_FIXED[15] | Pattern generator user defined pattern MSB. LSB located at channel Reg_0x7C. |
| | 6 | 0 | R | N | PRBS_FIXED[14] | |
| | 5 | 0 | R | N | PRBS_FIXED[13] | |
| | 4 | 0 | R | N | PRBS_FIXED[12] | |
| | 3 | 0 | R | N | PRBS_FIXED[11] | |
| | 2 | 0 | R | N | PRBS_FIXED[10] | |
| | 1 | 0 | R | N | PRBS_FIXED[9] | |
| | 0 | 0 | R | N | PRBS_FIXED[8] | |
| 98 | 7:6 | 0 | RW | N | RESERVED | RESERVED |
| | 5:0 | 0 | RW | Y | RESERVED | RESERVED |
| 99 | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 0 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |
| 9A | 7 | 0 | RW | Y | RESERVED | RESERVED |
| | 6 | 0 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 1 | RW | Y | RESERVED | RESERVED |
| | 3 | 1 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 1 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | Y | RESERVED | RESERVED |
| 9B | 7 | 1 | RW | Y | RESERVED | RESERVED |
| | 6 | 1 | RW | Y | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 0 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|------------------------|---|
| 9C | 7 | 0 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | Y | RESERVED | RESERVED |
| | 4 | 0 | RW | Y | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 0 | RW | Y | RESERVED | RESERVED |
| 9D | 7 | 1 | RW | N | RESERVED | RESERVED |
| | 6 | 0 | RW | N | RESERVED | RESERVED |
| | 5 | 1 | RW | N | RESERVED | RESERVED |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | Y | RESERVED | RESERVED |
| | 2 | 1 | RW | Y | RESERVED | RESERVED |
| | 1 | 0 | RW | Y | RESERVED | RESERVED |
| | 0 | 1 | RW | N | RESERVED | RESERVED |
| 9E | 7 | 0 | RW | Y | CP_EN_IDAC_PD[2] | Phase detector charge pump setting, when override is enabled. See reg_0C for other bits. |
| | 6 | 1 | RW | Y | CP_EN_IDAC_PD[1] | |
| | 5 | 0 | RW | Y | CP_EN_IDAC_PD[0] | |
| | 4 | 0 | RW | Y | CP_EN_IDAC_FD[2] | Frequency detector charge pump setting, when override is enabled. See reg_0C for other bits. |
| | 3 | 1 | RW | Y | CP_EN_IDAC_FD[1] | |
| | 2 | 0 | RW | Y | CP_EN_IDAC_FD[0] | |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |
| 9F | 7:0 | 0 | R | N | NOT USED | |
| A0 | 7:0 | 0 | R | N | NOT USED | |
| A1 | 7:0 | 0 | R | N | NOT USED | |
| A2 | 7:0 | 0 | R | N | NOT USED | |
| A3 | 7:0 | 0 | R | N | NOT USED | |
| A4 | 7:0 | 0 | R | N | NOT USED | |
| A5 | 7 | 0 | RW | Y | PFD_SEL_DATA_PSTLCK[2] | Output mode for when the CDR is in lock. For these values to take effect, Reg_0x09[5] must be set to 0, which is the default. 000: Raw Data 001: Retimed data (default) 100: PRBS Generator or Fixed Pattern Generator Data 101: 10M clock 111: Mute All other values are reserved. (Refer to the Programming Guide for more details) |
| | 6 | 0 | RW | Y | PFD_SEL_DATA_PSTLCK[1] | |
| | 5 | 1 | RW | Y | PFD_SEL_DATA_PSTLCK[0] | |
| | 4 | 0 | RW | N | RESERVED | RESERVED |
| | 3 | 0 | RW | N | RESERVED | RESERVED |
| | 2 | 0 | RW | N | RESERVED | RESERVED |
| | 1 | 0 | RW | N | RESERVED | RESERVED |
| | 0 | 0 | RW | N | RESERVED | RESERVED |

Table 10. Channel Registers, 3A to A9 (continued)

| ADDRESS (Hex) | BITS | DEFAULT VALUE (Hex) | MODE | EEPROM | FIELD NAME | DESCRIPTION |
|---------------|------|---------------------|------|--------|---------------------|--|
| A6 | 7 | 0 | RW | N | INCR_HIST_TMR | Provides an option to increase EOM timer given by 0x2A[7:4] for histogram collection by +8 for selection values < 8 |
| | 6 | 1 | RW | Y | EOM_TMR_ABRT_ON_HIT | Enables faster scan through the eye-matrix by moving on to the next matrix point as soon as hit is observed Note: This bit does not affect when slope measurement are in progress |
| | 5 | 0 | RW | Y | SLP_MIN_REQ_HITS[1] | Minimum required hit count for registering a hit during slope measurements. |
| | 4 | 0 | RW | Y | SLP_MIN_REQ_HITS[0] | |
| | 3 | 0 | RW | Y | LFT_SLP | 0: allows slope measurement for the right side of the eye 1: allows slope measurement for the left side of the eye |
| | 2 | 0 | RW | Y | TOP_SLP | 0: allows slope measurement for the bottom side of the eye 1: allows slope measurement for the top side of the eye |
| | 1 | 1 | RW | Y | DFE_BATHTUB_FOM | Enables slope-based bathtub FoM for DFE adaptation |
| | 0 | 1 | RW | Y | CTLE_BATHTUB_FOM | Enables slope-based bathtub FoM for CTLE adaptation |
| A7 | 7:0 | 0 | R | N | RESERVED | RESERVED |
| A8 | 7:0 | 0 | RW | N | RESERVED | RESERVED |
| A9 | 7:0 | 0 | RW | Y | RESERVED | RESERVED |

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

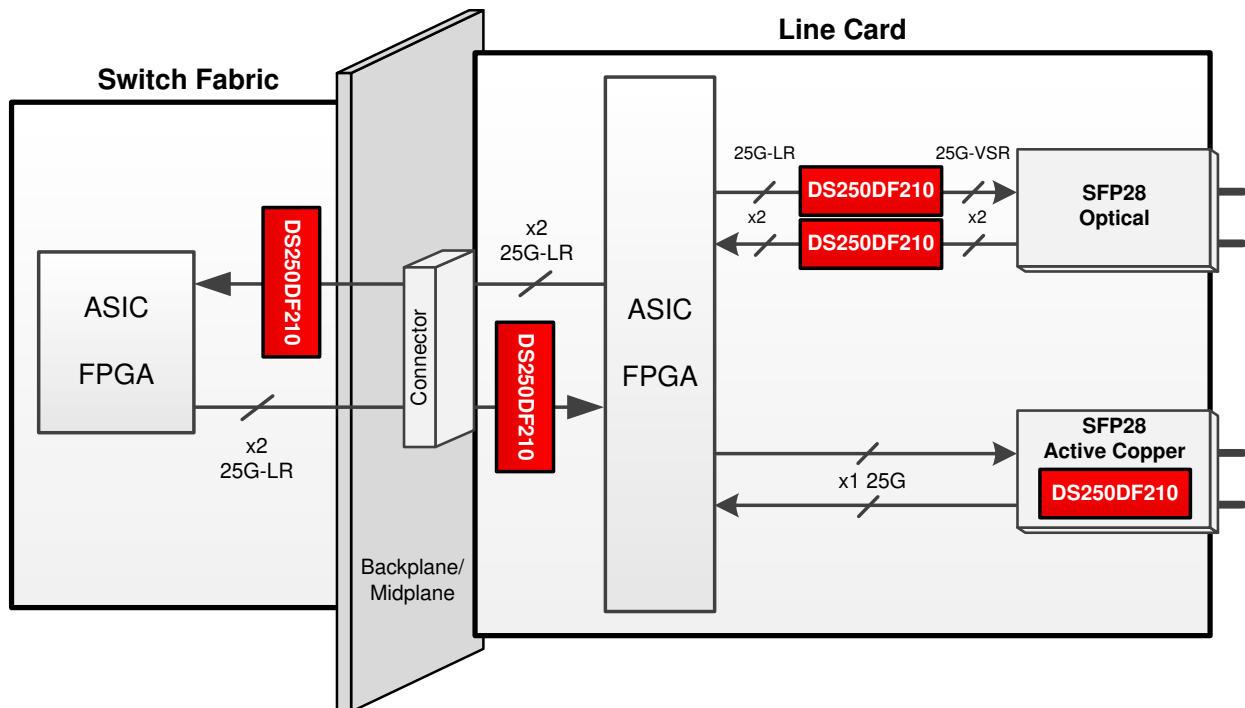
9.1 Application Information

The DS250DF210 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

9.2 Typical Applications

The DS250DF210 is typically used in the following application scenarios:

1. [Front-Port Jitter Cleaning Applications](#)
2. [Active Cable Applications](#)
3. [Backplane and Mid-Plane Applications](#)



☒ 15. Typical Uses for the DS250DF210 in a System

Typical Applications (continued)

9.2.1 Front-Port Jitter Cleaning Applications

The DS250DF210 has strong equalization capabilities that allow it to equalize insertion loss, reduce jitter, and extend the reach of front-port interfaces. A single DS250DF210 can be used to support the egress and ingress channel of a 25GbE port. Similarly, two DS250DF210 devices can be used to support a 50GbE (2x25G) port, one DS250DF210 for the two egress channels and another DS250DF210 for the two ingress channels.

For applications which require IEEE802.3 100GBASE-CR4 or 25GBASE-CR auto-negotiation and link training, a linear repeater device such as the DS280BR810 (or similar) is recommended.

Figure 16 illustrates this configuration, and Figure 17 shows an example simplified schematic for a typical front-port application.

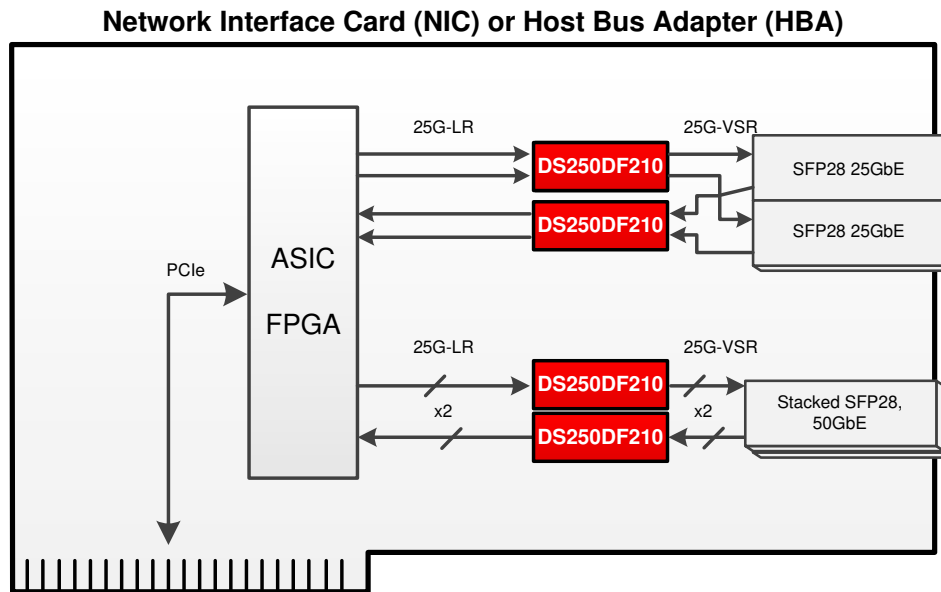
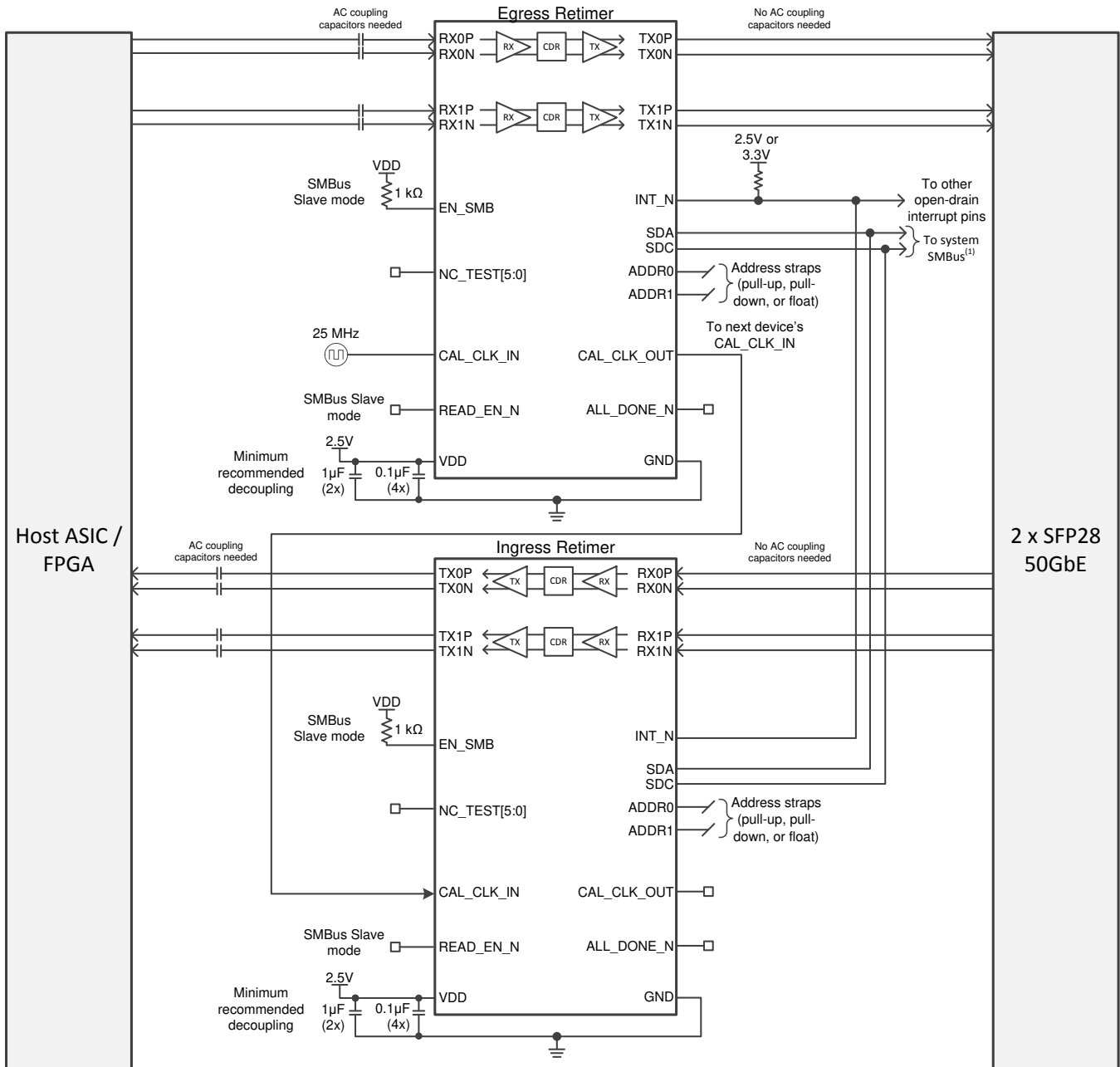


Figure 16. Front-Port Application Block Diagram

Typical Applications (continued)



(1) SMBus signals need to be pulled up elsewhere in the system.

17. Front-Port Application Schematic

Typical Applications (continued)

9.2.1.1 Design Requirements

For this design example, the following guidelines outlined in [表 11](#) apply.

表 11. Front-Port Application Design Guidelines

| DESIGN PARAMETER | REQUIREMENT |
|-------------------------------|--|
| AC-coupling capacitors | <i>Egress (ASIC-to-module) direction:</i> AC-coupling capacitors in the range of 100 to 220 nF are required for the RX inputs and are NOT required for the TX outputs. <i>Ingress (module-to-ASIC) direction:</i> AC-coupling capacitors in the range of 100 to 220 nF are required for the TX outputs and are NOT required for the RX inputs. |
| Input channel insertion loss | ≤ 35 dB at 25.78125 Gbps Nyquist frequency (12.9 GHz) |
| Output channel insertion loss | <i>Egress (ASIC-to-module) direction:</i> Follow CAUI-4 / CEI-25G-VSR host channel requirements (approximately 7dB at 12.9 GHz). <i>Ingress (module-to-ASIC) direction:</i> Depends on downstream ASIC / FPGA capabilities. The DS250DF210 has a low-jitter output driver with 3-tap FIR filter for equalizing a portion of the output channel. |
| Host ASIC TX launch amplitude | 800 mVppd to 1200 mVppd. |
| Host ASIC TX FIR filter | Depends on channel loss. Refer to Setting the Output V_{OD}, Precursor, and Postcursor Equalization . |

9.2.1.2 Detailed Design Procedure



The design procedure for front-port applications is as follows:

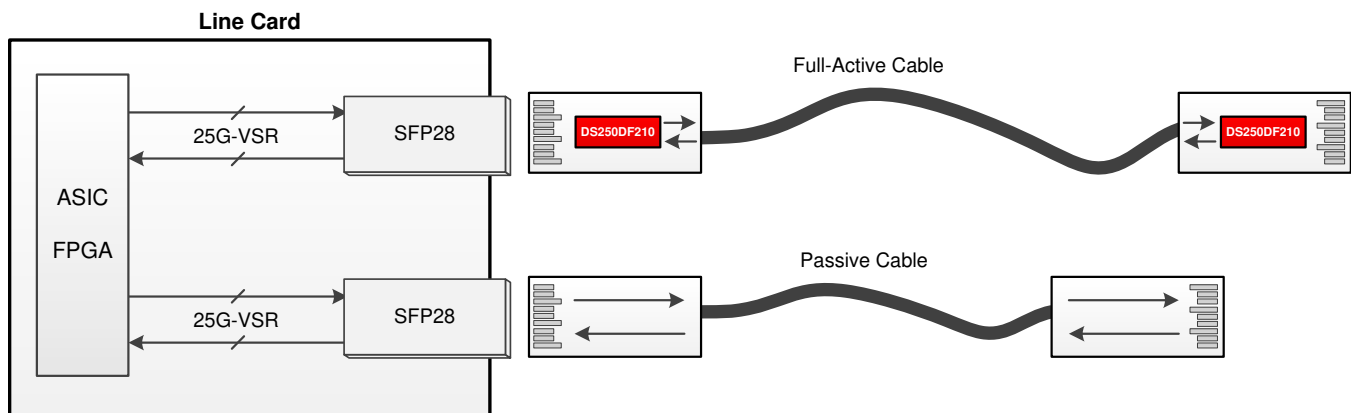
- Determine the total number of channels on the board which require a DS250DF210 for signal conditioning. This dictates the total number of DS250DF210 devices required for the board. TI recommends that channels connected to the same front-port cage be grouped together in the same DS250DF210 device. This simplifies the device settings, as similar loss channels generally utilize similar settings.
- Determine the maximum current draw required for all DS250DF210 retimers. This may impact the selection of the regulator for the 2.5-V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS250DF210 devices.
- Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
 - Maximum mission-mode operational power consumption is when all channels are locked and re-transmitting the data which is received. PRBS pattern checkers/generators are not used in this mode because normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS250DF210 devices.
 - Maximum debug-mode operational power consumption is when all channels are locked and re-transmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS250DF210 devices.
- Determine the SMBus address scheme needed to uniquely address each DS250DF210 device on the board, depending on the total number of devices identified in step 2. Each DS250DF210 can be strapped with one of 16 unique SMBus addresses. If there are more DS250DF210 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I2C expander like the **TCA/PCA family of I2C/SMBus switches and multiplexers** to split up the SMBus into multiple busses.
- Determine if the device is configured from EEPROM (SMBus Master Mode) or from the system I2C bus (SMBus Slave Mode).
 - If SMBus Master Mode is used, provisions must be made for an EEPROM on the board with 8-bit SMBus address 0xA0. Refer to [SMBus Master Mode](#) for more details on SMBus Master Mode including EEPROM size requirements.
 - If SMBus Slave Mode is used for all device configurations, an EEPROM is not needed.

6. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in [Pin Configuration and Functions](#) for more details.
7. Make provisions in the schematic and layout for a 25 MHz (± 100 ppm) single-ended CMOS clock. Each DS250DF210 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) retimers' calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5-V CMOS output, then no AC-coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one retimer's CAL_CLK_OUT output and the next retimer's CAL_CLK_IN input. The final retimer's CAL_CLK_OUT output can be left floating.
8. Connect the INT_N open-drain output to an FPGA or CPU if interrupt monitoring is desired. Note that multiple retimers' INT_N outputs can be connected together because this is an open-drain output. The common INT_N net must be pulled high.
9. If the application requires initial CDR lock acquisition at the ambient temperature extremes defined in [Recommended Operating Conditions](#), take care to ensure the operating junction temperature is met as well as the CDR stay-in-lock ambient temperature range defined in [Timing Requirements, Retimer Jitter Specifications](#). For example, if initial CDR lock acquisition occurs at an ambient temperature of 85°C, then maintaining CDR lock would require the ambient temperature surrounding the DS250DF210 to be kept above (85°C – TEMP_{LOCK-}).

9.2.2 Active Cable Applications

The DS250DF210 has strong equalization capabilities that allow it to recover data over long or thin-gauge copper cables. A single DS250DF210 can be used on a SFP28 paddle card to create a full-active cable assembly which is longer or thinner than passive cables.

 18 illustrates this configuration,  19 shows an example simplified schematic for a full-active cable application.



 18. Active Cable Application Block Diagram

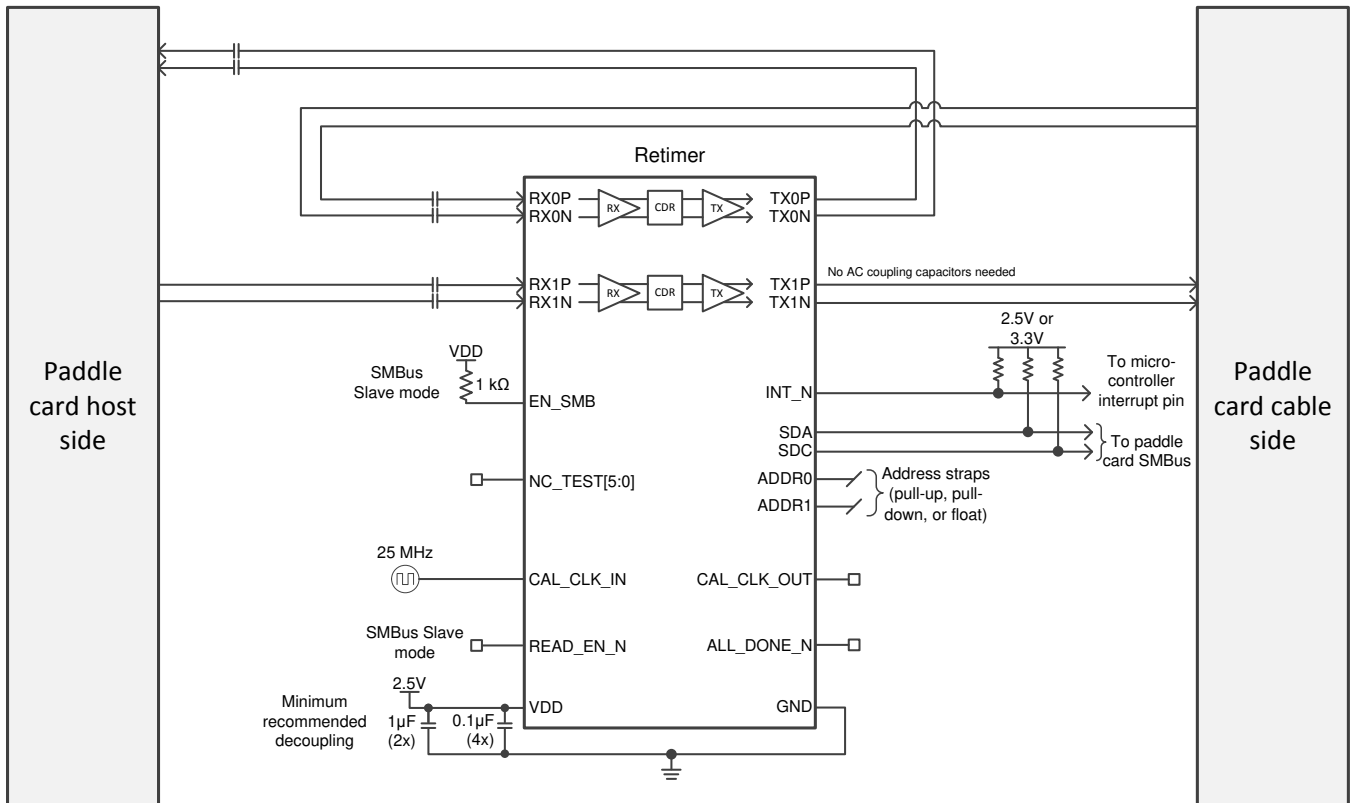


图 19. Full-Active Cable Application Schematic

9.2.2.1 Design Requirements

For this design example, the following guidelines outlined in 表 12 apply.

表 12. Full-Active Cable Application Design Guidelines

| DESIGN PARAMETER | REQUIREMENT |
|------------------------|---|
| Device placement | A full-active QSFP cable uses DS250DF210 per paddle card. |
| AC-coupling capacitors | <i>Transmit data direction (that is, data coming from the host system and towards the cable):</i> 100-nF AC-coupling capacitors are required for the RX inputs and are not required for the TX outputs. This link segment is AC-coupled on the paddle card at the opposite end of the cable. <i>Receive data direction (that is, data coming from the cable and towards the host system):</i> 100-nF AC-coupling capacitors are required for the RX inputs and the TX outputs. |
| Cable insertion loss | The raw cable insertion loss including the insertion loss of the paddle card must be ≤ 35 dB at 25.78125-Gbps Nyquist frequency (12.9 GHz). |

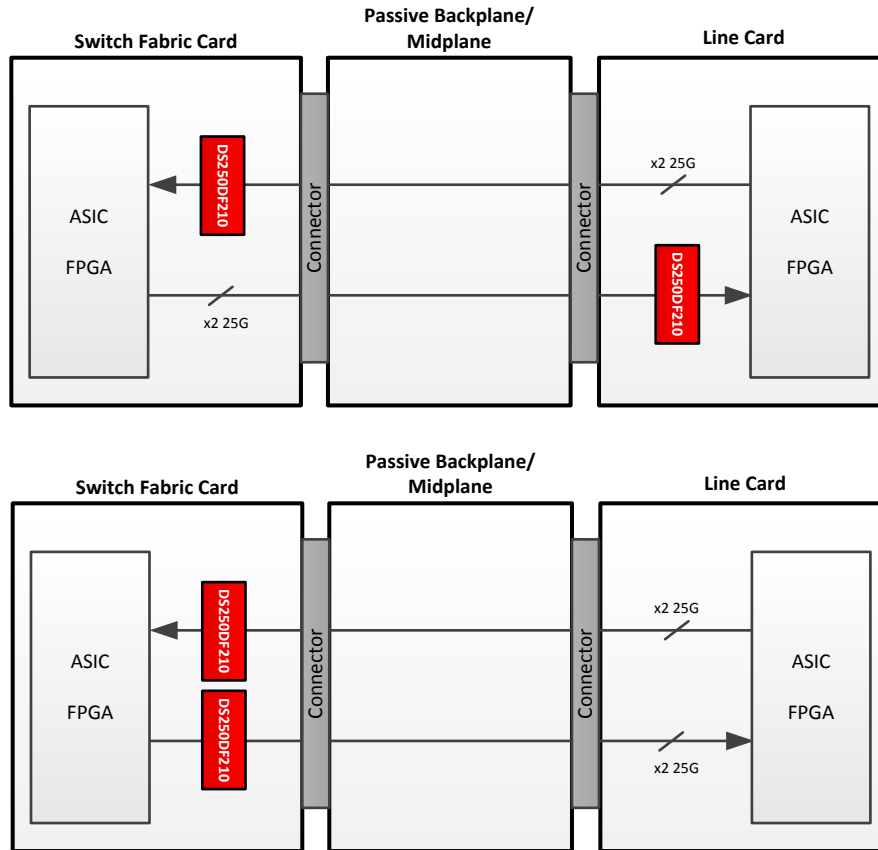
9.2.2.2 Detailed Design Procedure

The design procedure for active cable applications is as follows:

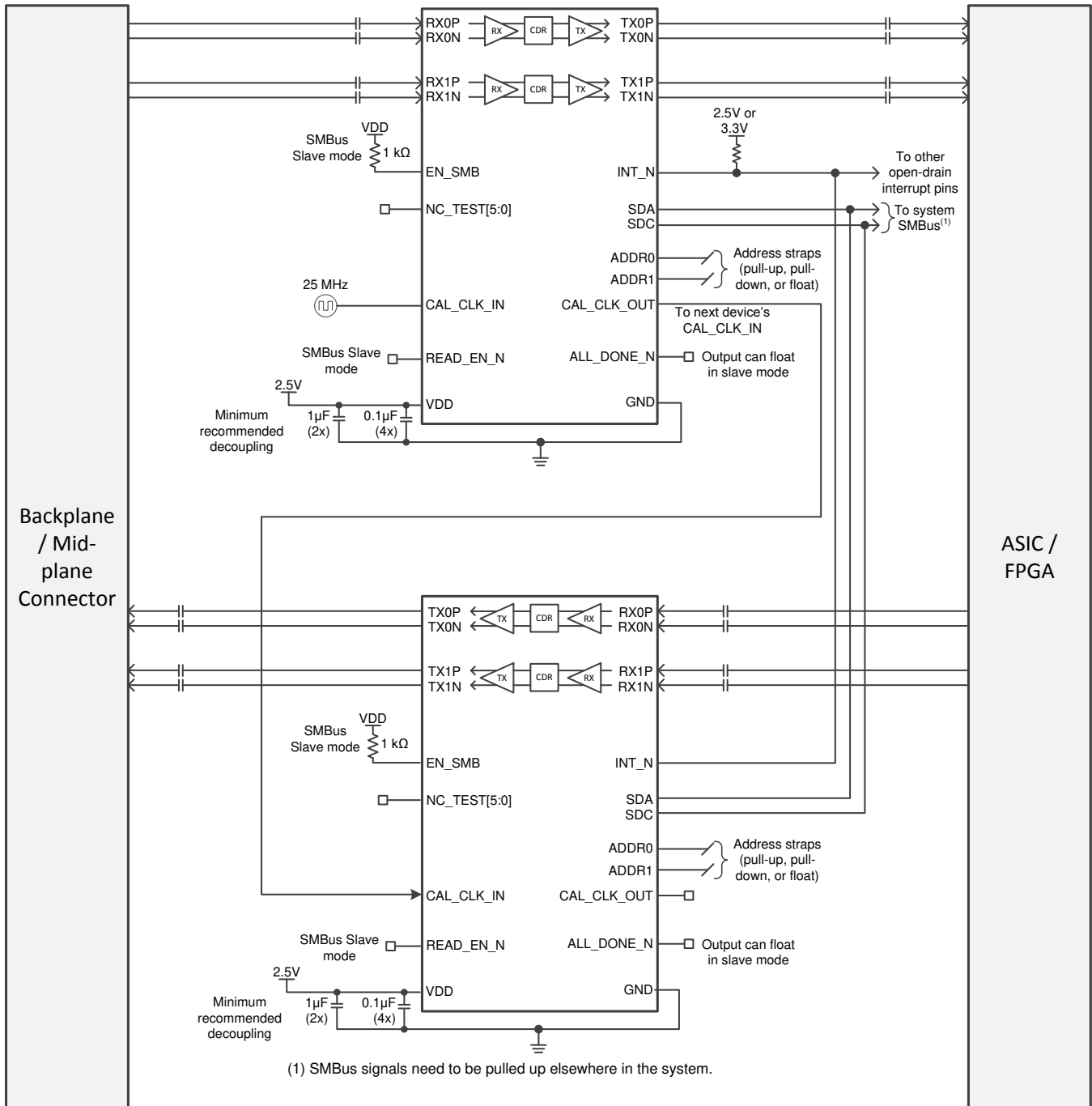
1. Determine the maximum current draw required for the DS250DF210 retimer(s) on the paddle card. This may impact the selection of the regulator for the 2.5-V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS250DF210 devices.
2. Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
 - a. Maximum mission-mode operational power consumption is when all channels are locked and re-transmitting the data which is received. PRBS pattern checkers/generators are not used in this mode because normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS250DF210 devices.
 - b. Maximum debug-mode operational power consumption is when all channels are locked and re-transmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS250DF210 devices.
3. Determine the SMBus address for the DS250DF210 Retimer(s). If using just one Retimer for a full-active cable, the ADDR[1:0] pins can be left floating for an 8-bit SMBus slave address of 0x44.
4. Determine if the device is configured from EEPROM (SMBus Master Mode) or from the system I2C bus (SMBus Slave Mode).
 - a. If SMBus Master Mode is used, provisions must be made for an EEPROM on the board with 8-bit SMBus address 0xA0. Refer to [SMBus Master Mode](#) for more details on SMBus Master Mode including EEPROM size requirements.
 - b. If SMBus Slave Mode is used for all device configurations, for example when the Retimer(s) is configured with a microcontroller, an EEPROM is not needed.
5. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in [Pin Configuration and Functions](#) for more details.
6. Make provisions in the schematic and layout for a 25 MHz (± 100 ppm) single-ended CMOS clock. The DS250DF210 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. When using two Retimers on a paddle card, only one 25 MHz clock is required. The CAL_CLK_OUT pin of one retimer can be connected to the CAL_CLK_IN pin of the other retimer.
7. Connect the INT_N open-drain output to the paddle card MCU if interrupt monitoring is desired, otherwise leave it floating. The INT_N net must be pulled high.
8. If the application requires initial CDR lock acquisition at the ambient temperature extremes defined in [Recommended Operating Conditions](#), take care to ensure the operating junction temperature is met as well as the CDR stay-in-lock ambient temperature range defined in [Timing Requirements, Retimer Jitter Specifications](#). For example, if initial CDR lock acquisition occurs at an ambient temperature of 85°C, then maintaining CDR lock would require the ambient temperature surrounding the DS250DF210 to be kept above $(85^{\circ}\text{C} - \text{TEMP}_{\text{LOCK-}})$.

9.2.3 Backplane and Mid-Plane Applications

The DS250DF210 has strong equalization capabilities that allow it to recover data over channels up to 35 dB insertion loss. As a result, the optimum placement for the DS250DF210 in a backplane/mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS250DF210 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.



⊗ 20. Backplane/Mid-Plane Application Block Diagram
(Top: Recommended Placement; Bottom: Placement With Both Retimers on the Same board)



21. Backplane/Mid-Plane Application Schematic

9.2.4 Design Requirements

For this design example, the following guidelines outlined in [表 13](#) apply.

表 13. Backplane/Mid-Plane Application Design Guidelines

| DESIGN PARAMETER | REQUIREMENT |
|----------------------------------|---|
| AC-coupling capacitors | AC-coupling capacitors in the range of 100 to 220 nF are required for the RX inputs and TX outputs |
| Input channel insertion loss | ≤ 35 dB at 25.78125 Gbps Nyquist frequency |
| Output channel insertion loss | Depends on downstream ASIC / FPGA capabilities. The DS250DF210 has a low-jitter output driver with 3-tap FIR filter for equalizing a portion of the output channel. |
| Link partner TX launch amplitude | 800 mVppd to 1200 mVppd |
| Link partner TX FIR filter | Depends on channel loss |

9.2.5 Detailed Design Procedure

The design procedure for backplane/mid-plane applications is as follows:

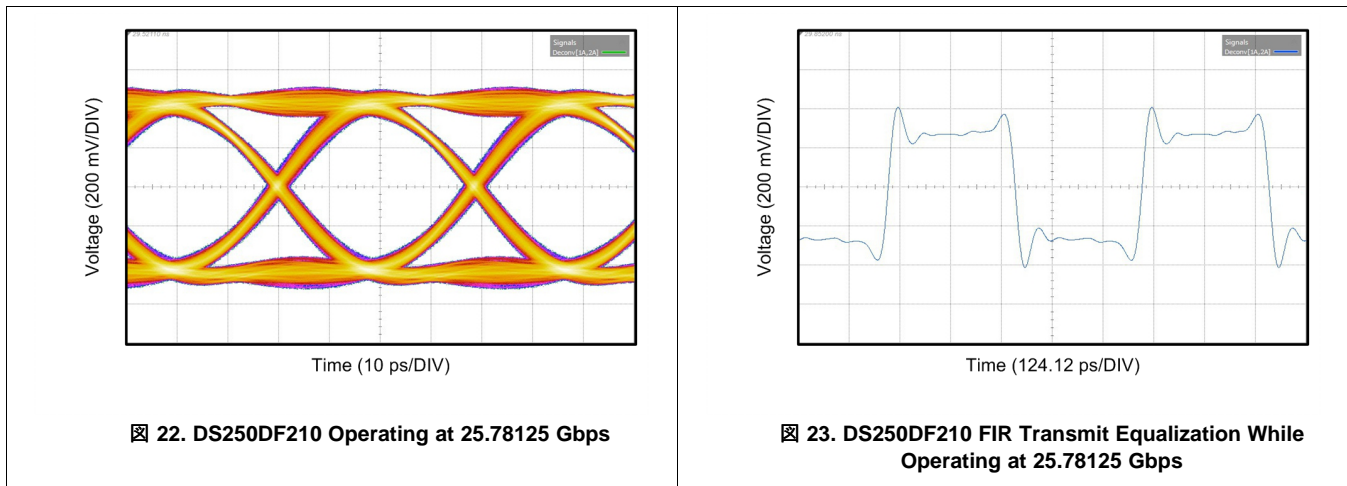
- Determine the total number of channels on the board which require a DS250DF210 for signal conditioning. This dictates the total number of DS250DF210 devices required for the board. TI recommends that channels with similar total insertion loss on the board be grouped together in the same DS250DF210 device. This simplifies the device settings, as similar loss channels generally utilize similar settings.
- Determine the maximum current draw required for all DS250DF210 retimers. This may impact the selection of the regulator for the 2.5 V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS250DF210 devices.
- Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
 - Maximum mission-mode operational power consumption is when all channels are locked and retransmitting the data which is received. PRBS pattern checkers/generators are not used in this mode because normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS250DF210 devices.
 - Maximum debug-mode operational power consumption is when all channels are locked and retransmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS250DF210 devices.
- Determine the SMBus address scheme needed to uniquely address each DS250DF210 device on the board, depending on the total number of devices identified in step 2. Each DS250DF210 can be strapped with one of 16 unique SMBus addresses. If there are more DS250DF210 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I2C expander like the **TCA/PCA family of I2C/SMBus switches and multiplexers** to split up the SMBus into multiple busses.
- Determine if the device is configured from EEPROM (SMBus Master Mode) or from the system I2C bus (SMBus Slave Mode).
 - If SMBus Master Mode is used, provisions must be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
 - If SMBus Slave Mode is used for all device configurations, an EEPROM is not needed.
- Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in [Pin Configuration and Functions](#) for more details.
- Make provisions in the schematic and layout for a 25MHz (±100 ppm) single-ended CMOS clock. Each DS250DF210 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) retimers' calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5 V CMOS output, then no AC-coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one retimer's CAL_CLK_OUT output and the next retimer's CAL_CLK_IN input. The final retimer's CAL_CLK_OUT output can be left floating.

8. Connect the INT_N open-drain output to an FPGA or CPU if interrupt monitoring is desired. Note that multiple retimers' INT_N outputs can be connected together because this is an open-drain output. The common INT_N net must be pulled high.
9. If the application requires initial CDR lock acquisition at the ambient temperature extremes defined in *Recommended Operating Conditions*, take care to ensure the operating junction temperature is met as well as the CDR stay-in-lock ambient temperature range defined in *Timing Requirements, Retimer Jitter Specifications*. For example, if initial CDR lock acquisition occurs at an ambient temperature of 85°C, then maintaining CDR lock would require the ambient temperature surrounding the DS250DF210 to be kept above (85°C – TEMP_{LOCK-}).

9.2.6 Application Curves

☒ 22 shows a typical output eye diagram for the DS250DF210 operating at 25.78125 Gbps with PRBS9 pattern using FIR main-cursor of +18, precursor of -1 and postcursor of +2. All other device settings are left at default.

☒ 23 shows an example of DS250DF210 FIR transmit equalization while operating at 25.78125 Gbps. In this example, the Tx FIR filter main-cursor is set to +15, postcursor to -3 and precursor to -3. An 8T pattern is used to evaluate the FIR filter, which consists of 0xFF00. All other device settings are left at default.



10 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the recommended operating conditions outlined in [Specifications](#) in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the DS250DF210 is provided in [Specifications](#). This figure can be used to calculate the maximum current the power supply must provide. Typical mission-mode current draw can be inferred from the typical power consumption in [Specifications](#).
3. The DS250DF210 does not require any special power supply filtering (that is, ferrite bead), provided the recommended operating conditions are met. Only standard supply decoupling is required. Refer to [Pin Configuration and Functions](#) for details concerning the recommended supply decoupling.

11 Layout

11.1 Layout Guidelines

Follow these guidelines when designing the layout:

1. Decoupling capacitors must be placed as close to the VDD pins as possible. Placing them directly underneath the device is one option if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN must be tightly coupled, skew matched, and impedance controlled.
3. Vias must be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers, or by back drilling.
4. GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND relief can be used beneath the AC-coupling capacitor pads to improve signal integrity by counteracting the pad capacitance.
6. GND vias must be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
7. BGA landing pads for a 0.5-mm pitch flip-chip BGA are typically 0.3 mm in diameter (exposed). The actual size of the copper pad depends on whether solder-mask-defined (SMD) or non-solder-mask-defined solder land pads are used. For more information, refer to TI's Surface Mount Technology (SMT) and Packaging application notes on the TI website.
8. If vias are used for the high-speed signals, ground via must be implemented adjacent to the signal via to provide return path and isolation. For differential pair, the typical via configuration is *ground-signal-signal-ground*.
9. Note that some BGA balls in the DS250DF210 pinout have been de-populated to allow for GND and VDD vias to be placed with ≥ 1.0 mm via-to-via spacing.

11.2 Layout Example

The following example layout demonstrates how all signals can be escaped from the BGA array using stripline routing on a generic 28-layer stackup. This example layout assumes the following:

- Trace width: 0.159 mm (6.25 mil)
- Trace edge-to-edge spacing: 0.197 mm (7.75 mil)
- VIA-to-VIA spacing: 0.7 mm (27.9 mil) minimum; Note: 1.0 mm VIA-to-VIA spacing is also achievable if PCB manufacturing rules stipulate
- No VIA-in-pad used

注

Some TI test pins (that is, NC_TEST[5:0]) are routed in this example layout, but in most applications these pins can be left floating.

Layout Example (continued)

Many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing depend on the PCB material, PCB routing density, and other factors.

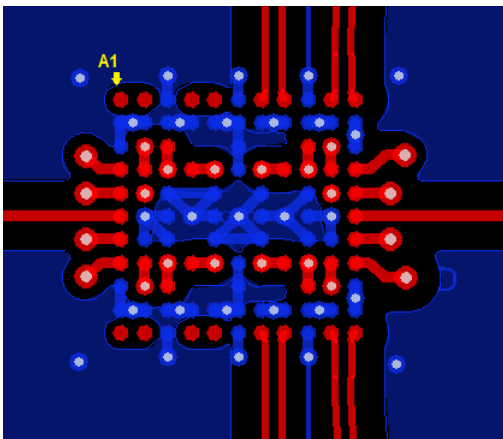


图 24. Top Layer (Pin A1 is Top-Left)

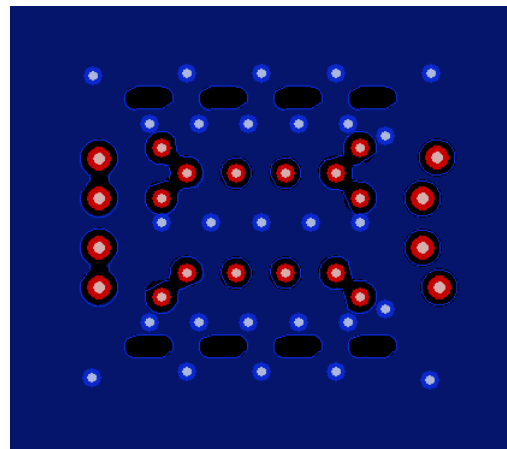


图 25. Layer 1 GND (Pin A1 is Top-Left)

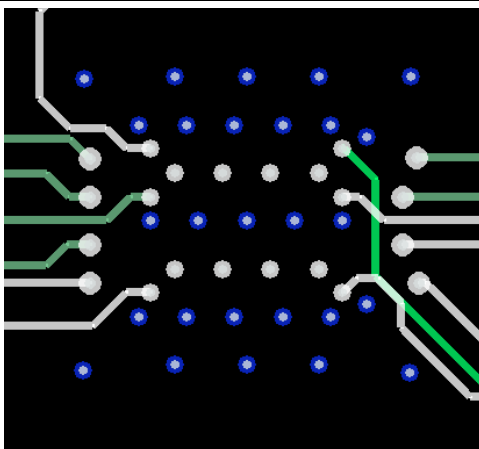


图 26. Internal Low-Speed Signal Layers (Pin A1 is Top-Left)

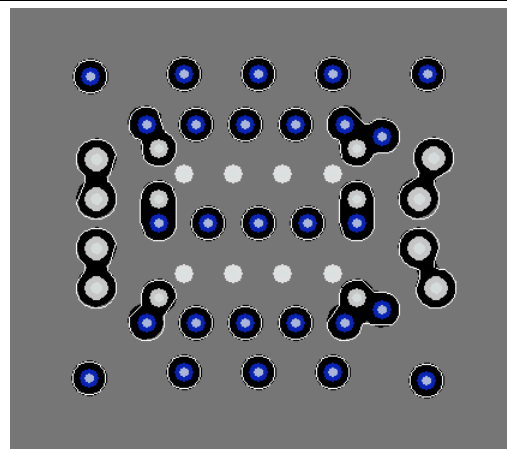


图 27. VDD Layer (Pin A1 is Top-Left)

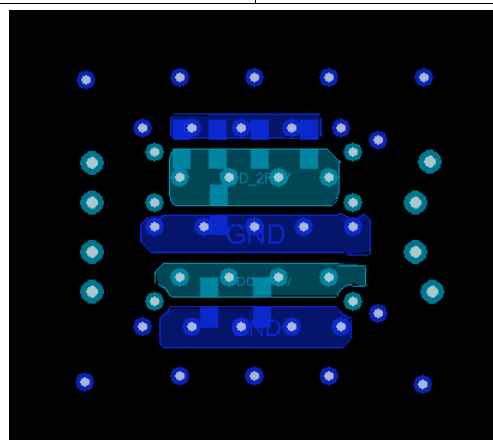


图 28. Bottom Layer (Pin A1 is Top-Left)

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

詳細情報については、TIの表面実装テクノロジー(SMT)リファレンスを参照してください。

<http://focus.ti.com/quality/docs>(「品質および鉛(Pb)フリーのデータ」メニューの下)

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『DS2x0DF810、DS250DFx10、DS250DF230プログラマ・ガイド』(SNLU182)

DS250DF210 MySecure フォルダ内で『DS2X0DFX10 IBIS-AMI Model and Programming Guide』(英語)へのアクセスを請求するには、[ここをクリック](#)してください。

12.3 ドキュメントの更新通知を受け取る方法

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12.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS250DF210ABMR | ACTIVE | FCCSP | ABM | 101 | 1000 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DS250DF2 | Samples |
| DS250DF210ABMT | ACTIVE | FCCSP | ABM | 101 | 250 | RoHS & Green | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DS250DF2 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS250DF210ABMR | FCCSP | ABM | 101 | 1000 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q1 |
| DS250DF210ABMT | FCCSP | ABM | 101 | 250 | 178.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

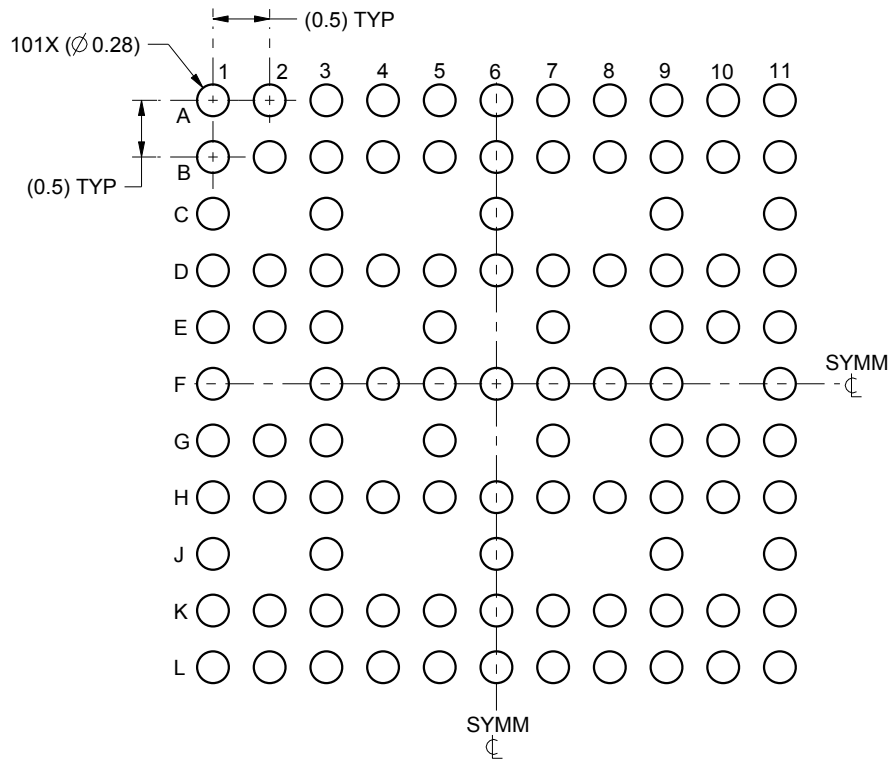
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS250DF210ABMR | FCCSP | ABM | 101 | 1000 | 356.0 | 356.0 | 36.0 |
| DS250DF210ABMT | FCCSP | ABM | 101 | 250 | 208.0 | 191.0 | 35.0 |

EXAMPLE BOARD LAYOUT

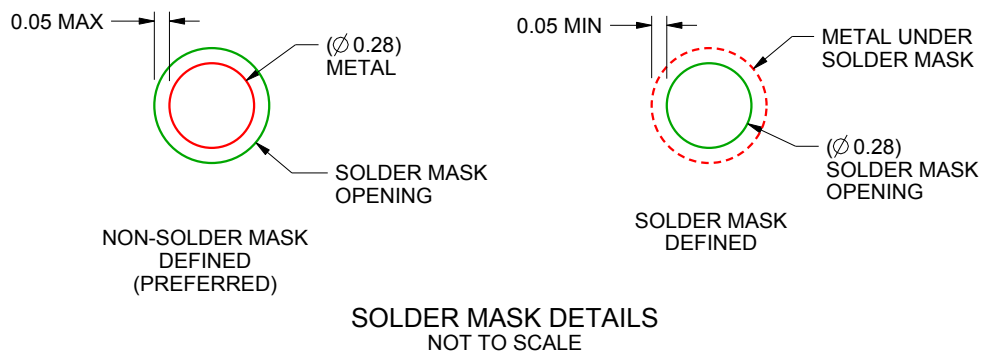
ABM0101A

FCBGA - 1.03 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

4222100/B 09/2015

NOTES: (continued)

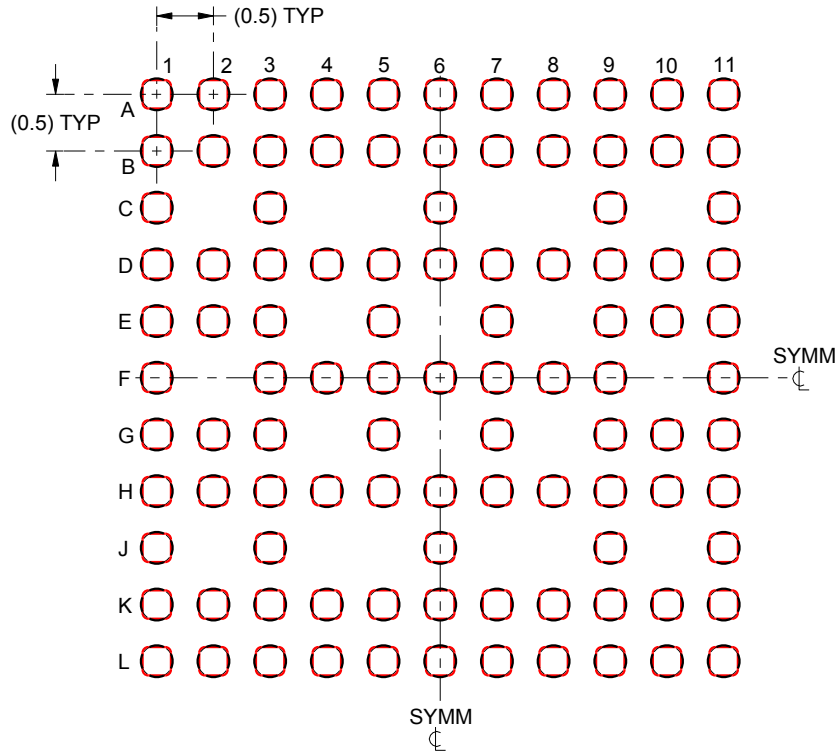
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

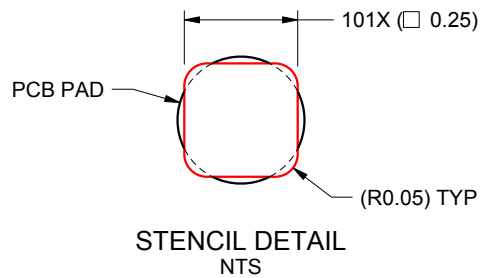
ABM0101A

FCBGA - 1.03 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 15X



4222100/B 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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