DS90LV028AQ-Q1 車載用 LVDS デュアル差動ライン・レシーバ

1 特長

- 車載アプリケーション用に AECQ-100 認定済み
  - 温度グレード 1：-40°C～+125°C、T_A
- 400Mbps (200MHz) を超えるスイッチング速度
- 差動スキュー：50ps (標準値)
- チャネル間スキュー：0.1ns (標準値)
- 最大伝搬遅延：2.5ns
- 3.3V 電源の設計
- フロースルーのピン配置
- パワーダウン時高インピーダンスのLVDS入力
- 低消費電力の設計(3.3V 静的で 18mW)
- LVDS 入力は LVDS/CML/LVPECL 信号に対応
- ANSI/TIA/EIA-644 規格に準拠
- SOIC パッケージで供給

2 アプリケーション

- LVDS-LVCMOS 間の変換
- インフォテインメントおよびクラスタ
- 車載用ヘッド・ユニット

3 概要

DS90LV028AQ はデュアル CMOS 差動ライン・レシーバで、超低消費電力、低ノイズ、高いデータ速度を必要とするアプリケーション用に設計されています。このデバイスは、低電圧差動信号 (LVDS) テクノロジを活用し、400Mbps (200MHz) を超えるデータ速度をサポートするよう設計されています。

DS90LV028AQ は低電圧 (標準値 350mV) の差動入力信号を受信し、3V CMOS 出力レベルへ変換します。DS90LV028AQ にはフロースルー設計が採用されているため、PCB レイアウトが容易です。

DS90LV028AQ と、対になる LVDS ライン・ドライバ DS90LV027AQ は、消費電力の大きい PECL/ECL デバイスの新しい代替品として、高速のポイント・ツー・ポイント・インターフェイス・アプリケーションに使用できます。

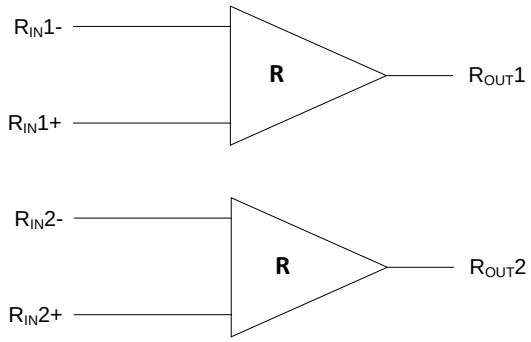
製品情報(1)

型番	パッケージ	本体サイズ(公称)
DS90LV028AQ	SOIC (D 8)	4.90mm × 3.91mm
	WSON (DQF 8)(2)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) 製品プレビュー

機能図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (November 2018) から Revision H に変更 **Page**

- Deleted the Thermal Pad from the DQF package ... 3
- Changed V_{CC} 0.3 To: V_{CC} + 0.3 in the *Absolute Maximum Ratings* table ... 4
- Added NOTE: "These parameters are specified by design." ... 5

Revision F (August 2018) から Revision G に変更 **Page**

- Changed the Pin image views ... 3
- Changed the Pin Descriptions format ... 3

Revision E (April 2013) から Revision F に変更 **Page**

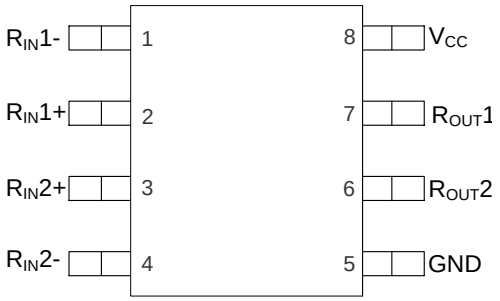
- 「*アプリケーション*」一覧、「*製品情報*」表、「*ESD 定格*」表、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクションを追加 ... 1
- Added the DQF package to the data sheet ... 3

Revision D (April 2013) から Revision E に変更 **Page**

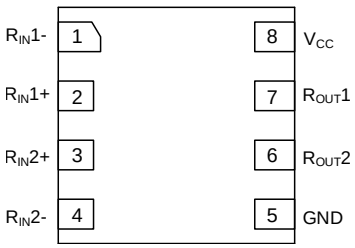
- Changed layout of National Data Sheet to TI format ... 7

5 Pin Configuration and Functions

D Package
SOIC 8 Pin
Top View



DQF Package
WSON 8 Pin
Top View



(1) DQF - Product Preview

Pin Descriptions

Pin Number	Name	Description
1	$R_{IN}1-$	Inverting receiver input pin
4	$R_{IN}2-$	
2	$R_{IN}1+$	Non-inverting receiver input pin
3	$R_{IN}2+$	
6	$R_{OUT}2$	Receiver output pin
7	$R_{OUT}1$	
8	V_{CC}	Power supply pin, +3.3V +/- 0.3V
5	GND	Ground pin

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		−0.3	4	V
Input Voltage (R_{IN}+, R_{IN}−)		−0.3	3.9	V
Output Voltage (R_{OUT})		−0.3	V_{CC} + 0.3	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Maximum Junction Temperature			135	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3	3.3	3.6	V
Receiver Input Voltage	GND		3	V
Operating Free Air Temperature (T_A)	−40	25	+125	°C

6.4 Thermal Information

THERMAL METRIC (1)		DS90LV028AQ		UNIT
		D (SOIC)	DQF (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	103.0	104	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	41.0	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (1)(2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2 V, 0 V, 3 V		R_{IN}+, R_{IN}−			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6 V or 0 V		−10	±1	+10	µA
		V_{IN} = 0V			−10	±1	+10	µA
		V_{IN} = +3.6V	V_{CC} = 0 V		-20		+20	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	2.7	3.1		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.3	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V (3)			−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current	Inputs Open		V_{CC}		5.4	9	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

6.6 Switching Characteristics(1)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF	1	1.6	2.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1	1.7	2.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (5)	(Figure 15 and Figure 16)	0	50	650	ps
t_{SKD2}	Differential Channel-to-Channel Skew-same device (6)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (7)		0		1	ns
t_{SKD4}	Differential Part to Part Skew (8)		0		1.5	ns
t_{TLH}	Rise Time			325	800	ps
t_{THL}	Fall Time			225	800	ps
f_{MAX}	Maximum Operating Frequency (9)			250		MHz

(1) These parameters are specified by design. The min/max limits are not tested in production and are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) C_L includes probe and jig capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(5) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(6) t_{SKD2} is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(7) t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(9) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), load = 15 pF (stray plus probes).

6.7 Typical Performance Curves

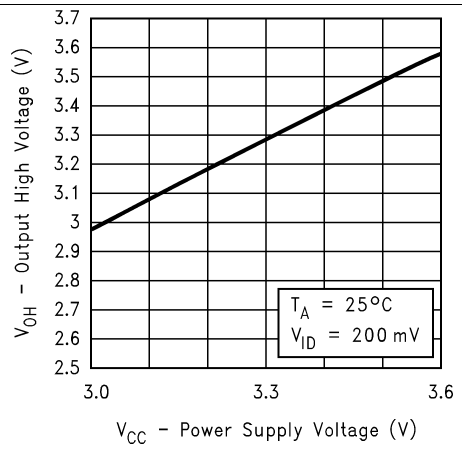


Figure 1. Output High Voltage vs Power Supply Voltage

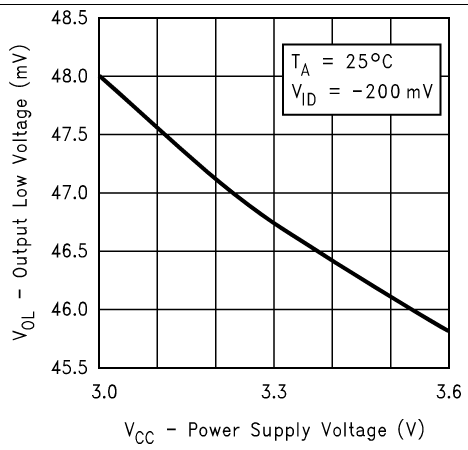


Figure 2. Output Low Voltage vs Power Supply Voltage

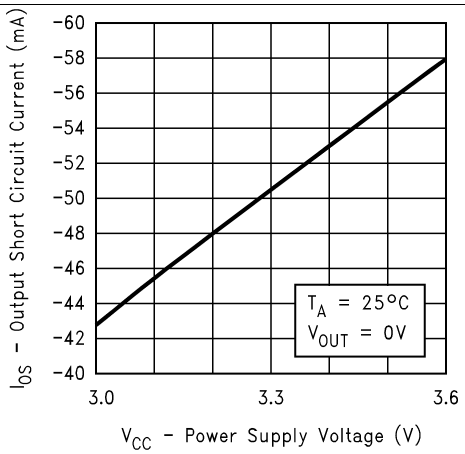


Figure 3. Output Short Circuit Current vs Power Supply Voltage

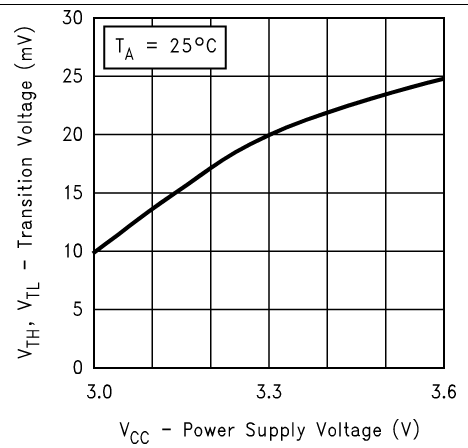


Figure 4. Differential Transition Voltage vs Power Supply Voltage

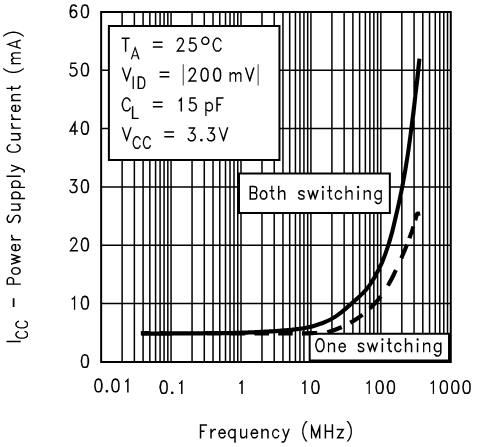


Figure 5. Power Supply Current vs Frequency

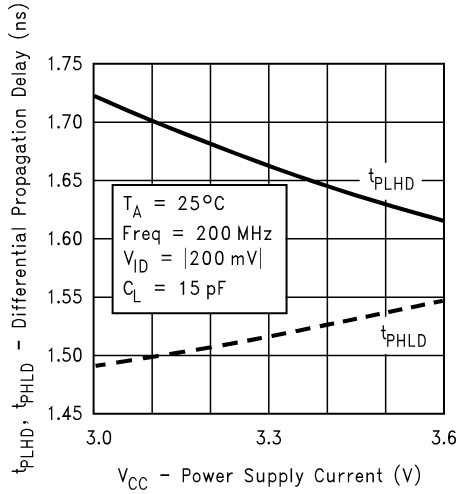


Figure 6. Differential Propagation Delay vs Power Supply Voltage

Typical Performance Curves (continued)

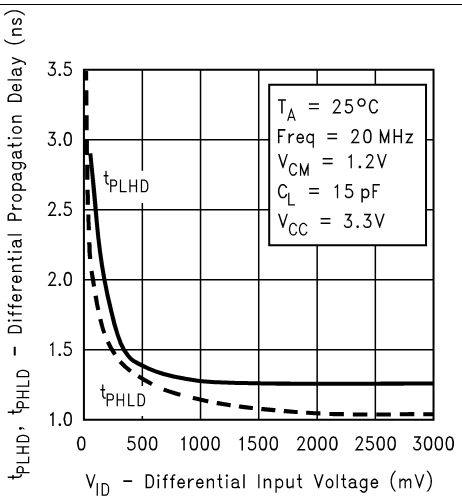


Figure 7. Differential Propagation Delay vs Differential Input Voltage

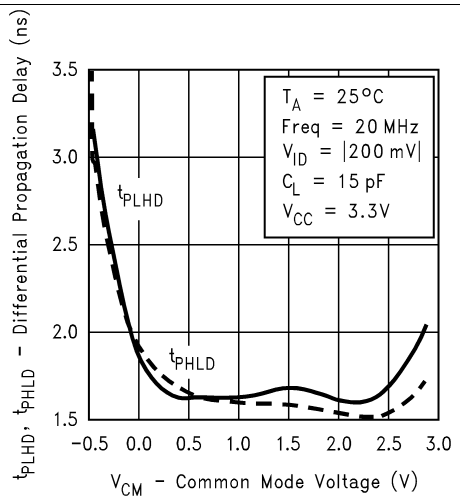


Figure 8. Differential Propagation Delay vs Common-Mode Voltage

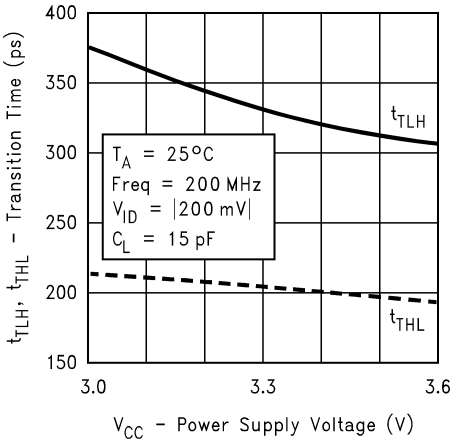


Figure 9. Transition Time vs Power Supply Voltage

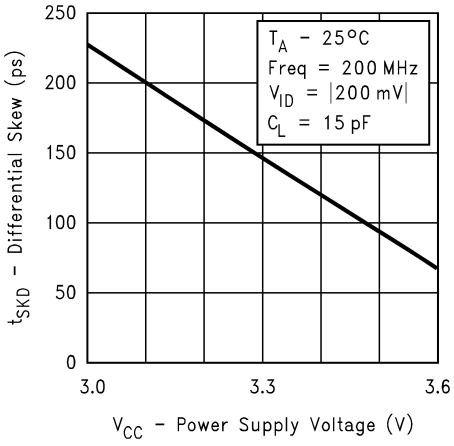


Figure 10. Differential Skew vs Power Supply Voltage

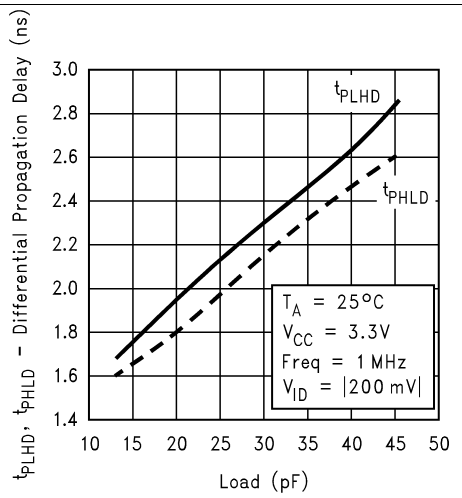


Figure 11. Differential Propagation Delay vs Load

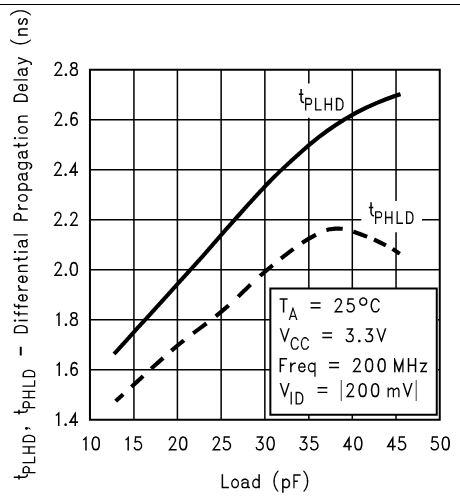


Figure 12. Differential Propagation Delay vs Load

Typical Performance Curves (continued)

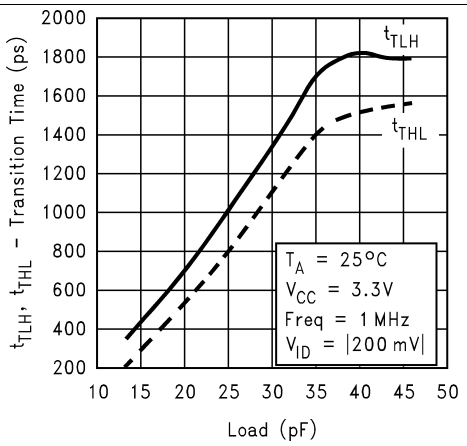


Figure 13. Transition Time vs Load

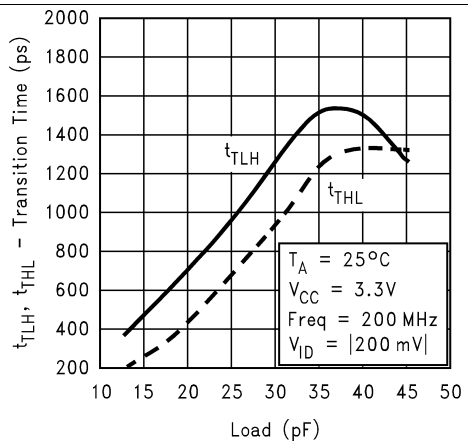


Figure 14. Transition Time vs Load

7 Parameter Measurement Information

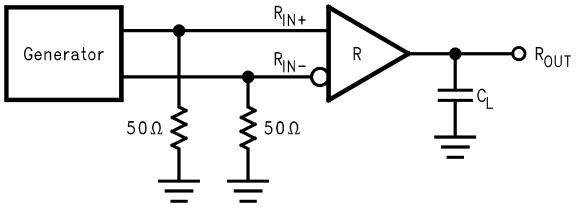


Figure 15. Receiver Propagation Delay and Transition Time Test Circuit

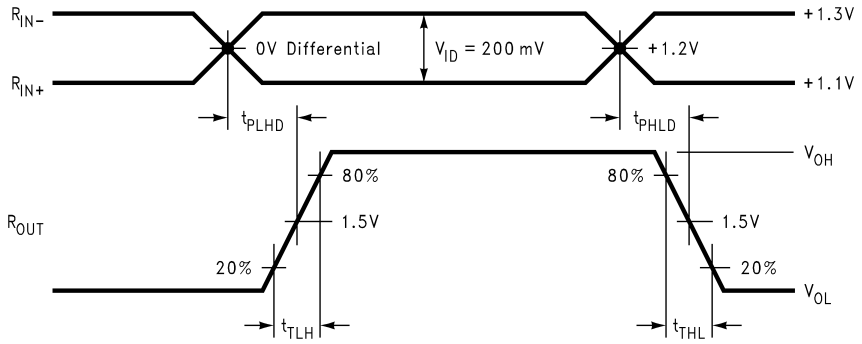
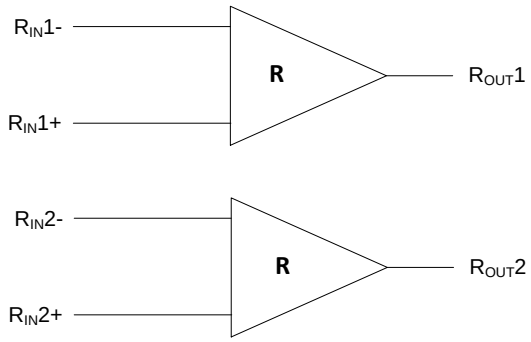


Figure 16. Receiver Propagation Delay and Transition Time Waveforms

8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes

Table 1. Truth Table

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L
$-0.1V \leq V_{ID} \leq 0.1V$	?(1)

(1) ? indicates state is indeterminate

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual at www.ti.com.

LVDS drivers and receivers are intended to be primarily used in a simple point-to-point configuration as is shown in Figure 17. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be used, and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV028AQ differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{CC}, but exceeding V_{CC} will turn on the ESD protection circuitry which will clamp the bus voltages.

9.2 Typical Application

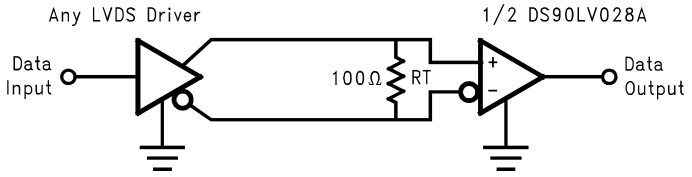


Figure 17. Balanced System Point-to-Point Application

9.2.1 Detailed Design Procedure

9.2.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1 μF and 0.01 μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10 μF (35 V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

9.2.1.2 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work correctly without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Typical Application (continued)

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm MAX).

9.2.1.3 Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5 kΩ to 15 kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry. Please refer to application note AN-1194, “Failsafe Biasing of LVDS Interfaces” (SNLA051)for more information.

9.2.1.4 Probing LVDS Transmission Lines

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

9.2.1.5 Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

10 Layout

10.1 Layout Guidelines

10.1.1 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

10.1.2 PC Board Considerations

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

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11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV028AQMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples
DS90LV028AQMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 28AQM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

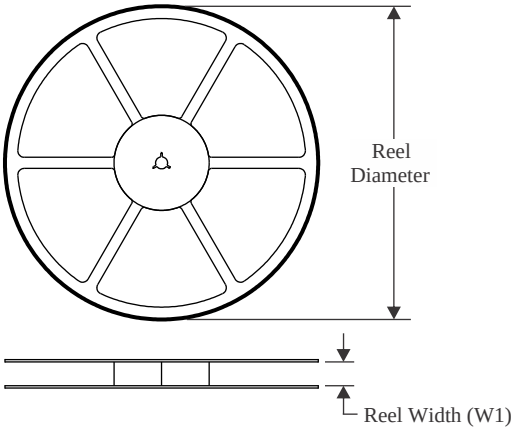
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

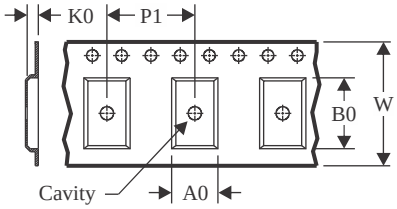
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

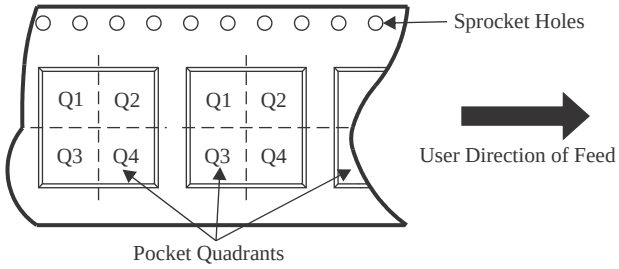


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

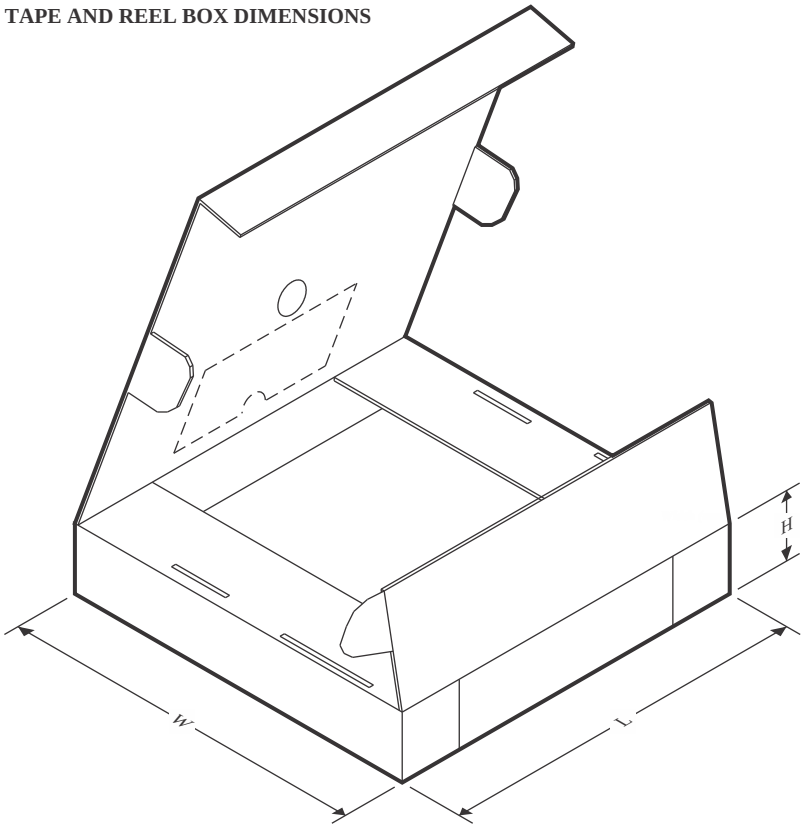
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV028AQMAX/ NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

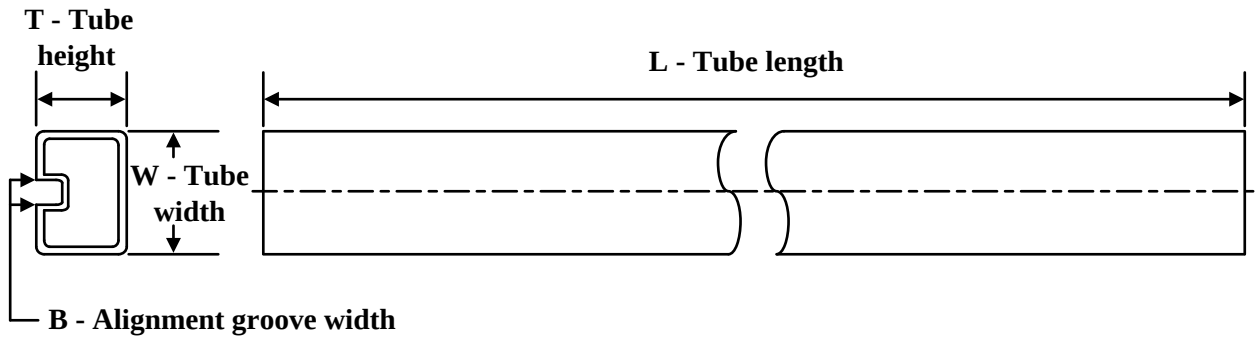
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

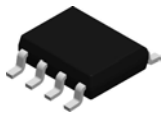
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV028AQMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV028AQMA/NOPB	D	SOIC	8	95	495	8	4064	3.05

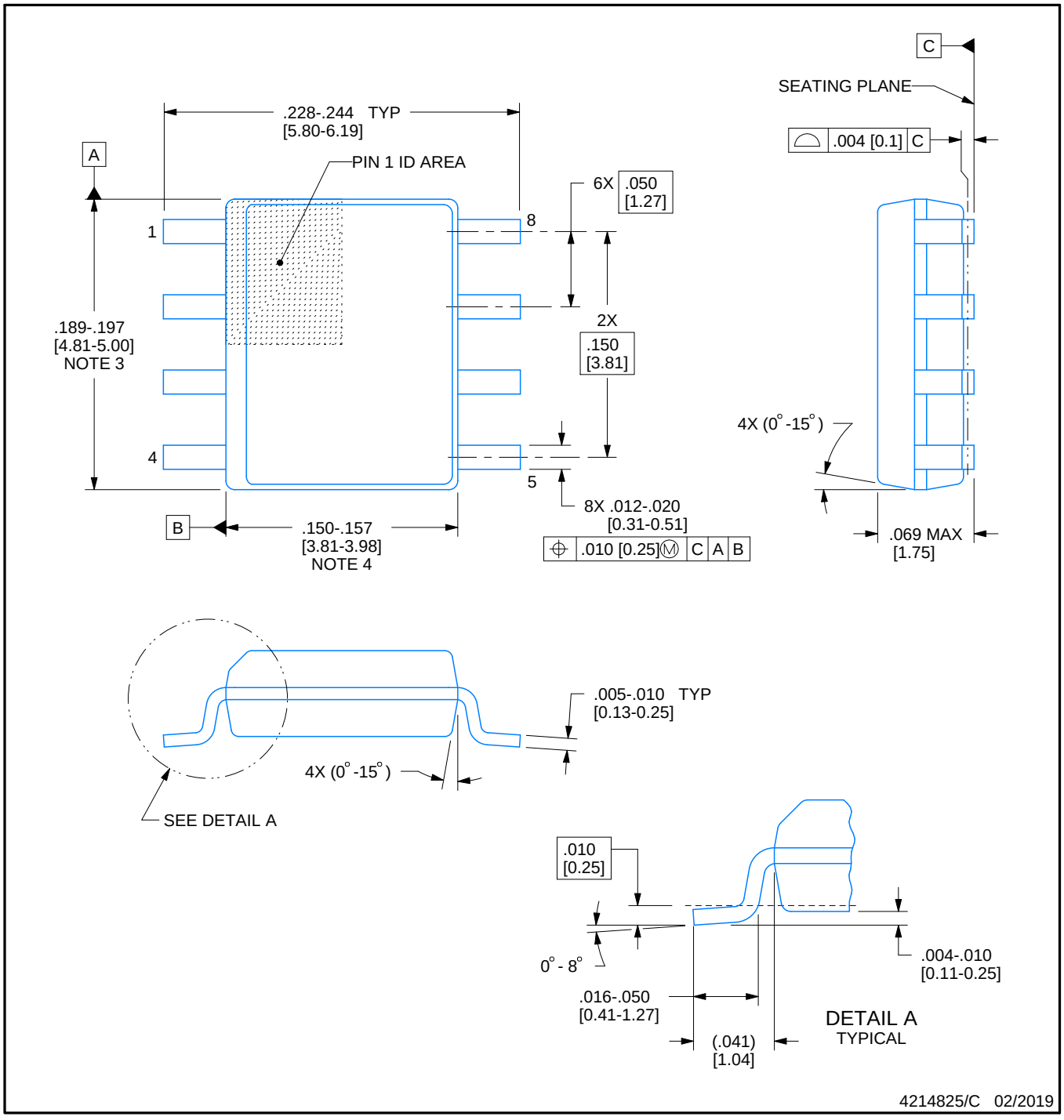


PACKAGE OUTLINE

D0008A

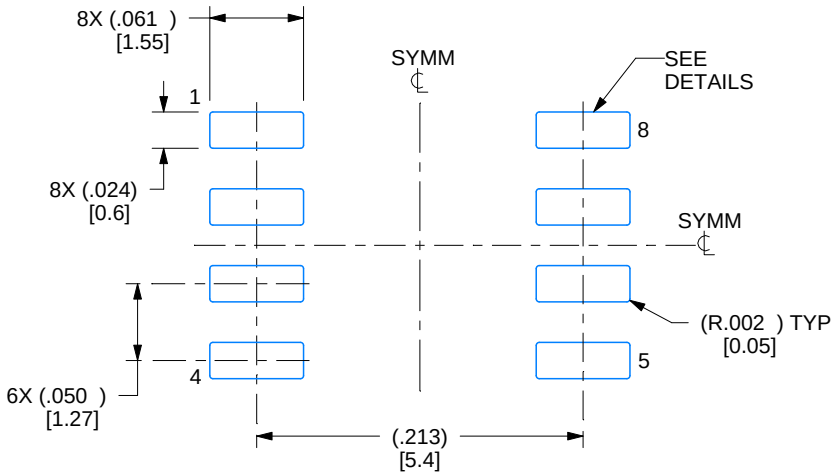
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

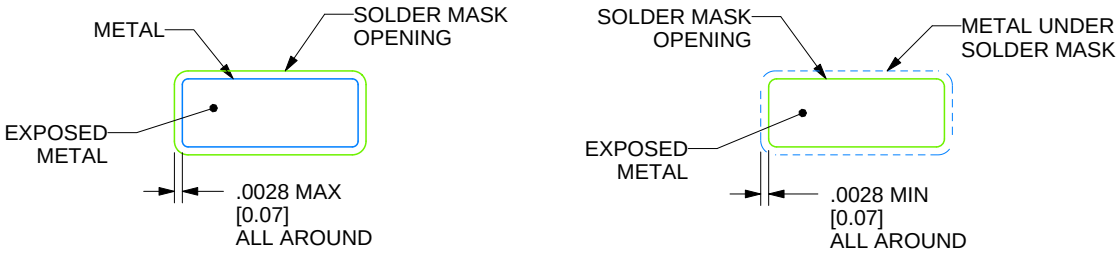


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

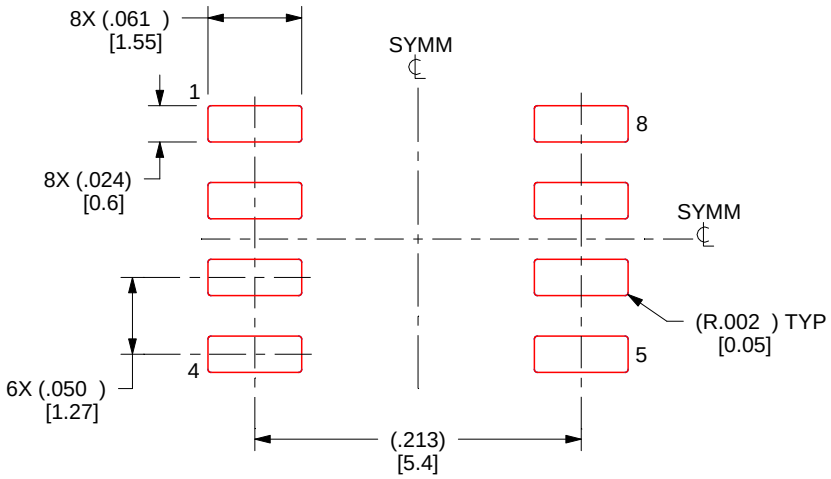
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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