

ESD224 HDMIインターフェイス用の低クランピング、4チャンネルのESD保護デバイス

1 特長

- IEC 61000-4-2 レベル4 ESD保護
 - 接触放電±12kV
 - エアギャップ放電±15kV
- IEC 61000-4-4 EFT保護
 - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
 - 2A (8/20µs)
- IO容量
 - 0.5pF (標準値)
- **HDMI 2.0準拠**
- 非常に低いリーク電流: 0.1nA (標準値)
- 非常に低いESDクランピング電圧: 16A TLPにおいて8V (システム側)
- 最大6Gbpsの高速インターフェイスをサポート
- 工業用温度範囲: -40°C ~ +125°C
- 業界標準のDQAパッケージ

2 アプリケーション

- 最終製品
 - セットトップ・ボックス
 - TVおよびモニタ
 - ラップトップおよびデスクトップPC
 - DVD、Blu-ray、マルチメディア・プレイヤー
- インターフェイス
 - HDMI 2.0/1.4
 - イーサネット10/100/1000Mbps
 - USB 3.0

3 概要

ESD224は、USB 3.0およびHDMI 2.0などの高速アプリケーション用の双方向TVS ESD保護ダイオード・アレイです。ESD224は、IEC 61000-4-2国際規格で規定されている最大レベル(レベル4)のESD耐性を備えています。ESD224は、差動マッチングされた直列素子を内蔵することで、下流のESDクランピング性能を拡張するとともに、高速インターフェイスへの信号の準拠を維持しています。ESD224の内蔵ESD保護回路で実現される非常に低いクランピング性能と高い差動帯域幅により、このデバイスはHDMI 2.0に準拠しながら、下流のHDMIデバイスを堅牢に保護できます。

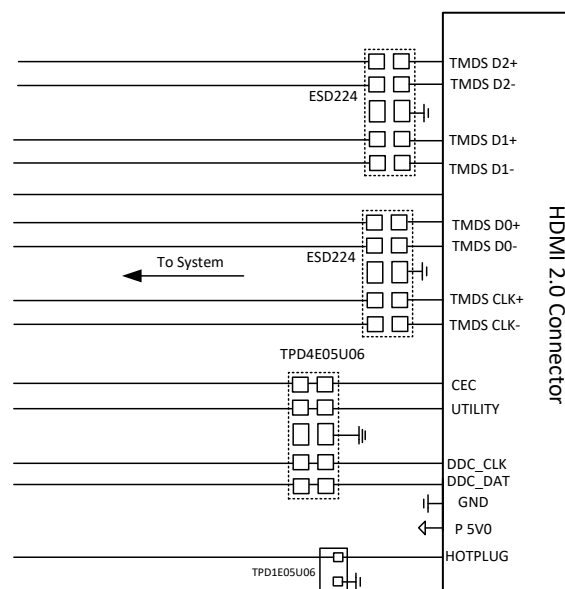
ESD224は、業界標準のUSON-10 (DQA)パッケージで供給されます。このパッケージは0.5mmピン・ピッチを採用しているため、実装が容易で、設計時間を短縮できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
ESD224	USON (10)	2.50mm×1.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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4 改訂履歴

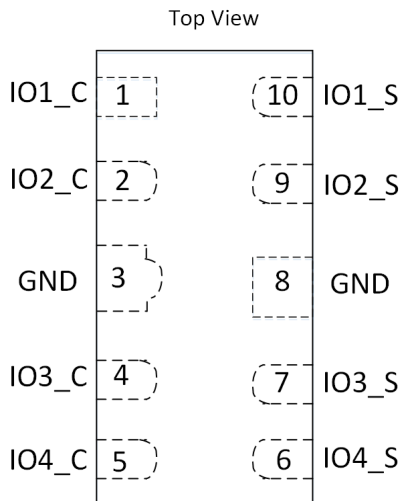
2018年2月発行のものから更新

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•	製品のステータスを「事前情報」から「量産データ」に変更	1
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5 Pin Configuration and Functions

**DQA Package
10-Pin USON
Top View**



USON-10 2.5 mm x 1.0 mm, 0.5 mm pitch

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground. These pins are shorted internally.
GND	8		
IO1_C	1	Connector Side I/O	ESD protected channel to be connected to the connector
IO2_C	2		
IO3_C	4		
IO4_C	5		
IO4_S	6	System Side I/O Pin corresponding to IO4_C	To be connected to the system side
IO3_S	7	System Side I/O Pin corresponding to IO3_C	
IO2_S	9	System Side I/O Pin corresponding to IO2_C	
IO1_S	10	System Side I/O Pin corresponding to IO1_C	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25°C		80	A
Peak Pulse	IEC 61000-4-5 Surge (t_p 8/20 μ s) Peak Power at 25°C		17	W
	IEC 61000-4-5 Surge (t_p 8/20 μ s) Peak Current at 25°C		2	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±12000
		IEC 61000-4-2 Air Discharge, all pins	±15000

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-3.6		3.6	V
T_A	Operating Free Air Temperature	-40		125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD224	UNIT
		DQA (USON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

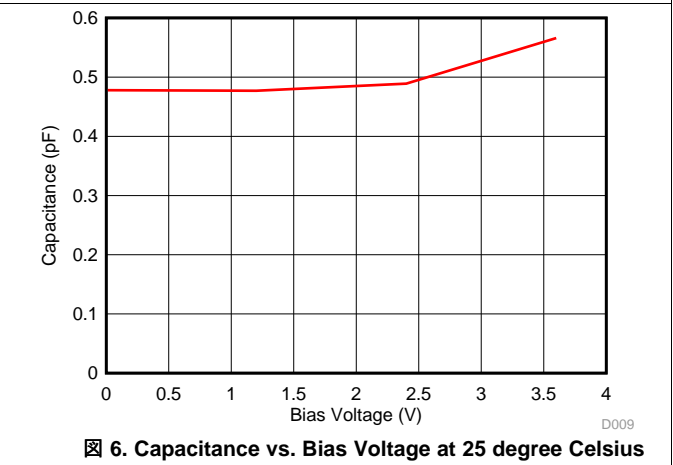
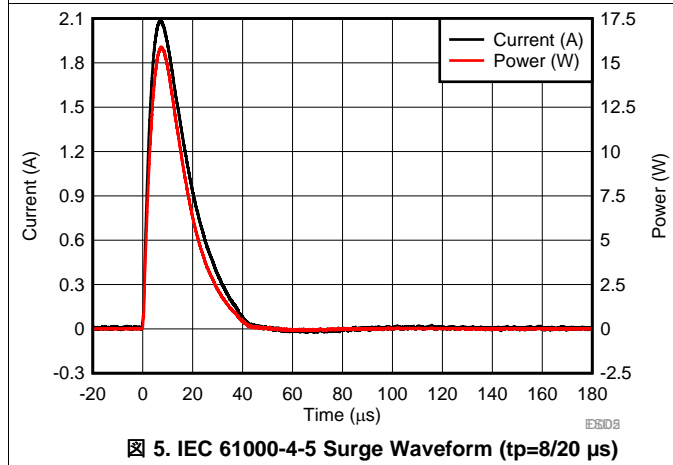
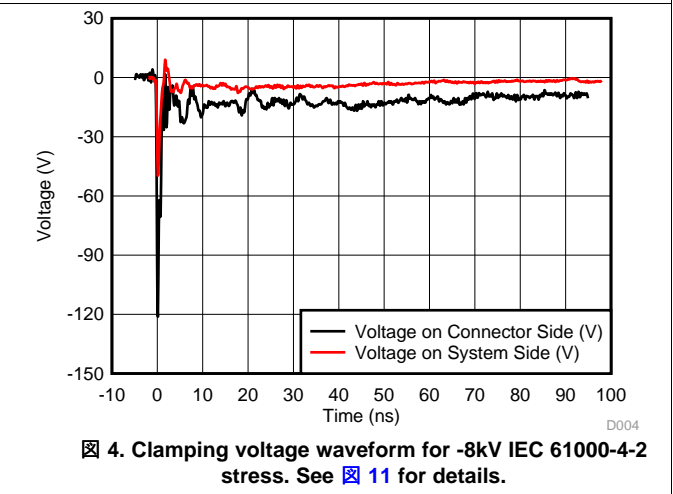
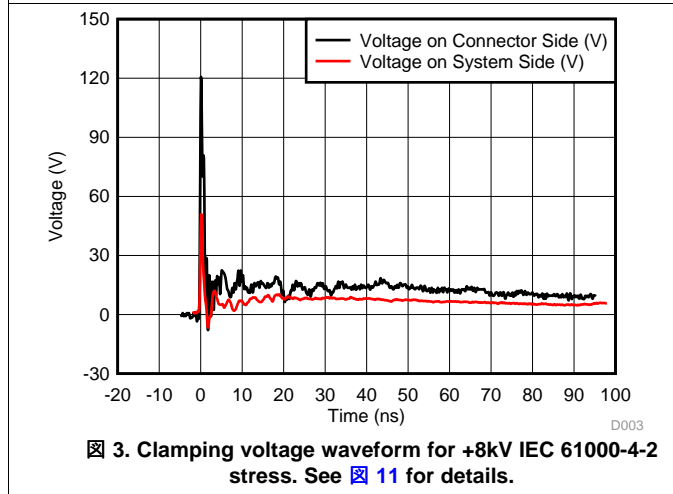
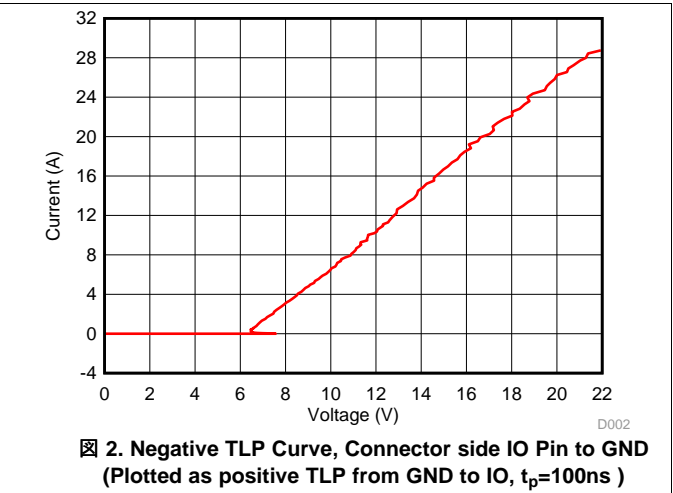
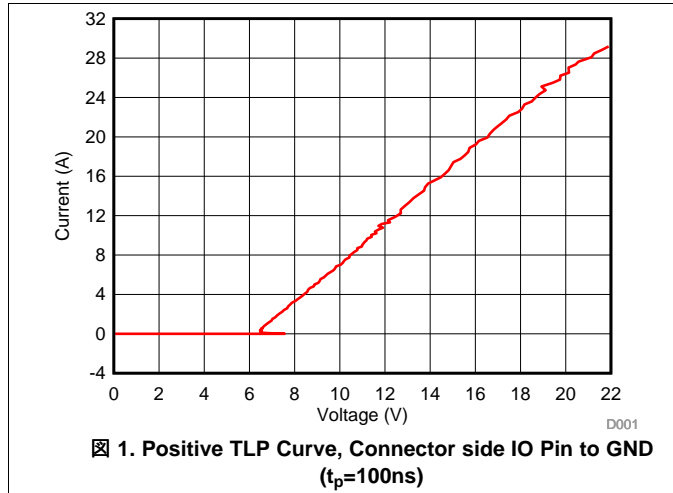
At $T_A = 25^\circ\text{C}$ unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 10 \text{ nA}$, across operating temperature range	-3.6		3.6	V
V_{BRF}	Breakdown voltage, Pin 1, 2, 4, 5 to 3 (GND) ⁽¹⁾	$I_{IO} = 1 \text{ mA}$	5		7.9	V
V_{BRR}	Reverse breakdown voltage, pin 1, 2, 4, 5 to 3 (GND) ⁽¹⁾	$I_{IO} = -1 \text{ mA}$	-7.9		-5	V
V_{HOLD}	Holding voltage, pin1, 2, 4, 5 to 3 (GND) and 3 (GND) to pin 1, 2, 4, 5 ⁽²⁾	$I_{IO} = 1 \text{ mA}$		6.3		V
$V_{HOLD-NEG}$	Breakdown voltage, pin1, 2, 4, 5 to 3 (GND) ⁽²⁾	$I_{IO} = -1 \text{ mA}$		-6.3		V
V_{CLAMP}	TLP Clamping voltage (Intrinsic)	IPP = 1 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		7		V
		IPP = 5 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		9		V
		IPP = 16 A, pin 1, 2, 4, 5 to 3 or 8(GND), GND to pin 1, 2, 4, 5		14		V
$V_{CLAMP-IEC-SYS}$	IEC 61000-4-2 30 ns Clamping voltage (system side) assuming system draws at least 3 A of current at 8 V. See measurement setup.	8-kV Contact discharge on pin 1, 2, 4, 5 with pin3 grounded. Voltage waveform measured at pin 6, 7, 9, 10 with respect to GND		8		V
		-8-kV Contact discharge on pin 1, 2, 4, 5 with pin3 grounded. Voltage waveform measured at pin 6, 7, 9, 10 with respect to GND		-5		V
R_{DYN}	Dynamic resistance	Pin 1, 2, 4, 5 to GND, 100 ns TLP		0.5		Ω
		GND to Pin 1, 2, 4, 5, 100 ns TLP		0.5		
C_{LINE}	Line capacitance, any IO to GND	$V_{IO} = 0 \text{ V}$, $V_{p-p} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.5	0.6	pF
ΔC_{LINE}	Variation of line capacitance	$C_{LINE1} - C_{LINE2}$, $V_{IO} = 0 \text{ V}$, $V_{p-p} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.02	0.07	pF
C_{CROSS}	Line-to-line capacitance between one differential pair to another differential pair	$V_{IO} = 0 \text{ V}$, $V_{rms} = 30 \text{ mV}$, $f = 1 \text{ MHz}$		0.28		pF
S_{21DC}	DC Insertion Loss	DC insertion loss at Ch1, Ch2, Ch3, Ch4		0.3		dB
$I_{leakage}$	Leakage Current	$V_{IO} = \pm 3.6 \text{ V}$, Pin 1,2,4,5 to Pin 3		0.1	10	nA

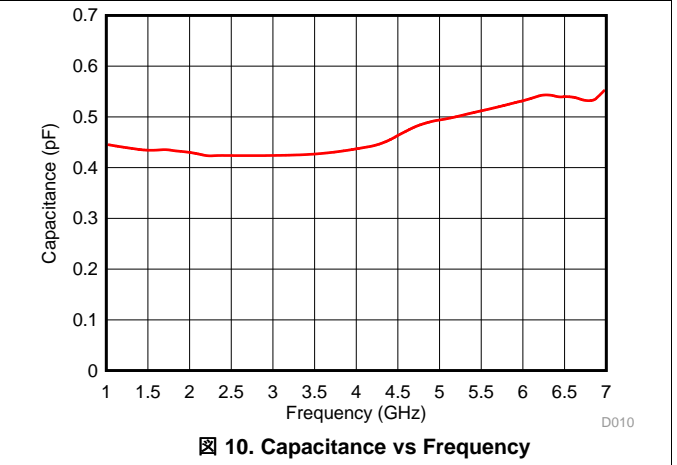
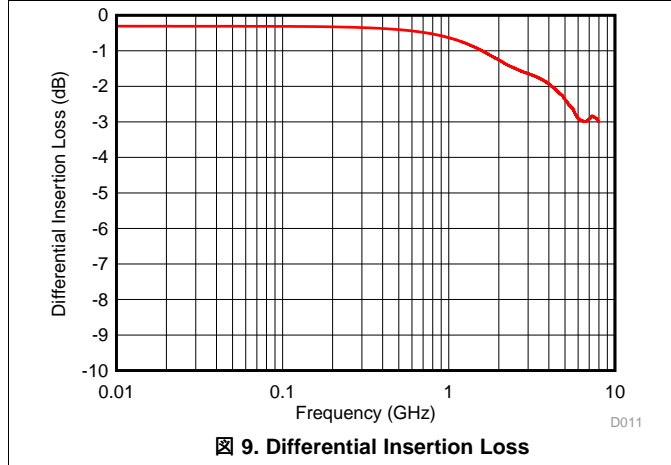
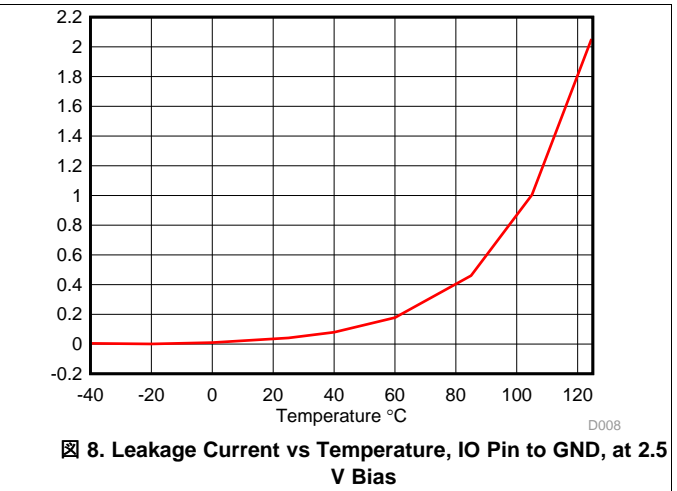
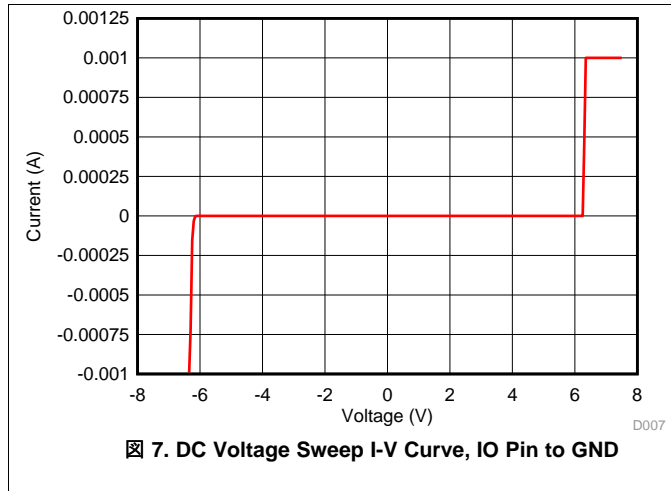
(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics




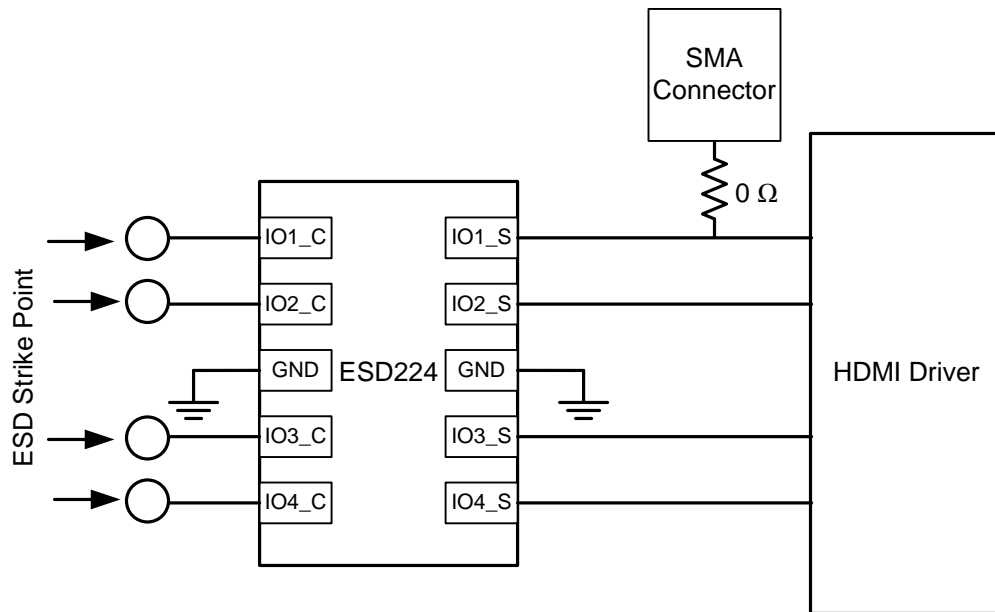
Typical Characteristics (continued)



7 Parameter Measurement Setup

7.1 IEC 61000-4-2 System Level ESD Test Setup with HDMI Driver for Clamping Voltage Measurement


11 shows the setup used to perform System Level ESD test to evaluate the clamping performance of ESD224 in real-world applications where the device is protecting a downstream HDMI driver System-on-Chip. IEC 61000-4-2 8kV Contact stress was applied at the connector pin and the voltage waveform on the system-side pin was captured to look at the clamping voltage presented by ESD224 to the down stream HDMI driver.



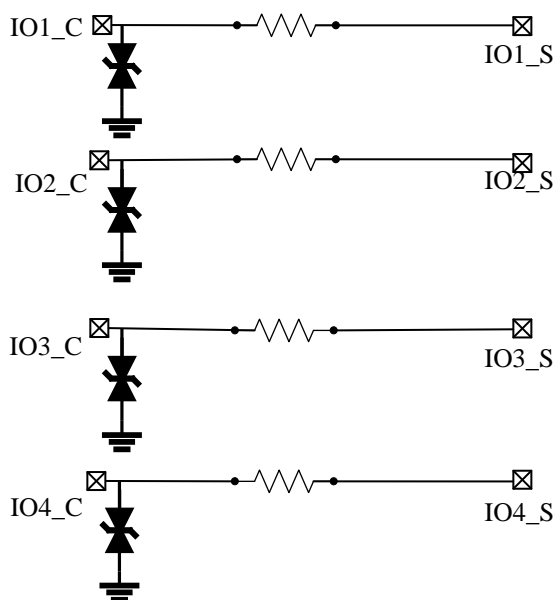

11. System Level IEC 61000-4-2 ESD Test Setup with ESD224 protecting an HDMI driver chip

8 Detailed Description

8.1 Overview

The ESD224 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ± 12 -kV contact and ± 15 -kV air gap. The ESD-surge clamp diverts the current to ground.

8.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50- Ω impedance). The ESD-surge clamp diverts the current to ground.

8.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 μ s waveform). The ESD-surge clamp diverts this current to ground.

8.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.5 pF (typical). This device supports data rates up to 6 Gbps.

8.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ± 5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 3.6 V.

Feature Description (continued)

8.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ± 2.5 V.

8.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8 V ($I_{PP} = 16$ A TLP) on the system side pins when the system draws at least 3 A.

8.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 6 Gbps, because of the extremely low IO capacitance.

8.3.9 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

8.4 Device Functional Modes

The ESD224 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR} . During ESD events, voltages as high as ± 15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD224 (usually within 100s of nano-seconds) the device reverts to passive.

9 Application and Implementation

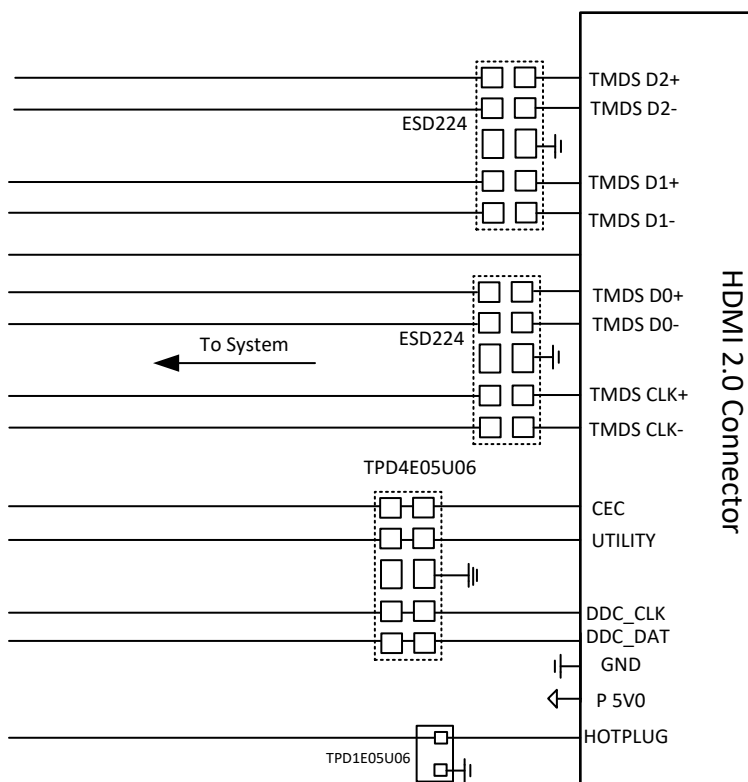
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ESD224 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. Part of this voltage drop across the diode drops across the series element between the connector side pin and the system-side pin. Therefore, the effective voltage drop across the protected IC is smaller than the voltage drop across the diode. It is recommended to avoid through-routing for this ESD diode (single trace connecting both the connector side pin and the system side pin) for the best ESD performance.

9.2 Typical Application



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图 12. ESD224 Protecting the HDMI Interface

Typical Application (continued)

9.2.1 Design Requirements

In this design example, two ESD224 devices, one TPD4E05U06 and one TPD1E05U06 device are used to protect an HDMI 2.0 interface. For HDMI 2.0 application design parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on high speed differential data lines	0 to 3.6 V
Operating frequency of high speed data lines	3 GHz (First Harmonic)
Signal range on control lines (CEC, UTILITY, DDC_CLK and DDC_DAT)	0 to 5 V

9.2.2 Detailed Design Procedure

9.2.2.1 Signal Range

ESD224 supports signal ranges between -3.6 V and 3.6 V , which supports the high-speed lines on the HDMI 2.0 application. The TPD4E05U06 and TPD1E05U06 support signal ranges between 0 V and 5.5 V , which supports the HDMI control lines.

9.2.2.2 Operating Frequency

The ESD224 has a 0.5 pF (typical) capacitance, which supports the HDMI 2.0 rate of 6 Gbps . The TPD4E05U06 and TPD1E05U06 have a typical capacitance of 0.5 pF and 0.42 pF respectively, which easily support the control lines. The ESD224 has 4 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

9.2.3 Application Curves

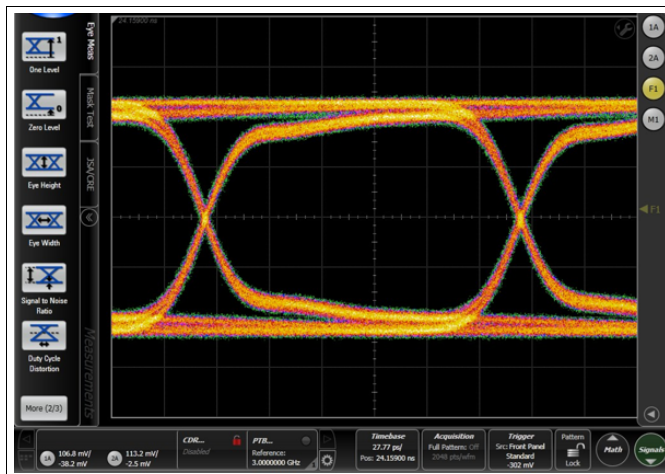


图 13. HDMI 2.0 6 Gbps Eye Diagram (Bare Board)

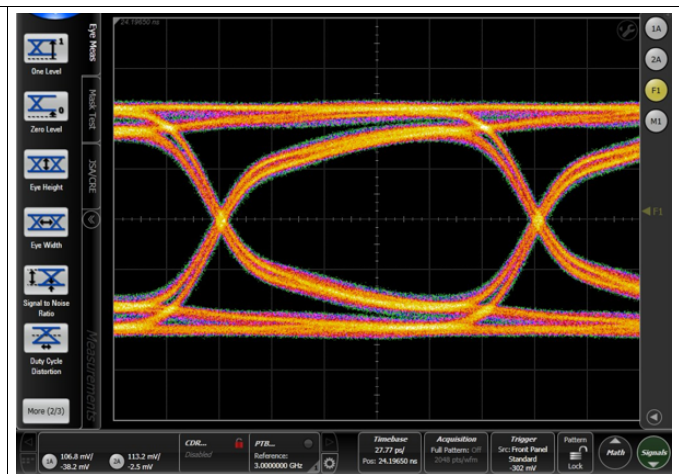


图 14. HDMI 2.0 6 Gbps Eye Diagram with ESD224

10 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- For the best ESD performance, do not use through-routing for the data channels. Connecting pins 1 and 10, 2 and 9, 4 and 7, 5 and 6 together with through routing will reduce the clamping voltage performance of ESD224.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Examples

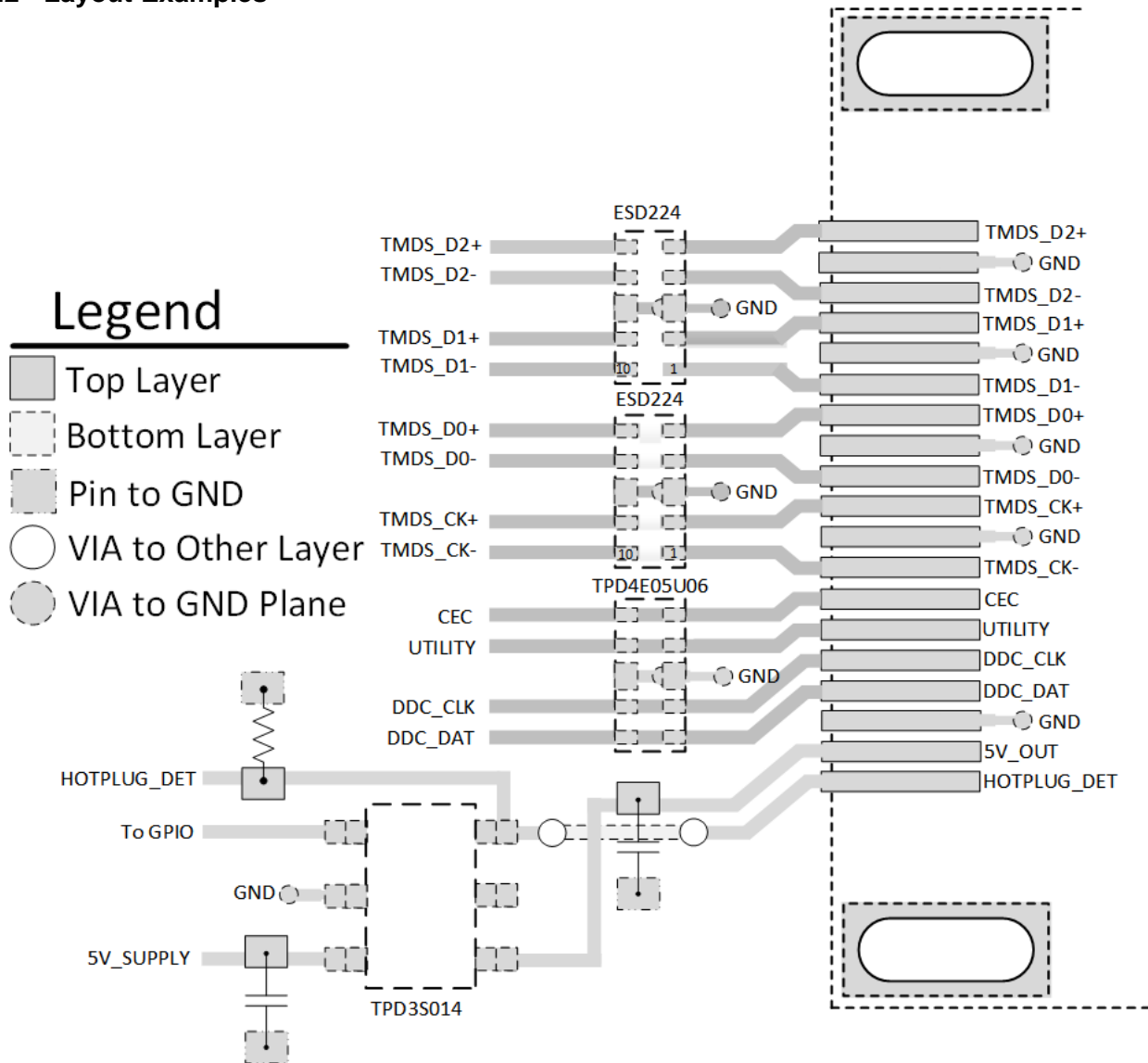


图 15. HDMI Type-A Transmitter Port Layout

注

There is no Through-Routing for the ESD224 Pins Connecting to the High Speed Data Lines.

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD224DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1AR	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

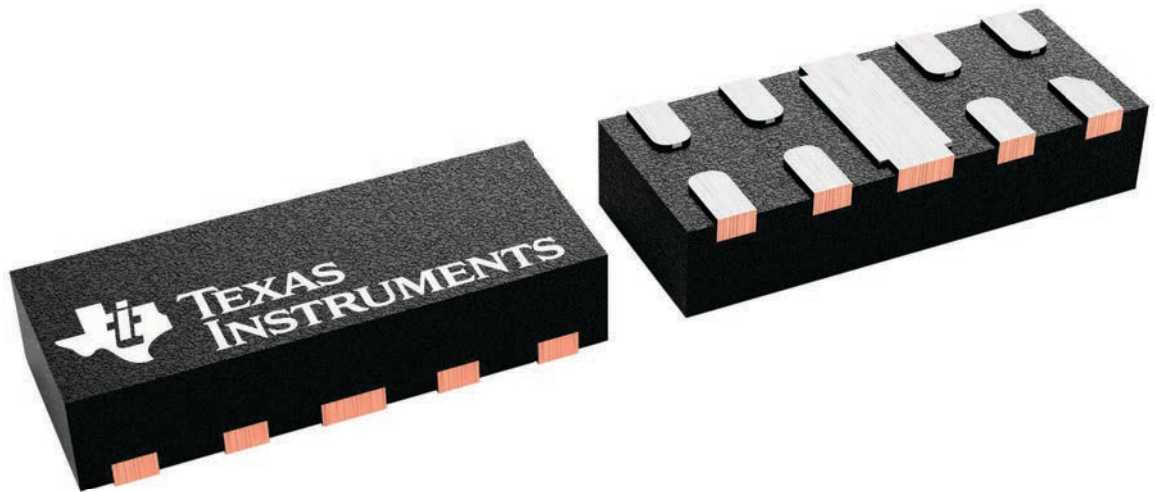
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230320/A

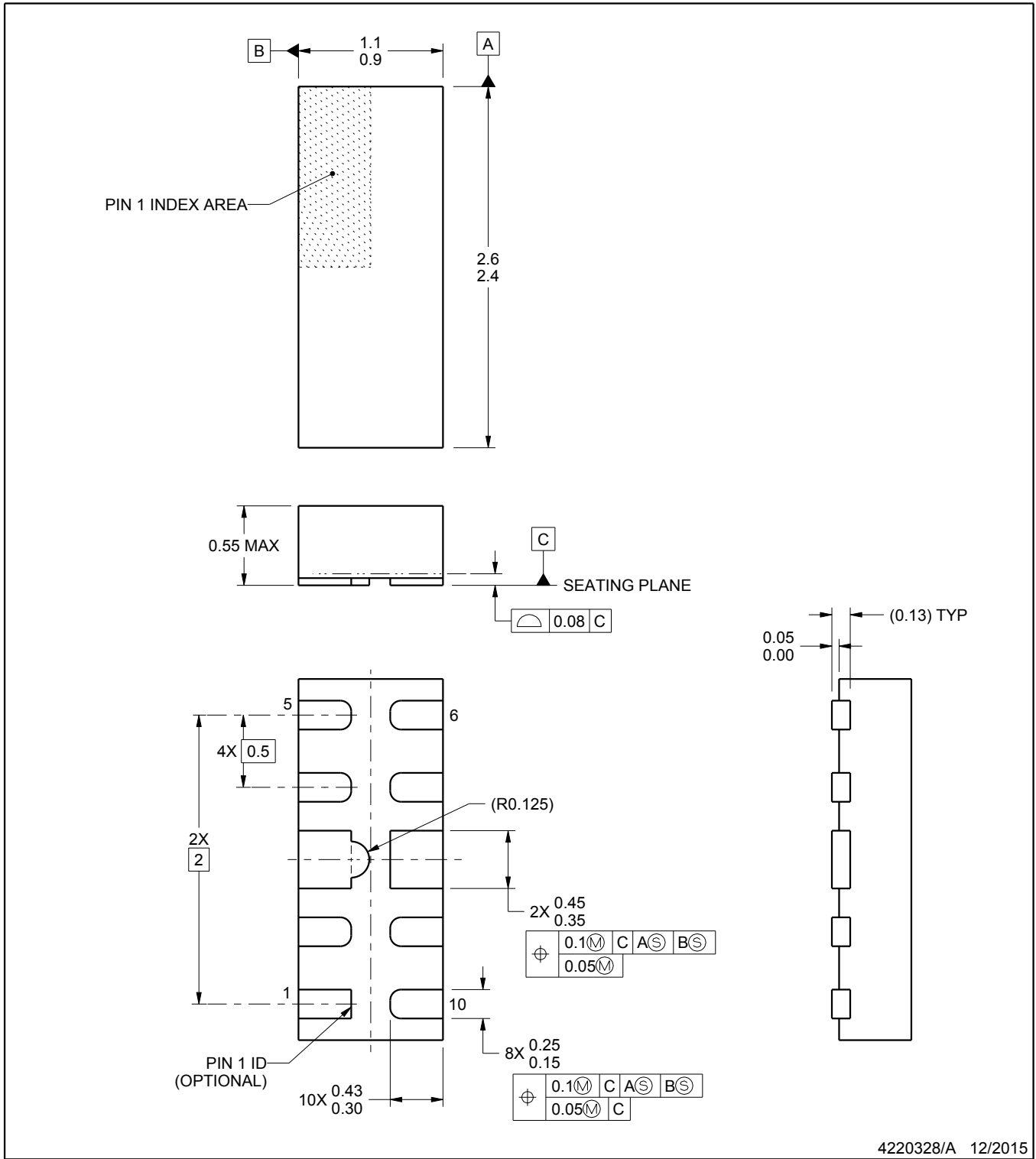
DQA0010A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

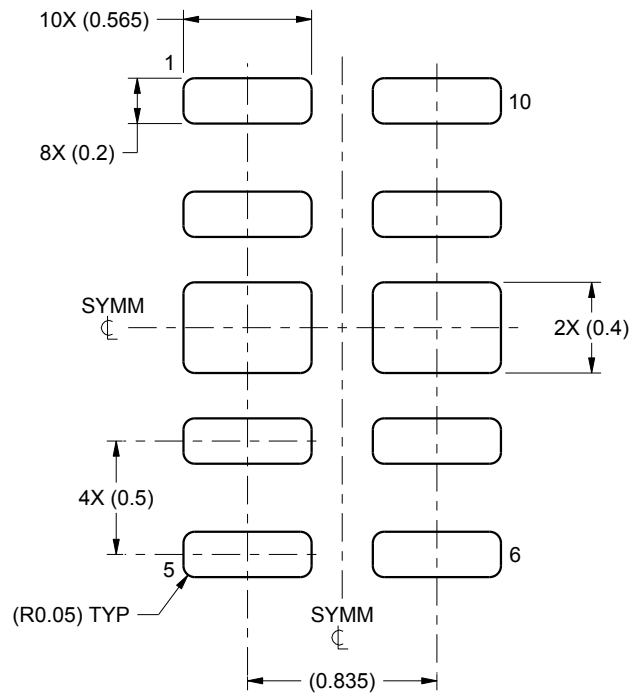
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

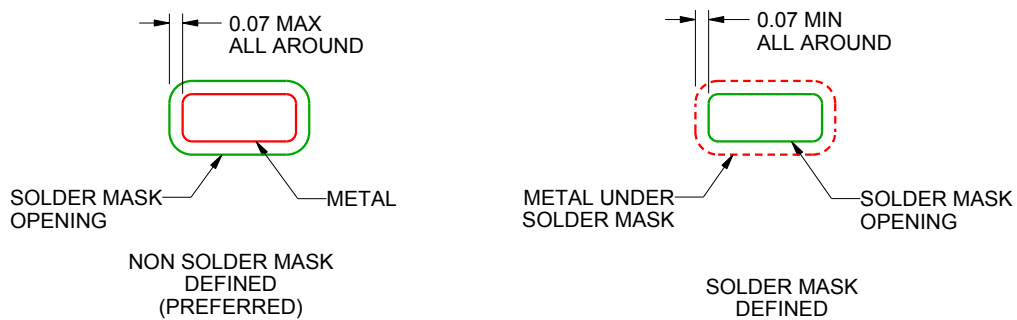
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

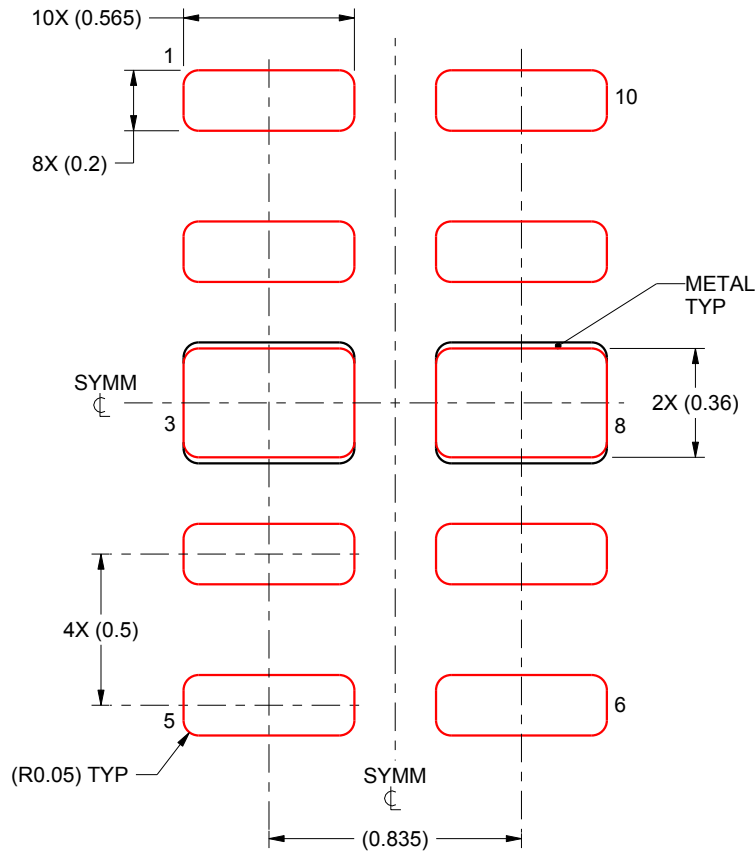
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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