HD3SS3202 2チャネル差動2:1/1:2 USB3.1マルチプレクサ/デマルチプレクサ

1 特長

- USB 3.1 Gen 1およびGen 2データ速度で、USB Type-C™エコシステム用のマルチプレクサ/デマルチプレクサ・ソリューションを提供
- MIPI DSI/CSI-2 DPHY、LVDS、PCIE Gen III、SATA Express、SATAと互換
- 最高10Gbpsで動作
- 8GHzを超える広い-3dB差動帯域幅
- 優れた動特性(5GHz時)
  - クロストーク = -41dB
  - オフ絶縁 = -20dB
  - 挿入損失 = -2.4dB
  - 反射損失 = -8dB
- 双方向「マルチプレクサ/デマルチプレクサ」差動スイッチ
- 0～2Vの同相電圧をサポート
- V_{CC}が3.3V±10%の単一電源
- 商業用温度範囲: 0℃～70℃ (HD3SS3202)
- 工業用温度範囲: -40℃～85℃ (HD3SS3202I)

2 アプリケーション

- USB Type-C™エコシステム
- デスクトップPCおよびノートPC
- 共有I/Oポート
- ドッキング・ステーション
- モニタ、テレビ
- セットトップ・ボックス
- ネットワーク・セキュリティ・カメラ

3 概要

HD3SS3202は、マルチプレクサまたはデマルチプレクサ構成の高速双方向パッシブ・スイッチで、USB 3.1 Gen 1およびGen 2データ速度をサポートするUSB Type-C™アプリケーションに適しています。このデバイスは制御ピンSELに従い、ポートBまたはポートCとポートAとの間で差動チャネルのスイッチングを行います。

HD3SS3202は汎用のアナログ差動パッシブ・スイッチです。0～2Vの同相電圧範囲と、最大1800mVppの差動振幅での差動信号処理を必要とする、任意の高速インターフェイス・アプリケーションで動作します。このデバイスには適応型トラッキング機能があり、同相電圧範囲の全体にわたってチャネルが変化せず維持されることを保証します。

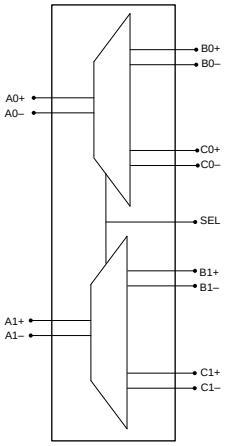
このデバイスにより、信号のアイ・ダイアグラムへの減衰を最小限に抑え、追加のジッタもほとんどなしに、高速なスイッチングが可能になります。動作時の消費電力は1.65mW未満(標準値)です。OEnピンによるシャットダウン・モードがあり、シャットダウン時の消費電力は0.02µW未満(標準値)です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
HD3SS3202 HD3SS3202I	UQFN (16)	2.60mm×1.80mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年5月発行のものから更新 **Page**

- Changed I_{CC} max from 0.6mA to 0.8mA ... 5

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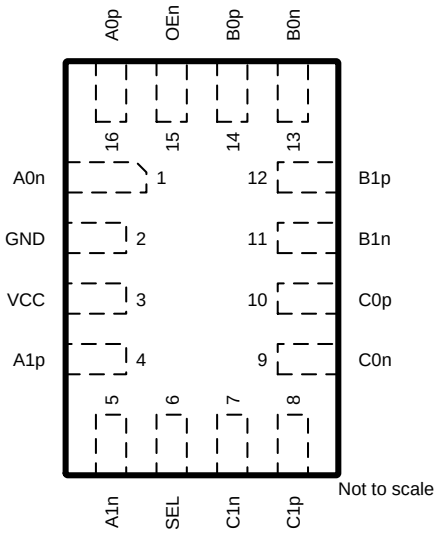
5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0n	1	I/O	Port A, channel 0, high-speed negative signal
GND	2	G	Ground
V_{CC}	3	P	3.3-V power
A1p	4	I/O	Port A, channel 1, high-speed positive signal
A1n	5	I/O	Port A, channel 1, high-speed negative signal
SEL	6	I	Port select pin. To help with noise immunity, a 0.01 µF capacitor to GND on this pin is suggested. L: Port A to Port B H: Port A to Port C
C1n	7	I/O	Port C, channel 1, high-speed negative signal (connector side)
C1p	8	I/O	Port C, channel 1, high-speed positive signal (connector side)
C0n	9	I/O	Port C, channel 0, high-speed negative signal (connector side)
C0p	10	I/O	Port C, channel 0, high-speed positive signal (connector side)
B1n	11	I/O	Port B, channel 1, high-speed negative signal (connector side)
B1p	12	I/O	Port B, channel 1, high-speed positive signal (connector side)
B0n	13	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	14	I/O	Port B, channel 0, high-speed positive signal (connector side)
OEn	15	I	Active-low chip enable. To help with noise immunity, a 0.01 µF capacitor to GND on this pin is suggested. L: Normal operation H: Shutdown
A0p	16	I/O	Port A, channel 0, high-speed positive signal

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4	V
	Voltage	Differential I/O	–0.5	2.5	V
		Control pins	–0.5	V_{CC}+ 0.5	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{ih}	Input high voltage (SEL, OEn pins)		2		V_{CC}	V
V_{il}	Input low voltage (SEL, OEn pins)		–0.1		0.8	V
V_{diff}	High-speed signal pins differential voltage		0		1.8	V_{pp}
V_{cm}	High speed signal pins common mode voltage		0		2	V
T_A	Operating free-air/ambient temperature	HD3SS3202RSV	0		70	°C
		HD3SS3202IRSV	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)		HD3SS3202 RSV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	V_{CC} = 3.3 V, OEn = 0		0.5	0.8	mA
I_{STDN}	Device shutdown current	V_{CC} = 3.3 V, OEn = V_{CC}		0.005	1	µA
C_{ON}	Output ON capacitance to GND			0.6		pF
C_{OFF}	Output OFF capacitance to GND			0.8		pF
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_{CM} = 0 to 2 V; I_O = –8 mA		5	8	Ω
ΔR_{ON}	On-resistance match between pairs of the same channel	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN)	V_{CC} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 2.35 V			1	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, OEn)				1	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, OEn)				1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for selected port, A and B with SEL = 0, and A and C with SEL = V_{CC}			1	µA
$I_{IH,HS}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 2 V for non-selected port, C with SEL = 0, and B with SEL = V_{CC} (1)		100	140	µA
$I_{IL,HS}$	Input low current, high-speed pins [Ax/Bx/Cx][p/n]				1	µA

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 0.3 MHz		-0.4		dB
		f = 0.625 MHz		-0.4		
		f = 2.5 GHz		-1.3		
		f = 4 GHz		-2.0		
		f = 5 GHz		-2.4		
BW	–3-dB bandwidth			8		GHz
R_L	Differential return loss	f = 0.3 MHz		-27		dB
		f = 2.5 GHz		-11		
		f = 4 GHz		-9		
		f = 5 GHz		-8		
O_{IRR}	Differential OFF isolation	f = 0.3 MHz		-77		dB
		f = 2.5 GHz		-23		
		f = 4 GHz		-21		
		f = 5 GHz		-20		
X_{TALK}	Differential crosstalk	f = 0.3 MHz		-82		dB
		f = 2.5 GHz		-44		
		f = 4 GHz		-41		
		f = 5 GHz		-41		

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6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay (see 図 4)				80	ps
t_{SW_ON}	Switching time SEL-to-Switch ON (see 図 3)				0.5	µs
t_{SW_OFF}	Switching time SEL-to-Switch OFF (see 図 3)				0.5	µs
t_{SK_INTRA}	Intra-pair output skew (see 図 4)				6	ps
t_{SK_INTER}	Inter-pair output skew (see 図 4)				20	ps
t_{PD}	Average propagation delay, see 図 1	f = 100 MHz	16		54	ps
		f = 200 MHz	33		63	
		f = 300 MHz	33		59	
		f = 400 MHz	33		57	
		f = 500 MHz	33		56	
		f = 600 MHz	33		53	
		f = 700 MHz	33		50	
		f = 750 MHz	33		50	
		f = 800 MHz	33		50	
		f = 900 MHz	31		50	
		f = 1000 MHz	30		50	

6.8 Typical Characteristics

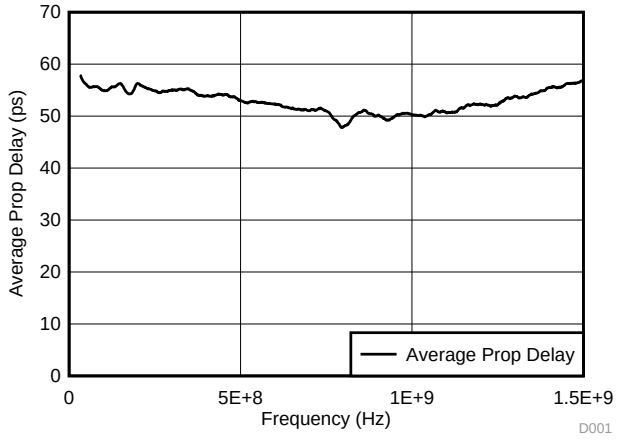

図 1. Average Propagation Delay vs Frequency

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7 Parameter Measurement Information

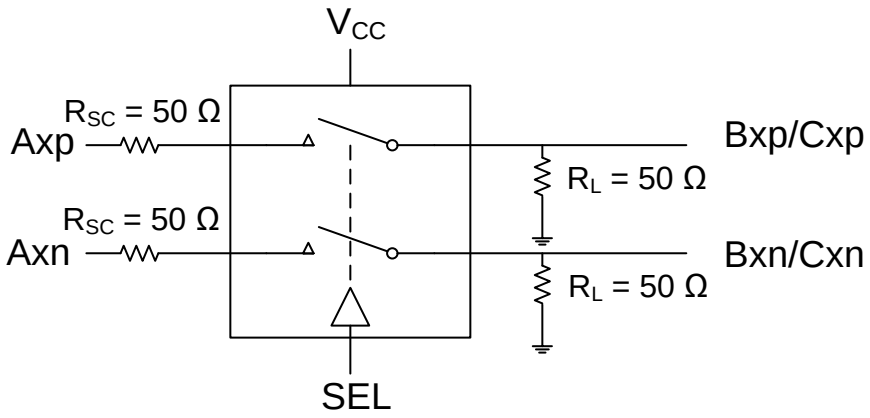

図 2. Test Setup

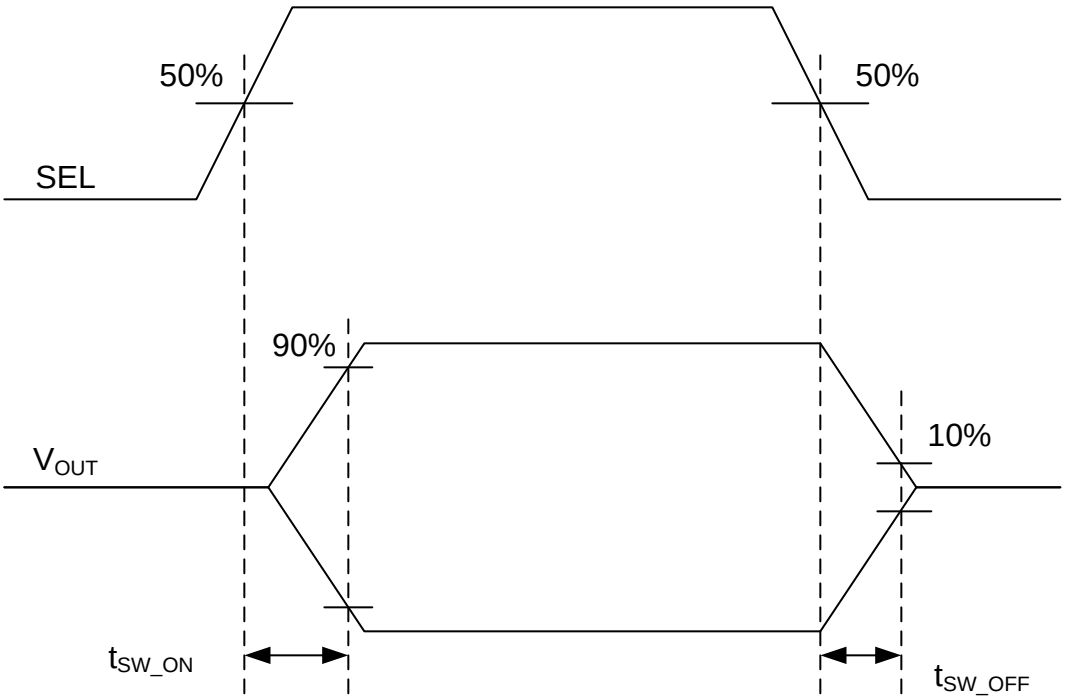

図 3. Switch On and Off Timing Diagram

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Parameter Measurement Information (continued)

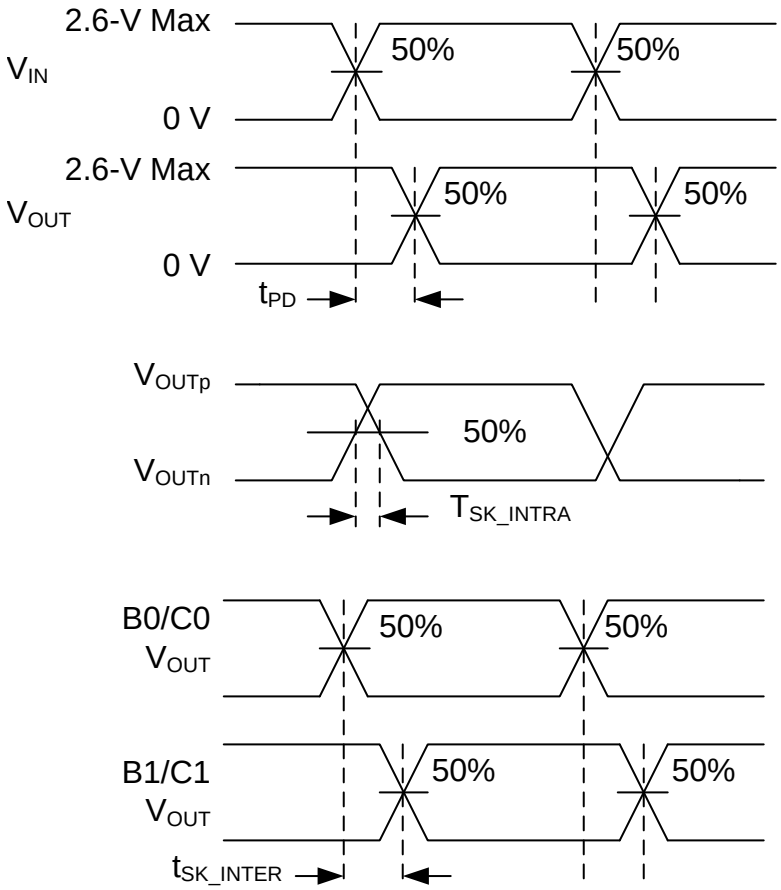

図 4. Timing Diagrams and Test Setup

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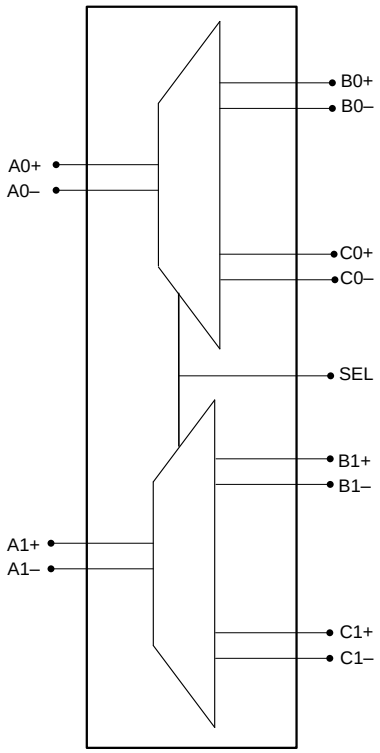
8 Detailed Description

8.1 Overview

The HD3SS3202 is a generic analog differential passive switch that can works for any high-speed interface applications requiring a common mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It uses adaptive tracking to ensures the channel remain unchanged for the entire common mode voltage range.

Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to the signal eye diagram with little added jitter. It consumes < 1.65 mW (typ) of power when operational and has a shutdown mode exercisable by OEn pin resulting < .02 µW (typical).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Enable and Power Savings

The HD3SS3202 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes little current to save the maximum power. To enter standby mode, the OEn control pin is pulled high through a resistor and must remain high. For active/normal operation, the OEn control pin should be pulled low to GND.

HD3SS3202 consumes < 1.65 mW (typ) of power when operational and has a shutdown mode exercisable by the OEn pin resulting < .02 µW (typ).

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8.4 Device Functional Modes

表 1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

(1) The HD3SS3202 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Take care to ensure the same polarity is maintained on Port A versus Ports B/C.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The HD3SS3202 is a generic 2-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS3202 supports several high-speed data protocols with a differential amplitude of <1800 mVpp and a common mode voltage of < 2 V, as with USB 3.1 and DisplayPort 1.2. The device has one select input (SEL) pin that can be controlled by an available GPIO pin within a system or from a microcontroller.

The HD3SS3202 with its adaptive common mode tracking technology can support applications where the common mode is different between the RX and TX pair. The two USB3.1 Type C connector applications show both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 capacitors are the preferred option to provide AC coupling; 0402 size capacitors also work. Avoid the capacitors greater than 0402 and C-packs. When placing AC coupling capacitors, symmetric placement is best. The designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board.

The AC coupling capacitors have several placement options. Because the HD3SS3202 requires a bias voltage, the designer must place the capacitors on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. 図 5 shows a few placement options. The coupling capacitors are placed between the HD3SS3202 and endpoint. In this situation, the HD3SS3202 is biased by the system/host controller.

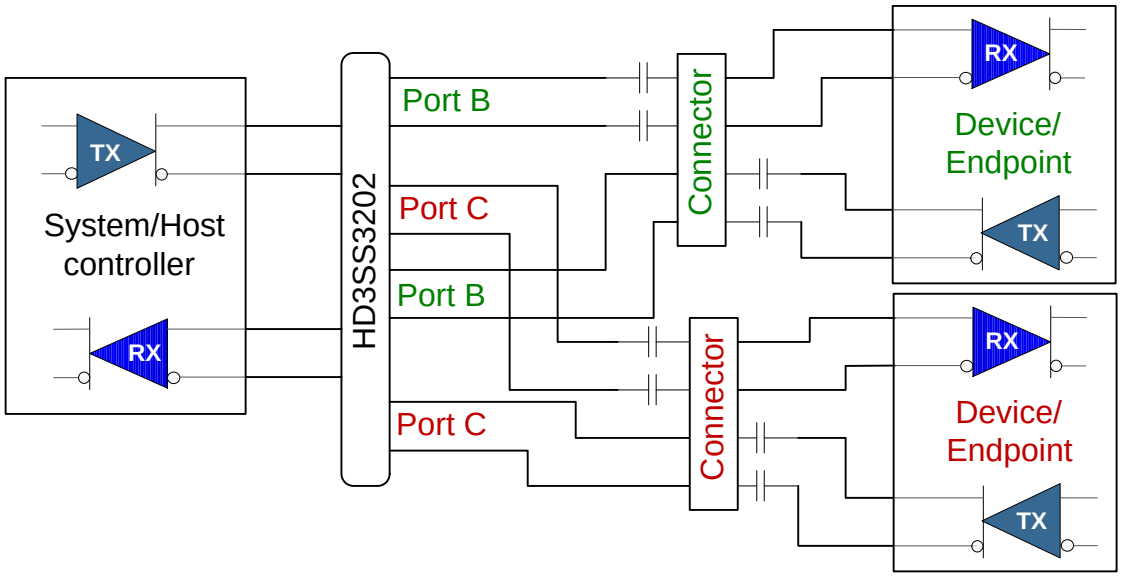


図 5. AC Coupling Capacitors between HD3SS3202 TX and Endpoint TX

Application Information (continued)

In 図 6, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on top is biased by the endpoint and the lower switch is biased by the host controller.

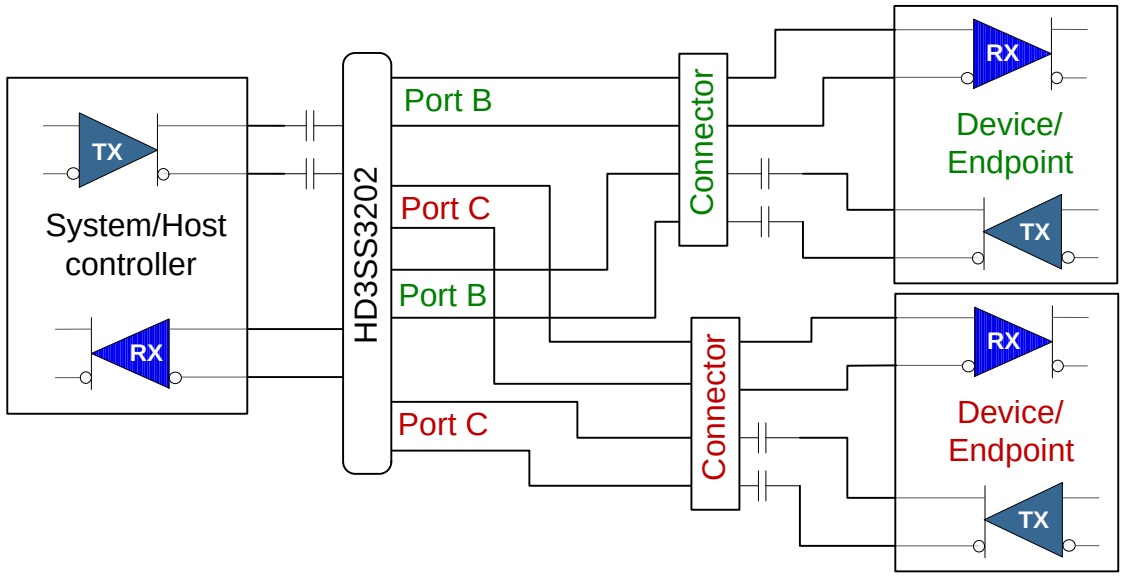
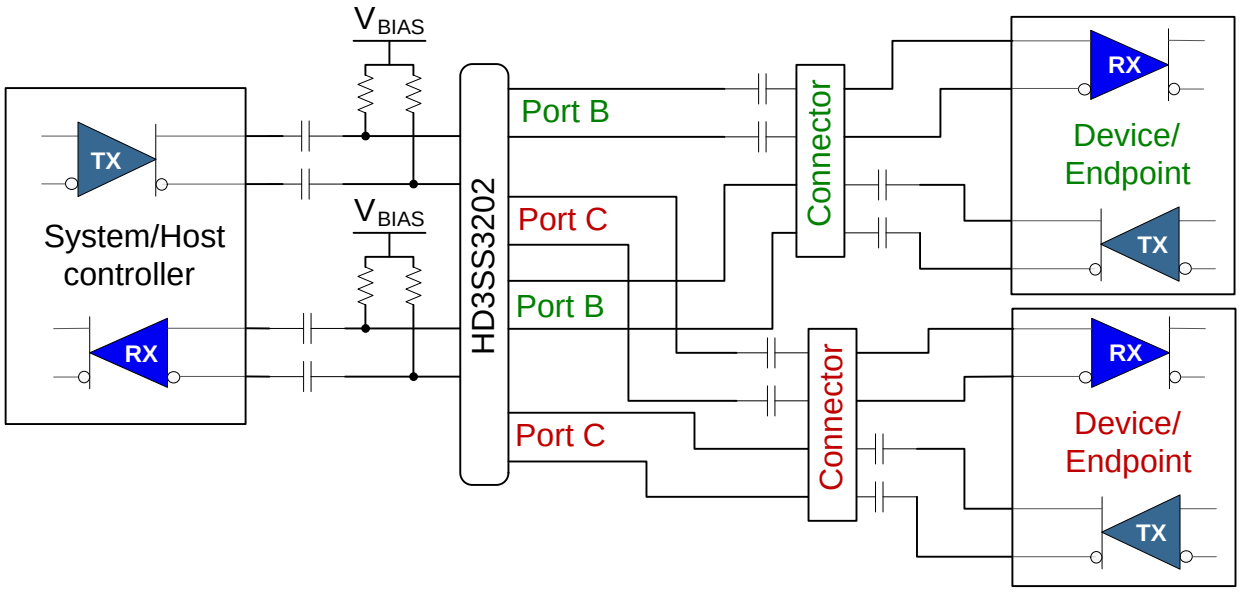


図 6. AC Coupling Capacitors on Host TX and Endpoint TX

If the common mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in 図 7). A biasing voltage of < 2 V is required in this case.



V_{BIAS} can be GND

Capacitor and resistor values depend upon application.

図 7. AC Coupling Capacitors on Both Sides of Switch

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Application Information (continued)

The HD3SS3202 can be used with the USB Type C connector to support the connector's flip ability. 図 8 provides the generic location for the AC coupling capacitors for this application.

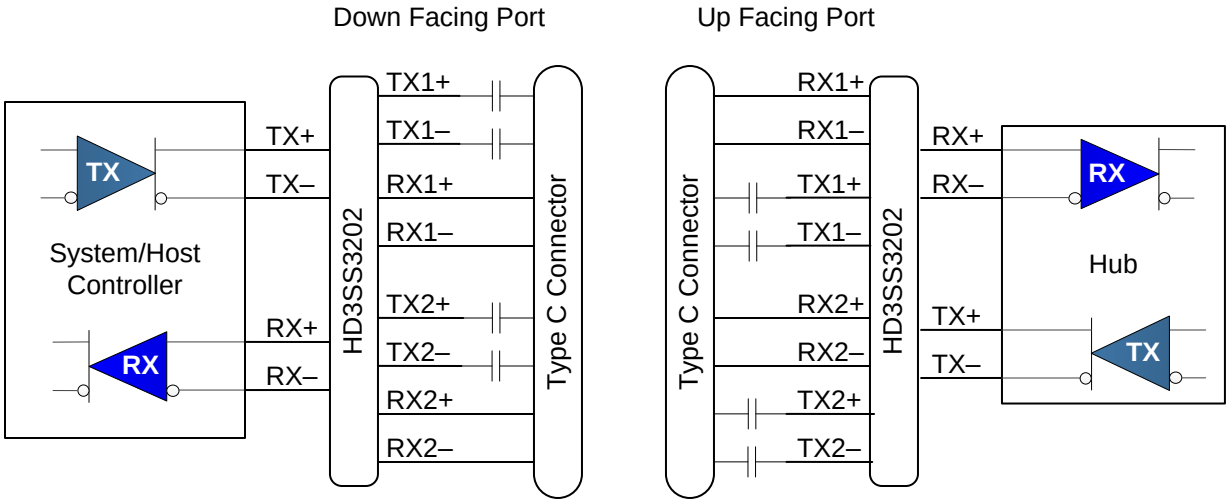

図 8. AC Coupling Capacitors for USB Type C

9.2 Typical Applications

9.2.1 Down Facing Port for USB3.1 Type C

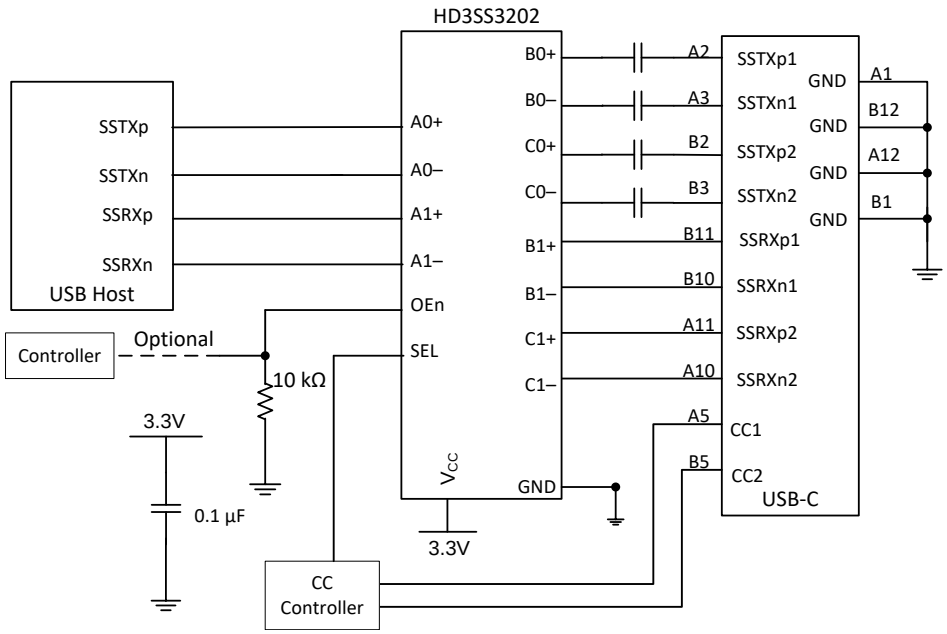

図 9. Down Facing Port for USB3.1 Type C Connector

9.2.1.1 Design Requirements

The HD3SS3202 can be designed into many different applications. All the applications have certain requirements for the system to work properly. The HD3SS3202 requires 3.3-V ±10% V_{CC} rail. The OEn pin must be low for device to work; otherwise, it disables the outputs. This pin can be driven by a processor. The expectation is that one side of the device has AC coupling capacitors. 表 2 provides information on expected values to perform properly.

表 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
AXp/n, BXp/n, CXp/n CM input voltage	0 to 2 V
Control/OEn pin max voltage for low	0.8 V
Control/OEn pin min voltage for high	2.0 V
AC coupling capacitor	75 nF to 265 nF.
R_{BIAS} (図 9) when needed	100 kΩ

9.2.1.2 Detailed Design Procedure

The HD3SS3202 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. The device can support 1 to 2 inches of board trace and a connector on either end.

To design in the HD3SS3202, the designer needs to understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Depending upon the application, determine the best place to put the 100-nF coupling capacitor.
- Provide a control signal for the SEL and OEn pins. It may be necessary to include a 0.01µF to GND on each of these pins to help with noise immunity.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground

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9.2.1.3 Application Curves

図 10 shows the eye at the input of the HD3SS3202 and 図 11 at the output of the HD3SS3202.

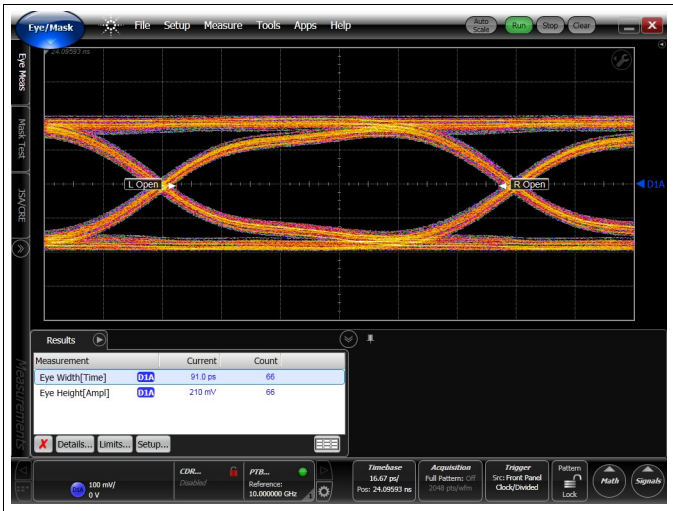

図 10. Source 10 Gbps Eye Diagram

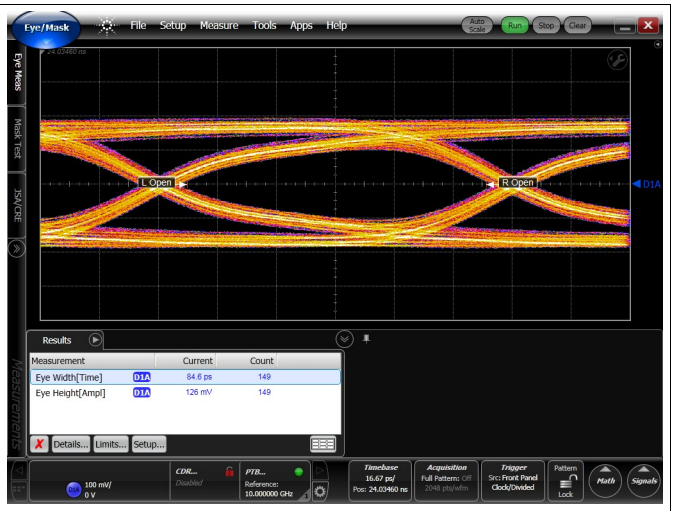

図 11. HD3SS3202 10 Gbps Output Eye Diagram

9.3 Systems Examples

9.3.1 Up Facing Port for USB3.1 Type C

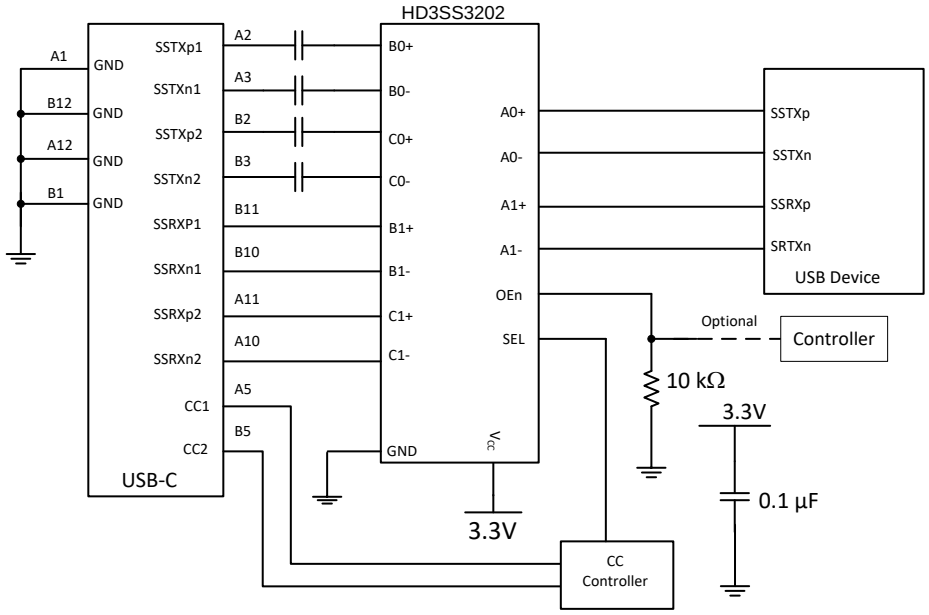

図 12. Up Facing Port for USB3.1 USB Type-C Connector

Systems Examples (continued)

9.3.2 PCIE/USB

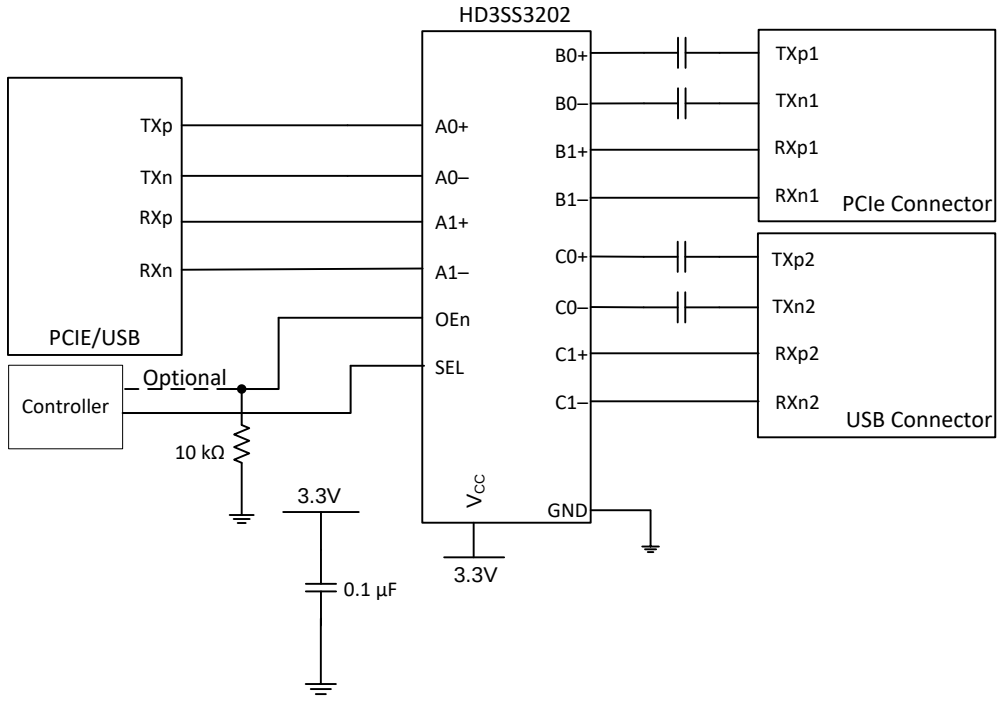

図 13. PCIE Motherboard

9.3.3 PCIE/eSATA

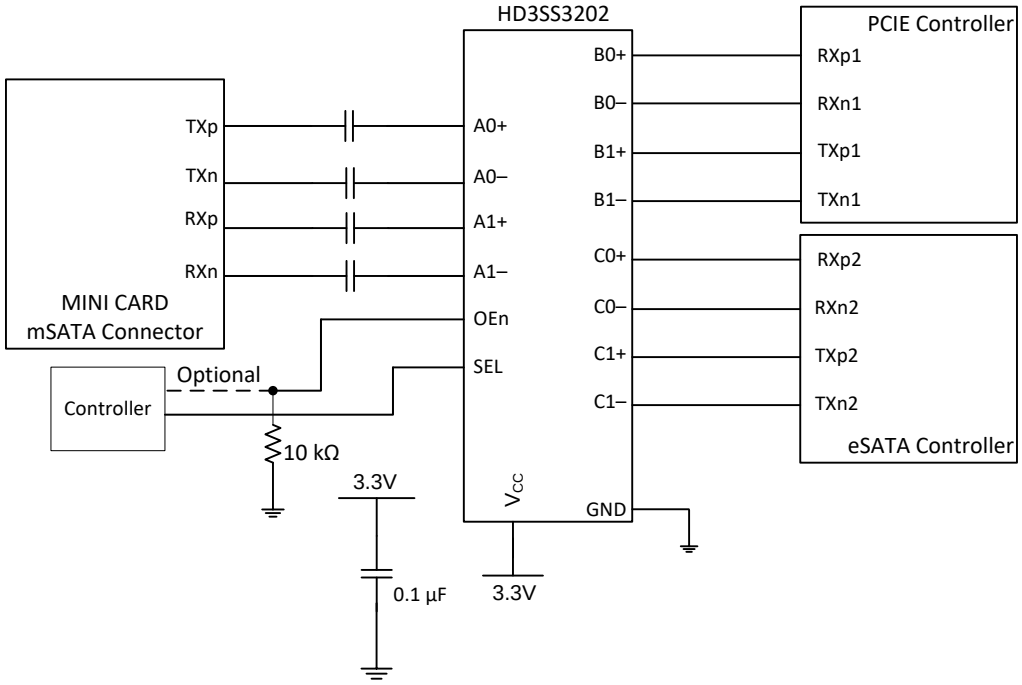

図 14. PCIE and eSATA Combo

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Systems Examples (continued)

9.3.4 USB/eSATA

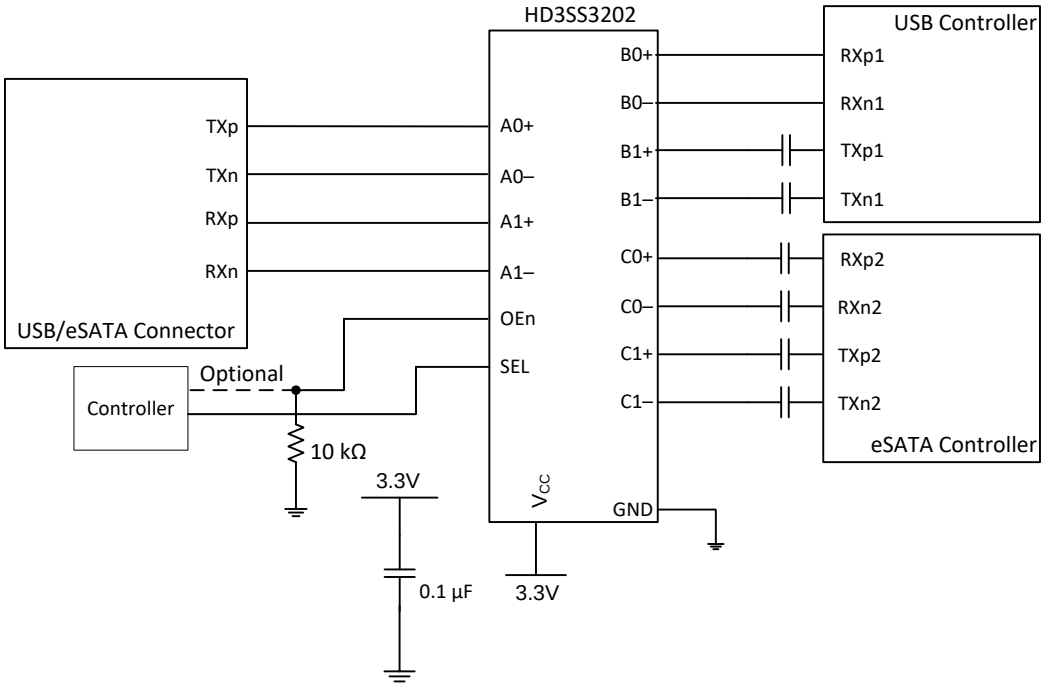

図 15. eSATA and USB 3.1 Combo Connector

9.3.5 MIPI Camera Serial Interface

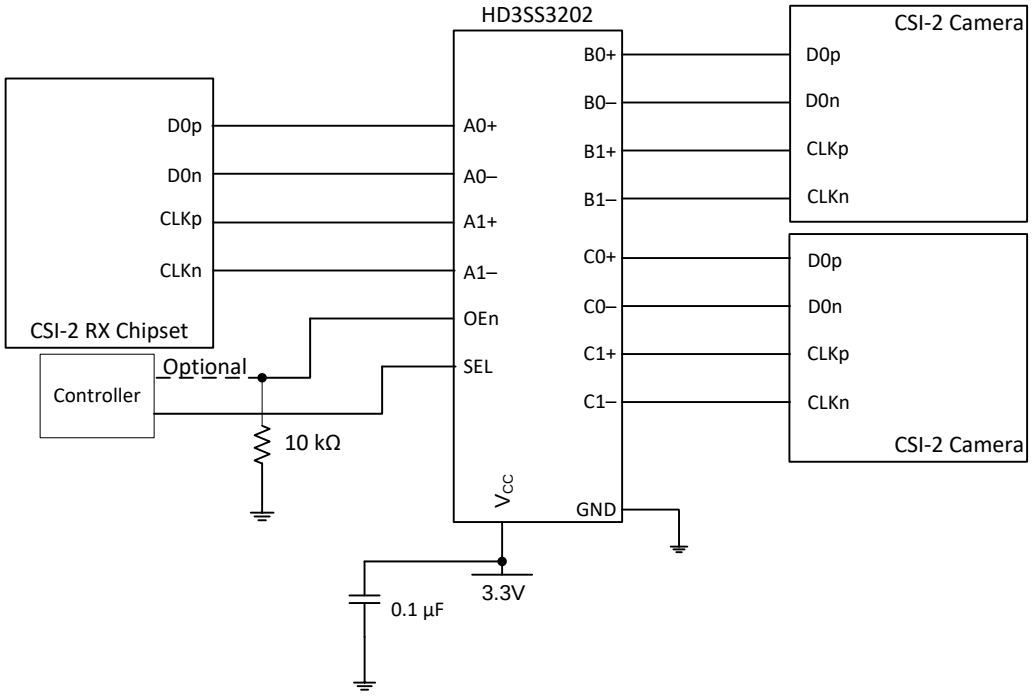

図 16. CSI Camera Array

10 Power Supply Recommendations

The HD3SS3202 does not require a power supply sequence. TI recommends placing a 100nF de-coupling capacitor at the device V_{CC} near the pin.

11 Layout

11.1 Layout Guidelines

11.2 Layout Example

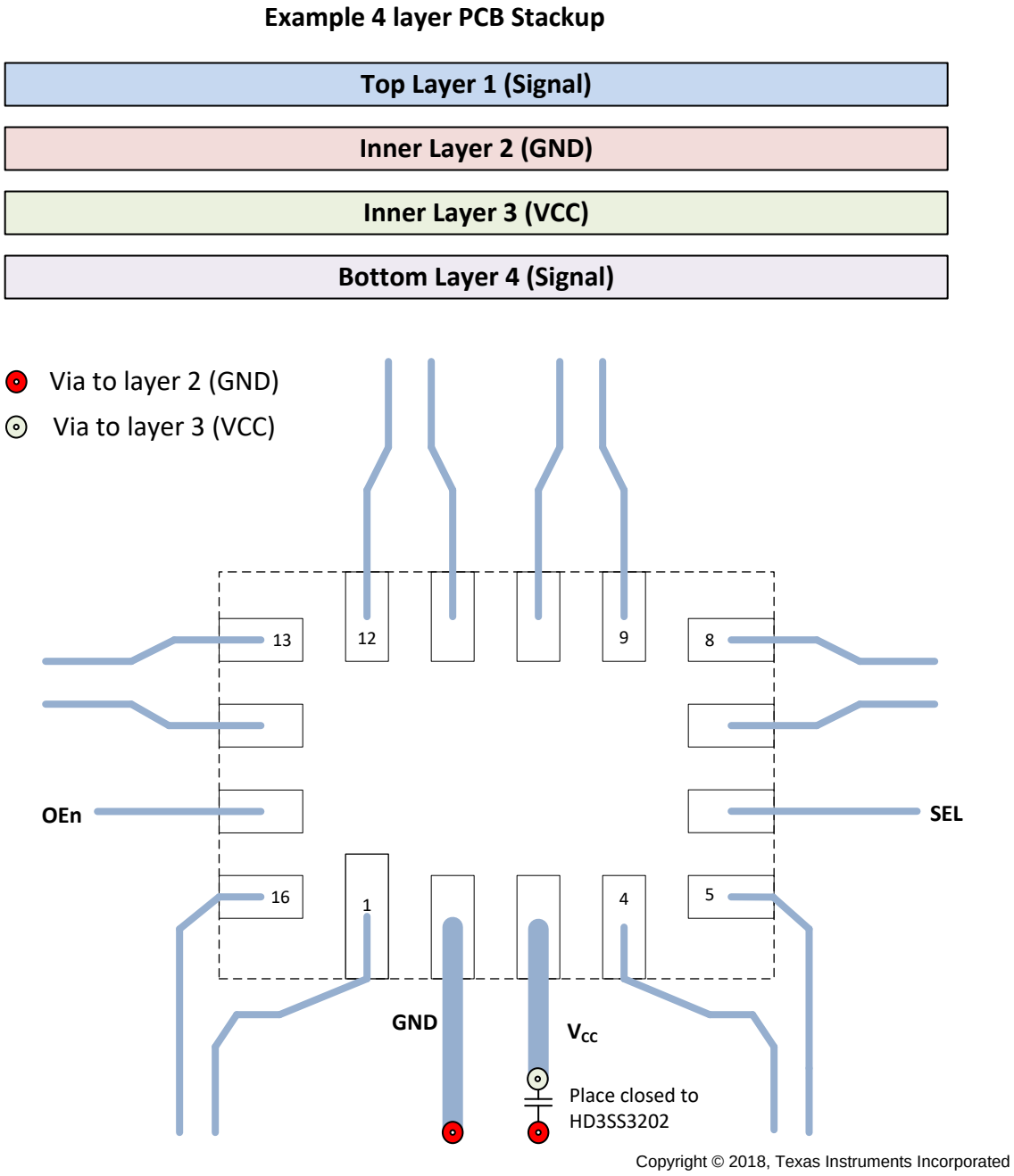

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図 17. HD3SS3202 Basic Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

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12.2 コミュニティ・リソース

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12.3 商標

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12.4 静電気放電に関する注意事項

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS3202IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3202	Samples
HD3SS3202IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3202	Samples
HD3SS3202RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3202	Samples
HD3SS3202RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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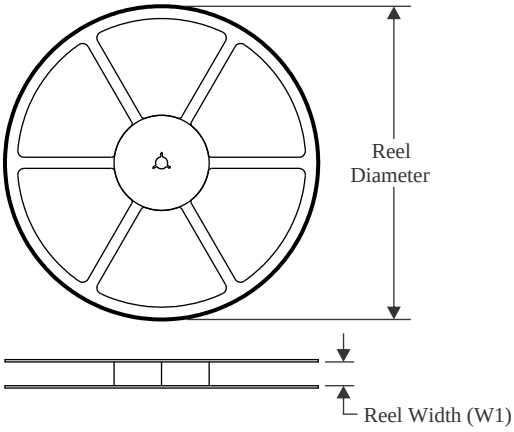
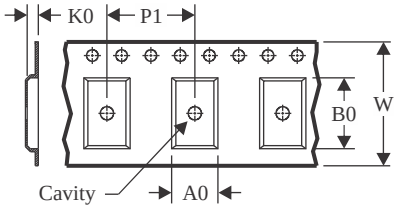
TAPE AND REEL INFORMATION

REEL DIMENSIONS

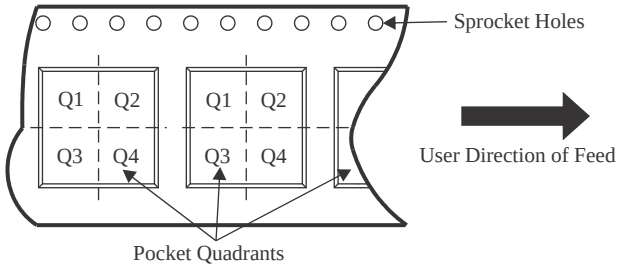


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

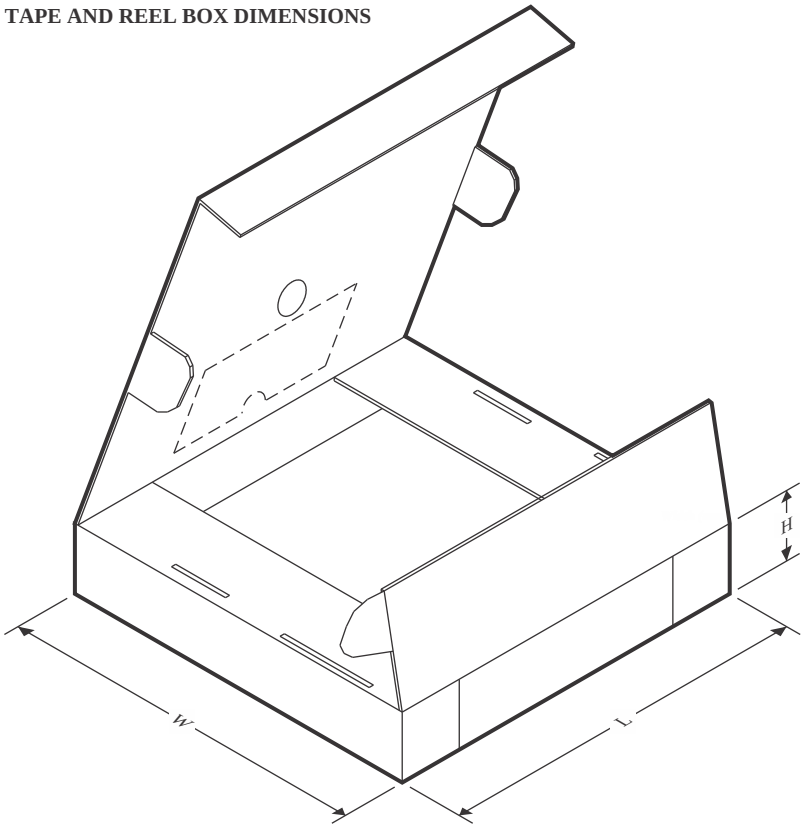
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3202IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
HD3SS3202RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

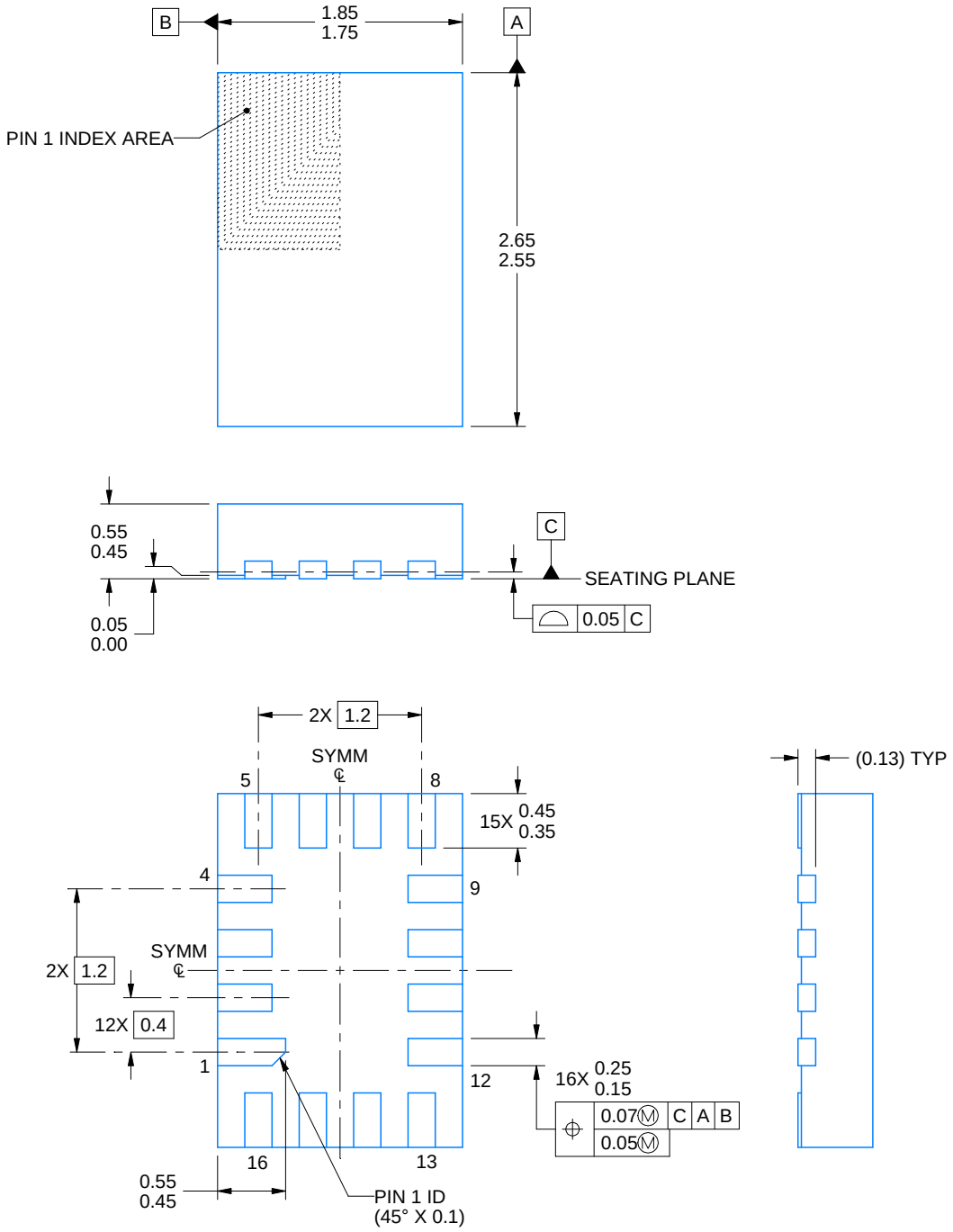
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3202IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
HD3SS3202IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
HD3SS3202RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
HD3SS3202RSVT	UQFN	RSV	16	250	189.0	185.0	36.0

RSV0016A

PACKAGE OUTLINE

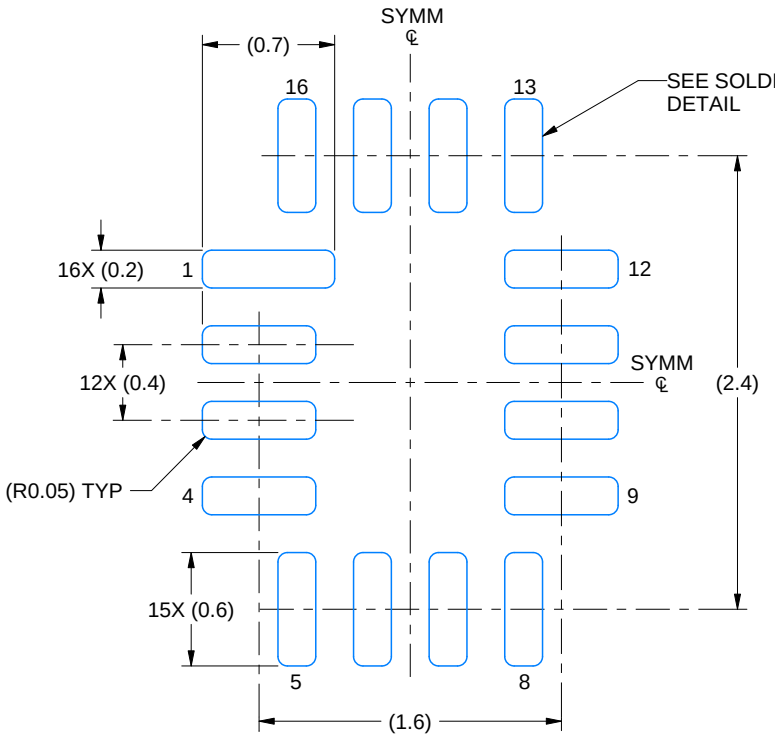
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

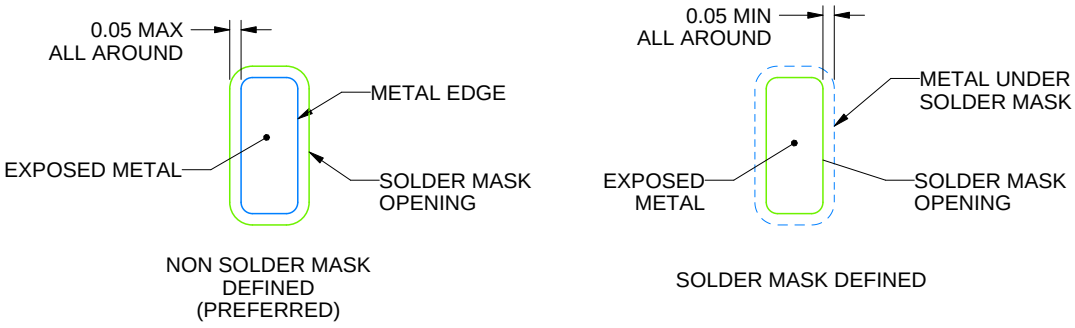


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

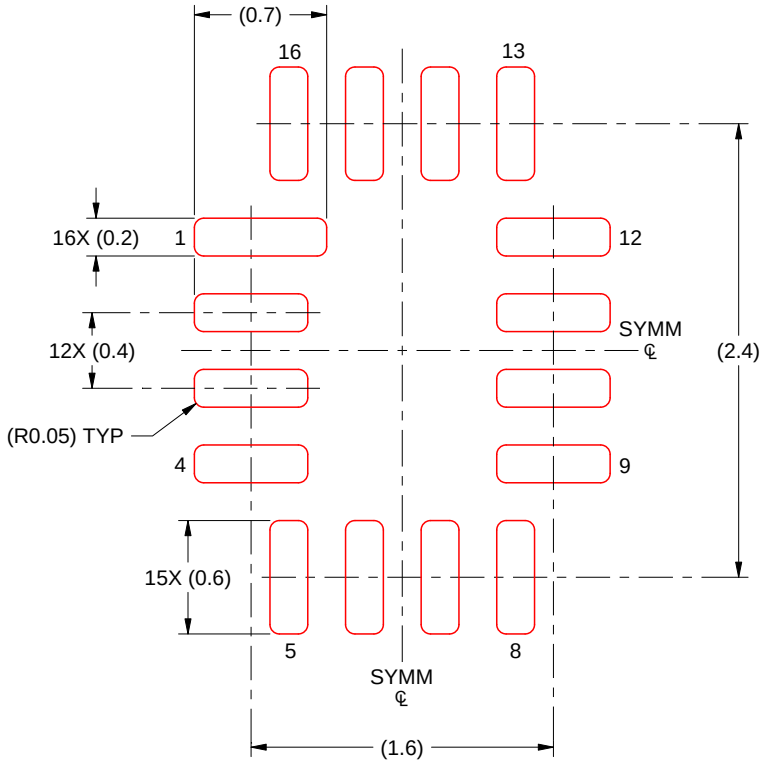


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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