INA114 高精度計測アンプ

1 特長

- 低いオフセット電圧：高ゲインの場合最大 50µV
- 低いドリフト：高ゲインの場合最大 0.3µV/℃
- 低い入力バイアス電流：最大 2nA
- 大きい同相除去：115dB 以上
- 入力過電圧保護回路：±40V
- 幅広い電源電圧範囲：±2.25V～±18V
- パッケージ：PDIP-8 および SOIC-16

2 アプリケーション

- 外科用機器
- アクチュエータ
- マルチファンクション リレー
- 列車制御 / 管理
- 路側信号伝送 / 制御

3 概要

INA114 は、精度の優れた低消費電力の汎用計装アンプです。本デバイスは、用途が広い 3 オペアンプ設計を採用しており、サイズが小型であるため、広範なアプリケーションに非常に適しています。

単一の外付け抵抗により、1～10,000 の範囲で任意のゲインを設定できます。内部入力保護機能は、損傷なしに ±40V まで耐えます。

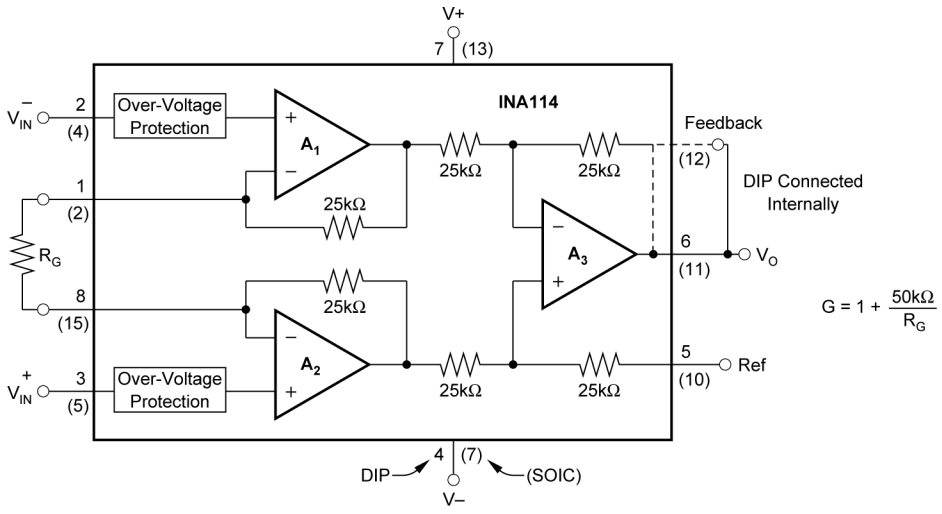
INA114 はレーザー トリムにより、非常に低いオフセット電圧 (50µV) と低ドリフト係数 (0.3µV/℃)、高い同相除去 (G = 1000 で 115dB) を実現しています。このデバイスは最低 ±2.25V の電源で動作するため、バッテリ駆動および 5V 単一電源のシステムで使用できます。

INA114 は 8 ピン PDIP および 16 ピン SOIC 表面実装パッケージで供給されます。どちらも、動作温度範囲の仕様は -40℃～+85℃です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
INA114	P (PDIP、8)	9.81mm × 9.43mm
	DW (SOIC、16)	10.3mm × 10.3mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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4 Pin Configuration and Functions

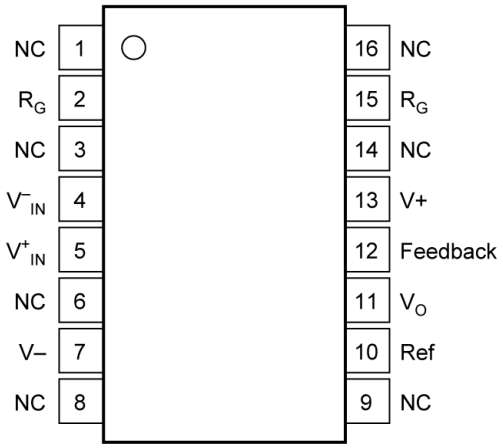


図 4-1. DW Package, 16-Pin SOIC (Top View)

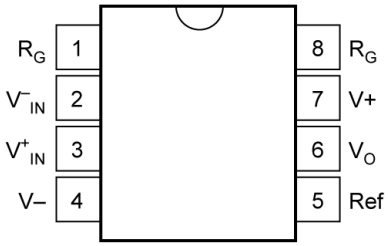


図 4-2. P Package, 8-Pin PDIP (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$		36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	–18	18	V
	Signal input pins		–40	40	V
V_O	Signal output voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
I_S	Output short-circuit (to $V_S/2$)		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$	4.5	36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	±2.25	±18	
T_A	Specified temperature		–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA114		UNIT
		DW (SOIC)	P (PDIP)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage	RTI	INA114BP, BU			±10 + 20/G	±50 + 150/G	µV
			INA114AP, AU			±25 + 30/G	±125 + 500/G	
	Offset voltage drift	T_A = –40°C to +85°C, RTI	INA114BP, BU			±0.1 + 0.5/G	±0.3 + 5/G	µV/°C
			INA114AP, AU			±0.25 + 5/G	±1 + 10/G	
	Long-term stability					±0.2 + 0.5/G		µV/mo
	Differential impedance					100 || 6		GΩ || pF
	Common-mode impedance					100 || 6		GΩ || pF
	Operating input voltage				(V–) + 4		(V+) – 4	V
PSRR	Power-supply rejection ratio	RTI, ±2.25V to ±18V				0.5 + 2/G	3 + 10/G	µV/V
CMRR	Common-mode rejection ratio	At dc to 60Hz, RTI, V_{CM} = ±10V, ΔR_S = 1kΩ	G = 1	INA114BP, BU	80	96		dB
				INA114AP, AU	75	90		dB
			G = 10	INA114BP, BU	96	115		
				INA114AP, AU	90	106		
			G = 100	INA114BP, BU	110	120		
				INA114AP, AU	106	110		
			G = 1000	INA114BP, BU	115	120		
				INA114AP, AU	106	110		
BIAS CURRENT								
I_B	Input bias current	V_{CM} = V_S / 2	INA114BP, BU			±0.5	±2	nA
			INA114AP, AU			±0.5	±5	
	Input bias current drift	T_A = –40°C to +85°C	INA114BP, BU			±8		pA/°C
			INA114AP, AU			±8		
I_{OS}	Input offset current	V_{CM} = V_S / 2	INA114BP, BU			±0.5	±2	nA
			INA114AP, AU			±0.5	±5	
	Input offset current drift	T_A = –40°C to +85°C	INA114BP, BU			±8		pA/°C
			INA114AP, AU			±8		
NOISE VOLTAGE								
	Voltage noise	G = 1000, R_S = 0Ω	f = 10Hz			15		nV/√Hz
			f = 100Hz			11		
			f = 1kHz			11		
			f_B = 0.1Hz to 10Hz			0.4		μV_{PP}
	Noise current	f = 10Hz				0.4		pA/√Hz
		f = 1kHz				0.2		pA/√Hz
		f_B = 0.1Hz to 10Hz				18		pA_{PP}

5.5 Electrical Characteristics (続き)

at T_A = 25°C, V_S = ±15V, R_L = 2kΩ, V_{REF} = 0V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
GAIN								
G	Gain equation					1 + (50kΩ / R_G)		V/V
	Range of gain				1		10000	V/V
GE	Gain error	V_O = ±10V, G = 1				±0.01	±0.05	%
		V_O = ±10V	G = 10	INA114BP, BU		±0.02	±0.4	
				INA114AP, AU		±0.02	±0.5	
			G = 100	INA114BP, BU		±0.05	±0.5	
				INA114AP, AU		±0.05	±0.7	
			G = 1000	INA114BP, BU		±0.5	±1	
				INA114AP, AU		±0.5	±2	
	Gain drift					±2	±10	ppm/°C
		R_S = 50kΩ(1)				±25	±100	
	Gain nonlinearity	V_O = –10V to +10V	G = 1	INA114BP, BU		±0.0001	±0.001	% of FSR
				INA114AP, AU		±0.0001	±0.002	
			G = 10, 100	INA114BP, BU		±0.0005	±0.002	
				INA114AP, AU		±0.0005	±0.004	
			G = 1000	INA114BP, BU		±0.002	±0.01	
				INA114AP, AU		±0.002	±0.02	
OUTPUT								
	Output voltage	I_O = 5mA, T_A = –40°C to 85°C			(V–) +1.5		(V+) –1.5	V
			V_S = ±11.4V		(V–) + 1.4		(V+) – 1.4	
			V_S = ±2.25V		(V–) +1		(V+) – 1	
	Load capacitance stability					1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2				+20 / –15		mA
FREQUENCY RESPONSE								
BW	Bandwidth, –3dB	G = 1				1		MHz
		G = 10				100		kHz
		G = 100				10		
		G = 1000				1		
SR	Slew rate	G = 10, V_O = ±10V			0.3	0.6		V/µs
t_S	Settling time	0.01%, V_{STEP} = 10V	G = 1			18		µs
			G = 10			20		
			G = 100			120		
			G = 1000			1100		
	Overload recovery	50% overdrive				20		µs
POWER SUPPLY								
I_Q	Quiescent current	V_S = ±2.25V to ±18V, V_{IN} = 0V				±2.2	±3	mA

(1) Temperature coefficient of the "50kΩ" term in the gain equation.

5.6 Typical Characteristics

at T_A = +25°C, V_S = ±15V, G = 1V/V (unless otherwise noted)

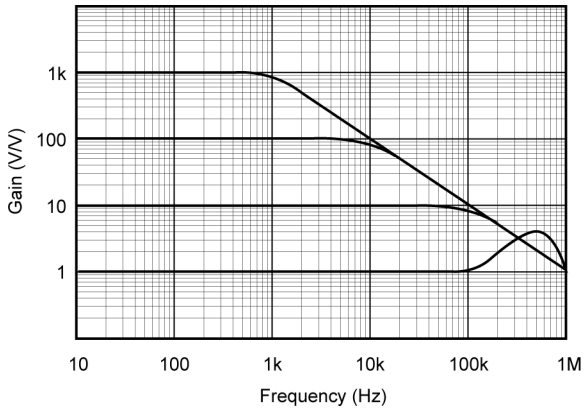


図 5-1. Gain vs Frequency

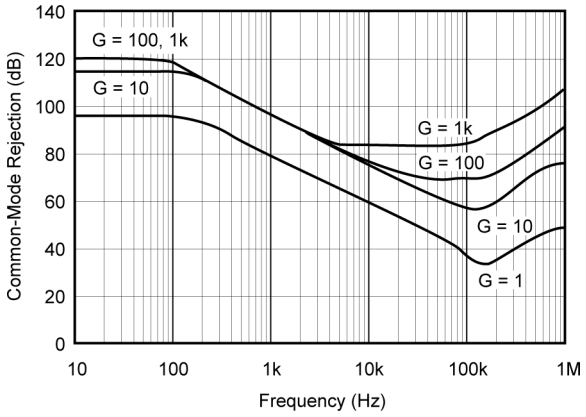


図 5-2. Common-mode Rejection vs Frequency

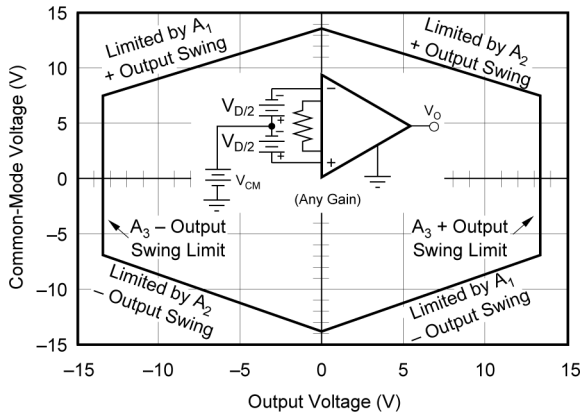


図 5-3. Input Common-mode Voltage Range vs Output Voltage

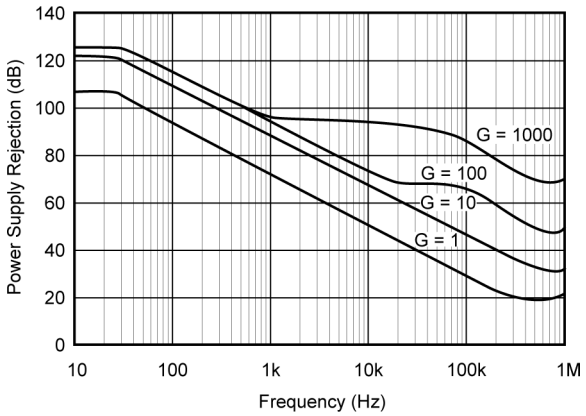


図 5-4. Positive Power Supply Rejection vs Frequency

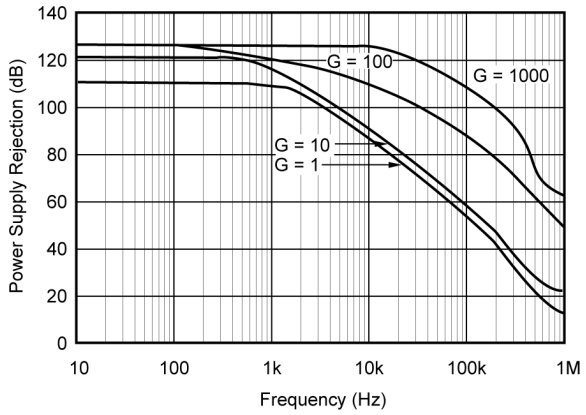


図 5-5. Negative Power Supply Rejection vs Frequency

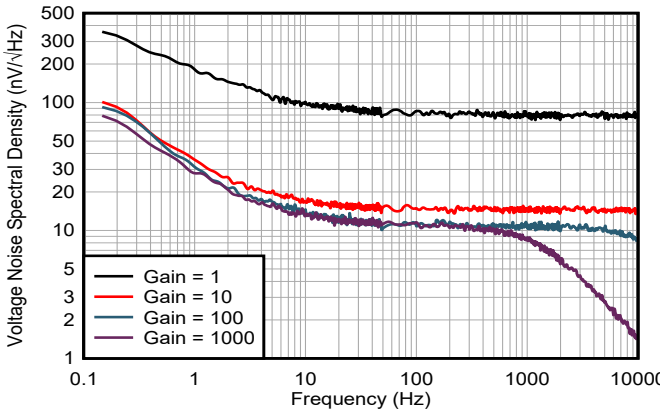


図 5-6. Input-Referred Noise Voltage vs Frequency

5.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, G = 1V/V (unless otherwise noted)

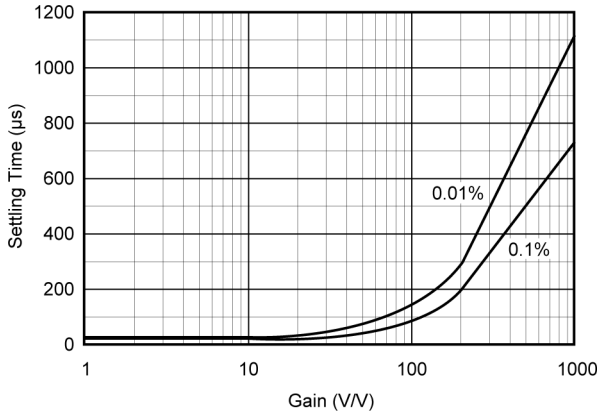


図 5-7. Settling Time vs Gain

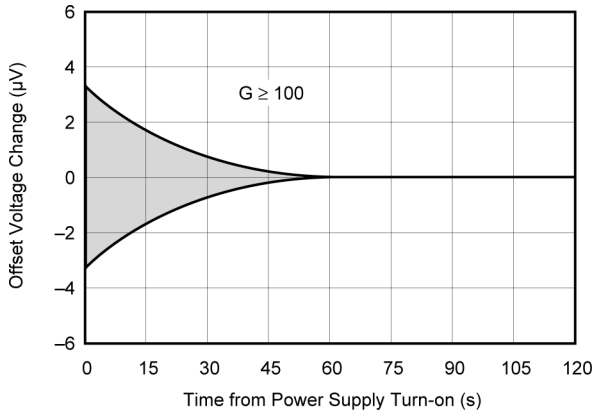


図 5-8. Offset Voltage Warm-up vs Time

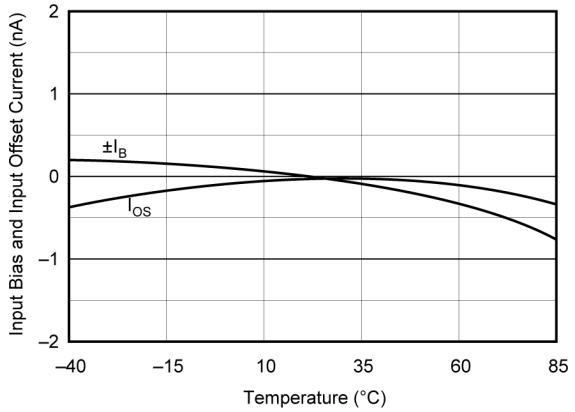


図 5-9. Input Bias and Input Offset Current vs Temperature

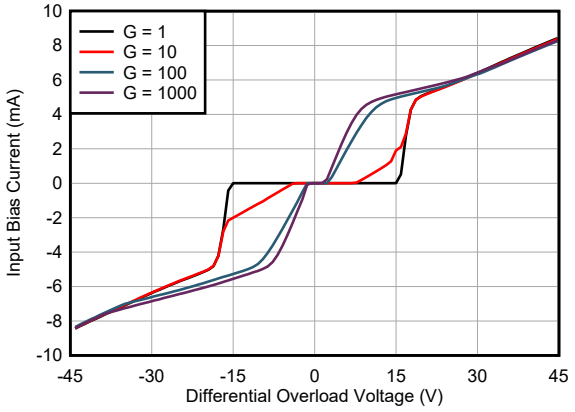


図 5-10. Input Bias Current vs Differential Input Voltage

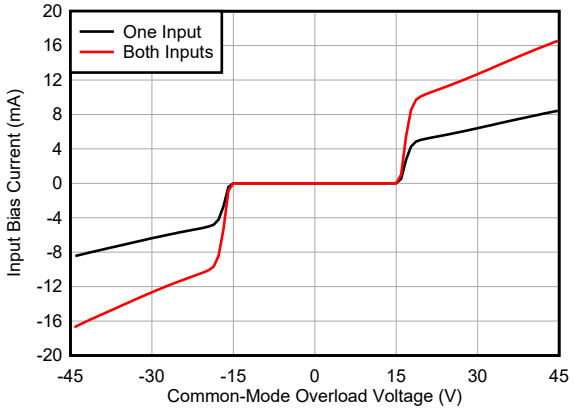


図 5-11. Input Bias Current vs Common-Mode Input Voltage

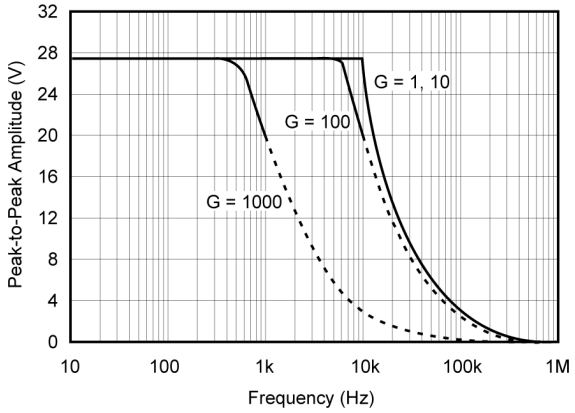


図 5-12. Maximum Output Swing vs Frequency

5.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, G = 1V/V (unless otherwise noted)

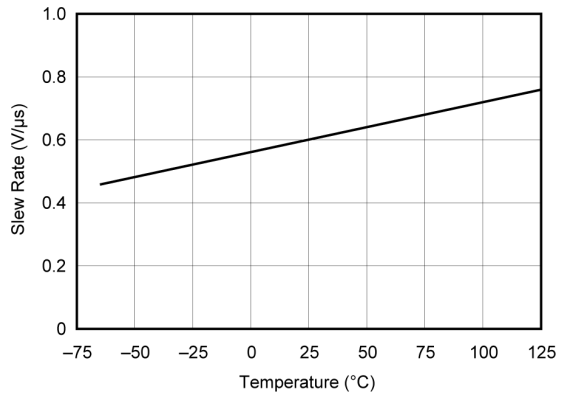


図 5-13. Slew Rate vs Temperature

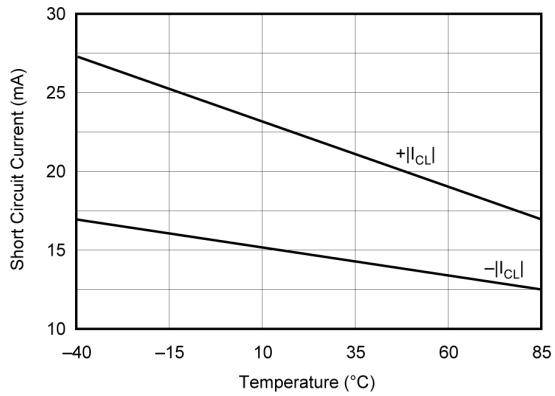


図 5-14. Output Current Limit vs Temperature

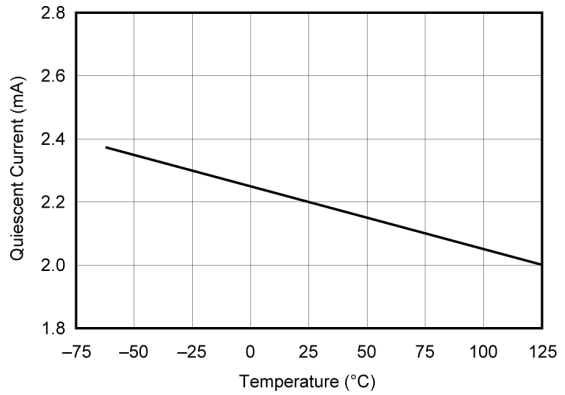


図 5-15. Quiescent Current vs Temperature

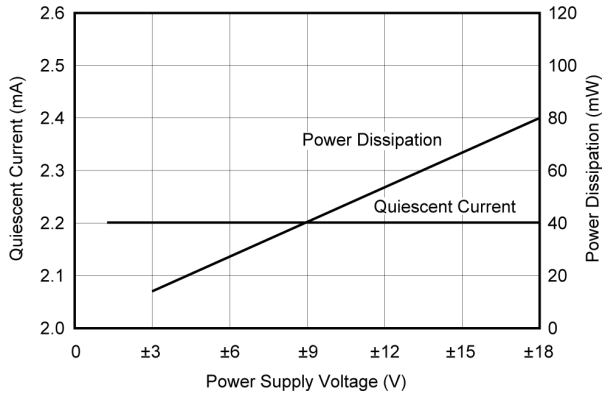
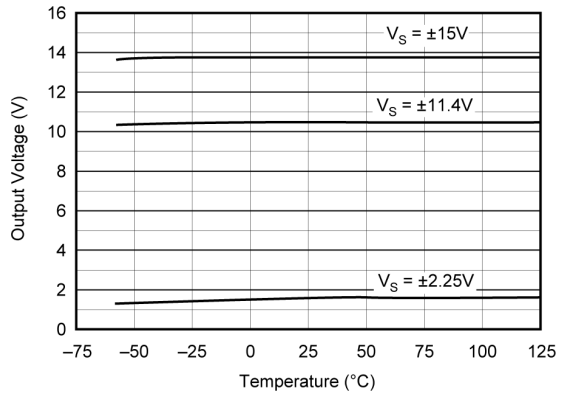
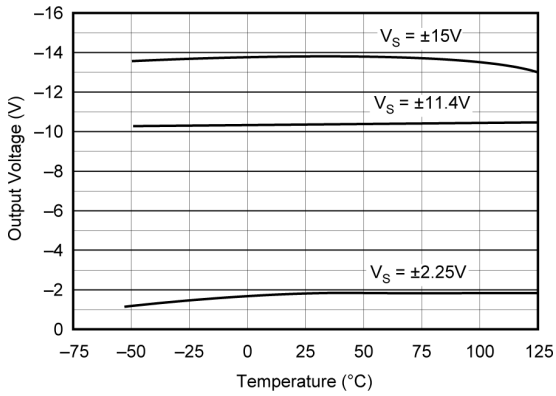


図 5-16. Quiescent Current and Power Dissipation vs Power Supply Voltage



R_L = 2kΩ

図 5-17. Positive Signal Swing vs Temperature



R_L = 2kΩ

図 5-18. Negative Signal Swing vs Temperature

5.6 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, G = 1V/V (unless otherwise noted)

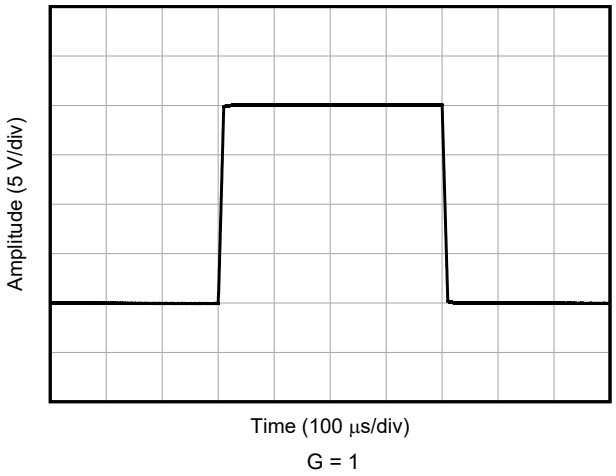


図 5-19. Large-Signal Response

図 5-20. Small-Signal Response

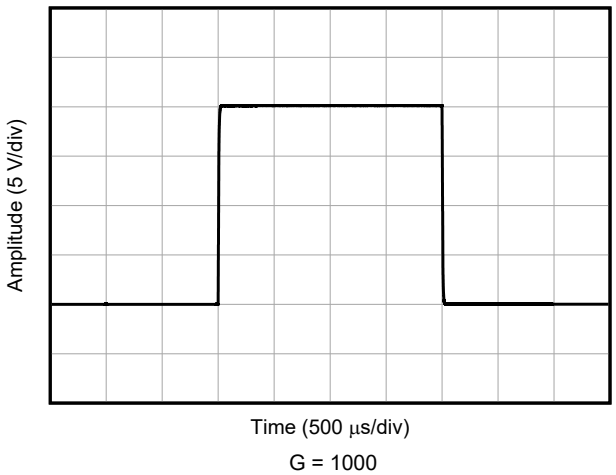


図 5-21. Large-Signal Response

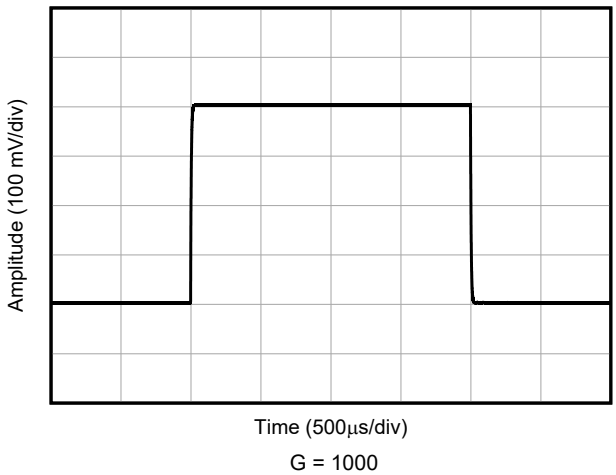


図 5-22. Small-Signal Response

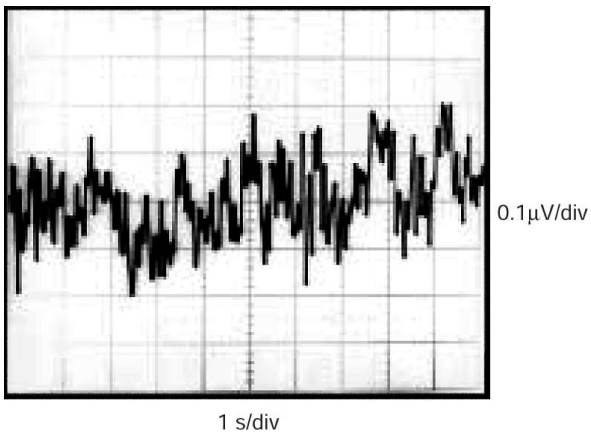


図 5-23. Input-Referred Noise, 0.1Hz to 10Hz

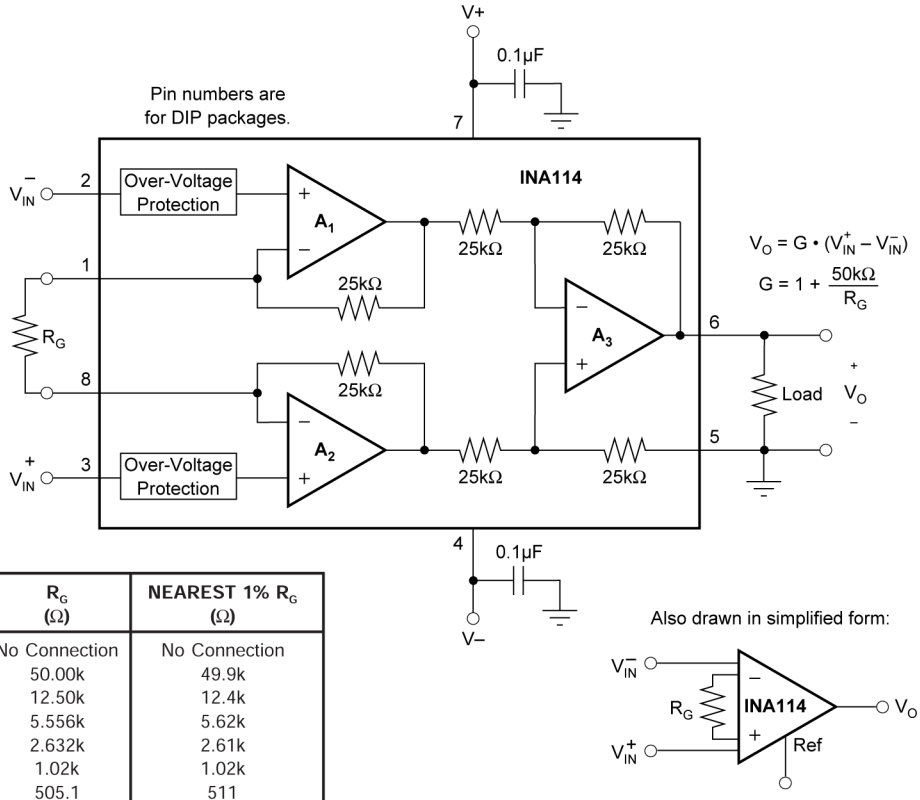
6 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

6.1 Application Information

図 6-1 shows the basic connections required for operation of the INA114. Applications with noisy or high-impedance power supplies can require decoupling capacitors close to the device pins as shown.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

図 6-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to provide good common-mode rejection. A resistance of 5Ω in series with the Ref pin causes a typical device to degrade to approximately 80dB CMR (G = 1).

6.1.1 Setting the Gain

Gain of the INA114 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50\ k\Omega}{R_G} \quad (1)$$

図 6-1 shows commonly used gains and resistor values.

The 50-kΩ term in 式 1 comes from the sum of the two internal feedback resistors. These resistors are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift is directly inferred from the gain 式 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

6.1.2 Noise Performance

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 can provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier can provide lower noise.

Low frequency noise of the INA114 is approximately $0.4\mu V_{PP}$ measured from 0.1Hz to 10Hz. This noise is approximately one-tenth the noise of *low noise* chopper-stabilized amplifiers.

6.1.3 Offset Trimming

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. 図 6-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is summed at the output. Maintain low impedance at this node to maintain good common-mode rejection by buffering trim voltage with an op amp as shown.

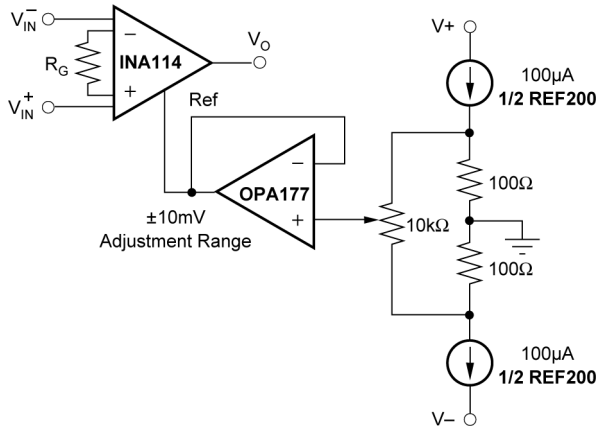


図 6-2. Optional Trimming of Output Offset Voltage.

6.1.4 Input Bias Current Return Path

The input impedance of the INA114 is extremely high-approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA, and can be either polarity as a result of cancellation circuitry. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. 図 6-3 shows various provisions for an input bias current path. Without a bias current return path, the inputs float to a potential that exceeds the common-mode range of the INA114 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see thermocouple example in 図 6-3). With higher source impedance, use two resistors to provide a balanced input, with the possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

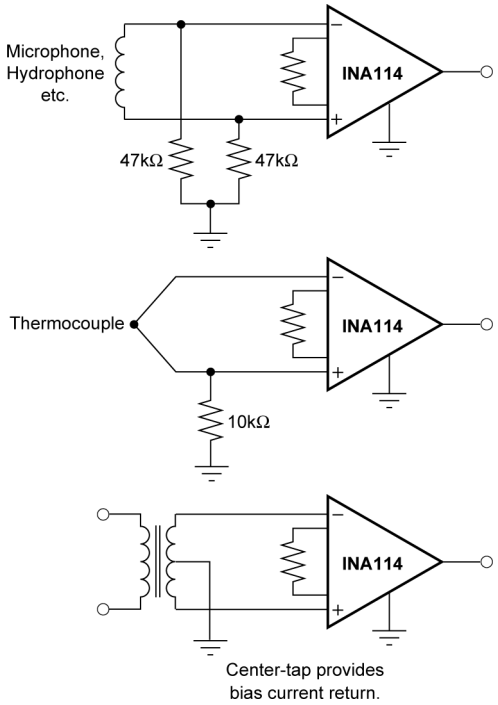


図 6-3. Providing an Input Common-Mode Current Path.

6.1.5 Input Common-Mode Range

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see typical characteristic curve *Input Common-Mode Range vs Output Voltage*.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. 図 6-4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve *Input Common-Mode Voltage Range vs Output Voltage*). If necessary, add gain after the INA114 to increase the voltage swing.

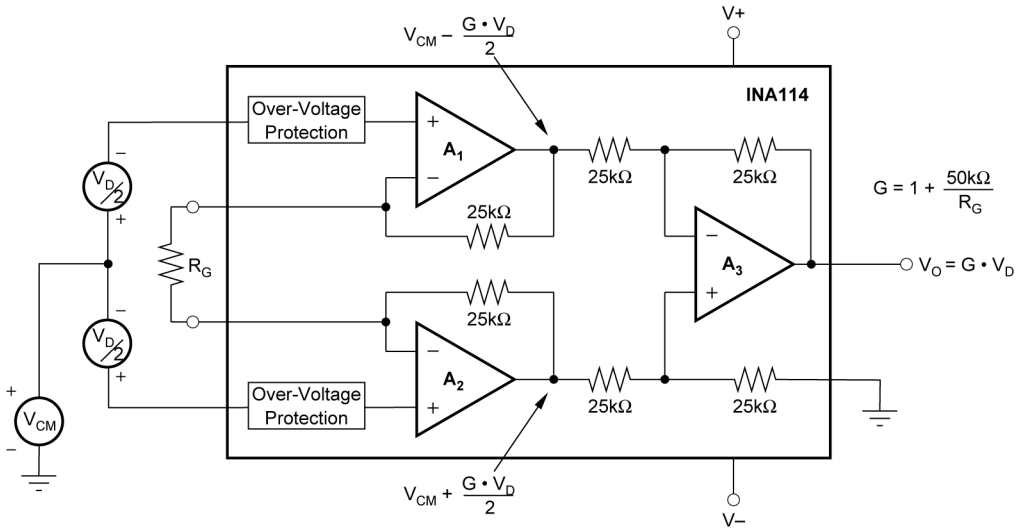


図 6-4. Voltage Swing of A_1 and A_2

Input overload often produces an output voltage that appears normal. For example, an input voltage of 20V on one input and 40V on the other input obviously exceeds the linear common-mode range of both input amplifiers. Both input amplifiers are saturated to nearly the same output voltage limit; therefore, the difference voltage measured by the output amplifier is near zero. The output of the INA114 is near 0V even though both inputs are overloaded.

6.1.6 Input Protection

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). Typical performance curve *Input Bias Current vs Common-Mode Input Voltage* shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

6.1.7 Output Voltage Sense (SOIC-16 Package Only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. 図 6-5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths can cause instability. This instability can be generally be eliminated with a high-frequency feedback path through C_1. Drive heavy loads or long lines by connecting a buffer inside the feedback path (see 図 6-6).

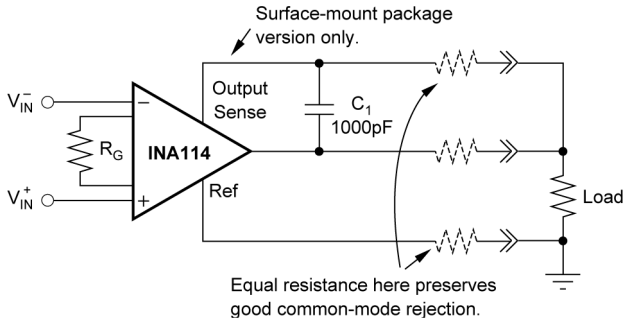


図 6-5. Remote Load and Ground Sensing

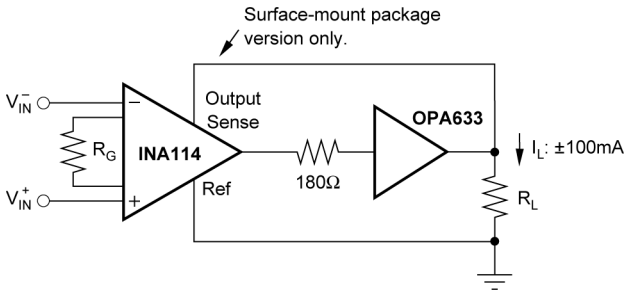


図 6-6. Buffered Output for Heavy Loads

7 Typical Applications

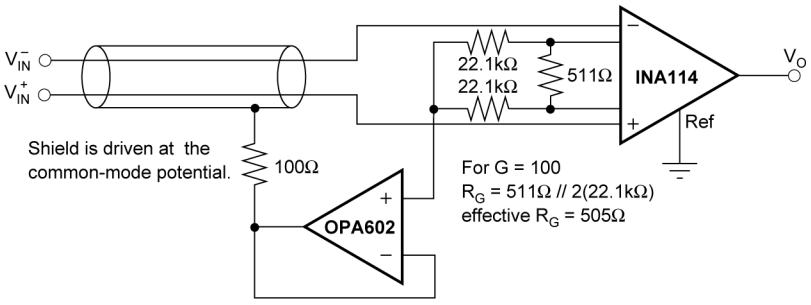


図 7-1. Shield Driver Circuit

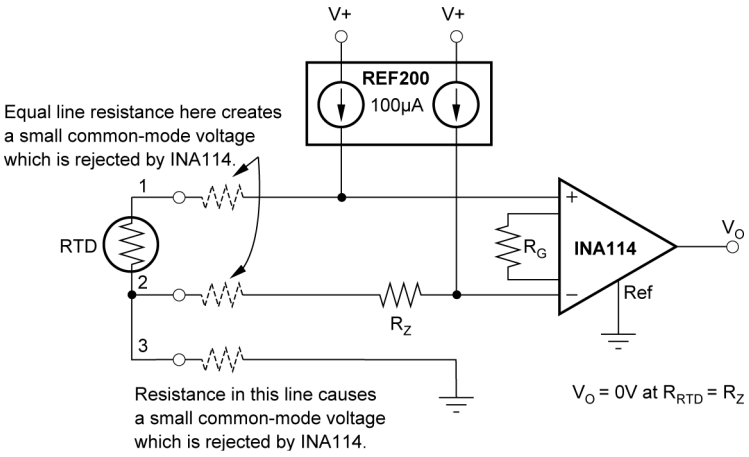
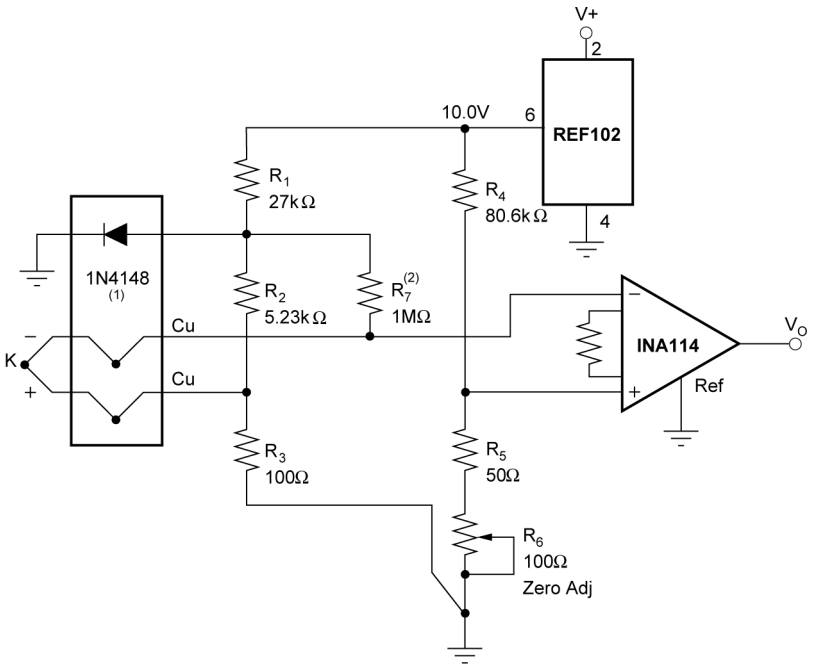


図 7-2. RTD Temperature Measurement Circuit



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200µA. (2) R_7 provides down-scale burn-out indication.

図 7-3. Thermocouple Amplifier with Cold Junction Compensation

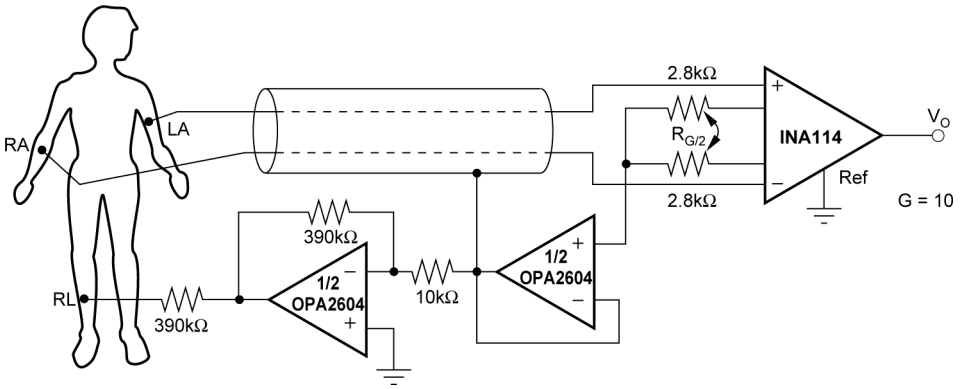


図 7-4. ECG Amplifier with Right-Leg Drive

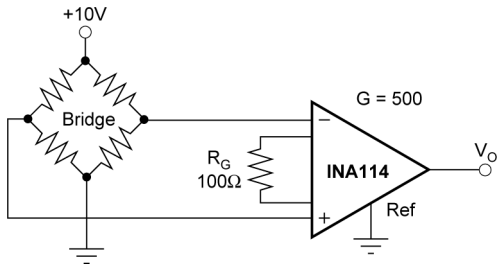


図 7-5. Bridge Transducer Amplifier

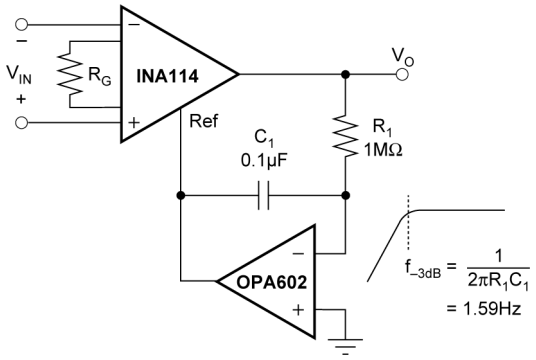
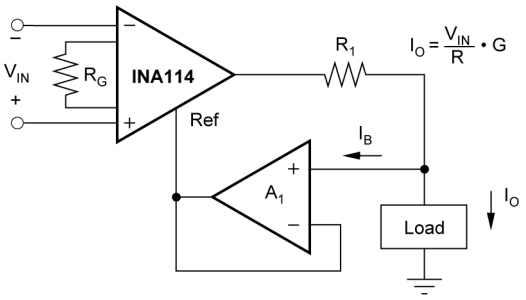


図 7-6. AC-Coupled Instrumentation Amplifier



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

図 7-7. Differential Voltage-to-Current Converter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 1998) to Revision A (January 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「ESD 定格」、「推奨動作条件」、「熱に関する情報」、「アプリケーションと実装」、「代表的なアプリケーション」、「デバイスおよびドキュメントのサポート 」、「メカニカル、パッケージ、および注文情報」の各セクションを追加	1
• データシート全体にわたって SOL パッケージ名を SOIC に変更	1
• 「特長」の「低オフセット電圧」と「低ドリフト」の箇条書き項目に「高ゲインの場合」を追加	1
• 「特長」で低ドリフトの箇条書き項目の値を 0.25µV/℃から 0.3µV/℃に変更	1
• 「アプリケーション」の箇条書き項目を更新	1
• Added symbols in *Absolute Maximum Ratings*	3
• Changed supply voltage to show dual supply and single supply in *Absolute Maximum Ratings*	3
• Changed "Input Voltage Range" to "Signal input pins" in *Absolute Maximum Ratings*	3
• Added signal output voltage to *Absolute Maximum Ratings*	3
• Changed output short-circuit from "ground" to "V_S / 2" in Absolute Maximum Ratings	3
• Added DW (SOIC) package ambient thermal resistance value	3
• Changed ambient thermal resistance value for P (PDIP) package from 80°C/W to 110.2°C/W	3
• Added symbols in *Electrical Characteristics*	4
• Changed offset voltage maximum value from ±50 + 100/G to ±50 + 150/G	4

- Changed "Offset Voltage vs Temperature" to "Offset voltage drift" 4
- Changed offset voltage drift test condition from $T_A = T_{MIN}$ to T_{MAX} to T_A = –40°C to +85°C 4
- Changed offset voltage drift maximum value from ±0.25 + 5/G to ±0.3 + 5/G 4
- Deleted safe input voltage from *Electrical Characteristics* 4
- Changed "Input Common-Mode Range" to "Operating input voltage" 4
- Changed "Offset Voltage vs Power Supply" to "Power-supply rejection ratio" 4
- Changed "Bias current vs Temperature" to "Input bias current drift" 4
- Added "T_A = –40°C to +85°C" test condition to input bias current drift 4
- Changed "Offset Current vs Temperature" to "Input offset current drift" 4
- Added "T_A = –40°C to +85°C" test condition to input offset current drift 4
- Added "V_O = ±10V" test condition to gain error 4
- Changed "Gain vs Temperature" to "Gain drift" 4
- Added "V_O = –10V to +10V" test condition to gain nonlinearity 4
- Changed output voltage values from ±13.5 (min) and ±13.7 (typ) to (V–) + 1.5 (min) and (V+) – 1.5 (max) 4
- Changed output voltage test condition from T_{MIN} to T_{MAX} to T_A = –40°C to +85°C 4
- Added output voltage test conditions for V_S = ±11.4V and V_S = ±2.25V 4
- Added V_{STEP} = 10V test condition to settling time 4
- Deleted power supply voltage range typical value of ±15V 4
- Moved voltage range, operating temperature range, and thermal resistance from *Electrical Characteristics* to *Recommended Operating Conditions* and *Thermal Information* 4
- Updated Figure 5-6, *Input-referred Noise Voltage vs Frequency* 6
- Updated Figure 5-10, *Input Bias Current vs Differential Input Voltage* 6
- Updated Figure 5-11, *Input Bias Current vs Common-Mode Input Voltage* 6
- Updated Figure 5-19 to Figure 22, Small- and Large-Signal Response plots 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA114AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114AP	Samples
INA114AU	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114AU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	INA114AU	Samples
INA114BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		INA114BP	Samples
INA114BU	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA114BU	Samples
INA114BU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA114BU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

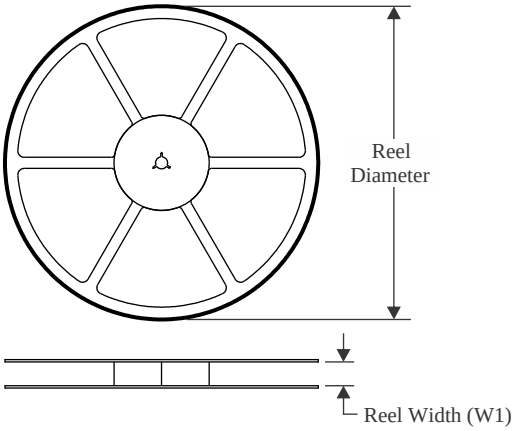
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

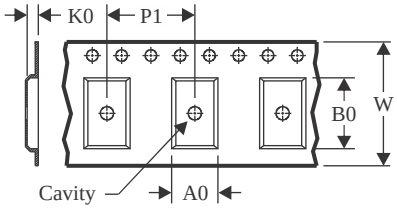
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

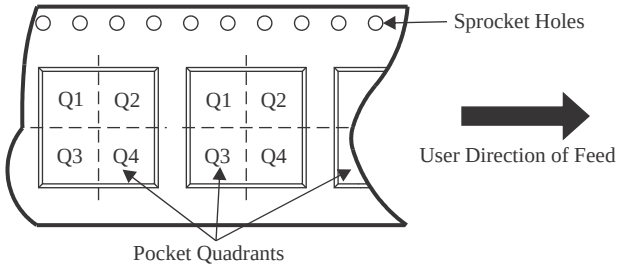


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

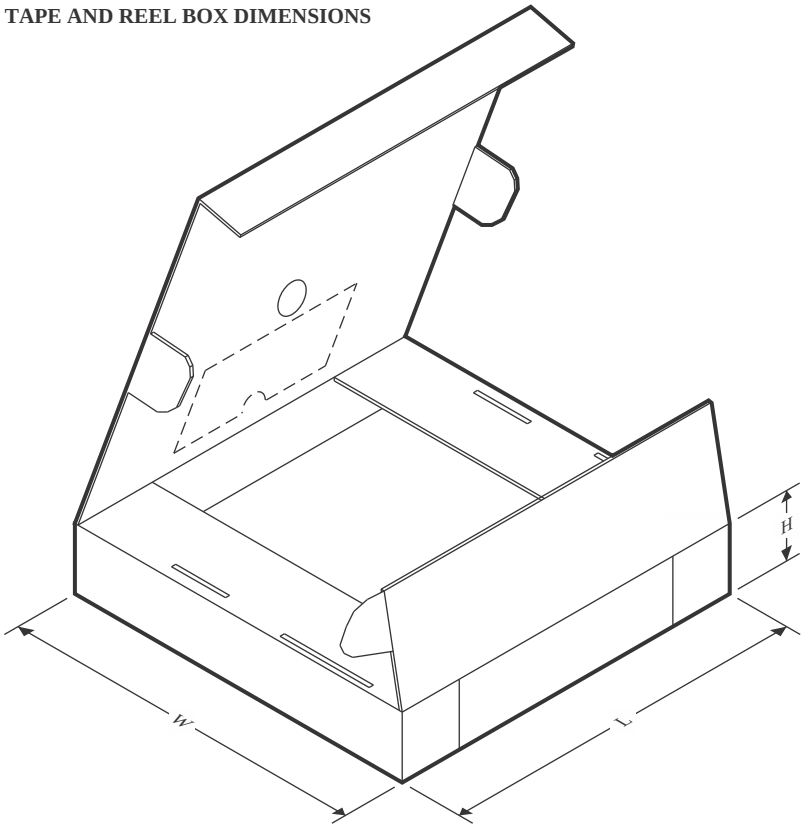
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA114AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA114BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

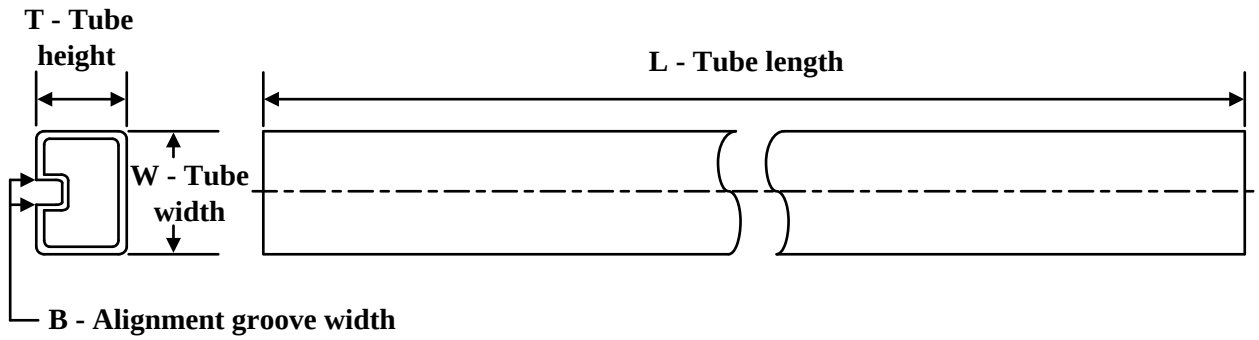
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA114AU/1K	SOIC	DW	16	1000	356.0	356.0	35.0
INA114BU/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA114AP	P	PDIP	8	50	506	13.97	11230	4.32
INA114AU	DW	SOIC	16	40	507	12.83	5080	6.6
INA114BP	P	PDIP	8	50	506	13.97	11230	4.32
INA114BU	DW	SOIC	16	40	507	12.83	5080	6.6

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