INA118 高精度、低消費電力計装アンプ

1 特長

- このデバイスには新しいバージョン INA818 が存在します
- 低いオフセット電圧:50µV (最大値)
- 低いドリフト:0.5µV/°C (最大値)
- 低い入力バイアス電流:5nA (最大値)
- 高い CMR:110dB (最小値)
- ±40V までの入力保護
- 広い電源電圧範囲:±2.25～±18V
- 低い静止電流:350µA
- パッケージ:8 ピンのプラスチック DIP、SO-8

2 アプリケーション

- 圧力トランスミッタ
- 温度トランスミッタ
- 重量計
- 心電図 (ECG)
- アナログ入力モジュール
- データ・アクイジション (DAQ)

3 概要

INA118 は、精度の優れた低消費電力の汎用計装アンプです。本デバイスは、用途が広い 3 オペアンプ設計を採用しており、サイズが小型であるため、広範なアプリケーションに非常に適しています。電流帰還入力回路により、高いゲインでも広い帯域幅が得られます (G = 100 で 70kHz)。

1 個の外付け抵抗で、1～10000 の任意のゲインを設定できます。内部入力保護機能は、損傷なしに ±40V まで耐えられます。

INA118 はレーザー・トリムにより、低いオフセット電圧 (50µV)、ドリフト係数 (0.5µV/°C)、高い同相信号除去比 (G = 1000 で 110dB) を実現しています。INA118 は、最低 ±2.25V の電源で動作し、静止電流がわずか 350µA であるため、バッテリ動作システムに非常に適しています。

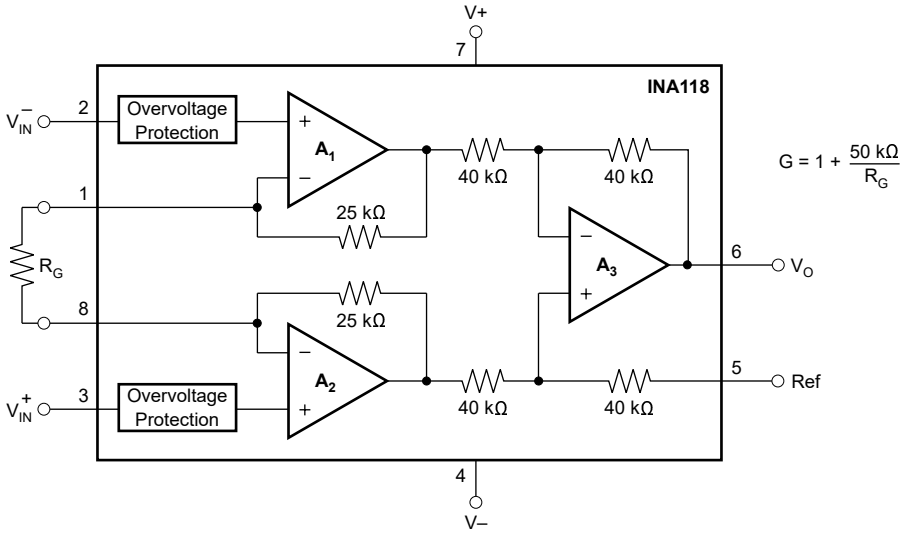
INA118 は 8 ピンのプラスチック DIP および SO-8 表面実装パッケージで供給され、-40°C～+85°Cの温度範囲で動作が規定されています。

アップグレードされた INA818 は、同じ静止電流で、より低い入力段オフセット電圧 (最大 35µV)、入力バイアス電流 (最大 0.5nA)、ノイズ (8nV/√Hz) を実現しています。テキサス・インスツルメンツの高精度計装アンプのラインナップについては、「デバイス比較表」を参照してください。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
INA118	SOIC (8)	3.91mm × 4.90mm
	PDIP (8)	6.35mm × 9.81mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2019) to Revision C (September 2022) **Page**

- ドキュメント全体を通して、最小電源電圧を ±1.35V から ±2.25V に、また 2.7V から 4.5V に変更 ... 1
- 「アプリケーション」セクションを www.tij.co.jp の最新の最終製品にリンクするよう変更 ... 1
- 「概略回路図」の抵抗を 60kΩ から 40kΩ に変更 ... 1
- Changed minimum and maximum input common-mode voltage from V^- + 1.1 V and V^+ – 1 V to V^- + 2 V and V^+ – 2 V respectively in *Recommended Operating Conditions* ... 5
- Changed minimum and maximum ambient temperature from –55°C and +150°C to –40°C and +125°C respectively in *Recommended Operating Conditions* ... 5
- Added V_{CM} = 0 V to test conditions below title in *Electrical Characteristics* ... 6
- Changed input offset voltage vs temperature test condition from $T_A = T_{MIN}$ to T_{MAX} to T_A = –40°C to +85°C in *Electrical Characteristics* ... 6
- Changed input offset voltage vs power supply test condition from V_S = ±1.35 V to ±18 V to V_S = ±2.25 V to ±18 V in *Electrical Characteristics* ... 6
- Changed high-side linear input voltage range from (V^+) – 1 V minimum and (V^+) – 0.65 V typical to (V^+) – 2 V minimum and (V^+) – 1.4 V typical in *Electrical Characteristics* ... 6
- Changed low-side linear input voltage range from (V^-) + 1.1 V minimum and (V^-) + 0.95 V typical to (V^-) + 2 V minimum and (V^-) + 1.2 V typical in *Electrical Characteristics* ... 6
- Added test condition of T_A = –40°C to +85°C to bias current vs temperature and offset current vs temperature in *Electrical Characteristics* ... 6
- Added test condition of T_A = –40°C to +85°C to gain vs temperature and 50-kΩ resistance vs temperature in *Electrical Characteristics* ... 6
- Changed single supply output voltage test condition from V_S = 2.7 V/0 V to V^+ = 4.5 V, V^- = 0 V in *Electrical Characteristics* ... 6
- Deleted power supply voltage range specification from *Electrical Characteristics* ... 6
- Deleted temperature range specifications from *Electrical Characteristics* ... 6
- Changed Figures 7-3, 7-4, 7-5, 7-6, 7-7, 7-8, 7-11, 7-12, 7-18, 7-19, and 7-20 in *Typical Characteristics* ... 8
- Changed FET transistor input current limit from approximately 1.5-5 mA to 6 mA in *Overview* ... 12
- Deleted internal node equations in *Overview* and *Functional Block Diagram* ... 12
- Changed schematic in *Functional Block Diagram* ... 12
- Changed linear input voltage range in *Input Common-Mode Range* and *Single-Supply Operation* ... 13
- Changed FET transistor input current limit from approximately 1.5-5 mA to 6 mA in *Input Protection* ... 13
- Changed resistors in Figure 9-1 from 60 kΩ to 40 kΩ in *Typical Application* ... 14

- Changed Figure 10-5 to use a 5-V supply voltage 19

Changes from Revision A (January 2016) to Revision B (April 2019) **Page**

- アップグレードされた新しい INA818 に関する情報を追加 1
- Added *Device Comparison Table* 4

Changes from Revision * (September 2000) to Revision A (January 2016) **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA819	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	2, 3
INA821	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV Offset, 0.5-µV/°C V_{OS} Drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1-µV/°C V_{OS} Drift, 1.8-V to 5-V, RRO, 50-µA I_Q, chopper-stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion	G = 0.2 V/V	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

6 Pin Configuration and Functions

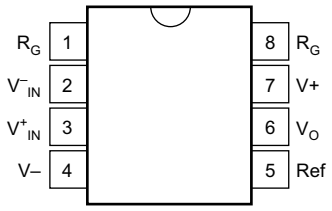


図 6-1. P (8-Pin PDIP) and D (8-Pin SOIC) Packages, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
2	V^-_{IN}	Input	Negative input
3	V^+_{IN}	Input	Positive input
4	V^-	Power	Negative supply
5	Ref	Input	Reference input. This pin must be driven by low impedance or connected to ground.
6	V_O	Output	Output
7	V^+	Power	Positive supply
8	R_G	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.

7 Specifications

7.1 絶対最大定格

自由気流での動作温度範囲内 (特に記述のない限り) (1)

		最小値	最大値	単位
	電源電圧		±18	V
	アナログ入力電圧		±40	V
	出力のグランドへの短絡	連続		
	動作温度範囲	-40	125	℃
	接合部温度		150	℃
	リード温度 (半田付け、10 秒)		300	℃
T_{stg}	保存温度	-40	125	℃

(1) 絶対最大定格を上回るストレスが加わった場合、デバイスに永続的な損傷が発生する可能性があります。これはストレスの定格のみについて示してあり、このデータシートのセクション 7.3 に示された値を超える状態で本製品が正常に動作することを暗黙的に示すものではありません。絶対最大定格の状態に長時間置くと、本製品の信頼性に影響を与えることがあります。

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Power supply	±2.25	±15	±18	V
	Input common-mode voltage (for V_O = 0 V)	V^- + 2		V^+ – 2	V
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA118		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	48	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59	25	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14	14	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58	25	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} = 0 V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset voltage, RTI	Initial	T_A = 25°C	INA118PB, UB		±10 ± 50 / G	±50 ± 500 / G	µV
			INA118P, U		±25 ±100 / G	±125 ±1000 / G	
	vs Temperature	T_A = –40°C to +85°C	INA118PB, UB		±0.2 ± 2 / G	±0.5 ± 20 / G	µV/°C
			INA118P, U		±0.2 ± 5 / G	±1 ± 20 / G	
	vs Power supply	V_S = ±2.25 V to ±18 V	INA118PB, UB		±1 ±10 / G	±5 ± 100 / G	µV/V
			INA118P, U		±1 ±10 / G	±10 ±100 / G	
	Long-term stability				±0.4 ±5 / G		µV/mo
Impedance	Differential				10^{10} || 1		Ω || pF
	Common-mode				10^{10} || 4		
Linear input voltage				(V^+) – 2	(V^+) – 1.4		V
				$(V^–)$ + 2	$(V^–)$ + 1.2		
Safe input voltage						±40	V
Common-mode rejection		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 1	INA118PB, UB	80	90		dB
			INA118P, U	73	90		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 10	INA118PB, UB	97	110		
			INA118P, U	89	110		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 100	INA118PB, UB	107	120		
			INA118P, U	98	120		
		V_{CM} = ±10 V, ΔR_S = 1 kΩ, G = 1000	INA118PB, UB	110	125		
			INA118P, U	100	125		
Bias current			INA118PB, UB		±1	±5	nA
			INA118P, U		±1	±10	
Bias current drift		T_A = –40°C to +85°C			±40		pA/°C
Offset current			INA118PB, UB		±1	±5	nA
			INA118P, U		±1	±10	
Offset current drift		T_A = –40°C to +85°C			±40		pA/°C
Noise voltage, RTI		G = 1000, R_S = 0 Ω	f = 10 Hz		11		nV/√Hz
			f = 100 Hz		10		nV/√Hz
			f = 1 kHz		10		nV/√Hz
			f_B = 0.1 Hz to 10 Hz		0.28		µVp-p
Noise current			f = 10 Hz		2		pA/√Hz
			f = 1 kHz		0.3		
			f_B = 0.1 Hz to 10 Hz		80		pAp-p
GAIN							
Gain equation					1 + (50 kΩ / R_G)		V/V
Gain				1		10000	V/V
Gain error		G = 1			±0.01%	±0.024%	
		G = 10			±0.02%	±0.4%	
		G = 100			±0.05%	±0.5%	
		G = 1000			±0.5%	±1%	
Gain drift		G = 1, T_A = –40°C to +85°C			±1	±10	ppm/°C
50-kΩ resistance drift(1)		T_A = –40°C to +85°C			±25	±100	ppm/°C
Nonlinearity		G = 1			±0.0003	±0.001	% of FSR
		G = 10			±0.0005	±0.002	
		G = 100			±0.0005	±0.002	
		G = 1000			±0.002	±0.01	

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = 0 V, and R_L = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage:	Positive	R_L = 10 kΩ	(V^+) – 1	(V^+) – 0.8		V
	Negative	R_L = 10 kΩ	(V^-) + 0.35	(V^-) + 0.2		
	Single supply high	V^+ = 4.5 V, V^- = 0 V(2), R_L = 10 kΩ	1.8	2		
	Single supply low	V^+ = 4.5 V, V^- = 0 V(2), R_L = 10 kΩ	60	35		mV
Load capacitance stability				1000		pF
Short circuit current				+5/–12		mA
FREQUENCY RESPONSE						
Bandwidth, –3 dB		G = 1		800		kHz
		G = 10		500		
		G = 100		70		
		G = 1000		7		
Slew rate		V_O = ±10 V, G = 10		0.9		V/µs
Settling time, 0.01%		G = 1		15		µs
		G = 10		15		
		G = 100		21		
		G = 1000		210		
Overload recovery		50% overdrive		20		µs
POWER SUPPLY						
Current		V_{IN} = 0 V		±350	±385	µA

(1) Temperature coefficient of the 50-kΩ term in the gain equation.
(2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

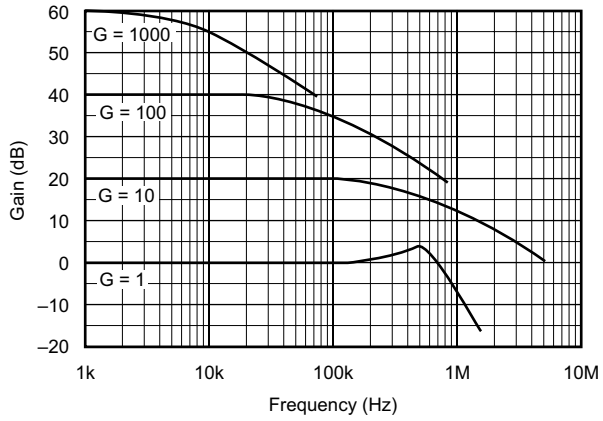


図 7-1. Gain vs Frequency

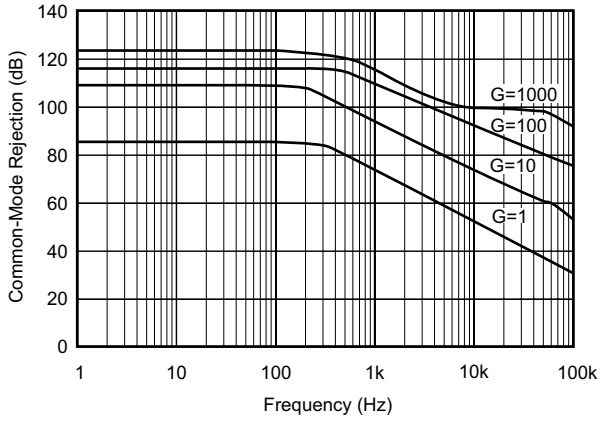
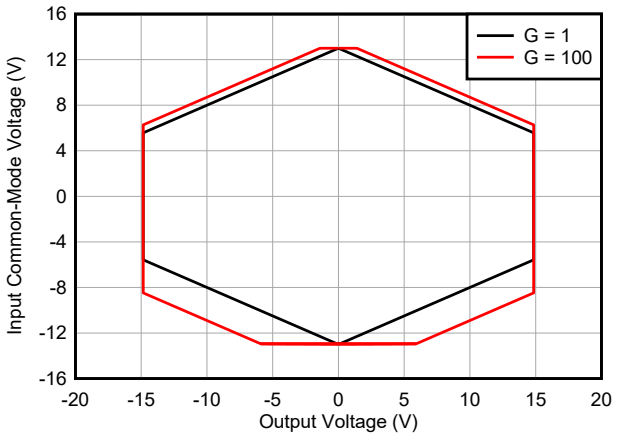
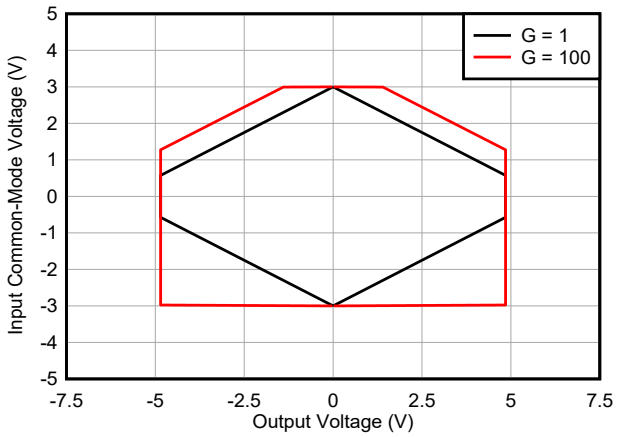


図 7-2. Common-Mode Rejection vs Frequency



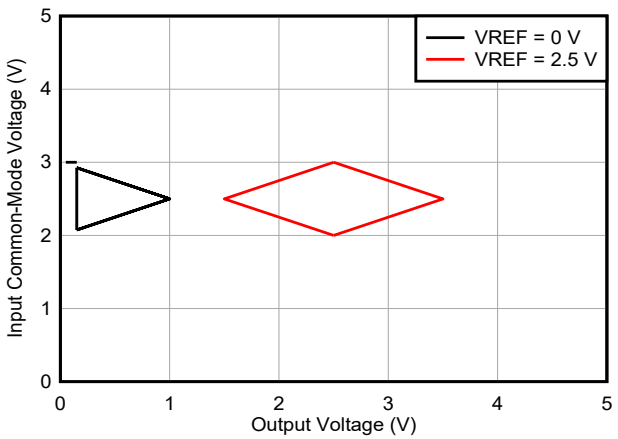
VS = ±15 V

図 7-3. Input Common-Mode Range vs Output Voltage



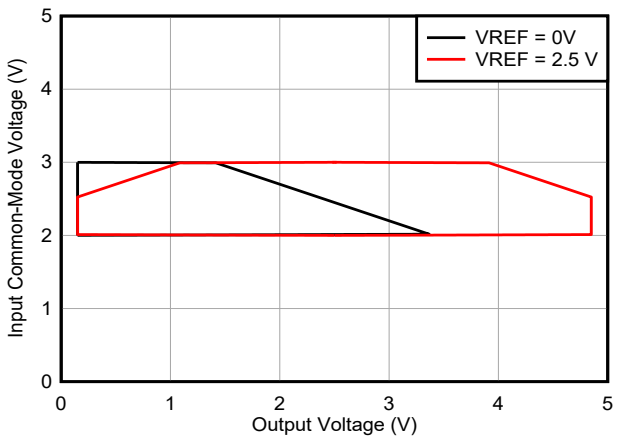
VS = ±5 V

図 7-4. Input Common-Mode Range vs Output Voltage



VS = 5 V
G = 1

図 7-5. Input Common-Mode Range vs Output Voltage



VS = 5 V
G = 100

図 7-6. Input Common-Mode Range vs Output Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

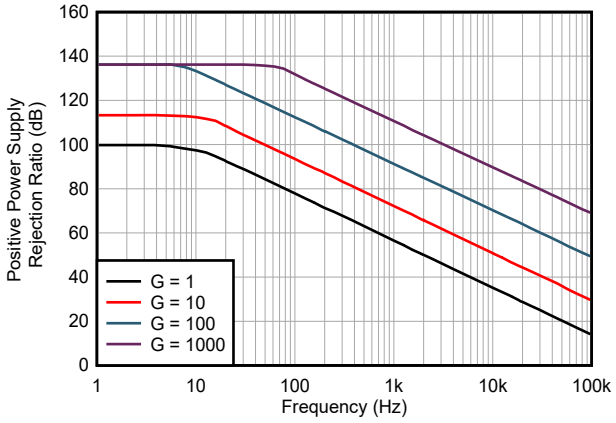


図 7-7. Positive Power Supply Rejection vs Frequency

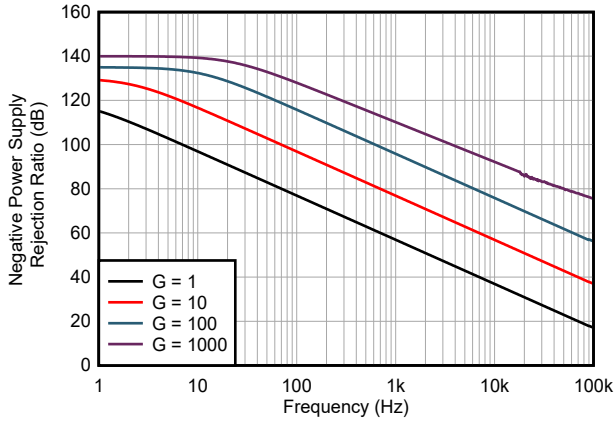


図 7-8. Negative Power Supply Rejection vs Frequency

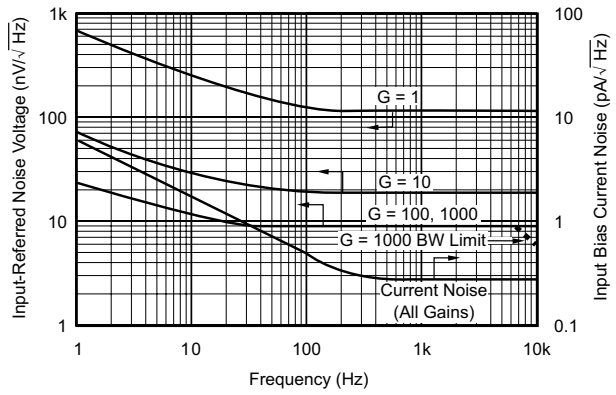


図 7-9. Input-Referred Noise Voltage vs Frequency

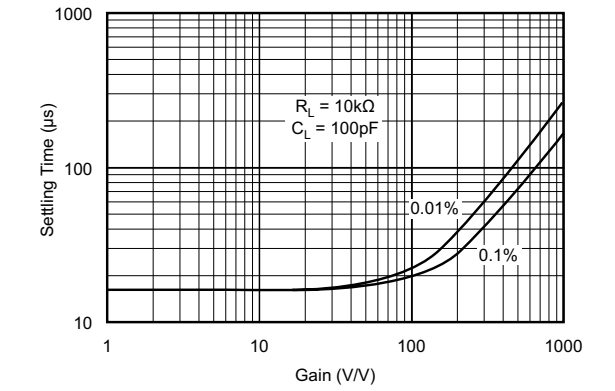


図 7-10. Settling Time vs Gain

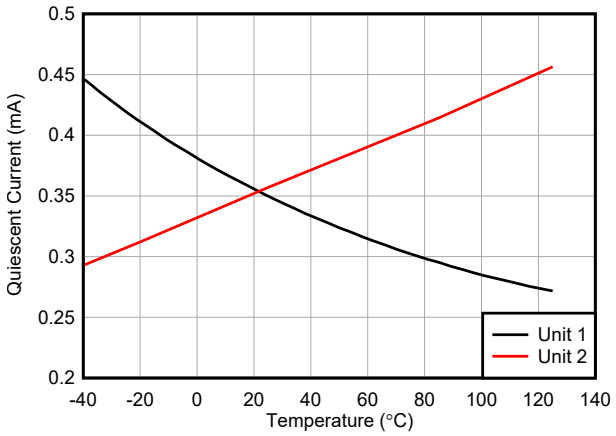


図 7-11. Quiescent Current and Slew Rate vs Temperature

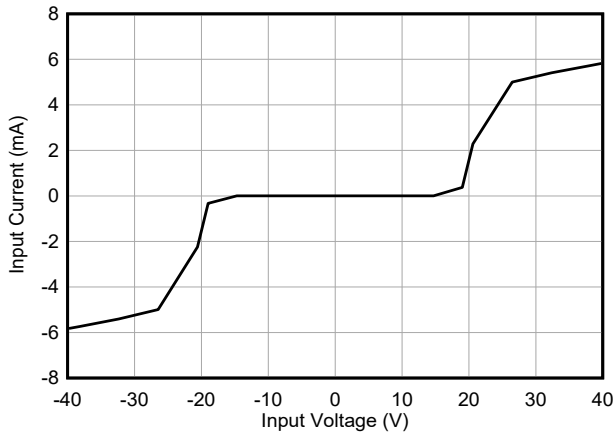


図 7-12. Input Bias Current vs Input Overload Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

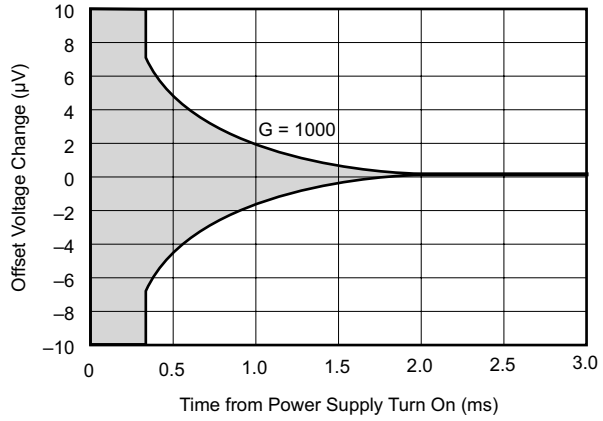


図 7-13. Offset Voltage vs Warm-Up Time

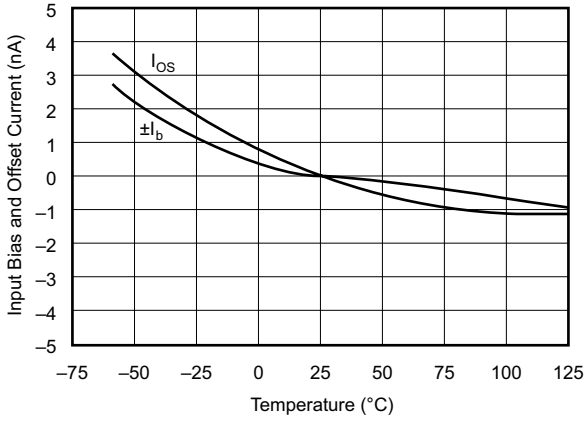


図 7-14. Input Bias and Offset Current vs Temperature

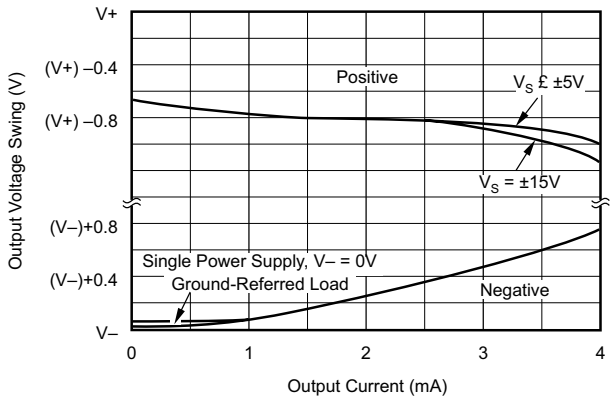


図 7-15. Output Voltage Swing vs Output Current

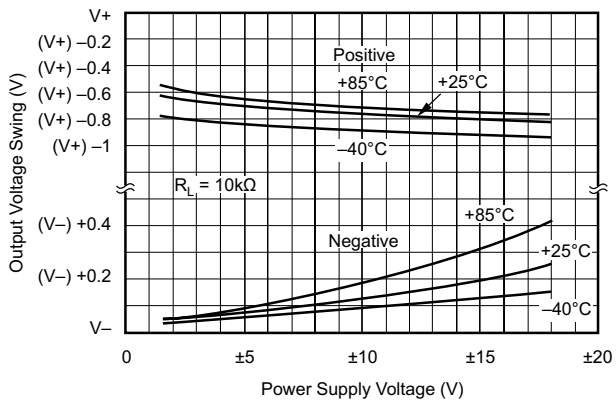


図 7-16. Output Voltage Swing vs Power Supply Voltage

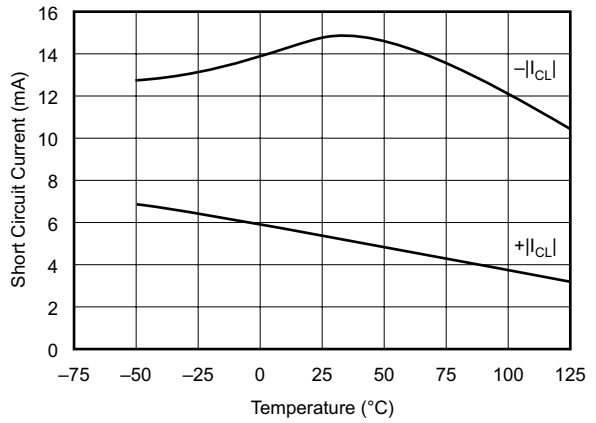


図 7-17. Output Current Limit vs Temperature

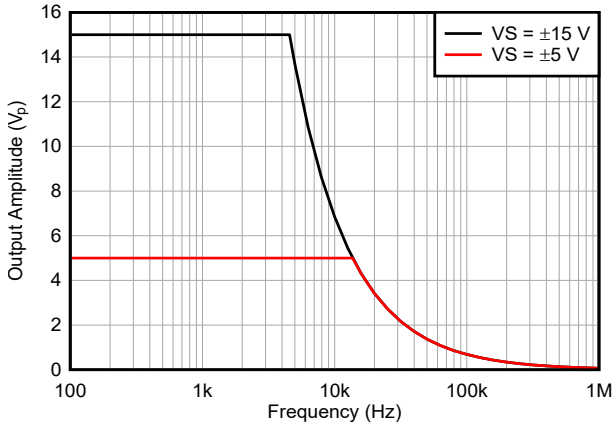


図 7-18. Maximum Output Swing vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

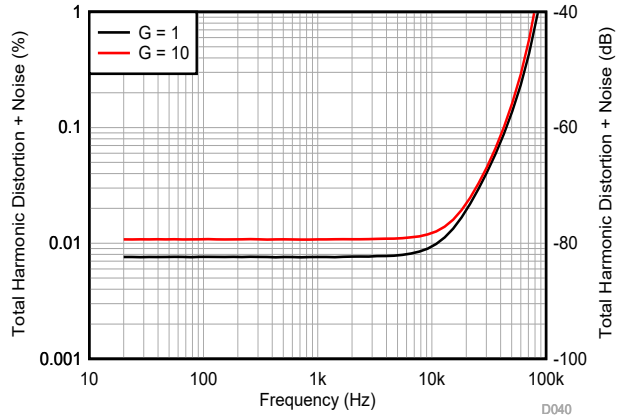
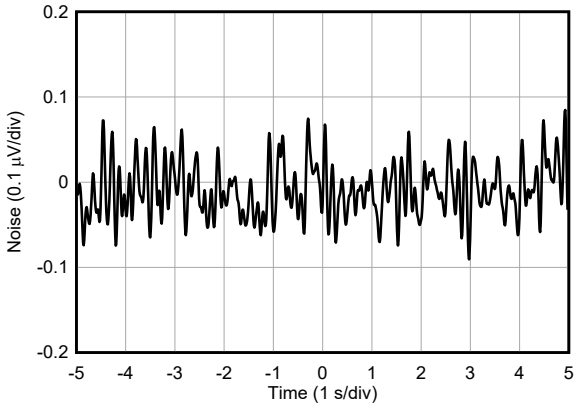


図 7-19. THD + N vs Frequency



G = 1000

図 7-20. Input-Referred Noise, 0.1 Hz to 10 Hz

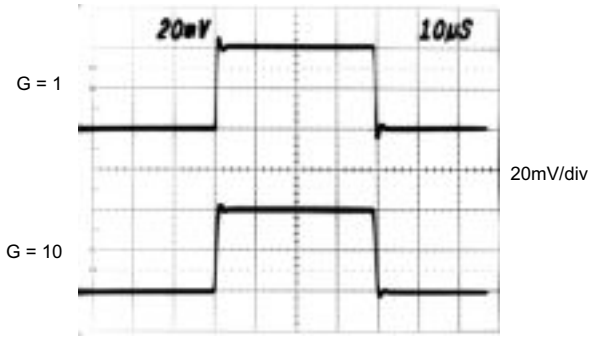


図 7-21. Small-Signal Response

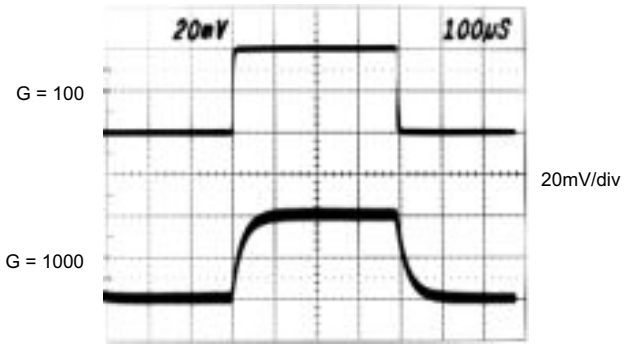


図 7-22. Small-Signal Response

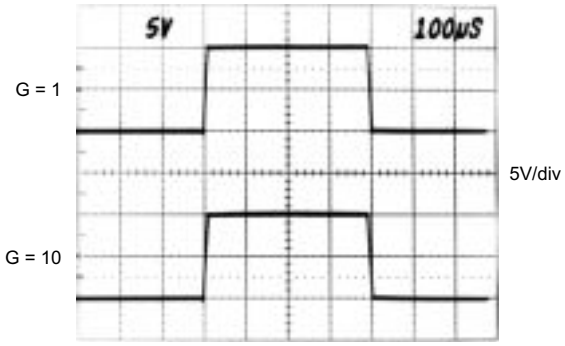


図 7-23. Large-Signal Response

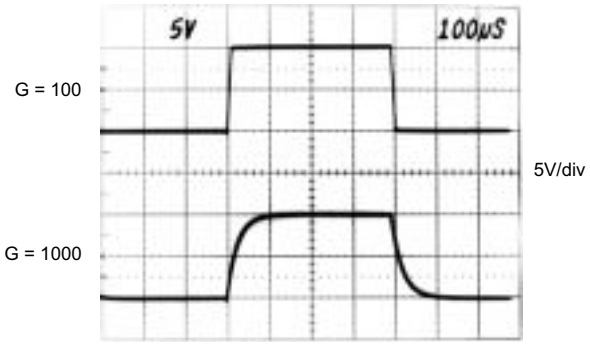


図 7-24. Large-Signal Response

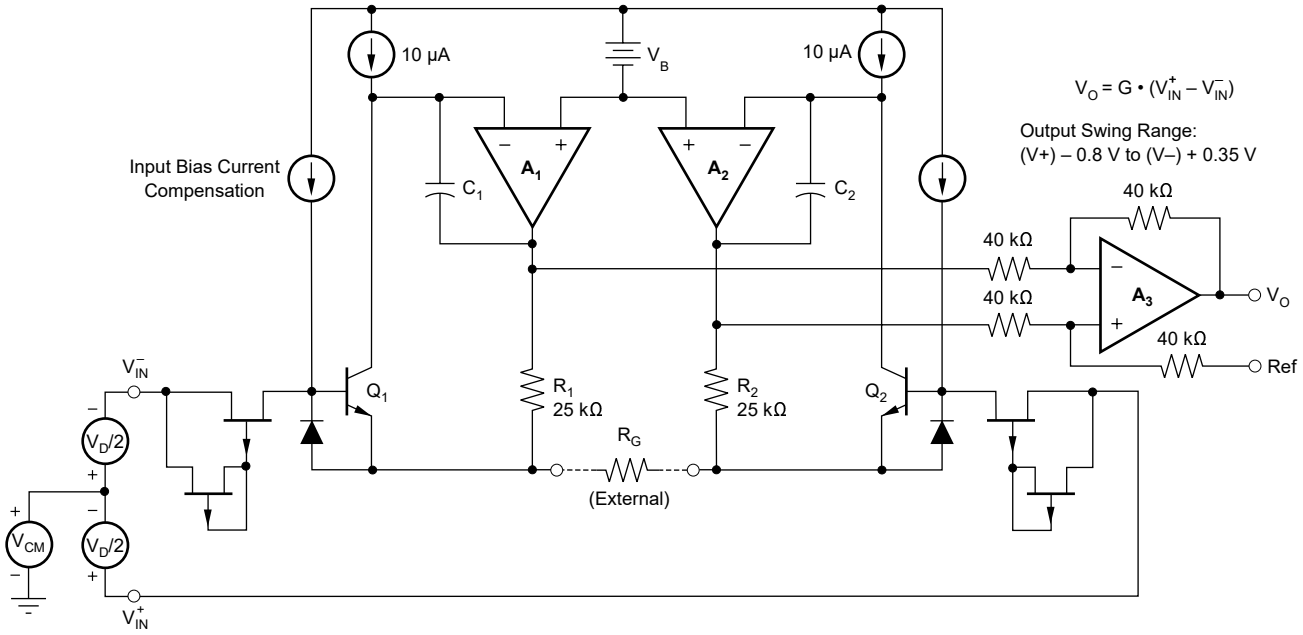
8 Detailed Description

8.1 Overview

セクション 8.2 shows a simplified representation of the INA118 and provides insight into device operation. Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, thus preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 6 mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G, causing a signal current to flow through R_G, R_1, and R_2. The output difference amp, A_3, removes the common-mode component of the input signal and refers the output signal to the Ref pin.

8.2 Functional Block Diagram



8.3 Feature Description

The INA118 input sections use junction field effect transistors (JFET) connected to provide protection up to ±40 V. The current-feedback architecture provides maximum bandwidth over the full range of gain settings.

8.4 Device Functional Modes

8.4.1 Noise Performance

The INA118 provides low noise in most applications. For differential source impedances less than 1 kΩ, the INA103 may provide lower noise. For source impedances greater than 50 kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

The low-frequency noise of the INA118 is approximately 0.28 μV_{PP}, measured from 0.1 Hz to 10 Hz (G ≥ 100). The INA118 provides dramatically improved noise performance when compared to state-of-the-art, chopper-stabilized amplifiers.

8.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA118 is from approximately 1.4-V less than the positive supply voltage to 1.2-V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see also 図 7-6.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. In this case, the output of the INA118 is near 0 V even though both inputs are overloaded.

8.4.3 Input Protection

The inputs of the INA118 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 6 mA. 図 7-12 shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

9 アプリケーションと実装

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 アプリケーション情報

INA118 は、非反転入力と反転入力に高い同相電圧がある場合でも、小さい差動電圧を測定します。同相信号除去比が高いため、広範なアプリケーションに適しています。リファレンス・ピンを設定することにより出力信号の機能を調整できるため、複数の構成に実用的な柔軟性が得られます。

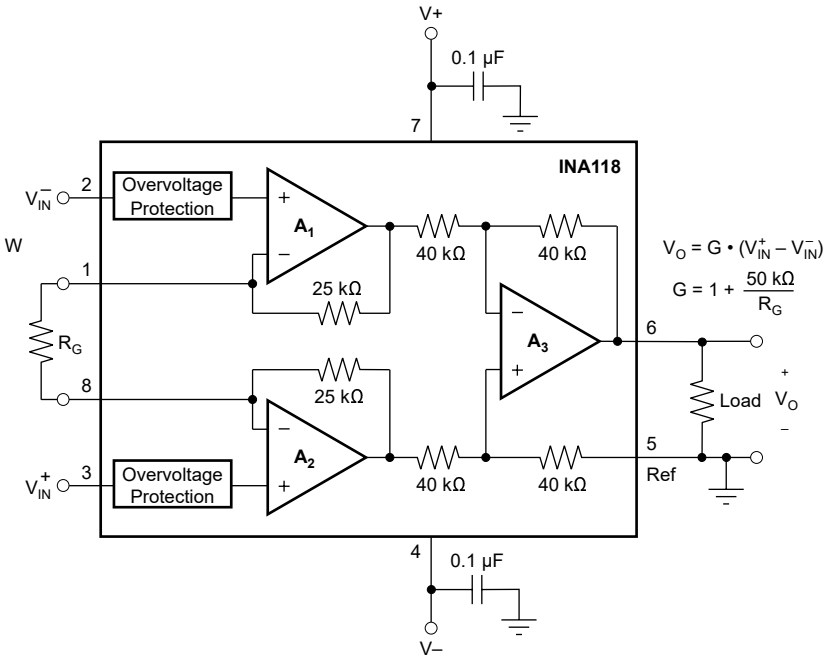
9.2 Typical Application

図 9-1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins, as shown. The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 12 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR (G = 1).

図 9-1 depicts an input signal with a 5-mV, 1-kHz signal with a 1-V_{PP} common-mode signal, a condition often observed in process-control systems. 図 9-2 depicts the output of the INA118 (G = 250) depicting the clean recovered 1-kHz waveform.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:

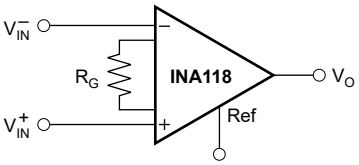


図 9-1. Basic Connections

9.2.1 Design Requirements

図 9-5 and 図 9-4 depict the performance of a typical application of the INA118 in a shop floor-vibration sensing application. Industrial process control systems often involve the interconnecting of multiple subsystems; therefore, ground loops are frequently encountered, and often are not easily solved. The inherent common-mode rejection of instrumentation amplifiers enables accurate measurements even in the presence of ground-loop potentials.

The typical application was tested in a system with these requirements:

- Transducer signal ≈ 5 mV_{PP}
- Transducer center frequency = 1 kHz
- Common-mode signal (required to be rejected): 1 V_{PP} at 60 Hz

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

As shown in 式 1, the gain of the INA118 is set by connecting a single external resistor, R_G, connected between pins 1 and 8.

$$G = 1 + \frac{50\ k\Omega}{R_G} \tag{1}$$

Commonly used gains and resistor values are shown in 図 9-1.

The 50-kΩ term in 式 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from 式 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

図 7-1 shows that, despite a low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This achievement is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3-dB peaking at 500 kHz in unity gain. This peaking is a result of the current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable 6-dB/octave due to a zero in the amplifier response. A simple pole at 300 kHz or less produces a flat pass-band unity gain response.

9.2.2.3 Offset Trimming

The INA118 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. 図 9-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is summed at the output. The op amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

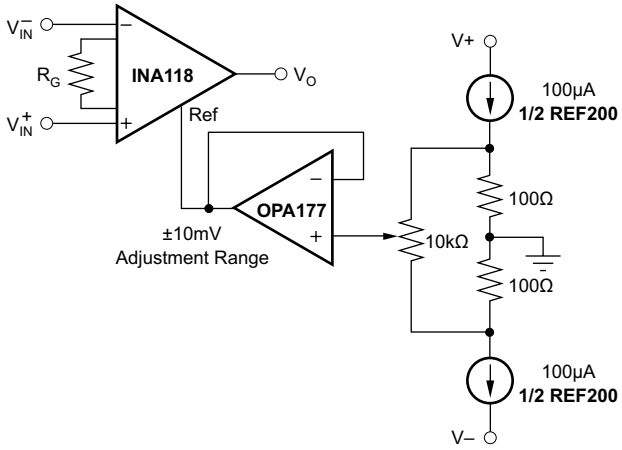


図 9-2. Optional Trimming of Output Offset Voltage

9.2.2.4 Input Bias Current Return Path

The input impedance of the INA118 is extremely high at approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±5 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. 図 9-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential which exceeds the common-mode range of the INA118, and the input amplifiers saturates.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in 図 9-3). With higher source impedance, using two equal resistors provides a balanced input, with the possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

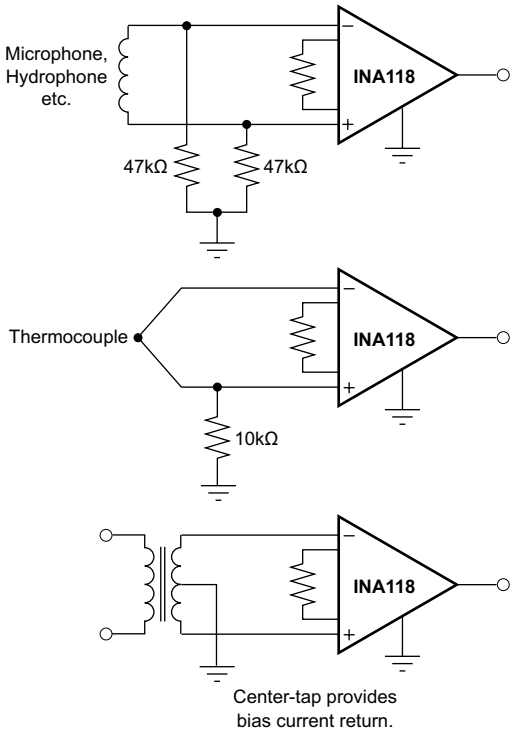
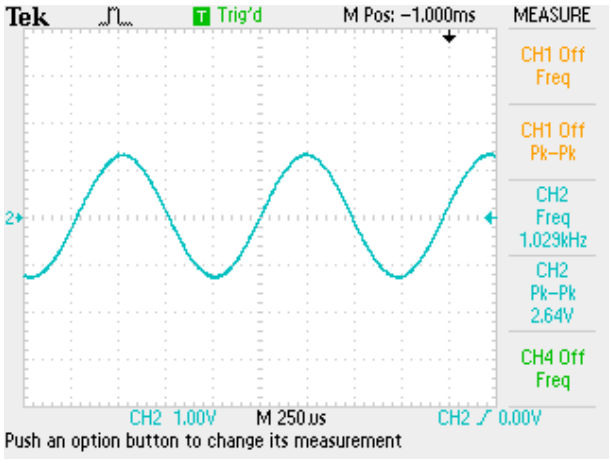


図 9-3. Providing an Input Common-Mode Current Path

9.2.3 アプリケーション曲線



1kHz の差動信号も存在しますが、この波形では確認できません。

図 9-4. 60Hz の同相信号を示す代表的なアプリケーションの入力

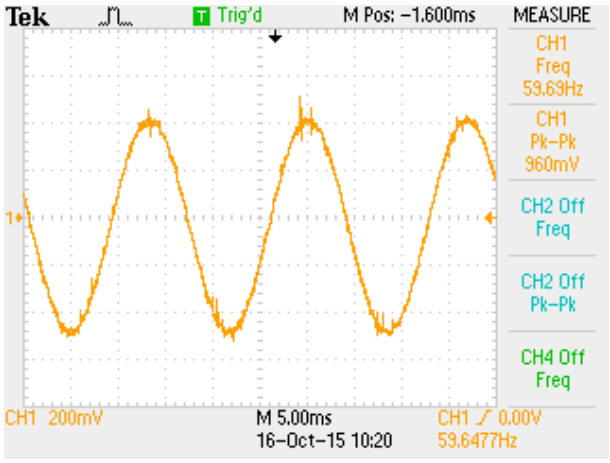


図 9-5. 必要な 1kHz の波形を示す代表的なアプリケーションの出力 (同相干渉は除去)

9.3 Power Supply Recommendations

9.3.1 Low-Voltage Operation

The INA118 operates on power supplies as low as ±2.25 V. Performance of the INA118 remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range; see also *セクション 7.6*. Operation at low supply voltage requires careful attention to make sure that the input voltages remain within the respective linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. 図 7-3 shows the range of linear operation for a various supply voltages and gains.

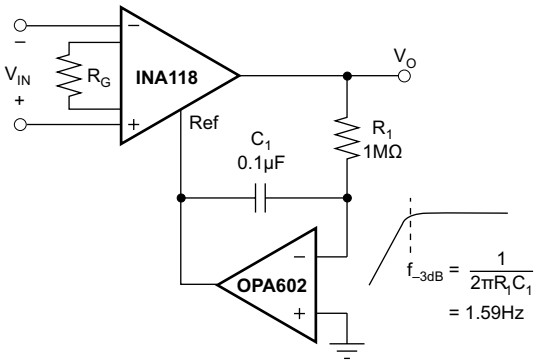
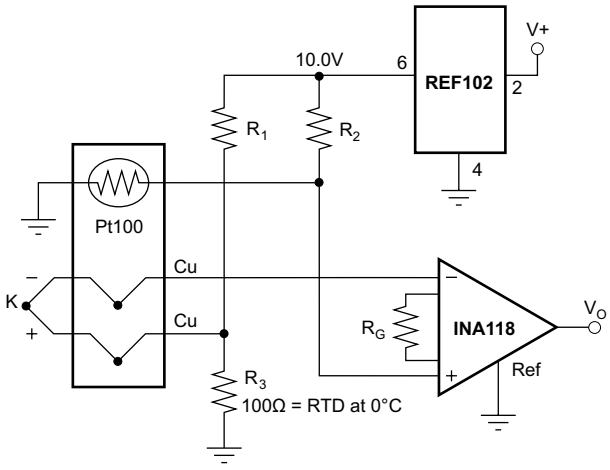
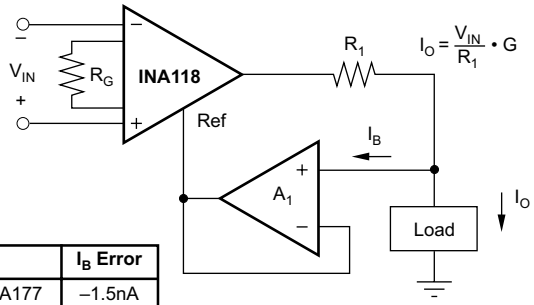


図 9-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

図 9-7. Thermocouple Amplifier With Cold Junction Compensation



A_1	I_B Error
OPA177	–1.5nA
OPA602	–1pA
OPA128	–75fA

図 9-8. Differential Voltage to Current Converter

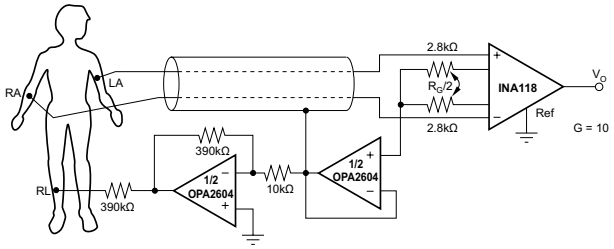


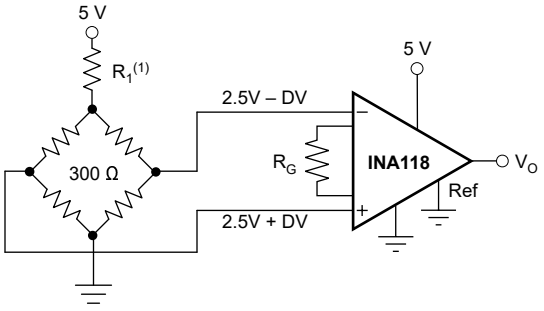
図 9-9. ECG Amplifier With Right-Leg Drive

9.3.2 Single-Supply Operation

The INA118 can be used on single power supplies of 4.5 V to 36 V. 図 9-10 shows a basic single-supply circuit. The output Ref pin is connected to ground. Zero differential input voltage demands an output voltage of 0 V (ground). The actual output voltage swing is limited to approximately 35-mV above ground, when the load is referred to ground as shown. 図 7-15 shows how the output voltage swing varies with output current.

With single supply operation, V^+_{IN} and V^-_{IN} must be 1.2-V greater than ground for linear operation. Connecting the inverting input to ground and measuring a voltage connected to the noninverting input is not possible.

To illustrate the issues affecting low-voltage operation, consider the circuit in 図 9-10, which shows the INA118 operating from a single 5-V supply. Depending on the desired gain, a resistor in series with the high side of the bridge can be required to make sure that the bridge output voltage is within the common-mode range of the amplifier inputs. See 図 7-5 for 5-V single supply operation.



NOTE: (1) R_1 may be required to create proper common-mode voltage, for low voltage operation with certain gains — see text.

図 9-10. Single-Supply Bridge Amplifier

9.4 Layout

9.4.1 Layout Guidelines

TI always recommends paying attention to good layout practices. For best operational performance of the device, use good printed-circuit-board (PCB) layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and of the individual device. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V^+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Keep the traces as short as possible.

9.4.2 Layout Example

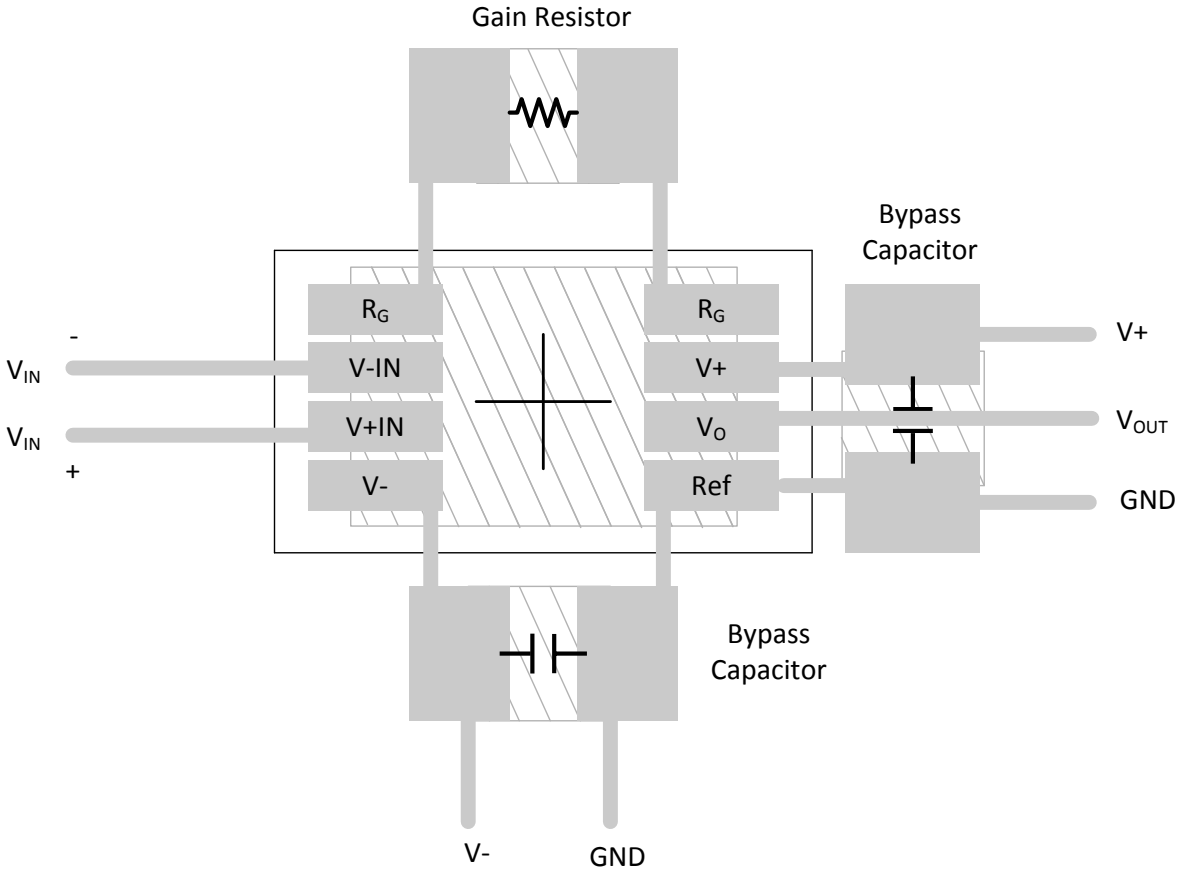


図 9-11. Layout Recommendation

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

表 10-1. Design Kits and Evaluation Modules

NAME	PART NUMBER	TYPE
DIP adapter evaluation module	DIP-ADAPTER-EVM	Evaluation modules and boards
Universal instrumentation amplifier evaluation module	INAEVM	Evaluation modules and boards

表 10-2. Development Tools

DESCRIPTION	PART NUMBER	TYPE
Analog engineer's calculator	ANALOG-ENGINEER-CALC	Calculation tool
TINA-TI™ software: SPICE-based analog simulation program	TINA-TI	Circuit design and simulation
PSpice® for TI design and simulation tool	PSPICE-FOR-TI	Circuit design and simulation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA118P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA118P	Samples
INA118PB	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA118P B	Samples
INA118U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 118U	Samples
INA118U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 118U	Samples
INA118U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	Samples
INA118UB	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UB/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 118U B	Samples
INA118UBG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U B	Samples
INA118UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

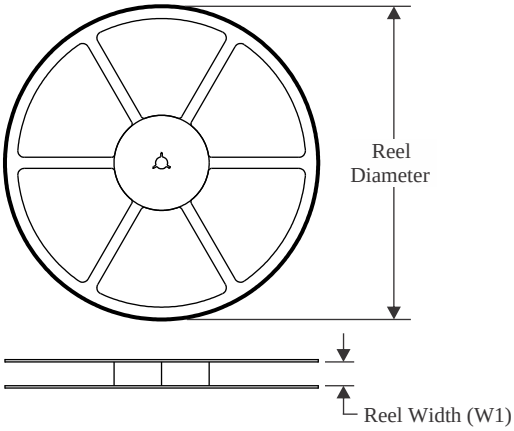
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

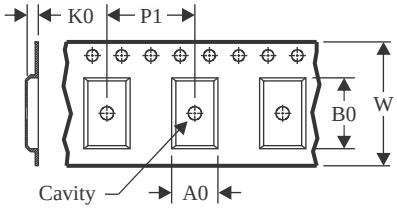
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

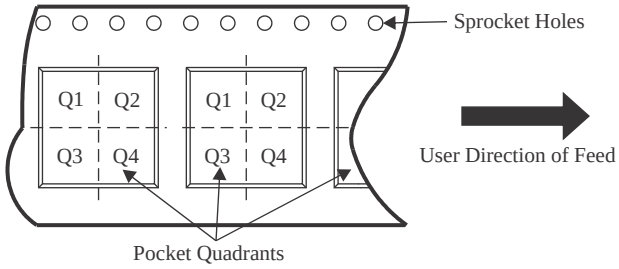


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

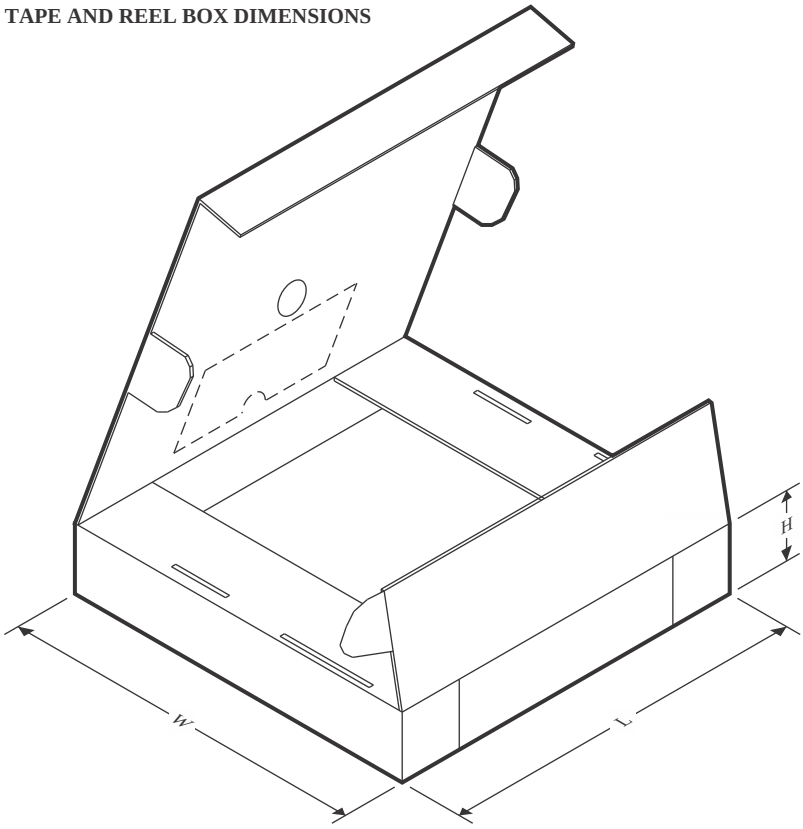
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

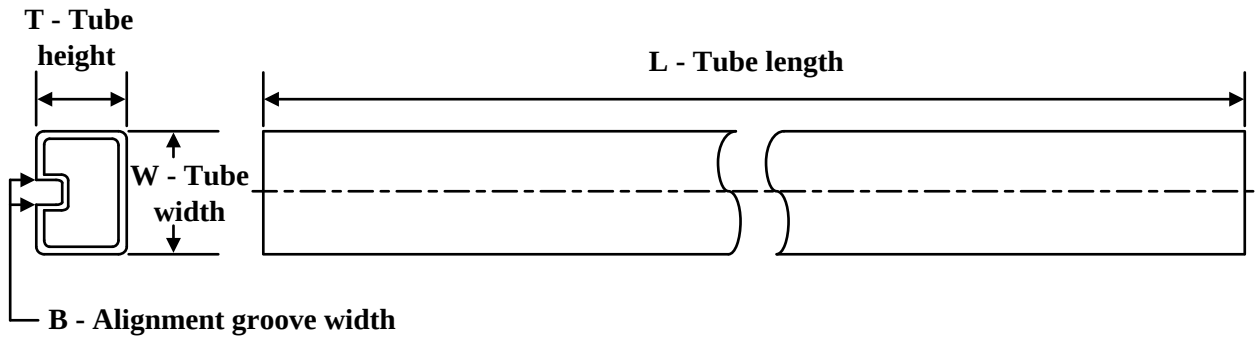
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

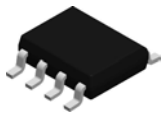
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA118U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA118U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA118UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA118UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA118P	P	PDIP	8	50	506	13.97	11230	4.32
INA118P	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB	P	PDIP	8	50	506	13.97	11230	4.32
INA118U	D	SOIC	8	75	506.6	8	3940	4.32
INA118UB	D	SOIC	8	75	506.6	8	3940	4.32
INA118UBG4	D	SOIC	8	75	506.6	8	3940	4.32
INA118UG4	D	SOIC	8	75	506.6	8	3940	4.32

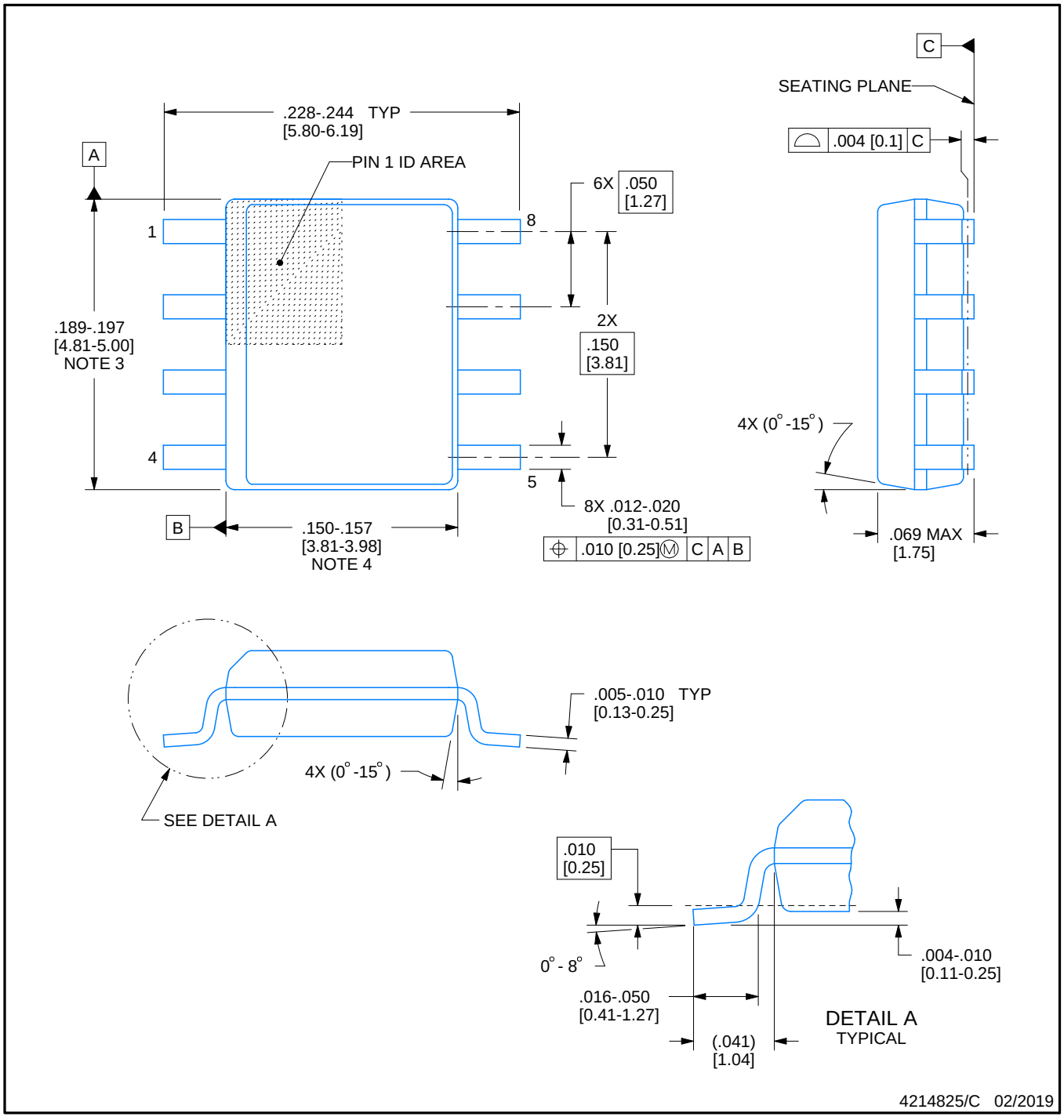


PACKAGE OUTLINE

D0008A

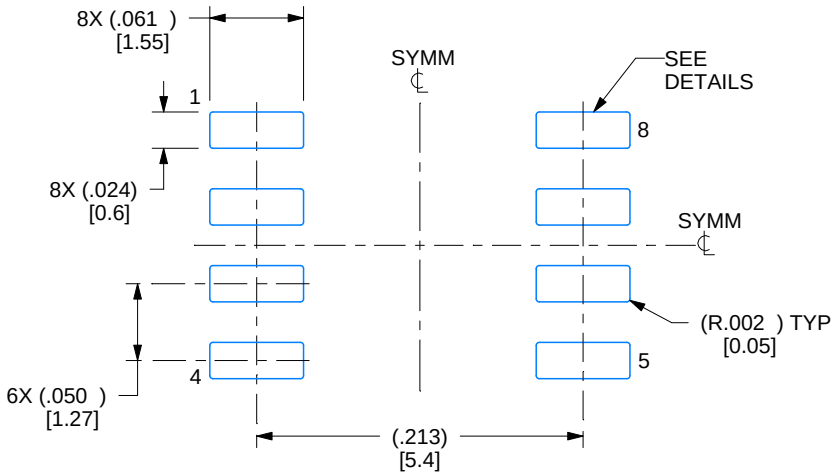
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

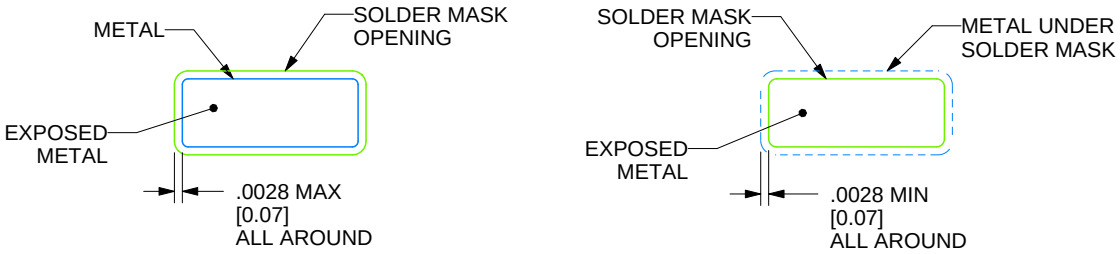


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

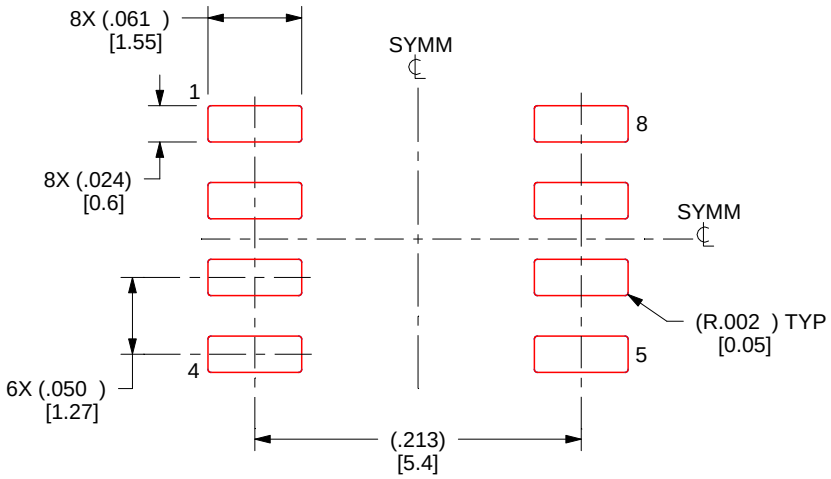
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



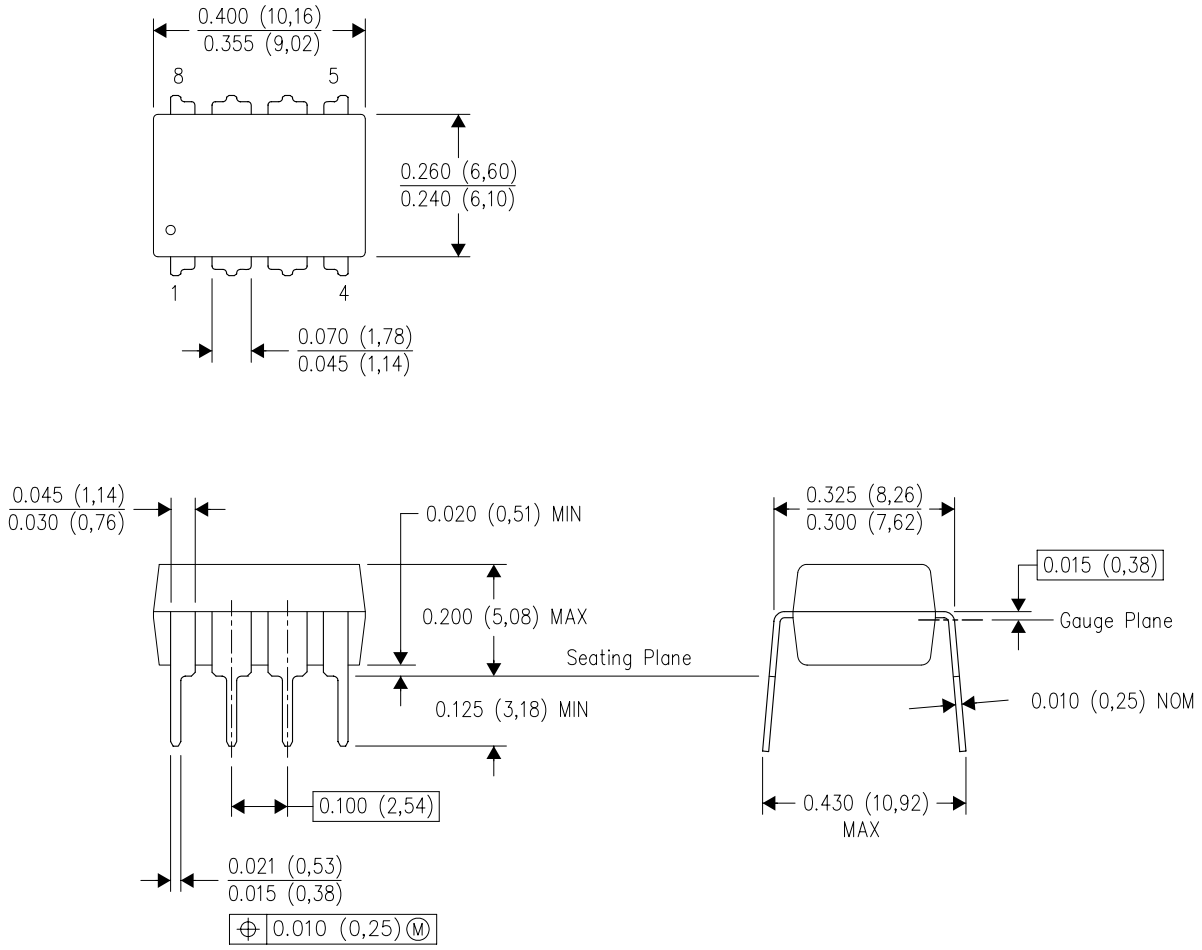
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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