

ISO1176 絶縁型 RS-485 Profibus トランシーバ

1 特長

- EN 50170 および TIA/EIA-485-A の要件を満たす、または超える性能
- 最大 40Mbps の信号速度
- 2.1V を超える差動出力 (54Ω の負荷)
- 低バス容量: 10pF (最大値)
- バス上のトランシーバ数は最大 160 個
- 50kV/μs の標準過渡電圧耐性
- バスの開放、短絡、またはアイドル時のフェイル・セーフを備えるレシーバ
- 3.3V 入力は 5V 許容
- バス・ピンの ESD 保護
 - バス・ピンと GND2 間で 16kV HBM
 - バス・ピンと GND1 間で 6kV HBM
- 安全および規制当局の承認
 - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した 4000V_{PK} の絶縁、560V_{PK} V_{IORM}
 - UL 1577 に準拠した 2500V_{RMS} の絶縁定格
 - CSA 62368-1 に準拠した 4000V_{PK} の絶縁定格

2 アプリケーション

- Profibus
- ファクトリ・オートメーション
- ネットワーク接続センサ
- モータおよびモーション制御
- HVA およびビルディング・オートメーション・ネットワーク
- ネットワーク接続セキュリティ・ステーション

3 概要

ISO1176 デバイスは、PROFIBUS アプリケーションでの使用を目的として設計された絶縁型差動ライン・トランシーバです。このデバイスは、大きな同相電圧範囲で動作できるようにグラウンド・ループが遮断されているため、長い伝送ラインに最適です。各デバイスの対称型絶縁バリアは、ラ

イン・トランシーバとロジック・レベル・インターフェイスとの間で、UL に従い、2500V_{RMS} で絶縁を行うことがテスト済みです。

ガルバニック絶縁された差動バス・トランシーバは、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計された IC です。このトランシーバは、ガルバニック絶縁された差動ライン・ドライバと差動入力ライン・レシーバを組み合わせたものです。このドライバは、アクティブ・ハイのイネーブルとともに、絶縁されたイネーブル状態出力を ISODE ピン (ピン 10) に備え、方向制御が容易になっています。ドライバの差動出力とレシーバの差動入力、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。このポートは、最大 160 ノードを許容するバスへの負荷を最小化するように設計されています。

PV ピン (ピン 7) は、フルチップ・イネーブル・オプションとして提供されています。PV ピンにロジック・ローが印加されると、すべてのデバイス出力が高インピーダンスになります。詳細については、[セクション 8.3](#) の機能表を参照してください。

ケーブル接続されたすべての I/O は、各種ノイズ源からの電氣的ノイズの過渡現象にさらされる可能性があります。このようなノイズ過渡は、十分な大きさと持続時間を持つ場合、トランシーバや近くにある感度の高い回路に損傷を与える可能性があります。ISO1176 は、データの破損や高価な制御回路の損傷が発生する危険性を大幅に低減できます。

このデバイスは、-40°C ~ +85°C の周囲温度範囲で動作が規定されています。

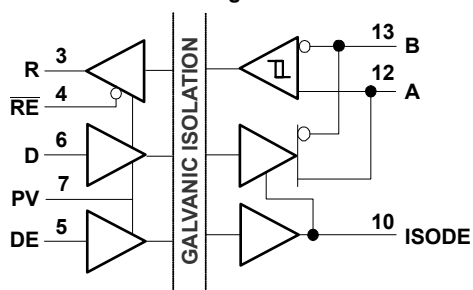
製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
ISO1176	SOIC (16)	10.30mm × 7.50mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



ISO1176
Function Diagram



概略回路図



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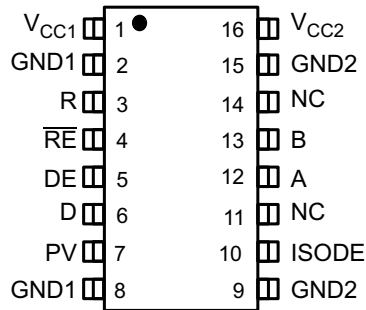
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (June 2015) to Revision F (August 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	5
• Updated electrical and switching characteristics to match device performance.....	7
Changes from Revision D (March 2010) to Revision E (June 2015)	Page
• 「ピン構成と機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1
• VDE 標準を「DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12」に変更.....	1
Changes from Revision C (October 2008) to Revision D (March 2010)	Page
• 「特長」の最初の一覧に「560Vpeak V_{IORM} 」を追加.....	1
• 「特長」の一覧に UL 1577、IEC 60747-5-2 (VDE 0884, Rev. 2) を追加.....	1
• Changed the ISO1176 “Sticky Bit” Issue section.....	26
Changes from Revision B (June 2008) to Revision C (October 2008)	Page
• 「概要」セクションの第 2 段落の文章を次のように変更: 「ドライバがディセーブルされているか $V_{CC2} = 0$ のときから「最大 160 ノードを許容する」に変更.....	1
Changes from Revision A (May 2008) to Revision B (June 2008)	Page
Changes from Revision * (March 2008) to Revision A (May 2008)	Page
• 「特長」の一覧に「3.3V 入力は 5V 許容」を追加.....	1
• 「特長」の一覧に「バス・ピンの ESD 保護」の箇条書き項目と副項目を追加.....	1

- Added the APPLICATION INFORMATION section.....24

5 Pin Configuration and Functions



**图 5-1. DW Package
16-Pin SOIC
Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Noninverting bus output
B	13	I/O	Inverting bus output
D	6	I	Driver input
DE	5	I	Driver logic-high enable
GND1	2, 8	—	Logic-side ground; internally connected
GND2	9, 15	—	Bus-side ground; internally connected
ISODE	10	—	Bus-side driver enable output
NC	11, 14	—	Not connected internally; may be left floating
PV	7	I	ISO1176 chip enable, logic high applied immediately after power up for device operation. A logic low 3-states all outputs.
R	3	O	Receiver output
RE	4	I	Receiver logic-low enable
V _{CC1}	1	—	Logic side power supply
V _{CC2}	16	—	Bus side power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾	V_{CC1}, V_{CC2}	-0.5	6	V
V_O	Voltage at any bus I/O terminal		-9	14	V
V_I	Voltage input	D, DE or RE	-0.5	6	V
I_O	Receiver output current		-10	10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Bus pins to 2, 8	±6000	V
		Bus pins to 9, 15	±16000	V
		All pins	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		±1000	V
	Machine model ANSI/ESDS5.2-1996		±200	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Logic-side supply voltage, V_{CC1} (with respect to GND1)		3.15		5.5	V
	Bus-side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	V
V_{CM}	Voltage at either bus I/O terminal	A or B	-7		12	V
V_{IH}	High-level input voltage	PV, RE	2		5.5	V
V_{IH}	High-level input voltage	D, DE	$0.7 \cdot V_{CC1}$			V
V_{IL}	Low-level input voltage	PV, RE	0		0.8	V
V_{IL}	Low-level input voltage	D, DE			$0.3 \cdot V_{CC1}$	V
V_{ID}	Differential input voltage	A with respect to B	-12		12	V
I_O	Output current	Driver	-70		70	mA
I_O	Output current	Receiver	-8		8	mA
	Input pulse width		10			ns
T_A	Ambient temperature		-40	25	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO1176	UNIT
		DW (SOIC)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	81.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	41.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	46.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	15.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	45.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D	Maximum power dissipation (both sides) V _{CC1} = V _{CC2} = 5.25 V, T _J = 150°C, C _L = 15 pF, Input at 20 MHz 50% duty cycle square wave			283	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V _{PK}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 x V _{IOTM} , t = 1 s (100% production)	4000	V _{PK}
q _{pd}	Apparent charge ⁽³⁾	Method b; At routine test (100% production) V _{ini} = 1.2 x V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.5 x V _{IORM} , t _m = 1 s	≤5	pC
C _{IO}	Barrier capacitance, input to output ⁽⁴⁾	V _{IO} = 0.4 x sin(2πft), f = 1 MHz	2	pF
C _I	Input capacitance to ground	V _I = VCC/ 2 + 0.4×sin(2πft), f = 1 MHz, VCC = 5 V	2	pF
R _{IO}	Isolation resistance ⁽⁴⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1 s (100% production)	2500	V _{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the

isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

- (2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program
Basic insulation, 4000 V _{PK} Maximum transient isolation voltage, 560 V _{PK} Maximum repetitive peak isolation voltage	4000 VPK Isolation Rating; Reinforced insulation per CSA 60950-1 and IEC 60950-1 148 V _{RMS} working voltage; Basic insulation per CSA 62368-1 and IEC 62368-1 300V _{RMS} working voltage	Single protection, 2500 V _{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 81.4°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C,			279	mA
T _S	Maximum case temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.
T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.
P_S = I_S × V_I, where V_I is the maximum input voltage.

6.9 Electrical Characteristics: Driver

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^\circ C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Open-circuit differential output voltage	$ V_A-V_B $, Figure 8	1.8		V_{CC2}	V
$ V_{OD(SS)} $	Steady state differential output voltage magnitude	See Figure 9 and Figure 13	2.1			V
	Steady state differential output voltage magnitude	Common mode loading with V_{test} from -7V to 12V, See figure 10	2.1			V
$\Delta V_{ODSS} $	Change in differential output voltage between two states	$R_L = 54$ ohms, See Figure 11 and Figure 12	-200		200	mV
$V_{OC(SS)}$	Steady state common-mode output voltage	$R_L = 54$ ohms, See Figure 11 and Figure 12	2		3	V
$\Delta V_{OC(SS)}$	change in steady-state common-mode output voltage between two states	$R_L = 54$ ohms, See Figure 11 and Figure 12	-200		200	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	$R_L = 54$ ohms, See Figure 11 and Figure 12		0.5		V
$V_{OD(RING)}$	Differential output voltage over and undershoot	See Figure 13 and Figure 17			10	% $V_{OD(PP)}$
$V_{I(HYS)}$	Input voltage hysteresis	See Figure 14		150		mV
I_I	Input current	D, DE at 0 V or V_{CC1}	-10		10	μA
		PV ⁽¹⁾ at 0 V or V_{CC1}			120	μA
$I_{O(OFF)}$	Output current with power off	$V_{CC} \leq 2.5V$	See receiver input current in Electrical Characteristics: Receiver			
I_{OZ}	High-impedance state output current	DE at 0 V				
$I_{OS(P)}$	Peak short circuit output current	DE at V_{CC} , See Figure 15 and Figure 16: $V_{OS} = -7$ to 12 V	-250		250	mA
$I_{OS(SS)}$	Steady state short-circuit output current	DE at V_{CC} , See Figure 15 and Figure 16: $V_{OS} = 12$ V, D at GND1			150	mA
		DE at V_{CC} , See Figure 15 and Figure 16: $V_{OS} = -7$ V, D at V_{CC1}	-150			mA
C_{OD}	Differential output capacitance			7	10	pF
CMTI	Common-mode transient immunity	See Figure 27	25			kV/ μs

(1) The PV pin has a 50-k Ω pullup resistor and leakage current depends on supply voltage.

6.10 Electrical Characteristics: Receiver

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^\circ C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8$ mA, See Figure 22		-80	-10	mV
V_{IT-}	Negative-going input threshold voltage	$I_O = 8$ mA, See Figure 22	-200	-120		mV
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			40		mV
V_{OH}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, $V_{ID} = 200mV$, $I_O = -8mA$	$V_{CC1}-0.4$	3		V
V_{OH}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, $V_{ID} = 200mV$, $I_O = -20\mu A$	$V_{CC1}-0.1$	3.3		V
V_{OL}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, $V_{ID} = -200mV$, $I_O = 8mA$		0.2	0.4	V
V_{OL}	Output Voltage	V_{CC1} at 3.3 V and V_{CC2} at 5V, $V_{ID} = -200mV$, $I_O = 20\mu A$		0	0.1	V
V_{OH}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, $V_{ID} = 200mV$, $I_O = -8mA$	$V_{CC1}-0.8$	4.6		V

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^{\circ}C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, $V_{ID} = 200mV$, $I_O = -20\mu A$	$V_{CC1}-0.1$	5		V
V_{OL}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, $V_{ID} = -200mV$, $I_O = 8mA$		0.2	0.4	V
V_{OL}	Output Voltage	V_{CC1} at 5 V and V_{CC2} at 5V, $V_{ID} = -200mV$, $I_O = 20\mu A$		0	0.1	V
I_A or I_B	Bus pin input current	$V_I = -7 V$ or 12 V, other input = 0V: $V_{CC} = 4.75 V$ or 5.25 V	-160		200	μA
$I_{A(OFF)}$ or $I_{B(OFF)}$		$V_I = -7 V$ or 12 V, other input = 0V: $V_{CC2} = 0 V$				
I_I	Receiver enable input current	$\overline{RE} = 0 V$ or V_{CC1}	-50		50	μA
I_{OZ}	High impedance state output current	$\overline{RE} = V_{CC1}$	-1		1	μA
R_{ID}	Differential input resistance	A, B	48			kohm
C_{ID}	Differential input capacitance	Test input signal is a 1.5MHz sine wave with $1V_{PP}$ amplitude, C_D is measured across A and B		7	10	pF
CMR	Common mode rejection	See Figure 26		4		V

6.11 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER ENABLED, RECEIVER DISABLED					
I_{CC1}	3 V: DE at 0 V		4	6	mA
	3 V: DE at V_{CC1} , 2 Mbps		5		mA
	3 V: DE at V_{CC1} , 25 Mbps		6		mA
	5.5 V: DE at 0 V		7	10	mA
	5.5 V: DE at V_{CC1} , 2 Mbps		8		mA
	5.5 V: DE at V_{CC1} , 25 Mbps		11		mA
I_{CC2}	5.25 V: DE at 0 V		15	18	mA
	5.25 V: DE at V_{CC1} , 2 Mbps, 54 ohm load		70		mA
	5.25 V: DE at V_{CC1} , 25 Mbps, 54 load ohm		75		mA

6.12 Electrical Characteristics: ISODE-Pin

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^\circ C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -8\text{ mA}$	$V_{CC2} - 0.4$	4.6	V
		$I_{OH} = -20\ \mu A$	$V_{CC2} - 0.1$	5	V
V_{OL}	Low-level output voltage	$I_{OL} = -8\text{ mA}$		0.2	0.4
		$I_{OL} = -20\ \mu A$		0	0.1

6.13 Switching Characteristics: Driver

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^\circ C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176						
t_{PHL} , t_{PLH}	Propagation delay	V_{CC1} at 5 V, V_{CC2} at 5 V			35	ns
tsk(p)	Pulse skew ($ t_{PHL} - t_{PLH} $)		2	7.5	ns	
t_{PHL} , t_{PLH}	Propagation delay	V_{CC1} at 3.3 V, V_{CC2} at 5 V			40	ns
tsk(p)	Pulse skew ($ t_{PHL} - t_{PLH} $)		2	7.5	ns	
t_r , t_f	Differential output rise time and fall time	See Figure 17	2	3	7.5	ns
t_{pDE}	DE to ISODE prop delay	See Figure 21			30	ns
$t_{(MLH)}$, $t_{(MHL)}$	Output transition skew	See Figure 18			1	ns
$t_{P(AZH)}$, $t_{P(BZH)}$, $t_{P(AZL)}$, $t_{P(BZL)}$	Propagation delay, high-impedance-to-active output	$C_L = 50$ pF, RE at 0 V, See Figure 19 and Figure 20			80	ns
$t_{P(AHZ)}$, $t_{P(BHZ)}$, $t_{P(ALZ)}$, $t_{P(BLZ)}$	Propagation delay time, active-to-high-impedance output				80	ns
$ t_{P(AZL)} - t_{P(BZH)} $, $ t_{P(AZH)} - t_{P(BZL)} $	Enable skew time		0.55	1.5	ns	
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See Figure 16		0.5		μs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	$T_A = 25^\circ C$, See Figure 16	100			μs

6.14 Switching Characteristics: Receiver

All typical specs are at $V_{CC1}=3.3V$, $V_{CC2}=5V$, $T_A=27^\circ C$, (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO1176						
t_{PHL} , t_{PLH}	Propagation delay	V_{CC1} at 5 V, V_{CC2} at 5 V			50	ns
tsk(p)	Pulse skew ($ t_{PHL} - t_{PLH} $)	V_{CC1} at 5 V, V_{CC2} at 5 V		2	7.5	ns
t_{PHL} , t_{PLH}	Propagation delay	V_{CC1} at 3.3 V, V_{CC2} at 5 V			55	ns
tsk(p)	Pulse skew ($ t_{PHL} - t_{PLH} $)	V_{CC1} at 3.3 V, V_{CC2} at 5 V		2	7.5	ns
t_r , t_f	Differential output rise time and fall time	See Figure 17		2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC1} , See Figure 24		13	25	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		13	25	ns	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC} , See Figure 25		13	25	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output		13	25	ns	

6.15 Insulation Characteristics Curves

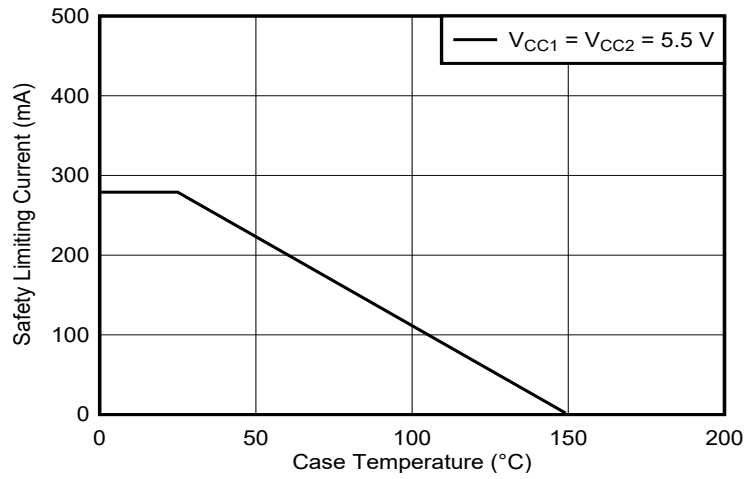
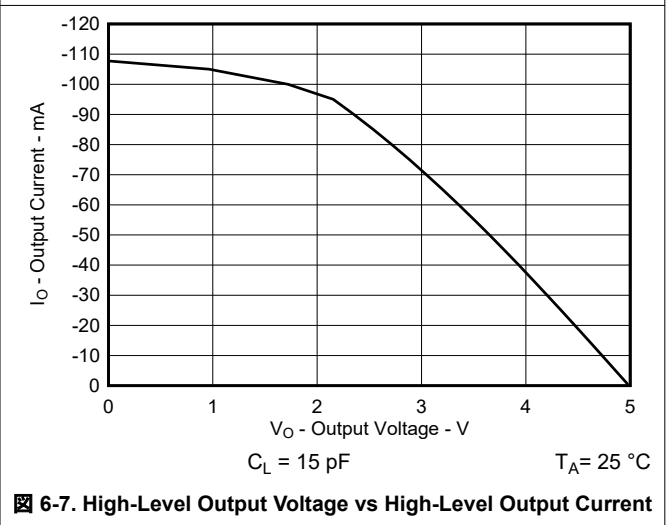
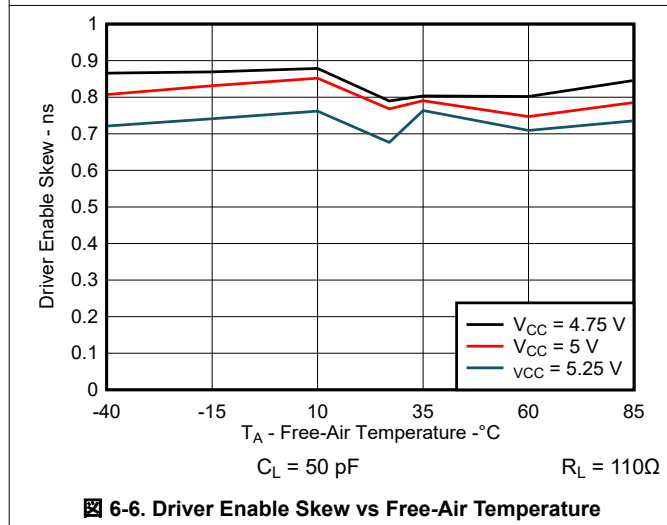
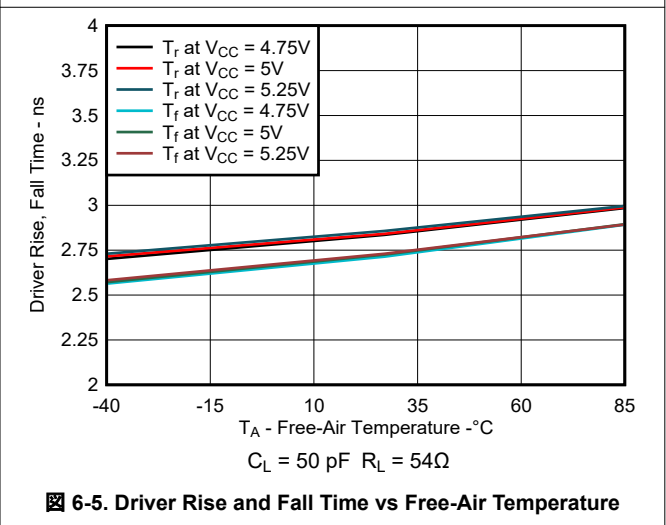
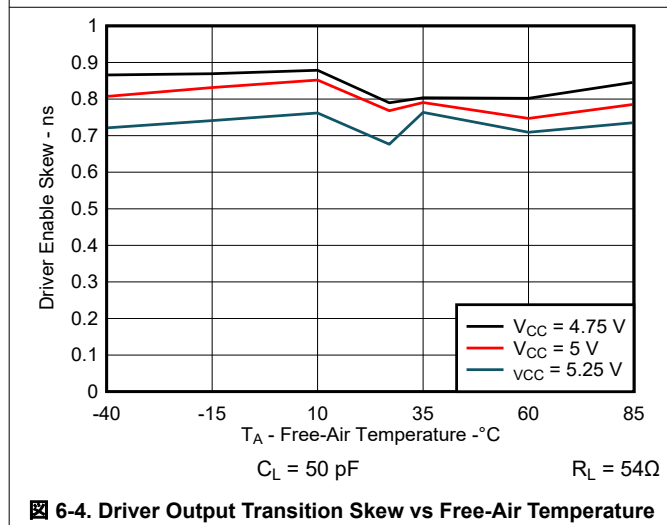
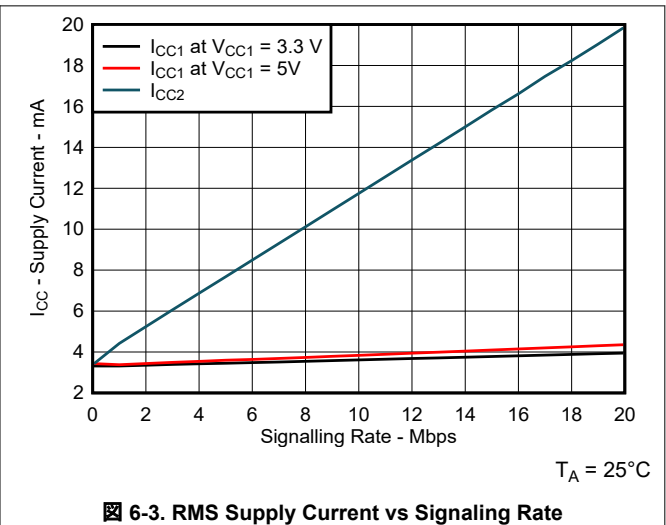
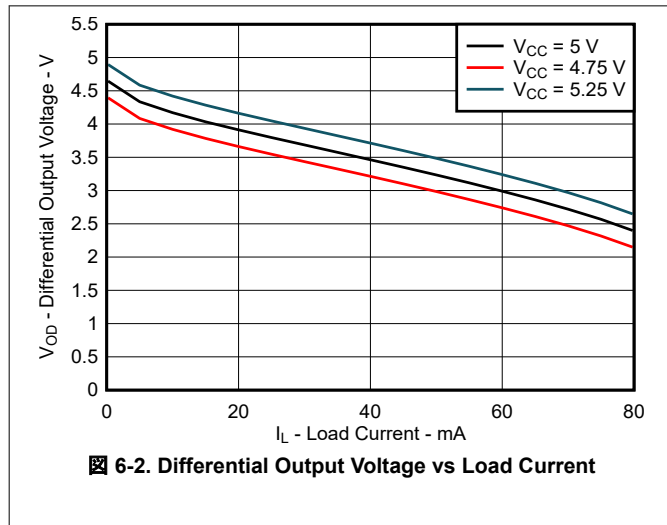
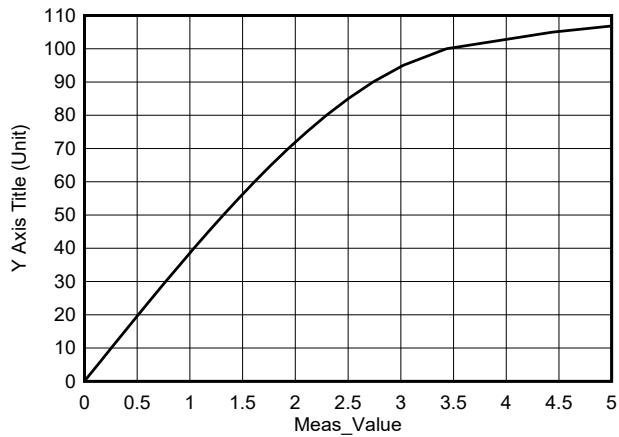


图 6-1. Thermal Derating Curve for Limiting Power per VDE

6.16 Typical Characteristics



6.16 Typical Characteristics (continued)

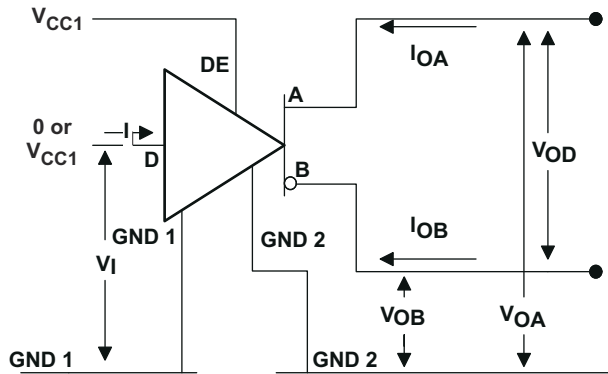


$C_L = 15 \text{ pF}$

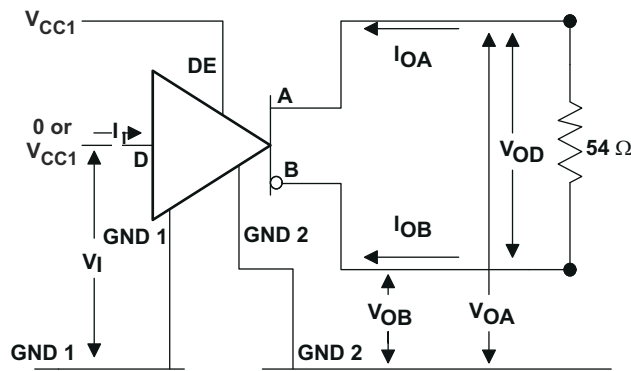
$T_A = 25 \text{ }^\circ\text{C}$

6-8. Low-Level Output Voltage vs Low-Level Output Current

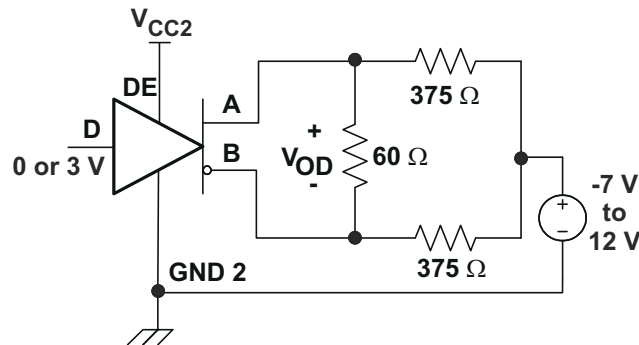
7 Parameter Measurement Information



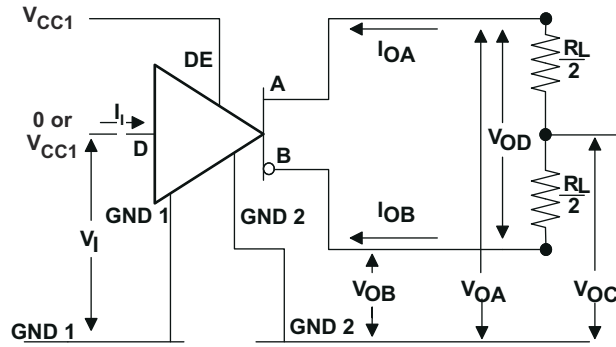
7-1. Open Circuit Voltage Test Circuit



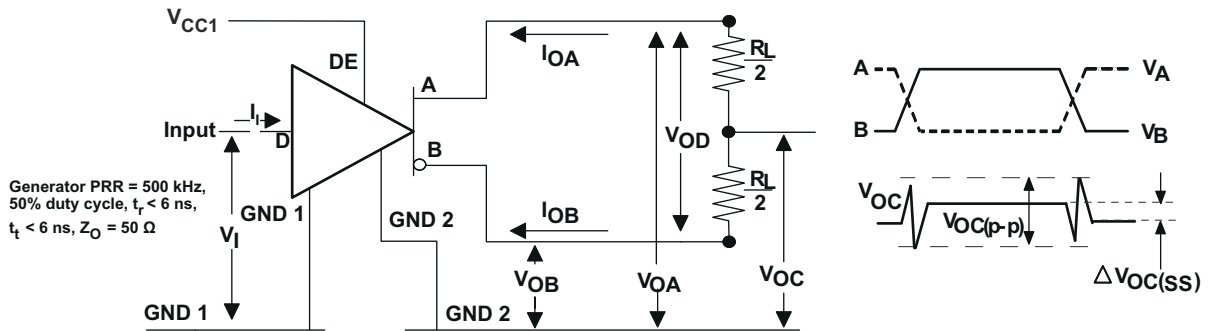
7-2. V_{OD} Test Circuit



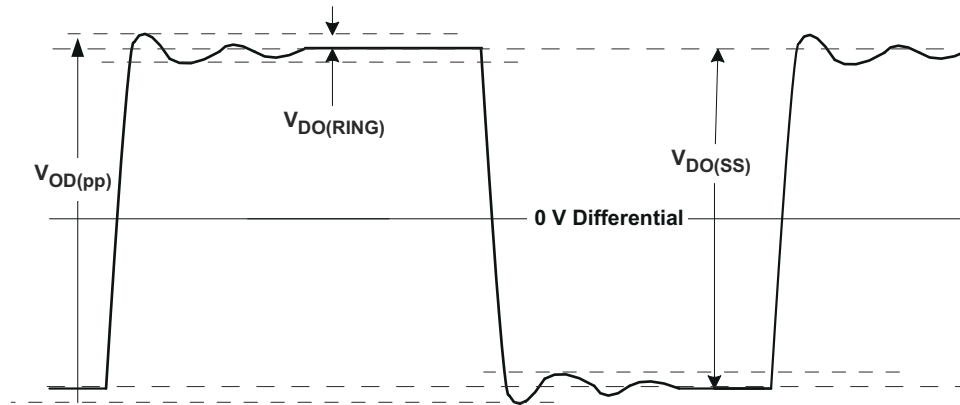
7-3. Driver V_{OD} With Common-Mode Loading Test Circuit



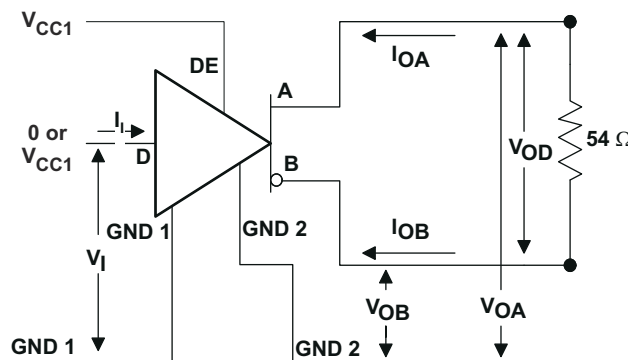
 **7-4. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit**



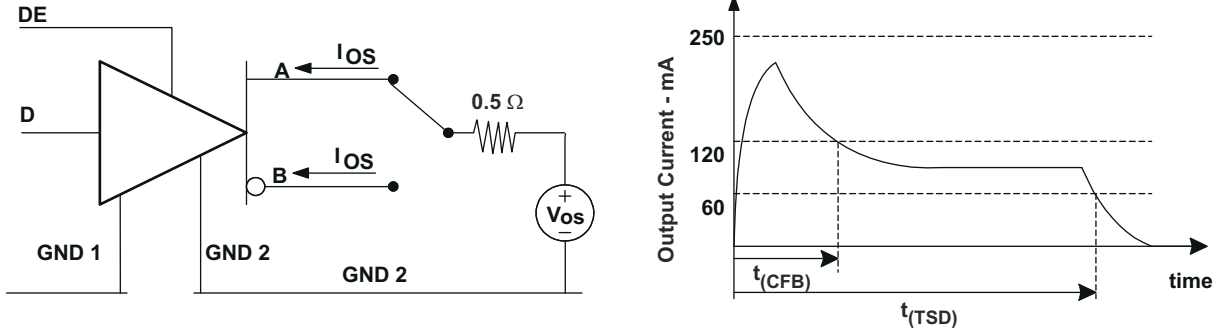
 **7-5. Steady-State Output Voltage Test Circuit and Voltage Waveforms**



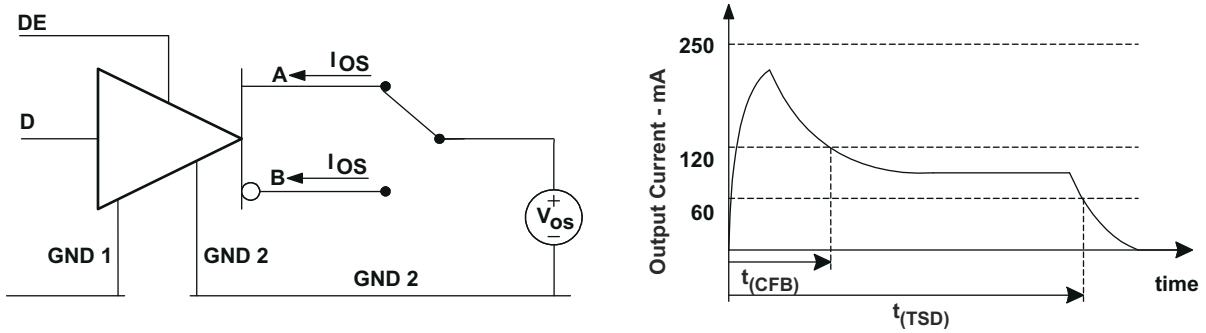
 **7-6. $V_{OD(RING)}$ Waveform and Definitions**



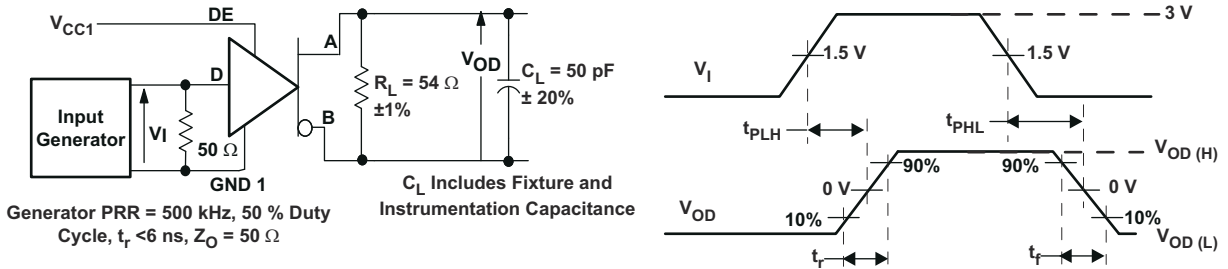
 **7-7. Input Voltage Hysteresis Test Circuit**



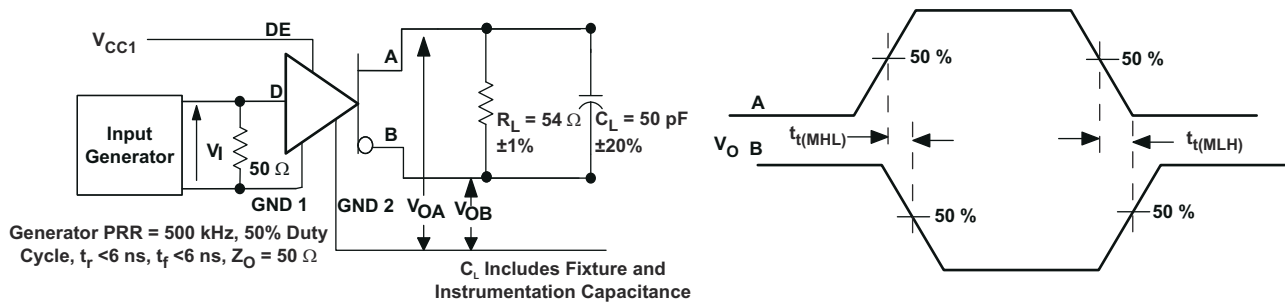
7-8. Driver Short-Circuit Test Circuit and Waveforms (Short-Circuit Applied at Time t=0)



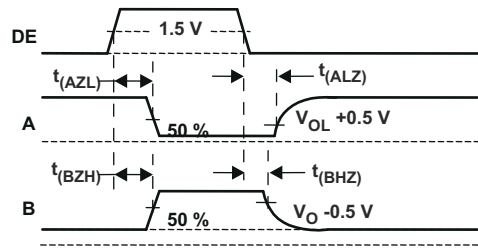
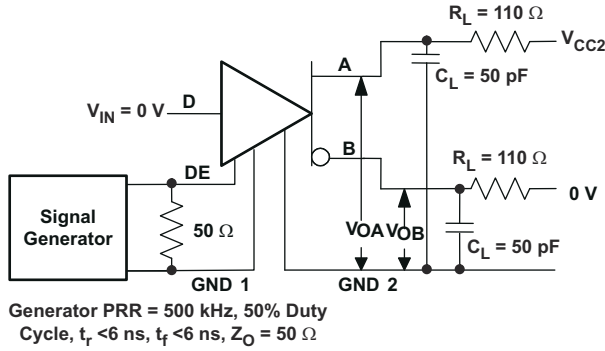
7-9. $I_{OS(ss)}$ Steady State Short-Circuit Output Current Test Circuit



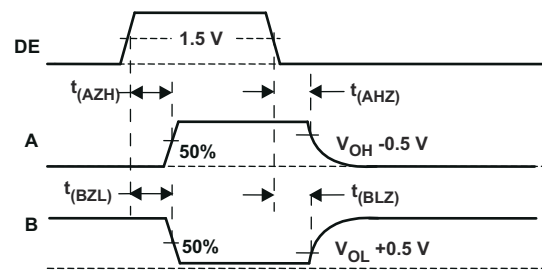
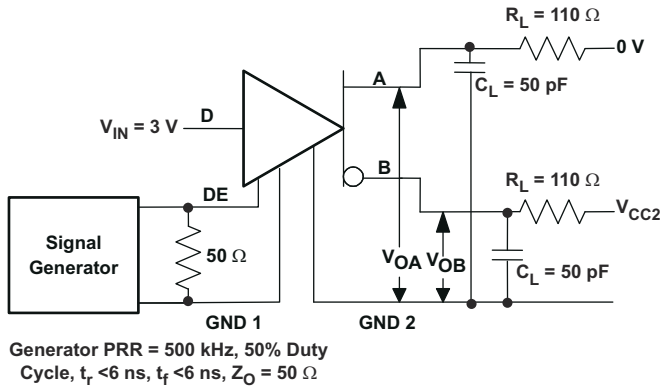
7-10. Driver Switching Test Circuit and Waveforms



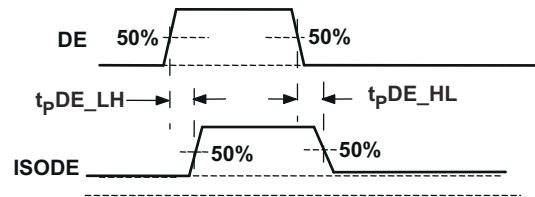
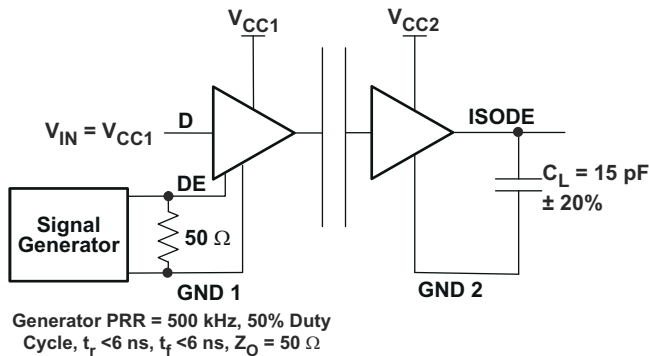
7-11. Driver Output Transition Skew Test Circuit and Waveforms



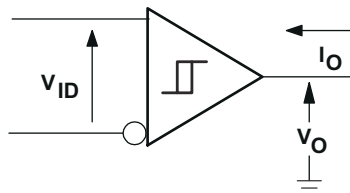
7-12. Driver Enable and Disable Test, D at Logic Low Test Circuit and Waveforms



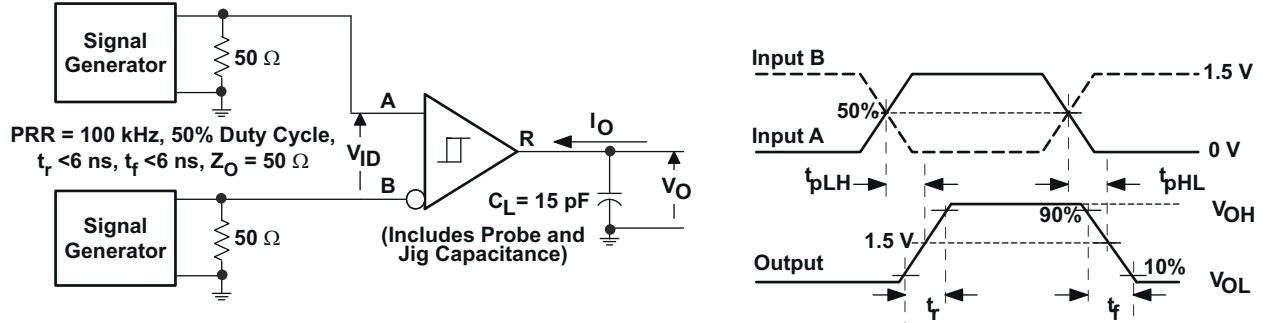
7-13. Driver Enable and Disable Test, D at Logic High Test Circuit and Waveforms



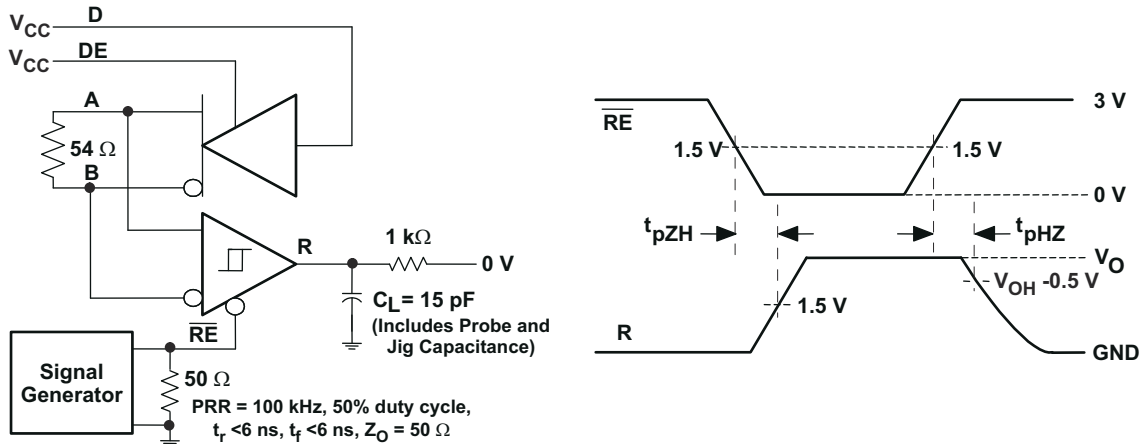
7-14. DE to ISODE Prop Delay Test Circuit and Waveforms



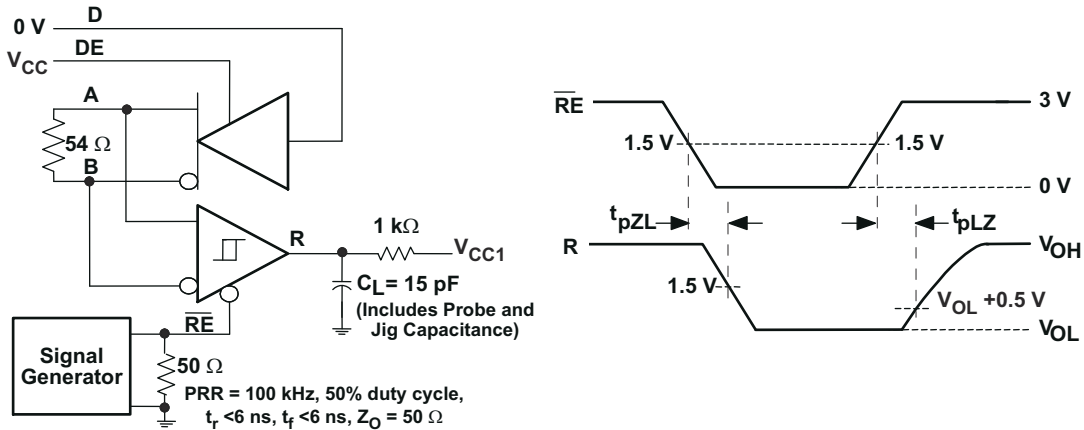
7-15. Receiver DC Parameter Definitions



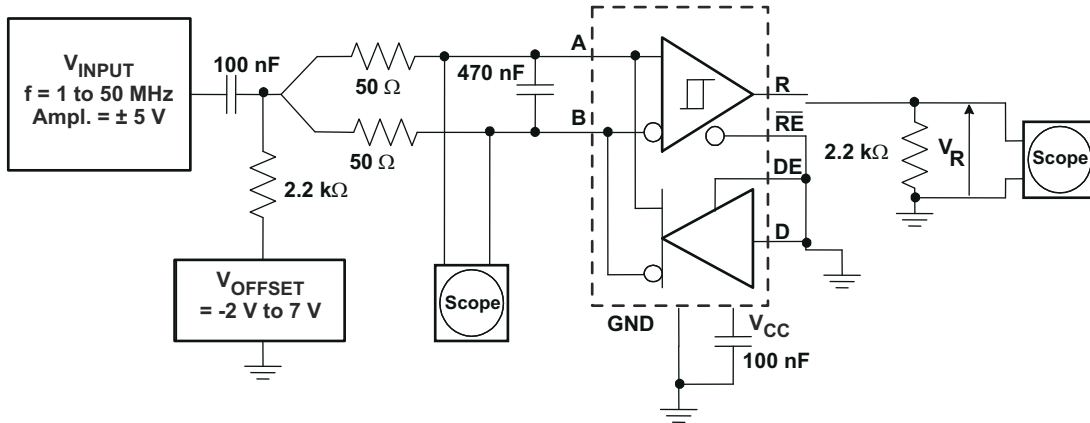
7-16. Receiver Switching Test Circuit and Waveforms



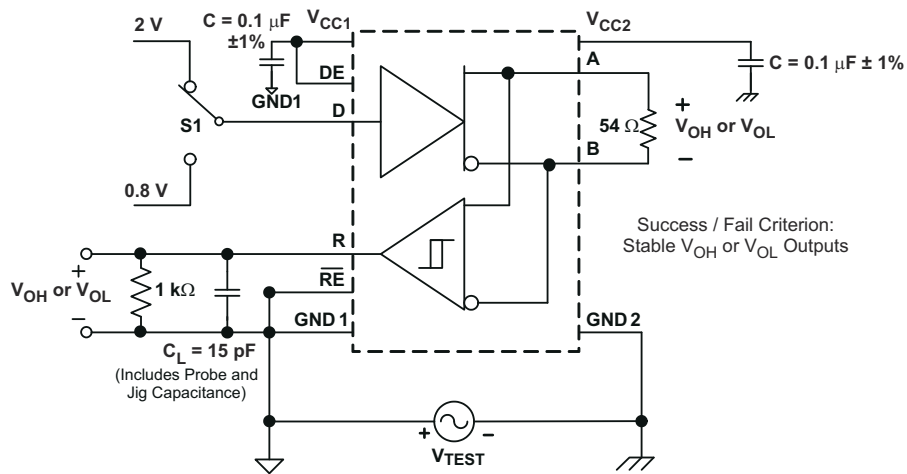
7-17. Receiver Enable Test Circuit and Waveforms, Data Output High



7-18. Receiver Enable Test Circuit and Waveforms, Data Output Low



7-19. Common-Mode Rejection Test Circuit



7-20. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

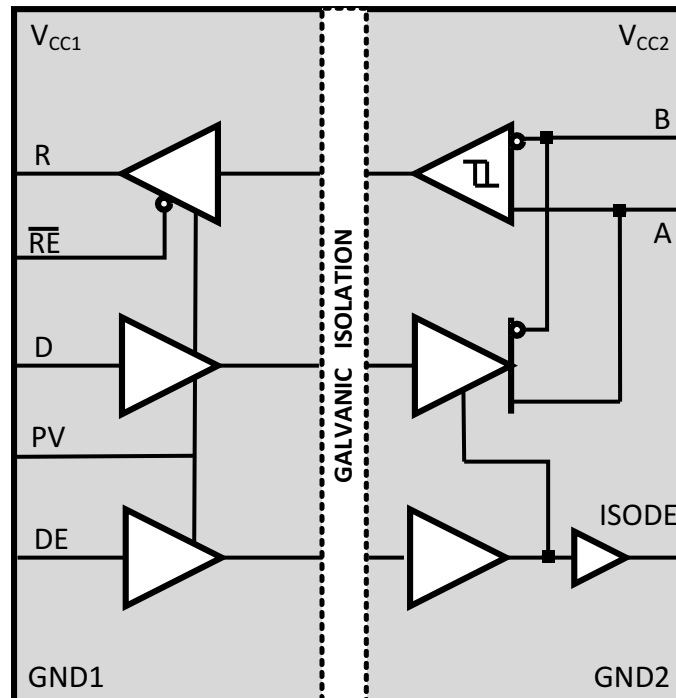
8.1 Overview

The ISO1176 is an isolated half-duplex differential line transceiver that meets the requirements of EN 50170 and TIA/EIA 485/422 applications. The device is rated to provide galvanic isolation of up to 2500 V_{RMS} for 60 s per UL 1577. The device has active-high driver enable and active-low receiver enable functions to control the data flow. The device has maximum data transmission speed of 40 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_{(A)} - V_{(B)}$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} - V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate. When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

8.2 Functional Block Diagram



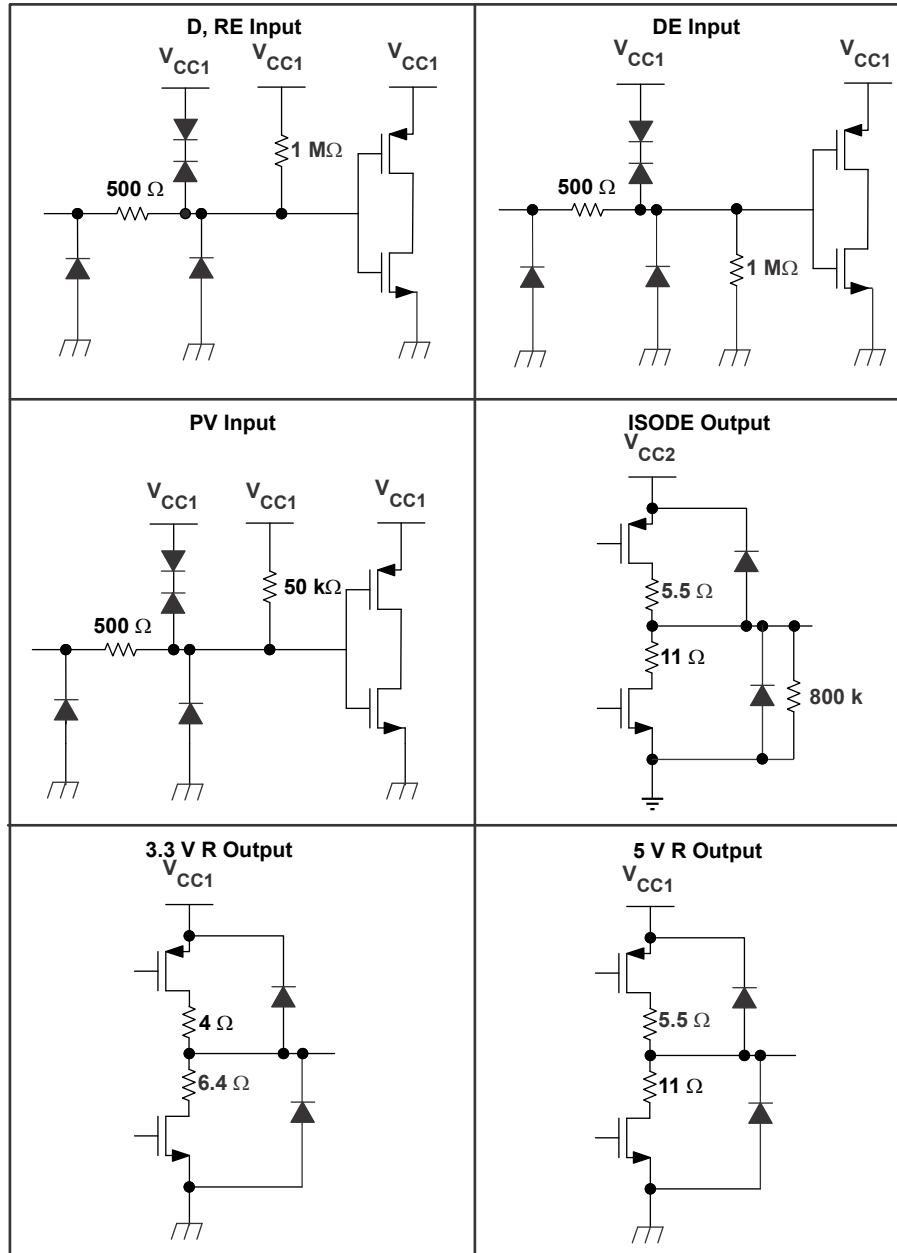
8.3 Device Functional Modes

表 8-1. Driver Function Table

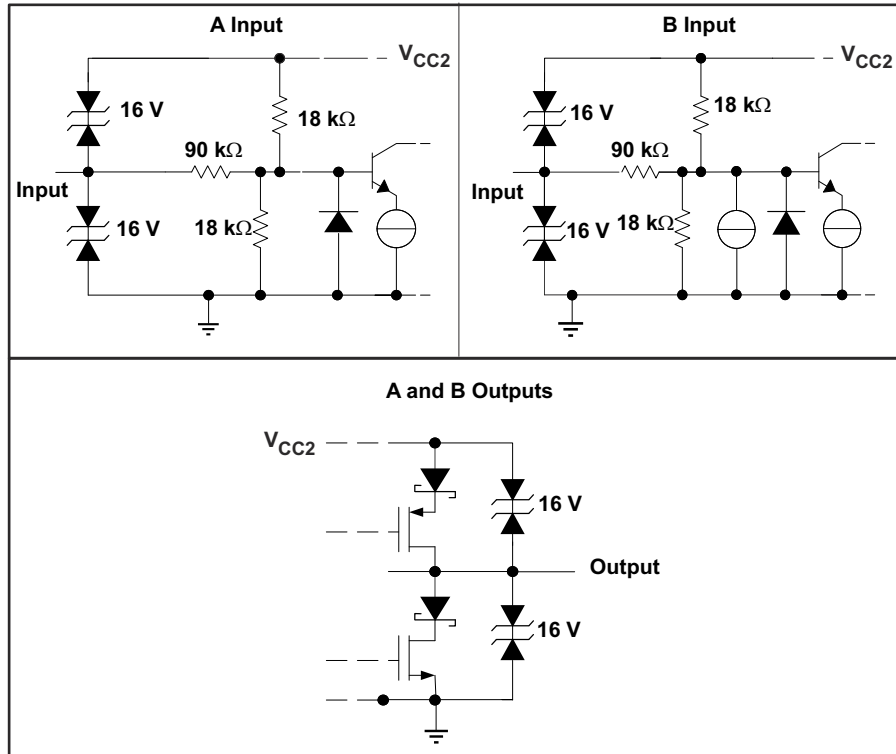
V _{CC1}	V _{CC2}	POWER VALID (PV) (ISO1176)	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
						A	B
PU	PU	H or open	H	H	H	H	L
PU	PU	H or open	L	H	H	L	H
PU	PU	H or open	X	L	L	Z	Z
PU	PU	H or open	X	open	L	Z	Z
PU	PU	H or open	open	H	H	H	L
PD	PU	X	X	X	L	Z	Z
PU	PD	X	X	X	L	Z	Z
PD	PD	X	X	X	L	Z	Z
X	X	L	X	X	L	Z	Z

表 8-2. Receiver Function Table

V _{CC1}	V _{CC2}	POWER VALID (PV) (ISO1176)	DIFFERENTIAL INPUT V _{ID} = (V _A – V _B)	ENABLE (RE)	OUTPUT (R)
PU	PU	H or open	$-0.01\text{ V} \leq V_{ID}$	L	H
PU	PU	H or open	$-0.2\text{ V} < V_{ID} < -0.01\text{ V}$	L	?
PU	PU	H or open	$V_{ID} \leq -0.2\text{ V}$	L	L
PU	PU	H or open	X	H	Z
PU	PU	H or open	X	open	Z
PU	PU	H or open	Open-circuit	L	H
PU	PU	H or open	Short-circuit	L	H
PU	PU	H or open	Idle (terminated) bus	L	H
PD	PU	X	X	X	Z
PU	PD	H or open	X	L	H
PD	PD	X	X	X	Z
X	X	L	X	X	Z



8-1. Equivalent I/O Schematics



 8-2. Equivalent I/O Schematics for A and B Inputs and Outputs

9 Application and Implementation

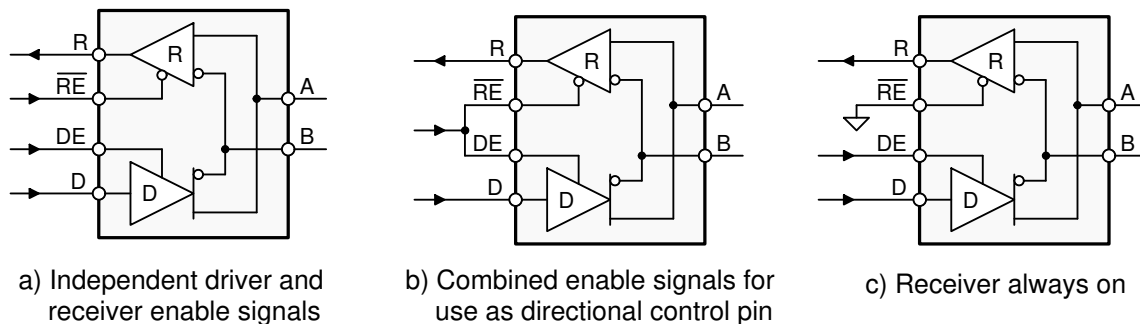
注

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9.1 Application Information

The ISO1176 device consists of a RS-485 transceiver, commonly used for asynchronous data transmissions. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, $R(T)$, whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

9.2 Typical Application



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図 9-1. Half-Duplex Transceiver Configurations

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

表 9-1. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 k Ω to 10 k Ω
Decoupling Capacitors	100 nF

9.2.2 Detailed Design Procedure

Isolating of a circuit insulates it from other circuits and earth, so that noise voltage develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation. The transient ratings of the ISO1176 standard are sufficient for all but the most severe installations. However, some equipment manufacturers use ESD generators to test equipment transient susceptibility. This practice can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high-voltage transients.

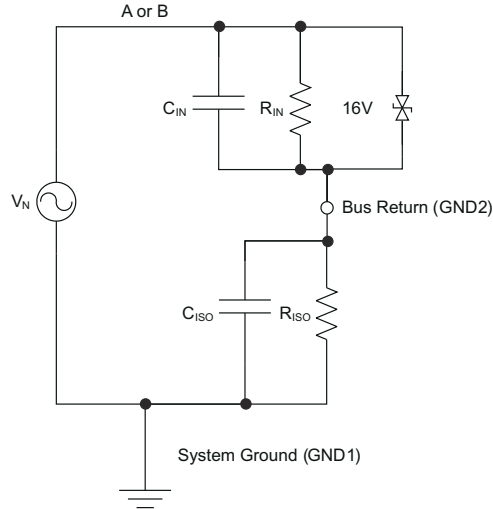


图 9-2. Device Model for Static Discharge Testing

图 9-2 models the ISO1176 bus IO connected to a noise generator. C_{IN} and R_{IN} is the device, and any other stray or added capacitance or resistance across the A or B pin to GND2. C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of the ISO1176, plus those of any other insulation (transformer, and so forth). Stray inductance is assumed to be negligible.

9.2.2.1 Transient Voltages

From this model, the voltage at the isolated bus return is

$$V_{GND2} = V_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \quad (1)$$

and is always less than 16 V from V_N . If the ISO1176 is tested as a stand-alone device,

- $R_{IN} = 6 \times 10^4 \Omega$,
- $C_{IN} = 16 \times 10^{-12} \text{ F}$,
- $R_{ISO} = 10^9 \Omega$ and
- $C_{ISO} = 10^{-12} \text{ F}$.

Notice from 图 9-2 that the resistor ratio determines the voltage ratio at low frequencies, and that the inverse capacitance ratio determines the voltage ratio at high frequencies. In the stand-alone case and for low frequencies,

$$\frac{V_{GND2}}{V_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4} \quad (2)$$

or essentially all of the noise appears across the barrier.

At high frequencies,

$$\frac{V_{GND2}}{V_N} = \frac{1/C_{ISO}}{1/C_{ISO} + 1/C_{IN}} = \frac{1}{1 + C_{ISO}/C_{IN}} = \frac{1}{1 + 1/16} = 0.94 \quad (3)$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN} , most of the transient noise appears across the isolation barrier, as it should.

Using ESD generators to test equipment transient susceptibility, or considering product claims of ESD ratings greater than the barrier transient ratings of an isolated interface is not recommended. ESD is best managed through recessing or covering connector pins in a conductive connector shell, and by proper installer training.

9.2.2.2 ISO1176 “Sticky Bit” Issue (Under Certain Conditions)

Summary: In applications with sufficient differential noise on the bus, the output of the ISO1176 receiver may “stick” at an incorrect state for up to 30 μ s.

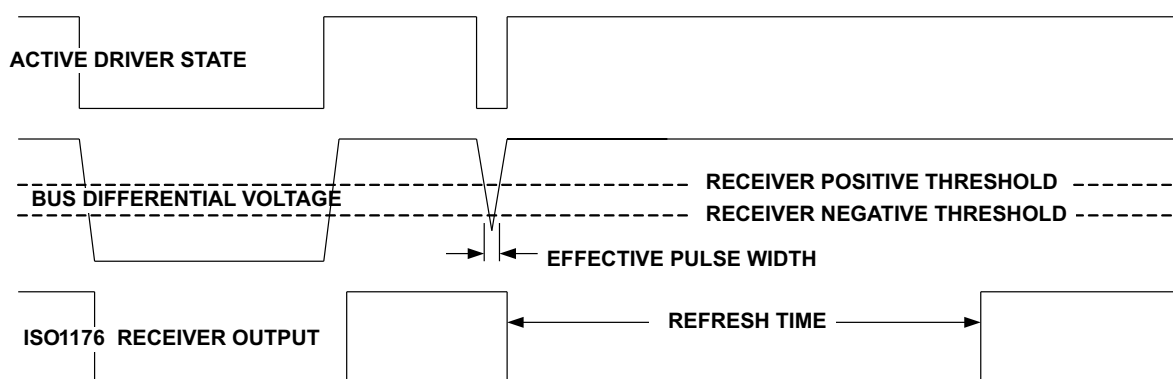
Description: The ISO1176 isolated Profibus (RS-485) transceiver is rated for signaling up to 40 Mbps on twisted-pair bus lines. The receiver thresholds comply with RS-485 and Profibus specifications; an input differential voltage $V_{ID} = V_A - V_B > 200$ mV causes a logic High on the R output, and $V_{ID} < -200$ mV causes a logic Low on the R output. To assure a known receiver output when the bus is shorted or idle, the upper threshold is set below zero, such that $V_{ID} = 0$ mV causes a logic High on the R output. The data sheet specifies a typical upper threshold (V_{IT+}) of -80 mV and a typical lower threshold (V_{IT-}) of -120 mV.

At a signaling rate of 40 Mbps, each valid data bit has a duration of 25 ns. At typical Profibus signaling rates of 12 Mbps or lower, each valid data bit has a duration of 83 ns or more. The ISO1176 correctly sets the R output for each of these valid data bits.

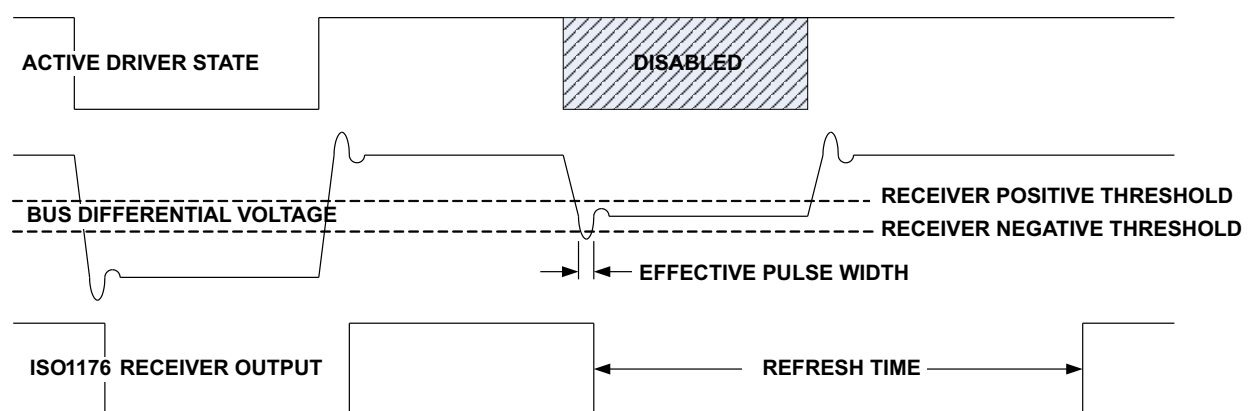
In applications with a high degree of differential noise on the bus lines, it is possible to get short periods when an invalid bus voltage triggers a change in state of the internal receiver circuits. An issue with the digital isolation channel in the ISO1176 may cause the invalid receiver state to “stick” rather than immediately transition back to the correct state. The receiver output will always transition to the correct state, but may stick in the incorrect state for up to 30 μ s. This can cause a temporary loss of data.

☒ 9-3 shows two cases which could result in temporary loss of data.

Case 1



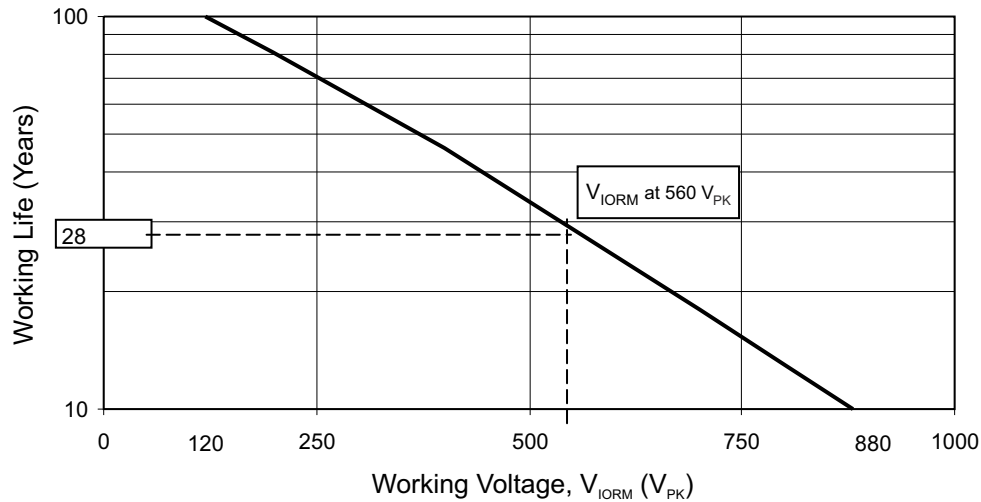
Case 2



☒ 9-3. “Sticky Bit” Issue Waveforms

9.2.3 Application Curve

At maximum working voltage, ISO1176 isolation barrier has more than 28 years of life.



9-4. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1 μF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's [SN6501](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501](#) data sheet ([SLLSEA0](#)).

11 Layout

11.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 11-1](#)).

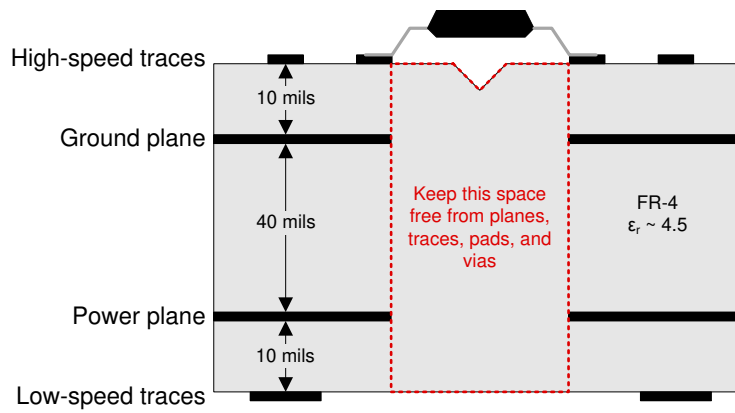
- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1- μ F bypass capacitors as close as possible to the V_{CC} -pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-k Ω to 10-k Ω pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

注

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, [SLLA284](#).

11.2 Layout Example



11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide application report](#)
- Texas Instruments, [Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [Isolation Glossary application report](#)

12.2 サポート・リソース

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12.4 静電気放電に関する注意事項



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12.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1176DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176DWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ISO1176DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO1176DWG4	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

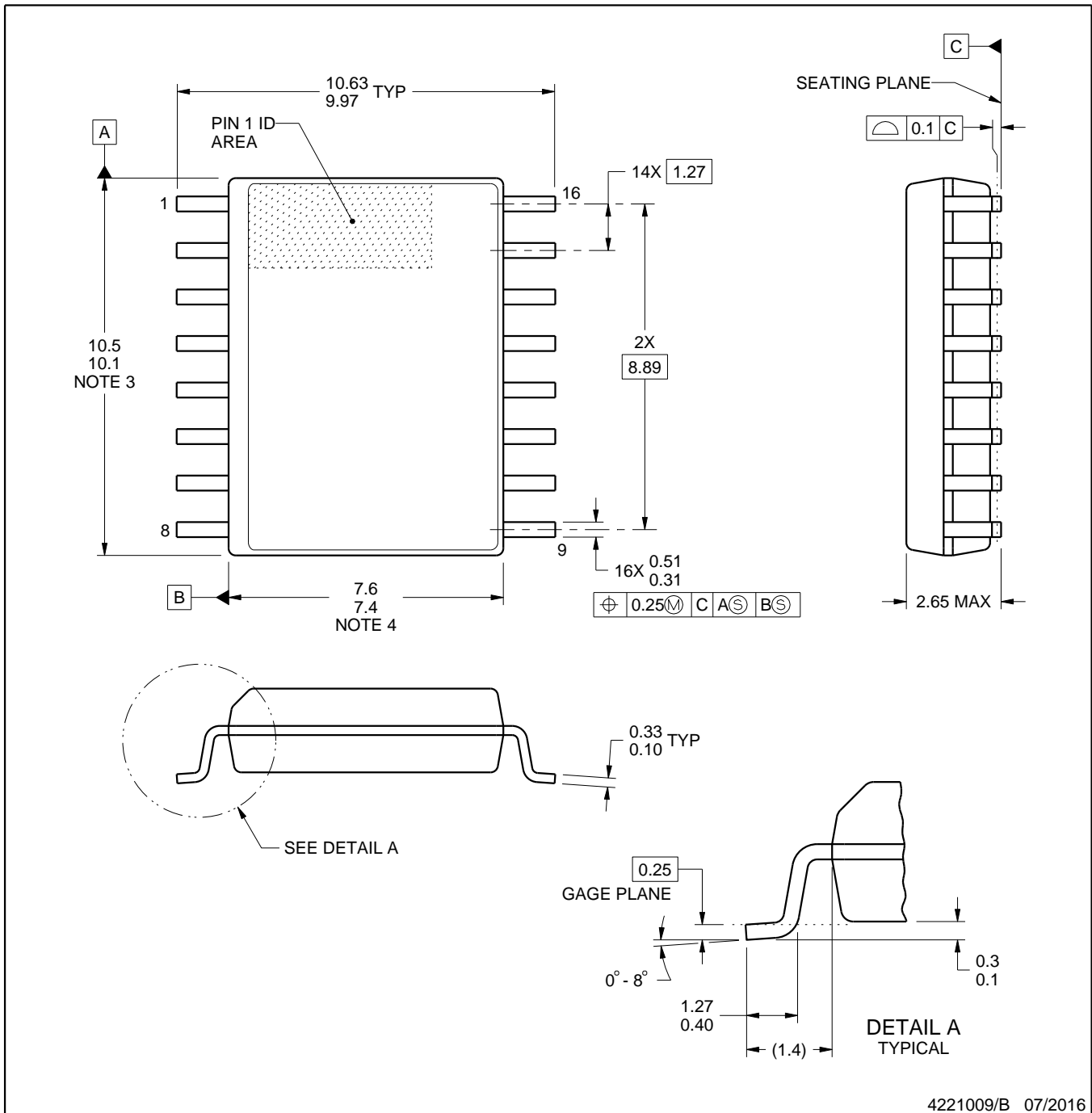


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

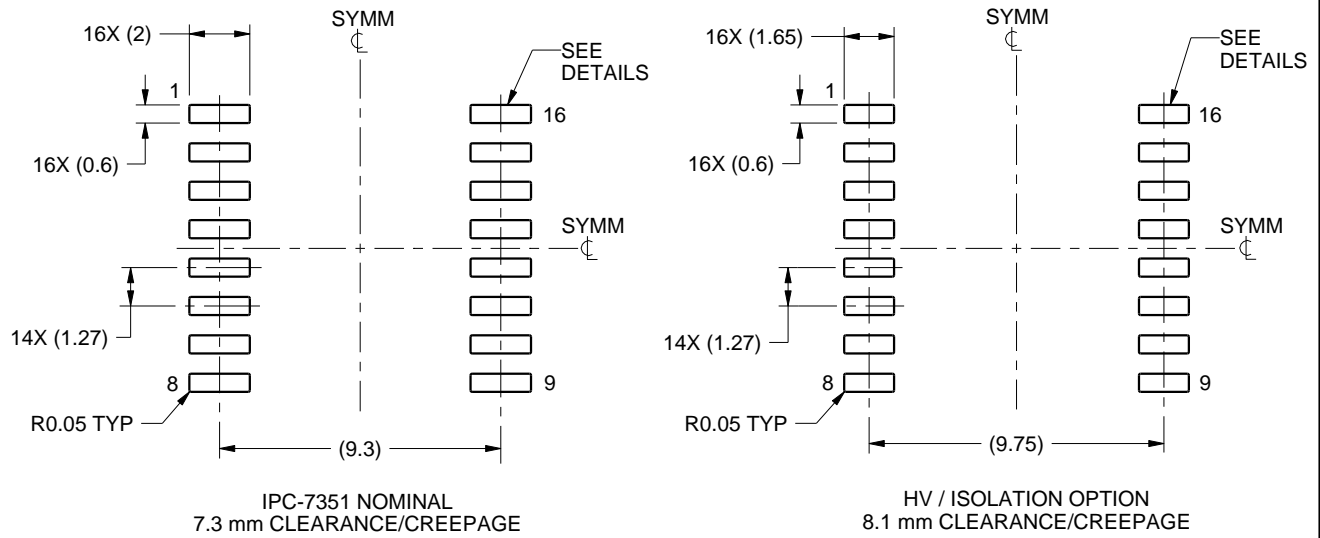
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

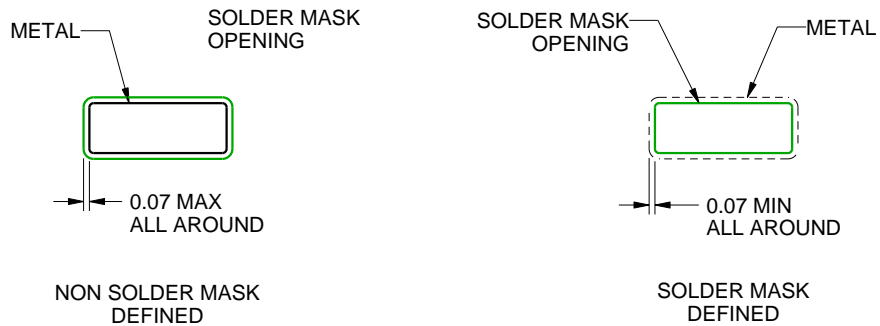
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

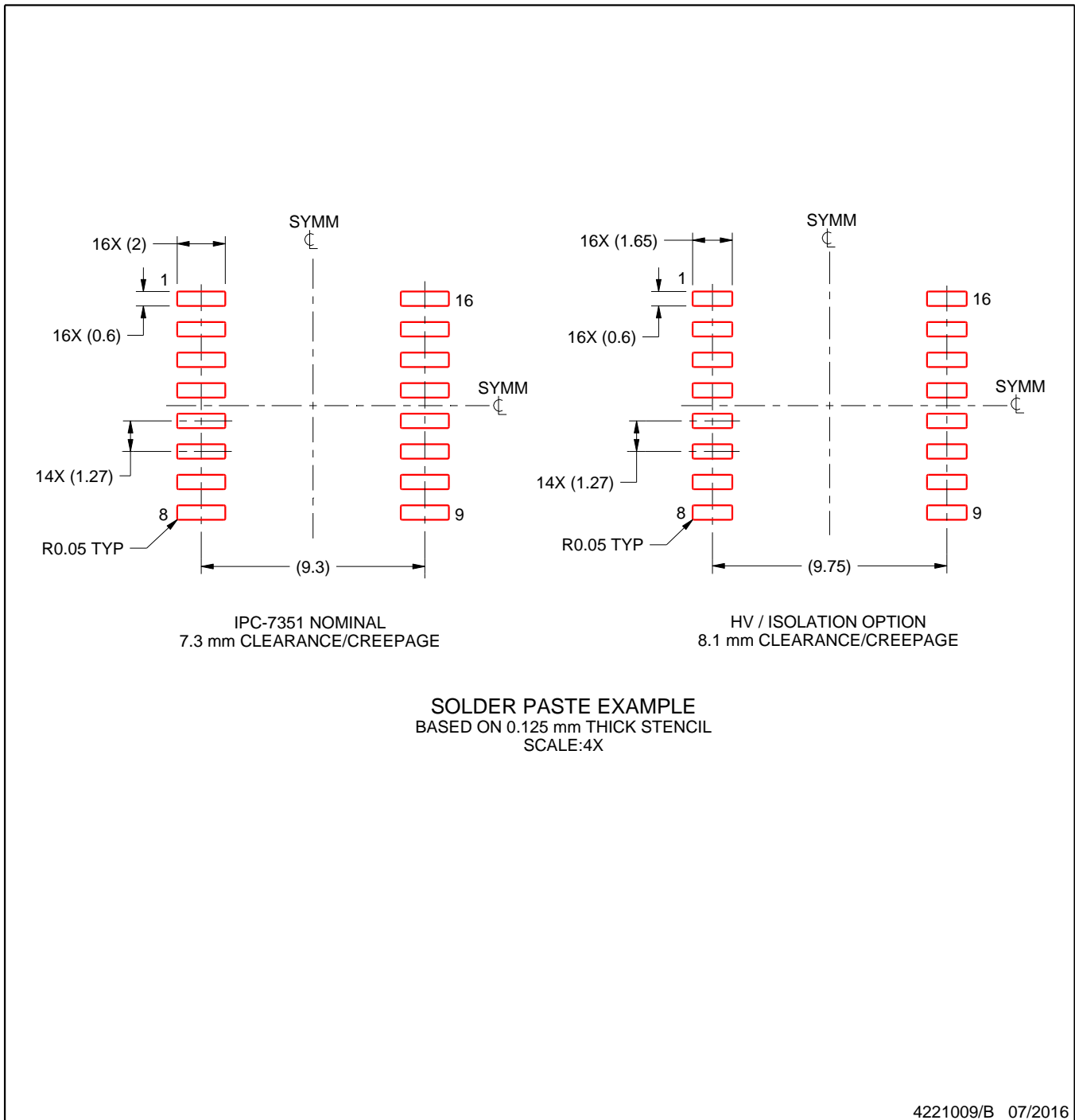
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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