ISO722x-Q1 デュアル チャネル デジタル アイソレータ

1 特長

- 1 および 25Mbps の信号速度オプション
  - 低いチャネル間の出力スキュー:
    最大値 1ns
  - 低いパルス幅歪み (PWD) :最大値 1ns
  - 低ジッタ成分:25Mbps で標準値 1ns
- 50kV/µs の標準過渡電圧耐性
- 2.8V (C グレード)、
  3.3V、または 5V の電源で動作
- ESD 保護:4kV
- 動作温度範囲: -40℃～+125℃
- 定格電圧で標準寿命 28 年
  (「絶縁寿命予測」を参照)
- 安全関連の認証
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1 認定、IEC 62368-1 認定

2 アプリケーション

- ファクトリ オートメーション
  - Modbus
  - Profibus™
  - DeviceNet™ データ バス
- コンピュータ ペリフェラル インターフェイス
- サーボ制御インターフェイス
- データ アクイジション

3 概要

ISO7220x-Q1 および ISO7221x-Q1 ファミリのデバイスは、デュアル チャネルのデジタル アイソレータです。PCB レイアウトを容易にするために、チャネルは ISO7220x-Q1 では同じ方向、ISO7221x-Q1 では反対方向に配置されています。これらのデバイスはテキサス・インスツルメンツのシリコン酸化膜 (SiO_2) 絶縁バリアによって分離されたロジック入出力バッファを搭載しており、VDE に準拠した最大 $4000V_{PK}$ のガルバニック絶縁を提供します。これらのデバイスを絶縁型電源と組み合わせて使用すると、高電圧がブロックされ、グランドが絶縁されます。また、データ バスや他の回路で発生したノイズ電流がローカル グランドに入り込み、ノイズに敏感な回路に干渉または損傷を与えることを防止できます。

バイナリ入力信号がコンディショニングされ、バランスされた信号に変換されてから、容量性絶縁バリアによって差動化されます。絶縁バリアを通過して、差動コンパレータがロジック変換情報を受け取り、それに応じてフリップフロップおよび出力回路を設定またはリセットします。バリアを通して周期的に更新パルスが送信され、出力の DC レベルが適切であることを検証します。この DC 更新パルスが 4µs ごとに受信されない場合、入力に電力が供給されていない、またはアクティブに駆動されていないと見なされ、フェイルセーフ回路により出力が論理 HIGH 状態に駆動されます。

容量が小さく、その結果として時定数も小さいため、高速な動作が可能で、0Mbps (DC) から 25Mbps までの信号速度に対応できます (ラインの信号速度は、1 秒あたりの電圧遷移回数であり、bps 単位で表されます)。A オプションおよび C オプションのデバイスは、入力に TTL 入力しきい値とノイズ フィルタを備えており、過渡的パルスがデバイスの出力に渡されることを防止します。M オプションのデバイスには CMOS $V_{CC}/2$ 入力しきい値が存在しますが、入力ノイズ フィルタはなく、追加の伝搬遅延が発生しません。

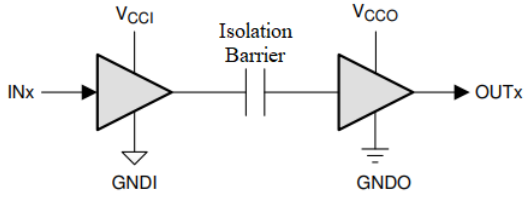
ISO7220x-Q1 および ISO7221x-Q1 ファミリのデバイスは、2.8V (C グレード)、3.3V、5V、またはいずれかの組み合わせの 2 つの電源電圧を必要とします。2.8V または 3.3V 電源で動作するとき、すべての入力は 5V 許容で、すべての出力は 4mA CMOS です。

ISO7220x-Q1 および ISO7221x-Q1 ファミリのデバイスは、-40℃～+125℃の周囲温度範囲で動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO7220x-Q1	D (SOIC、8)	4.90mm × 3.91mm	4.9mm × 6mm
ISO7221x-Q1			

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{CCI} および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。
V_{CCO} および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

概略回路図

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4 Pin Configuration and Functions

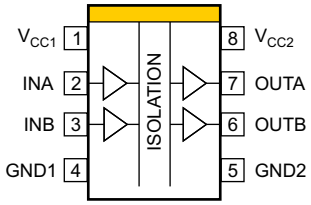


図 4-1. ISO7220x-Q1 D Package 8-Pin SOIC Top View

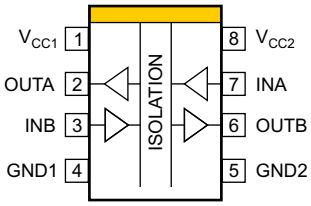


図 4-2. ISO7221x-Q1 D Package 8-Pin SOIC Top View

表 4-1. Pin Functions

PIN			Type[1]	DESCRIPTION
NAME	ISO7220x-Q1	ISO7221x-Q1		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

Parameter		Value
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	–0.5 V to 6 V
V_I	Voltage at IN, OUT	–0.5 V to V_{CC} + 0.5 V(2)
I_O	Output current	±15 mA
T_J	Maximum junction temperature	150°C
T_{stg}	Storage temperature	–65°C to 150°C

(1) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(2) Maximum voltage must not exceed 6 V.

5.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1)	V_{CC1}, V_{CC2}	3		5.5	V
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse width	ISO722xA-Q1	1			µs
		ISO722xC-Q1	40			ns
$1/t_{ui}$	Signaling rate	ISO722xA-Q1	0		1000	kbps
		ISO722xC-Q1	0		25	Mbps
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
T_A	Ambient temperature		–40		125	°C
T_J	Operating virtual-junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.3 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

5.4 Thermal Information

THERMAL METRIC(1)			ISO7220x-Q1 ISO7221x-Q1	UNIT
			D (SOIC)	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(1)	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter		47.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

5.5 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Thermal Information			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Thermal Information			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIORM , tm = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.3 × VIORM, tm = 10 s	≤5	
		Method b: At routine test (100% production); Vini = 1.2 x VIOTM, tini = 1s; Vpd(m) = 1.5 x VIORM, tm = 1s (method b1) or Vpd(m) = Vini, tm = tini (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(4)	VIO = 0.4 x sin (2πft), f = 1 MHz	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Electrical Characterstics

V_{CC1} = 3.3 V, V_{CC2} = 5 V(1), over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x-Q1				4.3	9.5	
		ISO7220A-Q1	1 Mbps			1	2	
		ISO7221A-Q1				5	11	
		ISO7221C-Q1	25 Mbps			6	12	
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x-Q1				8.5	17	
		ISO7220A-Q1	1 Mbps			18	32	
		ISO7221A-Q1				10	18	
		ISO7221C-Q1	25 Mbps			12	22	
V_{OH}	High-level output voltage		ISO7220x-Q1	I_{OH} = –4 mA	V_{CC} – 0.8			V
			ISO7221x-Q1 (3.3-V side)		V_{CC} – 0.4			
				I_{OH} = –20 µA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage			IOL = 4 mA			0.4	V
				IOL = 20 µA		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See 図 6-3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.8 Electrical Characteristics

V_{CC1} = V_{CC2} = 3.3 V[1], over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x-Q1				4.3	9.5	
		ISO7220A-Q1	1 Mbps			1	2	
		ISO7221A-Q1				5	11	
		ISO7221C-Q1	25 Mbps			6	12	
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x-Q1				4.3	9.5	
		ISO7220A-Q1	1 Mbps			9	19	
		ISO7221A-Q1				5	11	
		ISO7221C-Q1	25 Mbps			6	12	
V_{OH}	High-level output voltage			I_{OH} = –4 mA	V_{CC} – 0.4	3		V
				I_{OH} = –20 µA	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage			I_{OL} = 4 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V or V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See 図 6-3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.9 Electrical Characteristics

V_{CC1} = 5 V, V_{CC2} = 3.3 V(1), over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x-Q1				8.5	17	
		ISO7220A-Q1	1 Mbps	V_I = V_{CC} or 0 V, no load		2	3	
		ISO7221A-Q1				10	18	
		ISO7221C-Q1	25 Mbps	V_I = V_{CC} or 0 V, no load		12	22	
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x-Q1				4.3	9.5	
		ISO7220A-Q1	1 Mbps	V_I = V_{CC} or 0 V, no load		9	19	
		ISO7221A-Q1				5	11	
		ISO7221C-Q1	25 Mbps	V_I = V_{CC} or 0 V, no load		6	12	
V_{OH}	High-level output voltage		ISO7220x-Q1	I_{OH} = –4 mA	V_{CC} – 0.4			V
			ISO7221x-Q1 (5-V side)		V_{CC} – 0.8			
				I_{OH} = –20 µA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage			I_{OL} = 4 mA			0.4	V
				I_{OL} = 20 µA			0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See 図 6-3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.10 Electrical Charcteristics

V_{CC1} and V_{CC2} at 5 V[1], over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current, V_{CC1}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x-Q1				8.5	17	
		ISO7220A-Q1	1 Mbps			2	3	
		ISO7221A-Q1				10	18	
		ISO7221C-Q1	25 Mbps			12	22	
I_{CC2}	Supply current, V_{CC2}	ISO7220x-Q1	Quiescent	V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x-Q1				8.5	17	
		ISO7220A-Q1	1 Mbps			17	32	
		ISO7221A-Q1				10	18	
		ISO7221C-Q1	25 Mbps			12	22	
V_{OH}	High-level output voltage			I_{OH} = –4 mA	V_{CC} – 0.8	4.6		V
				I_{OH} = –20 µA	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage			I_{OL} = 4 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current			IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			IN from 0 V to V_{CC}	–10			µA
C_I	Input capacitance to ground			IN at VCC, VI = 0.4 sin (2πft), f=2MHz		1		pF
CMTI	Common-mode transient immunity			V_I = V_{CC} or 0 V, See 図 6-3	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

5.11 Switching Characteristics

V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10%, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA-Q1	See 図 6-1	268	395	605	ns
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$[1]				1	22	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC-Q1	See 図 6-1	21	36	48	ns
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$[1]				1	3	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO722xA-Q1				190	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 図 6-1		2.3		ns
t_f	Output signal fall time		See 図 6-1		2.3		ns
t_{fs}	Failsafe output delay time from input power loss		See 図 6-2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.12 Switching Characteristics

V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10%, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA-Q1	See 図 6-1	253	410	585	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	18	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC-Q1	See 図 6-1	21	36	48	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA-Q1				180	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 図 6-1		2.3		ns
t_f	Output signal fall time		See 図 6-1		2.3		
t_{fs}	Failsafe output delay time from input power loss		See 図 6-2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.13 Switching Characteristics

V_{CC1} = V_{CC2} = 3.3 V ± 10%, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA-Q1	See 図 6-1	267	400	610	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	22	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC-Q1	See 図 6-1	23	40	52	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	3	ns
$t_{sk(pp)}$	Part-to-part skew(2)	ISO722xA-Q1				190	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 図 6-1		2.3		ns
t_f	Output signal fall time		See 図 6-1		2.3		ns
t_{fs}	Failsafe output delay time from input power loss		See 図 6-2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.14 Switching Characteristics

V_{CC1} = V_{CC2} = 5 V ± 10%, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA-Q1	See 図 6-1	252	405	600	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	18	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC-Q1	See 図 6-1	21	32	42	ns
PWD	Pulse-width distortion $\lvert t_{pHL} - t_{pLH} \rvert$ (1)				1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA-Q1				180	ns
		ISO722xC-Q1				10	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A-Q1			3	15	ns
t_r	Output signal rise time		See 図 6-1		2.3		ns
t_f	Output signal fall time		See 図 6-1		2.3		ns
t_{fs}	Failsafe output delay time from input power loss		See 図 6-2		3		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.15 Typical Characteristics

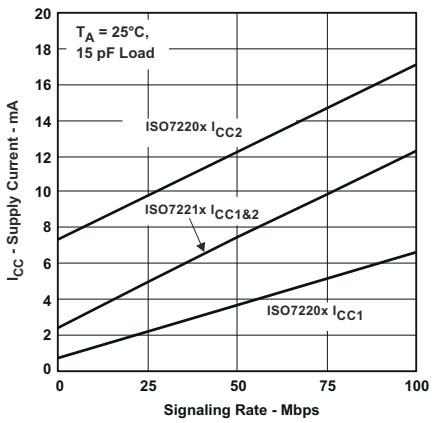


図 5-1. 3.3-V RMS Supply Current vs Signaling Rate (Mbps)

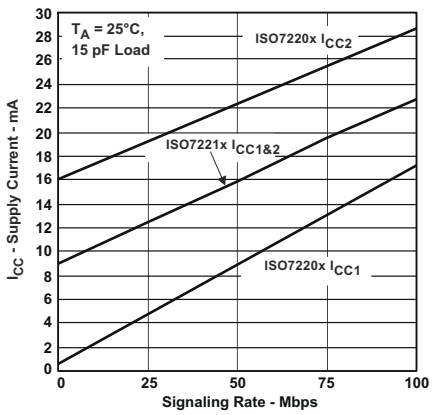


図 5-2. 5-V RMS Suppply Current vs Signaling Rate (Mbps)

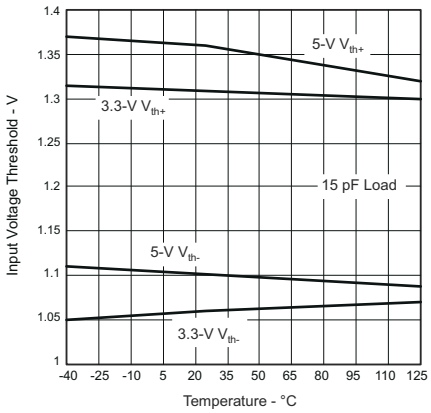


図 5-3. ISO722xA-Q1 and ISO722xC -Q1 Input Voltage Low-to-High Switching Threshold vs Free-Air Temperature

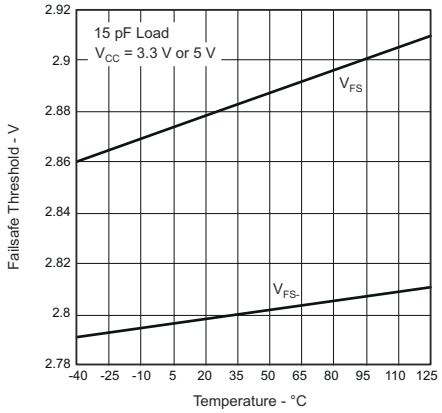


図 5-4. V_{CC} Failsafe Threshold vs Free-Air Temperature

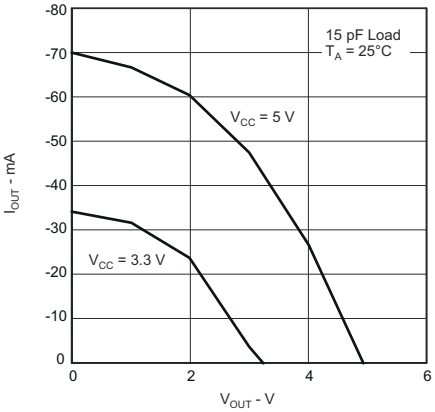


図 5-5. High-Level Output Current vs High-Level Output Voltage

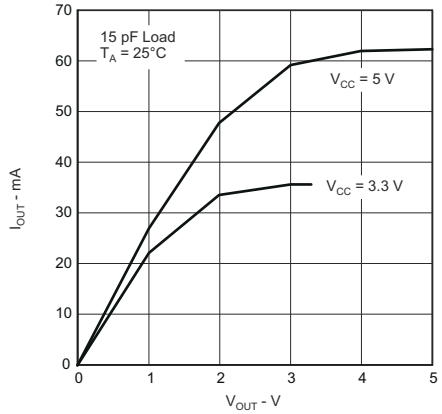
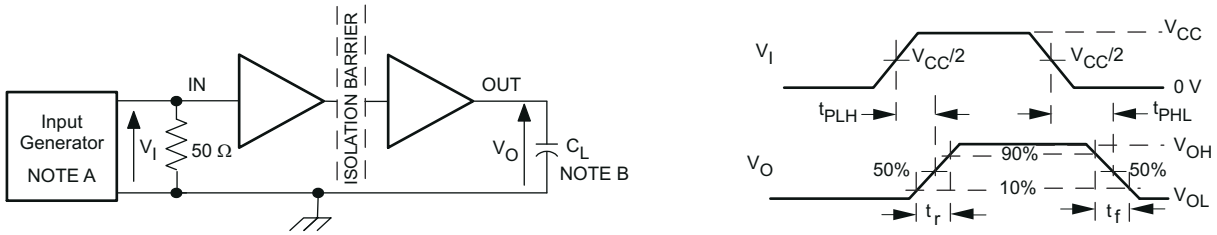


図 5-6. Low-Level Output Current vs Low-Level Output Voltage

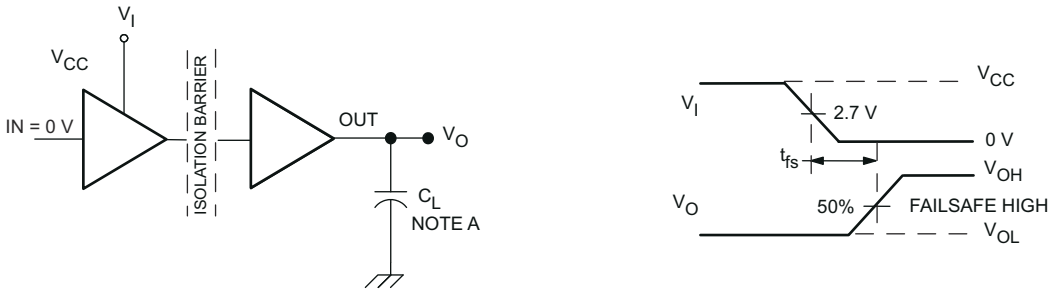
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

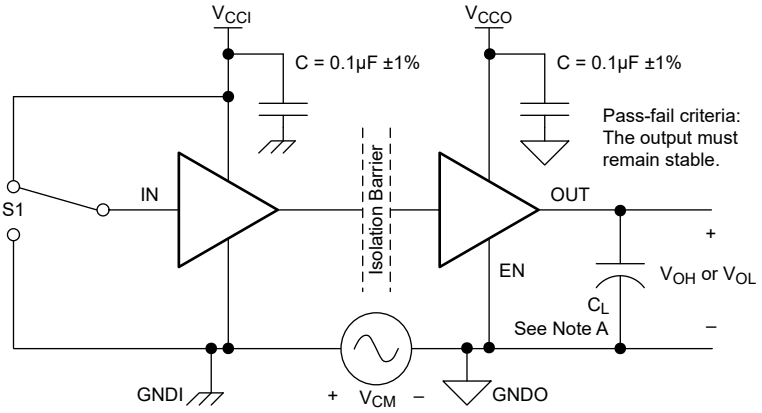
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

図 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



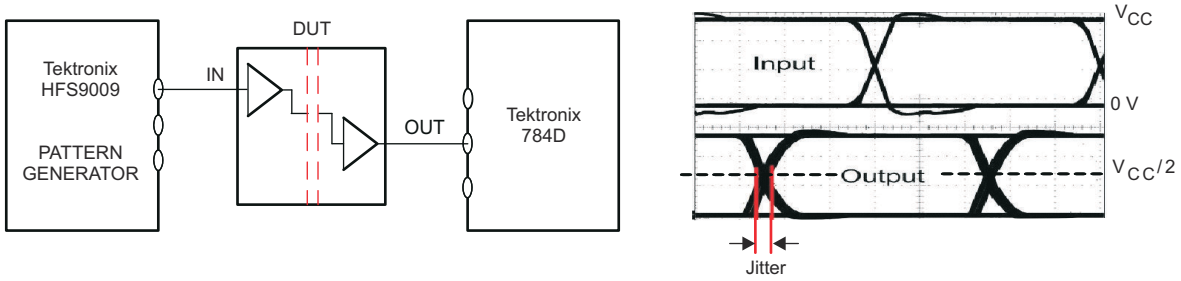
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

図 6-2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

図 6-3. Common-Mode Transient Immunity Test Circuit



PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

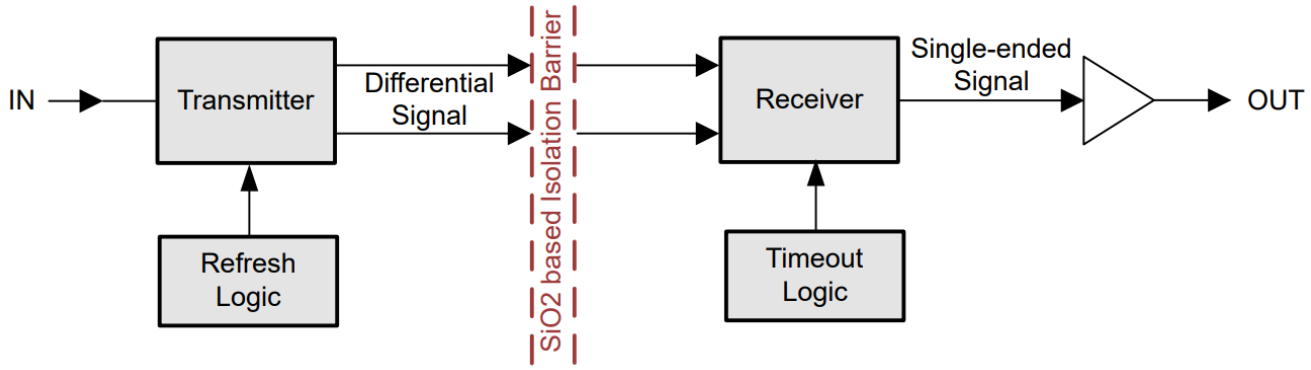
図 6-4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO722xx-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram



7.3 Feature Description

表 7-1 provides an overview of the device features.

表 7-1. Device Features

PART NUMBER	MAXIMUM SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
ISO7220A-Q1	1 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	2/0
ISO7221A-Q1	1 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	1/1
ISO7221C-Q1	25 Mbps	≅ 1.5 V (TTL) (CMOS compatible)	

7.4 Device Functional Modes

The ISO7220x-Q1 and ISO7221x-Q1 family of devices functional modes are listed in 表 7-2.

表 7-2. ISO7220x-Q1 or ISO7221x-Q1 Function Table

INPUT SIDE V_{CC} (1)	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) PU = Powered Up (V_{CC} ≥ 3.0 V), PD = Powered Down (V_{CC} ≤ 2.5 V), X = Irrelevant, H = High Level,
L = Low Level

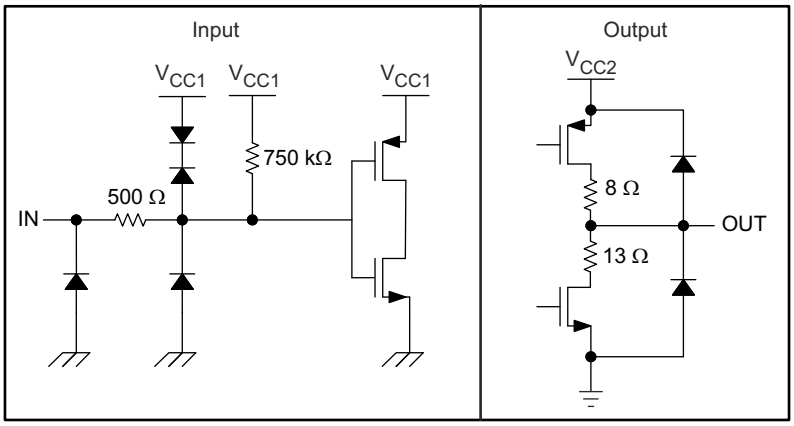


図 7-1. Device I/O Schematics

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO7220x and ISO7221x family devices use single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

The ISO7221x-Q1 family of devices can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

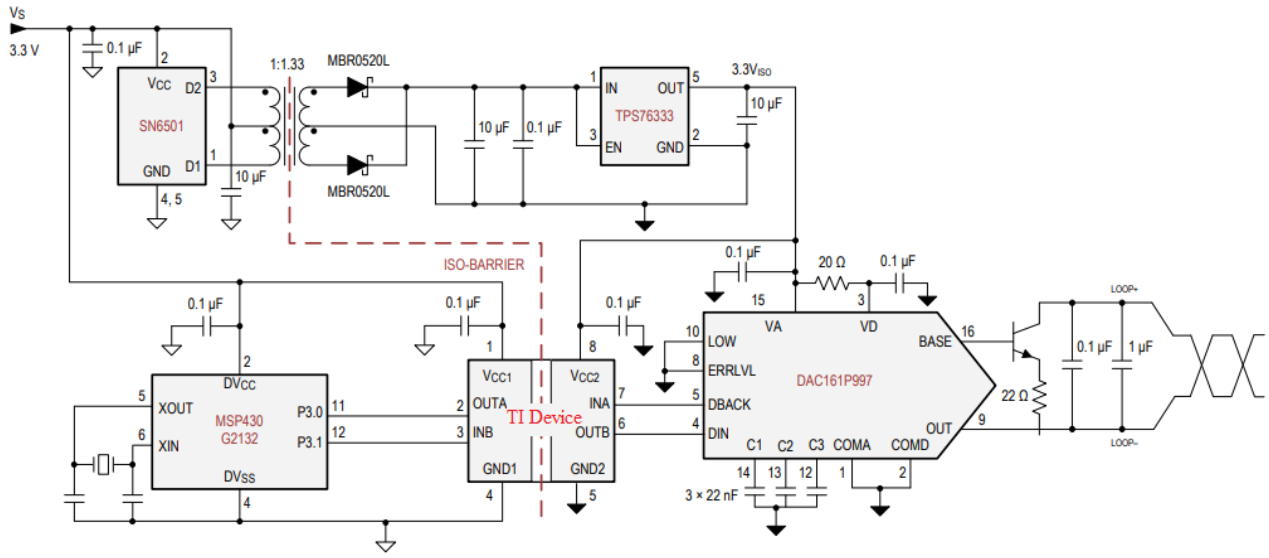


図 8-1. Isolated 4- to 20-mA Current Loop

8.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias (or limit current), the ISO7220x-Q1 and ISO7221x-Q1 devices require only two external bypass capacitors to operate.

8.2.2 Detailed Design Procedure

図 8-2 and 図 8-3 show the hookup of a typical ISO7220x-Q1 and ISO7221x-Q1 circuit. The only external components are two bypass capacitors.

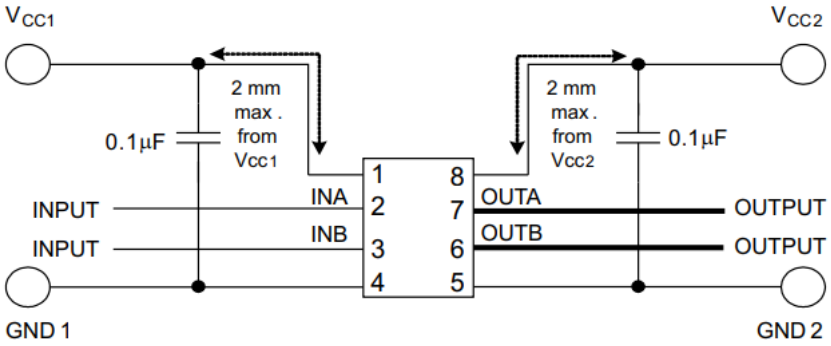


図 8-2. Typical ISO7220x-Q1 Circuit Hook-Up

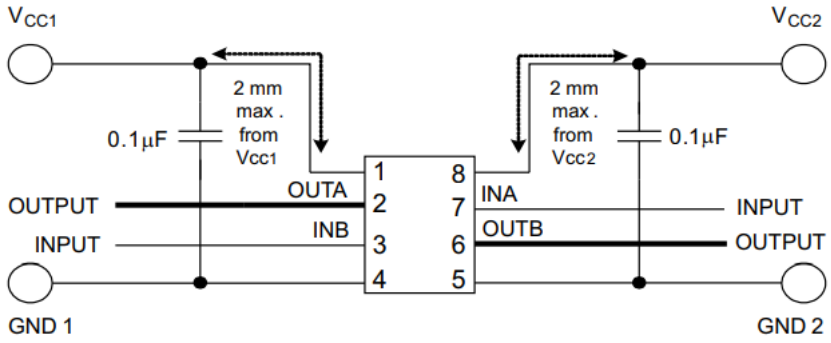


図 8-3. Typical ISO7221x-Q1 Circuit Hook-Up

8.2.3 Insulation Lifetime

At maximum working voltage, the isolation barrier of the ISO72x and ISO72xM family of devices has more than 28 years of life.

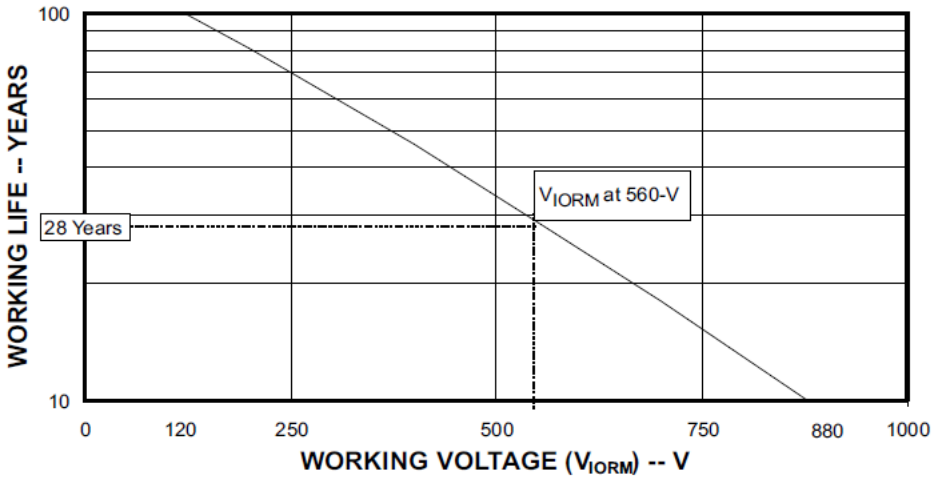


図 8-4. Insulation Lifetime Projection

8.3 Power Supply Recommendations

To help provide reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers are required to accomplish a low EMI PCB design (see 図 8-5). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Route the high-speed traces on the top layer to avoid the use of vias (and the introduction of the inductances) and allow for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Place a solid ground plane next to the high-speed signal layer to establish controlled impedance for transmission line interconnects and provide an excellent low-inductance path for the return current flow.
- Place the power plane next to the ground plane to create additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Route the slower speed control signals on the bottom layer to allow for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. Adding a second plane system to the stack makes the stack mechanically stable and prevents warping. The power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

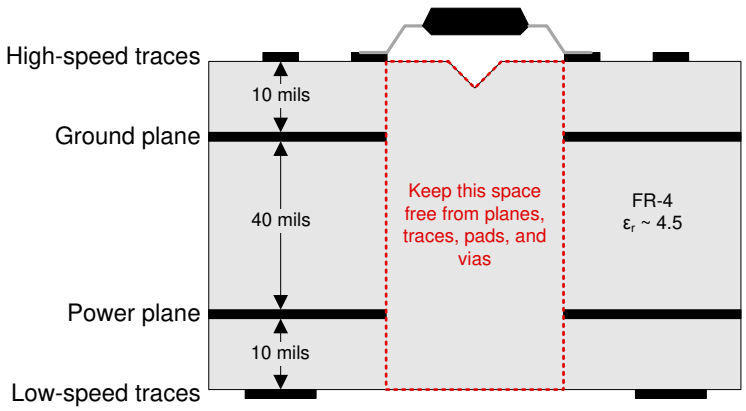


図 8-5. Recommended Layer Stack

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support, refer to:

- AC-mains LED Lighting with DALI DMX512 & Power Line Communications Reference Design
- Industrial Servo Drive and AC Inverter Drive Reference Design
- Low-Cost Single/Dual-Phase Isolated Electricity Measurement Reference Design
- Noise Tolerant Capacitive Touch HMI Reference Design
- Type 2 PoE PSE, 6kV Lightning Surge Reference Design

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops* data sheet
- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* application report
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *MSP430G2x32 Mixed Signal Microcontroller* data sheet
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *TPS763xx Low-Power 150-mA Low-Dropout Linear Regulators* data sheet

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.5 Trademarks

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9.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (April 2020) to Revision E (November 2024) **Page**

- デバイスの商用バージョンと整合するように、ドキュメント全体の内容を更新 1
- ドキュメント全体を通して容量性絶縁から絶縁バリアに参照を更新 1
- ドキュメント全体で VDE V 0884-11 を DIN VDE 0884-17 に更新 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations 4
- Updated electrical and switching characteristics to match device performance 6
- Added the *Detailed Description*, *Overview*, *Feature Description*, *Functional Block Diagram*, and *Device Functional Modes* sections 16
- Added the *Typical Application*, *Power Supply Recommendations*, and *Layout* sections 18

Changes from Revision C (May 2012) to Revision D (April 2020) **Page**

- 規格名称を以下のように変更:「IEC 60747-5-2 (VDE 0884, Rev 2)、IEC 61010-1」から「DIN VDE V 0884-11:2017-01、DIN EN 61010-1」に変更、「特長」に「IEC 62368-1」を追加 1
- ドキュメント全体を通して編集上および体裁上の変更を実施 1
- Deleted typical values (TYP) for 'Input pulse width' and 'Signaling rate' specifications in **Recommended Operating Conditions** table 4
- Added 'Ambient temperature' specification in **Recommended Operating Conditions** table 4
- Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 605 ns in **Switching Characteristics** at V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10% 9
- Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 18 ns To: 22 ns in **Switching Characteristics** at V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10% 9
- Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in **Switching Characteristics** at V_{CC1} = 3.3 V ± 10%, V_{CC2} = 5 V ± 10% 9
- Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 585 ns in **Switching Characteristics** at V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10% 11
- Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in **Switching Characteristics** at V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10% 11
- Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 14 ns To: 18 ns in **Switching Characteristics** at V_{CC1} = 5 V ± 10%, V_{CC2} = 3.3 V ± 10% 11
- Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 485 ns To: 610 ns in **Switching Characteristics** at V_{CC1} = V_{CC2} = 3.3 V ± 10% 11
- Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in **Switching Characteristics** at V_{CC1} = V_{CC2} = 3.3 V ± 10% 11
- Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 18 ns To: 22 ns in **Switching Characteristics** at V_{CC1} = V_{CC2} = 3.3 V ± 10% 11
- Changed 'ISO722xA' to 'ISO7220A' and deleted 'ISO722xC' row from 'Channel-to-channel output skew' specification in **Switching Characteristics** at V_{CC1} = V_{CC2} = 5 V ± 10% 12
- Changed 'Pulse-width distortion' maximum (MAX) limit for ISO722xA From: 14 ns To: 18 ns in **Switching Characteristics** at V_{CC1} = V_{CC2} = 5 V ± 10% 12
- Changed 'Propagation delay' maximum (MAX) limit for ISO722xA From: 480 ns To: 600 ns in **Switching Characteristics** at V_{CC1} = V_{CC2} = 5 V ± 10% 12

11 Mechanical, Packaging, and Orderable Information

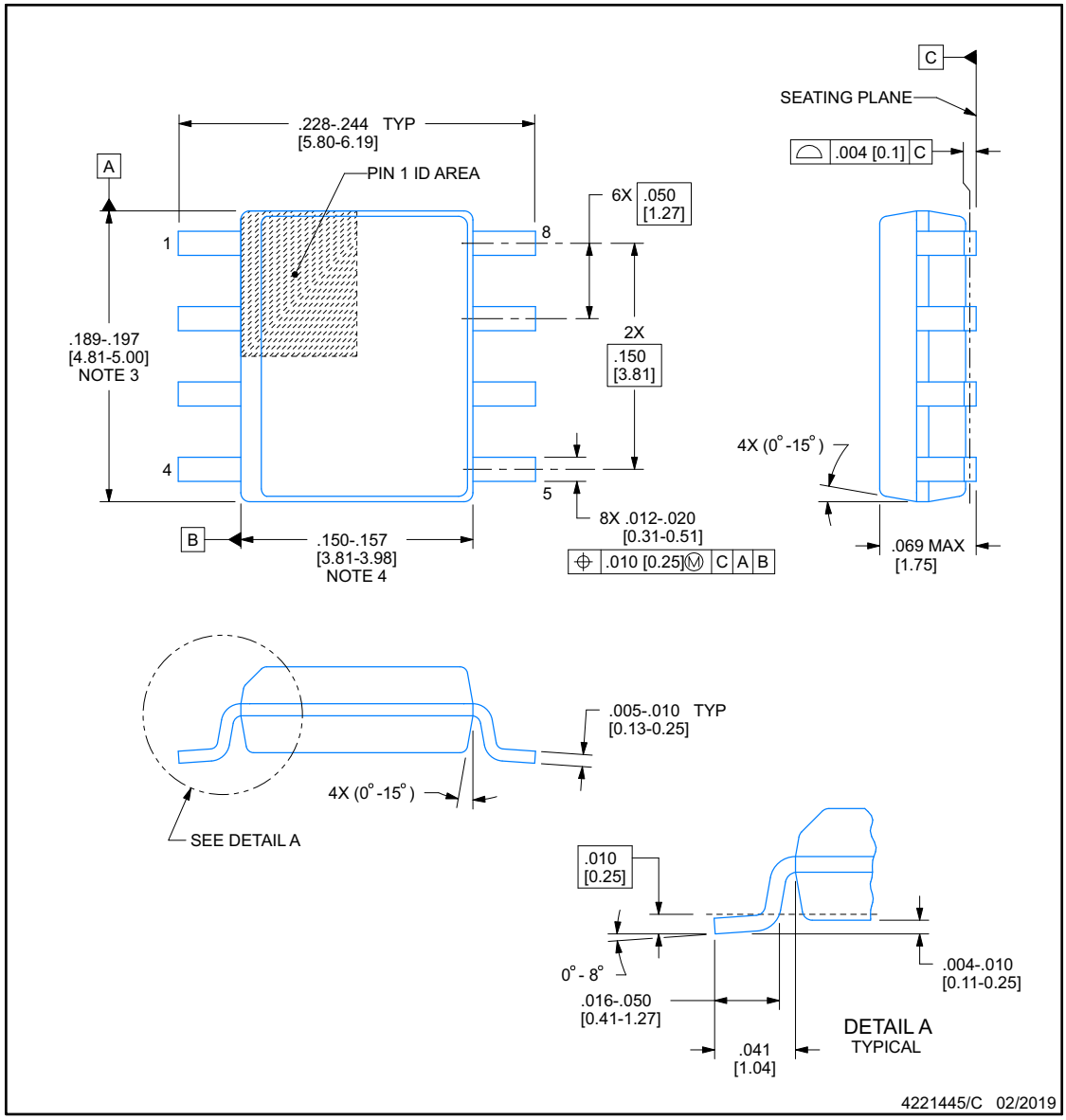
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

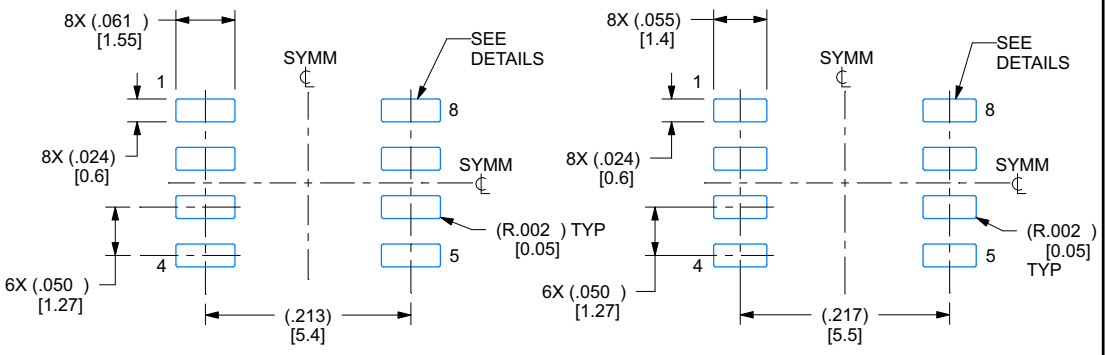
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

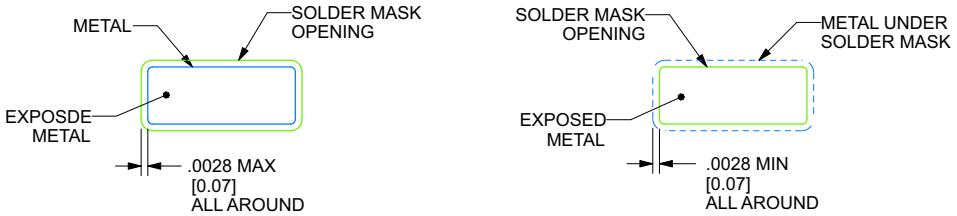
SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

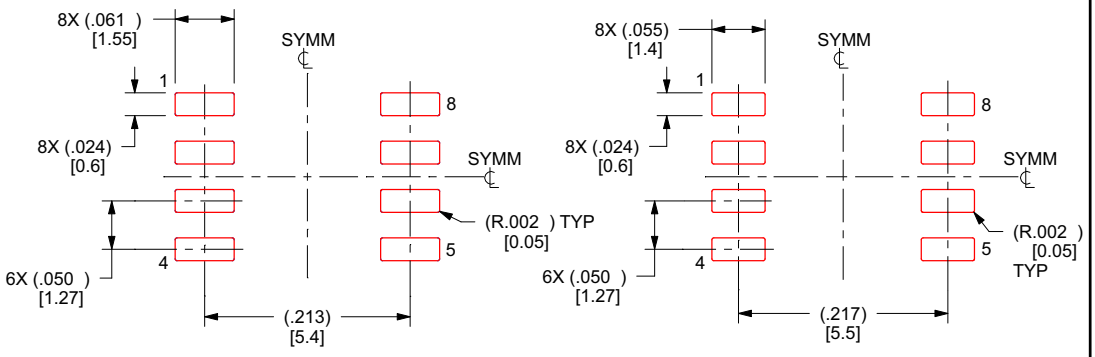
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7220AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7220AQ	Samples
ISO7221AQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221AQ	Samples
ISO7221CQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7221CQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1 :

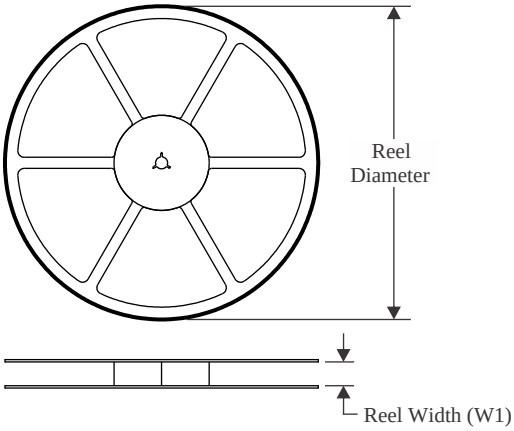
- Catalog : ISO7220A, ISO7221A, ISO7221C

NOTE: Qualified Version Definitions:

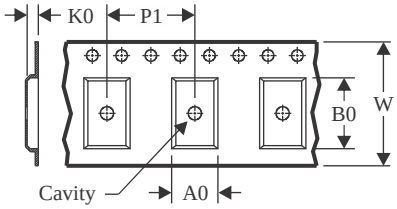
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

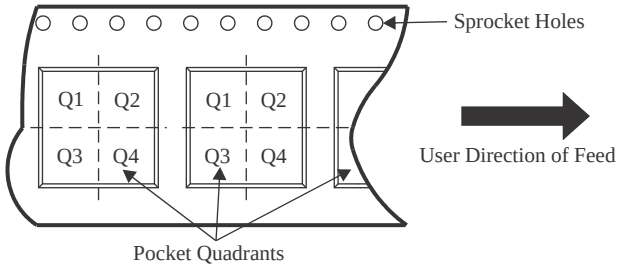


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

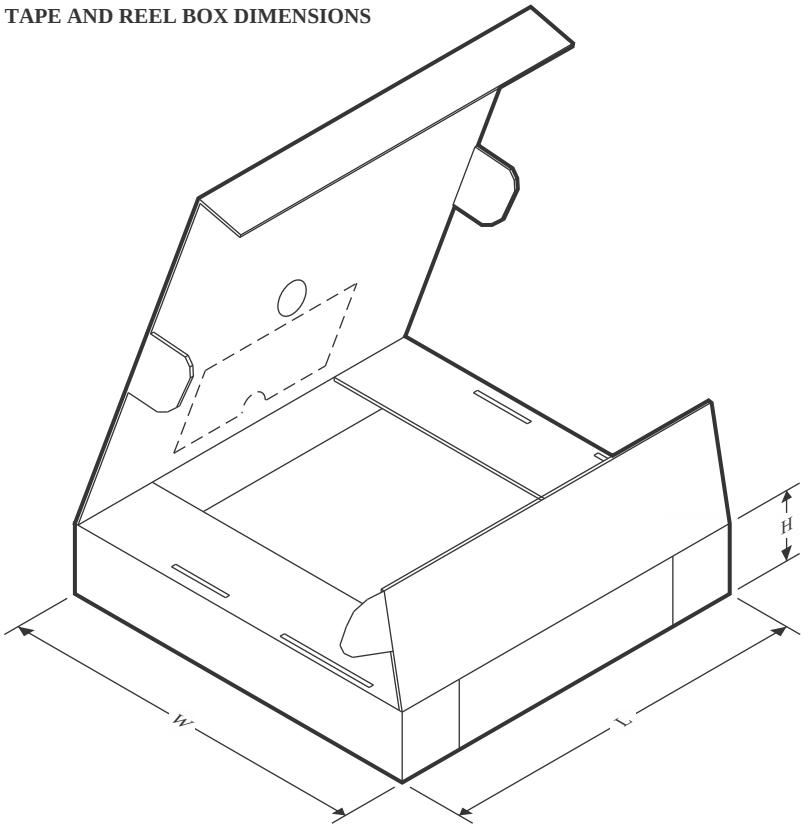
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

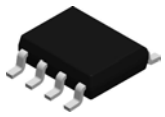
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221CQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

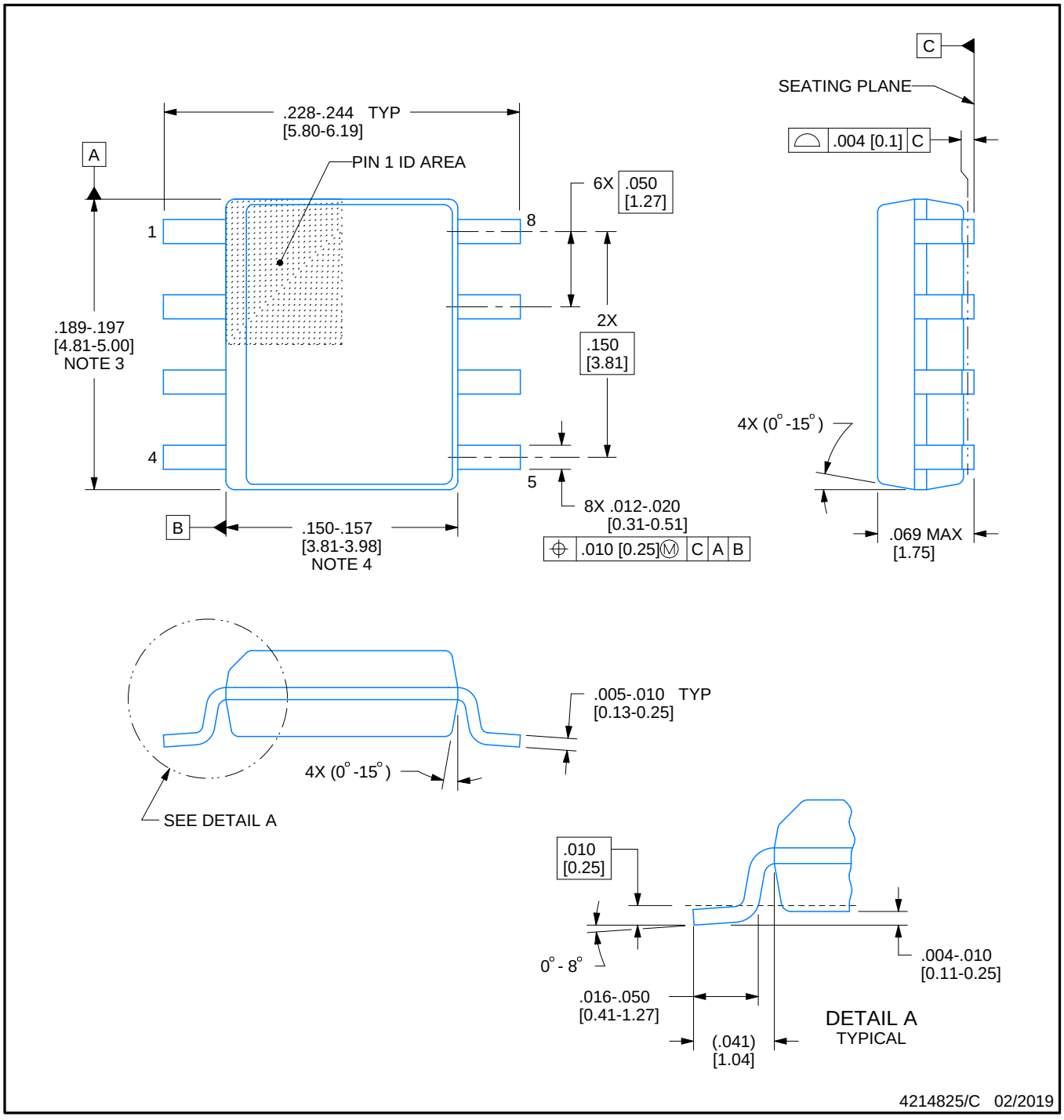


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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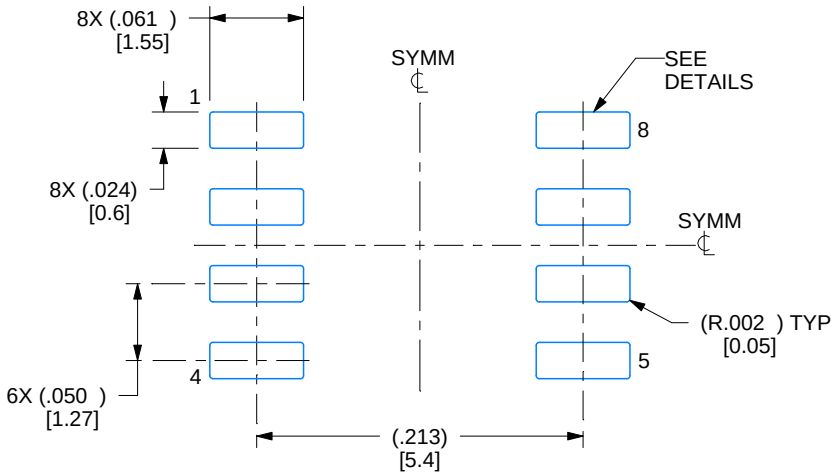
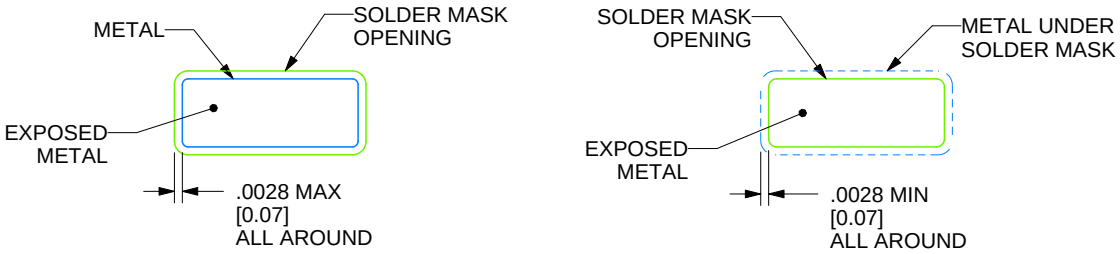
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

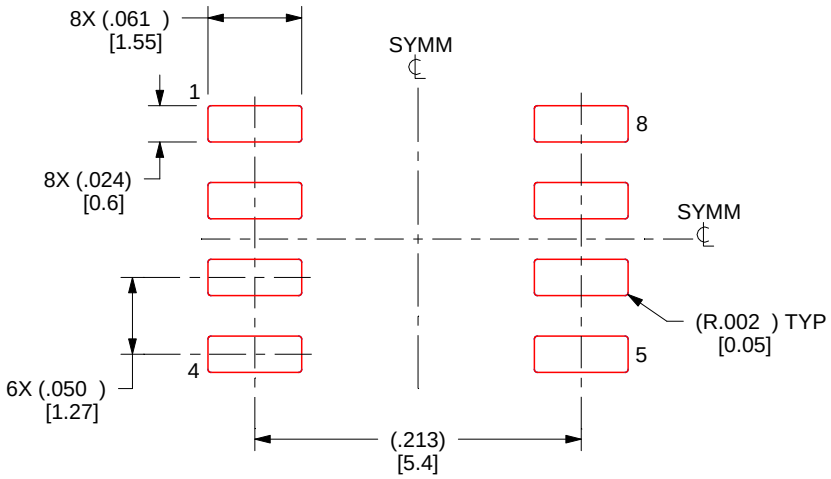
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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