ISO773x-Q1 高速、堅牢な EMC 強化型 3 チャネル・デジタル・アイソレータ

1 特長

- 車載アプリケーション認定済み
- 下記の内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:–40℃～+125℃の動作時周囲温度
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能:ISO7730-Q1、ISO7731-Q1
- 100Mbps のデータ レート
- 堅牢な絶縁バリア:
  - 1500V_{RMS} の動作電圧で 30 年を超える予測寿命
  - 最高 5000V_{RMS} の絶縁定格
  - 最高 12.8kV のサージ耐量
  - CMTI: ±100kV/µs (代表値)
- 幅広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧レベル変換
- デフォルト出力が HIGH (ISO773x) と LOW (ISO773xF) のオプション
- 低い消費電力:1Mbps でチャネルごとに標準値 1.5mA
- 小さい伝搬遅延:標準値 11ns (5V 電源)
- 堅牢な電磁両立性 (EMC)
  - システム レベルでの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 低い放射
- Wide-SOIC (DW-16) および QSOP (DBQ-16) のパッケージ オプション
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1、IEC 62368-1、IEC 60601-1、GB 4943.1 認証

2 アプリケーション

- ハイブリッド、電気自動車、およびパワートレイン システム (EV/HEV)
  - バッテリ管理システム (BMS)
  - オンボード チャージャ
  - トラクション インバータ
  - DC/DC コンバータ
  - インバータおよびモータ制御
- ボディ エレクトロニクス
  - 車載パーキング ヒーター モジュール
  - HVAC (エアコン) コンプレッサ モジュール
  - HVAC (エアコン) 制御モジュール
  - HVAC (エアコン) センサ
  - 車内ヒーター モジュール

パッケージ情報

部品番号 (1)	パッケージ	パッケージ サイズ(2)
ISO7730-Q1 ISO7731-Q1	DW (SOIC、16)	10.30mm × 7.50mm
	DBQ (SSOP、16)	4.90mm × 3.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

3 概要

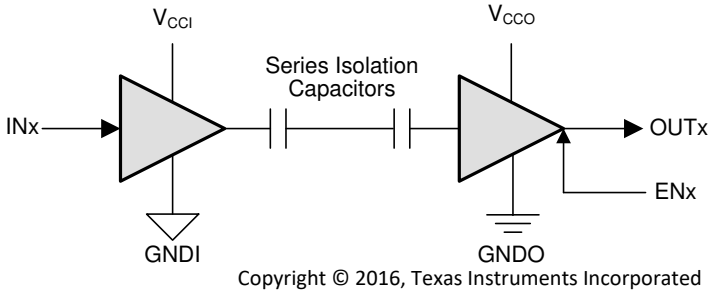
ISO773x-Q1 デバイスは、高性能の 3 チャネル デジタル アイソレータであり、UL 1577 準拠で 5000V_{RMS} (DW パッケージ) および 3000V_{RMS} (DBQ パッケージ) の絶縁定格を備えています。

このファミリのデバイスは、VDE、CSA、TUV、CQC に従って絶縁定格が強化されています。

ISO773x-Q1 ファミリのデバイスは電磁気耐性が高く、放射が低く、低消費電力を実現し、CMOS または LVCMOS デジタル I/O を絶縁します。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) 絶縁バリアによって分離されています。このデバイスは複数のイネーブル ピンを備えています。これらのイネーブル ピンを使うと、マルチコントローラ駆動アプリケーションにおいて、各出力を高インピーダンス状態にすることで、消費電力を低減できます。

ISO7730-Q1 デバイスには 3 つのチャネルがあり、すべて同じ方向です。ISO7731-Q1 デバイスには 2 つの順方向チャネルと、1 つの逆方向チャネルがあります。入力電力または入力信号が失われた場合のデフォルト出力は、接尾辞 F のないデバイスでは High、接尾辞 F のあるデバイスでは Low になります。詳細は「デバイスの機能モード」のセクションを参照してください。

絶縁電源と組み合わせて使用することで、このデバイス ファミリは、データ バス (たとえば CAN、LIN など) または他の回路からのノイズ電流がローカル グランドに入り込み、敏感な回路に干渉や損傷を引き起こすことを防ぐのに役立ちます。革新的なチップ設計およびレイアウト技法により、ISO773x-Q1 デバイスは電磁気互換性が大幅に強化されているため、システム レベルの ESD、EFT、サージ、および放射のコンプライアンスを容易に達成できます。ISO773x-Q1 ファミリのデバイスは、16 ピンの Wide-SOIC および QSOP パッケージで供給されます。



V_{CCI}=入力電源、V_{CCO}=出力電源
GNDI=入力グランド、GNDO=出力グランド

概略回路図

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4 Pin Configuration and Functions

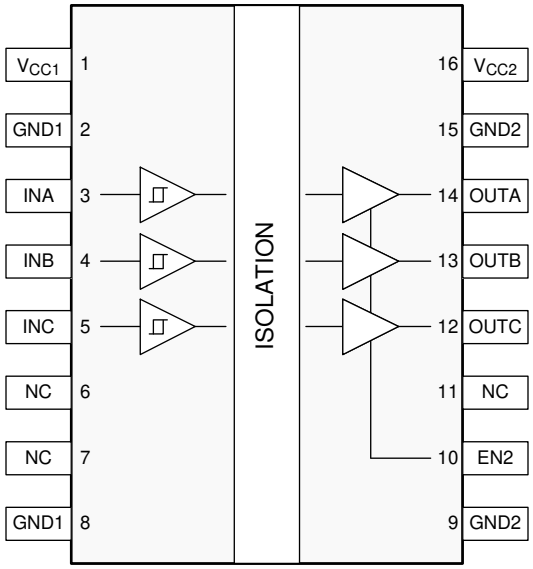


図 4-1. ISO7730-Q1 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

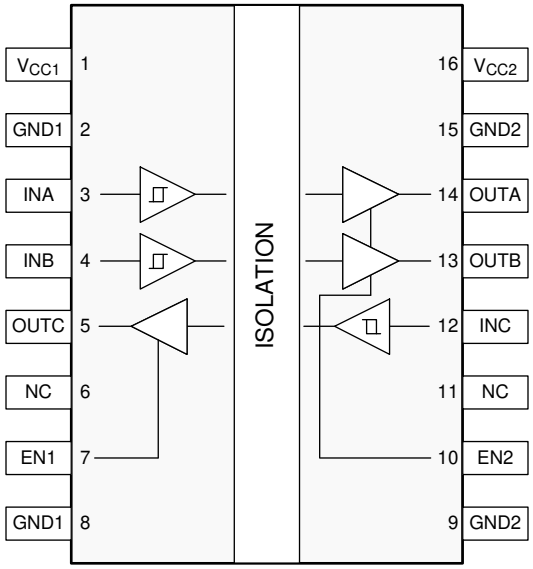


図 4-2. ISO7731-Q1 DW and DBQ Packages 16-Pin SOIC-WB and QSOP Top View

表 4-1. Pin Functions

PIN			Type[1]	DESCRIPTION
NAME	NO.			
	ISO7730-Q1	ISO7731-Q1		
EN1	—	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	—	Ground connection for V_{CC2}
INA	3	3	I	Input, channel A

表 4-1. Pin Functions (続き)

PIN			Type[1]	DESCRIPTION
NAME	NO.			
	ISO7730-Q1	ISO7731-Q1		
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	—	Not connected
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	—	Power supply, V_{CC2}

5 Specifications

5.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage (2)	-0.5	6	V
V	Voltage at INx, OUTx, ENx	-0.5	V_{CCX} + 0.5 (3)	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(2) (3)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High level output current	V_{CCO} (1) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			
		V_{CCO} = 2.5 V	-1			
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 x V_{CCI} (1)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 x V_{CCI}	V
DR (2)	Data rate		0		100	Mbps
T_A	Ambient temperature		-55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

5.4 Thermal Information

THERMAL METRIC(1)		ISO773x		UNIT
		DW (SOIC)	DBQ (QSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.4	109	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.9	46.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	60.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.1	35.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.5	60	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7730-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 50-MHz 50% duty cycle square wave			160	mW
P_{D1}	Maximum power dissipation (side-1)				30	mW
P_{D2}	Maximum power dissipation (side-2)				130	mW
ISO7731-Q1						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 50-MHz 50% duty cycle square wave			160	mW
P_{D1}	Maximum power dissipation (side-1)				60	mW
P_{D2}	Maximum power dissipation (side-2)				100	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS		VALUE		UNIT
				DW-16	DBQ-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air		>8	>3.7	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface		>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)		>17	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112, UL 746A		>600	>600	V
	Material group	According to IEC 60664-1		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}		I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}		I-IV	I-III	
		Rated mains voltage ≤ 600 V_{RMS}		I-IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}		I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17) (2)						
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	ISO773x	2121	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See セクション 8.2.3.1	ISO773x	1500	400	V_{RMS}
V_{IOWM}	Maximum working isolation voltage	DC voltage	ISO773x	2121	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t= 1 s (100% production)		8000	4242	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	ISO773x	8000	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	V_{IOSM} ≥ 1.3 x V_{IMP}; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	ISO773x	12800	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 x V_{IORM}, t_m = 10 s		≤5	≤5	pC
q_{pd}	Apparent charge(5)	Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s;	$V_{pd(m)}$ = 1.6 x V_{IORM}, t_m = 10 s (ISO773x)	≤5	≤5	pC
q_{pd}	Apparent charge(5)	Method b; At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM} (ISO773x) , t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)		≤5	≤5	pC
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz		≅0.7	≅0.7	pF
R_{IO}	Isolation resistance(6)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C		$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C		$>10^{9}$	$>10^{9}$	
	Pollution degree			2	2	
	Climatic category			55/125/21	55/125/21	
UL 1577						
V_{ISO}	Maximum withstanding isolation voltage	V_{TEST} = V_{ISO} , t = 60 s (qualification), V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)		5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in

certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package

(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 8000 V_{PK} (DW-16) and 4242 V_{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16, Reinforced), 1414 V_{PK} (DW-16, Basic) and 566 V_{PK} (DBQ-16); Maximum surge isolation voltage, 12800 V_{PK} (DW-16, Reinforced), 7800 V_{PK} (DW-16, Basic) and 10000 V_{PK} (DBQ-16)	Reinforced insulation per CSA 62368-1 and IEC 62368-1, 600 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V_{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V_{RMS}; DBQ-16: Single protection, 3000 V_{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage	5000 V_{RMS} (DW-16) and 3000 V_{RMS} (DBQ-16) Reinforced insulation per EN 61010-1 up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (DBQ-16) 5000 V_{RMS} (DW-16) and 3000 V_{RMS} (DBQ-16) Reinforced insulation per EN 62368-1 up to working voltage of 600 V_{RMS} (DW -16) and 370 V_{RMS} (DBQ-16) of 600 V_{RMS}
Certificate numbers: 40040142 (Reinforced) 40047657 (Basic)	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC18001199097 (DBQ-16)	Client ID number: 077311

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current.	$R_{\theta JA}$ = 81.4°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 5-3			279	mA
		$R_{\theta JA}$ = 81.4°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 5-3			427	
		$R_{\theta JA}$ = 81.4°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 5-3			558	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 81.4°C/W, T_J = 150°C, T_A = 25°C, see 図 5-3			1536	mW
T_S	Maximum safety temperature				150	°C
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 109.0°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 5-4			209	mA
		$R_{\theta JA}$ = 109.0°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 5-4			319	
		$R_{\theta JA}$ = 109.0°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see 図 5-4			417	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 109.0°C/W, T_J = 150°C, T_A = 25°C, see 図 5-4			1147	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

5.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See 図 6-1	V_{CCO} - 0.4 (1)	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See 図 6-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			28	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-28			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; See 図 6-4	85	100		kV/µs
C_I	Input capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

5.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.3	mA
			I_{CC2}		0.3	0.8	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		0.3	0.8	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.3	mA
			I_{CC2}		1.6	3.7	mA
	EN2 = V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	6	mA
			I_{CC2}		1.8	3.9	mA
Supply current - AC signal	EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	4.1	mA
			I_{CC2}		1.9	4	mA
		10 Mbps	I_{CC1}		2.7	4.3	mA
			I_{CC2}		3.3	5.7	mA
		100 Mbps	I_{CC1}		3.6	5.6	mA
			I_{CC2}		17.5	23.2	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI} (1)(ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	2.2	mA
			I_{CC2}		0.7	1.6	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.6	mA
			I_{CC2}		1.8	2.8	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (1)(ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		1.3	2.9	mA
			I_{CC2}		1.6	3.7	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = VCC_I (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5.4	mA
			I_{CC2}		2.8	5.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.7	4.2	mA
			I_{CC2}		2.3	4.6	mA
		10 Mbps	I_{CC1}		3	4.9	mA
			I_{CC2}		3.3	5.8	mA
		100 Mbps	I_{CC1}		8.5	11.5	mA
			I_{CC2}		13.1	17.8	mA

(1) V_{CCI} = Input-side V_{CC}

5.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2mA; See 図 6-1	V_{CCO} - 0.3 (1)	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; See 図 6-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			30	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-30			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; See 図 6-4	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

5.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.3	mA
			I_{CC2}		0.3	0.8	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	5.9	mA
			I_{CC2}		0.3	0.7	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.3	mA
			I_{CC2}		1.6	3.6	mA
	EN2 =V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	5.8	mA
			I_{CC2}		1.8	3.8	mA
Supply current - AC signal	EN2 = $V_{CCI;}$ All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	4.1	mA
			I_{CC2}		1.8	3.9	mA
		10 Mbps	I_{CC1}		2.7	4.1	mA
			I_{CC2}		2.8	5.1	mA
		100 Mbps	I_{CC1}		3.3	4.9	mA
			I_{CC2}		13	17.7	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI} (1)(ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	2.1	mA
			I_{CC2}		0.7	1.5	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.5	mA
			I_{CC2}		1.8	2.8	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731-Q1); V_I = 0 V (ISO7731-Q1with F suffix)		I_{CC1}		1.3	2.8	mA
			I_{CC2}		1.6	3.7	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5.3	mA
			I_{CC2}		2.8	5	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	4.1	mA
			I_{CC2}		2.2	4.5	mA
		10 Mbps	I_{CC1}		2.8	4.6	mA
			I_{CC2}		2.9	5.3	mA
		100 Mbps	I_{CC1}		6.7	9.2	mA
			I_{CC2}		10	14	mA

(1) V_{CCI} = Input-side V_{CC}

5.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA; See 図 6-1	V_{CCO} - 0.2 (1)	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; See 図 6-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			0.6 x V_{CCI}	0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			30	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-30			µA
CMTI	Common mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; See 図 6-4	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

5.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7730-Q1							
Supply current - disable	EN2 = 0 V; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.2	mA
			I_{CC2}		0.3	0.7	mA
	EN2 = 0 V; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	5.8	mA
			I_{CC2}		0.3	0.7	mA
Supply current - DC signal	EN2 = V_{CC2}; V_I = V_{CC1} (ISO7730-Q1); V_I = 0 V (ISO7730-Q1 with F suffix)		I_{CC1}		1	2.2	mA
			I_{CC2}		1.6	3.6	mA
	EN2 =V_{CC2}; V_I = 0 V (ISO7730-Q1); V_I = V_{CC1} (ISO7730-Q1 with F suffix)		I_{CC1}		4.3	5.8	mA
			I_{CC2}		1.8	3.8	mA
Supply current - AC signal	EN2 = V_{CCI};All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.6	4	mA
			I_{CC2}		1.8	3.8	mA
		10 Mbps	I_{CC1}		2.6	4.1	mA
			I_{CC2}		2.5	4.8	mA
		100 Mbps	I_{CC1}		3.1	4.7	mA
			I_{CC2}		10.2	14.3	mA
ISO7731-Q1							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI} (1)(ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		0.8	2.1	mA
			I_{CC2}		0.7	1.5	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3	4.5	mA
			I_{CC2}		1.8	2.7	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731-Q1); V_I = 0 V (ISO7731-Q1 with F suffix)		I_{CC1}		1.3	2.8	mA
			I_{CC2}		1.6	3.7	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731-Q1); V_I = V_{CCI} (ISO7731-Q1 with F suffix)		I_{CC1}		3.5	5.3	mA
			I_{CC2}		2.8	5	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	4.1	mA
			I_{CC2}		2.2	4.4	mA
		10 Mbps	I_{CC1}		2.7	4.4	mA
			I_{CC2}		2.7	5.1	mA
		100 Mbps	I_{CC1}		5.6	8	mA
			I_{CC2}		8	11.6	mA

(1) V_{CCI} = Input-side V_{CC}

5.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	11	17	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See 図 6-1		0.6	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 図 6-1		1.3	3.9	ns
t_f	Output signal fall time	See 図 6-1		1.4	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		8	22	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output	See 図 6-2		8	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x	See 図 6-2		7	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix	See 図 6-2		3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x	See 図 6-2		3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix	See 図 6-2		7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	11	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5	ns
t_r	Output signal rise time	See 図 6-1		1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		17	31	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix			3.2	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x			3.2	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	7.5	12	21	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				5.3	ns
t_r	Output signal rise time	See 図 6-1		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		22	41	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO773x			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO773x with F suffix			3.3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO773x			3.3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO773x with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.7V. See 図 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Insulation Characteristics Curves

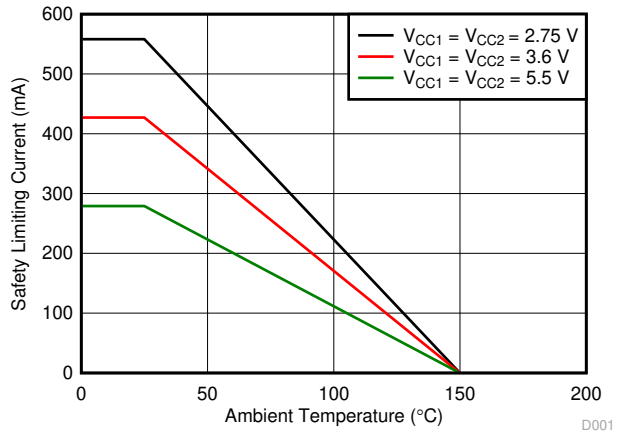


図 5-1. Thermal Derating Curve for Safety Limiting Current per VDE for DW-16 Package

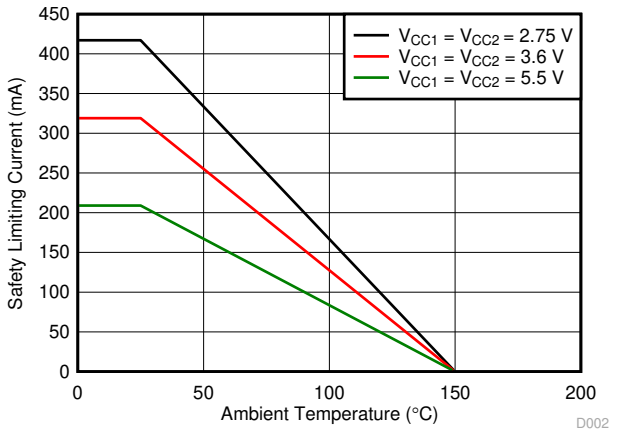


図 5-2. Thermal Derating Curve for Safety Limiting Current per VDE for DBQ-16 Package

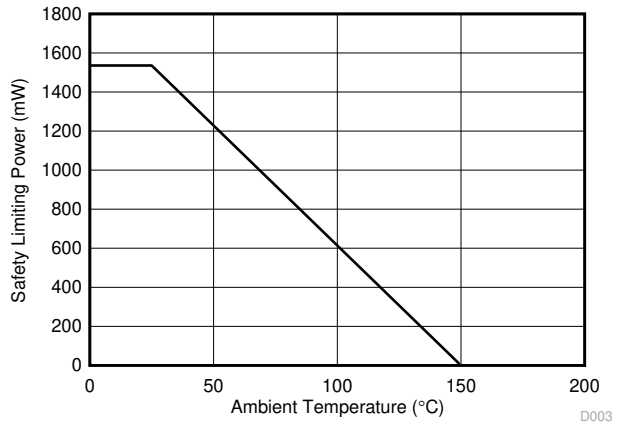


図 5-3. Thermal Derating Curve for Safety Limiting Power per VDE for DW-16 Package

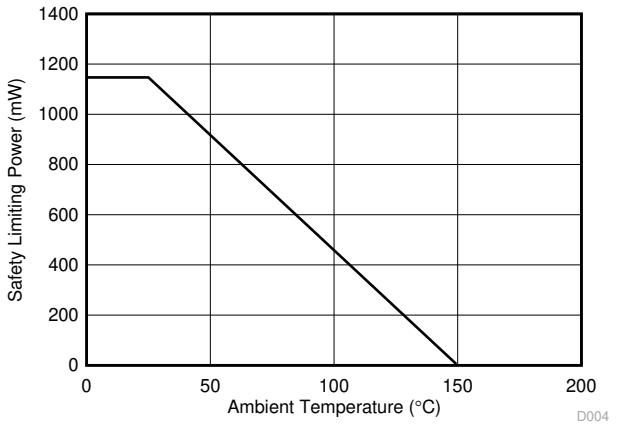
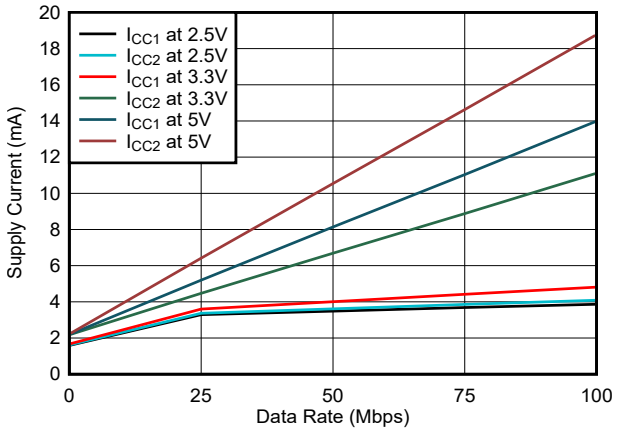


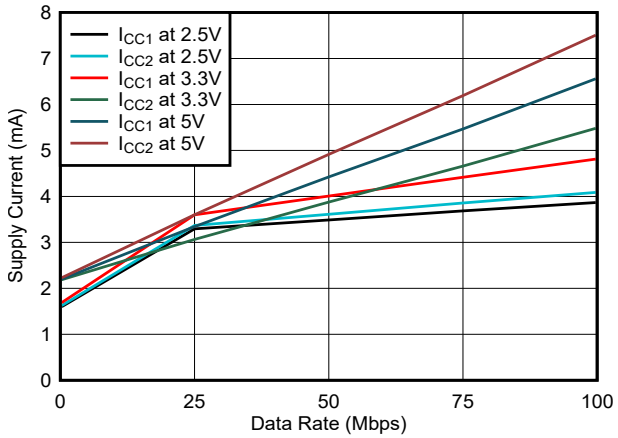
図 5-4. Thermal Derating Curve for Safety Limiting Power per VDE for DBQ-16 Package

5.19 Typical Characteristics



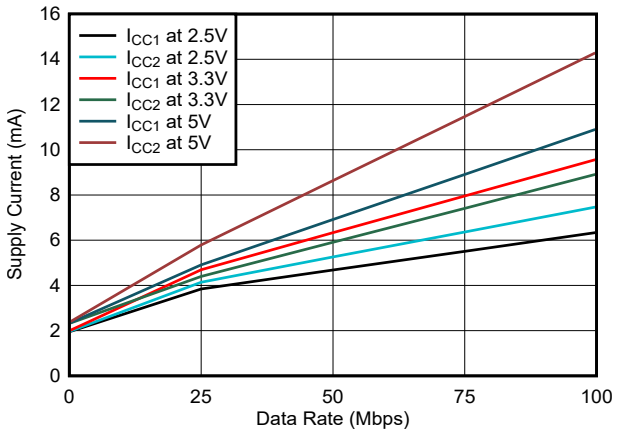
T_A = 25°C C_L = 15 pF

図 5-5. ISO7730-Q1 Supply Current vs Data Rate (With 15-pF Load)



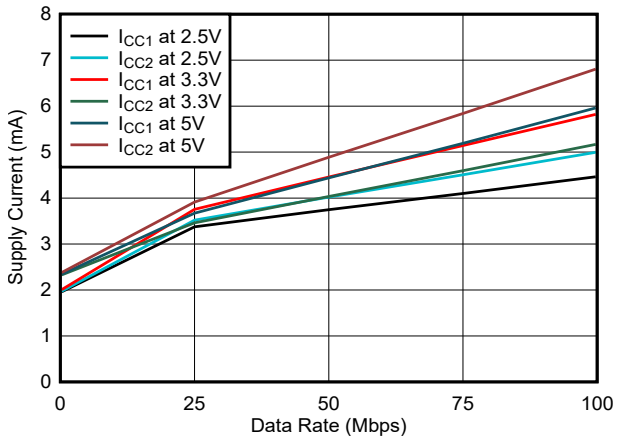
T_A = 25°C C_L = No Load

図 5-6. ISO7730-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C C_L = 15 pF

図 5-7. ISO7731-Q1 Supply Current vs Data Rate (With 15-pF Load)



A. T_A = 25°C C_L = No Load

図 5-8. ISO7731-Q1 Supply Current vs Data Rate (With No Load)

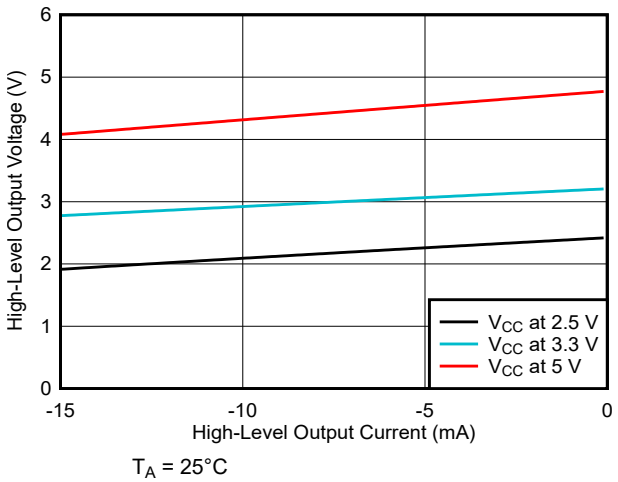


図 5-9. High-Level Output Voltage vs High-level Output Current

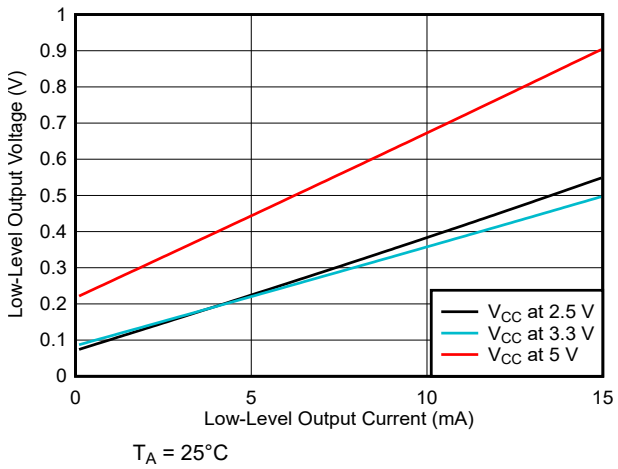


図 5-10. Low-Level Output Voltage vs Low-Level Output Current

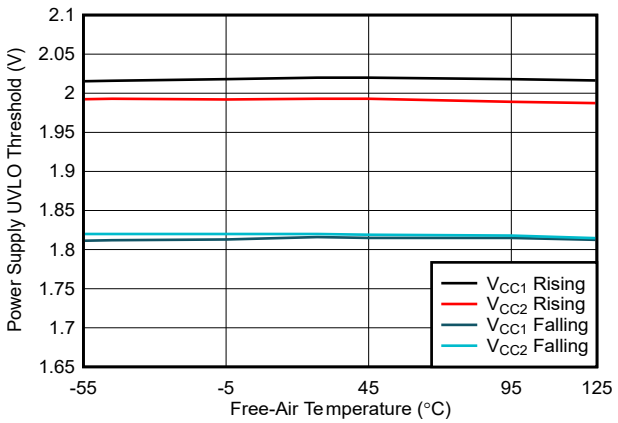


図 5-11. Power Supply Undervoltage Threshold vs Free-Air Temperature

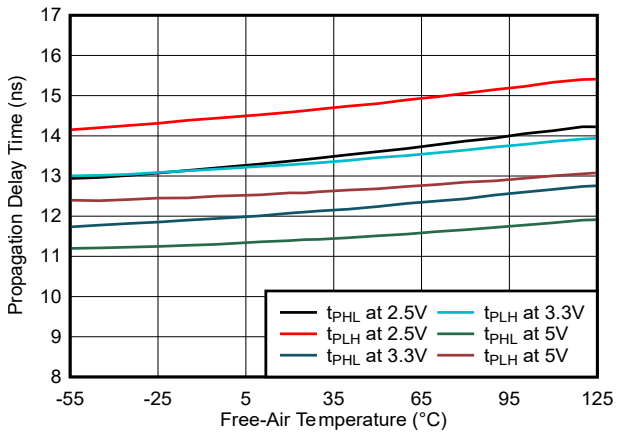
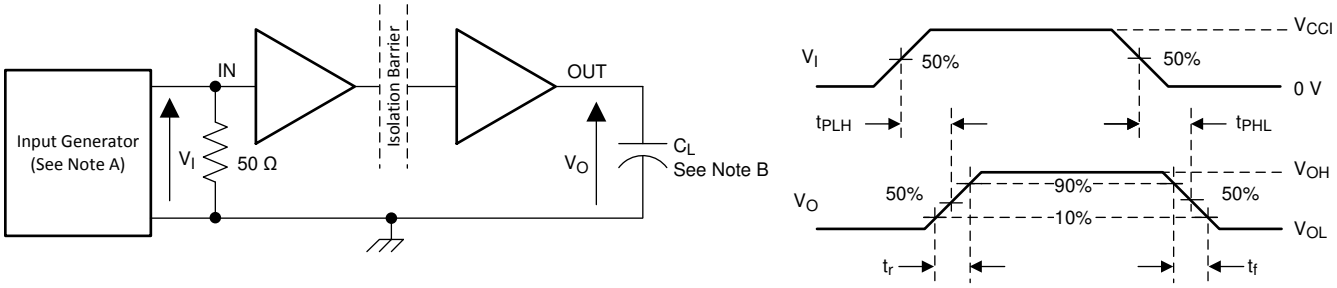


図 5-12. Propagation Delay Time vs Free-Air Temperature

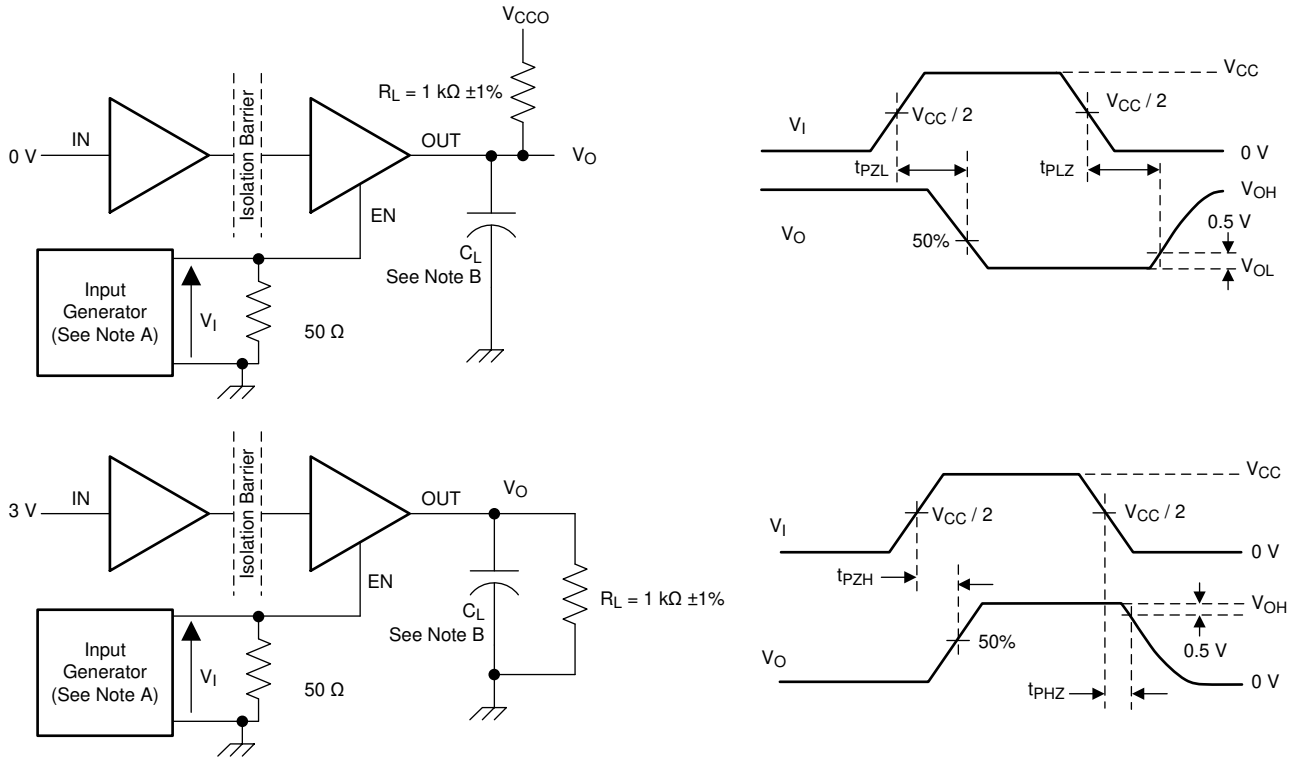
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω resistor is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

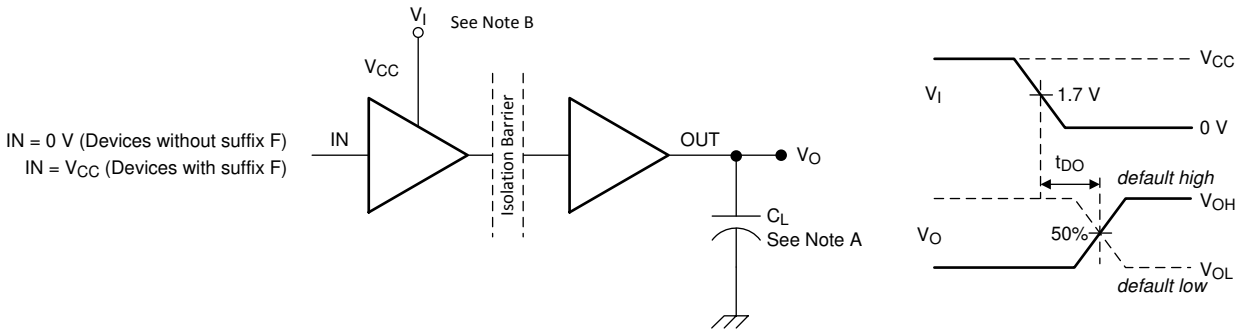
図 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

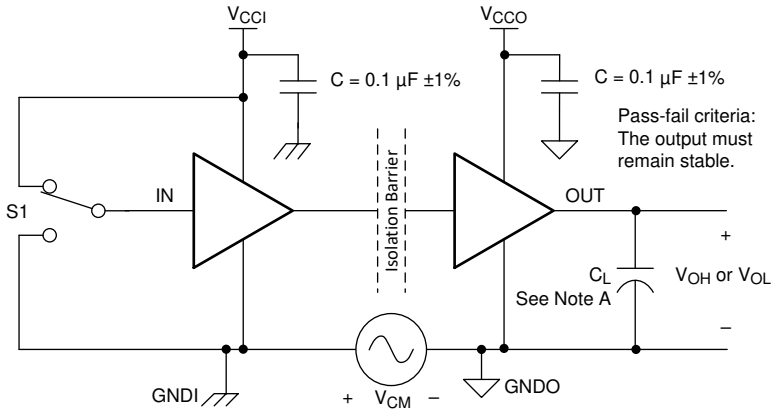
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. Power Supply Ramp Rate = 10 mV/ns

図 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO773x-Q1 family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO773x-Q1 family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

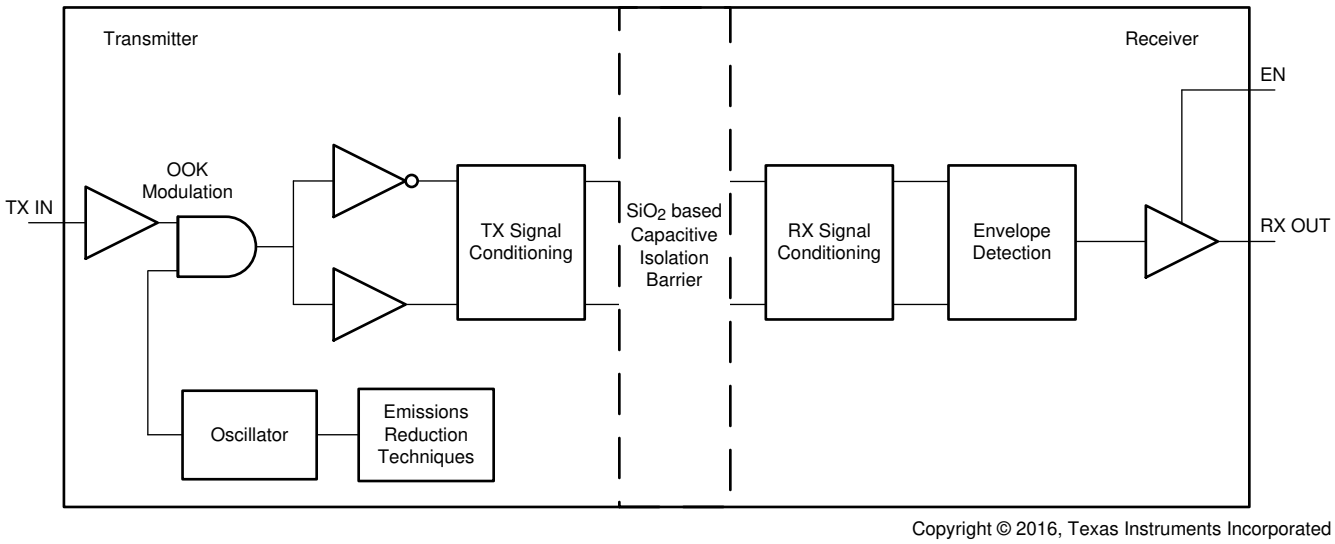


図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

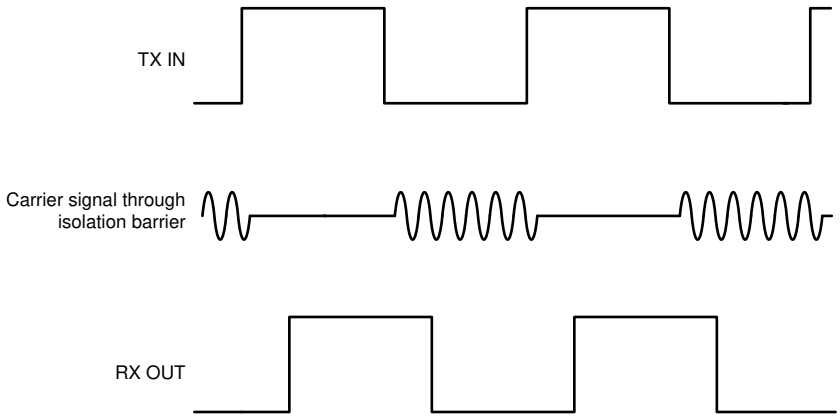


図 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

表 7-1 provides an overview of the device features.

表 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7730-Q1	3 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7730-Q1 with F suffix	3 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7731-Q1	2 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7731-Q1 with F suffix	2 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See *セクション 5.7* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO773x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.4 Device Functional Modes

表 7-2 lists the functional modes for the ISO773x-Q1 devices.

表 7-2. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx)(3)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO773x-Q1 and *Low* for ISO773x-Q1 with F suffix.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO773x-Q1 and *Low* for ISO773x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(3) A strongly driven input signal can weakly power the floating V_{CC} using an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

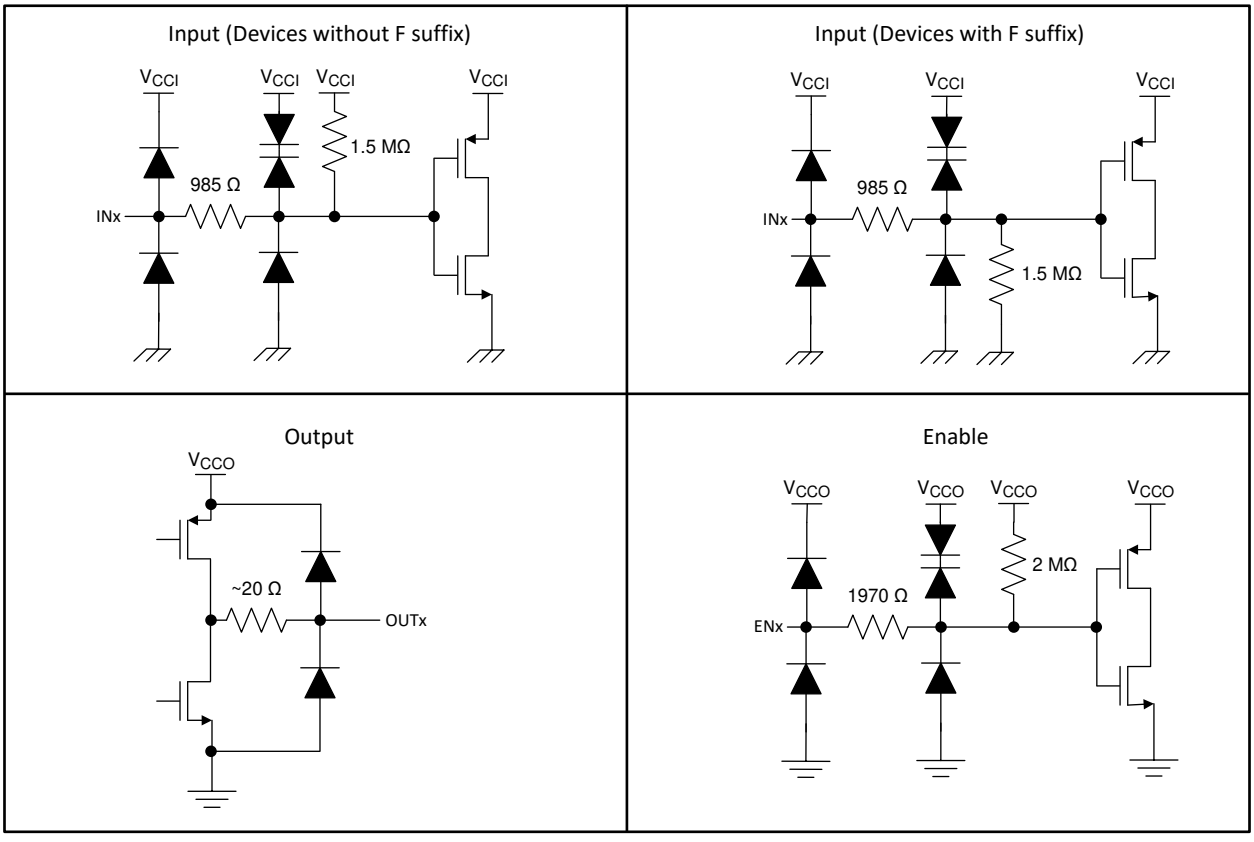


図 7-3. Device I/O Schematics

8 Application and Implementation

注

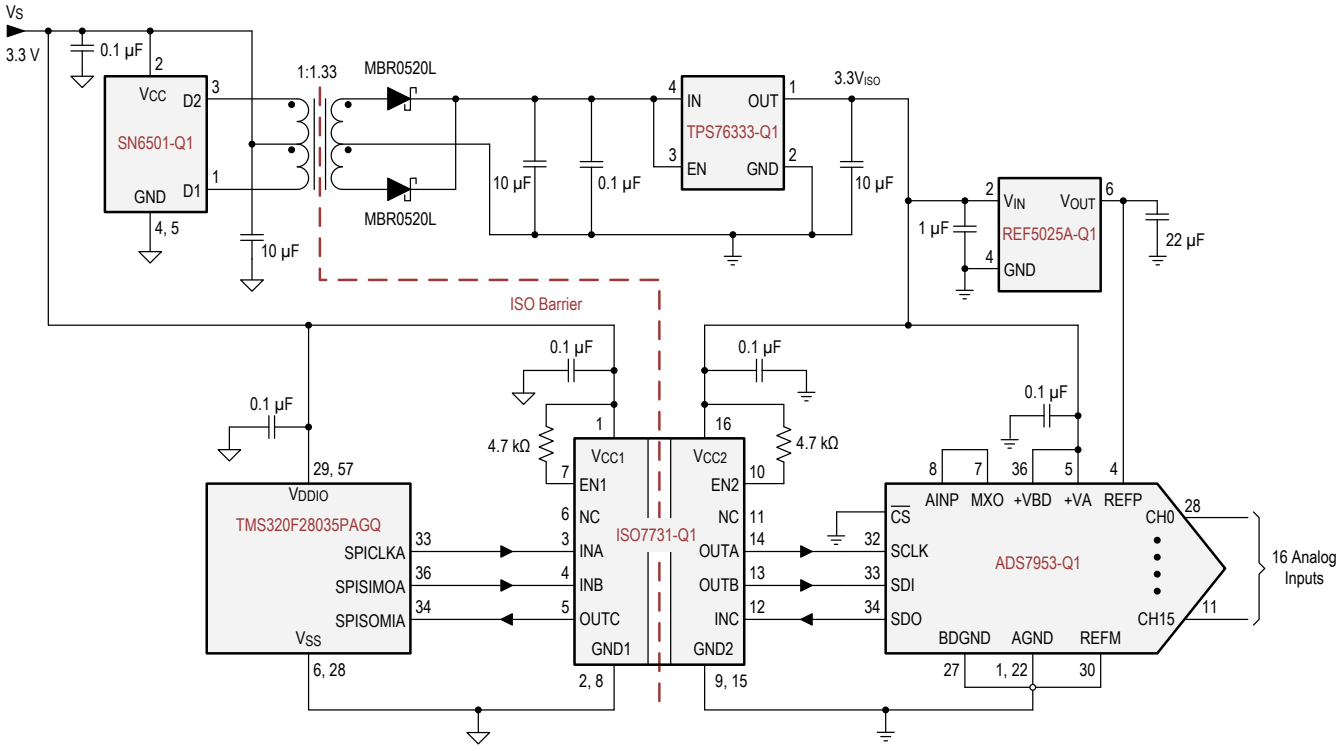
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The ISO773x-Q1 devices are high-performance, triple-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO773x-Q1 family of devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

The ISO7731-Q1 device combined with Texas Instruments' Piccolo™ microcontroller, analog-to-digital receiver, transformer driver, and voltage regulator can create an isolated serial peripheral interface (SPI) as shown in 図 8-1.



Multiple pins and discrete components are omitted for clarity.

図 8-1. Isolated SPI for an Analog Input Module With 16 Inputs and a Single Slave

8.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO773x-Q1 family of devices only requires two external bypass capacitors to operate. 図 8-2 and 図 8-3 show the typical circuit hook-up for the devices.

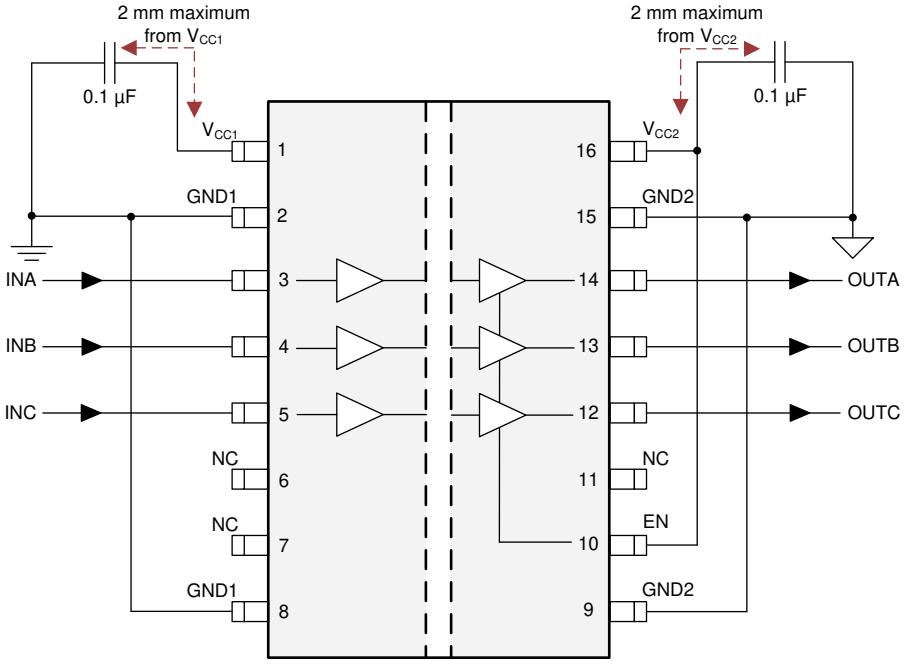


図 8-2. Typical ISO7730-Q1 Circuit Hook-Up

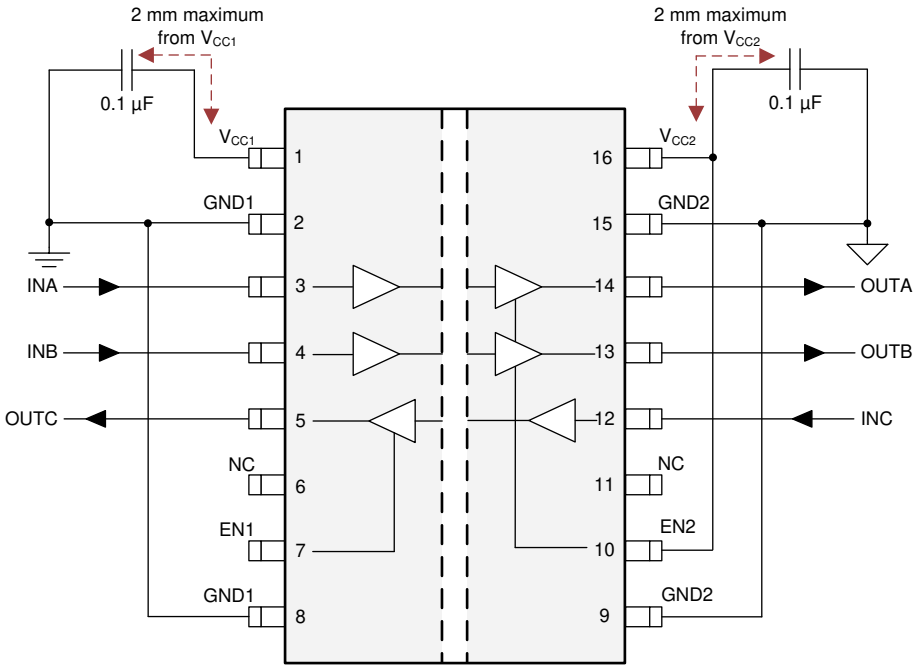


図 8-3. Typical ISO7731-Q1 Circuit Hook-Up

8.2.3 Application Curves

The following typical eye diagrams of the ISO773x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

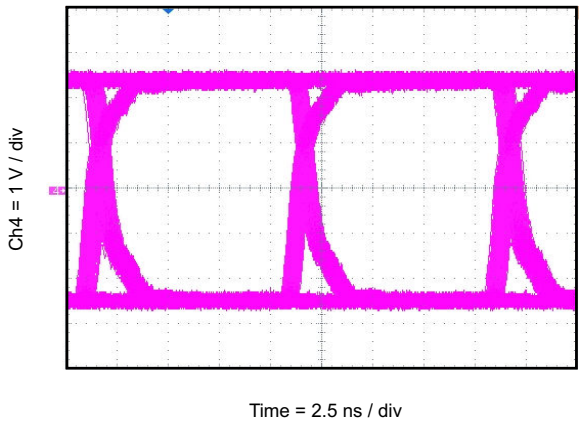


図 8-4. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 5 V and 25°C

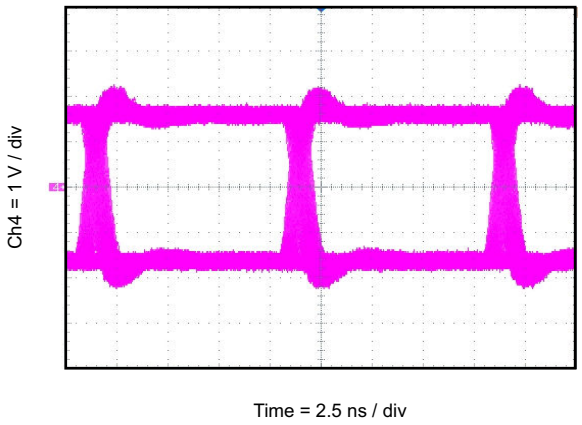


図 8-5. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

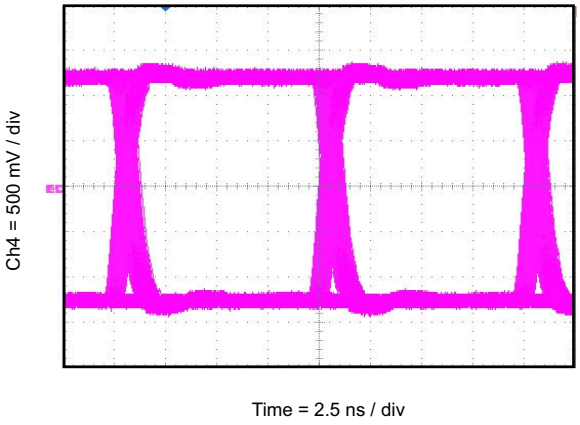


図 8-6. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

8.2.3.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 図 8-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

図 8-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years. DBQ-16 package at 400 V_{RMS} working voltage has a much longer lifetime than DW-16 package.

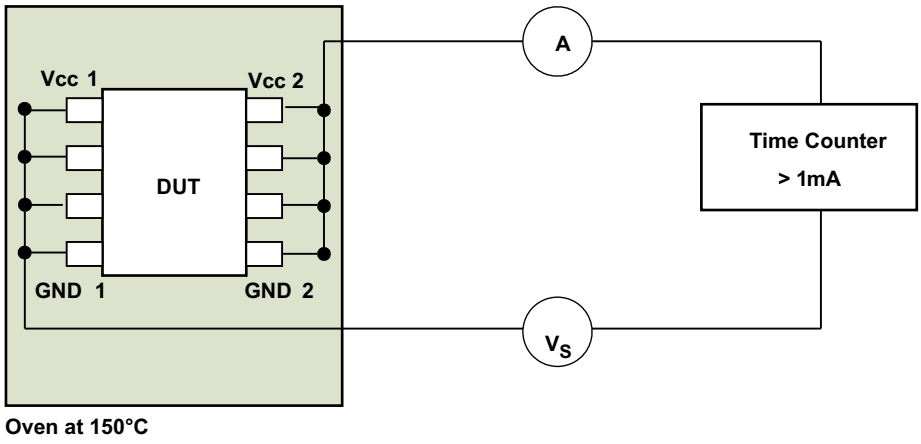


図 8-7. Test Setup for Insulation Lifetime Measurement

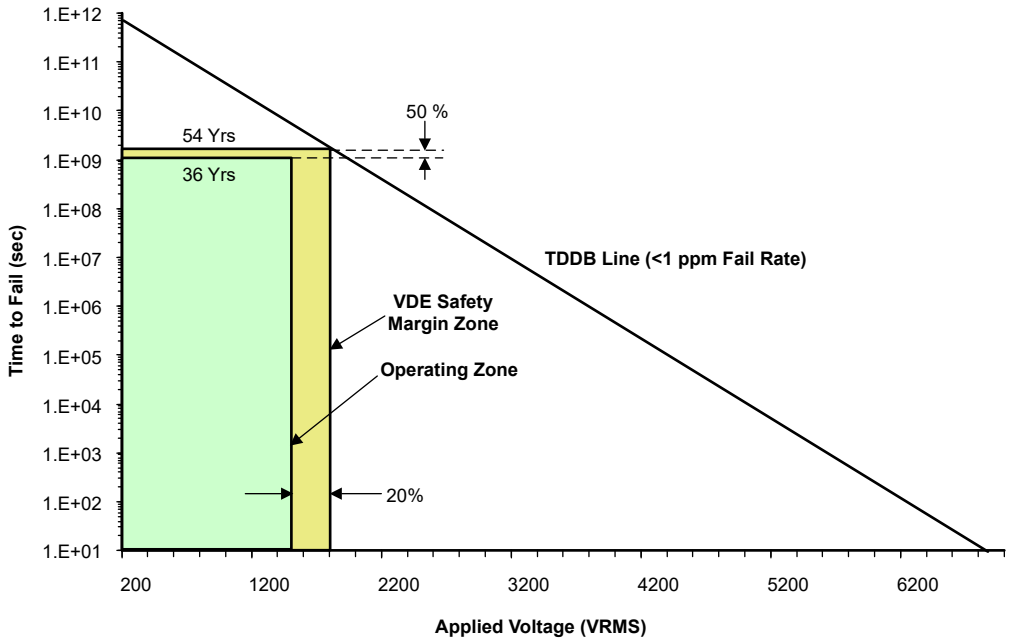


図 8-8. Insulation Lifetime Projection Data

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501-Q1 . For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet .

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 8-9). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

8.4.2 Layout Example

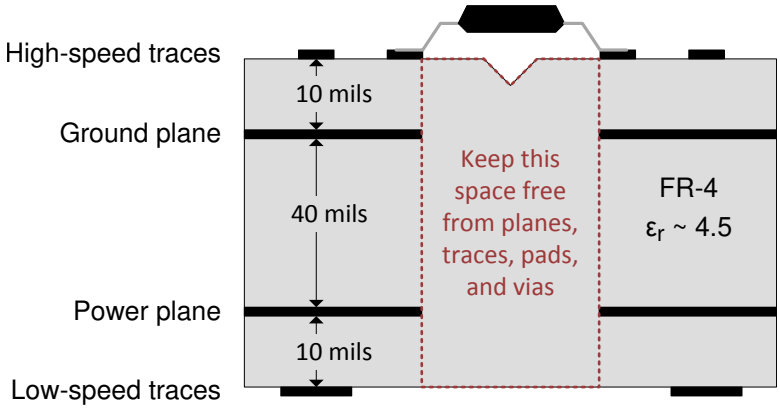


図 8-9. Layout Example Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems* application report
- Texas Instruments, *REF50xxA-Q1 Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, TPS76333-Q1 *Low-Power 150-mA Low-Dropout Linear Regulators* data sheet
- Texas Instruments, TMS320F28035 *Piccolo™ Microcontrollers* data sheet

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7730-Q1	Click here	Click here	Click here	Click here	Click here
ISO7731-Q1	Click here	Click here	Click here	Click here	Click here

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (August 2023) to Revision F (October 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations 6
- Updated electrical and switching characteristics to match device performance 6
- Updated maximum power dissipation in the power ratings section 8
- Updated distance through isolation, while maintaining all other insulation specifications 9
- Updated table entries 11
- Updated the input leakage current for ENx pins throughout the electrical characteristic sections 13
- Updated maximum total current consumption values throughout the supply current characteristics sections 14
- Updated maximum propagation delay specifications throughout the switching characteristics sections 19
- Updated the TDDB plot and the projected lifetime 33

Changes from Revision D (October 2020) to Revision E (August 2023) **Page**

- ドキュメント全体を通して標準名を以下のように変更:「DIN V VDE V 0884-11:2017-01」から「DIN EN IEC 60747-17 (VDE 0884-17)」 1
- ドキュメント全体を通して、すべての標準名から標準リビジョンおよび年への参照を削除 1
- Added V_{TEST} conditions for V_{IOTM}, updated DBQ package throughout the document, and updated method b1 condition 9
- Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDB from: 135 years to: 169 years per DIN EN IEC 60747-17 (VDE 0884-17) 33
- Changed 図 8-8 per DIN EN IEC 60747-17 (VDE 0884-17 33

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11 Mechanical, Packaging, and Orderable Information

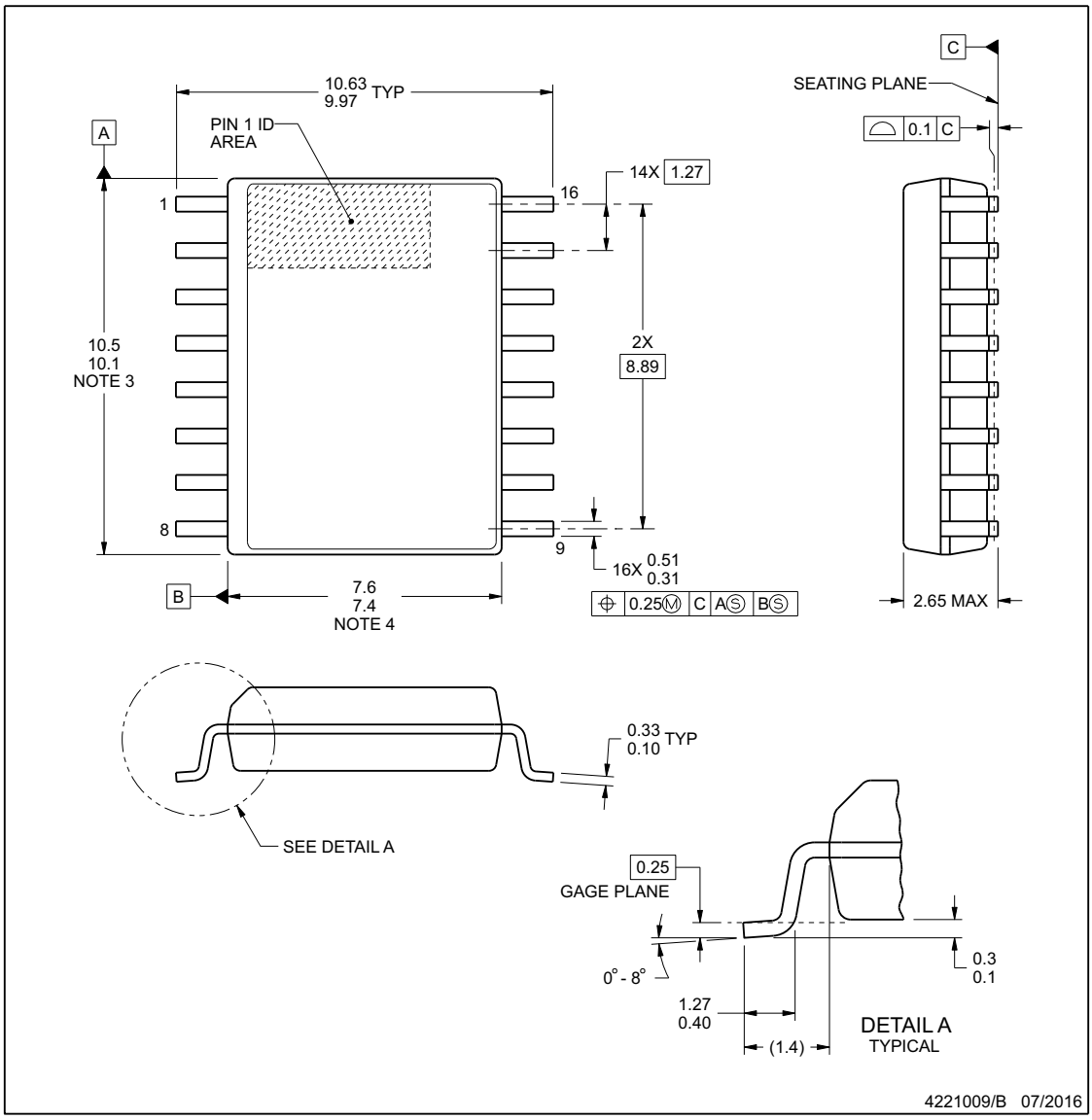
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

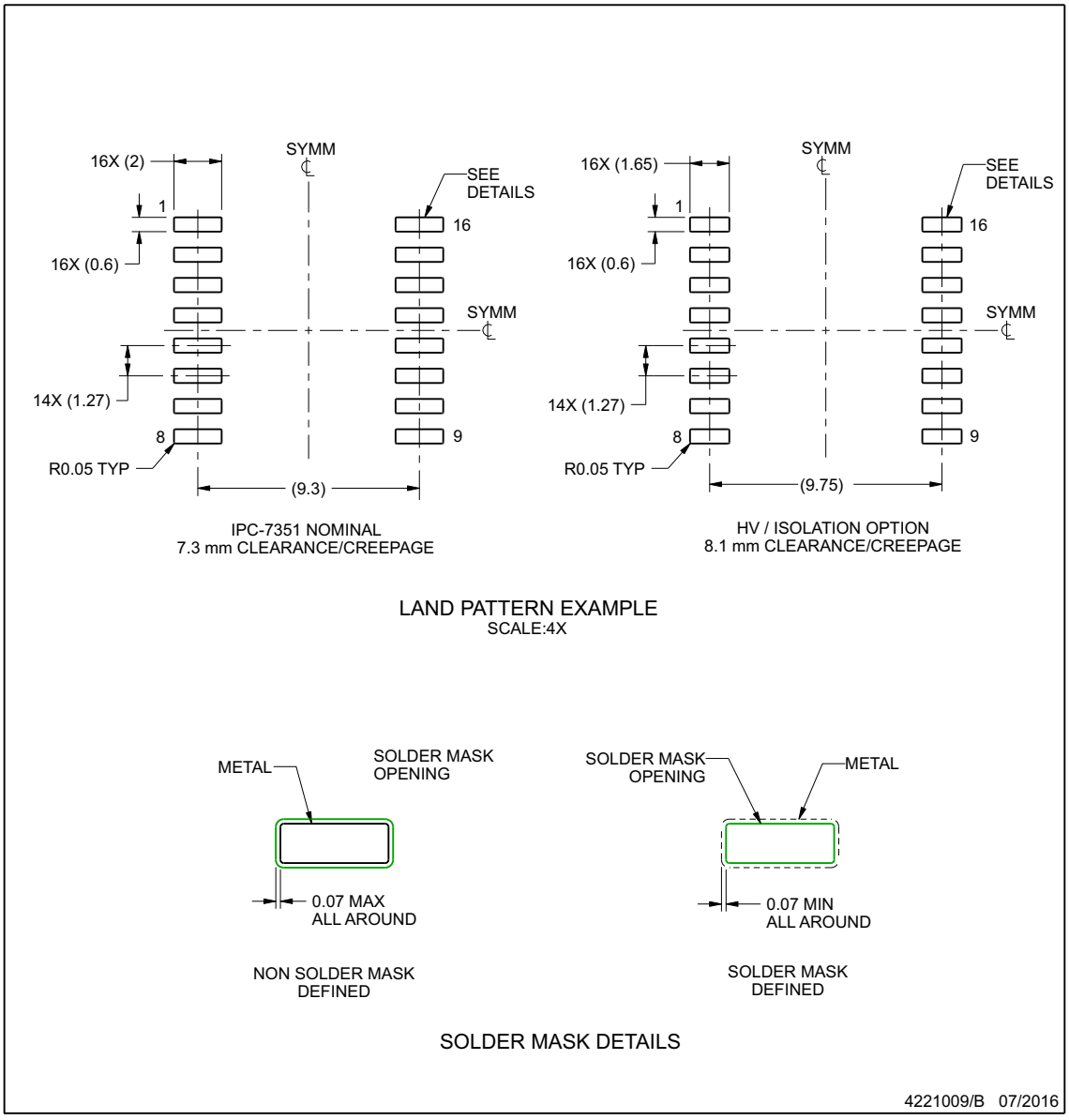
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

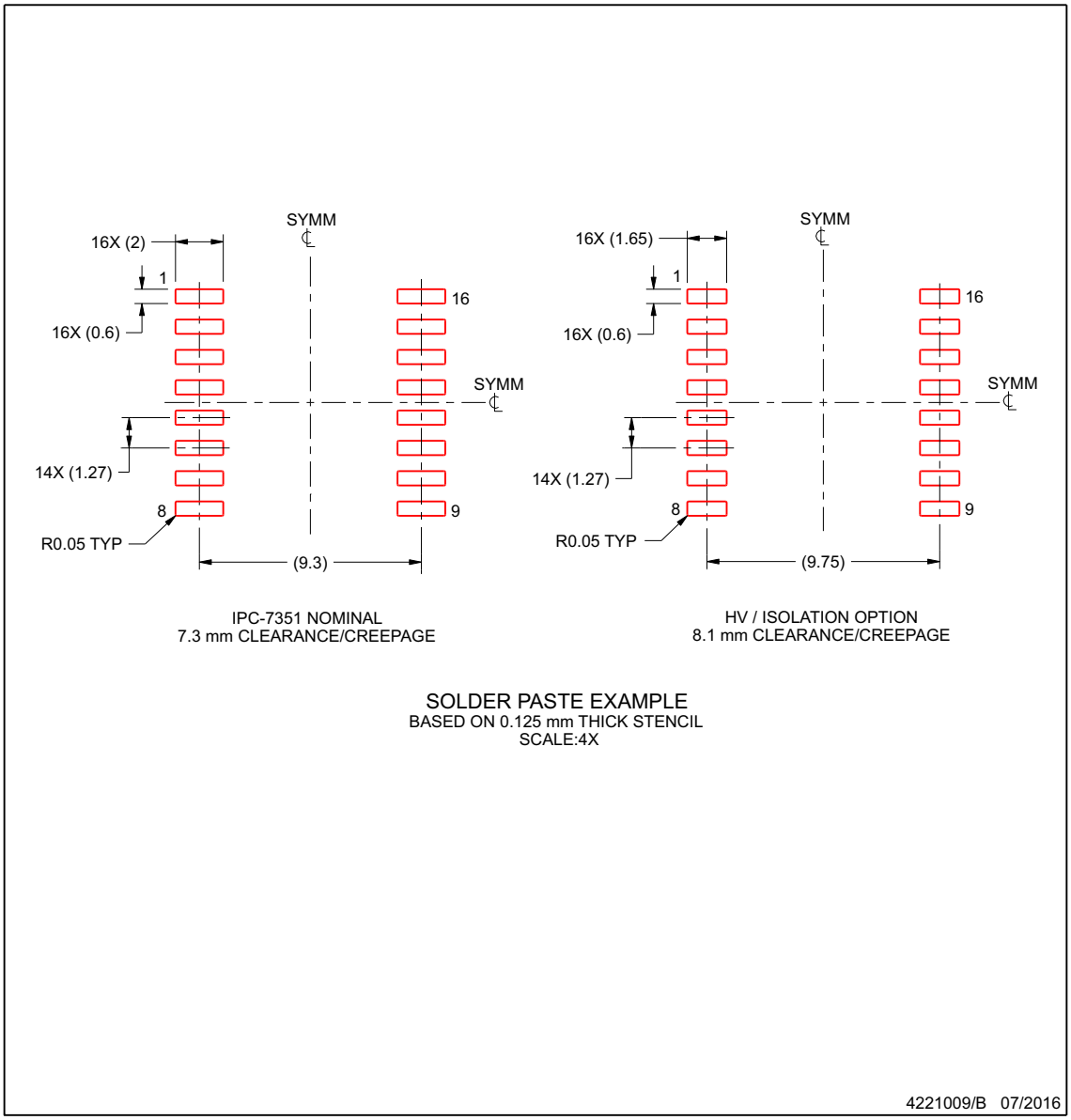
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

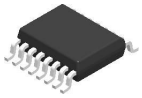
SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

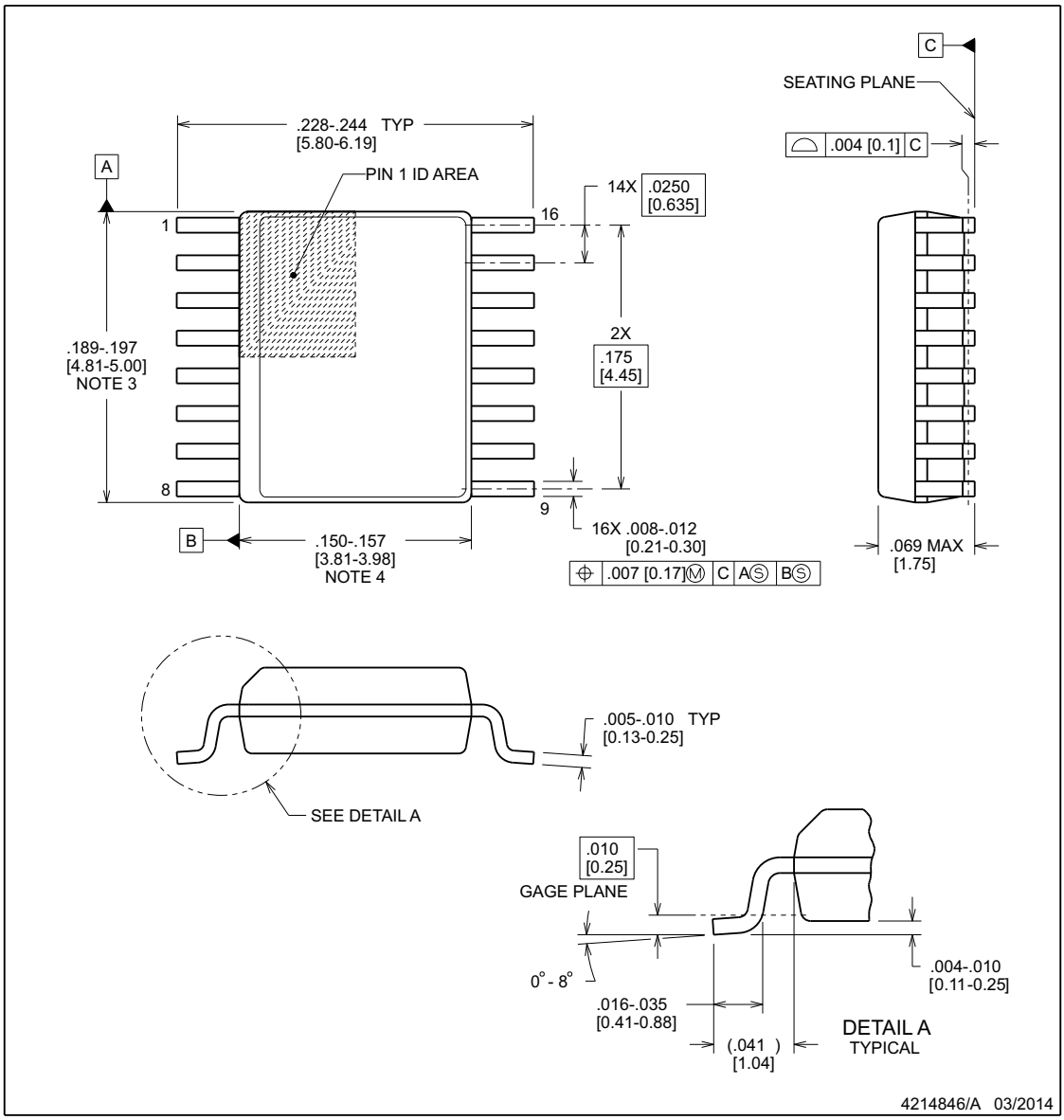


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

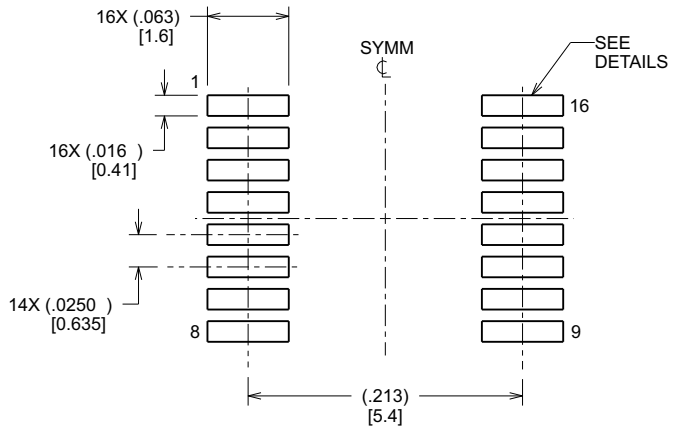
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

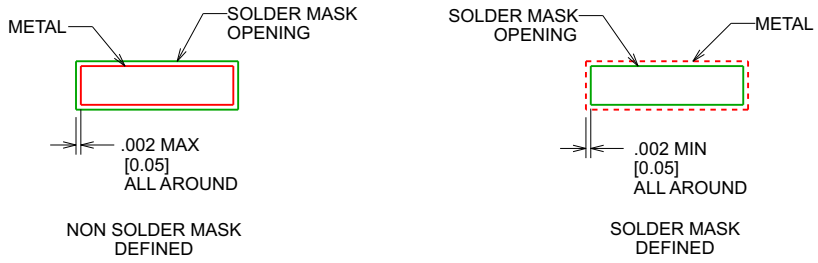
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

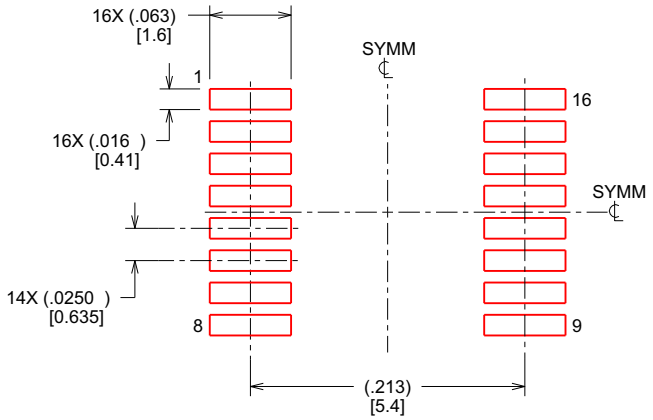
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7730FQDBQQ1	LIFEBUY	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730FQ	
ISO7730FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730FQ	Samples
ISO7730FQDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730FQ	
ISO7730FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7730F, ISO7730 FQ)	Samples
ISO7730QDBQQ1	LIFEBUY	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730Q	
ISO7730QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7730Q	Samples
ISO7730QDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7730Q	
ISO7730QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7730, ISO7730Q)	Samples
ISO7731FQDBQQ1	LIFEBUY	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731FQ	
ISO7731FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731FQ	Samples
ISO7731FQDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731FQ	
ISO7731FQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7731F, ISO7731 FQ)	Samples
ISO7731QDBQQ1	LIFEBUY	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731Q	
ISO7731QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7731Q	Samples
ISO7731QDWQ1	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731Q	
ISO7731QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7731, ISO7731Q)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7730-Q1, ISO7731-Q1 :

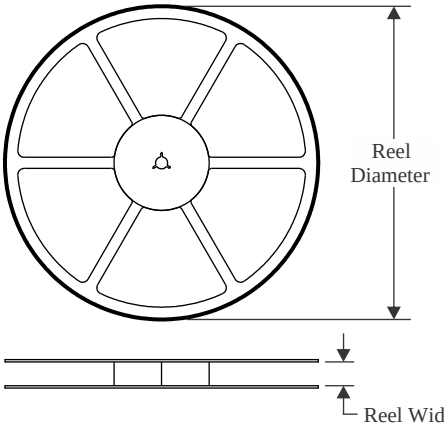
- Catalog : ISO7730, ISO7731

NOTE: Qualified Version Definitions:

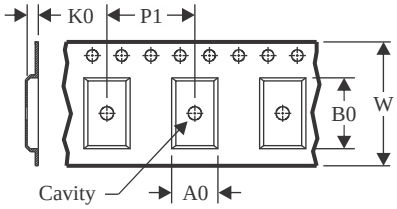
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

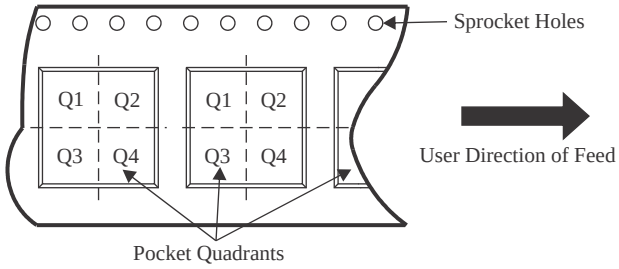


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

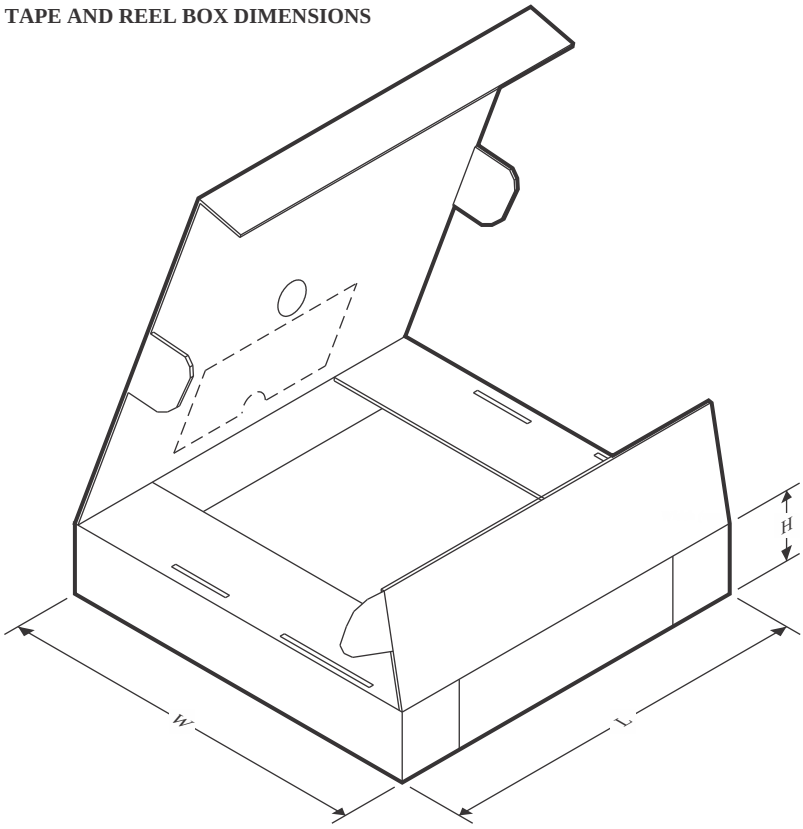


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7730QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

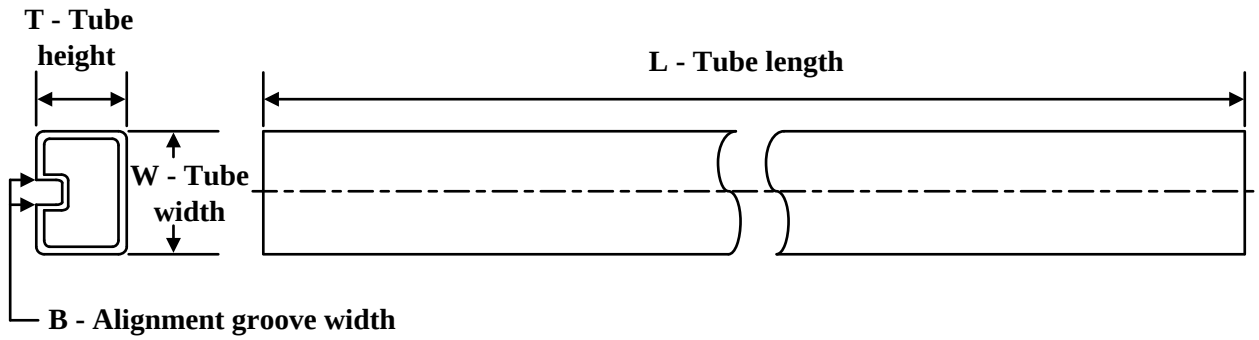


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7730QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7730QDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7731FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7731QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7731QDWRQ1	SOIC	DW	16	2000	367.0	367.0	45.0
ISO7731QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7730FQDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7730FQDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7730FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7730QDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7730QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7730QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7731FQDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7731FQDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7731FQDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7731QDBQQ1	DBQ	SSOP	16	75	505.46	6.76	3810	4
ISO7731QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
ISO7731QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

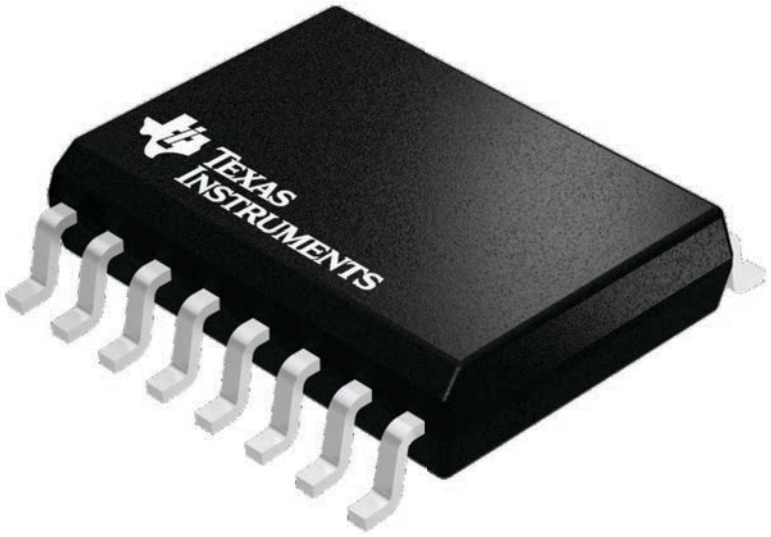
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

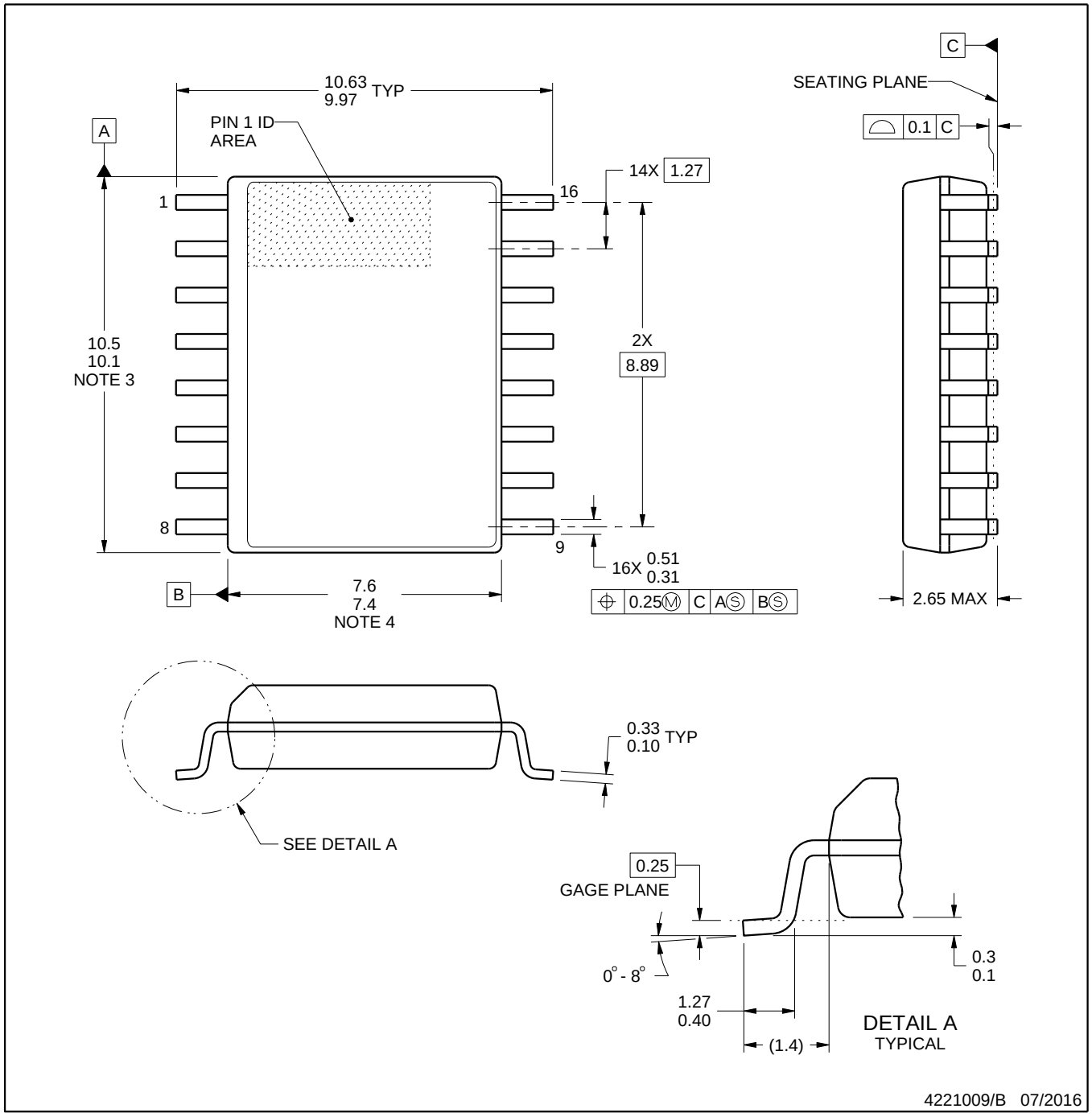
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



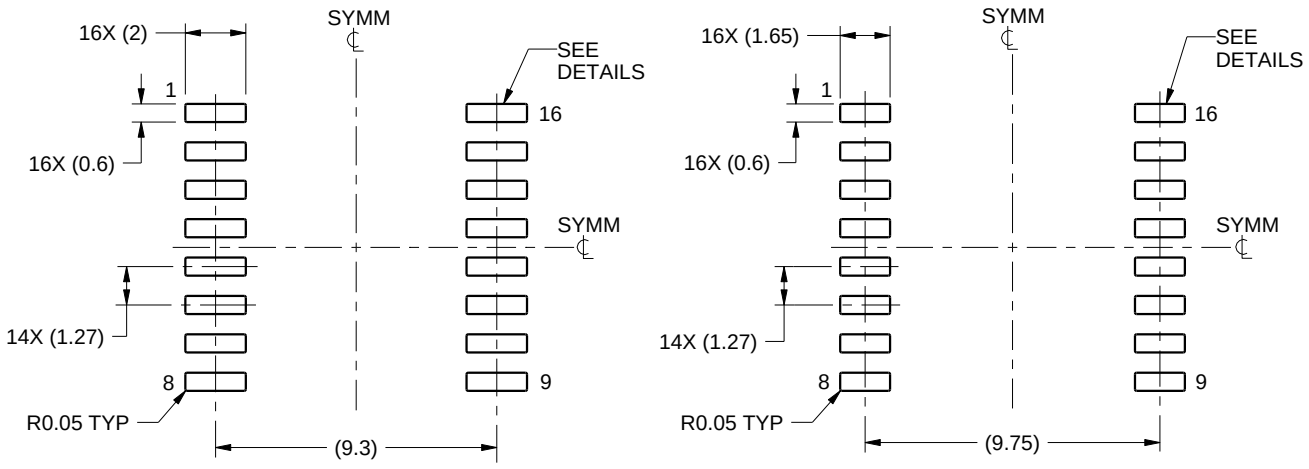
4224780/A

SOIC



NOTES:

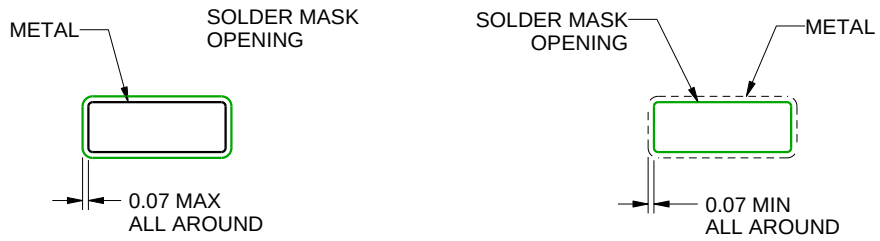
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

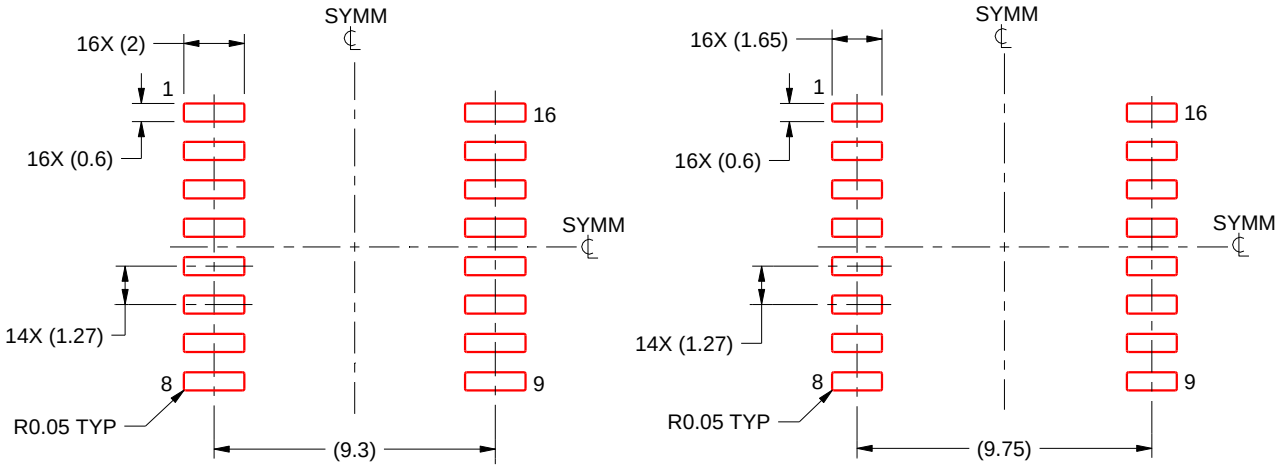
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

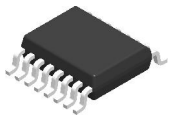
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

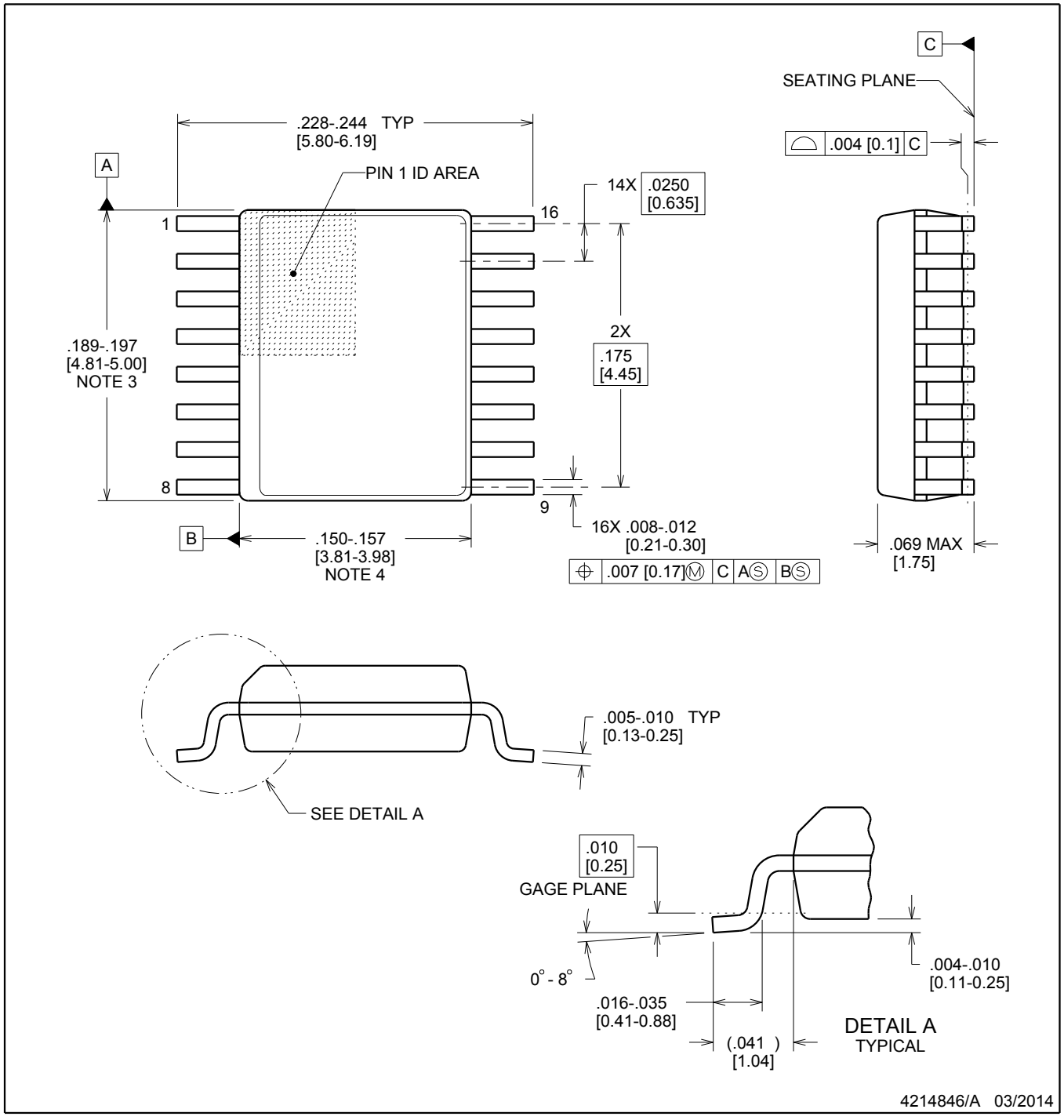


PACKAGE OUTLINE

DBQ0016A

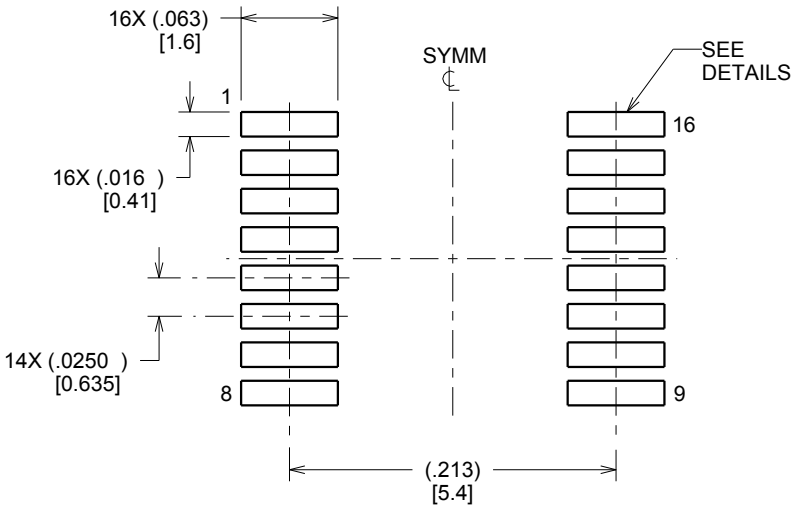
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

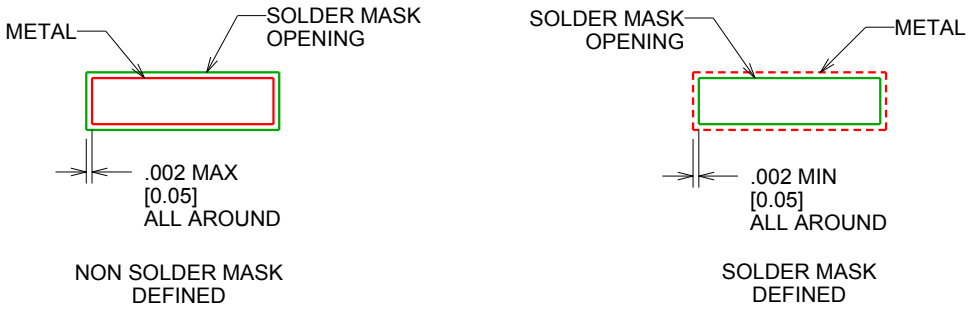


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

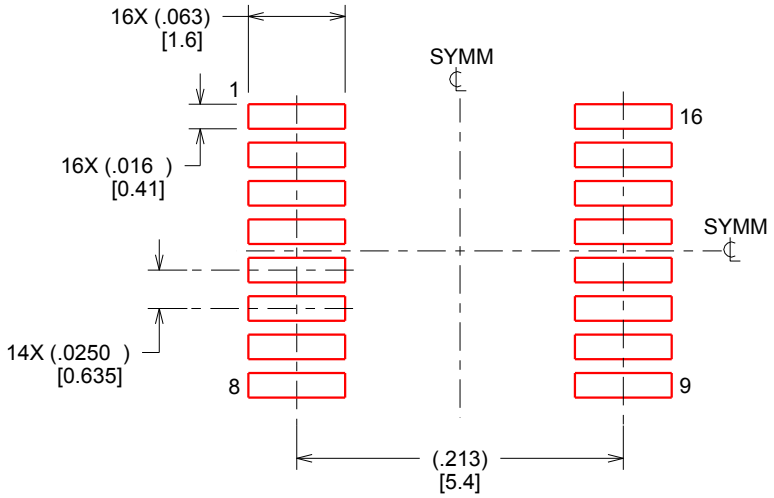
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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