ISO7821x 高性能、8000V_{PK} 強化絶縁デュアル チャネル デジタル アイソレータ

1 特長

- 信号速度:最大 100Mbps
- 広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧変換
- 広い温度範囲:-55℃～125℃
- 低い消費電力:1Mbps のとき、チャネルあたり 1.8mA (標準値)
- 小さい伝搬遅延時間:標準値 11ns (5V 電源)
- 業界をリードする CMTI (最小値):±100kV/μs
- 堅牢な電磁環境適合性 (EMC)
- システム レベルでの ESD、EFT、サージ耐性
- 低い放射
- 絶縁バリアの寿命:25 年超
- SOIC-16 幅広 (DW) および超幅広 (DWW) パッケージ オプション
- 安全および規制の認定:
  - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 に準拠した 8000V_{PK} の強化絶縁耐圧
  - UL 1577 に準拠した 5.7 kV_{RMS} での 1 分間の絶縁
  - CSA Component Acceptance Notice 5A、IEC 60950-1、および IEC 60601-1 最終機器標準
  - GB4943.1-2011 準拠の CQC 認定
  - EN 61010-1 および EN 60950-1 準拠の TUV 認定
  - すべての DW パッケージ認証は完了、DWW パッケージ認証は UL、TUV については完了、VDE、CSA、CQC については計画中

2 アプリケーション

- 産業用オートメーション
- モータ制御
- 電源
- ソーラー インバータ
- 医療機器
- ハイブリッド電気自動車 (HEV)

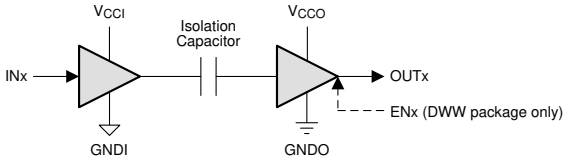
3 概要

ISO7821 は、8000V_{PK} の絶縁電圧を持つ高性能デュアルチャネル デジタル アイソレータです。このデバイスは、VDE、CSA、TUV、CQC に準拠した強化絶縁認証を取得しています。本アイソレータは、CMOS や LVCMOS のデジタル I/O を絶縁しながら、低消費電力で高い電磁気耐性と低い放射を実現します。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二酸化ケイ素 (SiO_2) の絶縁バリアによって分離されています。ISO7821 には、1 つの順方向チャネルと 1 つの逆方向チャネルがあります。入力電源または信号が失われた場合、デフォルト出力は、ISO7821 では「High」、ISO7821F デバイスでは「Low」です。このデバイスを絶縁型電源と組み合わせて使用すると、データ バスまたは他の回路上のノイズ電流がローカル グランドに入り込んでノイズに敏感な回路に干渉または損傷を与えることを防止できます。革新的なチップ設計およびレイアウト技法により、ISO7821 は電磁両立性が大幅に強化されているため、システム レベルの ESD、EFT、サージ、および放射のコンプライアンスを容易に達成できます。ISO7821 は、16 ピン SOIC 幅広 (DW) および超幅広 (DWW) パッケージで供給されます。DWW パッケージ オプションにはイネーブル ピンがあり、対応する出力を高インピーダンスに移行して、マルチ コントローラ駆動アプリケーションや、消費電力の低減に使用できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO7821、ISO7821F	DW (SOIC、16)	10.30mm × 7.50mm	
	DWW (超幅広 SOIC、16)	10.30mm × 14.0mm	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



A. V_{CCI} および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。
B. V_{CCO} および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

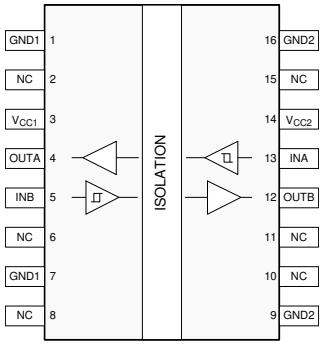

図 4-1. DW Package 16-Pin (SOIC) Top View

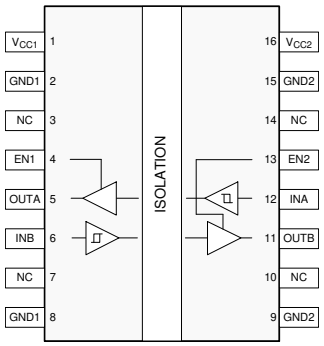

図 4-2. DWW Package 16-Pin (SOIC) Top View

表 4-1. Pin Functions

PIN			Type	DESCRIPTION
NAME	NO.	NO.		
	DW	DWW		
GND1	1, 7	2,8	–	Ground connection for V_{CC1}
GND2	9, 16	9,15	–	Ground connection for V_{CC2}
INA	13	12	I	Input, channel A
INB	5	6	I	Input, channel B
NC	2, 6, 8, 10 ,11, 15	3,7,10,14	–	Not connected
OUTA	4	5	O	Output, channel A
OUTB	12	11	O	Output, channel B
V_{CC1}	3	1	–	Power supply, V_{CC1}
V_{CC2}	14	16	–	Power supply, V_{CC2}
EN1	–	4	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	–	13	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.

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5 Specifications

5.1 Absolute Maximum Ratings

(1)		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx	–0.5	V_{CC} + 0.5(3)	V
Output Current	I_O	-15	15	mA
Surge Immunity			12.8	kV
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO} (2) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			
		V_{CCO} = 2.5 V	-1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 x $V_{CC\ I}$ (2)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 x V_{CCI}	V
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature(1)		-55		150	°C
T_A	Ambient temperature		-55	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.4 Thermal Information

THERMAL METRIC[1]		ISO7821		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 PINS	16-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.7	84.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	47.3	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	54.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.1	18.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.8	53.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Dissipation Characteristics

			VALUE	UNIT
P_D	Maximum power dissipation by ISO7821	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 50 MHz 50% duty cycle square wave	100	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7821 x		50	
P_{D2}	Maximum power dissipation by side-2 of ISO7821 x		50	

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5.6 Electrical Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see 図 6-4	100			kV/μs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.4	3.2	mA
I_{CC1}, I_{CC2}	100 Mbps			7.5	9.3	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.7	mA
I_{CC1}, I_{CC2}	10 Mbps			2.5	3.2	mA
I_{CC1}, I_{CC2}	100 Mbps			7.7	9.3	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.7 Electrical Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see 図 6-4	100			kV/μs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.2	3	mA
I_{CC1}, I_{CC2}	100 Mbps			5.8	7.1	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.3	3	mA
I_{CC1}, I_{CC2}	100 Mbps			5.9	7.1	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.8 Electrical Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see 図 6-4	100			kV/μs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.1	2.8	mA
I_{CC1}, I_{CC2}	100 Mbps			4.9	5.9	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.2	2.9	mA
I_{CC1}, I_{CC2}	100 Mbps			5	6	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.9 Power Ratings

表 5-1. IEC 60664-1 Ratings Table

PARAMETER		TEST CONDITIONS	SPECIFICATION
Material group			I
Overvoltage category / Installation classification	DW package	Rated mains voltage ≤ 600 V_{RMS}	I–IV
		Rated mains voltage ≤ 1000 V_{RMS}	I–III
	DWW package	Rated mains voltage ≤ 1000 V_{RMS}	I–IV

5.10 Insulation Specifications

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表 5-2. Insulation Characteristics

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	µm
V_{IOWM}	Maximum working isolation voltage	Time dependent dielectric breakdown (TDDB) test	1500	2000	V_{RMS}
			2121	2828	V_{DC}
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12					
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (1) (qualification)	8000	8000	V_{PK}
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{PR}	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	2545	3394	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	3394	4525	
		Method b1,After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	5303	
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	$>10^9$	Ω
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 sec (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 sec (100% production)	5700	5700	V_{RMS}

(1) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

表 5-3. Package Insulation and Safety-Related Specifications

(over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLR	External clearance	Shortest terminal-to-terminal distance through air	DW-16	8.15			mm
			DWW-16	14.5	15.0		
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	DW-16	8.15			mm
			DWW-16	14.5	15.0		
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		600			V
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		10^{11}			Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz			1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 x sin (2πft), f = 1 MHz, V_{CC} = 5 V			2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

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注

Creepage and clearance requirements must be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to verify that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

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5.11 Safety-Related Certifications

DW package certifications are complete; DWW package certifications completed for UL and TUV and planned for VDE, CSA, and CQC.

表 5-4. Regulatory Information

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW), 2828 V_{PK} (DWW); Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage (DW package)	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW package) and 1000 V_{RMS} (DWW package) 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

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5.12 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

表 5-5. Safety Limiting

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current for DW-16 package and DWW-16 Packages	$R_{\theta JA}$ = 84.7°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			268	mA
		$R_{\theta JA}$ = 84.7°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			410	
		$R_{\theta JA}$ = 84.7°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			537	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.7°C/W, T_J = 150°C, T_A = 25°C			1476	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *セクション 5.4* is that of a device installed on a High-K test board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

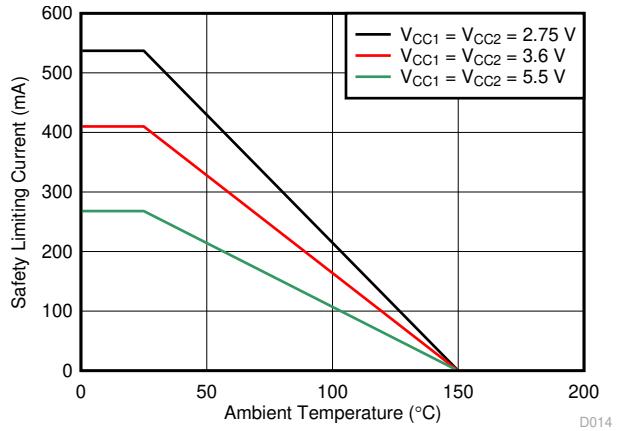

図 5-1. Thermal Derating Curve for Safety Limiting Current per VDE

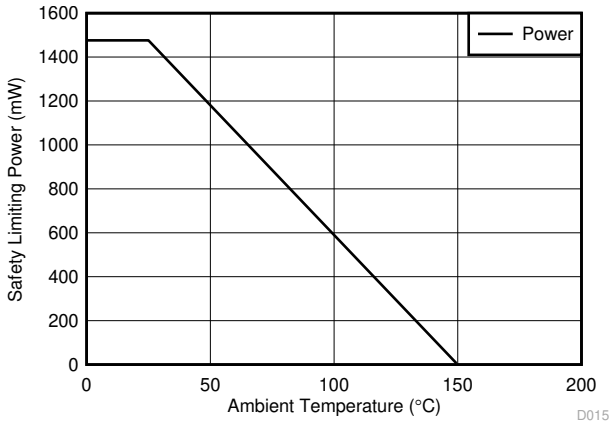

図 5-2. Thermal Derating Curve for Safety Limiting Power per VDE

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5.13 Switching Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	10.7	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.6	4.6	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See 図 6-1		2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See 図 6-2		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.14 Switching Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	10.8	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.7	4.7	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See 図 6-1		1.3	3	ns
t_f	Output signal fall time			1.3	3	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See 図 6-2		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.15 Switching Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	7.5	11.7	17.5	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.7	4.7	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See 図 6-1		1.8	3.5	
t_f	Output signal fall time			1.8	3.5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See 図 6-2		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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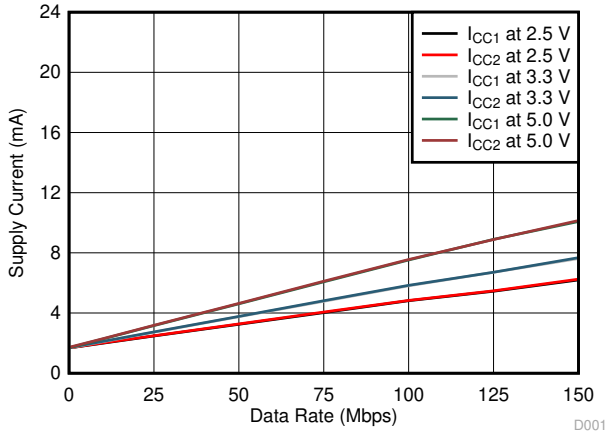
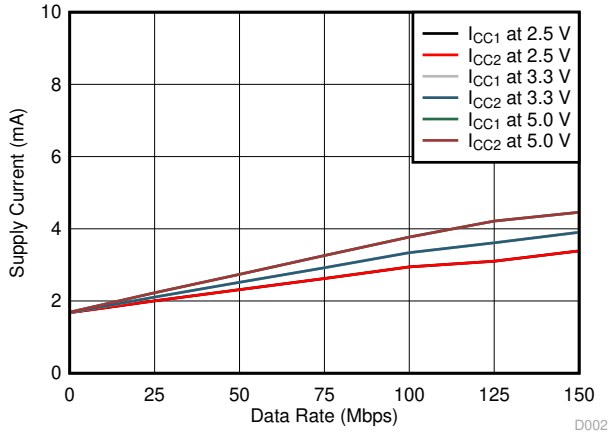
5.16 Typical Characteristics



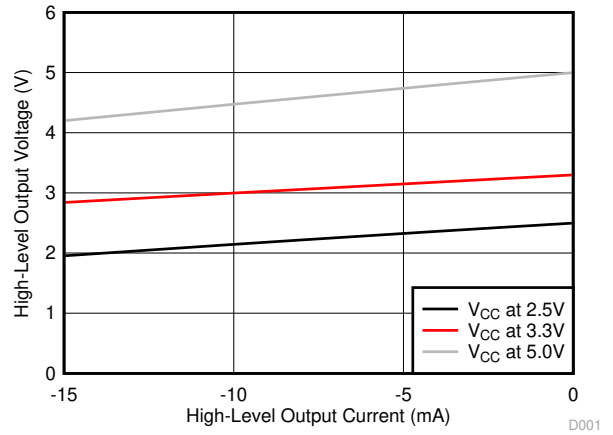
T_A = 25°C C_L = 15 pF

図 5-3. Supply Current vs Data Rate (With 15 pF Load)



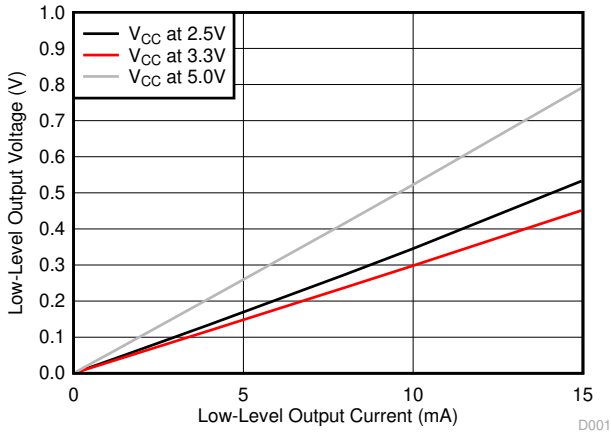
T_A = 25°C C_L = No Load

図 5-4. Supply Current vs Data Rate (With No Load)



T_A = 25°C

図 5-5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

図 5-6. Low-Level Output Voltage vs Low-Level Output Current

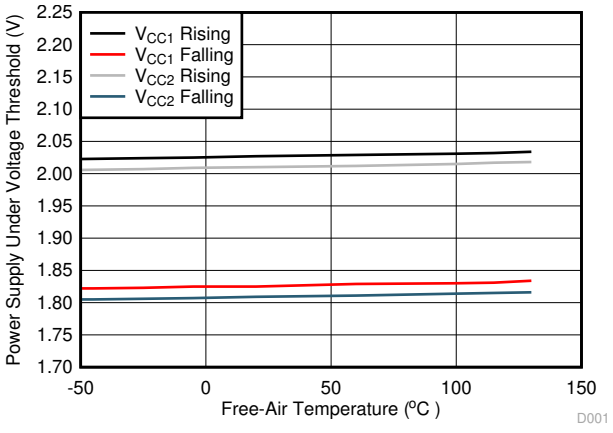


図 5-7. Power Supply Undervoltage Threshold vs Free-Air Temperature

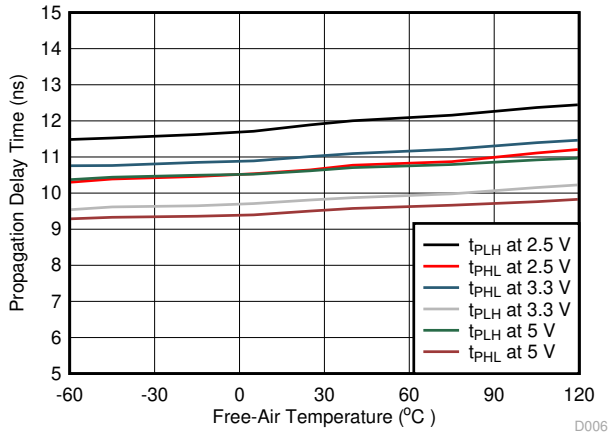


図 5-8. Propagation Delay Time vs Free-Air Temperature

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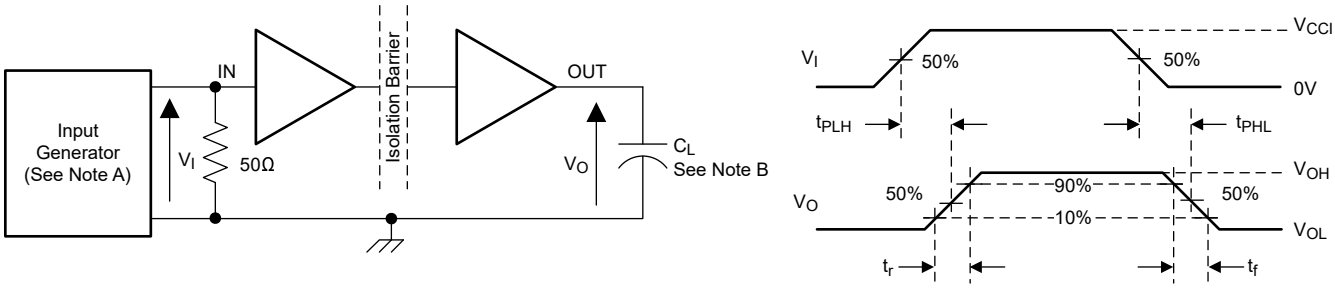
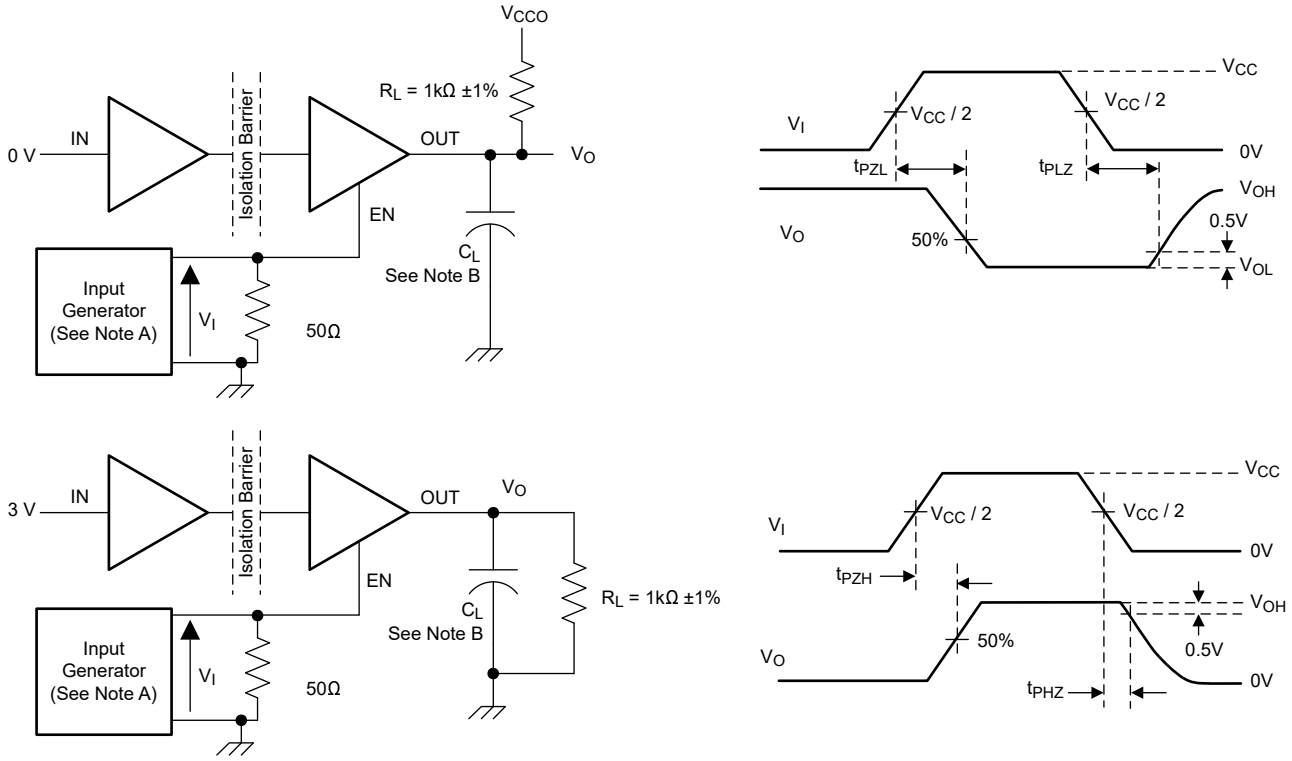
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω resistor is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

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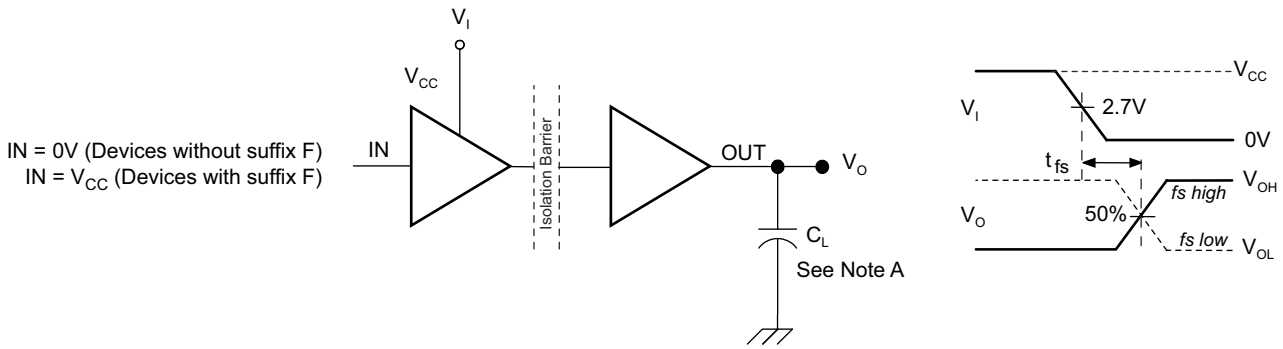
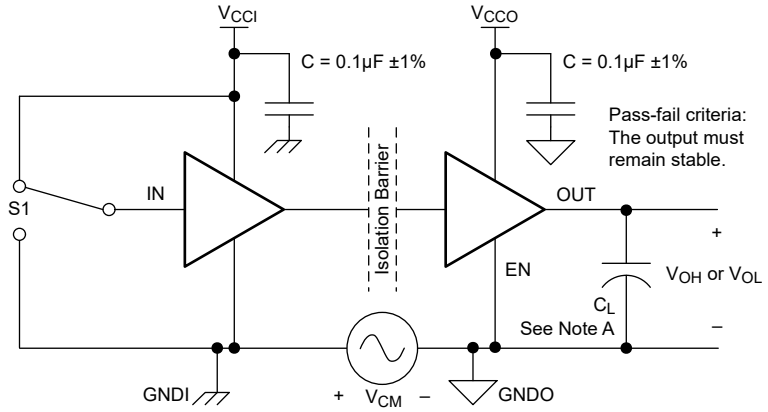


A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

ISO7821 employs an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

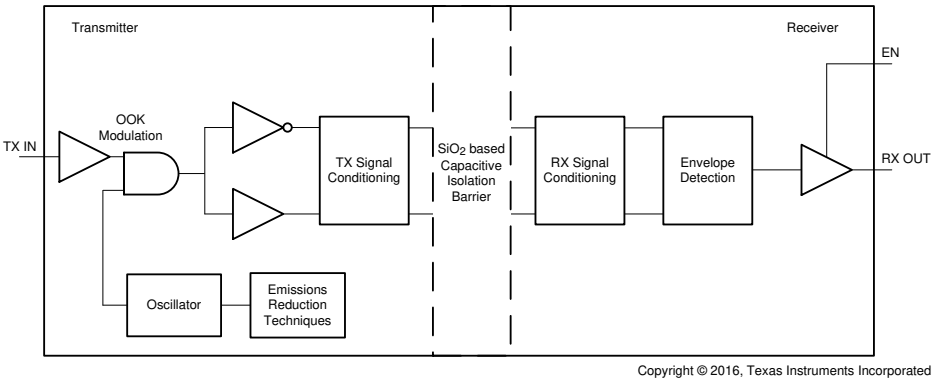


図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Also a conceptual detail of how the ON/OFF Keying scheme works is shown in 図 7-2.

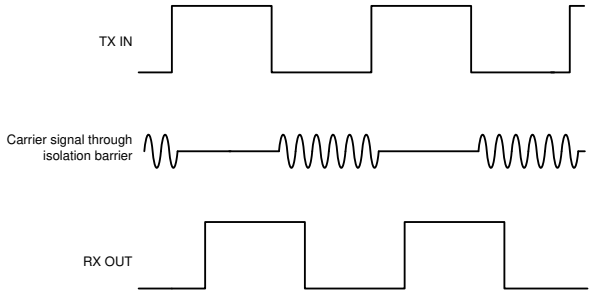


図 7-2. On-Off Keying (OOK) Based Modulation Scheme

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7.3 Feature Description

ISO7821 is available in two channel configurations and default output state options to enable a variety of application uses.

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7821	1 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7821F	1 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See the *Regulatory Information* section for detailed isolation ratings.

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7.4 Device Functional Modes

ISO7821 functional modes are shown in 表 7-1.

表 7-1. ISO7821 Function Table

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx) (DWW Package Only)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default high logic state. Default= High for ISO7821 and Low for ISO7821F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for ISO7821 and Low for ISO7821F. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (1). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(2) A strongly driven input signal can weakly power the floating V_{CC} using an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

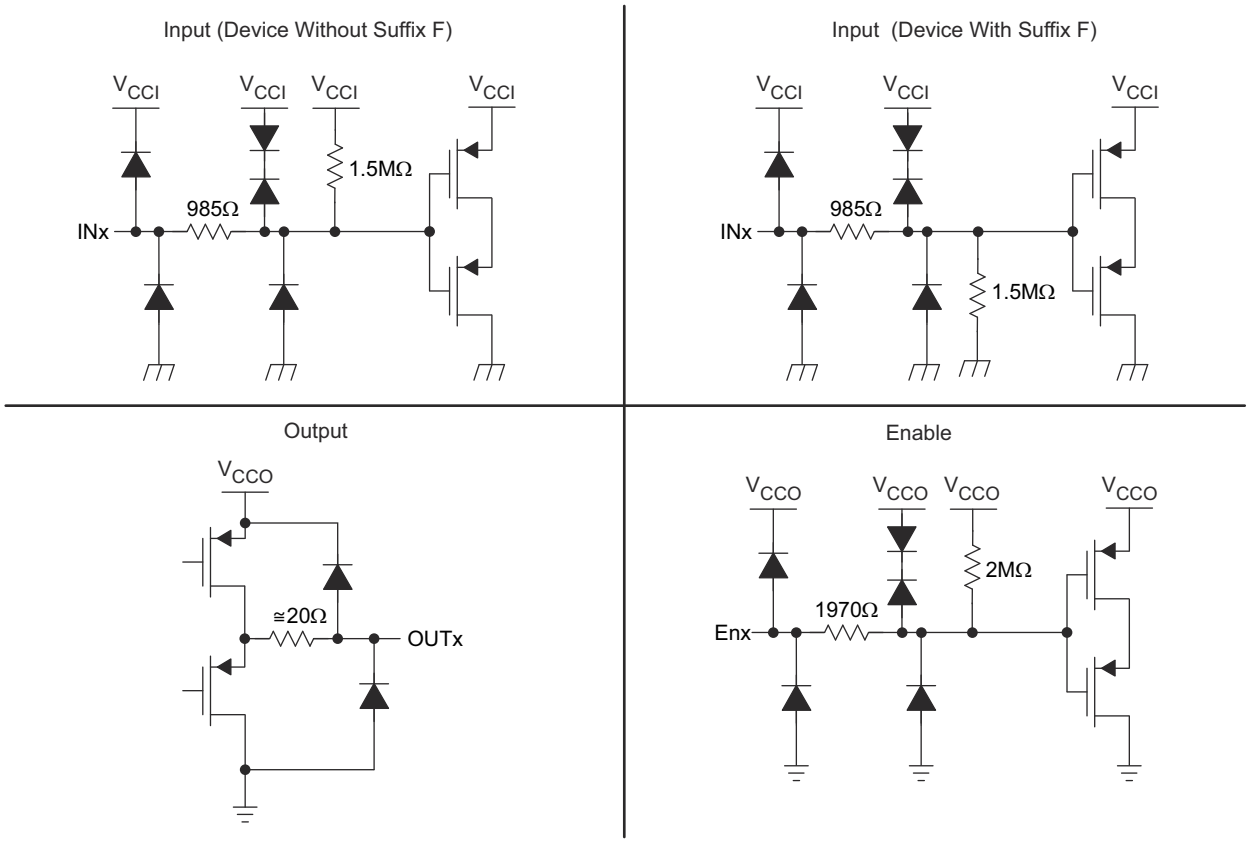

図 7-3. Device I/O Schematics

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO7821 is a high-performance, dual-channel digital isolator with 5.7 kV_{RMS} isolation voltage per UL 1577. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. Keep in mind that when designing with digital isolators, due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

ISO782 1 can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop .

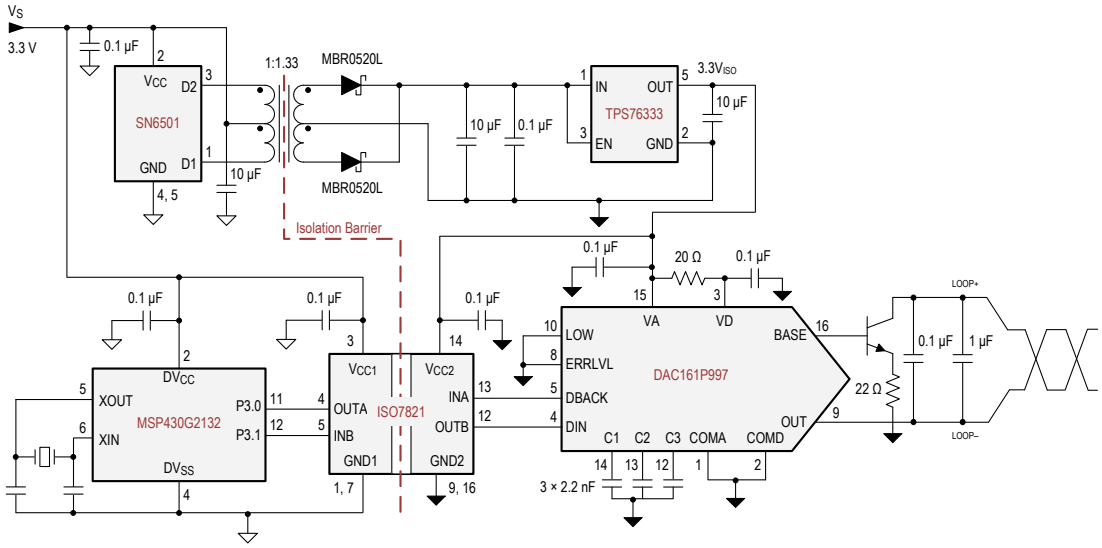

図 8-1. Isolated 4-20 mA Current Loop

8.2.1 Design Requirements

For the ISO7821, use the parameters shown in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO7821 only needs two external bypass capacitors to operate.

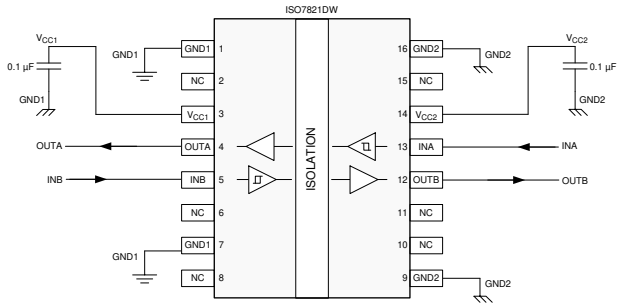

図 8-2. Typical ISO7821 Circuit Hook-up

8.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7821 incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

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8.2.3 Application Performance Curve

Typical eye diagram of ISO7821 indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

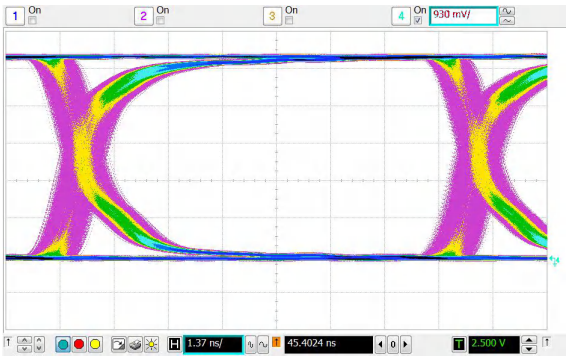

図 8-3. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

8.3 Power Supply Recommendations

To provide reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

8.4 Layout

8.4.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 8-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

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8.4.3 Layout Example

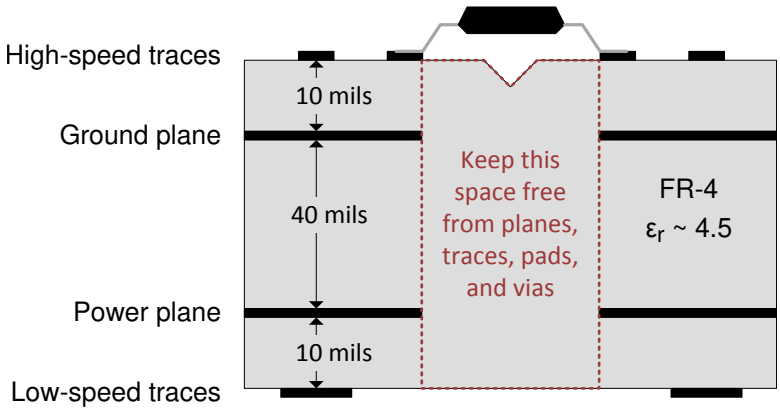

図 8-4. Layout Example

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9 Device and Documentation Support

9.1 Related Documentation

9.1.1 Related Documentation

See the *Isolation Glossary* (SLLA353)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (July 2022) to Revision H (November 2024)	Page
•	1
• Added content from the *High Voltage Feature Description* section to the *Specifications* section	4
• Moved the *IEC 60664-1 Ratings* table to the *Power Ratings* section in the *Specifications*	8
• Added typical specification to CPG/CLR in the *Insulation Specifications* section	8
• Moved the *Insulation Characteristics* table to the *Insulation Specifications* section	8
• Moved the *Package Insulation and Safety-Related Specification* table to the *Insulation Specifications* section	8
• Changed the *Regulatory Information Section* to the *Safety-related Certifications* section and moved to the *Specifications* section	11
• Moved the *Safety Limiting Values* to the *Specifications* section	12

Changes from Revision F (March 2016) to Revision G (July 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新。	1

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Changes from Revision E (December 2015) to Revision F (March 2016) **Page**

- セクション 1 の安全および規制の認定リストを変更 1
- セクション 1 に「EN 61010-1 および EN 60950-1 準拠の TUV 認証」を追加 1
- 「*セクション 3*」セクションの 3 番目の段落でテキストを次のように変更:「VDE、CSA、CQC に準拠した認証」から「VDE、CSA、CQC、TUV に準拠した認証」に変更。 1
- Added Note 1 to 表 5-2 8
- Added TUV to the *セクション 5.11* section and 表 5-4. Deleted Note 1 in Table 4 11
- Changed 図 7-3 20

Changes from Revision D (July 2015) to Revision E (December 2015) **Page**

- セクション 1 を以下のように変更:「8000V_{PK} V_{IOTM} および 2121V_{PK} V_{IORM} 強化...」を「8000V_{PK} の強化...」に変更. 1
- セクション 1 に「DW パッケージの認証は完了、DWW 認証は計画中」を追加 1
- 「概要」に次の記述を追加:「および超幅広 (DWW) パッケージ...」 1
- パッケージを追加:「 *製品情報*」表に超幅広 SOIC、DWW (16) を追加 1
- Added the DWW pinout image 3
- Added the DWW package to the *セクション 5.4* 5
- Changed the MIN value of CMTI in *セクション 5.6* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 6
- Added the DW package value to the Supply Current section of the *セクション 5.6* 6
- Added the DWW package value to the Supply Current section of the *セクション 5.6* 6
- Changed the MIN value of CMTI in *セクション 5.7* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 7
- Added the DW package value to the Supply Current section of the *セクション 5.7* 7
- Added the DWW package value to the Supply Current section of the *セクション 5.7* 7
- Changed the MIN value of CMTI in *セクション 5.8* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 8
- Added the DW package value to the Supply Current section of the *セクション 5.8* 8
- Added the DWW package value to the Supply Current section of the *セクション 5.8* 8
- Changed Parameter information and added the DWW package information in 表 5-1 8
- Added the DWW package to 表 5-3 8
- Changed C_{IO} typ value From: 2 To 1 pF in 表 5-3 8
- Added the DWW package to 表 5-2 8
- Added the DWW package information to 表 5-4 11
- added DWW-16 package options to 表 5-5 12
- Added t_{PHZ}, t_{PLZ}, t_{PZH}, and t_{PZL} to *セクション 5.14* 13
- Added t_{PHZ}, t_{PLZ}, t_{PZH}, and t_{PZL} to *セクション 5.15* 14
- Added 図 6-2 16
- Changed 表 7-1 20
- Added text to the *セクション 8.1* section: "isolation voltage per UL 1577." 21

Changes from Revision C (May 2015) to Revision D (July 2015) **Page**

- ISO7821F デバイスをデータシートに追加 1
- *セクション 3* を次の記述を含むように変更:「デフォルト出力は、ISO7821 デバイスでは「HIGH」、ISO7821F デバイスでは「LOW」です。」 1
- 概略回路図を変更 1
- Changed 表 5-3 title From: *IEC Insulation and Safety-Related Specifications for DW-16 Package* To: *Package Insulation and Safety-Related Specifications* 8

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- Changed 図 5-1, Added 図 5-2 12
- Changed t_{PLH} and t_{PHL} From: 5.5 V to 5 V in 図 5-8 15
- Changed 図 6-3 16
- Changed the *セクション 7.2* 18

Changes from Revision B (April 2015) to Revision C (May 2015) **Page**

- 以下のように変更:「V_{CC1} および V_{CC2}」から「V_{CCI} および V_{CCO}」に変更。「GND1 および GND2」から「GNDI および GNDO」に変更。*概略回路図* に注 1 および 2 を追加。..... 1
- Changed the MIN value of CMTI in *セクション 5.6* table From: 50 To: 70 kV/μs 6
- Changed the MIN value of CMTI in *セクション 5.7* table From: 50 To: 70 kV/μs 7
- Changed the MIN value of CMTI in *セクション 5.8* table From: 50 To: 70 kV/μs 8
- Changed the Installation classification of the 表 5-1 to include DW package information..... 8
- Added sentence "If the EN pin is available and low then the output goes to high impedance." to the *セクション 7.1* section 18
- Changed the *セクション 7.2* to include the EN pin on the Receiver side..... 18
- Changed "ISO782W functional modes" To: "ISO7821DW functional modes" in *セクション 7.4* 20
- Changed 表 7-1 title From: "Functional Table" To: "ISO7821DW Function Table"..... 20
- Added the *セクション 7.4.1* section 20
- Changed device number ISO7821 To: ISO7821DW in 図 8-2 22

Changes from Revision A (December 2014) to Revision B (April 2015) **Page**

- ドキュメントのタイトルを「チャネル デジタル アイソレータ」から「チャネル 1/1 デジタル アイソレータ」に変更..... 1
- セクション 1 を追加: 2.25V から 5.5V への電圧変換..... 1
- セクション 1 の安全および規制の認定リストを変更..... 1
- *セクション 3* のテキストを「このデバイスは、VDE および CSA による強化絶縁認証について審査中です。」から「このデバイスは VDE、CSA、CQC に準拠した強化絶縁認証を受けています。」に変更。..... 1
- Added Note (3) to the *セクション 5.1* table..... 4
- Changed From: V_{CCX} To: V_{CCO} In I_{OH} and I_{OL} of the *セクション 5.3* table 4
- Changed From: V_{CCX} To: V_{CCI} In V_{IH} and V_{IL} of the *セクション 5.3* table 4
- Changed Note (1) of the *セクション 5.3* table 4
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *セクション 5.6* table 6
- Changed From: V_{CCX} To: V_{CCO} In $V_{I(HYS)}$ of the *セクション 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *セクション 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In CMTI of the *セクション 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *セクション 5.6* table..... 6
- Changed Note (1) of the *セクション 5.6* table 6
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *セクション 5.7* table 7
- Changed From: V_{CCX} To: V_{CCO} In $V_{I(HYS)}$ of the *セクション 5.7* table 7
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *セクション 5.7* table..... 7
- Changed From: V_{CCX} To: V_{CCI} In CMTI of the *セクション 5.7* table 7
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *セクション 5.7* table 7
- Changed Note (1) of the *セクション 5.7* table 7
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *セクション 5.8* table 8
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *セクション 5.8* table 8
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *セクション 5.8* table 8
- Changed Note (1) of the *セクション 5.8* table 8

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- Changed the Test Condition of CTI in 表 5-3 8
- Changed the MIN value of CTI From" > 600 V To: 600 V.... 8
- Changed 表 5-2 title From: *DIN V VDE 0884-10 (VDE V 0884-10) and UL 1577 Insulation Characteristics* To: *Added the DWW package to* 8
- Changed 表 5-2 8
- Changed columns VDE and CSA to 表 5-4 11
- Changed title From: *IEC Safety Limiting Values* To: *セクション 5.12* 12
- Changed the table in *セクション 5.12*, added I_S DW-16 package options....12
- Changed 図 5-1 12
- Changed 図 6-1 16
- Changed From: V_{CC1} To: V_{CCI} in 図 6-3 16
- Changed 図 6-4 16
- Deleted INPUT-SIDE and OUTPUT-SIDE from columns 1 and 2 of 表 7-1 20
- Changed Note (1) of 表 7-1 20
- Changed the *セクション 8.1* section....21
- Changed the *セクション 8.2* section and 図 8-1 21
- Added text and 図 8-2 to the *セクション 8.2.2* section 22

Changes from Revision * (November 2014) to Revision A (December 2014) **Page**

- 以下のように変更：最初のページおよびピン配置セクションだけを記載した製品プレビューから完全なデータシートに変更.... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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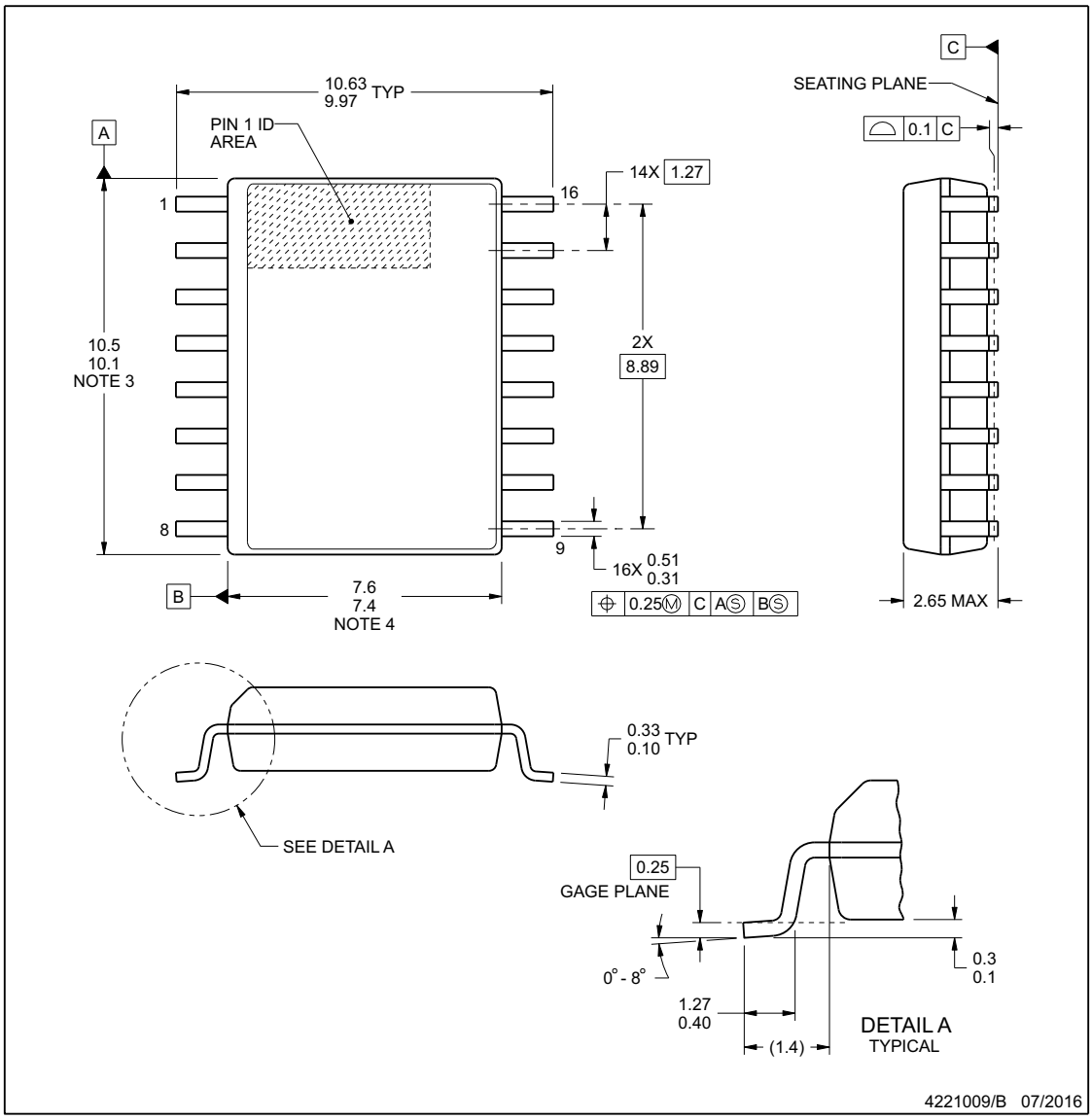
PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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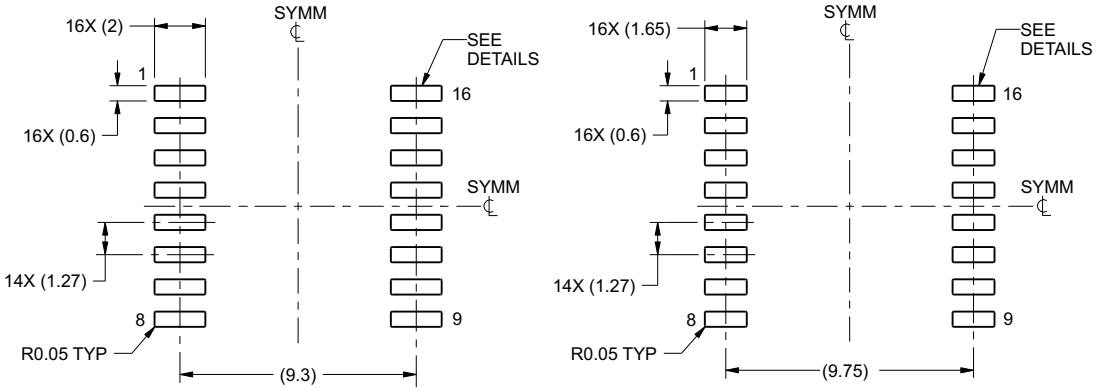
EXAMPLE BOARD LAYOUT

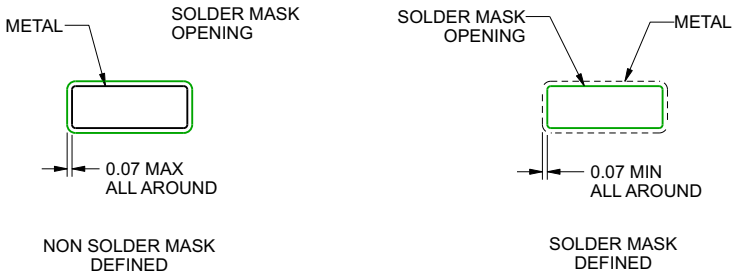
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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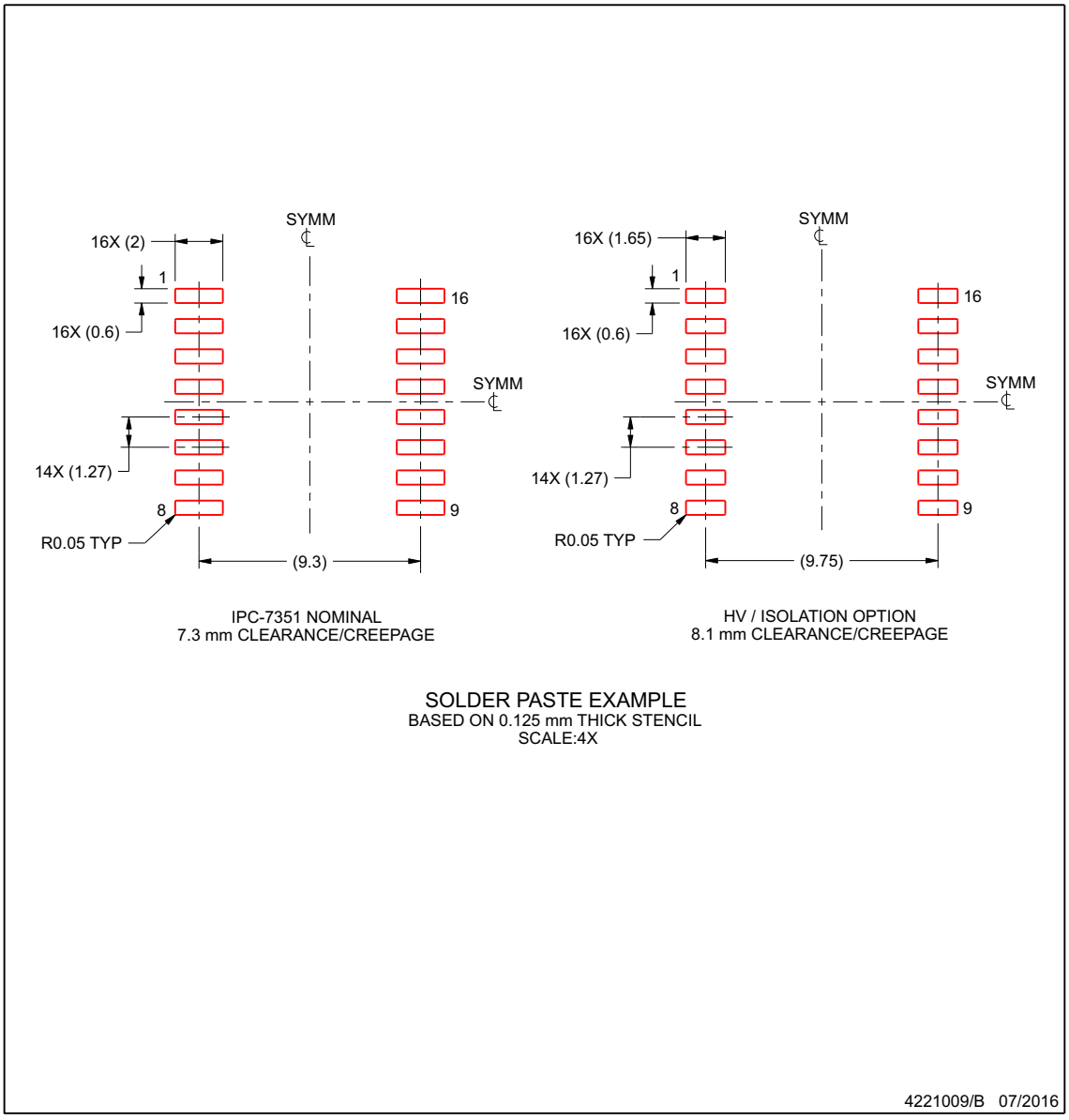
EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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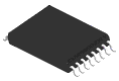
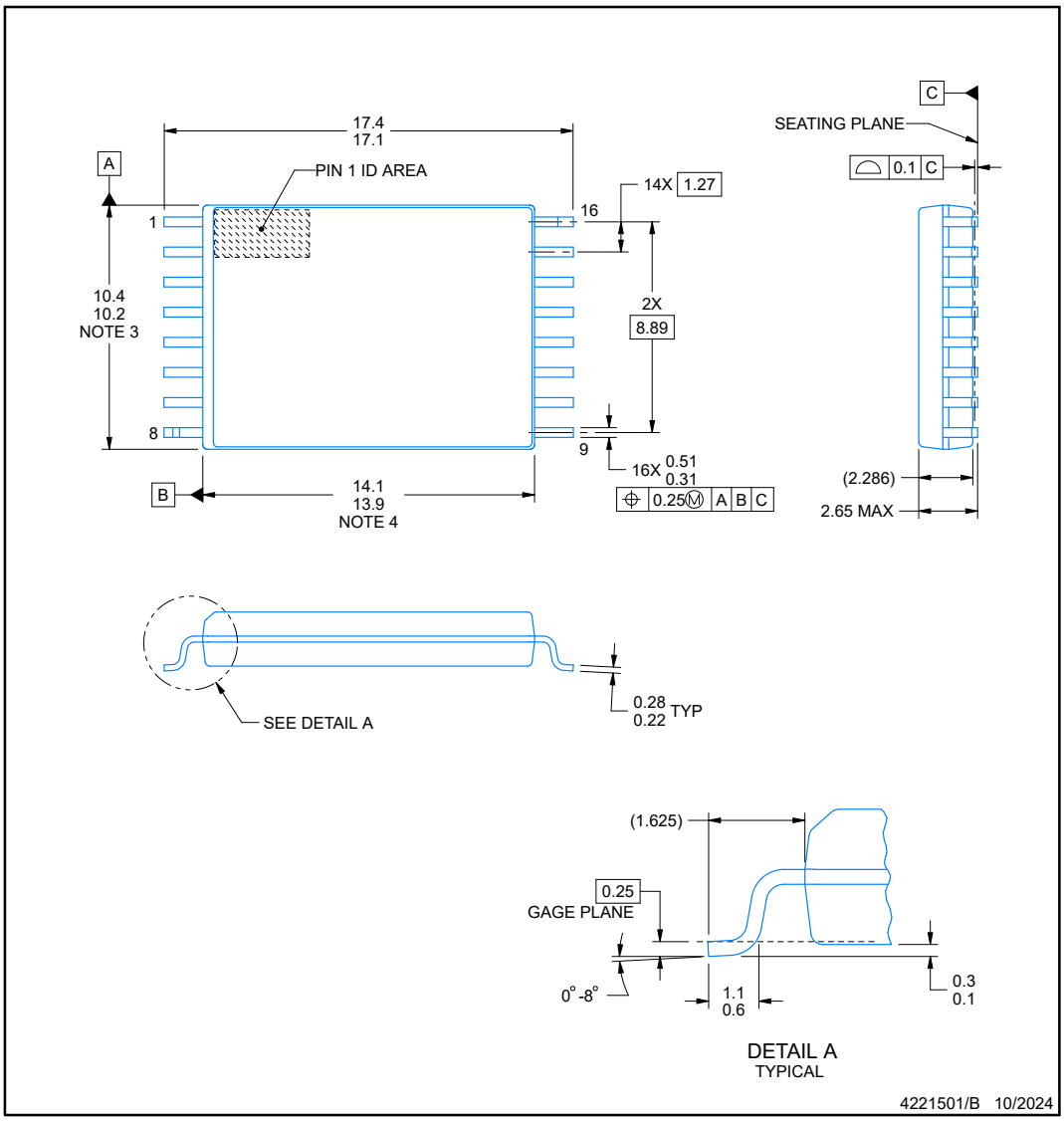


PACKAGE OUTLINE

DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

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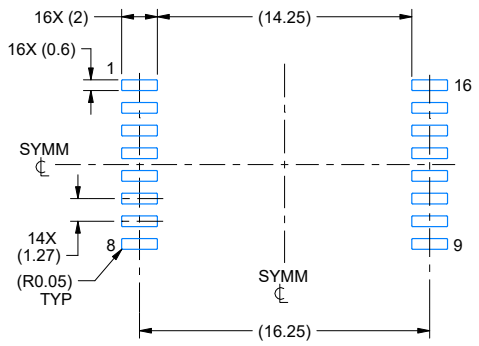
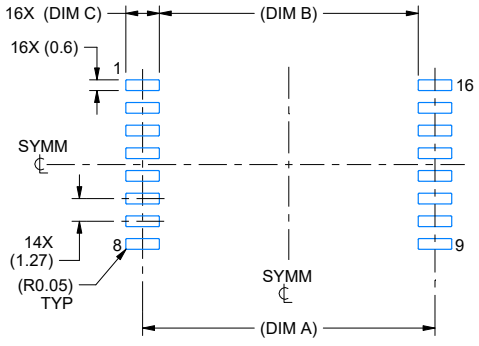
EXAMPLE BOARD LAYOUT

DWW0016A — **SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE

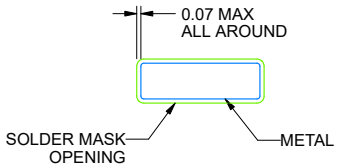


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

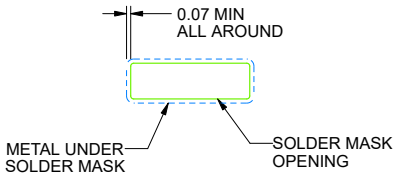


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/B 10/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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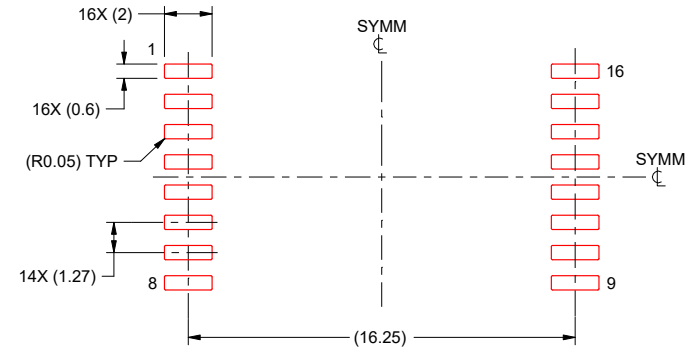
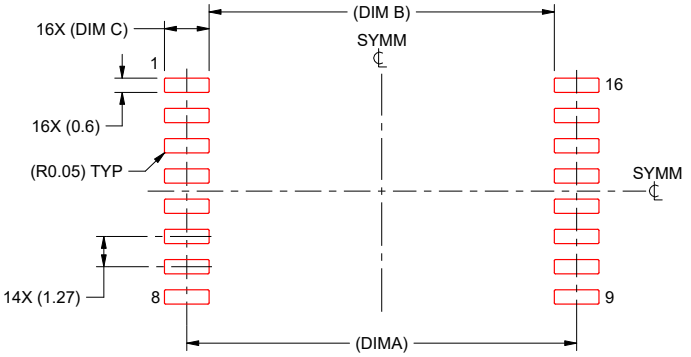
EXAMPLE STENCIL DESIGN

DWW0016A — **SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7821DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821	Samples
ISO7821DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821	Samples
ISO7821DWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821	Samples
ISO7821DWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821	Samples
ISO7821FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F	Samples
ISO7821FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F	Samples
ISO7821FDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F	Samples
ISO7821FDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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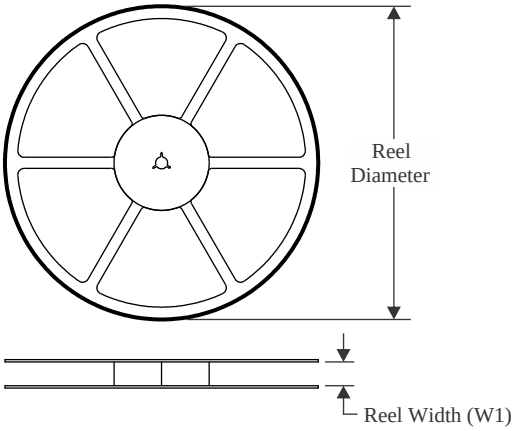
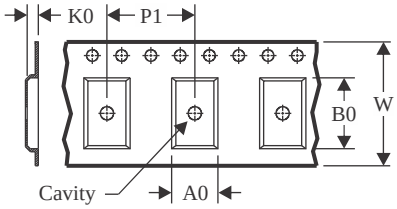
TAPE AND REEL INFORMATION

REEL DIMENSIONS

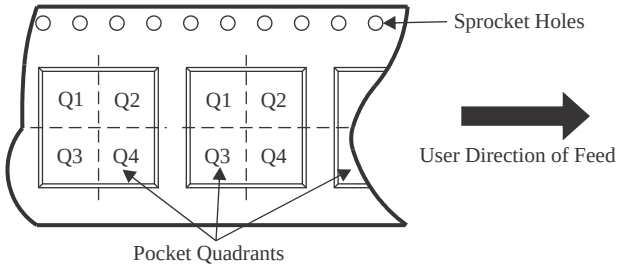


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

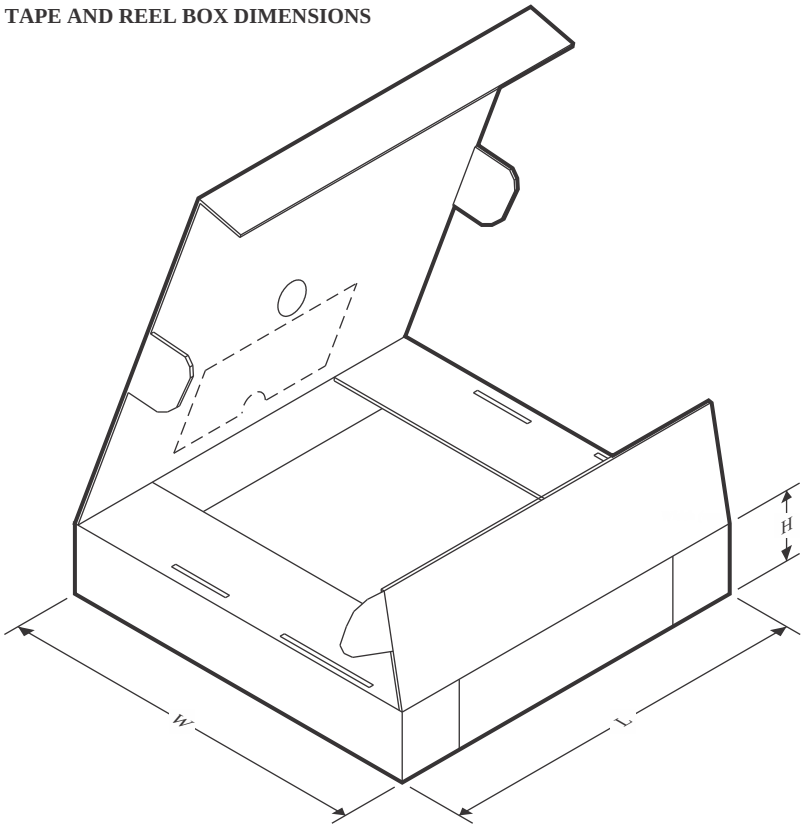
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7821DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7821FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

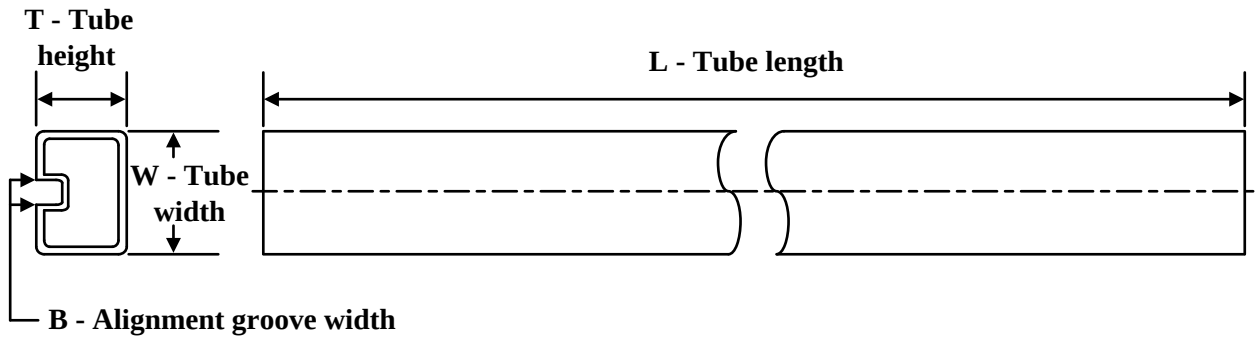
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7821DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7821FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7821DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7821FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821FDWW	DWW	SOIC	16	45	507	20	5000	9

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