ISO7841x 高性能 8000V_{PK} 強化絶縁型クワッド チャネル デジタル アイソレータ

1 特長

- 信号速度:最大 100Mbps
- 広い電源電圧範囲:2.25V～5.5V
- 2.25V から 5.5V への電圧変換
- 広い温度範囲:-55℃～125℃
- 低い消費電力:1Mbps でチャネルごとに標準値 1.7mA
- 小さい伝搬遅延時間:標準値 11ns (5V 電源)
- 業界をリードする CMTI (最小値): ±100kV/μs
- 堅牢な電磁環境適合性 (EMC)
- システム レベルでの ESD、EFT、サージ耐性
- 低い放射
- 絶縁バリアの寿命:40 年超
- ワイド ボディ SOIC-16 パッケージまたは超ワイド ボディ SOIC-16 パッケージを選択可能
- 安全および規制の認定:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:8000V_{PK}
  - UL 1577 に準拠した絶縁耐圧:5.7kV_{RMS} (1 分間)
  - CSA Component Acceptance Notice 5A、IEC 60950-1、および IEC 60601-1 最終機器標準
  - GB4943.1 準拠の CQC 認定
  - EN 61010-1 および EN 62368-1 準拠の TUV 認定

2 アプリケーション

- 産業用オートメーション
- モータ制御
- 電源
- ソーラー インバータ
- 医療機器
- ハイブリッド電気自動車 (HEV)

3 概要

ISO7841x デバイスは、8000V_{PK} の絶縁電圧を持つ高性能クワッド チャネル デジタル アイソレータです。このデバイスは、VDE、CSA、TUV、CQC に準拠した強化絶縁認証を取得しています。本アイソレータは、CMOS や LVCMOS のデジタル I/O を絶縁しながら、低消費電力で高い電磁気耐性と低い放射を実現します。各絶縁チャネルは、二酸化ケイ素 (SiO_2) の絶縁バリアで分離されたロジック入力および出力バッファを備えています。

このデバイスは複数のイネーブル ピンを備えています。これらのイネーブル ピンを使うと、マルチコントローラ駆動アプリケーションにおいて、各出力を高インピーダンス状態にすることで、消費電力を低減できます。ISO7841 デバイスには、3 個の順方向チャネルと 1 個の逆方向チャネルがあります。入力電源または信号が失われた場合のデフォルト出力は、ISO7841 デバイスでは「High」、ISO7841F バイスでは「Low」です。詳細については、「デバイスの機能モード」セクションを参照してください。

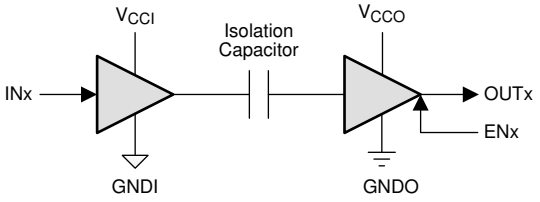
このデバイスを絶縁型電源と組み合わせて使用すると、データ バスや他の回路上のノイズ電流がローカル グランドに入り込んでノイズに敏感な回路に干渉または損傷を与えることを、防止できます。革新的なチップ設計およびレイアウト技法により、ISO7841 デバイスは電磁両立性が大幅に強化されているため、システム レベルの ESD、EFT、サージ、放射のコンプライアンスを容易に達成できます。

ISO7841 デバイスは、16 ピン SOIC ワイド ボディ (DW) および超ワイド ボディ (DWW) パッケージで供給されます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (公称)
ISO7841 ISO7841F	DW (16)	10.30mm × 10.30mm	10.30mm × 7.50mm
	DWW (16)	10.30mm × 17.25mm	10.30mm × 14.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{CCI} および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。
V_{CCO} および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

Pin Functions

PIN		Type(1)	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

(1) I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)		–0.5	6	V
	Voltage	INx	–0.5	V_{CCX} + 0.5(3)	V
		OUTx	–0.5	V_{CCX} + 0.5(3)	
		ENx	–0.5	V_{CCX} + 0.5(3)	
I_O	Output current		–15	15	mA
	Surge immunity			12.8	kV
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO} (2) = 5V	-4			mA
		V_{CCO} (2) = 3.3V	-2			
		V_{CCO} (2) = 2.5V	-1			
I_{OL}	Low-level output current	V_{CCO} (2) = 5V		4		mA
		V_{CCO} (2) = 3.3V		2		
		V_{CCO} (2) = 2.5V		1		
V_{IH}	High-level input voltage		0.7 × V_{CCI} (2)		V_{CCI} (2)	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI} (2)	V
DR	Signaling Rate		0		100	Mbps
T_J	Junction temperature(1)		-55		150	°C
T_A	Ambient temperature		-55	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see *セクション 5.4*.
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.4 Thermal Information

THERMAL METRIC(1)		ISO7841		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	49.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.5	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.1	48.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, input a 50MHz 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation by ISO7841x				200	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7841x				75	mW
P_{D2}	Maximum power dissipation by side-2 of ISO7841x				125	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
GENERAL					
CLR	External clearance(1)	Shortest pin-to-pin distance through air	>8	>14.5	mm
		Shortest pin-to-pin distance through air (typical)		15.0	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	>8	>14.5	mm
		Shortest pin-to-pin distance across the package surface (typical)		15.0	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 1000V_{RMS}	I–III	I–IV	
DIN EN IEC 60747-17 (VDE 0884-17)(2)					
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) Test, see 図 5-1 and 図 5-2	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = 1.2 × V_{IOTM} t = 60s (qualification) t= 1s (100% production)	8000	8000	V_{PK}
V_{IMP}	Maximum impulse voltage (3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	9800	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	V_{IOSM} ≥ 1.3 x V_{IMP}; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	12800	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IOTM} = 2545V_{PK} (DW) and 3394V_{PK} (DWW), t_m = 10s	≤5	≤5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 3394V_{PK} (DW) and 4525V_{PK} (DWW), t_m = 10s	≤5	≤5	
		Method b: At routine test (100% production); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	2	2	pF
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, T_A = 25°C	>10^{12}	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	>10^{11}	
		V_{IO} = 500V at T_S = 150°C	>10^9	>10^9	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700V_{RMS}, t = 60s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840V_{RMS}, t = 1s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the

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isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package.

(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Reinforced insulation Maximum transient isolation voltage, 8000V_{PK}; Maximum repetitive peak isolation voltage, 2121V_{PK} (DW), 2828V_{PK} (DWW); Maximum surge isolation voltage, 12800V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800V_{RMS} (DW) and 1450V_{RMS} (DWW) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250V_{RMS} (DW) and 400V_{RMS} (DWW) max working voltage	Single protection, 5700V_{RMS}	Reinforced Insulation, Altitude ≤ 5000m, Tropical Climate, 700V_{RMS} (DW) and 1450V_{RMS} (DWW) maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1 up to working voltage of 600V_{RMS} (DW) and 1000V_{RMS} (DWW); 5700V_{RMS} Reinforced insulation per EN 62368-1 up to working voltage of 800V_{RMS} (DW) and 1450V_{RMS} (DWW)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

5.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.9°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			288	mA
		$R_{\theta JA}$ = 78.9°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			440	
		$R_{\theta JA}$ = 78.9°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			576	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 78.9°C/W, T_J = 150°C, T_A = 25°C			1584	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *セクション 5.4* is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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5.9 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see 図 6-4	100			kV/µs
C_I	Input capacitance	V_I = V_{CC}/2 + 0.4 × sin (2πft), f = 1MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.10 Supply Current Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.1	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5	7.3	mA
			I_{CC2}		3.4	4.9	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.3	4.9	mA
			I_{CC2}		2.9	4.2	
		10Mbps	I_{CC1}		3.9	5.5	mA
			I_{CC2}		4.4	5.7	
		100Mbps	I_{CC1}		9.2	11.6	mA
			I_{CC2}		19	21.9	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.3	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5	7.5	mA
			I_{CC2}		3.4	5.2	
	All channels switching with square wave clock input;C_L = 15pF	1Mbps	I_{CC1}		3.4	5	mA
			I_{CC2}		3	4.4	
		10Mbps	I_{CC1}		4	5.6	mA
			I_{CC2}		4.5	6.1	
		100Mbps	I_{CC1}		9.4	12.1	mA
			I_{CC2}		19.5	22.6	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.11 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or ENx	-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see 図 6-4	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.12 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		1.9	2.9	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.1	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5	7.3	mA
			I_{CC2}		3.3	4.9	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.3	4.9	mA
			I_{CC2}		2.8	4.1	
		10Mbps	I_{CC1}		3.7	5.3	mA
			I_{CC2}		3.9	5.2	
		100Mbps	I_{CC1}		7.4	9.3	mA
			I_{CC2}		14.5	16.9	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.3	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5	7.5	mA
			I_{CC2}		3.4	5.2	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.4	5	mA
			I_{CC2}		2.9	4.4	
		10Mbps	I_{CC1}		3.8	5.4	mA
			I_{CC2}		4	5.5	
		100Mbps	I_{CC1}		7.5	9.9	mA
			I_{CC2}		14.8	17.2	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.13 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA; see 図 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; see 図 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see 図 6-4	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.14 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.7	mA
			I_{CC2}		0.8	1.2	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.5	mA
			I_{CC2}		1.9	2.8	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.6	2.3	mA
			I_{CC2}		2.2	3.1	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5.1	7.2	mA
			I_{CC2}		3.5	4.8	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.4	4.8	mA
			I_{CC2}		2.9	4	
		10Mbps	I_{CC1}		3.7	5.1	mA
			I_{CC2}		3.7	4.8	
		100Mbps	I_{CC1}		6.8	8.1	mA
			I_{CC2}		12	14.2	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0V, V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.1	1.7	mA
			I_{CC2}		0.8	1.2	
		EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		4.5	6.5	mA
			I_{CC2}		1.9	2.8	
	DC signal	V_I = 0V (ISO7841F), V_I = V_{CCI} (1) (ISO7841)	I_{CC1}		1.6	2.4	mA
			I_{CC2}		2.2	3.3	
		V_I = V_{CCI} (1) (ISO7841F), V_I = 0V (ISO7841)	I_{CC1}		5.1	7.5	mA
			I_{CC2}		3.5	5.2	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.5	5	mA
			I_{CC2}		3	4.3	
		10Mbps	I_{CC1}		3.8	5.3	mA
			I_{CC2}		3.8	5.2	
		100Mbps	I_{CC1}		6.9	8.8	mA
			I_{CC2}		12.3	14.2	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.15 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.55	4.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 図 6-1		1.7	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.16 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	6	10.8	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See 図 6-1		0.8	3	ns
t_f	Output signal fall time			0.8	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

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5.17 Switching Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 6-1	7.5	11.7	17.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.66	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See 図 6-1		1	3.5	ns
t_f	Output signal fall time			1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See 図 6-2		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See 図 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.18 Insulation Characteristics Curves

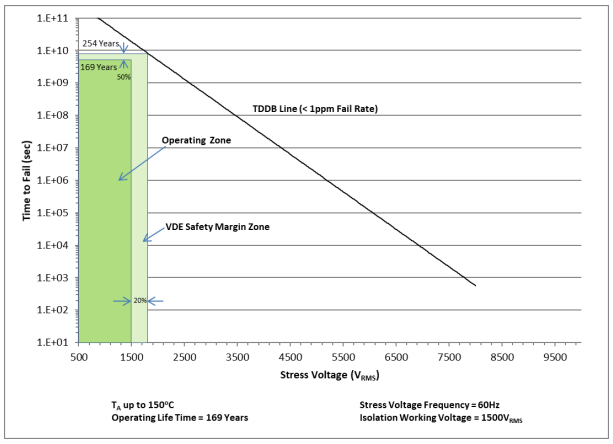

図 5-1. Reinforced Isolation Capacitor Life Time Projection for Devices in DW Package

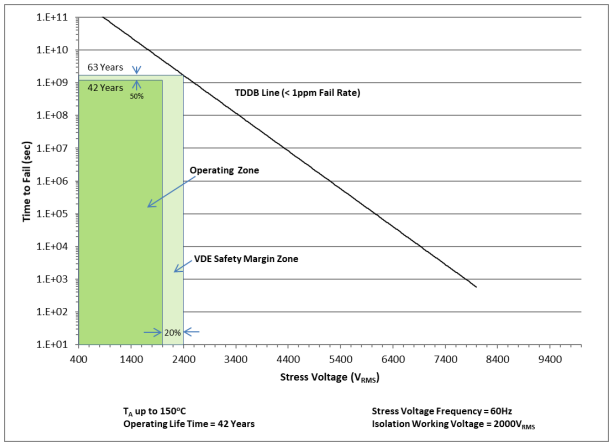

図 5-2. Reinforced Isolation Capacitor Life Time Projection for Devices in DWW Package

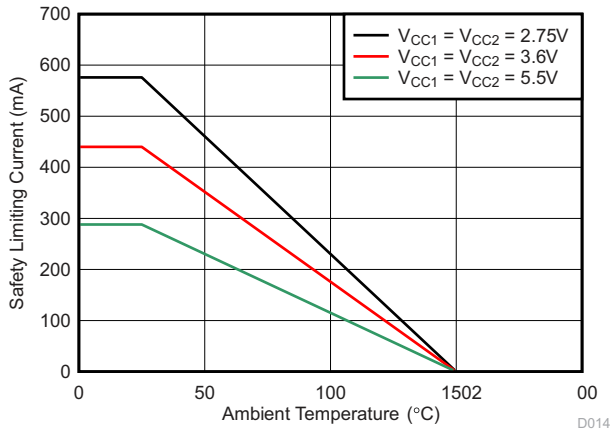

図 5-3. Thermal Derating Curve for Limiting Current per VDE

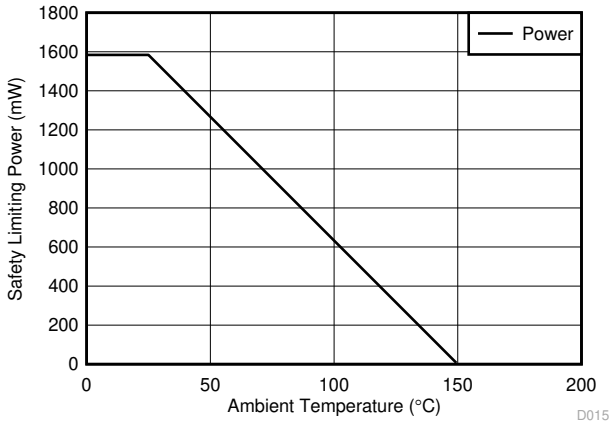

図 5-4. Thermal Derating Curve for Limiting Power per VDE

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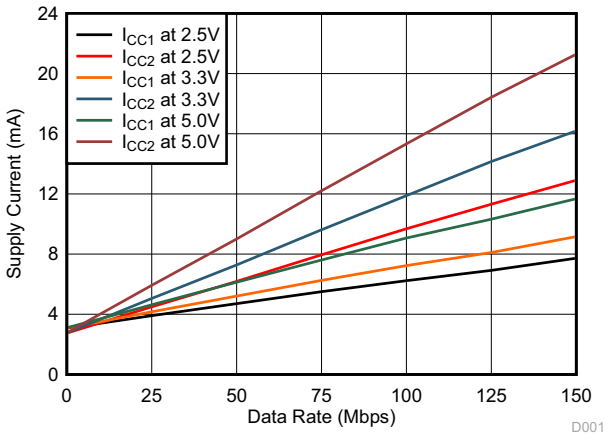
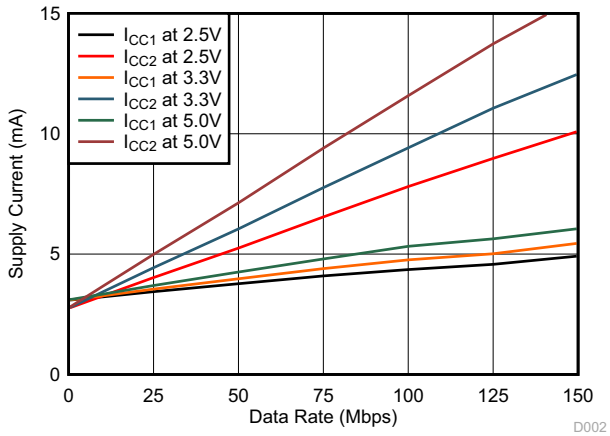
5.19 Typical Characteristics



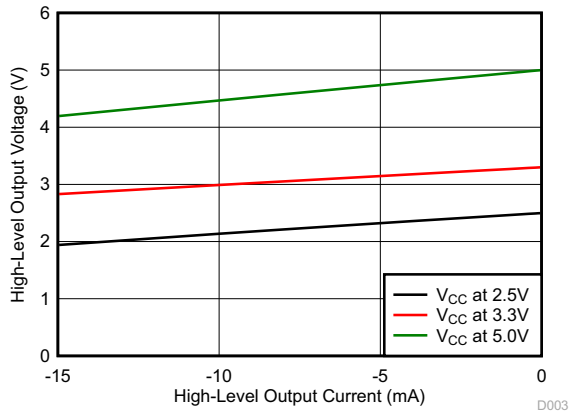
T_A = 25°C C_L = 15pF

図 5-5. Supply Current vs Data Rate (With 15pF Load)



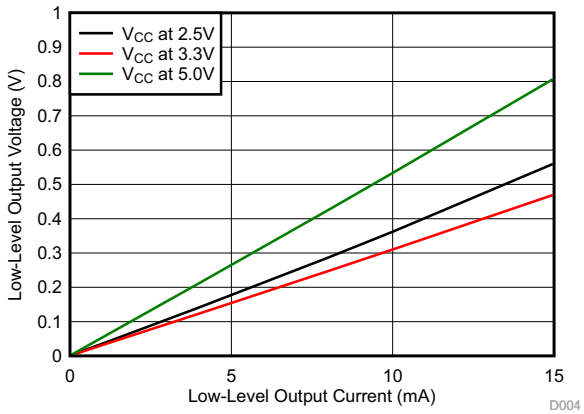
T_A = 25°C C_L = No Load

図 5-6. Supply Current vs Data Rate (With No Load)



T_A = 25°C

図 5-7. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

図 5-8. Low-Level Output Voltage vs Low-Level Output Current

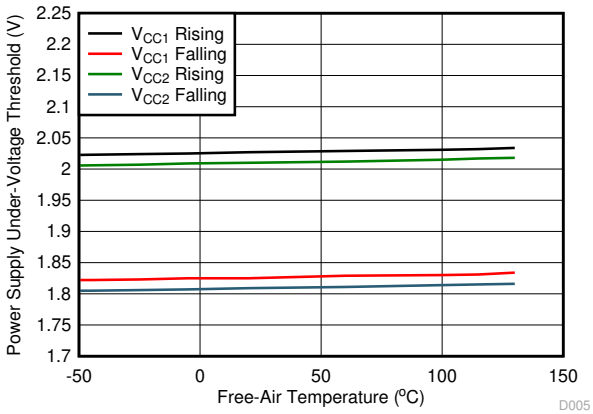


図 5-9. Power Supply Undervoltage Threshold vs Free-Air Temperature

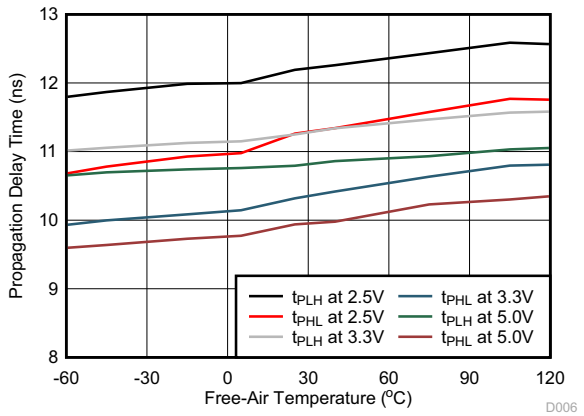


図 5-10. Propagation Delay Time vs Free-Air Temperature

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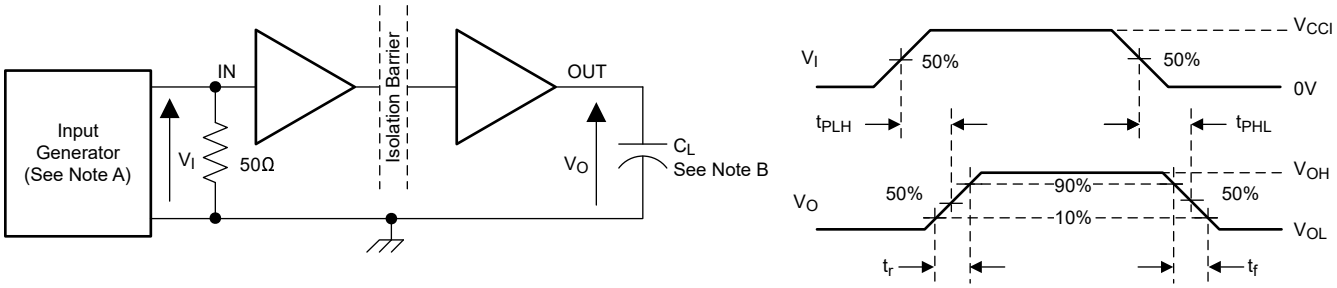
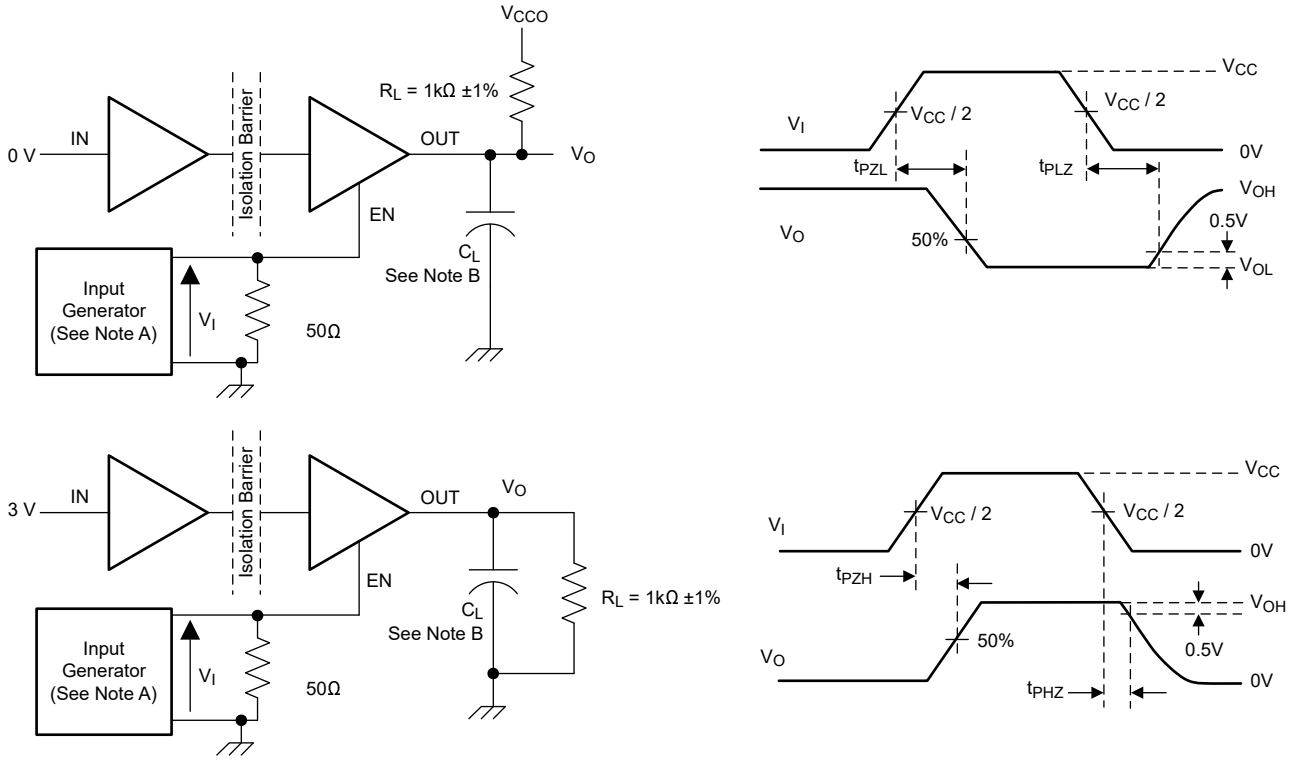
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, a 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 5Ω.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

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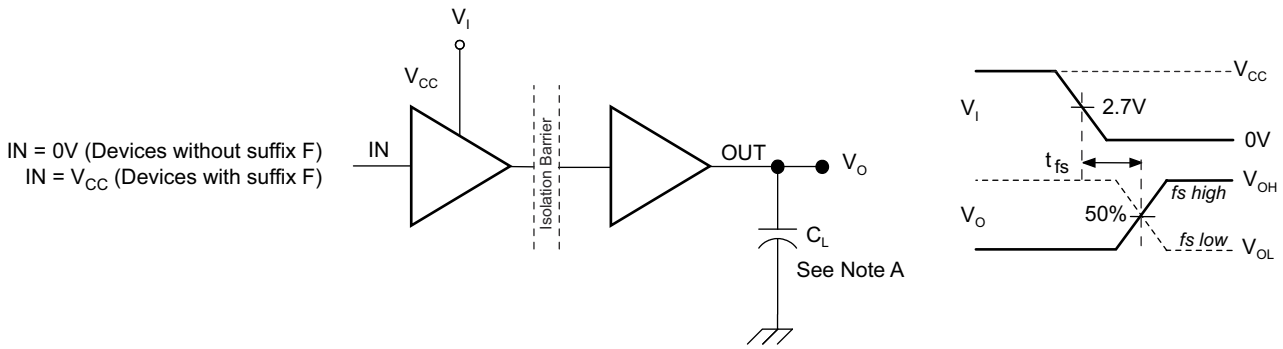
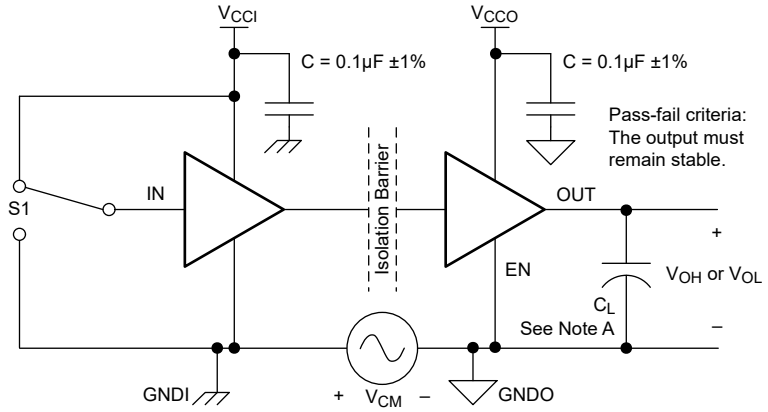


A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO7841 device uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. The ISO7841 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

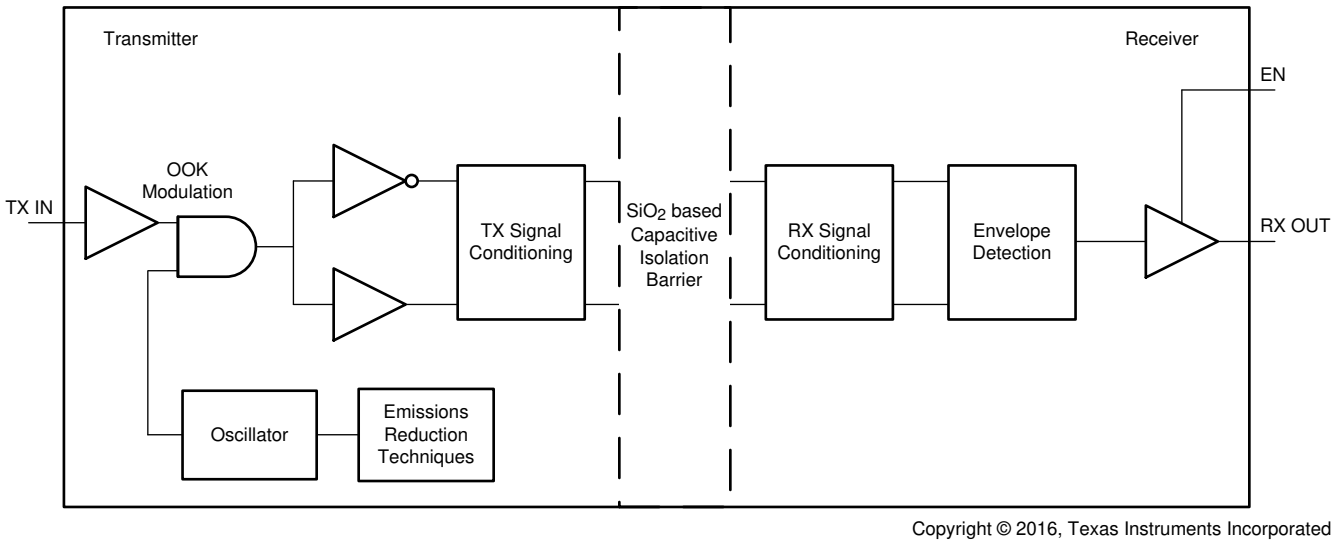


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図 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

図 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

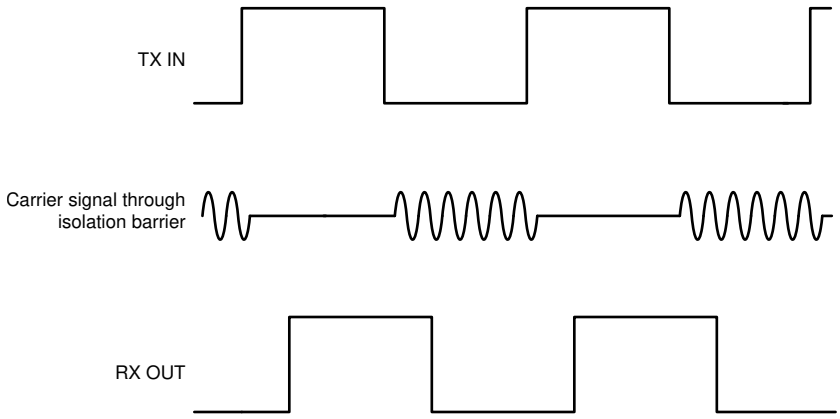

図 7-2. On-Off Keying (OOK) Based Modulation Scheme

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7.3 Feature Description

表 7-1 lists the device features.

表 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7841	3 Forward, 1 Reverse	$5700V_{RMS}$ / $8000V_{PK}$ (1)	100Mbps	High
ISO7841F	3 Forward, 1 Reverse	$5700V_{RMS}$ / $8000V_{PK}$ (1)	100Mbps	Low

(1) See *Insulation Specifications* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge, and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7841 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.4 Device Functional Modes

表 7-2 lists the ISO7841 functional modes.

表 7-2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default= High for ISO7841 and Low for ISO7841F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for IISO7841 and Low for ISO7841F. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (1). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) The outputs are undetermined when 1.7V < V_{CCI}, V_{CCO} < 2.25V.
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

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7.4.1 Device I/O Schematics

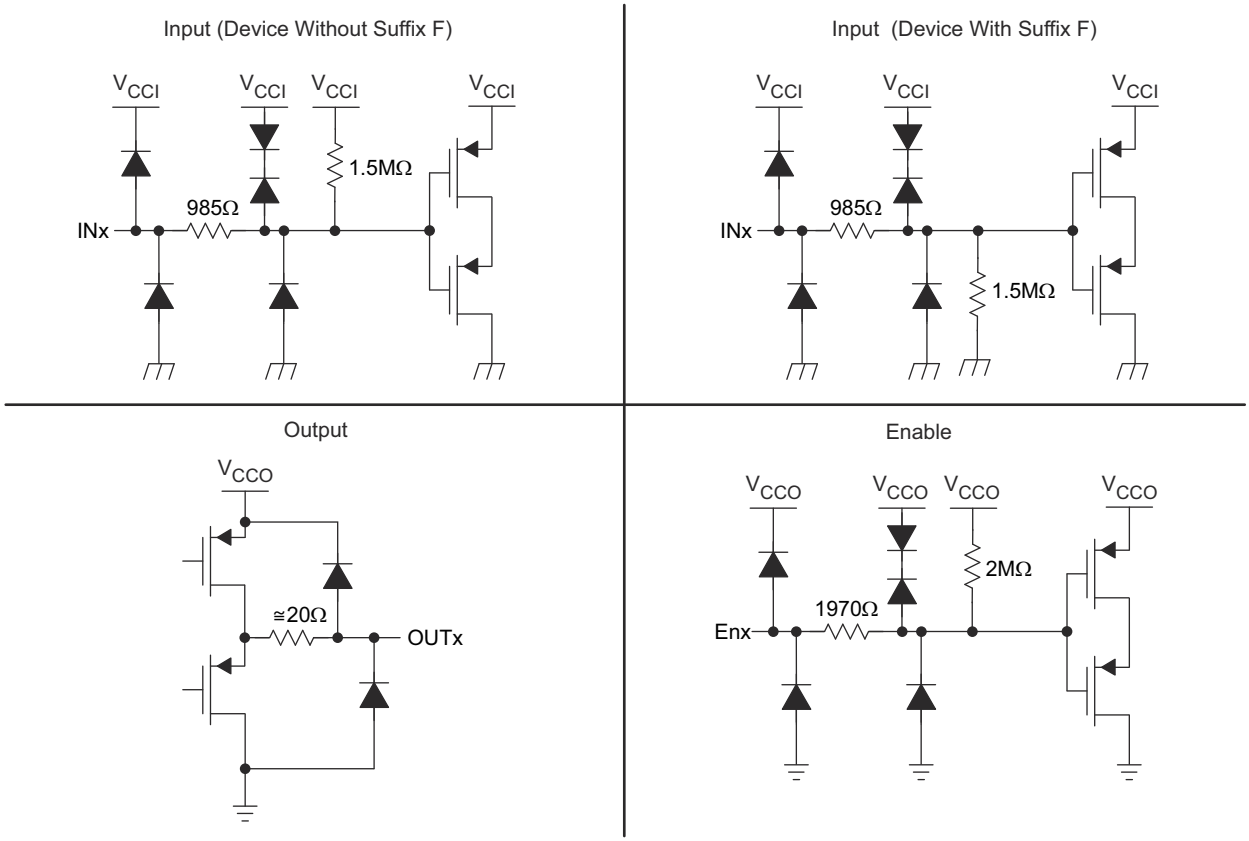

図 7-3. Device I/O Schematics

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO7841 device is a high-performance, quad-channel digital isolator with a 5.7kV$_{RMS}$ isolation voltage per UL 1577. The device comes with enable pins on each side that can be used to put the respective outputs in high impedance for multi-controller driving applications and reduce power consumption. The ISO7841 device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

図 8-1 shows the isolated SPI.

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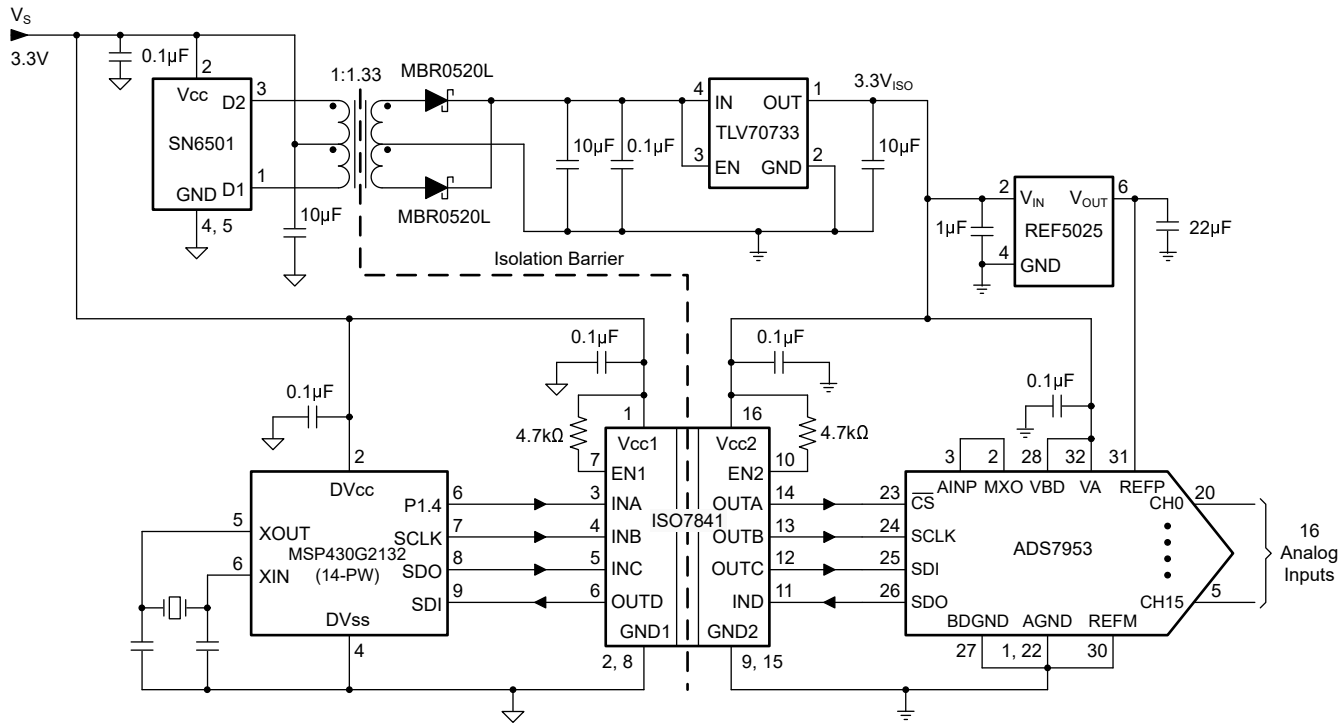

図 8-1. Isolated SPI for an Analog Input Module With 16 Input

8.2.1 Design Requirements

For this design example, use the parameters shown in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7841 device only requires two external bypass capacitors to operate.

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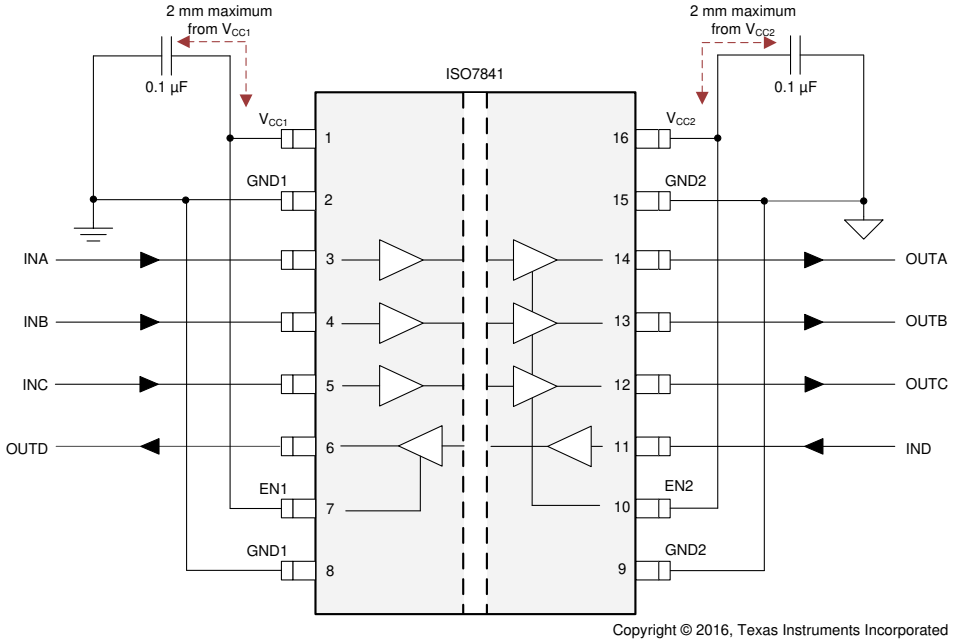

図 8-2. Typical ISO7841 Circuit Hook-Up

8.2.3 Application Curve

The typical eye diagram of the ISO7841 device indicates low jitter and wide open eye at the maximum data rate of 100Mbps.

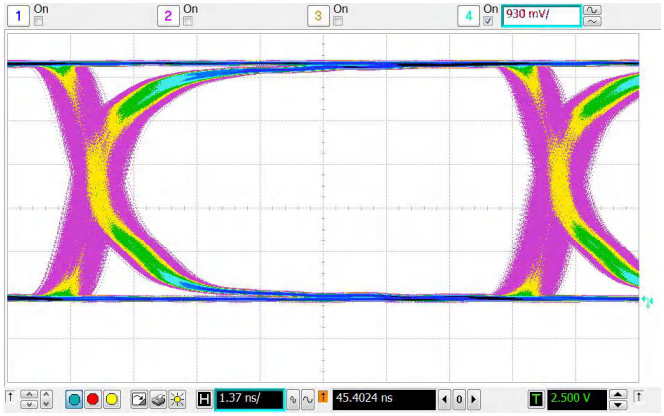

図 8-3. Eye Diagram at 100Mbps PRBS, 5V and 25°C

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 Transformer Driver for Isolated Power Supplies.

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8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 8-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

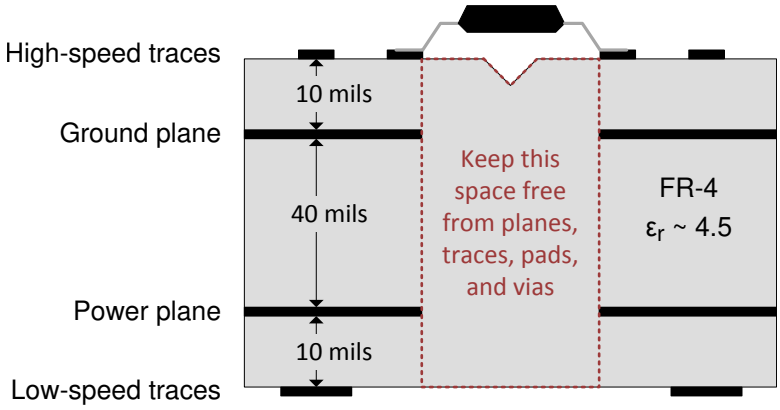

図 8-4. Layout Example Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ADS79xx Pin Compatible, 12-, 10-, 8-Bit, 1-MSPS, 16-, 12-, 8-, 4-Channel, Single-Ended, Serial Interface ADCs*, data sheet
- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *MSP430G2x32, MSP430G2x02 Mixed Signal Microcontrollers*, data sheet
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*, data sheet
- Texas Instruments, *Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*, data sheet

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7841	Click here	Click here	Click here	Click here	Click here
ISO7841F	Click here	Click here	Click here	Click here	Click here

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (November 2014) to Revision I (November 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added 15mm (typ) creepage/clearance to *Insulation Specifications* table ... 5

Changes from Revision G (March 2017) to Revision H (May 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- ドキュメント全体を通して規格名称を「DIN V VDE V 0884-10 (VDE V 0884-10):2006-12」から「DIN EN IEC 60747-17 (VDE 0884-17)」に更新 ... 1
- Added Maximum impulse voltage (V_{IMP}) specification to the *Insulation Specifications* section per DIN EN IEC 60747-17 (VDE 0884-17) ... 5
- Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17) ... 5
- Added clarification to method b test conditions for Apparent charge (q_{PD}) ... 5
- Changed the title of the *Electrical Characteristics—3.3V Supply* section to *Supply Current Characteristics—3.3V Supply* ... 10
- Changed *Reinforced Isolation Capacitor Life Time Projection* for DW and DWW packages per DIN EN IEC 60747-17 (VDE 0884-17) ... 16

Changes from Revision F (April 2016) to Revision G (March 2017) **Page**

- Changed part numbers in the *Power Ratings* table (previously *Power Dissipation Characteristics*) ... 4
- Changed the input-to-output test voltage parameter to apparent charge in the *Insulation Specifications* ... 5
- Added the *Receiving Notification of Documentation Updates* section ... 26

Changes from Revision E (March 2016) to Revision F (April 2016) **Page**

- 「特長」セクションの絶縁バリア寿命の年数を変更 ... 1
- VDE の認証が完了 ... 1
- Changed V_{CCO} to V_{CCI} for the minimum value of the input threshold voltage hysteresis parameter in all electrical characteristics tables ... 7
- Added V_{CM} to the test condition of the common-mode transient immunity parameter in all electrical characteristics tables ... 7
- Added the lifetime projection graphs for DW and DWW packages to the *Safety Limiting Values* section ... 16

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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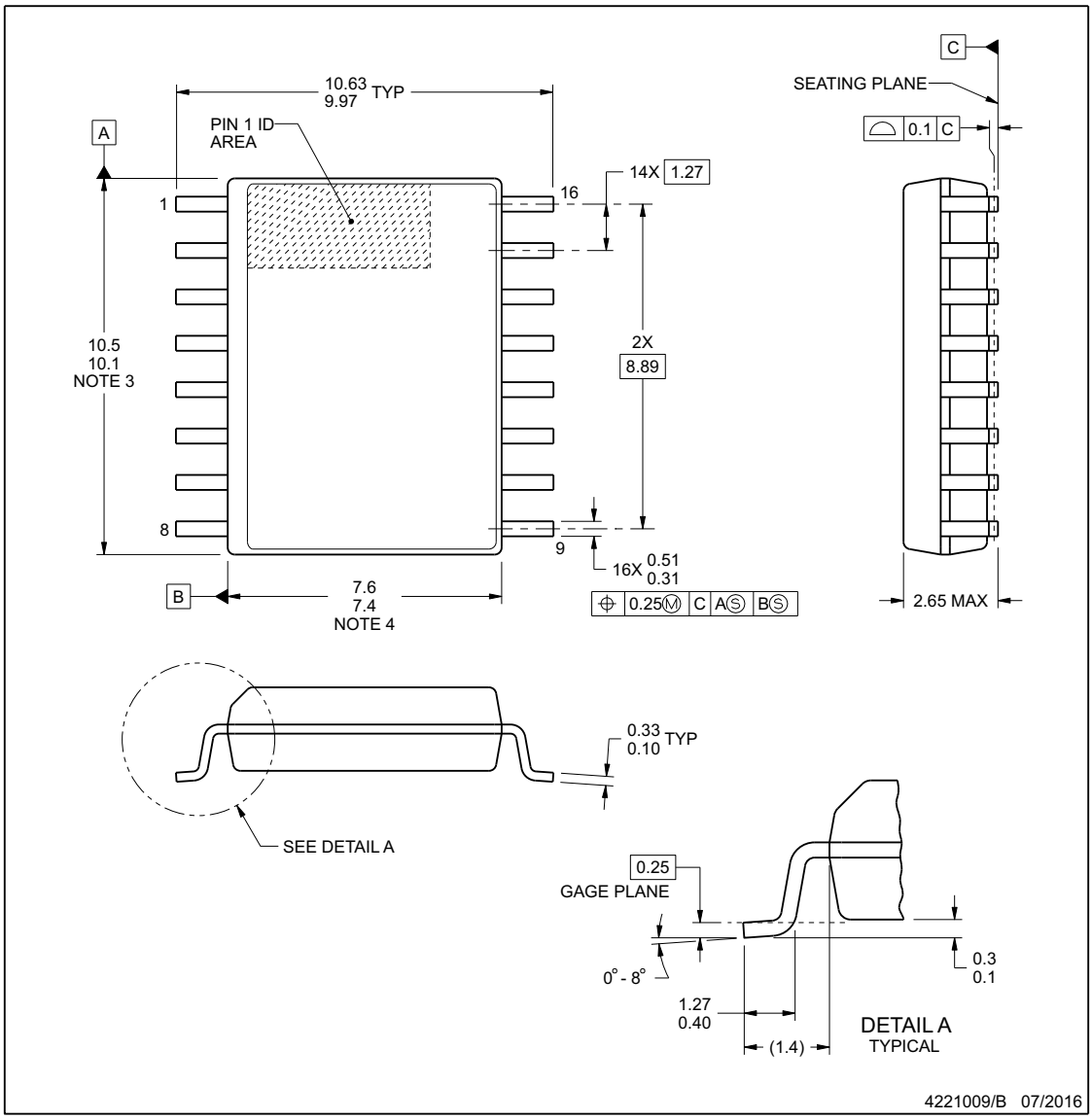
PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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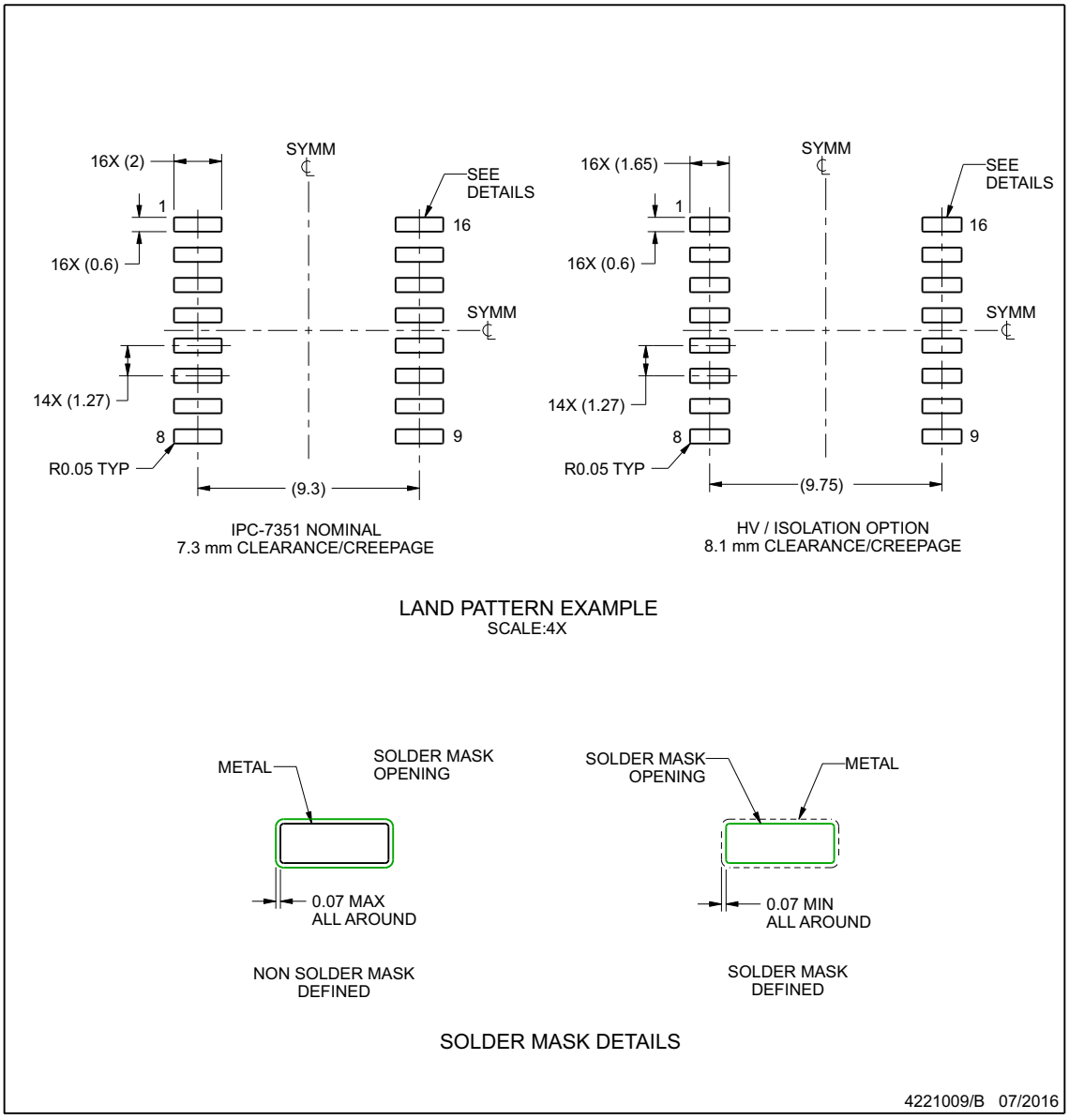
EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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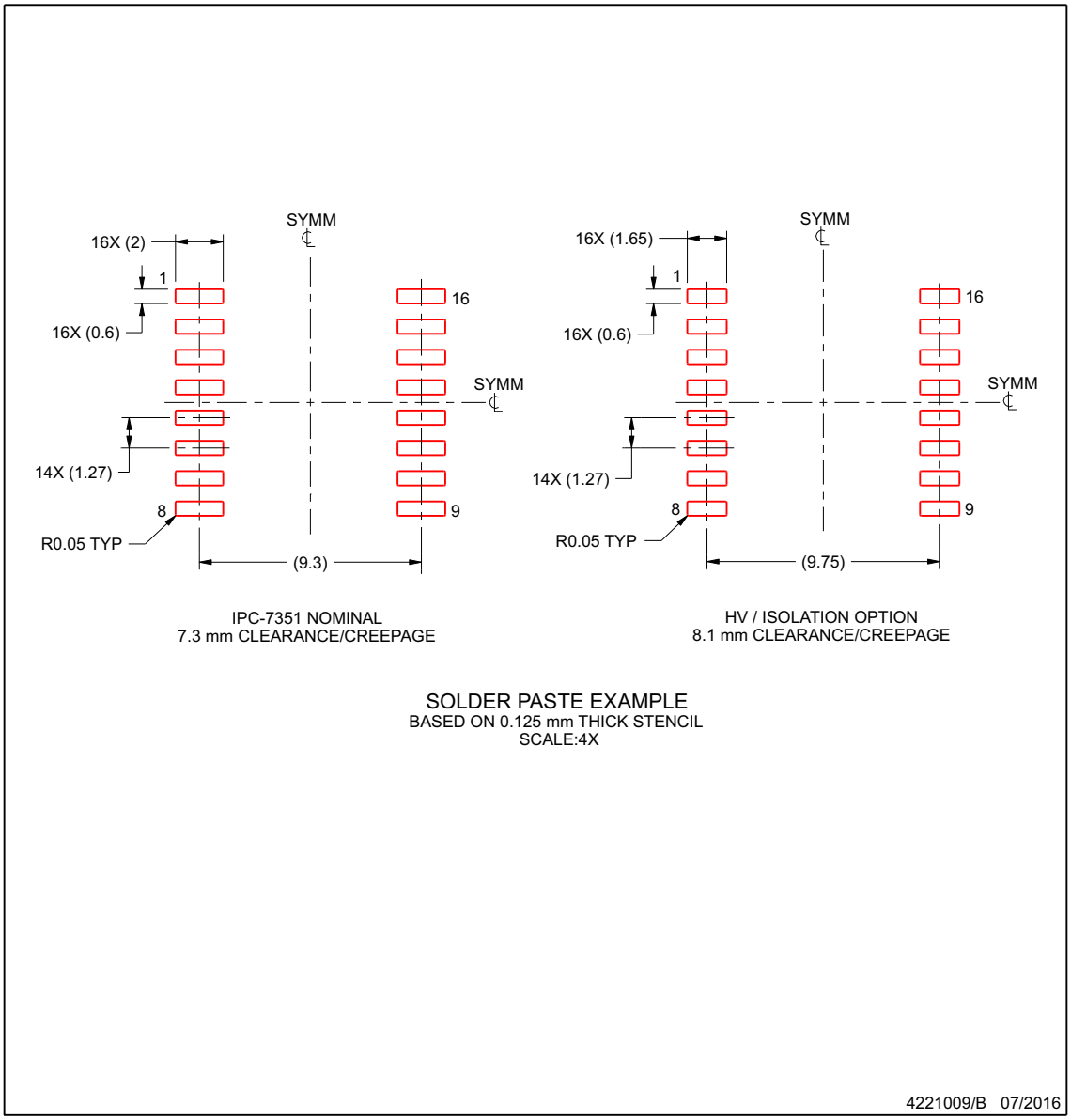
EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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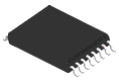
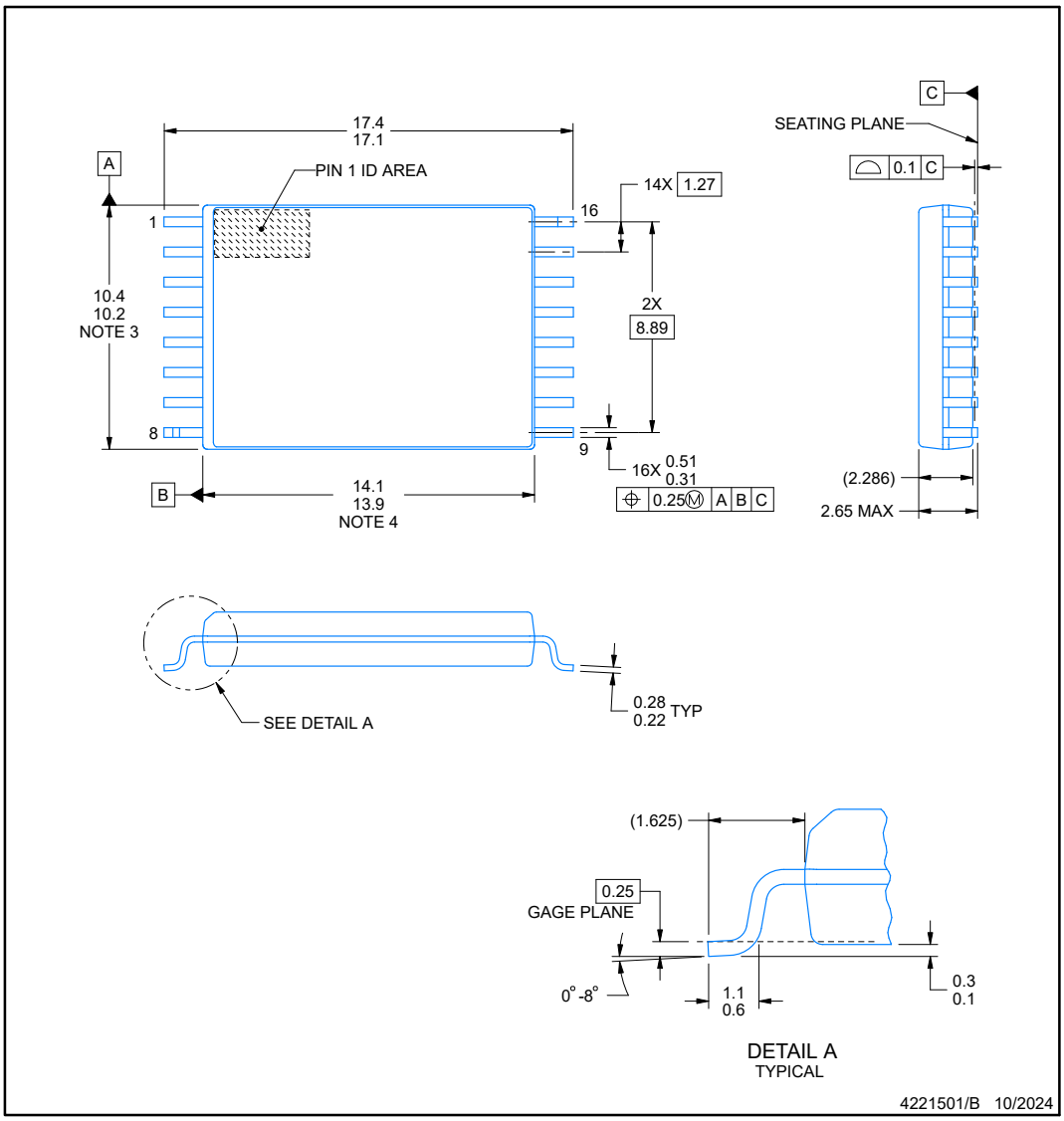
PACKAGE OUTLINE

DWW0016A



SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

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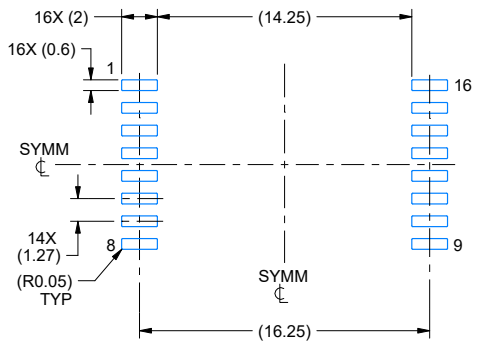
EXAMPLE BOARD LAYOUT

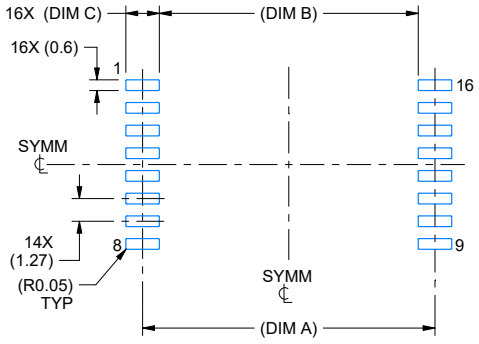
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

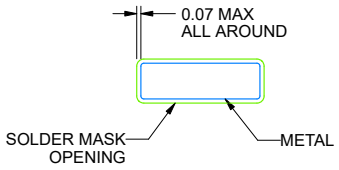


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

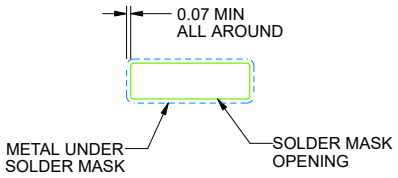


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/B 10/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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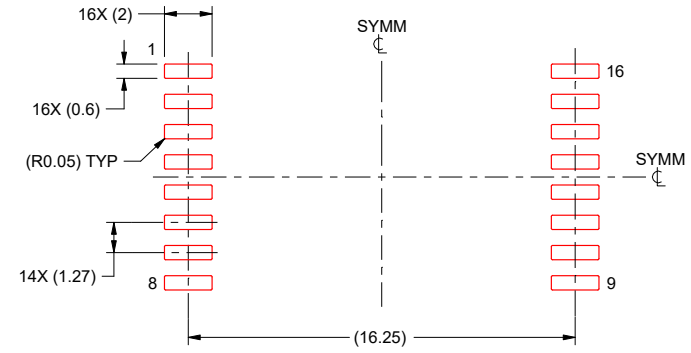
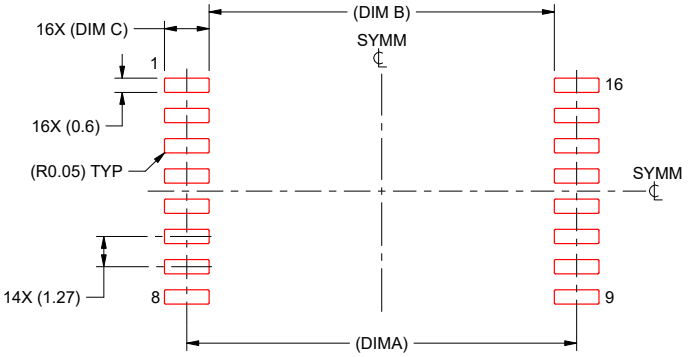
EXAMPLE STENCIL DESIGN

DWW0016A — **SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7841DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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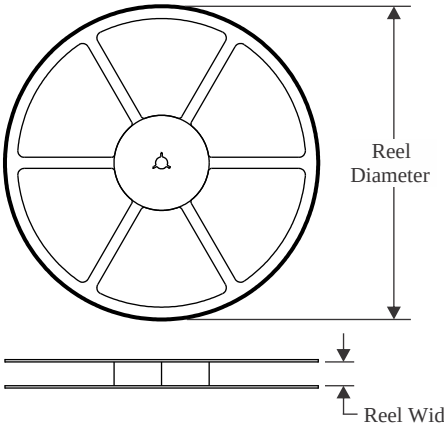
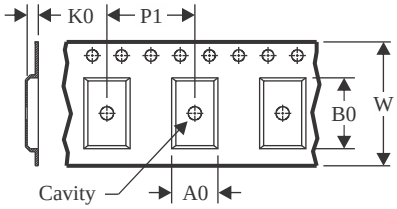
TAPE AND REEL INFORMATION

REEL DIMENSIONS

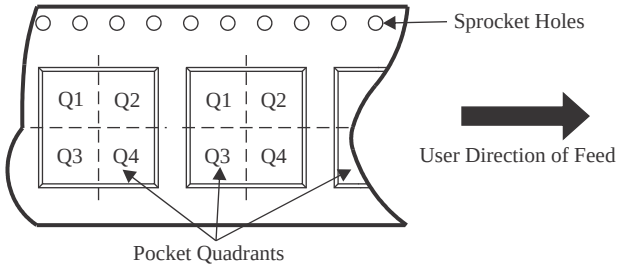


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

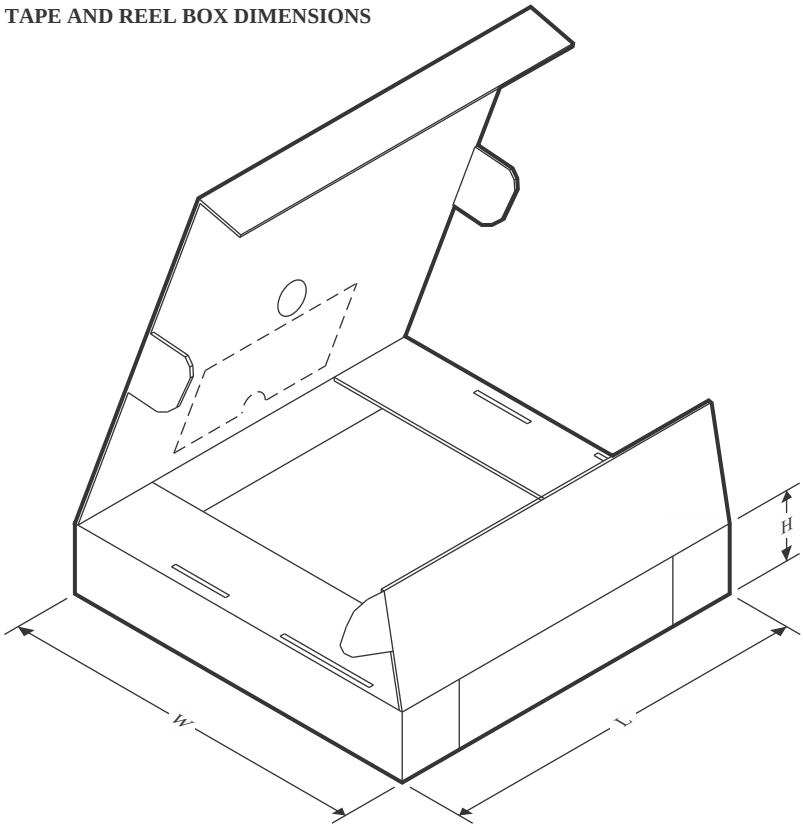
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7841DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7841DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7841FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7841FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

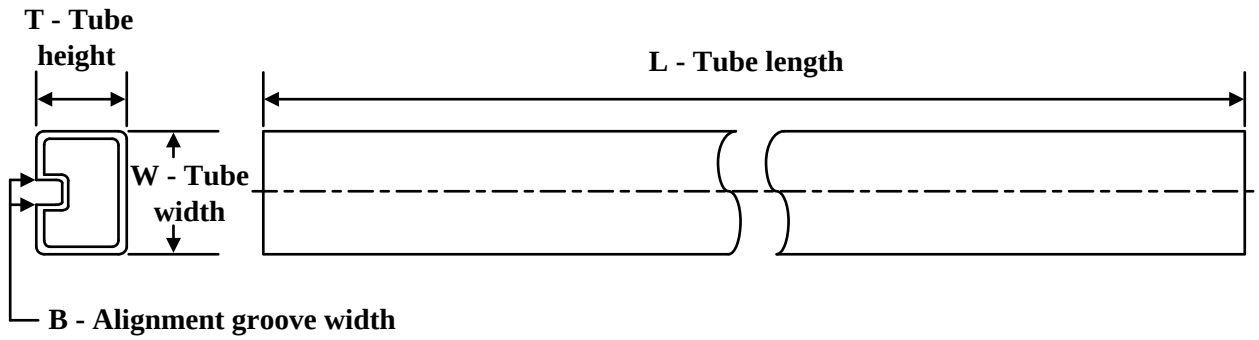
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7841DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7841DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7841FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7841FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7841DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7841DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7841FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7841FDWW	DWW	SOIC	16	45	507	20	5000	9

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