

# ISOM811x-Q1 3.75kV<sub>RMS</sub>、車載用シングルチャネルオプトエミュレータ、アナログトランジスタ出力付き

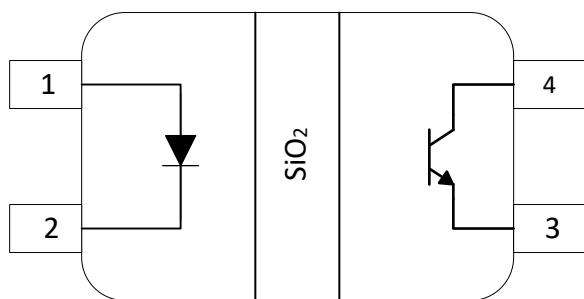
## 1 特長

- 業界標準のフォトトランジスタ オプトカプラに対してフットプリント互換かつピン互換アップグレード
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1: 動作時周囲温度範囲 -40°C ~ 125°C
- 1 チャネルの LED エミュレータ入力
- 電流伝達率 (CTR):  $I_F = 5\text{mA}$ ,  $V_{CE} = 5\text{V}$  のとき
  - ISOM8110-Q1, ISOM8115-Q1: 100% ~ 155%
  - ISOM8111-Q1, ISOM8116-Q1: 150% ~ 230%
  - ISOM8112-Q1, ISOM8117-Q1: 255% ~ 380%
  - ISOM8113-Q1, ISOM8118-Q1: 375% ~ 560%
- 高いコレクタ - エミッタ電圧:  $V_{CE}(\text{max}) = 80\text{V}$
- 堅牢な絶縁バリア
  - 絶縁定格: 3750V<sub>RMS</sub>
  - 動作電圧: 500V<sub>RMS</sub>, 707V<sub>PK</sub>
  - サージ耐性: 最大 10kV
- 応答時間:  $V_{CE} = 10\text{V}$ ,  $I_C = 2\text{mA}$ ,  $R_L = 100\Omega$  で 3 $\mu\text{s}$  (標準値)
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能: **ISOM811x-Q1**
- 安全性関連認証取得予定:
  - UL 1577 認定, 3750V<sub>RMS</sub> の絶縁
  - VDE による DIN EN IEC 60747-17 (VDE 0884-17) 準拠
  - IEC 62368-1 認定, IEC 61010-1 認定
  - CQC GB 4943.1 認定

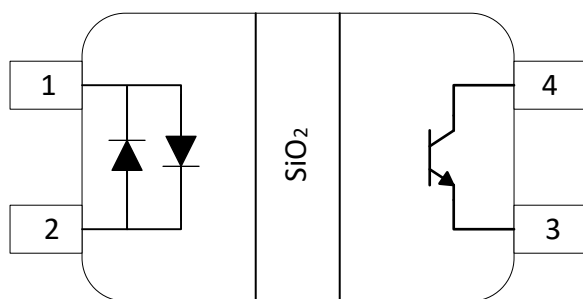
## 2 アプリケーション

- スイッチング電源
- 先進運転支援システム (ADAS)
- モータドライブの I/O および位置フィードバック

ISOM811(0-3)-Q1



ISOM811(5-8)-Q1



概略回路図

- ボディエレクトロニクス & 照明
- インフォテインメント & クラスタ
- HEV/EV のバッテリー管理システム (BMS)

## 3 概要

ISOM811x-Q1 デバイスは、LED エミュレータ入力とトランジスタ出力を備えたシングルチャネルのオプトカプラ エミュレータです。本デバイスは、従来の多くのオプトカプラとフットプリント互換かつピン互換のアップグレードであり、PCB の再設計なしで既存システムを拡張できます。

ISOM811x-Q1 オプトカプラ エミュレータは、オプトカプラと比較して信頼性が高く、高帯域幅、短いターンオフ遅延、低消費電力、広い温度範囲、厳格な CTR 制御とプロセス制御を実現しており、部品間スキューが小さい、という性能面での優位性もあります。経年変化や温度変化を補正する必要がないため、エミュレートされた LED 入力段の消費電力はオプトカプラよりも低減されます。

ISOM811x-Q1 デバイスは、2.54mm および 1.27mm ピッチの小型 SOIC-4 パッケージで供給され、3.75kV<sub>RMS</sub> の絶縁定格で、DC (ISOM811[0-3]-Q1) および双方向 DC (ISOM811[5-8]-Q1) 入力を選択できます。ISOM811x-Q1 は性能と信頼性が高いため、電源フィードバック設計、モータドライブ、産業用コントローラの I/O モジュール、ファクトリオートメーションアプリケーションなどに使用できます。

### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	パッケージサイズ <sup>(3)</sup>	本体サイズ (公称)
ISOM811x-Q1	SO-4 (DFG)	7.0mm × 3.5mm	4.8mm × 3.5mm
	SO-4 (DFH) <sup>(2)</sup>	7.0mm × 2.7mm	4.8mm × 2.7mm

- 詳細については、[セクション 12](#) を参照してください。
- プレビュー版のみ。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



## Table of Contents

<b>1 特長</b> .....	1	8.1 Overview.....	13
<b>2 アプリケーション</b> .....	1	8.2 Functional Block Diagram.....	13
<b>3 概要</b> .....	1	8.3 Feature Description.....	14
<b>4 Device Comparison</b> .....	3	8.4 Device Functional Modes.....	14
<b>5 Pin Configuration and Functions</b> .....	3	<b>9 Application and Implementation</b> .....	15
<b>6 Specifications</b> .....	4	9.1 Application Information.....	15
6.1 Absolute Maximum Ratings.....	4	9.2 Power Supply Recommendations.....	19
6.2 ESD Ratings .....	4	9.3 Layout.....	19
6.3 Recommended Operating Conditions .....	4	<b>10 Device and Documentation Support</b> .....	20
6.4 Thermal Information .....	4	10.1 Documentation Support.....	20
6.5 Insulation Specifications.....	5	10.2 ドキュメントの更新通知を受け取る方法.....	20
6.6 Safety-Related Certifications.....	6	10.3 サポート・リソース.....	20
6.7 Safety Limiting Values.....	6	10.4 Trademarks.....	20
6.8 Electrical Characteristics.....	7	10.5 静電気放電に関する注意事項.....	20
6.9 Switching Characteristics.....	9	10.6 用語集.....	20
6.10 Typical Characteristics.....	10	<b>11 Revision History</b> .....	20
<b>7 Parameter Measurement Information</b> .....	12	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	20
<b>8 Detailed Description</b> .....	13		

## 4 Device Comparison

表 4-1. Device Selection

PART NUMBER <sup>(2)</sup>	CTR	PACKAGE <sup>(1)</sup>	PIN PITCH
ISOM8110-Q1, ISOM8115-Q1	100% to 155%	4-pin SOIC (DFG), 4-pin SOIC (DFH)	2.54mm, 1.27mm
ISOM8111-Q1, ISOM8116-Q1	150% to 230%		
ISOM8112-Q1, ISOM8117-Q1	255% to 380%		
ISOM8113-Q1, ISOM8118-Q1	375% to 560%		

(1) DFH package is preview only.

(2) ISOM811(1-3)-Q1 and ISOM811(5-8)-Q1 are preview only.

## 5 Pin Configuration and Functions

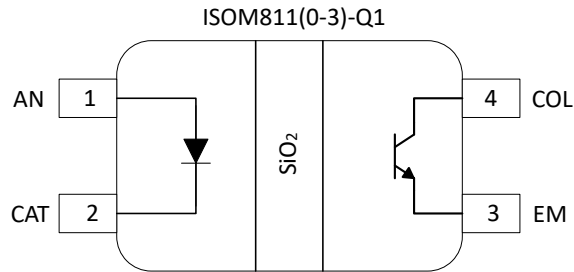


図 5-1. ISOM811(0-3)-Q1 4-Pin SOIC (Top View)

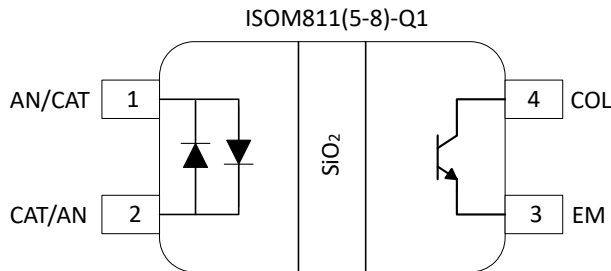


図 5-2. ISOM811(5-8)-Q1 4-Pin SOIC (Top View)

表 5-1. Pin Functions

NO.	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	NAME			
1	AN	I	I	Anode connection of input LED emulator
2	CAT	I	I	Cathode connection of input LED emulator
3	EM	O	O	Emitter for transistor
4	COL	O	O	Collector for transistor

(1) I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
$I_{F(max)}$	Maximum Input forward current		50	mA
$V_{CEO}$	Collector-emitter voltage		80	V
$V_{ECO}$	Emitter-collector voltage		7	V
$I_{FP}$	Input pulse forward current (1 $\mu$ s width)		1	A
$V_R$	Input reverse voltage at $I_R = 10\mu A$ <sup>(3)</sup>		7	V
$P_I$	Input power dissipation		140	mW
$I_C$	Collector current		50	mA
$P_C$	Collector power dissipation		150	mW
$P_T$	Total power dissipation		290	mW
$T_A$	Ambient temperature	-55	125	$^{\circ}C$
$T_J$	Operating junction temperature		150	$^{\circ}C$

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the operational sections of this document. If used outside the listed operational conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All specifications are at  $T_A = 25^{\circ}C$  unless otherwise noted
- (3) Only applies to ISOM8110-Q1, ISOM8112-Q1, and ISOM8113-Q1

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level 3A	$\pm 2000$	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	$\pm 1000$	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$I_{F(ON)}$	Input ON-state forward current	0.7		20	mA
$V_{CEO}$	Collector-emitter voltage	-5		48	V
$T_A$	Ambient temperature	-40		125	$^{\circ}C$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISOM811x-Q1		UNIT
		DFG (SOIC)	DFH (SOIC)	
		4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	283.9	288.8	$^{\circ}C/W$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	173.1	173.6	$^{\circ}C/W$
$R_{\theta JB}$	Junction-to-board thermal resistance	201.4	192.9	$^{\circ}C/W$
$\Psi_{JT}$	Junction-to-top characterization parameter	125.1	121.5	$^{\circ}C/W$
$\Psi_{JB}$	Junction-to-board characterization parameter	198.0	190.0	$^{\circ}C/W$

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) application note.



## 6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			4-DFG, 4-DFH	
<b>IEC 60664-1</b>				
CLR	External clearance <sup>(1)</sup>	Side 1 to side 2 distance through air	> 5	mm
CPG	External creepage <sup>(1)</sup>	Side 1 to side 2 distance across package surface	> 5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-III	
<b>DIN VDE V 0884-11:2017 <sup>(6)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	500	V <sub>RMS</sub>
		DC voltage	707	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production)	5303	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(2)</sup>	Tested in air, 1.2/50μs waveform per IEC 62368-1	7200	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	V <sub>IOSM</sub> ≥ 1.3 × V <sub>IMP</sub> ; tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2 πft), f = 1MHz	1	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1s (100% production)	3750	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) Testing is carried out in air to determine the surge immunity of the package.
- (3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

- (6) This coupler is suitable for *safe electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

### 6.6 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

### 6.7 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SO-4 PACKAGE (DFG)</b>						
I <sub>S</sub>	Safety limiting input current	R <sub>θJA</sub> = 283.9°C/W, V <sub>F</sub> = 1.4V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			300	mA
		R <sub>θJA</sub> = 283.9°C/W, V <sub>CEO</sub> = 40V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			10.5	mA
		R <sub>θJA</sub> = 283.9°C/W, V <sub>CEO</sub> = 24V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			17.5	mA
		R <sub>θJA</sub> = 283.9°C/W, V <sub>CEO</sub> = 15V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			28	mA
P <sub>S</sub>	Safety limiting total power	R <sub>θJA</sub> = 283.9°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			420	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> must not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>. The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.  
 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
 $P_S = I_S \times V_I$ , where V<sub>I</sub> is the maximum input voltage.

## 6.8 Electrical Characteristics

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
<b>INPUT</b>							
$V_F$	Input forward voltage	$I_F = 5\text{mA}$	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		1.2	1.4	V
$V_F$	Input forward voltage	$I_F = 5\text{mA}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		1.2	1.6	V
$V_F$	Input forward voltage	$I_F = \pm 5\text{mA}$	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		1.2	1.5	V
$V_F$	Input forward voltage	$I_F = \pm 5\text{mA}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		1.2	1.5	V
$I_R$	Input reverse current	$V_R = 5\text{V}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1			10	$\mu\text{A}$
$C_{IN}$	Input capacitance	At 1MHz, $V_F = 0\text{V}$	ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1		19		pF
$C_{IN}$	Input capacitance	At 1MHz, $V_F = 0\text{V}$	ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1		6		pF
<b>OUTPUT</b>							
$C_{CE}$	Collector-emitter capacitance	1MHz, $V_F = 0\text{V}$	ISOM811x-Q1		10		pF
$V_{CE(SAT)}$	Collector-emitter saturation voltage	$I_F = 20\text{mA}$ , $I_C = 1\text{mA}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM811x-Q1			0.3	V
$I_{C\_DARK}$	Collector dark current	$V_{CE} = 20\text{V}$ , $I_F = 0\text{mA}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM811x-Q1			100	nA
$I_{EC}$	Reverse current	$V_{EC} = 7\text{V}$ , $I_F = 0\text{mA}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM811x-Q1			100	$\mu\text{A}$
$I_{C\_OFF}$	OFF_state collector current	$V_F = 0.7\text{V}$ , $V_{CE} = 48\text{V}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM811x-Q1			10	$\mu\text{A}$
<b>CTR<sup>(1)</sup></b>							
CTR	Current Transfer Ratio	$I_F = 2\text{mA}$ , $V_{CE} = 5\text{V}$ , $T_A = -40$ to $125^\circ\text{C}$	ISOM8110-Q1	80	130	180	%
			ISOM8115-Q1	80	130	180	%
			ISOM8111-Q1	120	180	270	%
			ISOM8116-Q1	120	180	270	%
			ISOM8112-Q1	200	300	450	%
			ISOM8117-Q1	200	300	450	%
			ISOM8113-Q1	295	440	655	%
ISOM8118-Q1	295	440	655	%			

All specifications are at T<sub>A</sub> = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
CTR	Current Transfer Ratio	I <sub>F</sub> = 5mA, V <sub>CE</sub> = 5V, T <sub>A</sub> = -40 to 125°C	ISOM8110-Q1	100	120	155	%
			ISOM8115-Q1	100	120	155	%
			ISOM8111-Q1	150	180	230	%
			ISOM8116-Q1	150	180	230	%
			ISOM8112-Q1	255	300	380	%
			ISOM8117-Q1	255	300	380	%
			ISOM8113-Q1	375	440	560	%
			ISOM8118-Q1	375	440	560	%

(1) CTR (%) = (I<sub>C</sub> / I<sub>F</sub>) x 100%



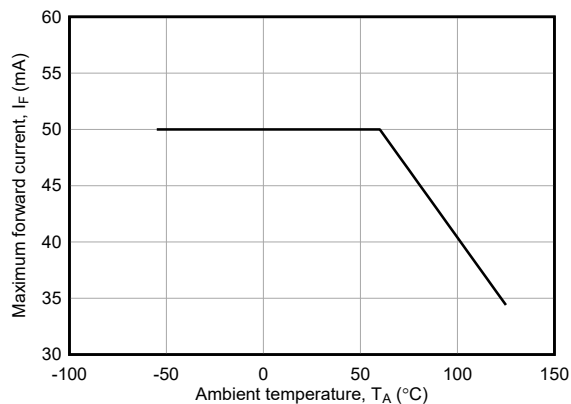


## 6.9 Switching Characteristics

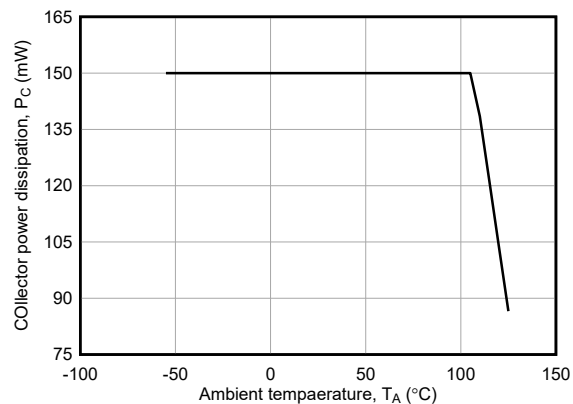
All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER	TEST CONDITIONS	GPN	MIN	TYP	MAX	UNIT
<b>AC</b>						
$t_r$	Rise time, see <a href="#">7-2</a> and <a href="#">7-3</a>	$V_{CC} = 10\text{V}$ , $I_C = 2\text{mA}$ , $R_L = 100\Omega$ , $C_L = 50\text{pF}$	ISOM8110-Q1	3.2		$\mu\text{s}$
			ISOM8113-Q1	2.5		$\mu\text{s}$
$t_f$	Fall time, see <a href="#">7-2</a> and <a href="#">7-3</a>	$V_{CC} = 10\text{V}$ , $I_C = 2\text{mA}$ , $R_L = 100\Omega$ , $C_L = 50\text{pF}$	ISOM8110-Q1	4.0		$\mu\text{s}$
			ISOM8113-Q1	7.5		$\mu\text{s}$
$T_{ON}$	Turn on time, see <a href="#">7-2</a> and <a href="#">7-3</a>	$V_{CC} = 10\text{V}$ , $I_C = 2\text{mA}$ , $R_L = 100\Omega$ , $C_L = 50\text{pF}$	ISOM8110-Q1, ISOM8115-Q1	5.7		$\mu\text{s}$
			ISOM8111-Q1, ISOM8116-Q1	4.5		$\mu\text{s}$
			ISOM8112-Q1, ISOM8117-Q1	6.2		$\mu\text{s}$
			ISOM8113-Q1, ISOM8118-Q1	16.7		$\mu\text{s}$
$T_{OFF}$	Turn off time, see <a href="#">7-2</a> and <a href="#">7-3</a>	$V_{CC} = 10\text{V}$ , $I_C = 2\text{mA}$ , $R_L = 100\Omega$ , $C_L = 50\text{pF}$	ISOM8110-Q1, ISOM8115-Q1	3.6		$\mu\text{s}$
			ISOM8111-Q1, ISOM8116-Q1	3.7		$\mu\text{s}$
			ISOM8112-Q1, ISOM8117-Q1	3.1		$\mu\text{s}$
			ISOM8113-Q1, ISOM8118-Q1	2.7		$\mu\text{s}$
$t_s$	Storage time; time required for the output waveform to change from 0% (100%) to 10% (90%) when input is turned on and back off, see <a href="#">7-3</a>	$V_{CC} = 5\text{V}$ , $I_F = 1.6\text{mA}$ , $R_L = 4.7\text{k}\Omega$	ISOM811x-Q1		21	$\mu\text{s}$
BW	Bandwidth, see <a href="#">7-4</a> and <a href="#">7-5</a>	$V_{IN\_DC} = 5\text{V}$ , $V_{IN\_AC} = 1\text{Vpk}$ , $R_{IN} = 2\text{k}\Omega$ , $V_{CC} = 5\text{V}$ , $R_{LOAD} = 100\Omega$ , $C_L = 50\text{pF}$ , measured at $V_{CE} -3\text{dB}$ sinewave	ISOM811x-Q1	680		kHz

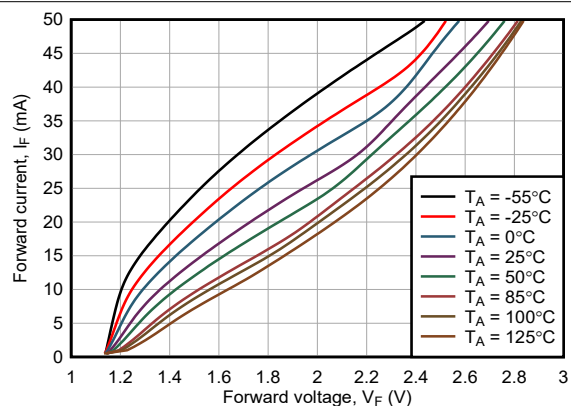
## 6.10 Typical Characteristics



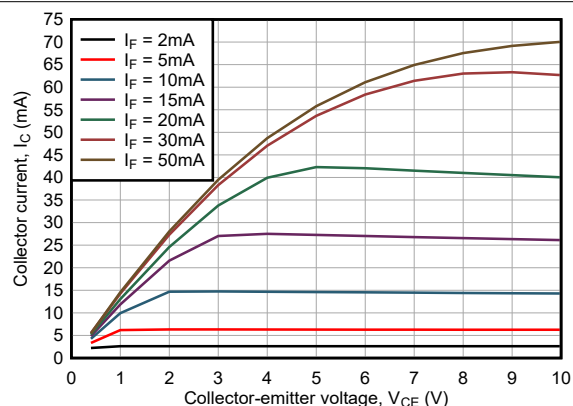
**6-1. Maximum Forward Current vs Ambient Temperature**



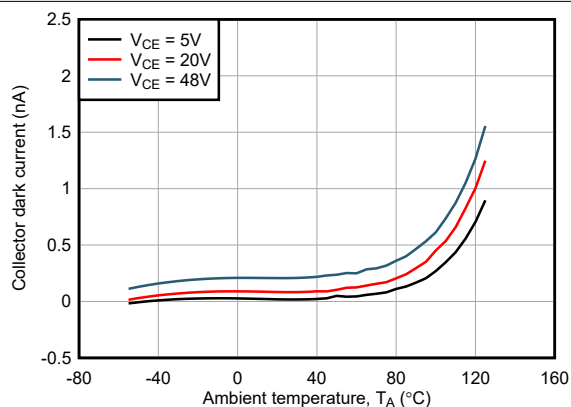
**6-2. Maximum Collector Power Dissipation vs Ambient Temperature**



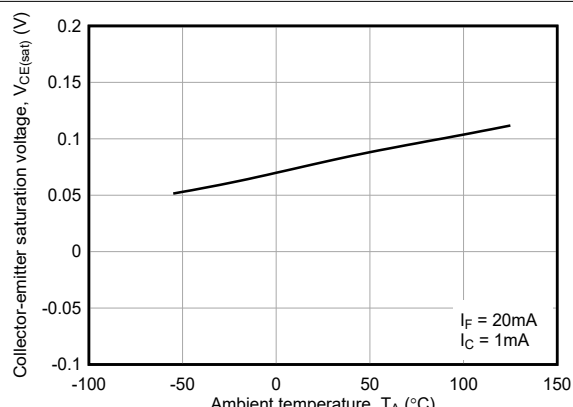
**6-3. Forward Voltage vs Forward Current**



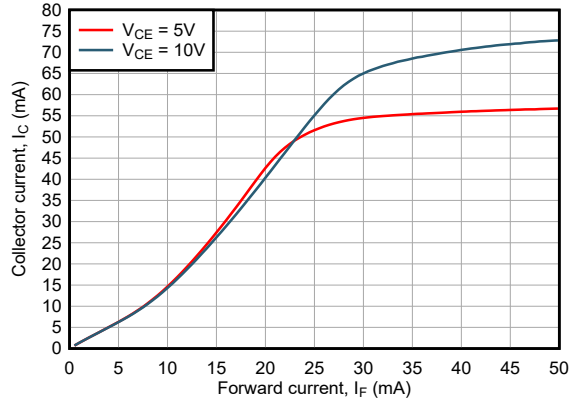
**6-4. Collector Current vs Collector-Emitter Voltage**



**6-5. Collector Dark Current vs Ambient Temperature**

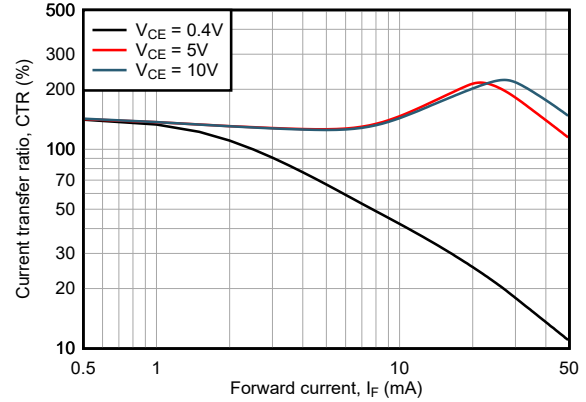


**6-6. Collector-Emitter Saturation Voltage vs Ambient Temperature**



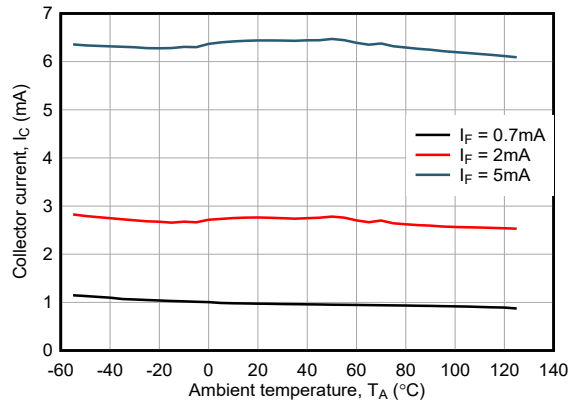
ISOM8110-Q1  $T_A = 25^\circ\text{C}$

6-7. Collector Current vs Forward Current



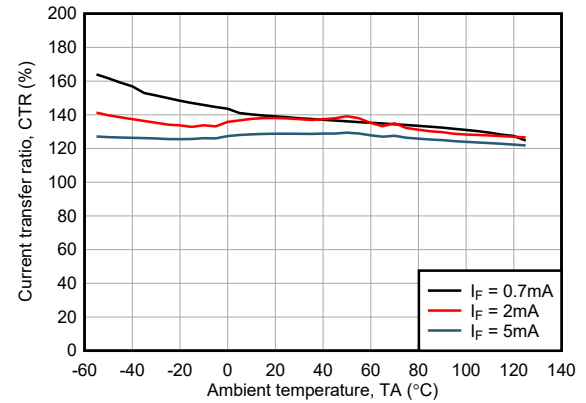
ISOM8110-Q1  $T_A = 25^\circ\text{C}$

6-8. Current Transfer Ratio vs Forward Current



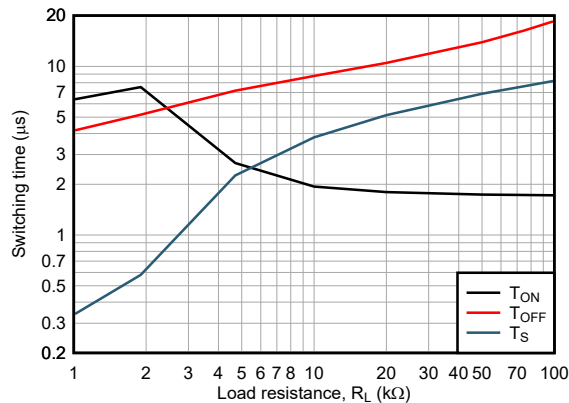
ISOM8110-Q1  $V_{CE} = 5\text{V}$

6-9. Collector Current vs Ambient Temperature



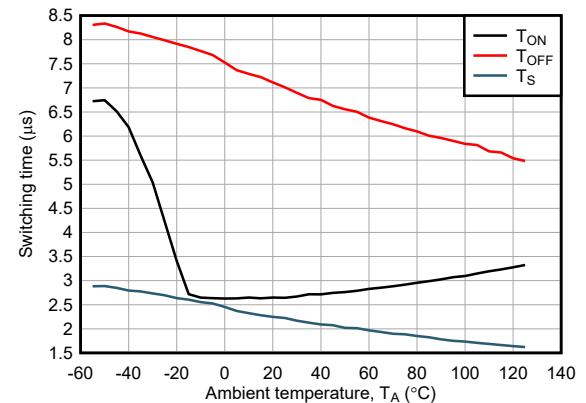
ISOM8110-Q1  $V_{CE} = 5\text{V}$

6-10. Current Transfer Ratio vs Ambient Temperature



$I_F = 1.6\text{mA}$  ISOM8110-Q1  $V_{CC} = 5\text{V}$

6-11. Switching Time vs Load Resistance



$I_F = 1.6\text{mA}$  ISOM8110-Q1  $V_{CC} = 5\text{V}$

$R_L = 4.7\text{k}\Omega$

6-12. Switching Time vs Ambient Temperature



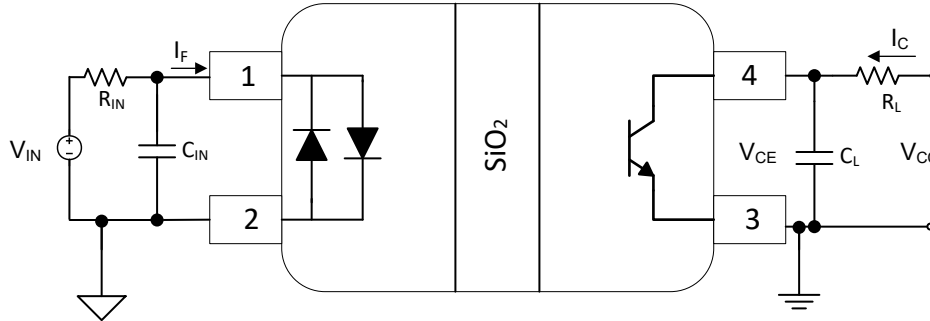


図 7-5. ISOM811(5-8)-Q1 Test Circuit for Bandwidth

## 8 Detailed Description

### 8.1 Overview

The ISOM811x-Q1 opto-emulators are single-channel, pin-to-pin upgrades for many traditional optocouplers. While standard optocouplers use an LED as the input stage, ISOM811x-Q1 uses an emulated LED as the input stage. The input and output stages are isolated by TI's proprietary silicon dioxide-based ( $\text{SiO}_2$ ) isolation barrier. This isolation technology makes ISOM811x-Q1 resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. Ordering options include four different ranges of current transfer ratio (CTR) and input options supporting uni-polar and bi-polar DC flow.

The ISOM811x-Q1 family of devices isolate DC and bidirectional DC signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers.

The functional block diagram of ISOM811x-Q1 devices are shown in [セクション 8.2](#). The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier that contains information on how much current is flowing through the input pins. The receiver demodulates the signal after advanced signal conditioning and produces the signal through the output stage. These devices also incorporate advanced circuit techniques to maximize bandwidth and minimize radiated emissions. [図 8-3](#) shows conceptual details of how the OOK scheme works.

### 8.2 Functional Block Diagram

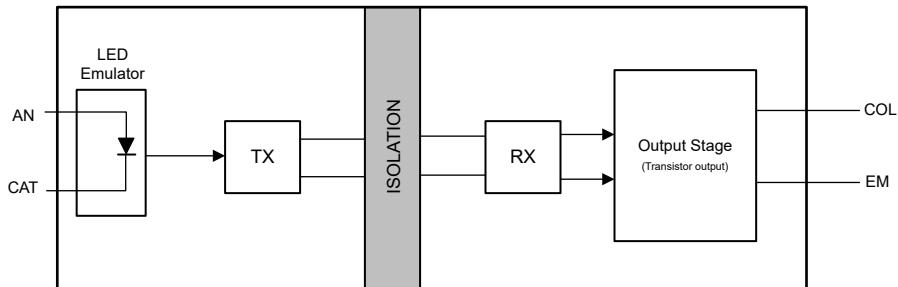


図 8-1. Conceptual Block Diagram of an Opto-emulator ISOM811(0-3)-Q1



## 9 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The ISOM811x-Q1 devices are single-channel opto-emulators with LED-emulator input and transistor output. The devices use on-off keying modulation to transmit data across the isolation barrier. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO<sub>2</sub>) isolation barrier which provides robust isolation. With wider temperature ratings than traditional optocouplers, ISOM811x-Q1 opto-emulators can provide reliable signal isolation in harsh environments.

The ISOM811x-Q1 devices are capable of sinking current when subjected to an external load being connected to the device. Like typical transistor output optocouplers, the output current depends on the input current level ( $I_F$ ) and the current transfer ratio (CTR). With multiple CTR options (100% - 560%), low input current, high bandwidth, low turn-off delay, low power consumption, and wider temperature range, ISOM811x-Q1 devices are designed for use in a variety of industries such as factory automation, building automation, e-mobility, automotive, avionics, medical, and power delivery.

#### 9.1.1 Typical Application

ISOM811x-Q1 opto-emulators are commonly used in the feedback control loops of isolated power supplies. These devices are used to solve the problem of feeding back current while isolating the primary and secondary domains to regulate the output voltage.

In power supplies, the output voltage is isolated from main input voltage using a transformer (for example: flyback converter). For analog power supply units, the controller IC is usually on the primary side of the transformer. For closed loop control, measuring the output voltage on the secondary side and feeding the voltage back to the controller on the primary is necessary. The most common method of achieving this design is using an opto-emulator such as ISOM811x-Q1, error amplifier (commonly TL431), and a voltage comparator to form a feedback loop across the isolation barrier

☒ 9-1 illustrates a typical isolated power supply. In this implementation, the output voltage is sensed by an error amplifier using the resistor divider (R1 and R2). Depending on the voltage level that the error amplifier senses, the TL431 can drive the current of the ISOM811x-Q1 higher or lower which is then compared to a voltage reference. The information is passed across the isolation barrier through ISOM811x-Q1 to the primary side, where the PWM control circuit modulates the power stage to regulate the output voltage. The TL431 and ISOM811x-Q1 play an important role for stable feedback and control loop.

The ISOM811x-Q1 devices enable improvements in transient response, reliability, and stability as compared to commonly used optocoupler as the CTR is stable over wide temperature range providing a small, low-cost, highly reliable, and easy-to-design implementation.

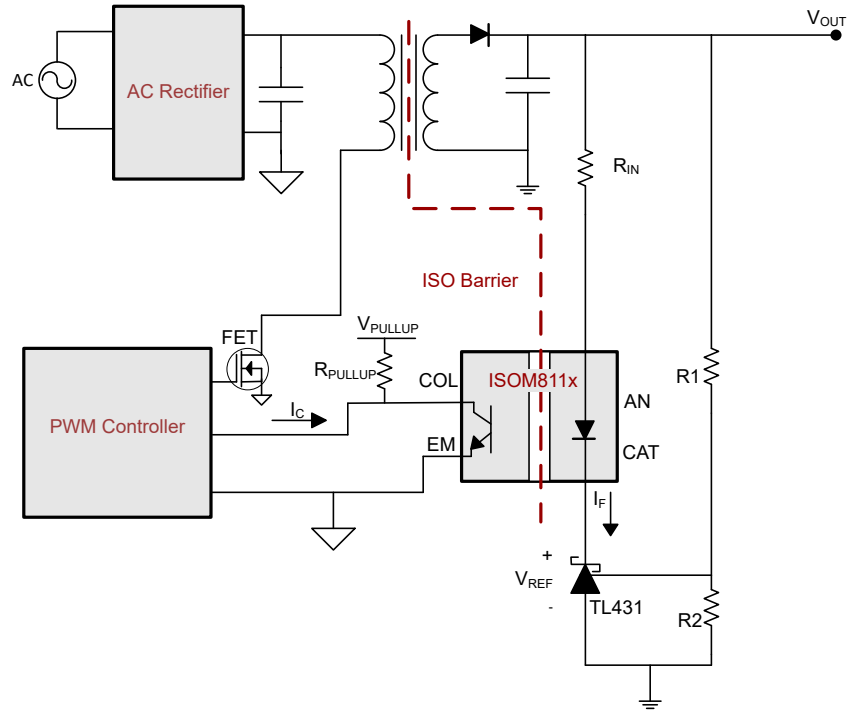


図 9-1. Typical Isolated Power Supply Application Using ISOM811x-Q1

### 9.1.1.1 Design Requirements

To design with ISOM811x-Q1 devices, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Input forward current range, $I_F$	0.7mA (min), 20mA (max)
Current transfer ratio at $I_F = 5\text{mA}$ , CTR	100% to 155%
Collector current tolerance, $I_C$	50mA (max)
Collector-emitter voltage (saturation), $V_{CE(SAT)}$	0.3V (max)
Input forward voltage, $V_F$	1.2V (typ)

### 9.1.1.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM811x-Q1 opto-emulators. External components must be selected to operate ISOM811x-Q1 within the *Recommended Operating Conditions*. The following recommendations on component selection focus on the design of a typical feedback control loop for an isolated flyback converter.

When using an optocoupler in a feedback control loop for an isolated power supply, many variables can affect how to properly use the optocoupler, including the output voltage of the power supply and the type of controller the feedback signal is being sent to. For this example, assume that the output voltage of this power supply,  $V_{OUT}$ , is 5V, and the PWM controller being used has an integrated error amplifier with a COMP pin that acts as the output of this amplifier.

#### 9.1.1.2.1 Sizing $R_{PULLUP}$

The transistor output of ISOM811x-Q1 operates in active, saturation, reverse, and cut-off regions, just like a regular transistor. To verify that the output does not get damaged when the output is saturated, the minimum value of  $R_{PULLUP}$  can be calculated for a given pull-up voltage,  $V_{PULLUP}$ , in 式 1:



$$R_{PULLUP} > \frac{V_{PULLUP} - V_{CE(SAT)}}{I_{C(MAX)}} \quad (1)$$

For the example of a feedback loop application, we can calculate the minimum required value for  $R_{PULLUP}$  for a given  $V_{PULLUP}$  of 10V, the maximum output voltage of the error amplifier ( $V_{COMP(MAX)}$ ) of 2.5V, and the maximum output current of the error amplifier is internally clamped at 1.6mA. The equation to calculate  $R_{PULLUP}$  is shown in 式 2:

$$R_{PULLUP} > \frac{V_{PULLUP} - V_{COMP(MAX)}}{I_{COMP(CLAMP)}} = \frac{10V - 2.5V}{1.6mA} = 4.66k\Omega \quad (2)$$

#### 9.1.1.2.2 Sizing $R_{IN}$

The input side of ISOM811x-Q1 is current-driven. To limit the amount of current flowing into the AN pin, placing a series resistor,  $R_{IN}$ , in series with the input as shown in 図 9-1 is recommended.

Depending on how the ISOM811x-Q1 device is being used, the value of  $R_{IN}$  can vary quite a bit. However, at a high level, to make sure the input does not get damaged, the minimum value of  $R_{IN}$  can be calculated for a given input voltage,  $V_{IN}$ , in 式 3:

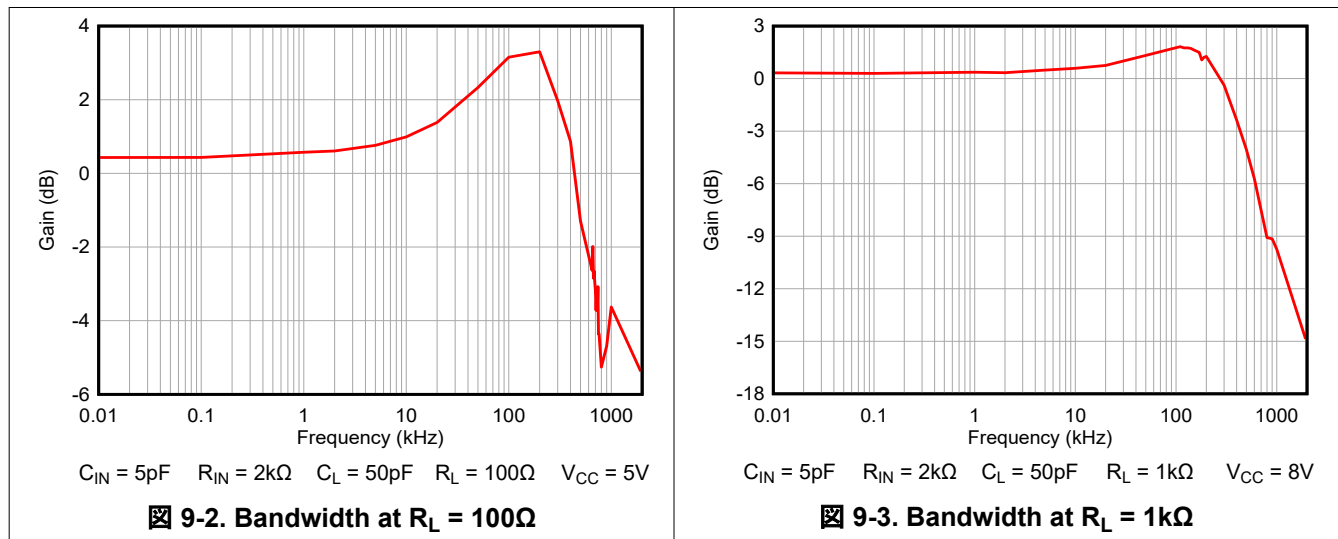
$$R_{IN} > \frac{V_{IN} - V_F}{I_{C(MAX)}} \quad (3)$$

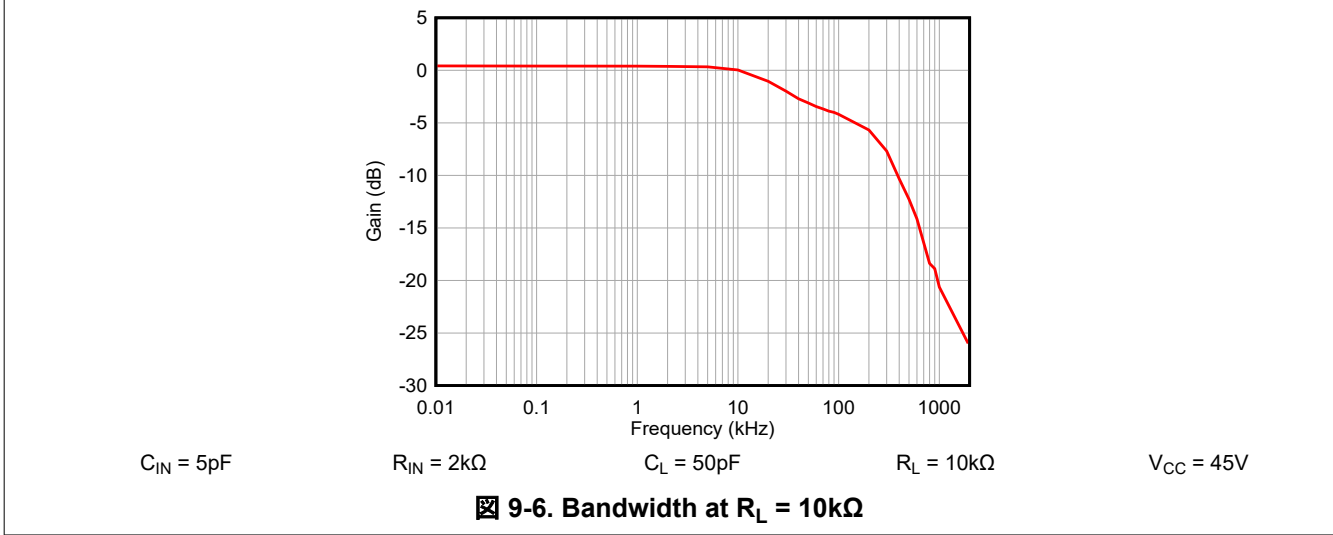
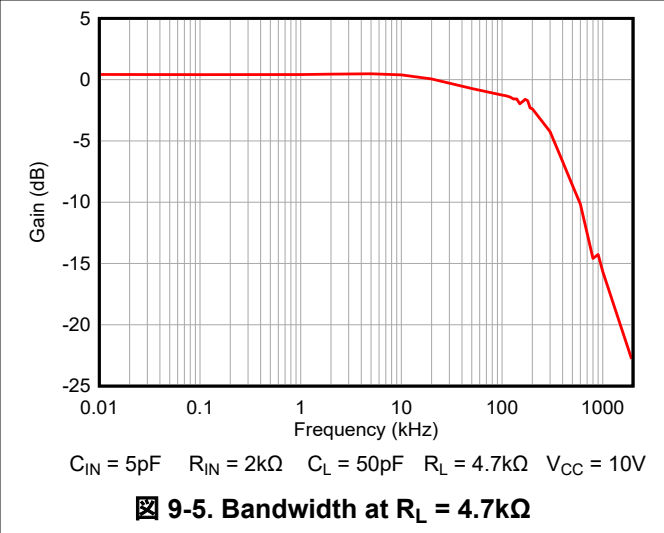
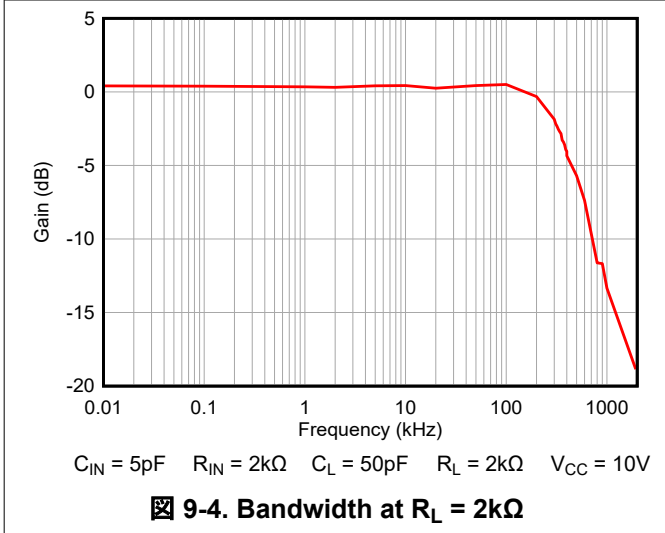
However, in the use case of a feedback loop,  $R_{IN}$  directly affects the mid-band gain of the loop. Assuming that the TL431 has been configured to give a reference voltage,  $V_{REF}$ , of 2.5V and  $R_{PULLUP}$  is 5k $\Omega$ , 式 4 is used to calculate the maximum value of  $R_{IN}$  verifying that the  $V_{COMP}$  voltage on the primary side can be pulled to the saturation voltage of the ISOM811x-Q1,  $V_{CE(SAT)}$ .

$$R_{IN} < \frac{(V_{OUT} - V_{REF} - V_F) \times R_{PULLUP} \times CTR_{MIN}}{V_{PULLUP} - V_{CE(SAT)}} = \frac{(5V - 2.5V - 1.2V) \times 5k\Omega \times 100\%}{10V - 0.3V} = 670\Omega \quad (4)$$

#### 9.1.1.3 Application Curves

The following curves show ISOM8110-Q1 bandwidth performance over different loading conditions where  $V_{IN} = 5V_{DC} + 2V_{PK}$ . See 図 7-4 for setup details.





## 9.2 Power Supply Recommendations

ISOM811x-Q1 does not require a dedicated power supply to operate since there is no supply pin. Take care to not violate recommended I/O specifications for proper device functionality.

## 9.3 Layout

### 9.3.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

### 9.3.2 Layout Example

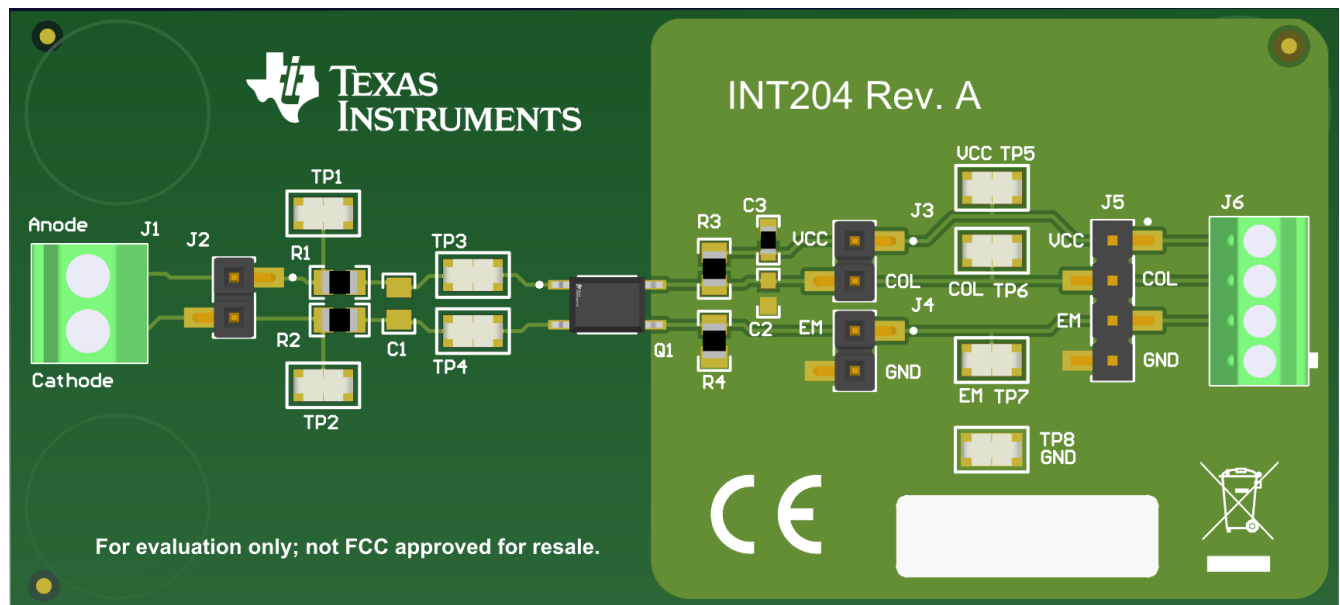


図 9-7. Layout Example of ISOM811x-Q1 With a Single Layer Board

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [Introduction to Opto-Emulators](#), application note
- Texas Instruments, [ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output Evaluation Module](#), EVM user's guide

### 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.  
 すべての商標は、それぞれの所有者に帰属します。

### 10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision \* (April 2024) to Revision A (July 2024)

Page

- |                                      |   |
|--------------------------------------|---|
| • ドキュメント全体にわたって図、表、相互参照の採番方法を更新..... | 1 |
| • ドキュメント全体にわたってパッケージおよび製品情報を更新.....  | 1 |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

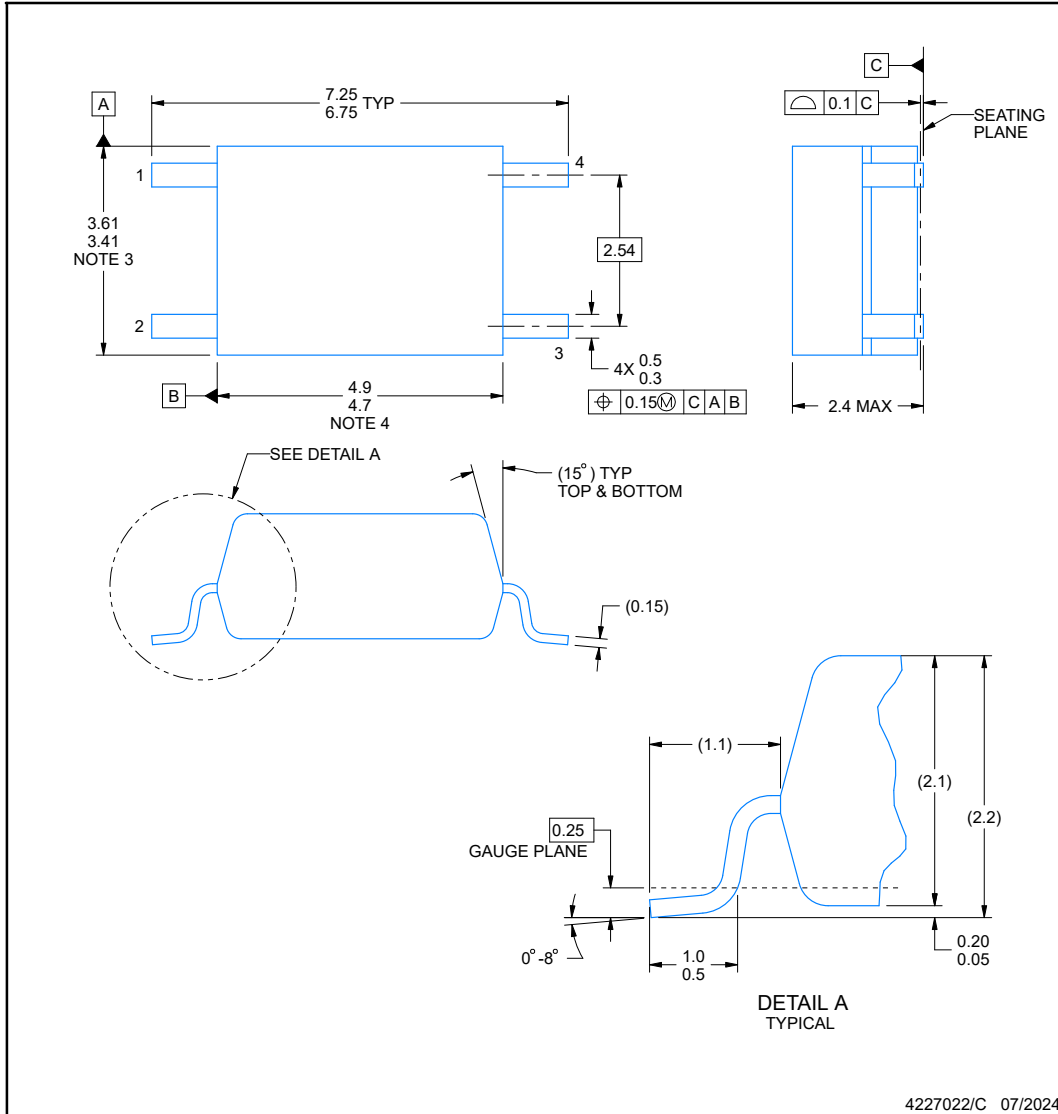


DFG0004A

PACKAGE OUTLINE

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

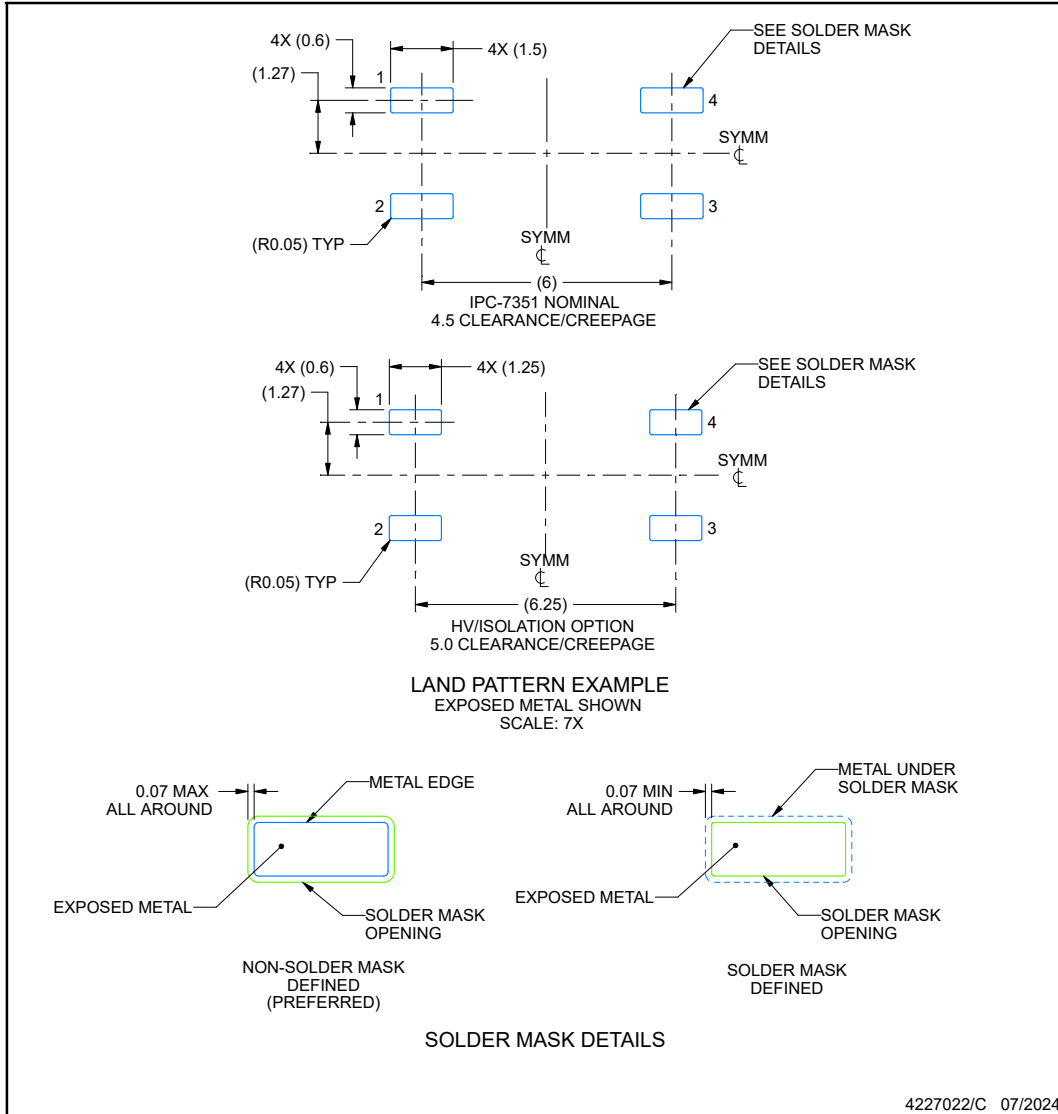
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash.

**EXAMPLE BOARD LAYOUT**

**DFG0004A**

**SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

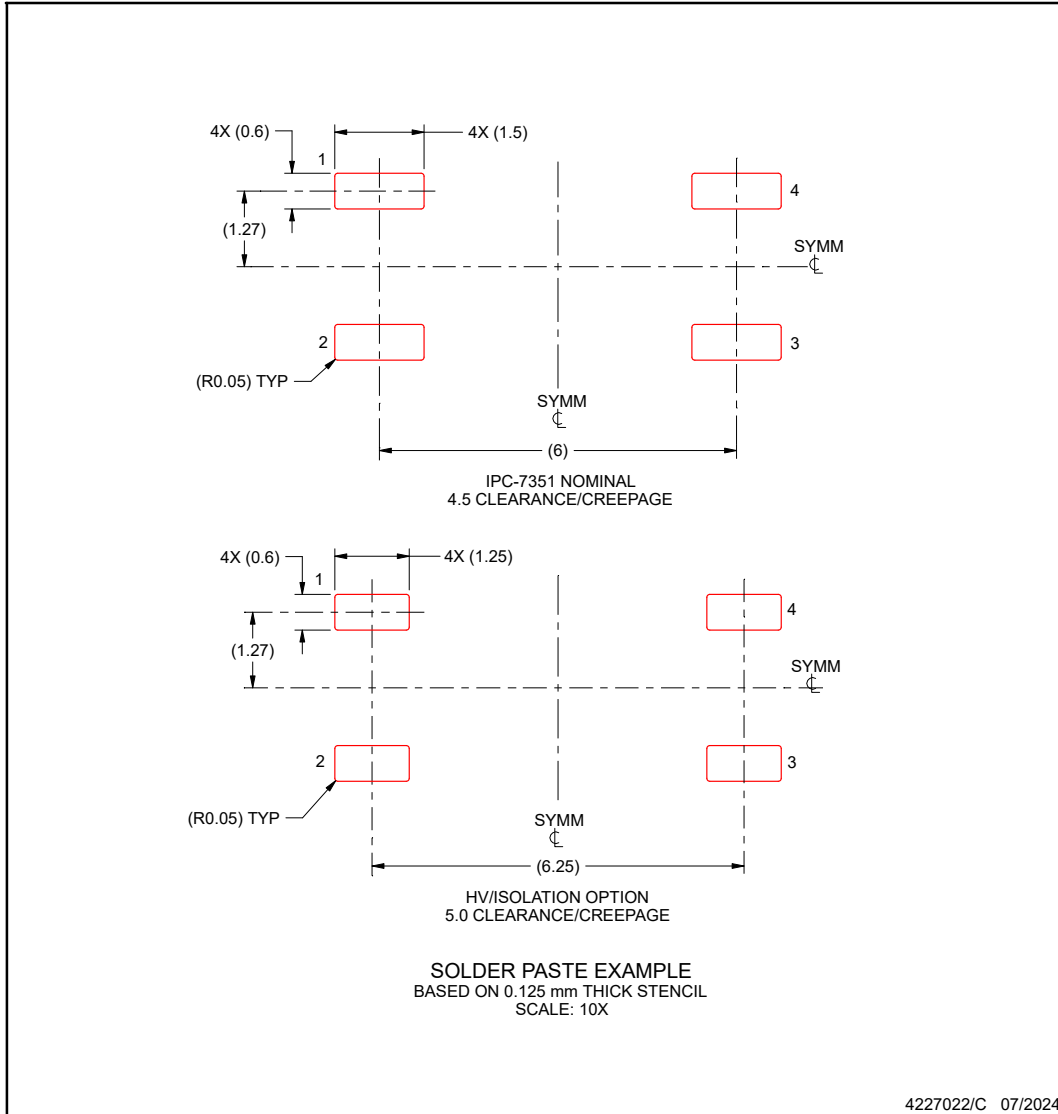


### EXAMPLE STENCIL DESIGN

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOM8110DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8110	<a href="#">Samples</a>
ISOM8111DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8111	<a href="#">Samples</a>
ISOM8112DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8112	<a href="#">Samples</a>
ISOM8113DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8113	<a href="#">Samples</a>
ISOM8115DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8115	<a href="#">Samples</a>
ISOM8116DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8116	<a href="#">Samples</a>
ISOM8117DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8117	<a href="#">Samples</a>
ISOM8118DFGRQ1	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8118	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISOM8110-Q1, ISOM8111-Q1, ISOM8112-Q1, ISOM8113-Q1, ISOM8115-Q1, ISOM8116-Q1, ISOM8117-Q1, ISOM8118-Q1 :**

● Catalog : [ISOM8110](#), [ISOM8111](#), [ISOM8112](#), [ISOM8113](#), [ISOM8115](#), [ISOM8116](#), [ISOM8117](#), [ISOM8118](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8110DFGRQ1	SOIC	DFG	4	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8110DFGRQ1	SOIC	DFG	4	2000	353.0	353.0	32.0

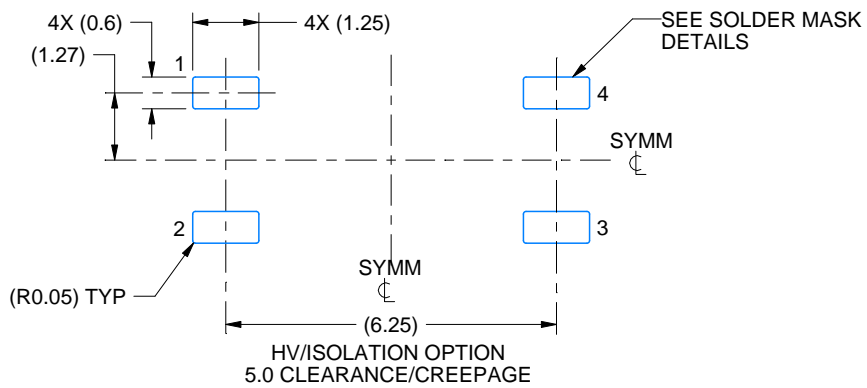
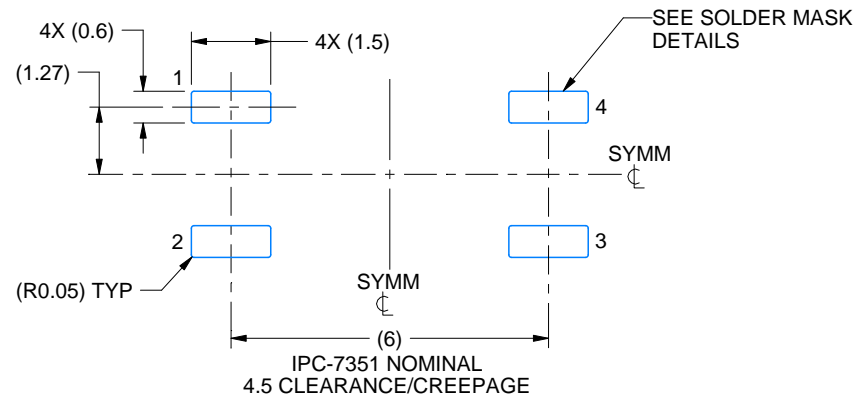


# EXAMPLE BOARD LAYOUT

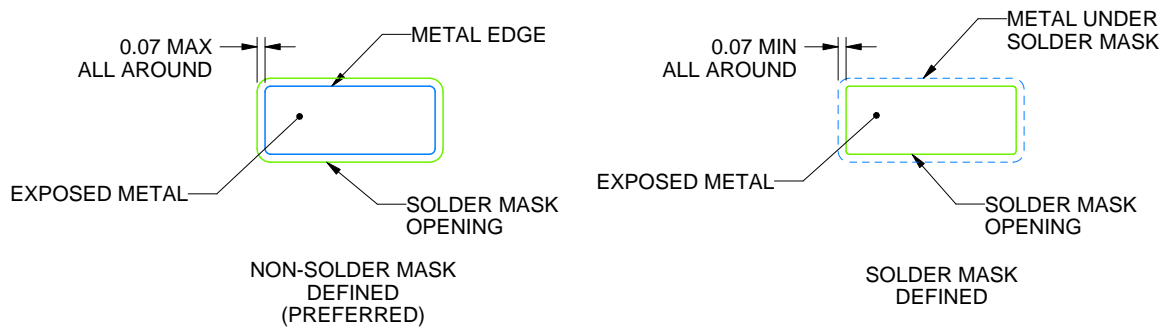
DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 7X



SOLDER MASK DETAILS

4227022/C 07/2024

NOTES: (continued)

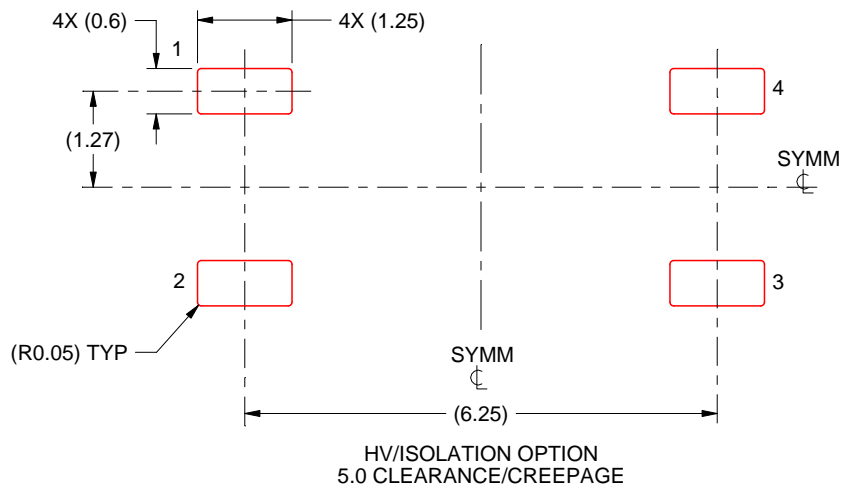
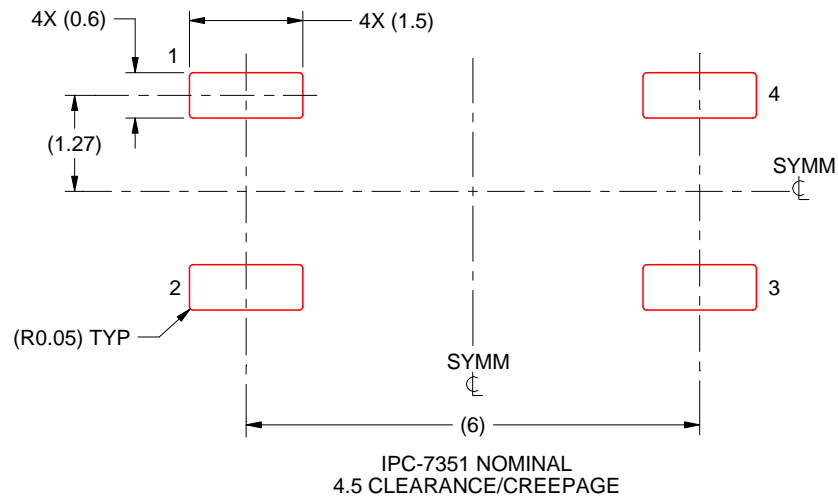
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4227022/C 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated