IWRL6432 WCSP Single-Chip 57 to 64GHz Industrial Radar Sensor

1 Features

- FMCW Transceiver
  - Integrated PLL, transmitter, receiver, baseband and ADC
  - 57GHz - 64GHz coverage with 7GHz continuous bandwidth
  - 3 receive channels and 2 transmit channels
  - Range typically up to 25m
  - 10dBm typical output power per Tx
  - 12dB Typical noise figure
  - -89dBc/Hz typical phase noise at 1MHz
  - FMCW operation
  - 5MHz IF bandwidth, real-only Rx channels
  - Ultra-accurate chirp engine based on fractional-N PLL
  - Per transmitter binary phase shifter
- Processing elements
  - Arm® M4F® core with single precision FPU (160MHz)
  - TI Radar Hardware Accelerator (HWA 1.2) for FFT, log magnitude, and CFAR operations (80MHz)
- Supports multiple low-power modes
  - Idle mode and deep sleep mode
- Power management
  - 1.8V and 3.3V IO support
  - Built-in LDO network for enhanced PSRR
  - BOM-Optimized and Power-Optimized modes
  - One or two power rails for 1.8V IO mode, two or three power rails for 3.3V IO mode

- Built-in calibration
  - Built-in *Firmware* (ROM)
  - Self-Contained on chip calibration system
- Host Interface
  - UART
  - CAN-FD
  - SPI
- RDIF (Radar Data Interface) for raw ADC sample capture
- Other interfaces available to user application
  - QSPI
  - I2C
  - JTAG
  - GPIOs
  - PWM Interface
- Internal memory
  - 1MB of On-Chip RAM
  - Configurable L3 shared memory for Radar Cube
  - Data and Code RAM of (512/640/768KB)
- WCSP package having 11 x 11 BGA grid, 111 BGA balls; Package size: 4.89mm x 4.5mm

- Clock source
  - 40.0MHz crystal for primary clock
  - Supports externally driven clock (Square/Sine) at 40.0MHz
  - 32kHz internal oscillator for low power operations
- Supports temperature operating range
  - Operating junction temperature range: –40°C to 105°C

2 Applications

- PC/Notebooks
- Portable electronics
- Televisions
- Tablets
- Earphones
- Smart watches
- Gaming
- Home theater & entertainment
- Automated door/gate
- Motion detector
- Occupancy detection / people tracking / people counting
- Video doorbell
- IP network camera
- Thermostat
- Air conditioner
- Refrigerators and freezers
- Vacuum robot
- Lawn mower

3 Description

The IWRL6432W mmWave Sensor device is an integrated single chip mmWave sensor based on FMCW radar technology. The device is capable of operation in the 57GHz to 63.9GHz band and is partitioned into mainly four power domains:

- **RF/Analog Sub-System**: This block includes all the RF and Analog components required to transmit and receive the RF signals.
- **Front-End Controller sub-System (FECSS)**: FECSS contains processor responsible for radar front-end configuration, control, and calibration.
- **Application Sub-System (APPSS)**: APPSS is where the device implements a user programmable ARM Cortex M4 allowing for custom control and automotive interface applications. Top Sub-System (TOPSS) is part of the APPSS power domain and contains the clocking and power management sub-blocks.
- **Hardware Accelerator (HWA)**: The HWA block supplements the APPSS by offloading common radar processing such as FFT, Constant False Alarm rate (CFAR), scaling, and compression.

The IWRL6432W is specifically designed to have separate control for each of the above-mentioned power domains to control the states (power ON or OFF) based on use case requirements. The device also features the capability to exercise various low-power states like sleep and deep sleep, where low-power sleep mode is achieved by clock gating and by turning off the internal IP blocks of the device. The device also provides the option of keeping some contents of the device, like Application image or RF profile retained in such scenarios.

Additionally, the device is built with TI's low power 45nm RF CMOS process and enables unprecedented levels of integration in an extremely small form factor. IWRL6432W is designed for low power, ultra-accurate radar systems in the industrial (and personal electronics) space for applications such as building/factory automation, commercial/residential security, personal electronics, presence/motion detection, and gesture detection/recognition for human machine interfaces

Table 3-1. Packaging Information

PRODUCTION PART NUMBER(1)	PACKAGE	BODY SIZE(2)	TRAY / TAPE AND REEL	DESCRIPTION
IWRL6432BDQGYFFR	YFF (WCSP, 111)	4.89mm x 4.5mm	Tape & Reel	Production; Deep sleep enabled; Generic Part
IWRL6432BDQAYFFR	YFF (WCSP, 111)	4.89mm x 4.5mm	Tape & Reel	Production; Deep sleep enabled; Authenticated boot capable

(1) For more information, see Device Nomenclature
(2) For more information, see Mechanical, Packaging, and Orderable Information

4 Functional Block Diagram

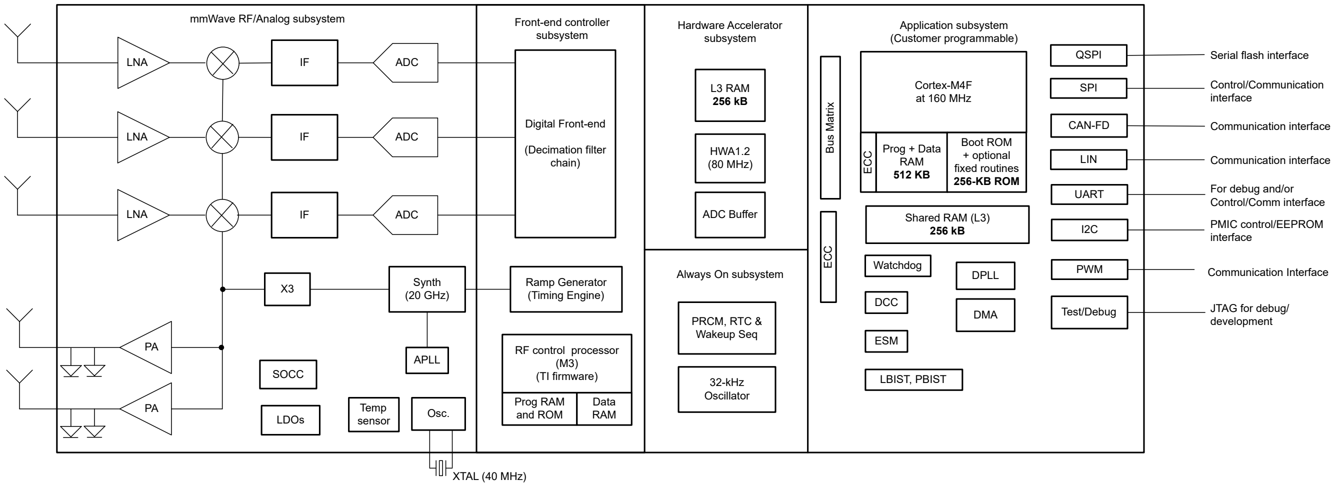

Figure 4-1. Functional Block Diagram

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5 Device Comparison

The following table compares the features of radar devices.

Table 5-1. Device Features Comparison

FUNCTION	IWRL6432 WCSP	IWRL6432AOP	IWRL6432	IWR6843AOP (1)	IWR6843 (1)	IWR6443	IWRL1432
Antenna on Package (AOP)	-	Yes	-	Yes	-	-	-
Number of receivers	3	3	3	4	4	4	3
Number of transmitters	2	2	2	3[2]	3[2]	3[2]	2
RF frequency range	57 to 64GHz	57 to 64GHz	57 to 64GHz	60 to 64 GHz	60 to 64 GHz	60 to 64GHz	76 to 81GHz
On-chip memory	1MB	1MB	1MB	1.75MB	1.75MB	1.4MB	1MB
Max I/F (Intermediate Frequency) (MHz)	5	5	5	10	10	10	5
Max real sampling rate (Msps)	12.5	12.5	12.5	25	25	25	12.5
Max complex sampling rate (Msps)	-	-	-	12.5	12.5	12.5	-
Safety and Security							
Functional Safety -Compliance	-	-	SIL-2 Targeted[3]	SIL-2	SIL-2	-	SIL-2 Targeted[3]
Device Security[4]	-	-	-	Yes	Yes	Yes	-
Processors							
MCU	M4F	M4F	M4F	R4F	R4F	R4F	M4F
DSP	-	-	-	C674x	C674x	-	-
HWA	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Peripherals							
Serial Peripheral Interface (SPI) ports	2	2	2	2	2	2	2
Quad Serial Peripheral Interface (QSPI)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Inter-Integrated Circuit (I^2C) interface	1	1	1	1	1	1	1
Controller Area Network (DCAN) interface	-	-	-	-	-	-	-

Table 5-1. Device Features Comparison (continued)

FUNCTION	IWRL6432 WCSP	IWRL6432AOP	IWRL6432	IWR6843AOP [(1)]	IWR6843 [(1)]	IWR6443	IWRL1432
Controller Area Network (CAN-FD) interface	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Trace	-	-	-	Yes	Yes	-	-
PWM	Yes	Yes	Yes	Yes	Yes	Yes	Yes
DMM Interface	-	-	-	Yes	Yes	Yes	-
Hardware In Loop (HIL/ DMM)	-	-	-	Yes	Yes	Yes	-
GPADC	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC Raw Data Capture	RDIF	RDIF	RDIF	LVDS	LVDS	LVDS	RDIF
UART	2	2	2	2	2	2	2
1V bypass mode	N/A	N/A	N/A	Yes	Yes	Yes	N/A
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Number of TX that can be used simultaneously	2	1	2	3	3	3	2
Per Chirp configurable TX phase shifter	BPM only	-	BPM only	Yes(5)	Yes(5)	Yes(5)	BPM only
Package Variant	WCSP	Under- Mount	FCCSP	Under- Mount	FCCSP	FCCSP	FCCSP
Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD(6)	AI	PD(6)	PD(6)	PD(6)	PD(6)	PD(6)

(1) Developed for Functional Safety applications, the device supports hardware integrity up to SIL-2. Refer to the related documentation for more details. Non-Functional Safety Variants are also available for these devices.
(2) 3 Tx Simultaneous operation on the applicable devices is supported only with 1V LDO bypass and PA LDO disable mode. In this mode, the 1V supply needs to be fed on the V_{OUT} PA pin.
(3) As the certification may get secured at different times and post certificate the target would be updated to "compliant" from "compliance targeted" only in related datasheets, please refer to the respective datasheets for most recent compliance status.
(4) Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.
(5) 6 bits linear Phase Shifter.
(6) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

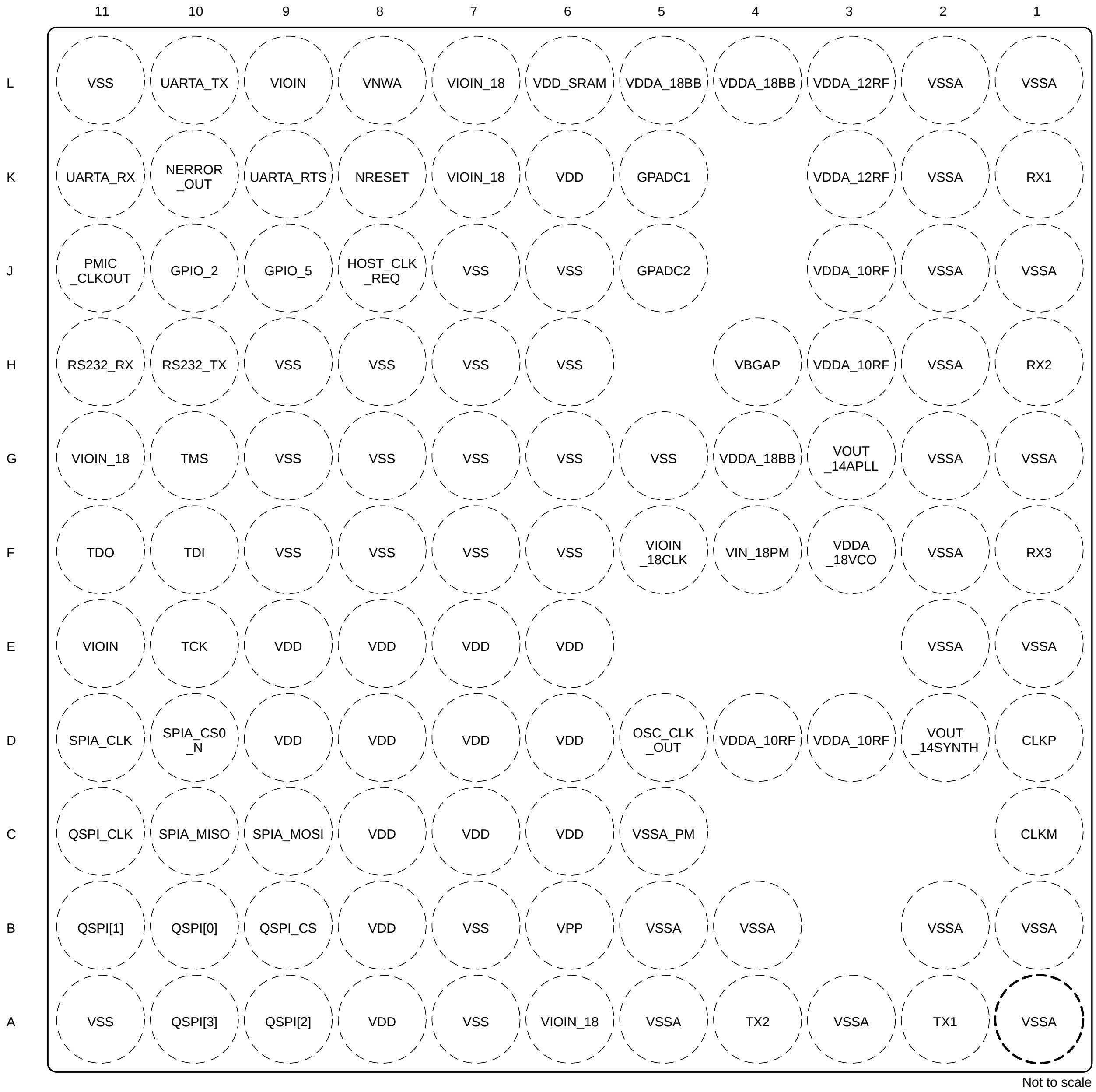
5.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave sensors	TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for Industrial applications.
mmWave IWR	The Texas Instruments IWRxxxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 57- to 64GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from short to ultra short range can be realized using these devices.
Companion products for IWRL6432WCSP	Review products that are similar to this product.
Reference designs for IWRL6432WCSP	The IWRL6432W TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/reference-designs.

6 Terminal Configurations and Functions

6.1 Pin Diagrams



	11	10	9	8	7	6	5	4	3	2	1
L	VSS	UARTA_TX	VIOIN	VNWA	VIOIN_18	VDD_SRAM	VDDA_18BB	VDDA_18BB	VDDA_12RF	VSSA	VSSA
K	UARTA_RX	NERROR_OUT	UARTA_RTS	NRESET	VIOIN_18	VDD	GPADC1		VDDA_12RF	VSSA	RX1
J	PMIC_CLKOUT	GPIO_2	GPIO_5	HOST_CLK_REQ	VSS	VSS	GPADC2		VDDA_10RF	VSSA	VSSA
H	RS232_RX	RS232_TX	VSS	VSS	VSS	VSS		VBGAP	VDDA_10RF	VSSA	RX2
G	VIOIN_18	TMS	VSS	VSS	VSS	VSS	VSS	VDDA_18BB	VOUT_14APLL	VSSA	VSSA
F	TDO	TDI	VSS	VSS	VSS	VSS	VIOIN_18CLK	VIN_18PM	VDDA_18VCO	VSSA	RX3
E	VIOIN	TCK	VDD	VDD	VDD	VDD				VSSA	VSSA
D	SPIA_CLK	SPIA_CS0_N	VDD	VDD	VDD	VDD	OSC_CLK_OUT	VDDA_10RF	VDDA_10RF	VOUT_14SYNTH	CLKP
C	QSPI_CLK	SPIA_MISO	SPIA_MOSI	VDD	VDD	VDD	VSSA_PM				CLKM
B	QSPI[1]	QSPI[0]	QSPI_CS	VDD	VSS	VPP	VSSA	VSSA		VSSA	VSSA
A	VSS	QSPI[3]	QSPI[2]	VDD	VSS	VIOIN_18	VSSA	TX2	VSSA	TX1	VSSA

Not to scale

Figure 6-1. WCSP Pin Diagram (Top View)

6.2 Signal Descriptions

Note

All digital IO pins of the device (except NRESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Table 6-1. Analog Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
CLKM	XTAL CLKM pin	A	C1
CLKP	XTAL CLKP pin	A	D1
GPADC1	GPADC input 1	A	K5
GPADC2	GPADC input 2	A	J5
NRESET	NRESET input	A	K8
OSC_CLK_OUT	Oscillator Clock output	A	D5
RX1	RX channel 1	A	K1
RX2	RX channel 2	A	H1
RX3	RX channel 3	A	F1
TX1	TX channel 1	A	A2
TX2	TX channel 2	A	A4
VBGAP	BandGap reference pin	A	H4

Table 6-2. CAN Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
CAN_FD_RX	CAN Receive Data	I	K11
CAN_FD_TX	CAN Transmit Data	O	L10

Table 6-3. Clock Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
MCU_CLKOUT	MCU clock output	O	J8, K10
PMIC_CLKOUT	PMIC clock output. This also serves as a Sense On Power Line. Impacts boot mode SOP1.	O	J11
RTC_CLK_IN	RTC clock input This is used as wakeup source for exiting from deep sleep. For more details, refer to the Technical Reference Manual	I	B11, G10, J10, K10,K9

Table 6-4. EPWM Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
EPWMA	EPWM Output A	O	C10, D10, F10, K9
EPWMB	EPWM Output B	O	C9, D11, E10, J9
EPWM_SYNC_IN	EPWM Sync Input	I	G10, H10, J9
EPWM_SYNC_OUT	EPWM Sync output	O	G10

Table 6-5. GPIO Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
GPIO_0	General Purpose Input/Output	IO	C9
GPIO_1	General Purpose Input/Output	IO	C10
GPIO_2	General Purpose Input/Output	IO	J10

Table 6-5. GPIO Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
GPIO_3	General Purpose Input/Output	IO	K11
GPIO_4	General Purpose Input/Output	IO	K10
GPIO_5	General Purpose Input/Output	IO	J9
GPIO_6	General Purpose Input/Output	IO	K9
GPIO_7	General Purpose Input/Output	IO	J8

Table 6-6. I2C Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
I2C_SCL	I2C Clock	IO	A9, D11, H10, J8, L10
I2C_SDA	I2C Data	IO	A10, D10, H11, J10, K11

Table 6-7. JTAG Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
TCK	JTAG Test Clock Input	I	E10
TDI	JTAG Test Data Input	I	F10
TDO	JTAG Test Data Output. Also serves as a Sense On Power [Reset] Line Impacts boot mode SOP0.	O	F11
TMS	JTAG Test Mode Select Input	I	G10

Table 6-8. LIN Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
LIN_RX	LIN Receive Data	I	H11, J10, J9, K11
LIN_TX	LIN Transmit Data	O	H10, J11, J8, K9, L10

Table 6-9. RDIF Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
RDIF_CLK	RDIF Clock	O	C11, D11, K9
RDIF_D0	RDIF data 0	O	B10, E10, J10
RDIF_D1	RDIF data 1	O	A9, C9, H10, K11
RDIF_D2	RDIF data 2	O	A10, C10, H11, L10
RDIF_D3	RDIF data 3	O	B11, D10, J8, J9, K10
RDIF_FRM_CLK	RDIF Frame Clock	O	B9, F11, J11, J8

Table 6-10. Power Supply Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
VDD	1.2V Core supply	PWR	A8, B8, C6, C7, C8, D6, D7, D8, D9, E6, E7, E8, E9, K6
VDDA_10RF	1.0V RF Supply (Routing resistance between the balls should be less than 15mOhm)	PWR	D3, D4, H3, J3
VDDA_12RF	1.2V RF Supply	PWR	K3, L3
VDDA_18BB	1.8V analog supply	PWR	G4, L4, L5
VDDA_18VCO	1.8V analog supply	PWR	F3
VDD_SRAM	1.2V SRAM supply	PWR	L6
VIN_18PM	1.8V core supply	PWR	F4

Table 6-10. Power Supply Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
VIOIN	1.8V analog supply	PWR	E11, L9
VIOIN_18	1.8V analog supply	PWR	A6, G11, K7, L7
VIOIN_18CLK	1.8V analog supply	PWR	F5
VNWA	1.2V VNWA supply	PWR	L8
VOUT_14APLL	1.4V analog cap (Internal LDO o/p. External Capacitor needed on this pin)	PWR	G3
VOUT_14SYNTH	1.4V analog cap (Internal LDO o/p. External Capacitor needed on this pin)	PWR	D2
VPP	1.8V VPP supply	PWR	B6
VSS	Ground	GND	A11, A7, B7, F6, F7, F8, F9, G5, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, L11
VSSA	Ground	GND	A1, A3, A5, B1, B2, B4, B5, E1, E2, F2, G1, G2, H2, J1, J2, K2, L1, L2
VSSA_PM	Ground	GND	C5

Table 6-11. QSPI Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
QSPI_D0	QSPI Data bit 0	IO	B10
QSPI_D1	QSPI Data bit 1	I	B11
QSPI_D2	QSPI Data bit 2	I	A9
QSPI_D3	QSPI Data bit 3	I	A10
QSPI_SCLK	QSPI clock	IO	C11
QSPI_CS	QSPI Chip select	O	B9

Table 6-12. RS232 Debug Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
RS232_RX	Debug UART (Operates as Bus Main) - Receive Signal	I	H11
RS232_TX	Debug UART (Operates as Bus Main) - Transmit Signal	O	H10

Table 6-13. SPIA Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
SPIA_CLK	SPIA Clock	IO	D11
SPIA_CS0_N	SPIA Chip Select 0	IO	D10
SPIA_MISO	SPIA MISO	IO	C10
SPIA_MOSI	SPIA MOSI	IO	C9

Table 6-14. SPIB Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
SPIB_CLK	SPIB Clock	IO	C11, D11, G10, K9
SPIB_CS0_N	SPIB Chip Select 0	IO	B9, D10, F10, K10
SPIB_MISO	SPIB MISO	IO	B11, C10, G10, H11, J8

Table 6-14. SPIB Signal Descriptions (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
SPIB_MOSI	SPIB MOSI	IO	B10, C9, E10, L10

Table 6-15. System Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
HOST_CLK_REQ	Host clock request output	O	J8
NERROR_OUT	NERROR output signal	O	K10
SYNC_IN	Sync input	I	A10, G10, J9, K10, K11
WARM_RESET_OUT	Warm reset output	O	G10, J10,
WU_REQIN	Wakeup Request input	I	A9, J10, J8, K10, K9, L10

Table 6-16. UARTA Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
UARTA_RTS	UARTA RTS output	O	K9
UARTA_RX	UARTA Receive Data	I	K11
UARTA_TX	UARTA Transmit Data	O	L10

Table 6-17. UARTB Signal Descriptions

SIGNAL NAME	DESCRIPTION	PIN TYPE	WCSP PIN
UARTB_RX	UARTB Receive Data	I	H11, K11
UARTB_TX	UARTB Transmit Data	O	H10, L10

Table 6-18. Pin Muxing Table

WCSP BALL NUMBER[1]	BALL NAME[2]	SIGNAL NAME[3]	PINCNTL REGISTER[4]	PIN CNTL REGISTER ADDRESS[5]	MODE[6]	TYPE[7]	POWER	PULL UP/DOWN TYPE[8]	BALL STATE DURING RST[9]	BALL STATE AFTER RST[10]
J10	GPIO_2	GPIO_2	PADAL_CFG_REG	0x5A00002C	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_RX			1	I				
		WARM_RESET_OUT			2	O				
		I2C_SDA			3	IO				
		SPIA_CS1_N			4	IO				
		WU_REQIN			5	I				
		RTC_CLK_IN			6	I				
		MDO_D0			7	O				
J9	GPIO_5	GPIO_5	PADAV_CFG_REG	0x5A000054	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SYNC_IN			1	I				
		LIN_RX			2	I				
		EPWMB			3	O				
		EPWM_SYNC_IN			4	I				
		MDO_D3			5	O				
J8	HOST_CLK_REQ	HOST_CLK_REQ	PADAX_CFG_REG	0x5A00005C	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/SS/OFF
		GPIO_7			1	IO				
		MCU_CLKOUT			2	O				
		LIN_TX			3	O				
		WU_REQIN			4	I				
		SPIB_MISO			5	IO				
		I2C_SCL			6	IO				
		MDO_D3			8	O				
		MDO_FRM_CLK			9	O				
K10	NERROR_OUT	NERROR_OUT	PADAU_CFG_REG	0x5A000050	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_4			1	IO				
		SYNC_IN			2	I				
		SPIB_CS0_N			3	IO				
		WU_REQIN			4	I				
		RTC_CLK_IN			5	I				
		MCU_CLKOUT			6	O				
		MDO_D3			7	O				
		PA_BLANK			9	I				

Table 6-18. Pin Muxing Table (continued)

WCSP BALL NUMBER[1]	BALL NAME[2]	SIGNAL NAME[3]	PINCNTL REGISTER[4]	PIN CNTL REGISTER ADDRESS [5]	MODE[6]	TYPE[7]	POWER	PULL UP/ DOWN TYPE[8]	BALL STATE DURING RST[9]	BALL STATE AFTER RST[10]
J11	PMIC_CLKOUT	PMIC_CLKOUT	PADAK_CFG_REG	0x5A00 0028	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_TX			1	O				
		SPIA_CS1_N			2	IO				
		MDO_FRM_CLK			3	O				
B10	QSPI[0]	QSPI[0]	PADAC_CFG_REG	0x5A00 0008	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_MOSI			1	IO				
		MDO_D0			2	O				
B11	QSPI[1]	QSPI[1]	PADAD_CFG_REG	0x5A00 000C	0	I	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_MISO			1	IO				
		RTC_CLK_IN			2	I				
		MDO_D3			3	O				
A9	QSPI[2]	QSPI[2]	PADAE_CFG_REG	0x5A00 0010	0	I	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		I2C_SCL			1	IO				
		WU_REQIN			2	I				
		MDO_D1			3	O				
A10	QSPI[3]	QSPI[3]	PADAF_CFG_REG	0x5A00 0014	0	I	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		I2C_SDA			1	IO				
		SYNC_IN			2	I				
		MDO_D2			3	O				
C11	QSPI_CLK	QSPI_CLK	PADAA_CFG_REG	0x5A00 0000	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_CLK			1	IO				
		MDO_CLK			2	O				
B9	QSPI_CS	QSPI_CS	PADAB_CFG_REG	0x5A00 0004	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		SPIB_CS0_N			1	IO				
		MDO_FRM_CLK			2	O				
H11	RS232_RX	RS232_RX	PADAP_CFG_REG	0x5A00 003C	0	I	vddshv	PU/PD	OFF/OFF/UP	OFF/OFF/UP
		I2C_SDA			1	IO				
		UARTB_RX			2	I				
		LIN_RX			3	I				
		MDO_D2			4	O				
		SPIB_MISO			5	IO				

Table 6-18. Pin Muxing Table (continued)

WCSP BALL NUMBER(1)	BALL NAME(2)	SIGNAL NAME(3)	PINCNTL REGISTER(4)	PIN CNTL REGISTER ADDRESS (5)	MODE(6)	TYPE(7)	POWER	PULL UP/ DOWN TYPE(8)	BALL STATE DURING RST(9)	BALL STATE AFTER RST(10)
H10	RS232_TX	RS232_TX	PADAO_CFG_REG	0x5A000038	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFFI
		I2C_SCL			1	IO				
		UARTB_TX			2	O				
		LIN_TX			3	O				
		EPWM_SYNC_IN			4	I				
		MDO_D1			5	O				
		SPIB_CS1_N			6	IO				
D11	SPIA_CLK	SPIA_CLK	PADAG_CFG_REG	0x5A000018	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		EPWMB			1	O				
		I2C_SCL			2	IO				
		SPIB_CLK			3	IO				
		MDO_CLK			4	O				
D10	SPIA_CS0_N	SPIA_CS0_N	PADAH_CFG_REG	0x5A00001C	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		EPWMA			1	O				
		I2C_SDA			2	IO				
		SPIB_CS0_N			3	IO				
		MDO_D3			4	O				
C10	SPIA_MISO	SPIA_MISO	PADAJ_CFG_REG	0x5A000024	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_1			1	IO				
		EPWMA			2	O				
		SPIB_MISO			3	IO				
		MDO_D2			4	O				
C9	SPIA_MOSI	SPIA_MOSI	PADAI_CFG_REG	0x5A000020	0	IO	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_0			1	IO				
		EPWMB			2	O				
		SPIB_MOSI			3	IO				
		MDO_D1			4	O				
E10	TCK	TCK	PADAT_CFG_REG	0x5A00004C	0	I	vddshv	PU/PD	OFF/OFF/DOWN	OFF/OFF/DOWN
		EPWMB			1	O				
		SPIB_CS1_N			2	IO				
		SPIB_MOSI			3	IO				
		MDO_D0			4	O				

Table 6-18. Pin Muxing Table (continued)

WCSP BALL NUMBER(1)	BALL NAME(2)	SIGNAL NAME(3)	PINCNTL REGISTER(4)	PIN CNTL REGISTER ADDRESS(5)	MODE(6)	TYPE(7)	POWER	PULL UP/ DOWN TYPE(8)	BALL STATE DURING RST(9)	BALL STATE AFTER RST(10)
F10	TDI	TDI	PADAR_CFG_REG	0x5A00 0044	0	I	vddshv	PU/PD	OFF/OFF/ DOWN	OFF/OFF/ DOWN
		EPWMA			1	O				
		SPIB_CS0_N			2	IO				
F11	TDO	TDO	PADAS_CFG_REG	0x5A00 0048	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		MDO_FRM_CLK			1	O				
G10	TMS	TMS	PADAQ_CFG_REG	0x5A00 0040	0	I	vddshv	PU/PD	OFF/OFF/UP	OFF/OFF/UP
		WARM_RESET_OUT			1	O				
		SPIA_CS1_N			2	IO				
		SYNC_IN			3	I				
		SPIB_MISO			4	IO				
		SPIB_CLK			5	IO				
		RTC_CLK_IN			6	I				
		EPWM_SYNC_IN			7	I				
		EPWM_SYNC_OUT			8	O				
K9	UARTA_RTS	UART_RTS	PAD_CFG_REG	0x5A00 0058	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_6			1	IO				
		LIN_TX			2	O				
		SPIB_CLK			3	IO				
		WU_REQIN			4	I				
		EPWMA			5	O				
		RTC_CLK_IN			6	I				
		MDO_CLK			7	O				
		PA_BLANK			9	I				
K11	UARTA_RX	UARTA_RX	PADAM_CFG_REG	0x5A00 0030	0	I	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		GPIO_3			1	IO				
		LIN_RX			2	I				
		CAN_FD_RX			3	I				
		SYNC_IN			4	I				
		UARTB_RX			5	I				
		I2C_SDA			6	IO				
		MDO_D1			7	O				

Table 6-18. Pin Muxing Table (continued)

WCSP BALL NUMBER(1)	BALL NAME(2)	SIGNAL NAME(3)	PINCNTL REGISTER(4)	PIN CNTL REGISTER ADDRESS (5)	MODE(6)	TYPE(7)	POWER	PULL UP/ DOWN TYPE(8)	BALL STATE DURING RST(9)	BALL STATE AFTER RST(10)
L10	UARTA_TX	UARTA_TX	PADAN_CFG_REG	0x5A00 0034	0	O	vddshv	PU/PD	OFF/OFF/OFF	OFF/OFF/OFF
		LIN_TX			1	O				
		CAN_FC_TX			2	O				
		SPIB_MOSI			3	IO				
		WU_REQIN			4	I				
		UARTB_TX			5	O				
		I2C_SCL			6	IO				
		MDO_D2			7	O				

(1) **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
(2) **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
(3) **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
(4) **PINCNTL_REGISTER:** APPSS Register name for PinMux Control
(5) **PINCNTL ADDRESS:** APPSS Address for PinMux Control
(6) **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
(7) **TYPE:** Signal type and direction:

- I = Input
- O = Output
- IO = Input or Output

(8) **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- Pull Up: Internal pullup
- Pull Down: Internal pulldown
- An empty box means No pull.

(9) **BALL STATE DURING RST**: State of Ball during reset in the format of RX/TX/Pull Status

- RX (Input buffer)
  - Off: The input buffer is **disabled**.
  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- Pull Status (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

(10) **BALL STATE AFTER RST**: State of Ball after reset in the format of RX/TX/Pull Status

- RX (Input buffer)
  - Off: The input buffer is **disabled**.
  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - SS: The subsystem selected with MUXMODE determines the output buffer state.
- Pull status (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up resistor** is turned on.
  - Down: Internal **pull-down resistor** is turned on.
  - NA: No internal pull resistor.
- An empty box, NA, or "-" means Not Applicable.

7 Specifications

7.1 Absolute Maximum Ratings

PARAMETERS(1) (2)		MIN	MAX	UNIT
VDD	1.2Vdigital power supply	–0.5	1.4	V
VIOIN	I/O supply (3.3Vor 1.8 V): All CMOS I/Os operate on the same VIOIN voltage level	–0.5	3.8	V
VIOIN_18	1.8Vsupply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8Vsupply for clock module	–0.5	2	V
VIN_18BB	1.8V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8V RF VCO supply	–0.5	2	V
VPP	Voltage supply for fuse chain	-0.5	2	V
RX1-3	Externally applied power on RF inputs		10	dBm
TX1-2	Externally applied power on RF outputs(3)		10	dBm
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3Vor 1.8V(Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8V(Transient Overshoot/Undershoot) or external oscillator input		VIOIN + 20% up to 20% of signal period	
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3Vabove or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	105	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ ESDA/JEDEC JS-001 (1)	All Pins	±1000	V
		Charged-device model (CDM), per ANSI/ ESDA/JEDEC JS-002 (2)	All Pins	±500	
			Corner Pins	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j)(1)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
105°C T_j	50% RF duty cycle	1.2	100,000

1. This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	1.2Vdigital power supply	1.14	1.2	1.26	V
VIOIN	I/O supply (3.3V or 1.8V): All CMOS I/Os can operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8Vsupply for CMOS IO	1.71	1.8	1.89	V
VIN_18CLK	1.8Vsupply for clock module	1.71	1.8	1.89	V
VIN18BB	1.8V Analog baseband power supply	1.71	1.8	1.89	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.89	V
V_{IH}	Voltage Input High (1.8Vmode)	1.17			V
	Voltage Input High (3.3Vmode)	2.25			
V_{IL}	Voltage Input Low (1.8Vmode)			0.3*VIOIN	V
	Voltage Input Low (3.3Vmode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6mA)			450	mV
NRESET SOP[1:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

7.5 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for authenticated boot devices. During the process of writing the customer specific keys or other fields like software version etc. in the efuse, the user needs to provide the VPP supply.

7.5.1 Recommended Operating Conditions for OTP eFuse Programming

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VPP	Supply voltage range for the eFuse ROM domain during normal operation		NC(2)		
	Supply voltage range for the eFuse ROM domain during OTP programming (1)	1.65	1.7	1.75	V
Duration of VPP Supply	If VPP voltage is supplied for more than recommended Hours, it can cause reliability issue			24	Hours
I(VPP)				50	mA

(1) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the external regulator attached to the VPP terminal.

(2) NC: No Connect

Note

Power up sequence: VPP must be ramped up at the end i.e after all other rails ramp up is done

7.5.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.

7.5.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, in these cases of faulty EFUSE programmability, TI WILL HAVE NO LIABILITY.

7.6 Power Supply Specifications

7.6.1 Power Optimized 3.3V I/O Topology

Table 7-1 describes the power rails from an external power supply block to the device via a 3.3V I/O topology.

Table 7-1. Power Supply Rails Characteristics: Power Optimized 3.3V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
3.3V	Digital I/Os	Input: VIOIN
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.2V	Core Digital and SRAMs, RF, VNWA	Input: VDD, VDD_SRAM, VNWA, VDDA_12RF LDO Output: VDDA_10RF

7.6.2 BOM Optimized 3.3V I/O Topology

Table 7-2 describes the power rails from an external power supply block to the device via a BOM Optimized 3.3V I/O Topology.

Table 7-2. Power Supply Rails Characteristics: BOM Optimized 3.3V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
3.3V	Digital I/Os	Input: VIOIN
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM LDO Output: VOUT_14SYNTH, VDDA_10RF, VDD_SRAM, VNWA, VOUT_14APLL, VDDA_12RF, VDD,

7.6.3 Power Optimized 1.8V I/O Topology

Table 7-3 describes the power rails from an external power supply block to the device via a power optimized 1.8V I/O topology.

Table 7-3. Power Supply Rails Characteristics: Power Optimized 1.8V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC	Input: VIOIN, VIN_18PM, VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.2V	Core Digital and SRAMs, RF, VNWA	Input: VDD, VDD_SRAM, VNWA,VDDA_12RF LDO Output: VDDA_10RF

7.6.4 BOM Optimized 1.8V I/O Topology

Table 7-4 describes the power rails from an external power supply block to the device via a BOM optimized 1.8V I/O topology.

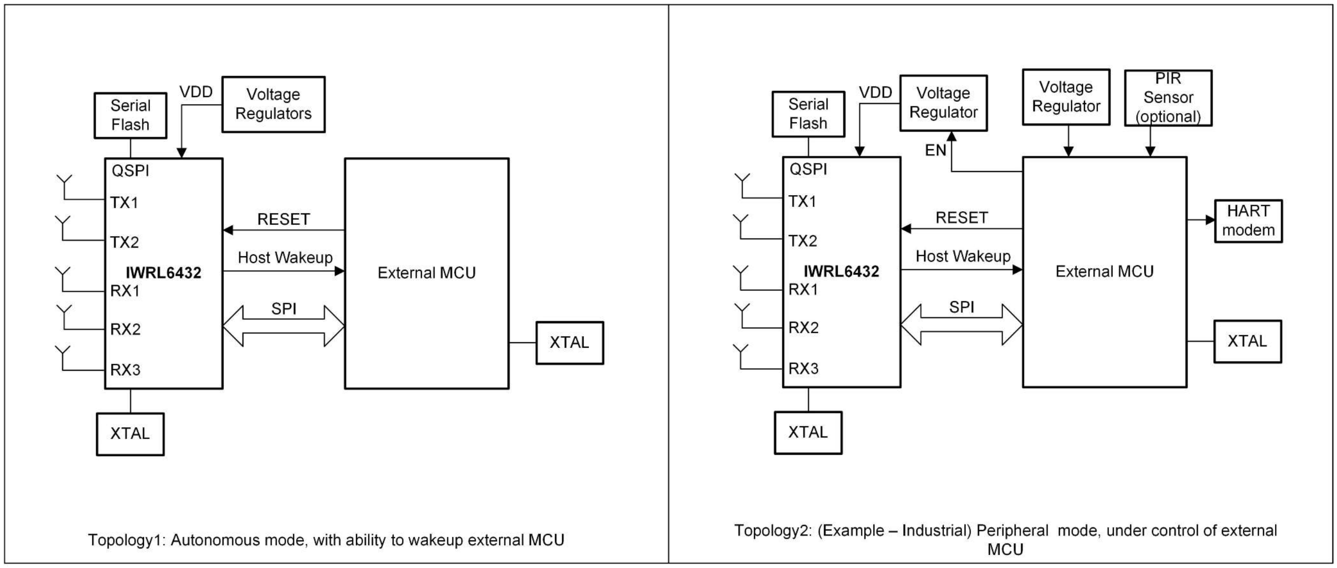
Table 7-4. Power Supply Rails Characteristics: BOM Optimized 1.8V I/O Topology

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOs IN THE DEVICE
1.8V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, Digital I/Os	Input: VIOIN, VDDA_18VCO, VIOIN_18CLK, VIOIN_18, VDDA_18BB, VIN_18PM, VDDA_18VCO LDO Output: VDD, VDD_SRAM, VNWA, VDDA_10RF, VDDA_12RF, VOUT_14APLL, VOUT_14SYNTH

7.6.5 System Topologies

The following the system topologies are supported.

- Topology 1: Autonomous mode, with ability to wake-up external MCU
- Topology 2: Peripheral mode, under control of external MCU



Topology1: Autonomous mode, with ability to wakeup external MCU

Topology2: (Example – Industrial) Peripheral mode, under control of external MCU

Figure 7-1. System Topologies

In Topology 1: Autonomous mode, the IWRL6432W can be used as full sensor along with M4F application processor. In this case the internal application processor does all the processing and interrupts the host processor to communicate to take action based on the sensor data. Most of the processing happens on the *internal* MCU of the IWRL6432W chip and only high level desired results are communicated to external host. In this topology MIPS, processing capability on the external MCU is relaxed and very low cost and low power MCU can be used.

In Topology 2: Peripheral mode, the IWRL6432W is controlled by an *external* MCU and most of the processing is done on an external MCU. In this case, computational and power requirements are higher and the external MCU stays active most of the time.

7.6.5.1 Power Topologies

The device supports two unique power topologies for BOM optimized and Power Optimized modes. The tables above, from Section 7.6.1 to Section 7.6.4, summarize these options.Two power topologies come into account based on whether the 1.2V rail is generated internally or is provided externally.

In BOM optimized mode the device can be powered up using one rail (1.8V) or two rails (3.3V and a 1.8V) provided externally. The 1.2V rail is internally generated in BOM optimized topology.

In power optimized mode, the device can either be powered using two rails (1.8V and 1.2V) or with three rails (3.3V, 1.8V and 1.2V), all provided externally. The 1.2V rail is NOT internally generated in the Power optimized topology. The device senses the external 1.2V supply and decides which topology the device will operate on.

7.6.5.1.1 BOM Optimized Mode

In this mode, the device can be powered using a 1.8V regulator OR using a 3.3V and a 1.8V regulator mode. The choice of one rail vs two rails is dependent on the IO voltages needed.

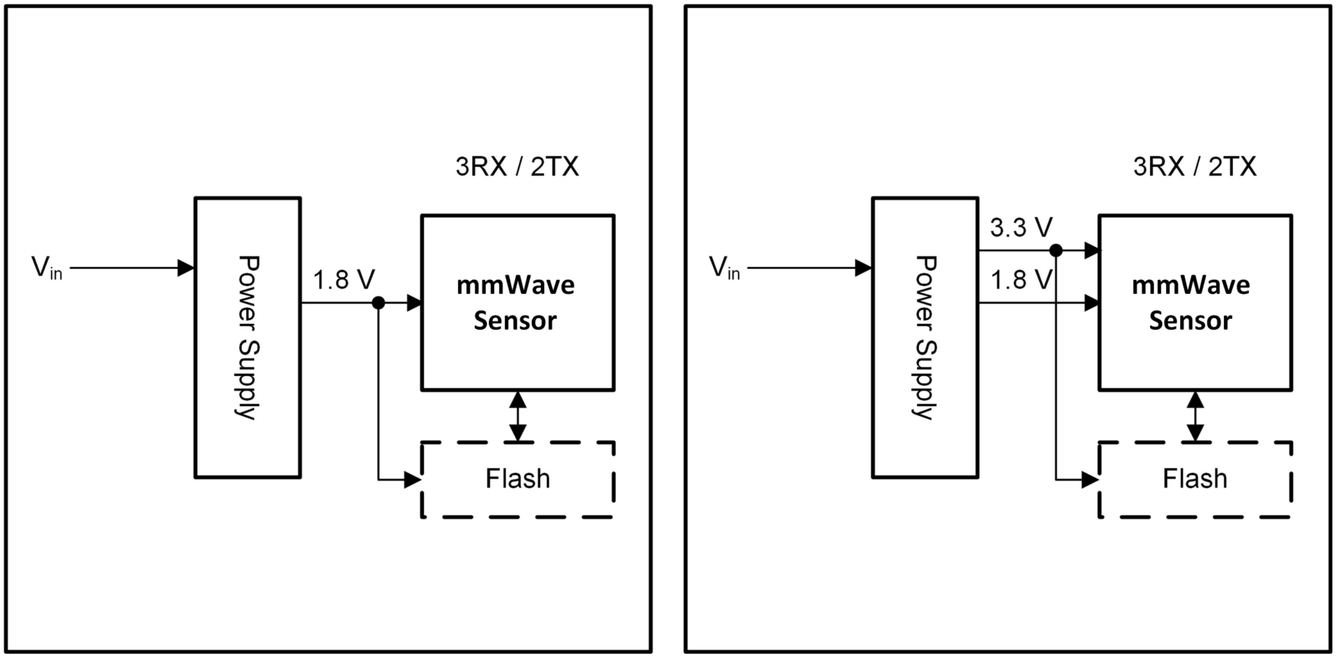


Figure 7-2. BOM Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.6.5.1.2 Power Optimized Mode

This mode is designed for applications needing ultra-low power applications. The device can either be powered using two rails (1.8V and 1.2V) or with three rails (3.3V, 1.8V and 1.2V).

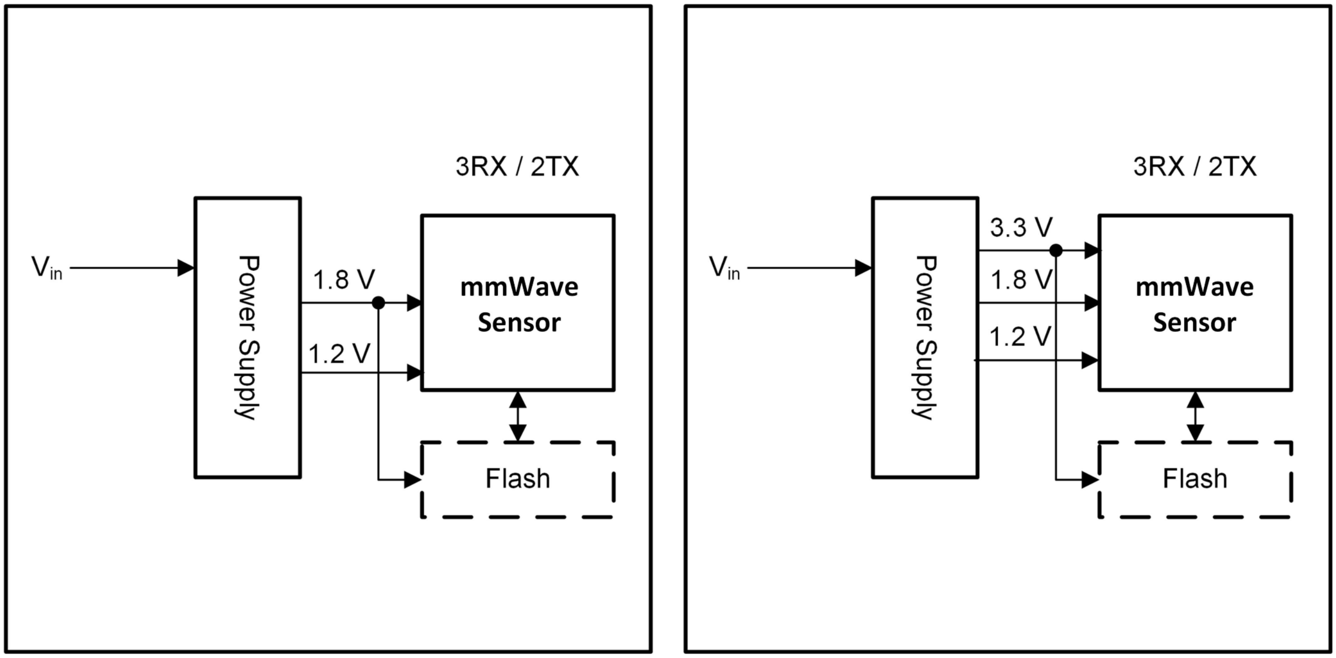


Figure 7-3. Power Optimized Mode Power Management (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.6.6 Internal LDO output decoupling capacitor and layout conditions for BOM optimized topology

This section depicts the recommended values of de-coupling capacitors and range of allowable parasitic inductance and resistance in particular sections of the output path for the internal LDOs. Like all low dropout regulators, the internal LDO requires an output capacitor connected between OUTPUT and GND to stabilize the internal control loop. We recommended using X7R type capacitors which have a low variation across temperature. The minimum and maximum values of the capacitor captured in the table below. The table includes variation of a given capacitor due to DC bias, tolerance and temperature variation.

Note

1. If the parasitic values are not kept within the specified range, performance of the device can degrade.
2. Typical values of de-coupling capacitors are recommended to use. Any capacitance value taken near the edge of the range can degrade the performance. The working range of the chosen capacitor can not exceed the specified range.

7.6.6.1 Single-Capacitor Rail

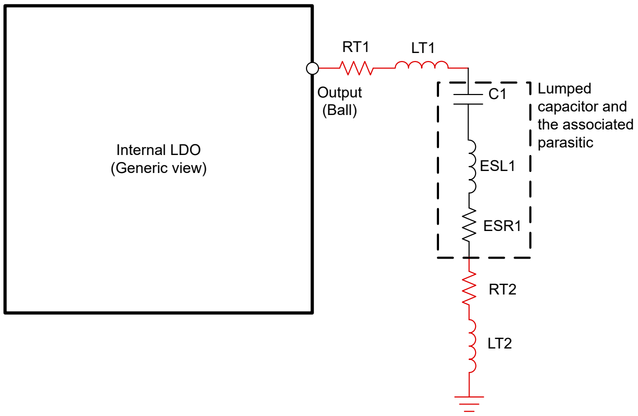


Figure 7-4. Parasitic offered by different portion of the output path (for one capacitor)

The 1.2V Digital LDO requires one decoupling capacitor with a typical value of 4.7uF. The parasitics offered by different portions of the output path is illustrated in Figure 7-4. “RT1” and “RT2” are the parasitic resistances offered by the ball to capacitor lead trace and the ground trace respectively. Similarly, “LT1” and “LT2” are parasitic inductances offered by the ball to capacitor lead trace and the ground trace respectively. “ESL1” and “ESR1” are the effective series inductance and resistance of the decoupling capacitor. Table 7-5 gives the minimum, maximum and typical values of the capacitance and the parasitics.

7.6.6.1.1 1.2V Digital LDO

Ball name: VDD

Table 7-5. 1.2V Dig LDO Output

	Min	Typ	Max	Unit
Recommended value of C	3.6	4.7	5.2	uF
Allowed output parasitic inductance Lp (1)	1	1.5	2	nH
Allowed output parasitic resistance Rp (2)	15	20	35	mOhm

(1) Lp = LT1 + ESL1 + LT2
(2) Rp = RT1 + ESR1 + RT2

7.6.6.2 Two-capacitor rail

The 1.2V RF LDO, 1.2V SRAM LDO and 1.0V RF LDO require two decoupling capacitors with typical values of 10uF and 2.2uF.

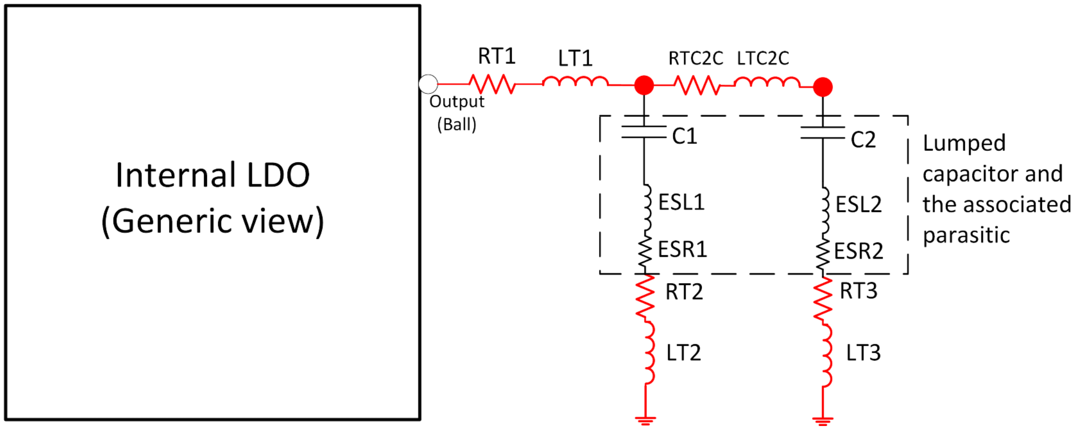


Figure 7-5. Parasitic offered by different portion of the output path (for two capacitors)

The parasitics offered by different portions of the output path is illustrated in Figure 7-5. As shown in figure Figure 7-5, the output path can be divided into four portions:

Ball to first capacitor: “RT1” and “LT1” are the parasitic resistance and inductance offered by the ball to the first capacitor lead.

Along the first capacitor: “ESL1” and “ESR1” are the effective series inductance and resistance of the first decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the first capacitor ground trace.

First capacitor lead to second capacitor lead: “RTC2C” and “LTC2C” are the resistance and inductance of the trace between two capacitors.

Along the second capacitor: “ESL2” and “ESR2” are the effective series inductance and resistance of the second decoupling capacitor. “RT3” and “LT3” are the ground trace resistance and inductance respectively of the second capacitor ground trace.

Note

Both the capacitors are recommended to be placed close to the respective ball.

7.6.6.2.1 1.2V RF LDO

Ball name: VDDA_12RF

Table 7-6. 1.2V RF LDO Output

		Min	Typ	Max	Unit
Recommended value(s) of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.3		0.6	nH
	Along 1st Capacitor (ESL1 + LT2)	0.4		0.7	
	Between two Capacitor leads (LTC2C)	0.1		0.3	
	Along the 2nd Capacitor (ESL2 + LT3)	0.4		0.7	

Table 7-6. 1.2V RF LDO Output (continued)

		Min	Typ	Max	Unit
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)	1		5	mOhm
	Along 1st Capacitor (ESR1 + RT2)	15		25	
	Between two Capacitor leads (RTC2C)	1		5	
	Along the 2nd Capacitor (ESR2 + RT3)	15		25	

7.6.6.2.2 1.2V SRAM LDO

Ball name: VDD_SRAM

Table 7-7. 1.2V SRAM LDO Output

		Min	Typ	Max	Unit
Recommended value(s) of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.5		1.0	nH
	Along 1st Capacitor (ESL1 + LT2)	1.0		1.5	
	Between two Capacitor leads (LTC2C)	0.5		1.0	
	Along the 2nd Capacitor (ESL2 + LT3)	1.0		1.5	
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)			1	mOhm
	Along 1st Capacitor (ESR1 + RT2)	15		35	
	Between two Capacitor leads (RTC2C)			1	
	Along the 2nd Capacitor (ESR2 + RT3)	15		35	

7.6.6.2.3 1.0V RF LDO

Ball name: VDDA_10RF

Table 7-8. 1.0V RF LDO Output

		Min	Typ	Max	Unit
Recommended value(s) of C	C1	4.9	10.0	11.0	uF
	C2	1.3	2.2	2.4	uF
Allowed output parasitic inductance	Ball to 1st Capacitor lead (LT1)	0.3	0.3	0.6	nH
	Along 1st Capacitor (ESL1 + LT2)	0.3		1.0	
	Between two Capacitor leads (LTC2C)	0.1		0.3	
	Along the 2nd Capacitor (ESL2 + LT3)	0.3		1.0	
Allowed output parasitic resistance	Ball to 1st Capacitor lead (RT1)	1		5	mOhm
	Along 1st Capacitor (ESR1 + RT2)	15		25	
	Between two Capacitor leads (RTC2C)	1		5	
	Along the 2nd Capacitor (ESR2 + RT3)	15		25	

7.6.7 Noise and Ripple Specifications

The 1.8V power supply ripple specifications mentioned in Table 7-9 are defined to meet a target spur level of –105dBc (RF Pin = –15dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1-dB increase in supply ripple leads to a ~1dB increase in spur level. Values quoted are peak-peak levels for a sinusoidal input applied at the specified frequency.

Table 7-9. Noise and Ripple Specifications

FREQ (kHZ)	NOISE SPECIFICATION		RIPPLE SPECIFICATION	
	1.8V(µV/√Hz)	1.2V (µV/√Hz)(1)	1.8V(mVpp)	1.2V (mVpp)(1)
10	6.057	44.987	0.035	1.996
100	2.677	26.801	0.760	2.233
200	2.388	28.393	0.955	3.116
500	0.757	9.559	0.504	1.152
1000	0.419	1.182	0.379	0.532
2000	0.179	1.256	0.153	0.561
5000	0.0798	0.667	0.079	0.297
10000	0.0178	0.104	0.017	0.046

(1) 1.2V noise/ripple specification is only for power optimized supply configurations. For BOM optimized topology 1.2V noise/ripple specification is not applicable.

Note

Same 1.8V noise/ripple specification is applicable for the 1.8V supply in the BOM optimized topology

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7.7 Power Save Modes

Table 7-10 lists the supported power states.

Table 7-10. Device Power States

Power State	Details
Active	Active Power State is when RF/chirping activity is ongoing
Processing	Processing Power State is when data is being processed RF turned off(1)
Idle	Idle Power State is during inter-frame/inter-burst/inter-chirp idle time
Deep Sleep	Lowest possible power state of the device where the contents of the device can be retained (Application Image, Chirp Profile etc) and device need not boot from scratch again. Device can enter this state after the frame processing is complete in order to save power significantly. Deep sleep exit can be through a number of external wakeup sources and internal timing maintenance.

(1) The power consumed here also includes the Hardware Accelerator Power Consumption.

7.7.1 Typical Power Consumption Numbers

Table 7-11 and Table 7-12 lists the typical power consumption for each power save modes in different power topologies and antenna configurations for a nominal device at 25C ambient temperature and nominal voltage conditions.

Table 7-11. Estimated Power Consumed in 3.3V IO Mode

Power Mode		Power Consumption (mW)	
		Power Optimized Mode	BOM Optimized Mode
Active (2TX, 3RX)	Sampling: 12.5 MSps, Start freq = 60GHz BW = 2GHz RX gain = 30dB TX back off = 0dB	960	1290
Active (2TX, 2RX)		870	1180
Active (1TX, 2RX)		720	950
Active (1TX, 1RX)		690	910
Processing	Major motion SDK OOB chain is used for measurement.	80	120
Idle	APPSS CM4 = 20MHz, FECSS, HWA powered off, SPI active	11.2	19.0
Deep sleep	Memory Retained = 114KB	0.66	0.67

Table 7-12. Estimated Power Consumed in 1.8V IO Mode

Power Mode		**Power Consumption (mW)**	
		Power Optimized Mode	**BOM Optimized Mode**
Active (2TX, 3RX)	Sampling: 12.5 MSps, Start freq = 60GHz BW = 2GHz RX gain = 30dB TX back off = 0dB	960	1290
Active (2TX, 2RX)		870	1180
Active (1TX, 2RX)		720	950
Active (1TX, 1RX)		690	910
Processing	Major motion SDK OOB chain is used for measurement.	80	120
Idle	APPSS CM4 = 20MHz, FECSS, HWA powered off, SPI active	10.9	18.6
Deep Sleep	Memory Retained = 114KB	0.48	0.48

Table 7-13. Use-Case Power Consumed in 3.3V Power Optimized Topology

Parameter		**Condition**	**Typical (mW)**
Average Power Consumption (Presence Detection -Major Motion)	**RF Front End Configuration :** 1TX, 1RX ADC Sampling Rate = 12.5Msps Ramp End time = 25us Chirp Idle Time = 6us Chirp Slope = 35MHz/us Number of chirps per burst = 10 Burst Periodicity = 300us Number of bursts per frame = 1 Device configured to go to deep sleep state after active operation. Memory Retained in deep sleep = 114KB	1Hz Update Rate	1.2

7.8 Peak Current Requirement per Voltage Rail

Table 7-14 provides the max split rail current numbers.

Table 7-14. Maximum Peak Current per Voltage Rail

Mode(1)	**IO Voltage**(3)	**Maximum Current (mA)** (2)		
		1.2V: total current drawn by all nodes driven by 1.2V rail	1.8V: total current drawn by all nodes driven by 1.8V rail	3.3V: total current drawn by all nodes driven by 3.3V rail
BOM Optimized	3.3V	NA	1360	90
BOM Optimized	1.8V	NA	1450	NA
Power Optimized	3.3V	1100	270	90
Power Optimized	1.8V	1100	360	NA

(1) Exercise full functionality of device, including operation, HWA, M4F and various host comm/interface peripherals active (CAN, I2C, GPADC), test across full temperature range
(2) The specified current values are at typical supply voltage level.
(3) The exact VIOIN current depends on the peripherals used and the frequency of operation.

7.9 RF Specification

Over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure	57 to 63.9GHz		12		dB
	1-dB compression point (Out Of Band)(1)			–9		dBm
	Maximum gain			40		dB
	Gain range			10		dB
	Gain step size			2		dB
	IF bandwidth(2)				5	MHz
	ADC sampling rate (real)				12.5	Msps
	ADC resolution			12		Bits
	S11(3)			-8		dB
Transmitter	Output Power			10		dBm
	Power backoff range			15		dB
	S11(3)			-8		dB
Clock subsystem	Frequency range		57		63.9	GHz
	Ramp rate				400	MHz/µs
	Phase noise at 1MHz offset	57 to 63.9GHz		–89		dBc/Hz

(1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone well below the lowest HPF cut-off frequency.

(2) The analog IF stages include high-pass filtering, with configurable first-order high-pass corner frequency. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)
175, 350, 700, 1400

The filtering performed by the digital baseband chain is targeted to provide less than ±0.5dB pass-band ripple/droop.

(3) RX3 and TX1 channels show degraded S11 (-5.5dB) compared to the rest of the channels due to impedance mismatch in the die to package transition.

Figure 7-6 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

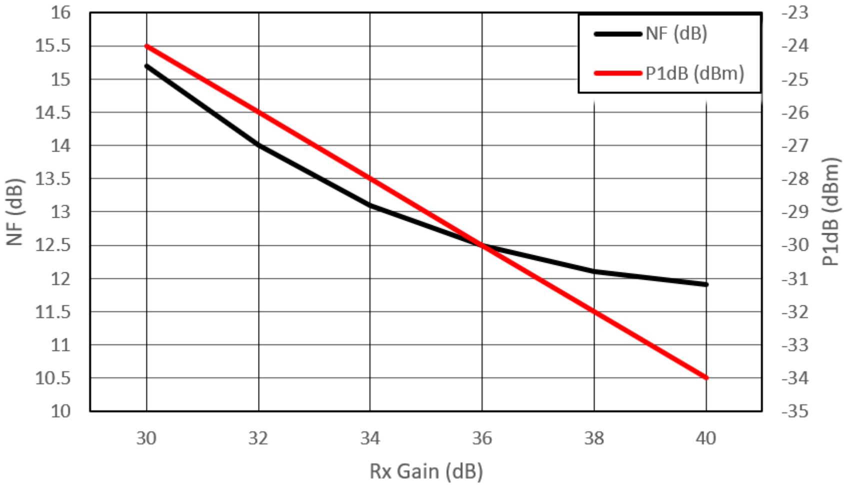
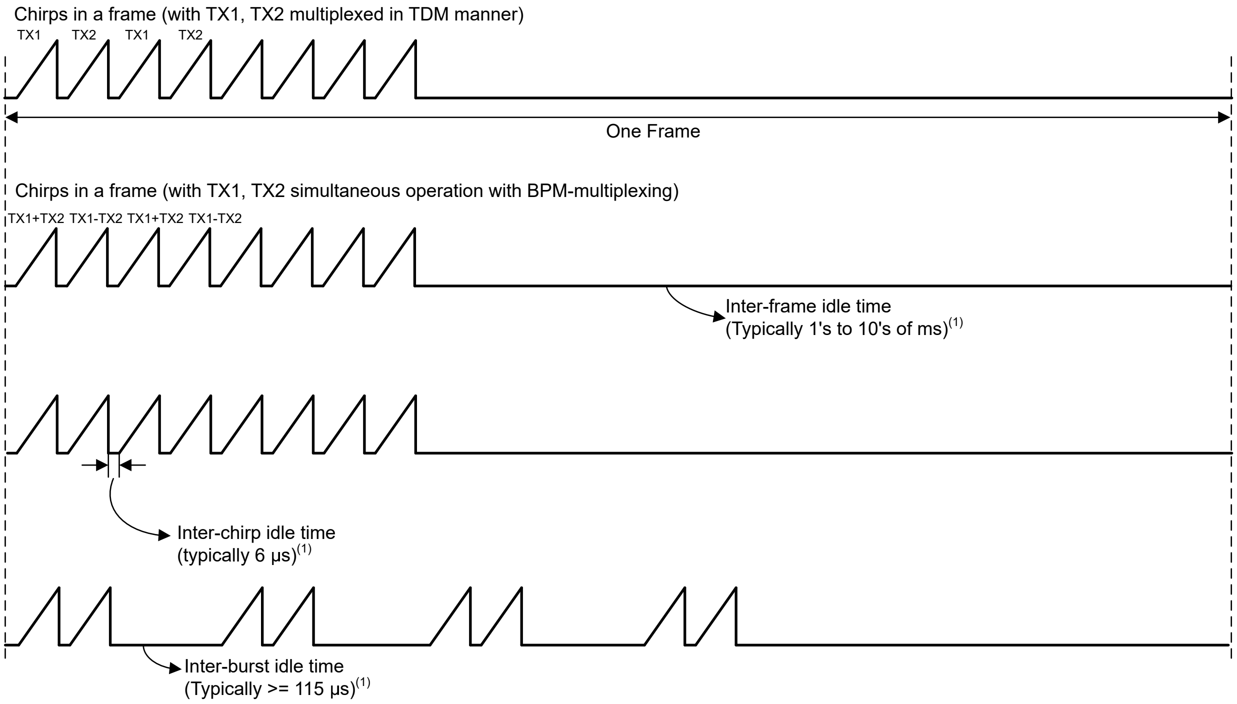


Figure 7-6. Noise Figure, In-band P1dB vs Receiver Gain

7.10 Supported DFE Features

- TX output back-off
  - TX back-off is supported from 0dB to 15dB in 1dB steps
  -
  - Binary Phase Modulation is supported on each TX
- RX gain
  - Real only RX channels
  - Total RX gain range of 30 dB to 40dB, in 2dB steps
- VCO
  - Single VCO covering entire RF sweep bandwidth up to 7GHz.
- High-pass filter
  - Supports corner frequency options: 175kHz, 350kHz, 700kHz, 1400kHz
  - First-order high pass filter only
- Low-pass filter
  - Max IF bandwidth supported is 5MHz
  - 40dB stopband rejection, two filtering options supported
  - 90% visibility – IF bandwidth is 90% of Nyquist (has longer setting time due to larger filter length)
  - 80% visibility – IF bandwidth is 80% of Nyquist and is 30% faster due to quicker settling time, compared with 90% visibility
- Supported ADC sampling rates
  - 1.0, 1.25, 1.667, 2.0, 2.5, 4.0, 5.0, 6.667, 7.692, 10.0, 12.5Msps
- Timing Engine
  - Support for chirps, bursts and frames
    - Longer frame idle time gives more power saving than a longer burst idle time. Further, a longer chirp idle time gives lesser power saving than a longer burst idle time. For more details please refer power calculator in the mmWave sensing estimator.
    - Chirp accumulation (averaging) possible across closely spaced chirps to reduce memory requirement
  - Provision for per-chirp dithering of parameters



1. Refer to DFP API documentation

Figure 7-7. Chip Profile Supported by Timing Engine

7.11 CPU Specifications

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TYP	UNIT
Application Subsystem (M4F Family)	Clock Speed	160	MHz
	Tightly Coupled Memory - A (Program + Data)	512	KB
Shared Memory	Shared L3 Memory(1)	256	KB
	L3 Memory dedicated for HWA	256	KB

(1) L3 memory is configurable

7.12 Thermal Resistance Characteristics

Table 7-15. Thermal Resistance Characteristics for WCSP Package [YFF0111-C01]

THERMAL METRICS(1) (4)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	0.11
$R\Theta_{JB}$	Junction-to-board	3.9
$R\Theta_{JA}$	Junction-to-free air	21.8
Psi_{JC}	Junction-to-package top	0.6
Psi_{JB}	Junction-to-board	3.8

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

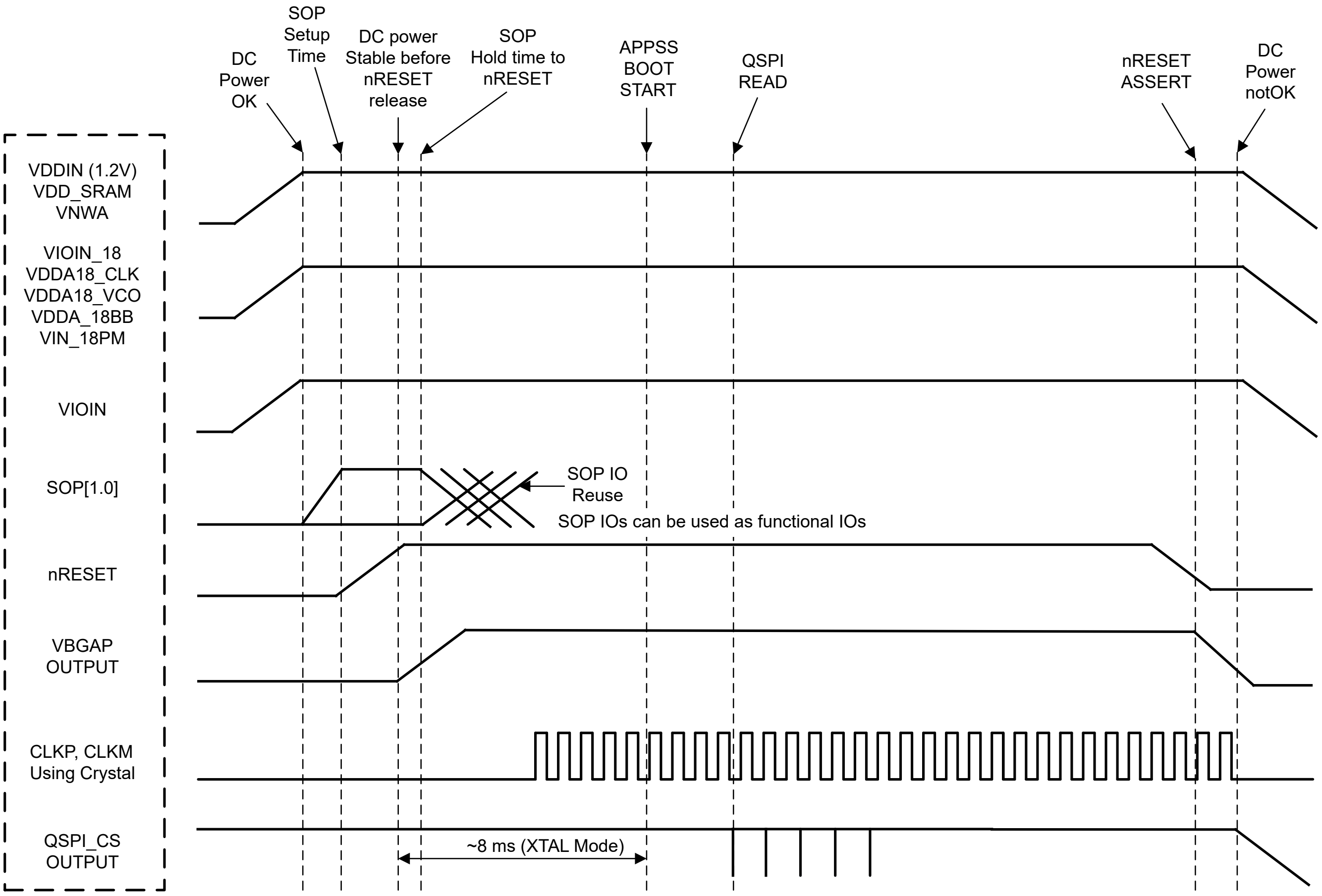
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(4) Test Condition: Power=1.305W at 25°C

7.13 Timing and Switching Characteristics

7.13.1 Power Supply Sequencing and Reset Timing

The IWRL6432W device expects all external voltage rails to be stable before reset is deasserted. Figure 7-8 describes the device wake-up sequence.



A. MCU_CLK_OUT in autonomous mode, where IWRL6432W application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 7-8. Device Wake-up Sequence

7.13.2 Synchronized Frame Triggering

The IWRL6432W device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. A software API trigger must be provided to set up the device for the hardware SYNC_IN trigger. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

The periodicity of the external SYNC_IN pulse should be always greater than the programmed frame periodicity in the frame configurations in all instances.

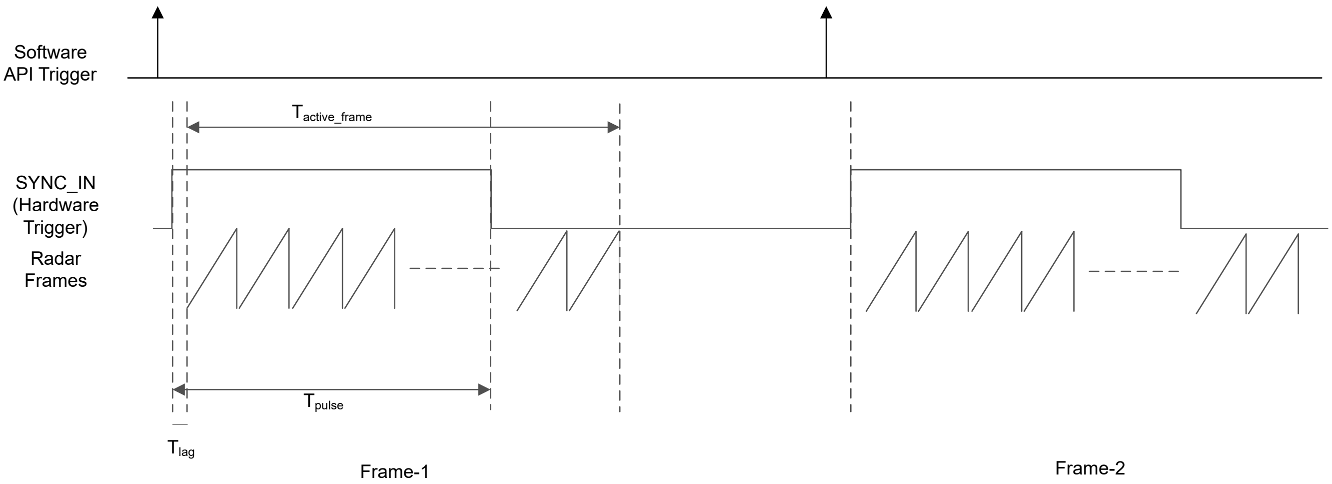


Figure 7-9. Sync In Hardware Trigger

Table 7-16. Frame Trigger Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{active_frame}	Active frame duration	User defined		ns
T_{pulse}		25	$< T_{active\_frame}$ or 4000	

7.13.3 Input Clocks and Oscillators

7.13.3.1 Clock Specifications

The IWRL6432W requires external clock source (that is, a 40MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal connected to the device pins Figure 7-10 shows the crystal implementation.

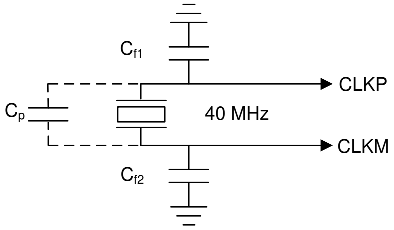


Figure 7-10. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in Figure 7-10, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \tag{1}$$

Table 7-17 lists the electrical characteristics of the clock crystal.

Table 7-17. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		105	°C
Frequency tolerance	Crystal frequency tolerance(1) (2) (3)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects radar sensor accuracy.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40MHz clock is fed externally. Table 7-18 lists the electrical characteristics of the external clock signal.

Table 7-18. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DCV_{il}	0.00		0.20	V
	DCV_{ih}	1.6		1.95	V
	Phase Noise at 1kHZ			–132	dBc/Hz
	Phase Noise at 10 kHZ			–143	dBc/Hz
	Phase Noise at 100 kHZ			–152	dBc/Hz
	Phase Noise at 1MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Frequency Tolerance	-200		200	ppm

7.13.4 MultiChannel buffered / Standard Serial Peripheral Interface (McSPI)

The McSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus

7.13.4.1 McSPI Features

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receive mode
- Controller multichannel mode:
  - Full duplex/half duplex
  - Transmit-only/receive-only/transmit-and-receive modes
  - Flexible input/output (I/O) port controls per channel
  - Programmable clock granularity
  - Per channel configuration for clock definition, polarity enabling, and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for McSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

7.13.4.2 SPI Timing Conditions

Table 7-19 presents timing conditions for McSPI

Table 7-19. McSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.13.4.3 SPI—Controller Mode

7.13.4.3.1 Timing and Switching Requirements for SPI - Controller Mode

Table 7-20 and Table 7-21 present timing requirements for SPI - Controller Mode.

Table 7-20. SPI Timing Requirements - Controller Mode

NO.(1) (8)			MODE	MIN	MAX	UNIT
SM4	$t_{su(MISO\text{-}SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge (1)		5		ns
SM5	$t_{h(SPICLK\text{-}MISO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge (1)		3		ns

Table 7-21. SPI Switching Characteristics - Controller Mode

NO.(1) (8)			MODE	MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK (1) (2)		24.6(3)		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low (1)		-1 + 0.5P(3) (4)		ns
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high (1)		-1 + 0.5P(4)		ns
SM6	$t_{d(SPICLK\text{-}SIMO)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition (1)		-2	5	ns
SM7	$t_{sk(CS\text{-}SIMO)}$	Delay time, SPI_CS[x] active to SPI_D[x] transition		5		ns
SM8	$t_{d(SPICLK\text{-}CS)}$	Delay time, SPI_CS[x] active to SPI_CLK first edge	Controller_PHA0_POL 0; Controller_PHA0_POL 1;(5)	-4 + B(6)		ns
			Controller_PHA1_POL 0; Controller_PHA1_POL 1;(5)	-4 + A(7)		ns
SM9	$t_{d(SPICLK\text{-}CS)}$	Delay time, SPI_CLK last edge to SPI_CS[x] inactive	Controller_PHA0_POL 0; Controller_PHA0_POL 1;(5)	-4 + A(7)		ns
			Controller_PHA1_POL 0; Controller_PHA1_POL 1; (5)	-4 + B(6)		ns
SM11	Cb	Capacitive load for each bus line		3	15	pF

(1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data
(2) Related to the SPI_CLK maximum frequency
(3) 20 ns cycle time = 50 MHZ
(4) P = SPICLK period
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register
(6) B = (TCS + .5) × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even >= 2.
(7) When P = 20.8 ns, A = (TCS + 1) × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
When P > 20.8 ns, A = (TCS + 0.5) × Fratio × TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.

This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data

Note

Supported frequency of Radar SPI Peripheral mode is 40MHz in full cycle and 20MHz in Half cycle mode.

7.13.4.3.2 Timing and Switching Characteristics for SPI Output Timings—Controller Mode

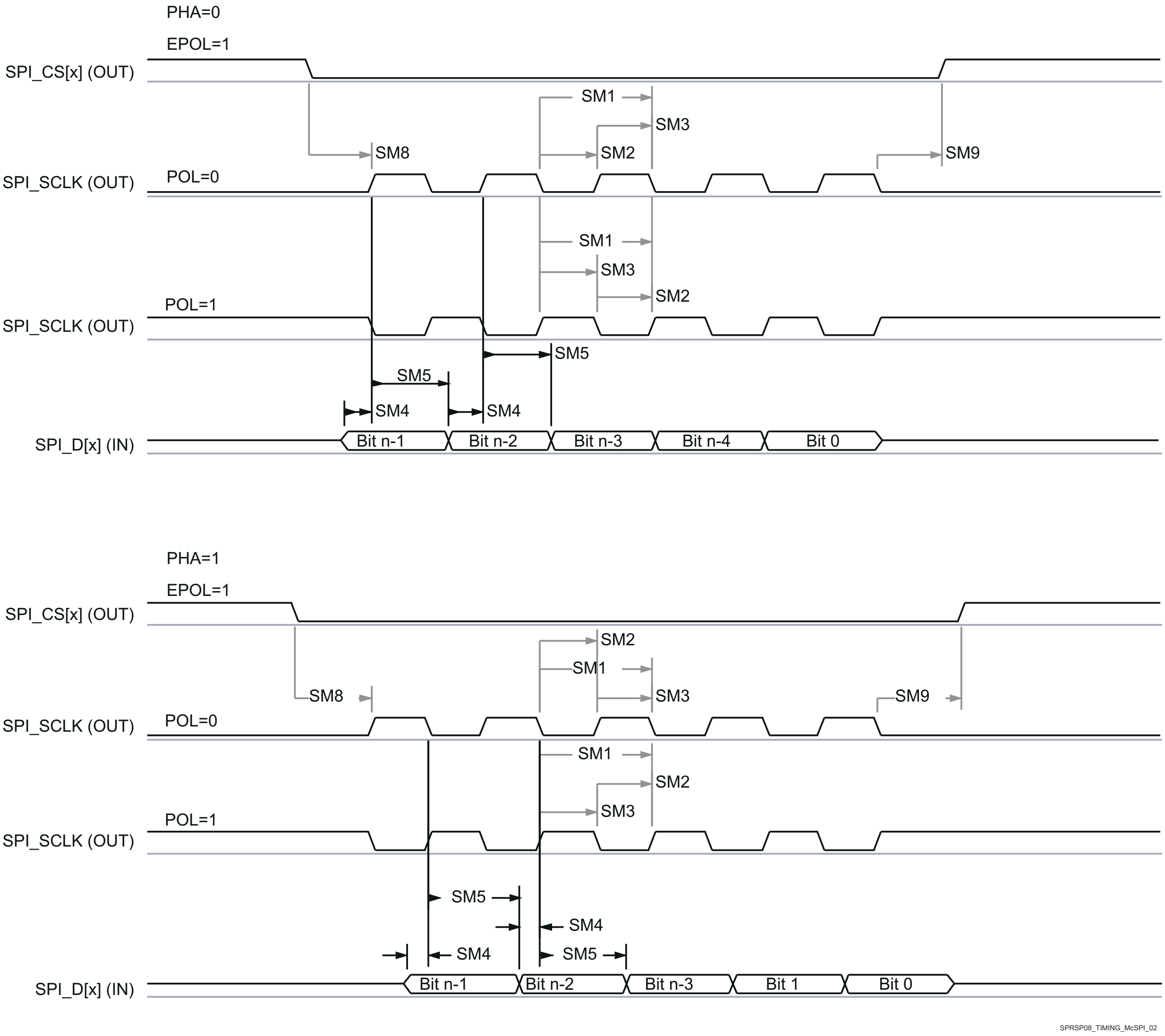


Figure 7-11. SPI Timing -Controller Mode Receive

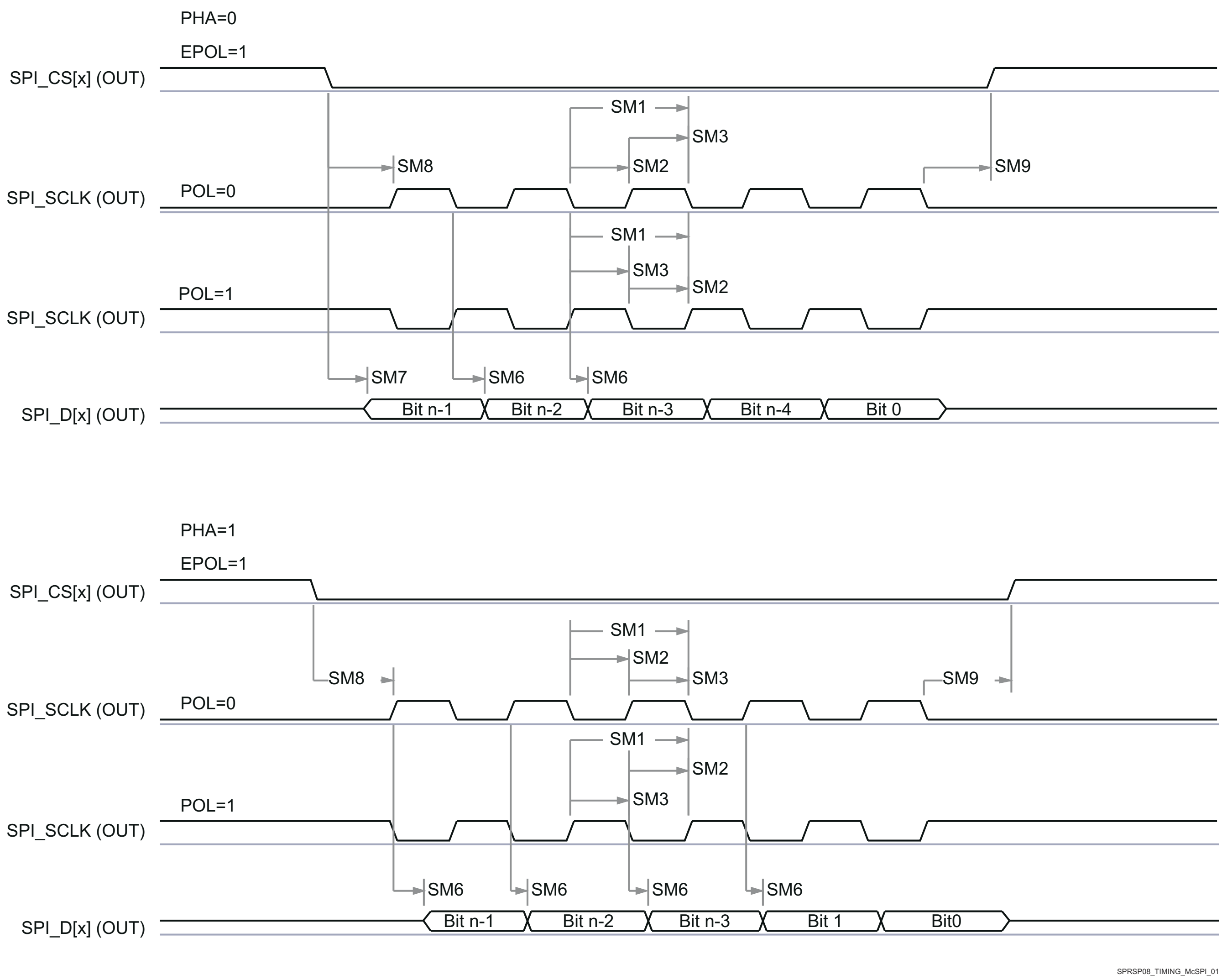


Figure 7-12. SPI Timing- Controller Mode Transmit

7.13.4.4 SPI—Peripheral Mode

7.13.4.4.1 Timing and Switching Requirements for SPI - Peripheral Mode

Table 7-22 and Table 7-23 present timing requirements for SPI -Peripheral Mode.

Table 7-22. SPI Timing Requirements - Peripheral Mode

NO.(1) (3)	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK	24.6		ns
SS2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_CLK low	0.45*P(2)		ns
SS3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_CLK high	0.45*P(2)		ns
SS4	$t_{su(SIMO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge	3		ns
SS5	$t_{h(SPICLK-SIMO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge	1		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPI_CS[x] valid before SPI_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPI_CS[x] valid after SPI_CLK last edge	5		ns
SS10	sr	Input Slew Rate for all pins	1	3	ns
SS11	Cb	Capacitive load on D0 and D1	2	15	pF

Table 7-23. SPI Switching Characteristics Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-SOMI)}$	Delay time, SPI_CLK active edge to McSPI_somi transition	0	5.77	ns
SS7	$t_{sk(CS-SOMI)}$	Delay time, SPI_CS[x] active edge to McSPI_somi transition	5.77		ns

(1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) P = SPICLK period.
(3) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

7.13.4.4.2 Timing and Switching Characteristics for SPI Output Timings—Secondary Mode

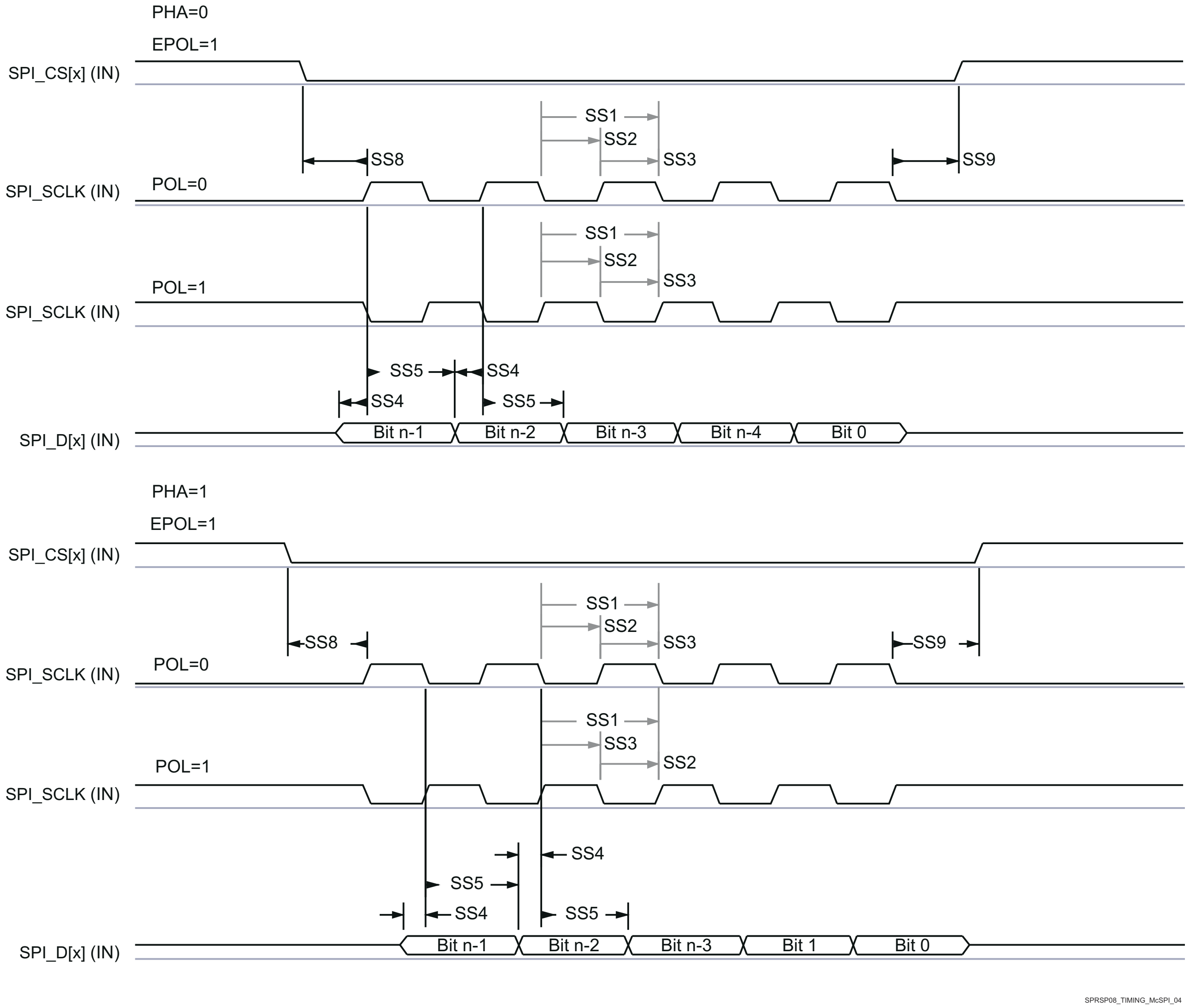


Figure 7-13. SPI Timing - Peripheral mode Receive

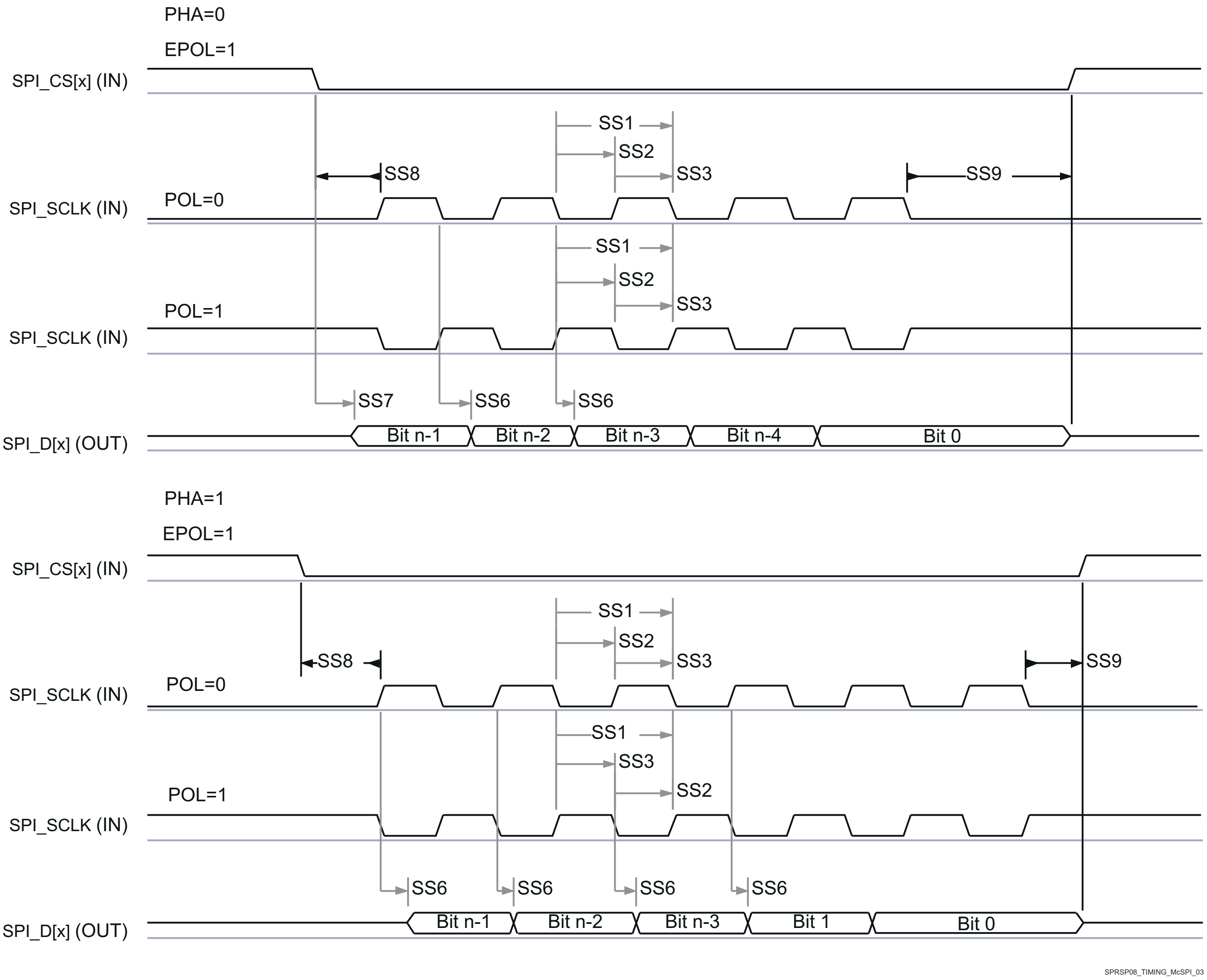


Figure 7-14. SPI Timing - Peripheral mode Transmit

7.13.5 RDIF Interface Configuration

The supported Radar Data InterFace (RDIF) is developed as a debug interface (for example: to capture raw ADC data) and not as a production interface. The RDIF has four data lanes, one Bit Clock lane, and one Frame Clock lane. From this interface, high-speed data is sent out for debug purposes. The RDIF interface supports the following data rates[1]:

- 400Mbps
- 320Mbps
- 200Mbps
- 160Mbps

7.13.5.1 RDIF Interface Timings

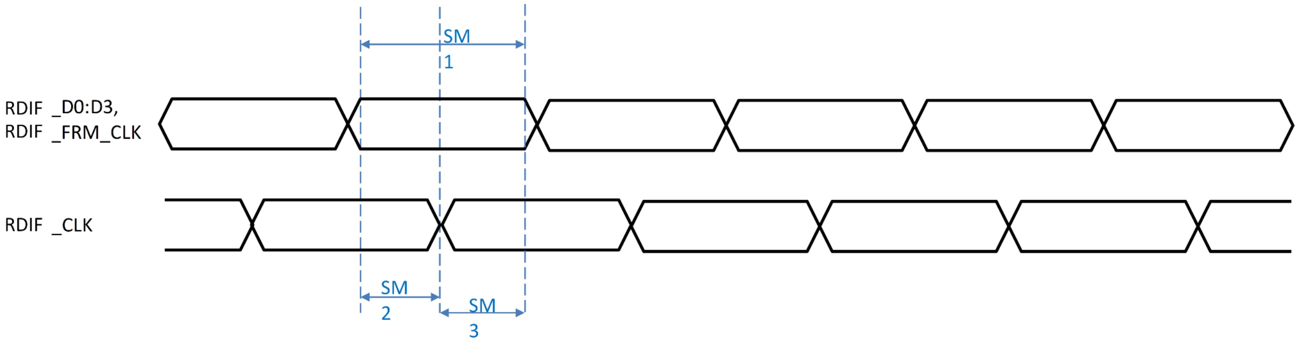


Figure 7-15. RDIF Timing Requirements

Table 7-24. Timing Requirements for RDIF Interface

No.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	Tb (RDIF_D[x])	Bit Interval, RDIF_d[x]	Internal Clock	9.6		ns
SM2	Tvb (RDIF_D[x] - RDIF_CLK)	Data valid time, RDIF_d[x] and RDIF_frm_clk valid before RDIF_clk active edge	Internal Clock	4.8		ns
SM3	Tva (RDIF_CLK - RDIF_D[x])	Data valid time, RDIF_d[x] valid after RDIF_clk active edge	Internal Clock	4.8		ns
SM4	C_b	Capacitive load for each bus line		3	15	pF

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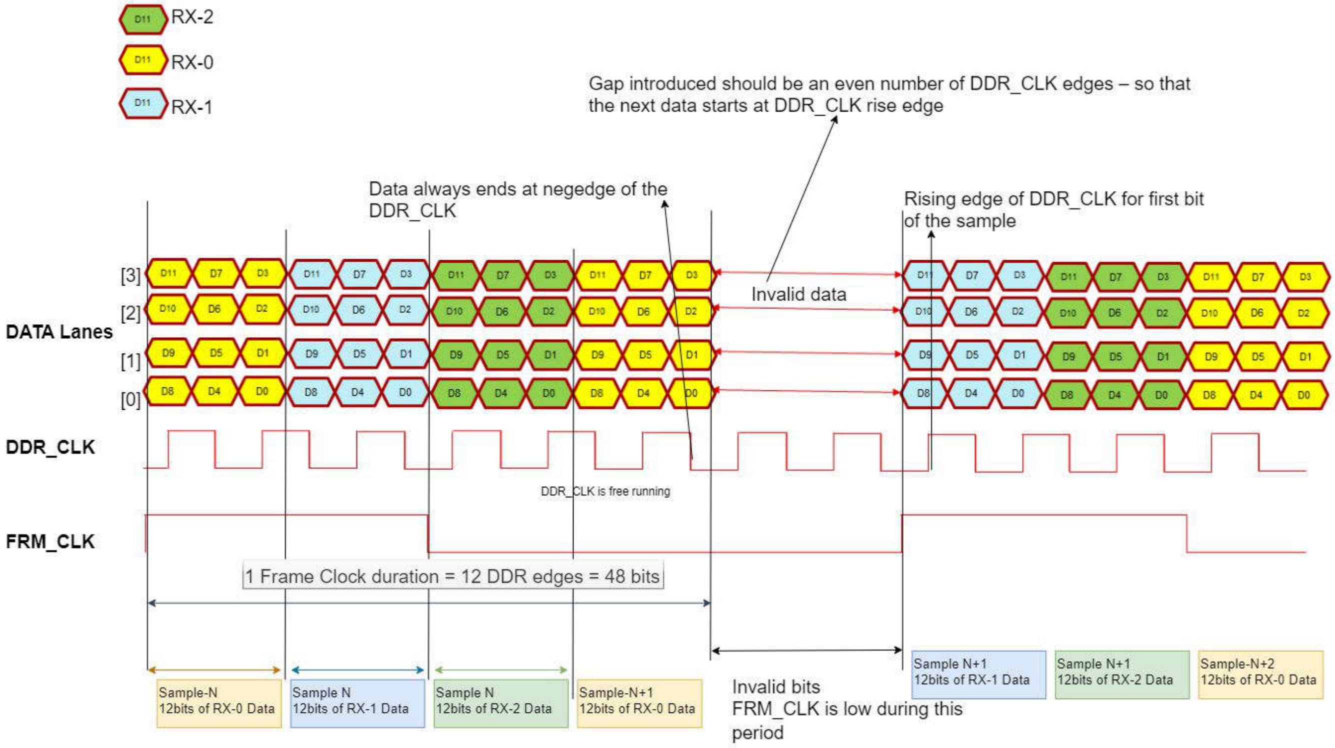
[1] Aggregated data rate over four data lanes.

7.13.5.2 RDIF Data Format



Gap introduced should be an even number of DDR_CLK edges – so that the next data starts at DDR_CLK rise edge

Data always ends at negedge of the DDR_CLK

Rising edge of DDR_CLK for first bit of the sample

DDR_CLK is free running

1 Frame Clock duration = 12 DDR edges = 48 bits

Invalid bits
FRM_CLK is low during this period

Figure 7-16. RDIF Data Format

- The samples are sent one channel by one channel as shown in the diagram above. All the 12-bits of one channel are sent on 4 data lanes in 3 DDR_CLK edges, followed by next RX channel.
- The frame clock (FRM_CLK) spans 12 DDR_CLK edges and 48 bits are sent in 1 FRM_CLK
- The FRM_CLK can have gaps in between. This is required as the interface rate is greater than the incoming rate
- DDR_CLK is continuous.
- DDR_CLK is generated from 400MHz ADC CLK (one of the ADC CLKs) - selected for the DFE. It is the same 400MHz clock selected for DFE.
- New sample always starts at the rise edge of the DDR_CLK
- The FRM_CLK is valid for the entire data bit and is meets the Tsu/Th wrt DDR_CLK.

7.13.6 General-Purpose Input/Output

7.13.6.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

Table 7-25 lists the switching characteristics of output timing relative to load capacitance.

Table 7-25. Switching Characteristics for Output Timing versus Load Capacitance (C_L)

PARAMETER(1) (2)		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20pF	2.8	3.0	ns
			C_L = 50pF	6.4	6.9	
			C_L = 75pF	9.4	10.2	
t_f	Max fall time		C_L = 20pF	2.8	2.8	ns
			C_L = 50pF	6.4	6.6	
			C_L = 75pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20pF	3.3	3.3	ns
			C_L = 50pF	6.7	7.2	
			C_L = 75pF	9.6	10.5	
t_f	Max fall time		C_L = 20pF	3.1	3.1	ns
			C_L = 50pF	6.6	6.6	
			C_L = 75pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

7.13.7 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECDED) mechanism
- Full Message Memory capacity (4352 words).

7.13.7.1 Dynamic Characteristics for the CANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_FD\_tx)}$	Delay time, transmit shift register to CAN_FD_tx pin(1)			15	ns
$t_{d(CAN\_FD\_rx)}$	Delay time, CAN_FD_rx pin to receive shift register(1)			15	ns

(1) These values do not include rise/fall times of the output buffer.

7.13.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions in compatibility mode
- Supports two individually enabled interrupt lines: level 0 and level 1
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from one to eight bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or one parity bit, odd or even parity
  - Stop programmable for one or two stop bits
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Two multiprocessor communication formats allow communication between more than two devices
- Sleep mode is available to free CPU resources during multiprocessor communication and then wake up to receive an incoming message
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Five error flags and Seven status flags provide detailed information regarding SCI events
- Two external pins: RS232_RX and RS232_TX
- Multi-buffered receive and transmit units

7.13.8.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20pF		115.2(1)	1250(2)	kBaud

(1) Maximum supported standard baud rate.
(2) Maximum supported custom baud rate.

7.13.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multi-controller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^{2}C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - START byte
  - Multi-controller transmitter/ target receiver mode
  - Multi-controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

7.13.9.1 I2C Timing Requirements

		STANDARD MODE[1]		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		μs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		μs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		μs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45[1]	0	0.9	μs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b [2] [3]	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.

(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

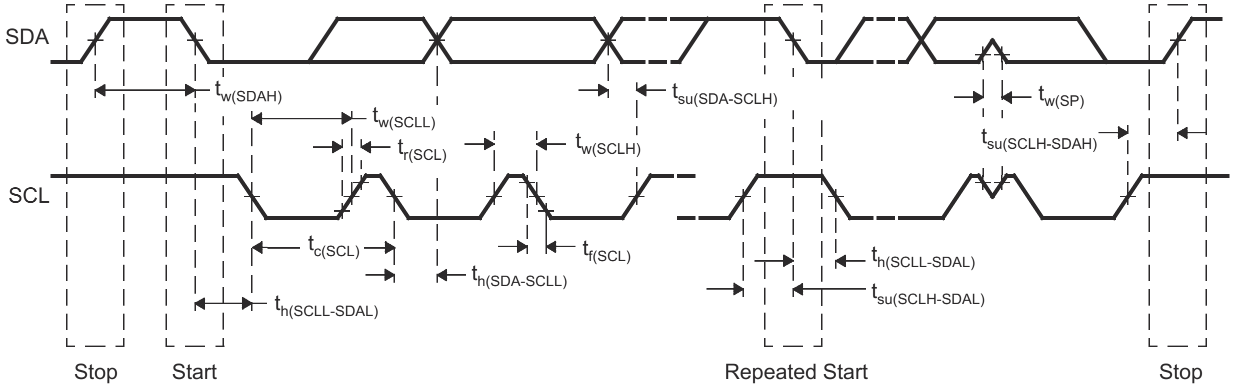


Figure 7-17. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

7.13.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Section 7.13.10.2 and Section 7.13.10.3 assume the operating conditions stated in Section 7.13.10.1.

7.13.10.1 QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.13.10.2 Timing Requirements for QSPI Input (Read) Timings

		MIN(1) (2)	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	5			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	5 – P(3)			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1 + P(3)			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

7.13.10.3 QSPI Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	12.5			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	Y*P – 3(1) (2)			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	Y*P – 3(1) (2)			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1(2) (3)		–M*P + 2.5(2) (3)	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1(2) (3)		N*P + 2.5(2) (3)	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[1] transition	–2		4	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[1] driven (lo-z)	–P – 4(2)		–P +1(2)	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[1] tri-stated (hi-z)	–P – 4(2)		–P +1(2)	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–2 – P(2)		4– P(2)	ns
Q12	$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge	5			ns
Q13	$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge	1			ns
Q14	$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	5 — P(2)			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1 + P(2)			ns

(1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
(2) P = SCLK period in ns.
(3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

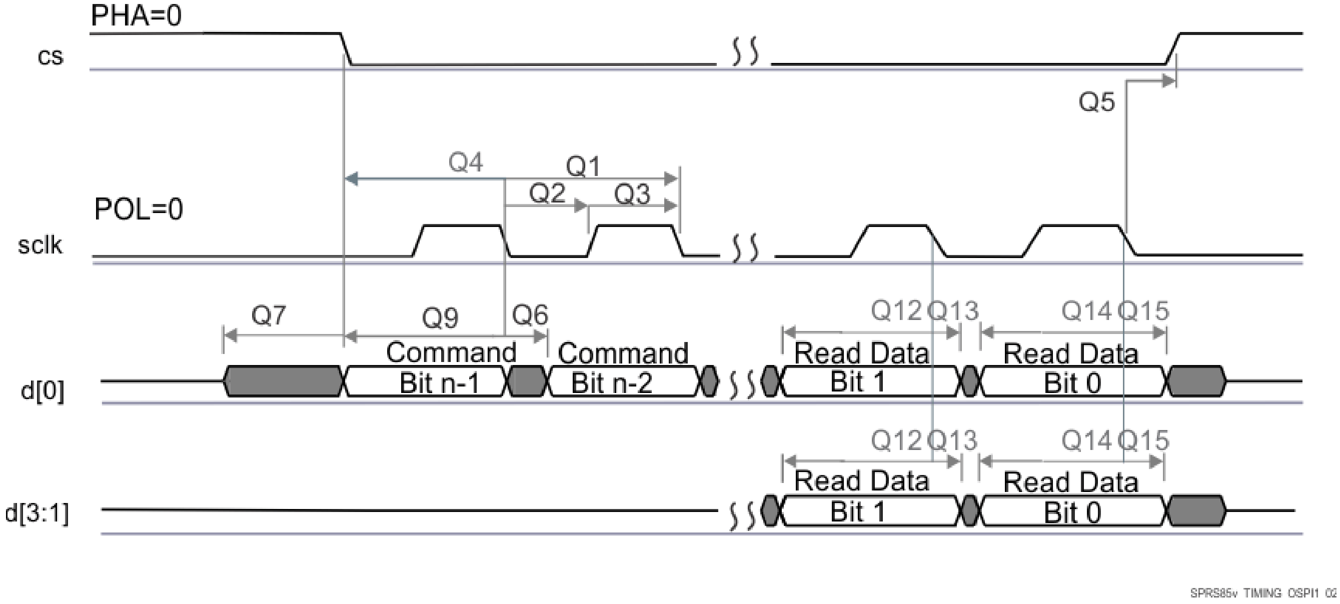


Figure 7-18. QSPI Read (Clock Mode 0)

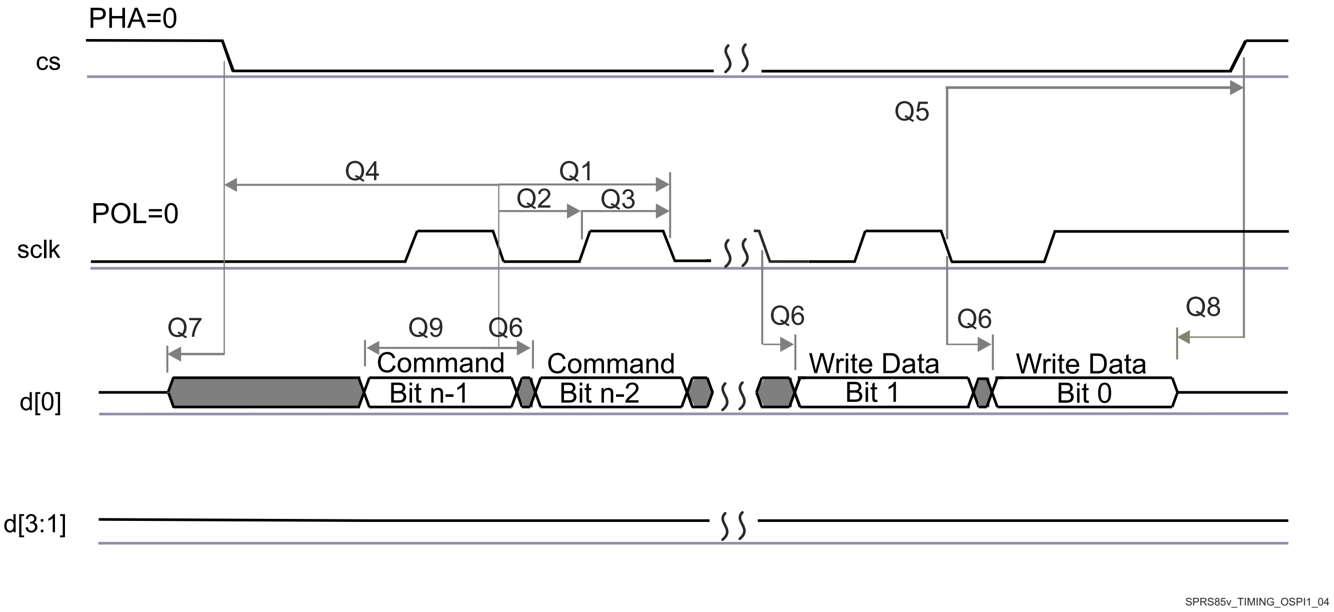


Figure 7-19. QSPI Write (Clock Mode 0)

7.13.11 JTAG Interface

Section 7.13.11.2 and Section 7.13.11.3 assume the operating conditions stated in Section 7.13.11.1.

7.13.11.1 JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

7.13.11.2 Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	20			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	20			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

7.13.11.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		15	ns

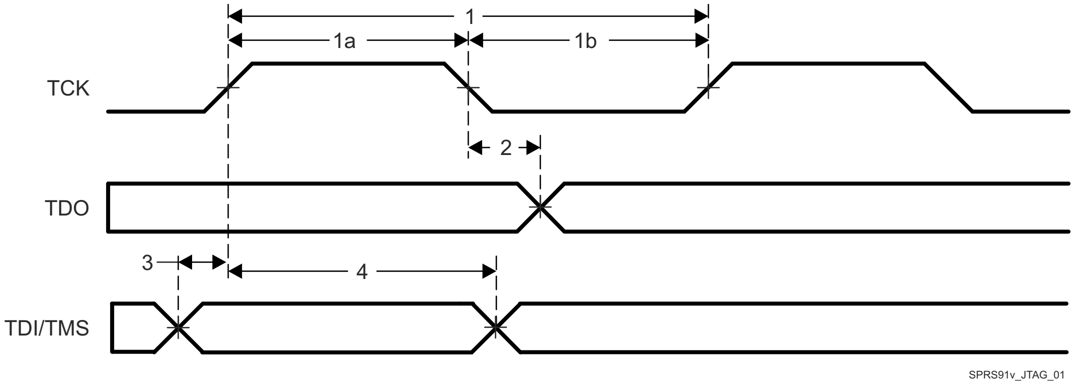


Figure 7-20. JTAG Timing

8 Detailed Description

8.1 Overview

The IWRL6432W device is a complete SOC which includes the mmWave front end, customer programmable MCU and analog baseband signal chain for two transmitters and three receivers. This device is intended as a radar-on-a-chip in use-cases with quality provision for memory, processing capacity and application code size. Use-cases include cost-effective industrial radar sensing applications. Examples are:

- Industrial-level sensing
- Industrial automation sensor fusion with radar
- Traffic intersection monitoring with radar
- Industrial radar-proximity monitoring
- People counting
- Gesture detection

In terms of scalability, the IWRL6432W device could be paired with a low-end external MCU to address more complex applications that might require additional memory for a larger application software footprint and faster interfaces.

8.2 Functional Block Diagram

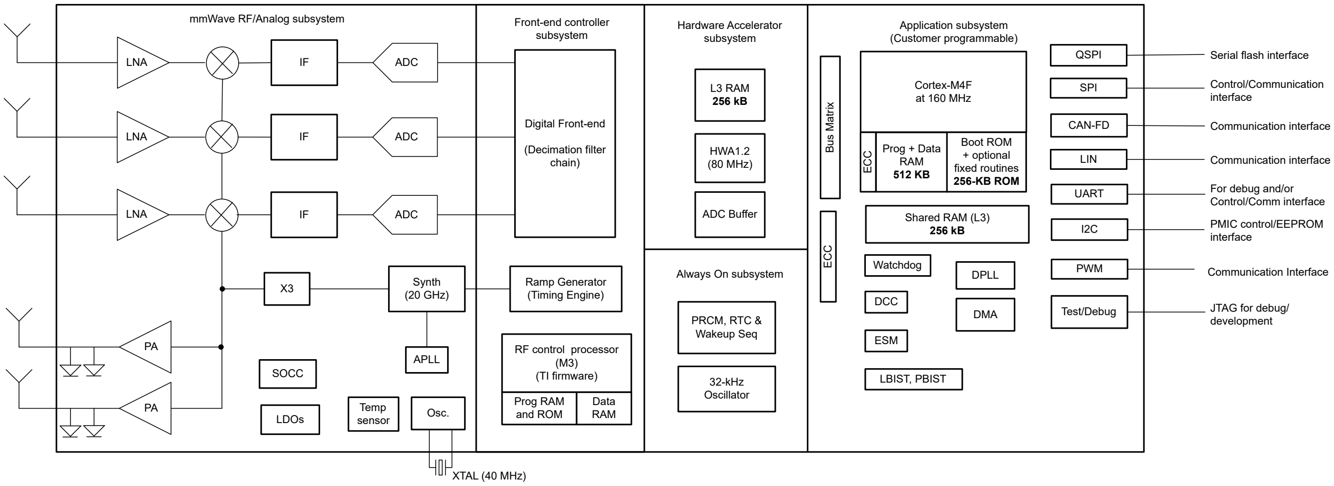


Figure 8-1. Functional Block Diagram

8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The two TX can be operated simultaneously for beam forming in BPM mode or individually in TDM mode. Similarly, the device allows configuring the number of receive channels based on application and power requirements. For system power saving, RF and analog subsystems can be put into low power mode configuration.

8.3.2 Clock Subsystem

The IWRL6432W clock subsystem generates 57 to 63.9GHz from an input reference from a crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X3 multiplier to create the required frequency in the 57 to 63.9 spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

Figure 8-2 describes the clock subsystem.

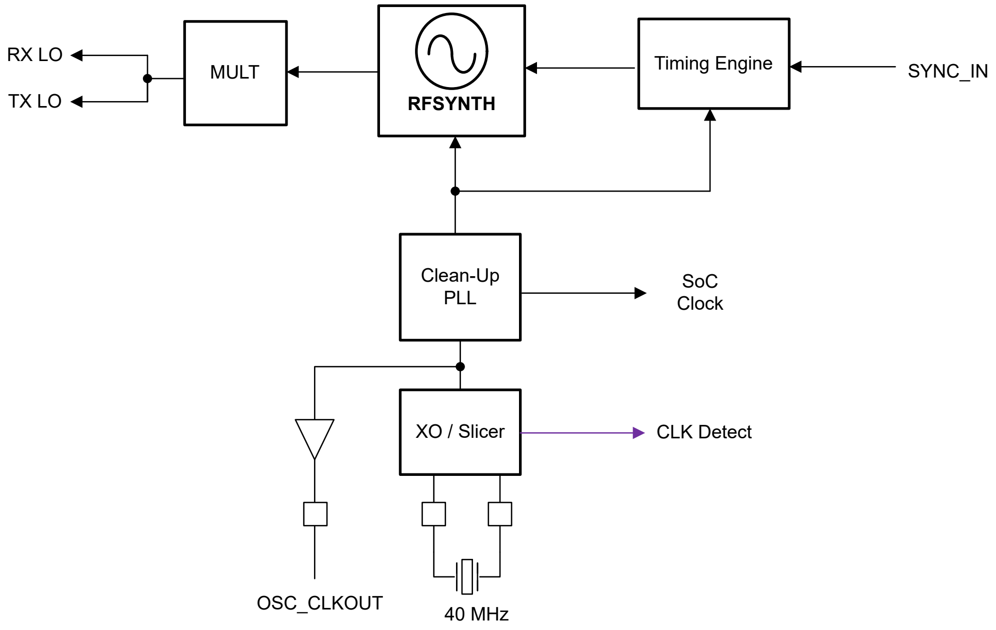


Figure 8-2. Clock Subsystem

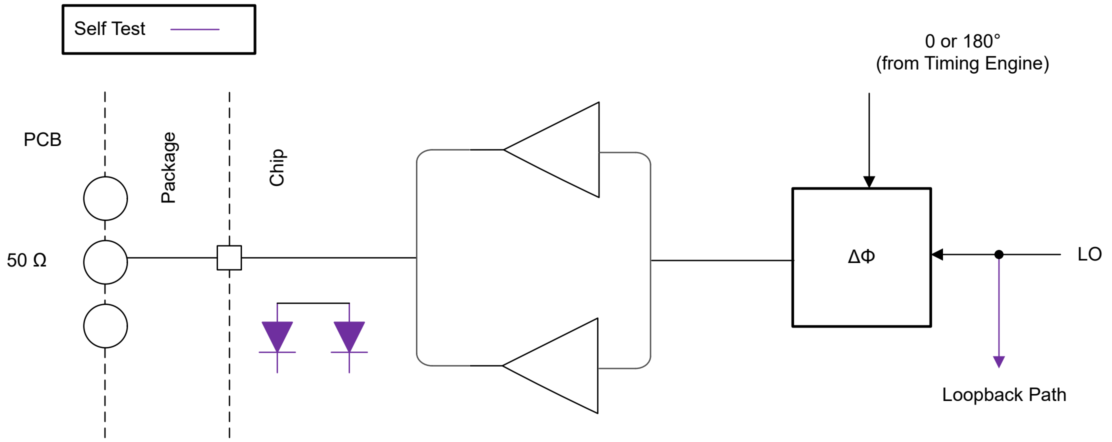
8.3.3 Transmit Subsystem

The IWRL6432W transmit subsystem consists of two parallel transmit chains, each with independent phase and amplitude control. The device supports binary phase modulation for MIMO radar.

The transmit chains also support programmable backoff for system optimization.

Figure 8-3 describes the transmit subsystem.

Figure 8-3. Transmit Subsystem (Per Channel)



8.3.4 Receive Subsystem

The IWRL6432W receive subsystem consists of three parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can either operate simultaneously OR can be powered down individually based on system power needs and application design.

The IWRL6432W device supports a real baseband architecture, which uses real mixer, single IF and ADC chains to provide output for each receiver channel. The device is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175kHZ and can support bandwidths up to 5MHz.

Figure 8-4 describes the receive subsystem.

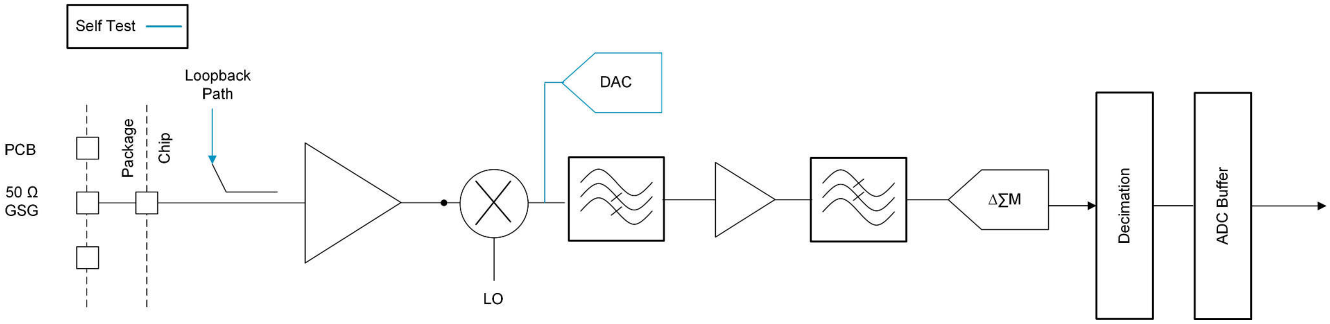


Figure 8-4. Receive Subsystem (Per Channel)

8.3.5 Processor Subsystem

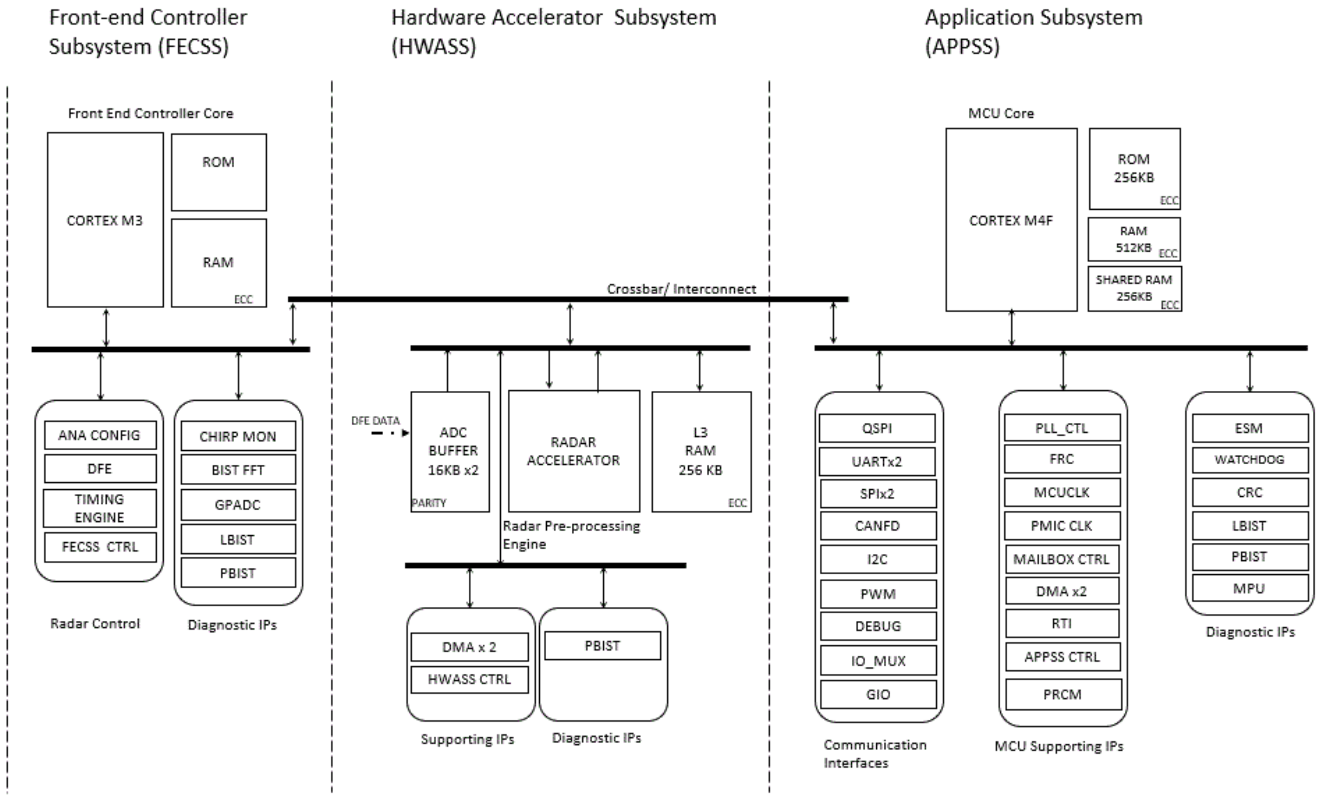


Figure 8-5. Processor Subsystem

Figure 8-5 shows the block diagram for customer programmable processor subsystems in the IWRL6432W device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. The center panel shows the HWA, a high-bandwidth interconnect for high performance (64-bit, 80MHz), and associated peripherals data transfer. RDIF interface for Measurement data output, L3 Radar data cube memory, the ADC buffers, the CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Application Subsystem. The Application Subsystem is the brain of the device and controls all the device peripherals and house-keeping activities of the device. The Application Subsystem contains Cortex-M4F processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I^{2}C, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Main Interconnect through Peripheral Central Resource (PCR interconnect).

8.3.6 Host Interface

The host interface can be provided through a SPI, UART, or CAN-FD interface. In some cases the serial interface for industrial applications is transcoded to a different serial standard.

The IWRL6432W device communicates with the host radar processor over the following control signals:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral) for host control . All radio control commands (and response) flow through this interface
- Reset – Active-low reset for device wakeup from host
- Host Interrupt - an indication that the mmWave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

8.3.7 Application Subsystem Cortex-M4F

The application system includes an ARM Cortex M4F processor clocked with a maximum operating frequency of 160MHz. User applications executing on this processor control the overall operation of the device, including radar control through well-defined API messages, radar signal processing (assisted by the radar hardware accelerator), and peripherals for external interfaces.

See the Technical Reference Manual for a complete description and memory map.

8.3.8 Hardware Accelerator (HWA1.2) Features

- Fast FFT computation, with programmable 2^N sizes, up to 1024-point complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good Signal-to-Quantization-Noise Ratio (SQNR) performance
- Fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for pre-FFT processing – Ex: DC estimation and subtraction
- DC estimation & subtraction, Interference estimation & zero-out, Real window, Complex pre-multiplication
- Magnitude (absolute value) and Log-magnitude computation
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
- Chaining and looping mechanism to sequence a set of operations one after another with minimal intervention from the main processor
- Peak detection – CFAR (CFAR-CA, CFAR-OS) detector
- Basic statistics, including Sum and 1D Max
- Compression engine for radar cube memory optimization

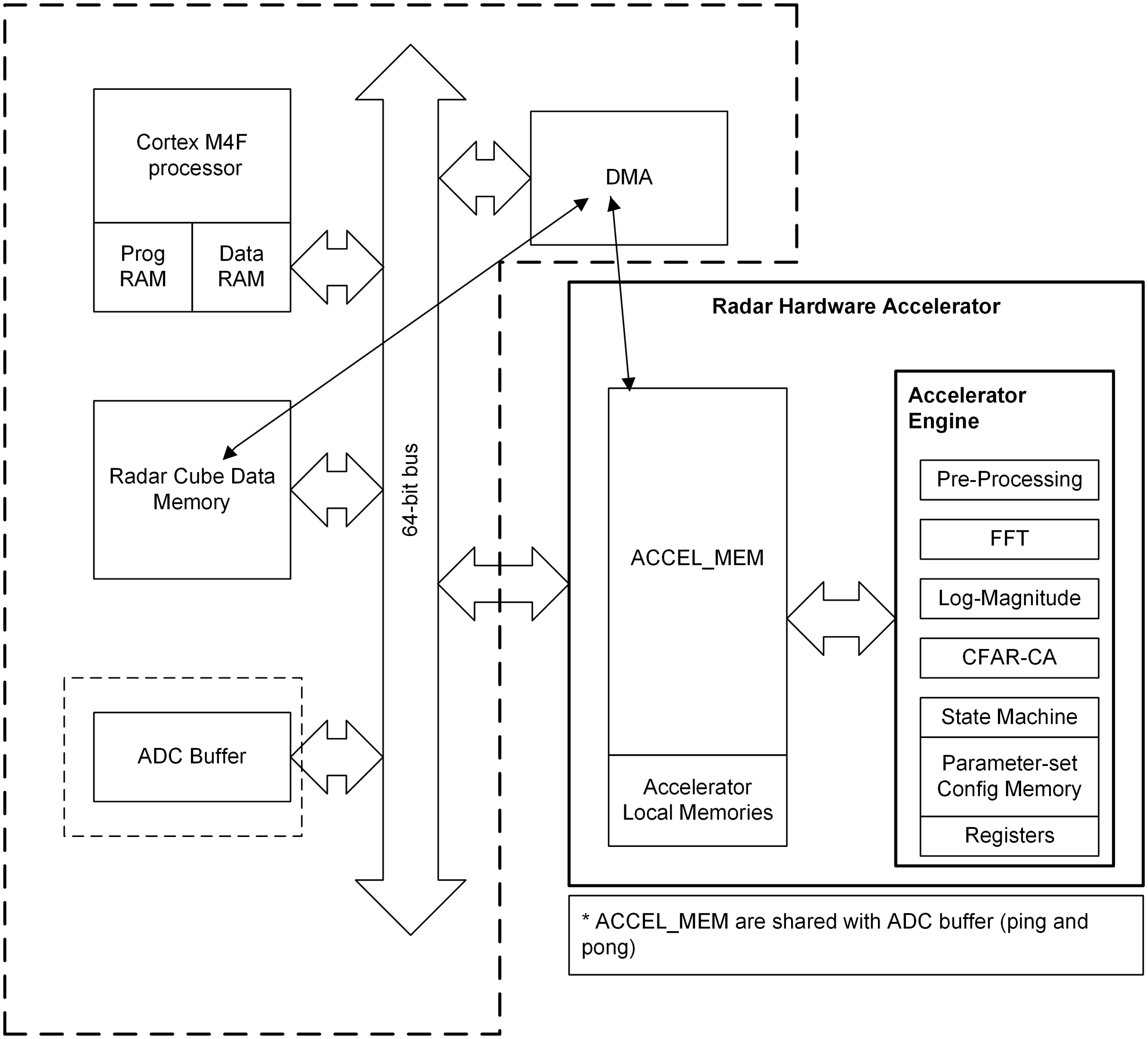


Figure 8-6. HWA 1.2 Functional Block Diagram

8.3.8.1 Hardware Accelerator Feature Differences Between HWA1.1 and HWA1.2

Feature		HWA1.0, HWA1.1 (xWR1843, xWR6843)	HWA1.2 (xWRL6432, xWRL1432)
FFT features	FFT sizes	1024, 512, 256, ...	1024, 512, 256, ...
	Internal bit-width	24-bit I, 24-bit Q	24-bit I, 24-bit Q
		Configurable butterfly scaling at each stage	Configurable butterfly scaling at each stage
	FFT stitching	up to 4096 point	up to 4096 point
FFT benchmark for **four** 256-pt FFTs		1312 clock cycles (6.56 µs at 200MHz)	1320 clock cycles (16.5 µs at 80MHz)
No. of parameter-sets		16	32
Local memory		64KB	64KB

Feature	HWA1.0, HWA1.1 (xWR1843, xWR6843)	HWA1.2 (xWRL6432, xWRL1432)
Input and Output formatter	• A and B-dim addressing of local memory • Programmable scaling	• A and B-dim addressing of local memory • Programmable scaling
Pre-FFT processing	• Interference zero out with fixed threshold, based on magnitude • Complex multiplication (7 modes) • Real window coefficients	• DC estimation and subtraction • Interference zero out with adaptive statistics, based on mag, mag-diff. Interference count indication. • Complex multiplication (7 modes) • Real window coefficients
Post-FFT processing	Log-magnitude (0.3dB accuracy)	Log-magnitude (0.06dB accuracy)
Compression and De-compression support	Not available in HWA1.0 (xWR1843), Available in HWA1.1 (xWR6843)	Available
Detection	CFAR-CA (linear and log modes)	• CFAR-CA (linear and log modes) • CFAR-OS (window size up to 32 on each side)
Statistics	1D Sum, 1D Max	1D Sum, 1D Max

8.4 Other Subsystems

8.4.1 GPADC Channels (Service) for User Application

The IWRL6432W device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to two external voltages. The GPADC1 , and GPADC2 pins are used for this purpose.

- GPADC itself is controlled by TI firmware running inside the FEC sub-system and access to it for customer's external voltage monitoring purpose is via 'APPSS' calls routed to the FEC subsystem. This API could be linked with the user application running on APPSS Cortex M4F®.
- Device Firmware package (DFP) provides APIs to configure and measure these signals. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

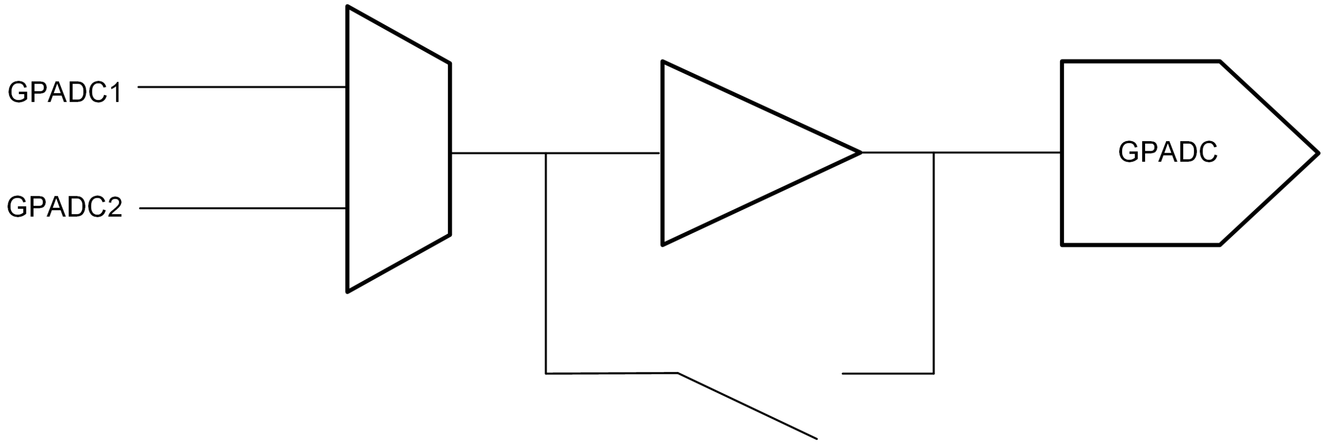


Figure 8-7. GPADC Path

GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7°C.

8.4.2 GPADC Parameters

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	8	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate(2)	831	Ksps
ADC sampling time(2)	300	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.
(2) GPADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

8.5 Memory Partitioning Options

IWRL6432W devices will have a total memory of 1MB. The L3 memory has two memory banks and can be associated with radar cube memory or with the Cortex-M4F RAM.

Table 8-1. Memory Partition Options

		Config 1	Config 2	Config 3
Radar data memory* (L3)	Includes data cube, detection matrix, heatmap	256KB	384kB	512KB
Application (M4F program + data)	Includes drivers, mmWavelink, BIOS	768KB	640KB	512KB
Total memory		1024KB	1024KB	1024KB

The entire RAM is retainable. Additionally, each memory cluster can be independently turned off (if needed). The clusters are defined as below

Table 8-2. Memory Retention Options

RAM_1			RAM_2		RAM_3	Shared	HWA
256KB			128KB		128KB	256KB	256KB
BANK #1(1)			BANK #2		BANK #3		
Cluster #1	Cluster #3	Cluster #4	Cluster #2	Cluster #5		Cluster #6	
64kB	64KB	128KB	16KB	112KB	128KB	256KB	256KB

(1) Retention memories have power switches. These Banks represent memory configurations.

8.6 Boot Modes

As soon as device reset is de-asserted, the processor of the APPSS starts executing its bootloader from an on-chip ROM memory.

The bootloader operates in three basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

Table 8-3 enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 8-3. SOP Combinations

SOP1	SOP0	BOOTLOADER MODE AND OPERATION
0	0	**Flashing Mode** Device Bootloader spins in loop to allow flashing of user application (or device firmware patch - Supplied by TI) to the serial flash.
0	1	**Functional Mode** Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it.
1	1	**Debug Mode** Bootloader is bypassed and M4F processor is halted. This allows user to connect emulator at a known point.

9 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Application information can be found on IWR Application web page.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWRL6432W*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
P	Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
null	Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, YFF0111-C01), the temperature range (for example, blank is the default commercial temperature range). Figure 10-1 provides a legend for reading the complete device name for any *IWRL6432W* device.

For orderable part numbers of *IWRL6432W* devices in the AMF0102A YFF0111-C01 package types, see the Package Option Addendum of this document (when available), the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *IWRL6432W Device Errata* .

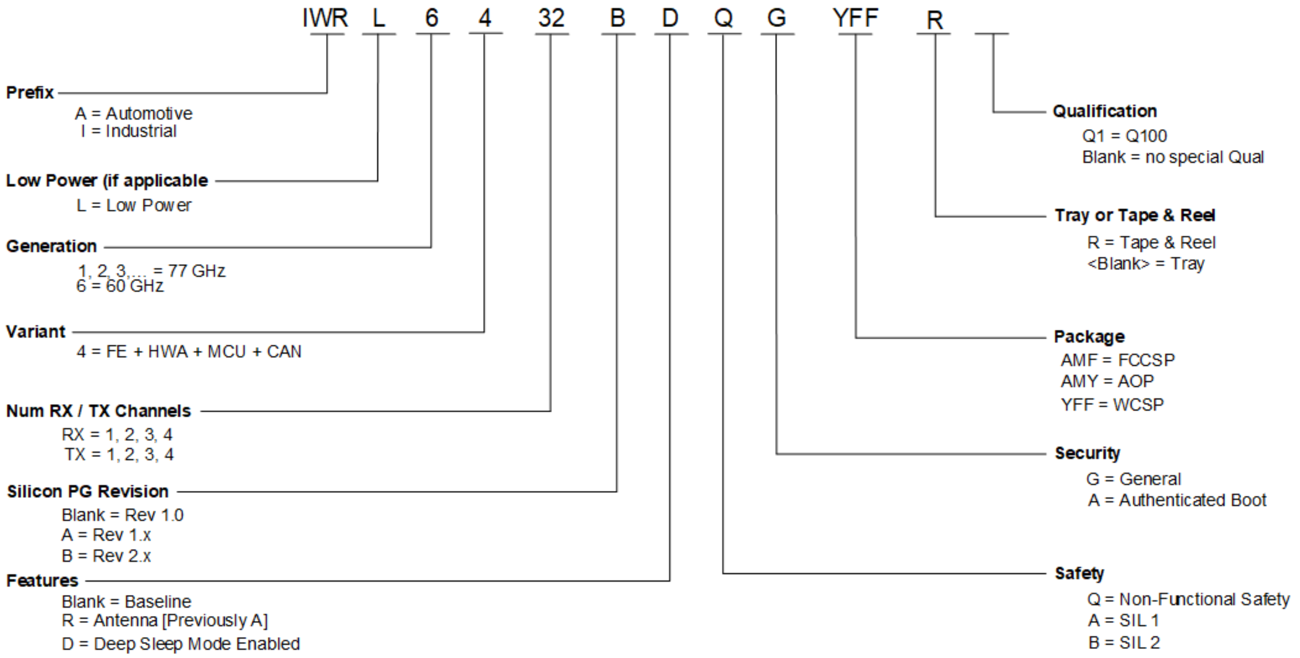


Figure 10-1. Device Nomenclature

10.2 Tools and Software

Models

IWRL6432W BSDL model

Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

IWRL6432W IBIS model

IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the peripherals, and other technical collateral follows.

Errata

- IWRL6432W device errata

  Describes known advisories, limitations, and cautions on silicon and provides workarounds.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help—straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVISION	NOTES
December 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

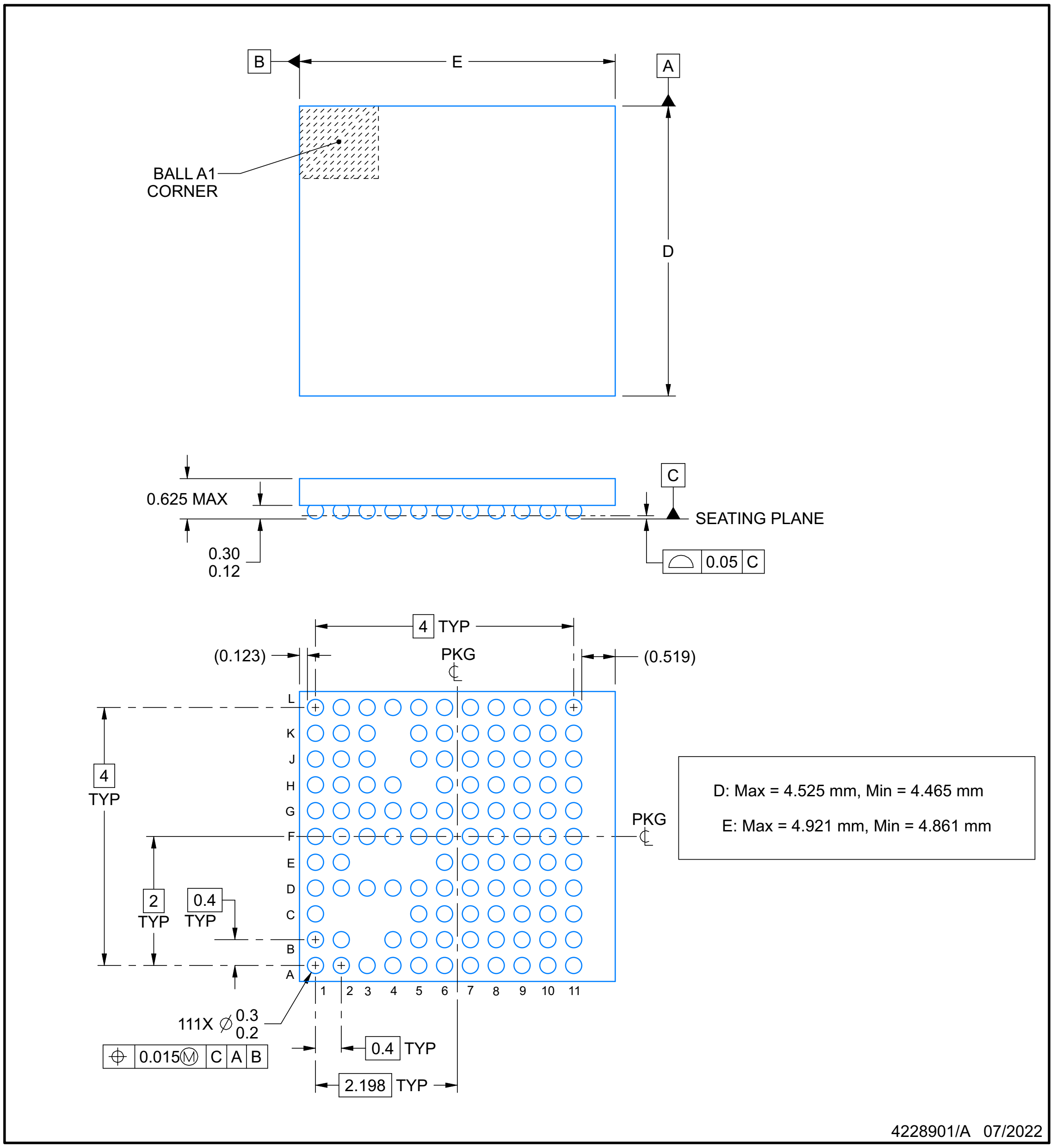
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

PACKAGE OUTLINE

YFF0111-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 4.525 mm, Min = 4.465 mm

E: Max = 4.921 mm, Min = 4.861 mm

NOTES:

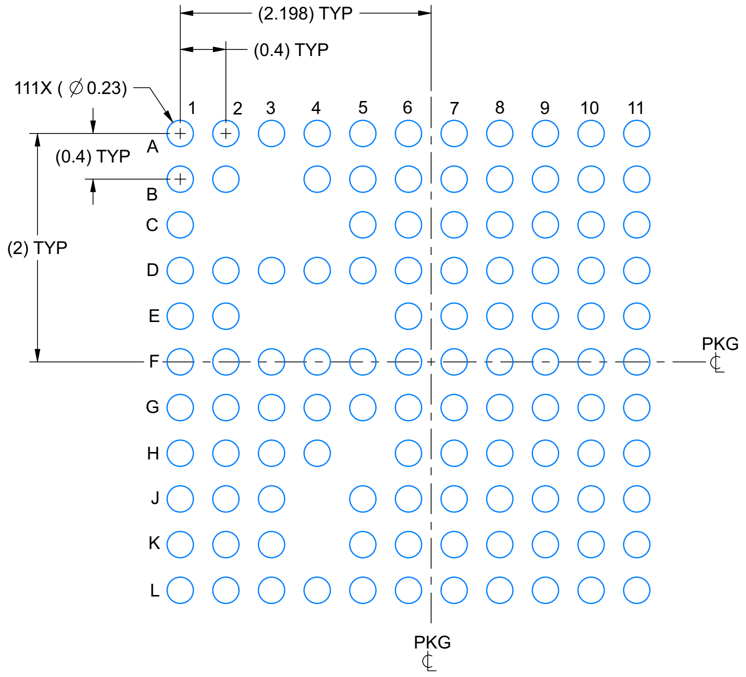
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

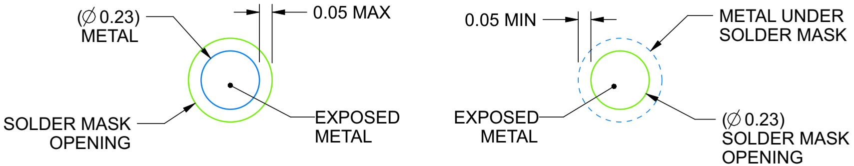
YFF0111-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4228901/A 07/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

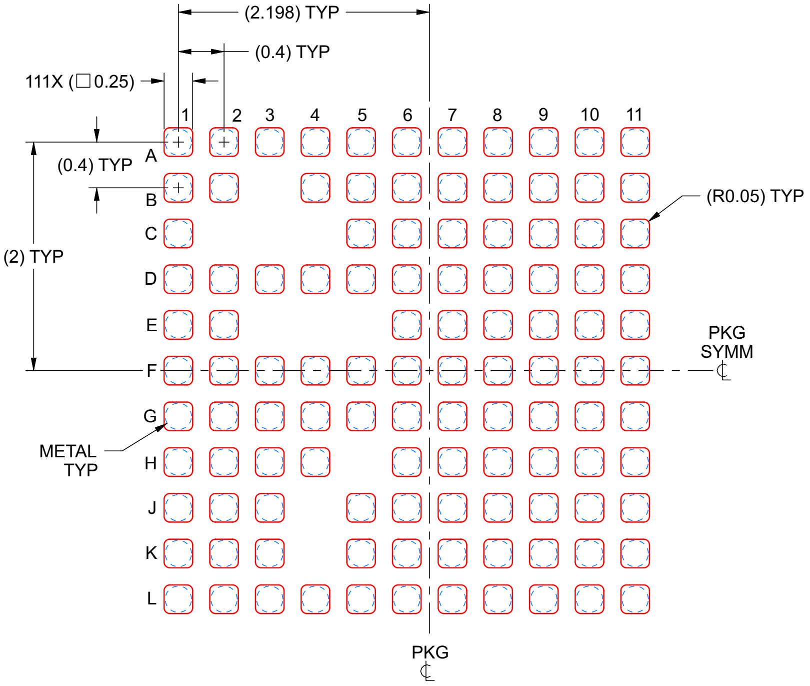
www.ti.com

EXAMPLE STENCIL DESIGN

YFF0111-C01

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:18X

4228901/A 07/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
IWRL6432BDQAYFFR	ACTIVE	DSBGA	YFF	111	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	IWRL6432 QA YFF	Samples
IWRL6432BDQGYFFR	ACTIVE	DSBGA	YFF	111	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 105	IWRL6432 QG YFF	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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