LDC5072-Q1 正弦および余弦インターフェイス付き誘導性位置センサ・フロント・エンド

1 特長

- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 0:–40℃～+160℃の動作時周囲温度範囲
- 0°～360° の絶対回転位置に対応する非接触型誘導性位置センサ向けアナログ・フロント・エンド IC 内蔵
- 磁石が不要になり、システム・コストを削減
- 過酷な環境での動作をサポートし、浮遊磁界、汚れ、汚染に対する耐性
- 最大 480,000 RPM の回転速度で 1 度以下の高分解能と精度
- 広いダイナミック入力範囲に対応する正弦出力と余弦出力を持つ差動信号パス
- 5V および 3.3V 入力電源動作モード
- 誘導性センサ・コイルを励起するための 2.4MHz～5MHz 帯域の内蔵 LC 発振器
- 高電圧保護機能を搭載し、大容量性負荷に対応できる差動出力ドライバ
- 出力ドライバのダイナミック・レンジを最大化する自動 / 手動ゲイン制御
- 機能安全準拠
  - 機能安全アプリケーション向けに開発
  - ISO 26262 システムの設計に役立つ資料を利用可能
  - ASIL C(D) までの決定論的対応能力
  - ASIL C までのハードウェア機能
- IC、センサの入力、出力、電源ピンに関する包括的な診断機能
- –15V～30V の入力電源および出力ピンの逆電圧保護と過電圧保護
- 機能安全の冗長モードに対応

2 アプリケーション

- 回転位置センサは以下の用途に対応:
  - EV/HEV のトラクション・モータ・インバータ
  - 電動パワー・ステアリング
  - ブレーキ・ブースト・モータ
  - スタータ・ジェネレータ内蔵
- 小型の角度センサまたはアークモーション・センサは以下の用途に対応:
  - ペダル位置
  - バルブとアクチュエータ
  - ロボット

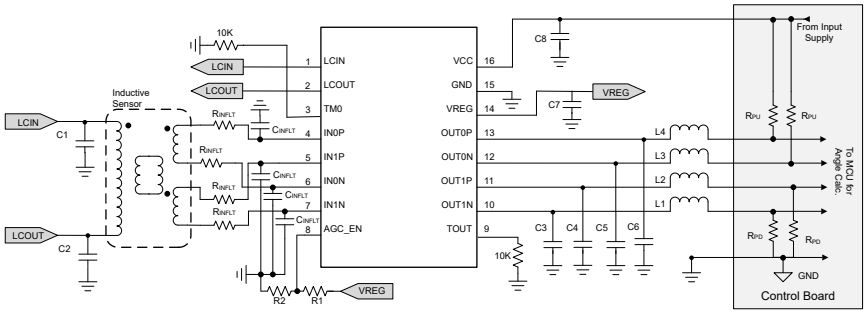
3 概要

LDC5072-Q1 IC は、車載用および産業用アプリケーションの絶対回転位置を対象とした非接触型誘導性位置センサ用のアナログ・フロントエンドです。LDC5072-Q1 は、通常プリント基板 (PCB) にプリントされているコイルを励起します。PCB の近くに配置した導電性ターゲットを使用して、同じ PCB 上の 2 組のレシーバ・コイルに励起が結合されます。導電性ターゲットは、別の PCB にパターンをプリントすることもできます。コイル PCB は静止状態にとどまり、ターゲットはモータ、アクチュエータ、またはバルブとともに移動します。励起コイルは、レシーバ・コイルに対するターゲットの位置に応じて、レシーバ・コイルに 2 次電圧を生成します。位置の信号表現は、レシーバ・コイルから電圧を読み取り、それを処理し、ターゲットの位置の正弦成分と余弦成分を表すアナログ出力を与えることで得られます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
LDC5072-Q1	TSSOP (16)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



LDC5072-Q1 代表的なアプリケーションの図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2021) to Revision C (July 2023) — **Page**

- データシートのステータス可視性を公開リリースに変更 ... 1

Changes from Revision A (September 2020) to Revision B (August 2021) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「概要」セクションのアプリケーション図、および図 9-1、9-3、9-4、9-5 が更新されました。 ... 1
- Separated output comparator short into positive and negative limits ... 10
- The tPRWR_ON_DT in the “Switching Characteristics” is incorrectly specified. The values “360/400/440” will be changed to “302/336/370” ... 12
- The AGC rate change is imprecisely specified in *Automatic Gain Control*: “1 code each second” was updated to “one code approximately every 840mS”. Added eight codes every 3.2uS during start-up in the fast AGC region ... 18
- Updated application diagram in *5-V Supply Mode* and updated 表 9-1 to include connection instructions for the AGC_EN pin ... 26
- The resistor R2 in the example design in *AGC Mode* was updated to 1.5KΩ. ... 27
- Changed 図 9-3 ... 29

Changes from December 7, 2018 to September 30, 2020 (from Revision * (December 2018) to Revision A (September 2020)) — **Page**

- デバイスの最大動作時周囲温度を 160℃に更新。 ... 1
- 機能安全能力のテキストを更新。 ... 1
- Updated pin description for better clarity replacing inverted and non-inverted with negative and positive respectively. ... 5
- Updated T_A to 160℃ in *Absolute Maximum Ratings* ... 6
- Updated T_J to 170℃ in *Absolute Maximum Ratings* ... 6
- Added 4000V HBM ESD information to ESD Ratings ... 6
- Changed INL to Err_{INL} and updated definition and values in Signal Path section of *Electrical Characteristics* ... 7

- Changed maximum value of t_{PROP_CH} over temperature and changed maximum T_A to 160°C in Signal Path section of *Electrical Characteristics* 7
- Changed maximum value of t_{PROP_DIFF} in Signal Path section of *Electrical Characteristics* 7
- Added V_{OUT_SE} in Signal Path section of *Electrical Characteristics* 7
- Changed maximum value of $V_{OUT\_DIFF\_TC}$ over temperature and changed maximum T_A to 160°C in Signal Path section of *Electrical Characteristics* 7
- Added $G_{MIS\_SIG\_PATH}$ parameter in Signal Path section of *Electrical Characteristics* 7
- Added V_{in_off} parameter in Signal Path section of *Electrical Characteristics* 7
- Added $n_{SIG\_PATH\_SE}$ parameter in Signal Path section of *Electrical Characteristics* 7
- Added $n_{SIG\_PATH\_DIFF}$ parameter in Signal Path section of *Electrical Characteristics* 7
- Split V_{AMP_LC} between 25°C and over temperature and specified values wnen VREG is below regulation voltage in Excitation section of *Electrical Characteristics* 7
- Split V_{DC_LC} between 25°C and over temperature and specified values wnen VREG is below regulation voltage in Excitation section of *Electrical Characteristics* 7
- Changed limits and test conditions for I_{LIM_LC} in Excitation section of *Electrical Characteristics* 7
- Added Internal Pull Up resistor parameter R_{PU_LCx} in Excitation section of *Electrical Characteristics* 7
- Added Internal Pull down resistor parameter R_{PD_LCx} in Excitation section of *Electrical Characteristics* 7
- Expanded limits for input differential input signal amplitude V_{DIFF_REC} in Receiver section of *Electrical Characteristics* 7
- Added Internal pull-up resistor parameter R_{PU_INxN} in Receiver section of *Electrical Characteristics* 7
- Added Internal pull-down resistor parameter R_{PD_INxP} in Receiver section of *Electrical Characteristics* 7
- Split $R_{ACG\_EN\_AUTO}$ parameter into $R_{AGC\_EN\_MIN}$ and $R_{AGC\_EN\_MAX}$ in AGC section of *Electrical Characteristics* 7
- Added internal pull-up resistor $R_{PU\_AGC\_EN}$ parameter in AGC section of *Electrical Characteristics* 7
- Updated definition of AGC_Target, AGC_FH, AGC_SH, AGC_SL and AGC_FL for clarity and split parameter across temperature and VCC in AGC section of *Electrical Characteristics* 7
- Changed V_{ILIM_OUT} to I_{ILIM_OUT} for clarity in Output Stage section of *Electrical Characteristics* 7
- Removed required conditions for VCC and GND connection to be valid and added min, and max values for R_{PD_OUT} and R_{PU_OUT} parameters in Output Stage section of *Electrical Characteristics* 7
- Added $I_{OUT\_NOVCC\_*}$ and $I_{OUT\_NOGND\_*}$ parameters in Output Stage section of *Electrical Characteristics* 7
- Removed required conditions for VCC and GND connection to be valid and added test conditions for $V_{OUT\_FLT\_LOW}$ and $V_{OUT\_FLT\_HIGH}$ parameters in Output Stage section of *Electrical Characteristics* 7
- Split $V_{OUT\_FLT\_HIGH}$ and $V_{OUT\_FLT\_LOW}$ parameters across temperature and VCC in Output Stage section of *Electrical Characteristics* 7
- Added $I_{OUT\_LK\_PU}$ parameter in Output Stage section of *Electrical Characteristics* 7
- Added internal impedance parameters $I_{PD\_INx*\_BIST}$ in *Diagnostics* 10
- Added pin BIST comparator thresholds $V_{TH\_FALL\_INx*\_BIST}$ in *Diagnostics* 10
- Added internal impedance parameter $I_{PU\_AGC\_EN\_BIST}$ on AGC_EN pin in *Diagnostics* 10
- Added value for VREG capacitor loss C_{LOSS_VREG} in *Diagnostics* 10
- Moved $V_{POR\_VREG\_xth}$ to *Diagnostics* 10
- Added LC Frequency fault detection parameter f_{FLTH_LC} in *Diagnostics* 10
- Added internal impedance on LCx pins parameters, $I_{Px\_LCx\_BIST}$ in *Diagnostics* 10
- Added $t_{MIN\_PH\_IMB}$ in *Diagnostics* 10
- Added AGC fault limits, $VAL_{AGC\_INP\_OOR\_x}$ in *Diagnostics* 10
- Added input out-of-range pin and low-pass filter parameters, $V_{OOR\_H\_INx\_x}$ in *Diagnostics* 10
- Added common mode fault parmeters for output pin, $V_{CM\_x\_OUTx\_PIN}$ in *Diagnostics* 10
- Added $V_{OUTx\_SHRT\_CMP\_OFF}$ in *Diagnostics* 10
- Added internal regulator under voltage parameter, V_{UV_DVDD} in *Diagnostics* 10
- Added $V_{TOGGLE\_AGC\_EN}$ in *Diagnostics* 10
- Added thermal shutdown parameters T_{TSD_x} in *Diagnostics* 10
- Combined VCC out of range fault degltich times in $t_{VCC\_FLT\_DT}$ and updated value in *Switching Characteristics* 12
- Added VREG over voltage deglitch time $t_{VREG\_OV\_DT}$ in *Switching Characteristics* 12
- Added LC amplitude fault deglitch times in *Switching Characteristics* 12
- Updated values for $t_{AGC\_EN\_x\_DT}$ parameters *Switching Characteristics* 12

- Added input pin and low pass filter fault deglitch times in *Switching Characteristics* 12
- Added and updated outpin fault deglitch times $t_{OUT\_x\_DT}$ in *Switching Characteristics* 12
- Added AGC deglitch times $t_{AGC\_x\_DT}$ in *Switching Characteristics* 12
- Renamed t_{FLT_SIGNAL} to t_{FLT_RECOV} in *Switching Characteristics* 12
- Added power on degltich time $t_{PWR\_ON\_DT}$ in *Switching Characteristics* 12
- Added 図 7-6 for OUTx leakage current..... 13
- Updated text in *Signal Processing Block* for clarity..... 16
- Updated *Fixed Gain Control* section based on new design..... 18
- Updated variable name in 式 8 for clarity..... 18
- Updated text in *Automatic Gain Control* to add information on time-step of the AGC block..... 18
- Added details on output pin diagnostics and output ratiometricity to VCC in *Output Stage* 19
- Added *Undervoltage Diagnostics*, *Initialization Diagnostics*, *Normal State Diagnostics* and *Fault State Diagnostics* to list details on the diagnsostics available in LDC5072-Q1 20
- Added details for device functional modes. Added 図 8-5 and described each of the states in LDC5072-Q1 23
- Updated application diagram in *5-V Supply Mode* and updated 表 9-1 with new optional component values for EMC robustness..... 26
- Updated application diagram in *3.3-V Supply Mode* with new optional component values for EMC robustness..... 29
- Updated application diagram in セクション 9.2.3 with new optional component values for EMC robustness..... 31

5 概要 (続き)

LDC5072-Q1 には 3.3V または 5V の入力電圧が供給され、アナログの正弦および余弦出力をマイコンに接続して角度を計算できます。このデバイスは、出力ピンの高電圧への短絡に対する ESD、EMC/EMI 耐性、逆バッテリ保護、逆電流保護を備えています。電源ピンと出力ピンは、すべて高電圧対応です。このデバイスはモータのノイズに対する耐性があり、帯域外の低周波および高周波ノイズをフィルタリングできます。LDC5072-Q1 は、短絡や開放などのセンサ・フォルトを検出するための広範な診断機能と、電流制限、過電圧、低電圧検出などの内部診断機能を備えています。LDC5072-Q1 は、機能安全アプリケーションを対象とした ISO 26262 仕様に従って設計されています。

6 Pin Configuration and Functions

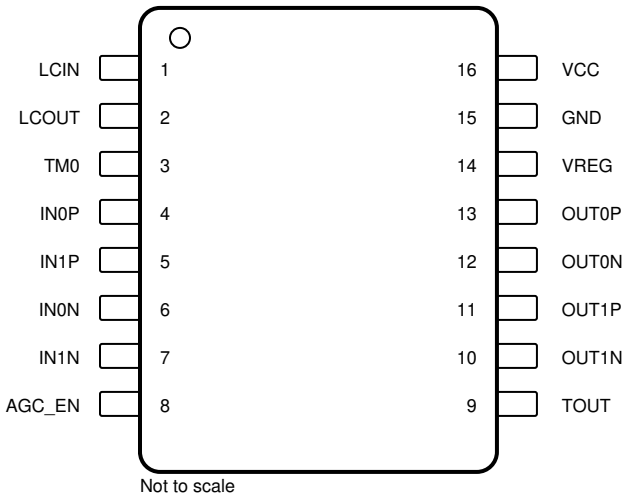


図 6-1. PW Package 16-Pin TSSOP Top View

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	LCIN	I/O	LC oscillator input
2	LCOUT	I/O	LC oscillator output
3	TM0	I/O	Test Mode Input
4	IN0P	I	Input channel 0 positive
5	IN1P	I	Input channel 1 positive
6	IN0N	I	Input channel 0 negative
7	IN1N	I	Input channel 1 negative
8	AGC_EN	I	Automatic Gain Control Enable and Fixed Gain Setting
9	TOUT	I/O	Test Mode Output
10	OUT1N	O	Output channel 1 negative
11	OUT1P	O	Output channel 1 positive
12	OUT0N	O	Output channel 0 negative
13	OUT0P	O	Output channel 0 positive
14	VREG	I/O	Regulated 3.3-V Supply output
15	GND	G	Ground
16	VCC	P	Input Voltage Supply

(1) I = input, O = output, I/O = input and output, G = ground, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	Input Supply voltage	-15	30	V
OUT0P, OUT0N, OUT1P, OUT1N	Output pin voltage	-15	30	
VREG	Regulator output voltage	-0.3	5.5	
GND	Ground Pin voltage	-0.3	0.3	
LCOUT, LCIN	LC Oscillator pin voltage	-0.3	5.5	
AGC_EN, TM0, TOUT, IN0P, IN0N, IN1P, IN1N	All other pin voltage	-0.3	5.5	
T_A	Operating free air temperature	-40	160	°C
T_J	Operating junction temperature	-40	170	
T_{stg}	Storage temperature range	-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2	All pins	±2000	V
			OUT0x, OUT1x, IN0x, IN1x, LCIN, LCOUT, VCC to GND only	±4000	
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins (1, 8, 9, 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC_50}	V_{CC} input voltage (5V input mode)	4.5	5	5.6	V
V_{CC_33}	V_{CC} and V_{REG} input voltage (3.3V input mode)	3.15	3.3	3.6	
I_Q	During startup and in operation (excluding LC oscillator load and OUTxx load)			22	mA

7.4 Thermal Information

THERMAL METRIC(1)		LDC5072-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
over recommended V_{cc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply						
VCC_{Ramp}	Allowed VCC ramp up rate		0.17		100e6	V/s
C_{EXT_VCC}	External VCC decoupling capacitor range		80	100		nF
Internal LDO Regulator VREG						
V_{VREG}	Internal LDO output voltage		3.15	3.3	3.6	V
$V_{POR\_VREG\_UTH}$	VREG power-on upper threshold				3.15	V
$V_{POR\_VREG\_LTH}$	VREG power-on lower thershold		2.91			V
$I_{LOAD\_REG\_EXT}$	Maximum external load on VREG (used for setting voltage on AGC_EN pin externally) (Information Only)				1	mA
I_{LIM_VREG}	VREG current limit		40		90	mA
C_{EXT_VREG}	External VREG decoupling capacitor		180		2000	nF
Signal Path						
Err_{INL}	Integral Non-Linearity error(3) of the signal path transfer function for each channel measured as: Maximum % deviation of output from a best fit line through measured outputs when input is swept from minium to maximum value.	For static inputs; VCC=5V; -3.5V ≤(V_{OUTxP}-V_{OUTxN}) ≤ 3.5V		1%	2.5	%
t_{PROP_CH}	Propagation Delay through receive stage at room temperature.	Measured as zero crossing of diffrential input (INx) to zero crossing of differential output (OUTx) C_{OUT} on each pin = 10nF	3.3		4.6	µs
	Propagation Delay through receive stage across temperature (-40℃ to 160℃).		3		5	µs
t_{PROP_DIFF}	Propagation Delay difference between two channels across temperature	Measured as delay between the zero crossings of the diffrential outputs.			500	ns
V_{OUT_SE}	Difference between single ended outputs calculated at V_{OUT0P}-V_{OUT1P}	Measured for static inputs only for VCC=5V; -1.75V ≤ (V_{OUT0P}-V_{OUT1P}) ≤ 1.75V		50	65	mV
V_{OUT_DIFF}	Difference between differential output calculated as (V_{OUT0P}-V_{OUT0N}) - (V_{OUT1P}-V_{OUT1N}) at room temperature	Measured for static inputs only for VCC=5V; -3.5V ≤ (V_{OUTxP}-V_{OUTxN}) ≤ 3.5V			100	mV
$V_{OUT\_DIFF\_TC}$	Deviation of V_{OUT_DIFF} at -40℃ from room temperature				20	mV
	Deviation of V_{OUT_DIFF} at 160℃ from room temperature				38	mV
$G_{MIS\_SIG\_PATH}$	Gain mismatch between Channel 1 and Channel 2 signal path calculated as ($Gain_{out1}$-$Gain_{out0}$)/ (($Gain_{out1}$+$Gain_{out0}$)*0.5)(2)	Fixed Gain Mode; VCC=3.3V 4.55%VREG < V_{AGC_EN} < 95.45%VREG -40℃ ≤ T_A ≤ 160°C	-0.4		0.4	%
		Fixed Gain Mode; VCC=5.0V; 4.55%VREG < V_{AGC_EN} < 95.45%VREG -40℃ ≤ T_A ≤ 160°C	-0.35		0.55	%
V_{in_off}	Input referred offset for IN0 channel(2) measured with input shorted and exciter coil connected	VCC=3.3V, 5.0V; Fixed Gain Mode; 30%VREG < V_{AGC_EN} < 95.45%VREG -40℃ ≤ T_A ≤ 160°C		150	170	µV
	Input referred offset for IN1 channel(2) measured with input shorted and exciter coil connected			50	100	µV
$n_{SIG\_PATH\_SE}$	Input referred noise for the complete signal path for single ended output for each channel(2)			25		nV/√Hz
$n_{SIG\_PATH\_DIFF}$	Input referred noise for the complete signal path for differential output for each channel(2)			36		nV/√Hz
Excitation						

over operating free-air temperature range (unless otherwise noted)
over recommended V_{cc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AMP_LC}	LC oscillator differential amplitude	3.15V ≤ V_{VREG} ≤ 3.6; T_A=25°C	70	75.8	81.5	%Vreg
		3.15V ≤ V_{VREG} ≤ 3.6; -40°C < T_A < 160°C	64		87	
	LC oscillator differential amplitude when V_{VREG} is below regulation voltage	$V_{POR\_VREG\_LTH}$ ≤ V_{VREG} ≤ $V_{POR\_VREG\_UTH}$; T_A=25°C	69.5		82.5	
		$V_{POR\_VREG\_LTH}$ ≤ V_{VREG} ≤ $V_{POR\_VREG\_UTH}$; -40°C < T_A < 160°C	63		88	
V_{DC_LC}	DC operating point for LC oscillator	3.15V ≤ V_{VREG} ≤ 3.6; T_A=25°C	47	50	52.5	%VREG
		3.15V ≤ V_{VREG} ≤ 3.6; -40°C < T_A < 160°C	43.5		56.5	
	DC operating point for LC oscillator when V_{VREG} is below regulation voltage	$V_{POR\_VREG\_LTH}$ ≤ V_{VREG} ≤ $V_{POR\_VREG\_UTH}$; T_A=25°C	47.5		53	
		$V_{POR\_VREG\_LTH}$ ≤ V_{VREG} ≤ $V_{POR\_VREG\_UTH}$; -40°C < T_A < 160°C	42.5		57.5	
I_{LIM_LC} (2)	RMS value of LC oscillator current limit		13		30	mA
f_{OSC_LC} (2)	LC oscillator resonant frequency		2.4		5	MHz
THD_{LC} (2)	Total harmonic distortion of oscillator output (V_{LCIN}-V_{LCOUT})				-30	dB
R_{PU_LCx}	Internal pull up resistance to VREG on LCIN and LCOUT pins		220		330	KΩ
R_{PD_LCx}	Internal pull down resistance to GND on LCIN and LCOUT pins		220		330	KΩ
Rp	Allowed range for equivalent parallel resistance of LC oscillator coil		167		5000	Ω
L	Allowed range of inductance of excitation coil resonator			5		µH
C_{LC1}, C_{LC2}	Allowed range for capacitors for excitation coil		100	370		pF
C_{MIS}	Allowed capacitor mismatch (between C_{LC1} and C_{LC2})		-10		10	%
Receiver						
V_{DIFF_REC}	Allowed range for differential input signal amplitude	In fixed gain mode, voltage on AGC_EN pin adjusted to set gain to avoid clipping	5		400	mVp-p
V_{COM_REC}	Common mode voltage forced on input signals		45	50	55	%VREG
$f_{LF\_BPF\_REC}$	Bandpass filter lower cutoff frequency(1)		430	600	760	kHz
$f_{UF\_BPF\_REC}$	Bandpass filter upper cutoff frequency(1)		12	20	26	MHz
f_{LPF_REC}	Low pass filter (after demodulation)		65	100	125	kHz
$V_{N\_DIFF\_REC}$	Amplitude of differential noise on input rejected by receive path for fundamental frequency between 10KHz to 20KHz	Differential input signal >20mVpp, VCC=5V, Sqaure wave noise signal ramp time = 8µs			1	Vpp
$V_{N\_COM\_REC}$	Amplitude of common mode noise on input rejected by receive path for fundamental frequency between 10KHz to 20KHz	Differential input signal >20mVpp, VCC=5V, Sqaure wave noise signal ramp time = 8µs			1	
R_{PU_INxN}	Internal pull up resistor to VREG on each of the INxN pins		0.8	1	1.2	MΩ
R_{PD_INxP}	Internal pull down resistor to GND on each of the INxP pins		0.8	1	1.2	
L_{REC}	Typical Receiver coil inductance (Information only)			0.2		µH
R_{REC}	Typical Receiver coil resistance (Information only)			6		Ω

over operating free-air temperature range (unless otherwise noted)
over recommended V_{CC} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Automatic Gain Control						
$V_{AGC\_EN\_AUTO}$	Voltage on AGC_EN pin to set AGC in auto mode				2	%VREG
$V_{AGC\_EN\_MANUAL}$	Voltage range on AGC_EN pin to manually set different AGC gains		4.55		95.45	
$R_{AGC\_EN\_MIN}$	Minimum value of required external resistor on AGC_EN to ground to enable AGC mode (Information Only)		1			KΩ
$R_{AGC\_EN\_MAX}$	Maximum value of required external resistor on AGC_EN to ground to enable AGC mode (Information Only)				16.3	KΩ
$R_{PU\_AGC\_EN}$	Internal pull up resistor to VREG on AGC_EN		0.8	1	1.2	MΩ
AGC_Target[4]	Value of $\sqrt{(OUT0^2 + OUT1^2)}$	$V_{CC} = V_{CC\_33}$; T_A=25°C	54.5	59.5	64.5	%VCC
		$V_{CC} = V_{CC\_33}$; -40°C≤T_A≤160°C	53.5		65	
		$V_{CC} = V_{CC\_50}$; T_A=25°C	55	60	65	
		$V_{CC} = V_{CC\_50}$; -40°C≤T_A≤160°C	54		66	
AGC_FH	Automatic gain control - fast regulation region high threshold.	$V_{CC} = V_{CC\_33}$; T_A=25°C	75.5	78.9	83	%VCC
		$V_{CC} = V_{CC\_33}$; -40°C≤T_A≤160°C	75		83.5	
		$V_{CC} = V_{CC\_50}$; T_A=25°C	77	80.1	84	
		$V_{CC} = V_{CC\_50}$; -40°C≤T_A≤160°C	76		85	
AGC_SH	Automatic gain control - slow regulation region high threshold.	$V_{CC} = V_{CC\_33}$; T_A=25°C	66	68.8	73.5	%VCC
		$V_{CC} = V_{CC\_33}$; -40°C≤T_A≤160°C	65.5		74	
		$V_{CC} = V_{CC\_50}$; T_A=25°C	67	70	74	
		$V_{CC} = V_{CC\_50}$; -40°C≤T_A≤160°C	66.5		74.8	
AGC_SL	Automatic gain control - slow regulation region low threshold.	$V_{CC} = V_{CC\_33}$; T_A=25°C	45	48.6	52	%VCC
		$V_{CC} = V_{CC\_33}$; -40°C≤T_A≤160°C	44.5		52.5	
		$V_{CC} = V_{CC\_50}$; T_A=25°C	46.5	49.8	53	
		$V_{CC} = V_{CC\_50}$; -40°C≤T_A≤160°C	46		53.5	
AGC_FL	Automatic gain control - fast regulation region low threshold.	$V_{CC} = V_{CC\_33}$; T_A=25°C	34.5	38.3	42.5	%VCC
		$V_{CC} = V_{CC\_33}$; -40°C≤T_A≤160°C	34		43	
		$V_{CC} = V_{CC\_50}$; T_A=25°C	36.7	39.9	42.7	
		$V_{CC} = V_{CC\_50}$; -40°C≤T_A≤160°C	36		43.5	
Output Stage						
V_{OUT}	Output signal range	OUTxy pins single-ended measurement	7		93	%VCC
V_{REF_OUT}	Output reference voltage		48	50	52	
I_{ILIM_OUT}	Current limit source or sink on output pins		3		20	mA
I_{OUT}	Load current on output pins				1.5	
R_{PD_OUT}	Allowed range for resistor on OUT pins to GND for output pins during a detected fault condition. Refer to $V_{OUT\_FLT\_LOW}$ for error band		4		20	kΩ
R_{PU_OUT}	Allowed range for resistor on OUT pins to VCC for output pin during a detected fault condition. Refer to $V_{OUT\_FLT\_HIGH}$ for error band		4		20	

over operating free-air temperature range (unless otherwise noted)
over recommended V_{cc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Capacitors on OUT pins (Information Only)	R_{PD_OUT} = R_{PU_OUT} = 10kΩ, 8kHz rotation speed	1		8	nF
C_{OUT}	Capacitors on OUT pins (Information Only)	Maximum rotational speed limited	8		200	
I_{SCB_OUT}	Short circuit current into OUT pins when shorted to voltage higher than VCC	V_{OUT}>8V; VCC=5V			5	mA
$I_{OUT\_NOVCC\_DIFF}$	Leakage current in to each OUT pin when VCC is lost; Outputs used in differential mode.	VCC pin open; R_{PU_OUT} =5K on each OUTx pin; VCC=3.3V			12	µA
		VCC pin open; R_{PU_OUT} =5K on each OUTx pin; VCC=5.0V			25	
$I_{OUT\_NOVCC\_SE}$	Leakage current in to each OUT pin when VCC is lost; Outputs used in single-ended mode.	VCC pin open; R_{PU_OUT} =5K on each OUTxP pins; VCC=3.3V			17	
		VCC pin open; R_{PU_OUT} =5K on each OUTxP pins; VCC=5.0V			35	
$I_{OUT\_NOGND\_DIFF}$	Leakage current out of each OUT pin when GND is lost; Outputs used in differential mode.	GND pin open; R_{PD_OUT} = 5K on each OUTx pin; VCC=3.3V			30	µA
		GND open; R_{PD_OUT} = 5K on each OUTx pin; VCC=5.0V			50	
$I_{OUT\_NOGND\_SE}$	Leakage current out of each OUT pin when GND is lost; Outputs used in single-ended mode.	GND pin open; R_{PD_OUT} = 5K on each OUTxP pin; VCC=3.3V			35	
		GND pin open; R_{PD_OUT} = 5K on each OUTxP pin; VCC=5.0V			60	
$V_{OUT\_FLT\_LOW}$	Voltage on OUT pins in fault state with external pulldown resistors to ground on OUT pins	4KΩ ≤ R_{PD_OUT} ≤ 20KΩ on each OUTx pin; VCC=3.3V;5.0V; -40°C ≤ TA ≤ 160°C			4	%VCC
$V_{OUT\_FLT\_HIGH}$	Voltage on OUT pins in fault state with external pullup resistors to VCC on OUT pins	4KΩ ≤ R_{PU_OUT} ≤ 5KΩ on each OUTx pin; VCC=3.3V; -40°C ≤ T_A ≤ 160°C	96			%VCC
		4KΩ ≤ R_{PU_OUT} ≤ 10KΩ on each OUTx pin; VCC=5.0V; -40°C ≤ T_A ≤ 160°C	96			
$I_{OUT\_LK\_PU}$ (2)	Leakge current on OUT pins in fault state with external pullup resistors to VCC on OUT pins when V_{OUTx} > $V_{OUT\_FLT\_HIGH}$	5KΩ ≤ R_{PU_OUT} ≤ 20KΩ on each OUTx pin; VCC=3.3V; -40°C ≤ T_A ≤ 160°C			30	µA
		10KΩ ≤ R_{PU_OUT} ≤ 20KΩ on each OUTx pin; VCC=5.0V; -40°C ≤ T_A ≤ 160°C			20	

(1) Guaranteed by design
(2) Not tested in production
(3) This INL error is not same as INL error in calculated angle in the external MCU
(4) (AGC_SH-AGC_TARGET) and (AGC_TARGET-AGC_SL) ≥ 3% across temperature and allowed VCC range

7.6 Diagnostics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PD\_INxN\_BIST}$	Pull down current to GND during startup on INxN pins for sensor BIST		150	200	270	µA
$I_{PU\_INxP\_BIST}$	Pull up current from VREG during startup on INxP pins for sensor BIST		150	200	270	

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TH\_FALL\_INxP\_BIST}$	Falling threshold of window comparator for sensor BIST on INxP pins		22.7	25	30	%VREG
$V_{TH\_FALL\_INxN\_BIST}$	Falling threshold of window comparator for sensor BIST on INxN pins		70	75	77.3	
$I_{PU\_AGC\_EN\_BIST}$	Pull up current from VREG during startup BIST on AGC_EN pin to check short to ground		200	250	350	µA
V_{UVUTH_VCC}	VCC under voltage upper threshold(1)				4.5	V
V_{UVLTH_VCC}	VCC under voltage lower threshold(1)		3.6			
V_{OVUTH_VCC}	VCC over voltage upper threshold				6.5	
V_{OVLTH_VCC}	VCC over voltage lower threshold		5.6			
C_{LOSS_VREG}	VREG external capacitor loss check. Capacitor values below this will trigger a fault.	5V VCC mode only	1			nF
V_{OVUTH_VREG} (3)	VREG overvoltage upper threshold				4.2	V
V_{OVLTH_VREG}	VREG overvoltage lower threshold		3.6			
$V_{POR\_VREG\_uth}$	VREG power-on upper threshold				3.15	V
$V_{POR\_VREG\_lth}$	VREG power-on lower thershold		2.91			
f_{FLTH_LC}	LC oscillator frequency too high fault detection		5.3		6.2	MHz
f_{FLTL_LC}	LC oscillator frequency too low fault detection		2.0		2.4	
$I_{PU\_LCx\_BIST}$	Pull up current from VREG during startup on LCOUT and LCIN pins for sensor BIST		1.7	2.6	4.0	mA
$I_{PD\_LCx\_BIST}$	Pull down current to GND during startup on LCOUT and LCIN pins for sensor BIST		1.7	2.6	4.0	
$t_{MIN\_PH\_IMB}$	Minimum time between zero crossing of sine output and the following zero crossing of cosine output and vice versa to not signal a phase imbalance fault(2).		8.5	10	11.5	µs
$VAL_{AGC\_INP\_OOR\_L}$	AGC quantized step out of 256 (min to max gain) in auto gaib mode to signal FAULT when input signal is very low amplitude		251			AGC code
$VAL_{AGC\_INP\_OOR\_H}$	AGC quantized step out of 256 (min to max gain) in auto gain modet o signal FAULT when input signal is very high amplitude				4	
$V_{OOR\_H\_INx\_PIN}$	Out of range single ended fault threshold voltage for each IN pin - High		70	75	77.3	%VREG
$V_{OOR\_L\_INx\_PIN}$	Out of range single ended fault threshold voltage for each IN pin - Low		22.7	25	30	%VREG
$V_{OOR\_H\_INx\_LPF}$	Out of range single ended fault threshold voltage at low pass filter output - High		87.5	92.5	98	%VREG
$V_{OOR\_L\_INx\_LPF}$	Out of range single ended fault threshold voltage at low pass filter output - Low		1	7.5	12	%VREG
$V_{OOR\_H\_OUTx\_PIN}$	Out of range single ended fault threshold voltage for each OUT pin - High		93	95	97	%VCC
$V_{OOR\_L\_OUTx\_PIN}$	Out of range single ended fault threshold voltage for each OUT pin - Low		3	5	7	%VCC
$V_{CM\_H\_OUTx\_PIN}$	Deviation of output common mode above V_{REF_OUT} to trigger a FAULT		0.8		10	%VCC
$V_{CM\_L\_OUTx\_PIN}$	Deviation of output common mode below V_{REF_OUT} to trigger a FAULT		0.8		10	%VCC
$V_{OUTx\_SHRT\_P\_CMP\_OFF}$	Offset between internal AGC diffrential output value and OUTxP differential value before short between OUTxP pins is detected.		+100	+250	+440	mV

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUTx\_SHRT\_N\_CMP\_OFF}$	Offset between internal AGC diffrential output value and OUTxN differential value before short between OUTxN pins is detected.		-380	-250	-100	mV
V_{UV_DVDD}	Internal Digital Supply undervoltage check.		1.2		1.3	V
$V_{TOGGLE\_AGC\_EN}$	Checks if the comparator on AGC_EN toggles after AGC_EN status determination		50		200	mV
T_{TSD_rise}	Abmient temperature above which thermal shutdown fault is triggered.			190		℃
T_{TSD_fall}	Abmient temperature below which thermal shutdown fault is cleared			160		℃

(1) Continuously checked in VCC = 5V mode. Ignored in VCC=VREG=3.3V mode
(2) Fault is signaled only at occurance of 3 consecutive violations of the minimum time.
(3) Device will continue normal operation until the over-voltage threshold on VREG triggered

7.7 Switching Characteristics

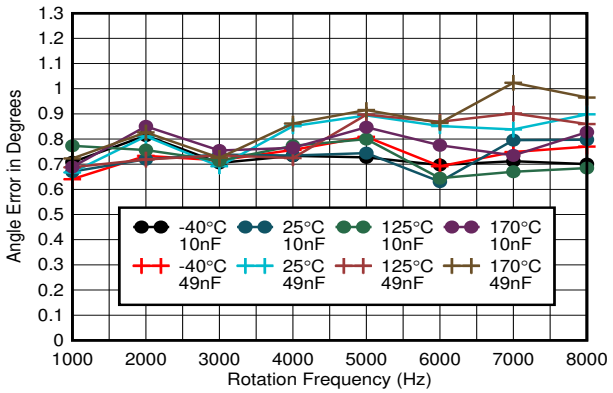
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VCC\_FLT\_DT}$	Deglitch time for VCC over voltage and under voltage detection		180	200	220	µs
$t_{VREG\_OV\_DT}$	Deglitch time for VREG over voltage detection		180	200	220	µs
$t_{LC\_FLT\_DT}$	Deglitch times for LC amplitude related faults		180	200	220	µs
$t_{AGC\_EN\_DT}$	Deglitch time for AGC_EN pin for AGC mode detection		2.7	3	3.3	µs
$t_{AGC\_EN\_TGL\_DT}$	Deglitch time on AGC_EN pin toggle fault after power up into normal state		450	500	550	µs
$t_{IN\_OOR\_DT}$	Deglitch time applied to each input out of range signal individually		180	200	220	µs
$t_{INx\_FLT\_DT}$	Deglitch time applied to the fault signal determined by OR of all individual input out of range faults which are deglitched for $t_{IN\_OOR\_DT}$		180	200	220	µs
$t_{LPF\_OOR\_DT}$	Deglitch time for AFE Low Pass Filter Out of Range check		180	200	220	µs
$t_{OUT\_OOR\_DT}$	Deglitch time for output voltage out of range fault.		180	200	220	µs
$t_{OUTx\_SHORT\_DT}$	Deglitch time for AFE Output Short detection		450	500	550	µs
$t_{OUT\_CM\_DT}$	Deglitch time for OUT pin common mode check		90	100	110	µs
$t_{OUT\_ZC\_DT}$	Deglitch time for OUT differential output zero crossing fault detection		9	10	11	µs
$t_{AGC\_ZC\_DT}$	Deglitch time for AGC differential output zero crossing fault detection		9	10	11	µs
$t_{AGC\_CMP\_DT}$	Deglitch time to detect AGC fast/slow amplitude regulation threshold has been crossed		180	200	220	ns
$t_{AGC\_VAL\_DT}$	Deglitch time for AGC OOR range faults		180	200	220	µs
t_{FLT_RECOV}	Fault recovery time once device tranistions from FAULT to DIAGNOSTIC state	C_{EXT_VREG}=680nF, 2.2µF	12		16	ms
t_{PWR_ON}	From VREG power on until OUTx pins are released from HI-Z state.	C_{EXT_VREG}=680nF, 2.2µF	10		14	ms

over operating free-air temperature range (unless otherwise noted)

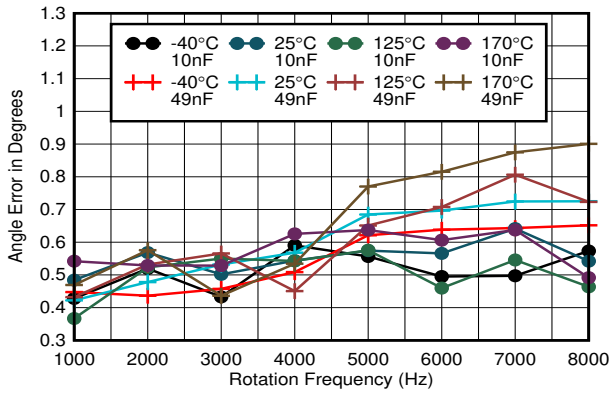
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PRWR\_ON\_DT}$	Deglitch time after t_{PWR_ON} for which OUTx faults are ignored.		302	336	370	µs

7.8 Typical Characteristics



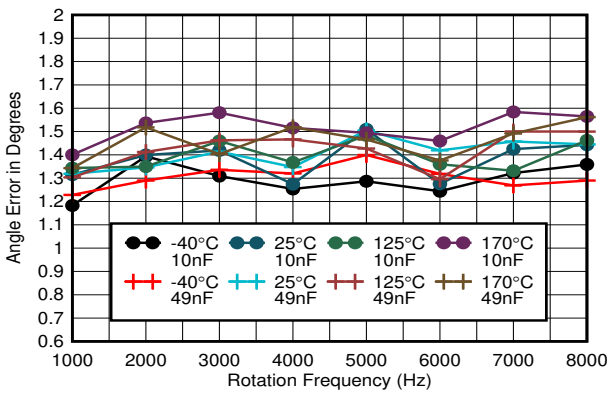
VCC = 5V, LC_{freq}=5MHz, Ideal Inputs, No offset and gain correction
Signal path delay compensated

図 7-1. Angle Error VCC = 5 V, C_{OUT} < 50 nF



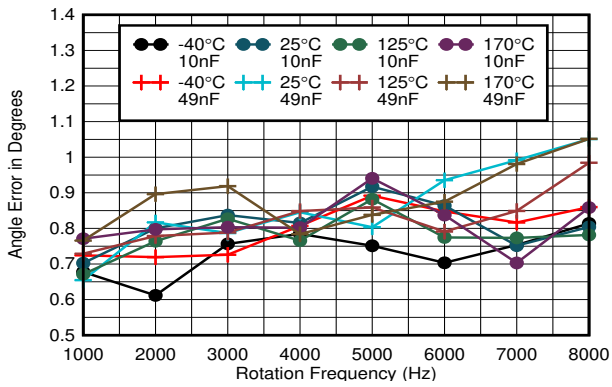
VCC = 5V, LC_{freq}=5MHz, Ideal Inputs, With offset and gain correction
Signal path delay compensated

図 7-2. Angle Error VCC = 5 V, C_{OUT} < 50 nF



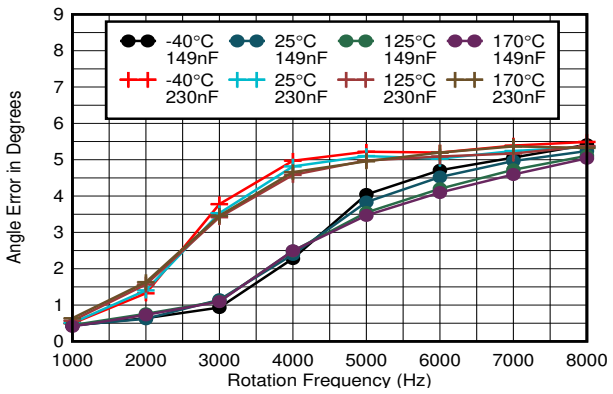
VCC = 3.3V, LC_{freq}=5MHz, Ideal Inputs, No offset and gain correction
Signal path delay compensated

図 7-3. Angle Error VCC = 3.3 V, C_{OUT} < 50 nF



VCC = 3.3V, LC_{freq}=5MHz, Ideal Inputs, With offset and gain correction
Signal path delay compensated

図 7-4. Angle Error VCC = 3.3 V, C_{OUT} < 50 nF



VCC = 5V, LC_{freq}=5MHz, Ideal Inputs, With offset and gain correction
Signal path delay compensated

図 7-5. Angle Error VCC = 5 V, C_{OUT} > 100 nF

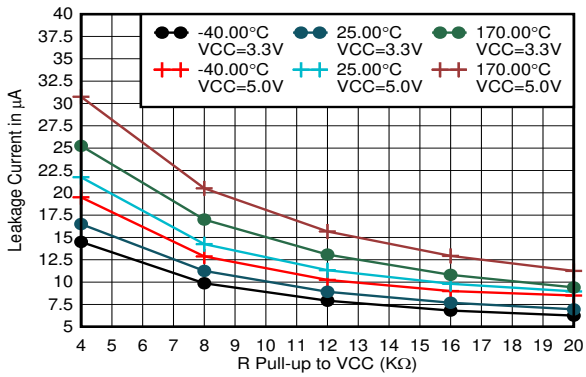


図 7-6. OUTx Pin Leakage Current When Device is in a SAFE State and Output Pulled to VCC With R Pull-up

8 Detailed Description

8.1 Overview

The LDC5072-Q1 is an inductive position sensor front-end IC for use in automotive and industrial applications. The sensor typically consists of an excitation coil and a set of two receiver coils, all drawn on the same PCB. The sensor also has a metal target which is typically printed on another PCB. The coil PCB is mounted in a fixed position on the motor and the metal target is mounted on a rotating shaft. The device excites the excitation coil, which then couples to the receiver coils. The amount of coupling from the excitation to receiver coils depends on the relative position of the metal target to the receiver coils and also on the air gap between the coil PCB and the target. The LDC5072-Q1 has an LC oscillator driver that can drive an excitation coil with a constant amplitude and supports a wide range of LC combinations.

Two receiver coils are placed such that the LDC5072-Q1 outputs are shifted by 90°. These Sine and Cosine outputs are ratiometric to each other and can be used to calculate the angle at any given instant. The LDC5072-Q1 receiver filters out the out-of-band noise, demodulates, and amplifies the signal. The device has a gain block that can be either set manually or in automatic mode. In automatic mode, the LDC5072-Q1 will regulate output amplitude to a fixed band, which can remove sensor variability such as the lifetime variation of air gap. The device has two differential output drivers that can drive a wide range of capacitive loads. Typically these are digitized by an ADC of an MCU for further angle calculation, for motor control, or for linear position information extraction.

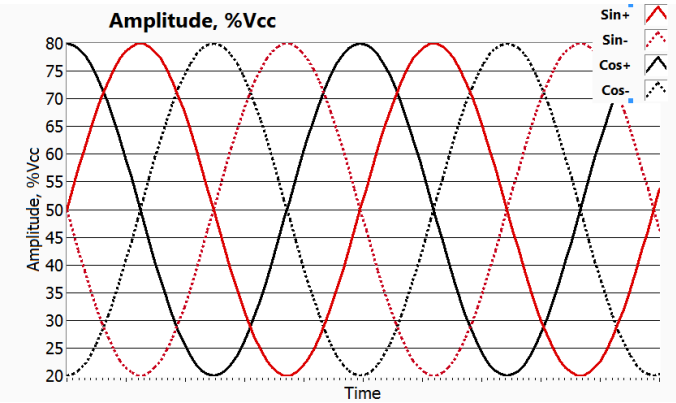
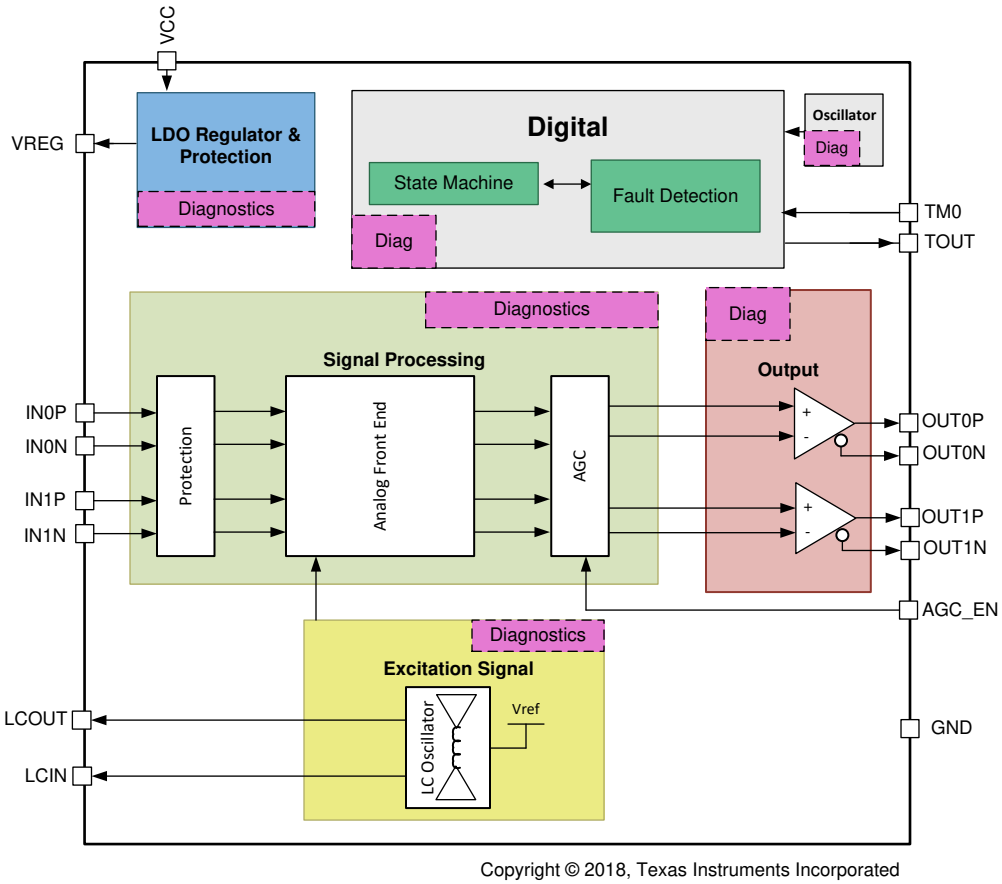


図 8-1. LDC5072-Q1 Typical Output

The LDC5072-Q1 was developed in accordance with ISO 26262 to support functional safety. The device implements a pin-level built-in self-test at power up to check for sensor pins open, shorts to supplies, and short between the coils. The device also has analog and digital built-in self-test to test internal safety mechanisms. The LDC5072-Q1 also implements run-time checks to continuously monitor sensor functionality. In an event that a fault is detected, the output drivers are driven to high-impedance state.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Supply Voltage

The main voltage supply for this device is on the VCC pin. The VCC pin can be supplied either by a 3.3-V or 5-V regulator. This pin is protected internally from possible negative voltages on the pin and from possible back-feeding of current from the device to the regulator. The pin can also withstand voltages as high as 30 V. For 3.3-V mode, the VREG and VCC pins are shorted together on the PCB.

There is an internal 3.3-V regulator with a capacitor on the VREG pin. This regulator is the supply for all internal blocks, the LC oscillator, and the regulator is also used as a reference block for various sections of the signal chain. Additionally, an internal 1.5-V regulator supplies the digital logic. This device has two modes of operation: a 5-V supply mode and a 3.3-V supply mode. For 5-V supply mode, 5 V is required on the VCC pin that the internal regulator will use to generate voltage on VREG. For 3.3-V supply mode, the VREG and VCC pins must be connected externally and supplied with regulated 3.3 V. This will change the common-mode voltage on the device outputs, because this voltage is derived from half the value on the VCC pin. The device includes an automatic check to figure out which mode the device is in during power up.

8.3.2 Excitation Signal

The excitation signal is generated by an LC oscillator. The LCIN and LCOUT pins will be connected to the excitation coil. The oscillator signal driver automatically regulates the signal to V_{AMP_LC}. The user can adjust the external capacitors on LCIN and LCOUT to select the excitation frequency. For best performance, two capacitors should be used. One should be placed from LCIN to ground and the other from LCOUT to ground (C_1 and C_2). This is instead of using one capacitor between LCIN and LCOUT.

Use 式 1 to calculate the excitation frequency.

$$f_{OSC\_LC} = \frac{1}{2\pi \times \sqrt{\left(L \times \left(\frac{C_1 \times C_2}{C_1 + C_2} \right) \right)}} \quad (1)$$

where

- L is inductance of excitation coil
- C1, C2 are the external capacitors on LCIN and LCOUT, respectively

8.3.3 Signal Processing Block

The inputs to the signal processing block come from the outputs of the receiver coils of the position sensor. This block will demodulate the position signals, filter out noise, and amplify the signal in preparation for angle calculation by an external control unit. The first stage of the signal processing block contains ESD protection circuitry and sets the common-mode voltage. The second stage of this block is an EMC filter to eliminate noise. The next stage of this block is a demodulator for the input signals. This demodulation uses the frequency of the LC oscillator as a reference. The signals will then go through a low-pass filter with fixed gain. The last stage in the signal processing block is a gain stage where the gain is either set by an automatic gain control routine (AGC_EN pin pulled to GND through an external resistor), or set to a fixed gain by the voltage on the AGC_EN pin. The signal path gain for both channels is same and are matched very closely by careful design.

図 8-2 shows a block diagram of the analog front-end in the IC that demodulates the incoming signal to extract position information.

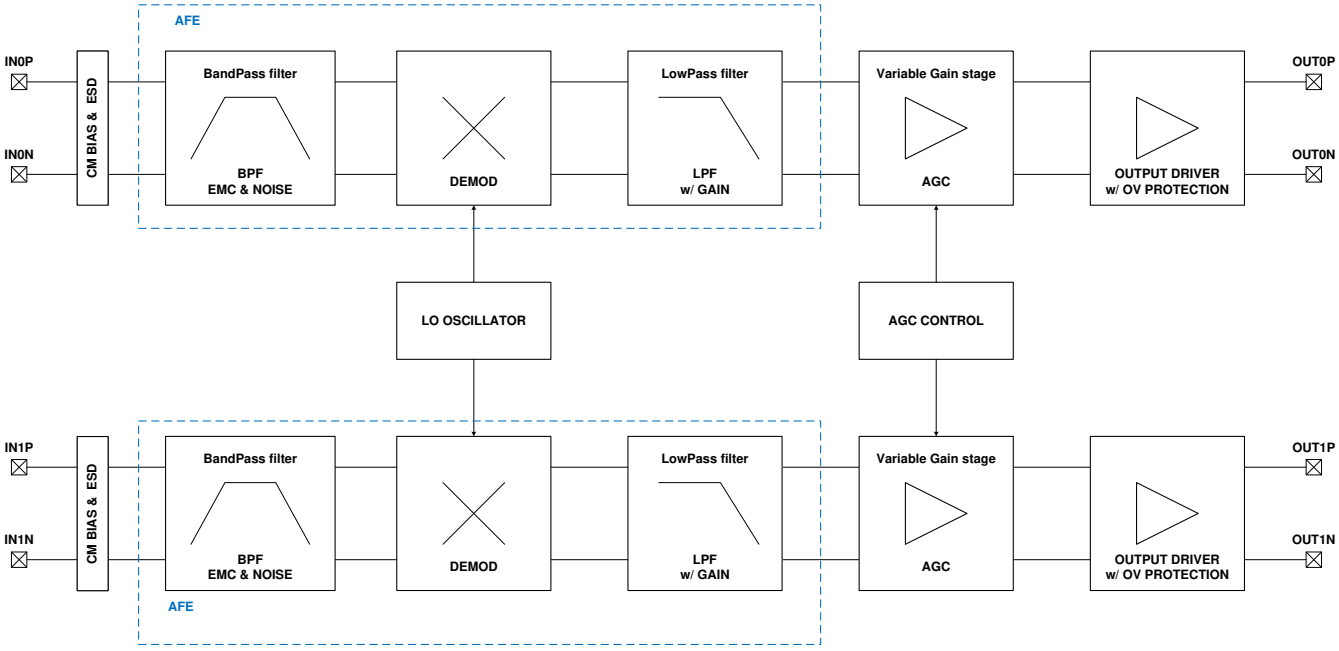


図 8-2. Signal Processing Block Diagram

8.3.3.1 Demodulation

The receive path for the sine path can be modeled by 式 2 through 式 5.

$$RXi_{sin} = V_{AMP\_LC} \times \eta \times \sin\left(2 \times \pi \times f_{OSC\_LC} \times t\right) \times \sin(\Theta) \quad (2)$$

where

- RXi_{sin}: Receiver path sine coil input
- V_{AMP_LC}: LC oscillator signal amplitude
- η: Coupling factor between exciter and receive coil
- f_{OSC_LC}: LC oscillator excitation frequency
- Θ: Instantaneous motor angle

$$Demod_{sin} = G_{MIXER} \times G_{BPF} \times V_{AMP\_LC} \times \eta \times \sin(\Theta) \times \frac{1}{2} \times \left(1 + \sin\left(2 \times \pi \times f_{OSC\_LC} \times t\right)\right) \quad (3)$$

where

- $Demod_{sin}$: Demodulator sine path output
- V_{AMP_LC}: LC oscillator signal amplitude
- η: Coupling factor between exciter and receive coil
- f_{OSC_LC}: LC oscillator excitation frequency
- Θ: Instantaneous motor angle
- G_{MIXER}: gain due to the mixer
- G_{BPF}: gain due to the bandpass filter

$$LPF_{sin} = \frac{1}{2} \times G_{MIXER} \times G_{BPF} \times G_{LPF} \times V_{AMP\_LC} \times \eta \times \sin(\Theta) \quad (4)$$

where

- LPF_{sin}: Low pass filter sine path output
- V_{AMP_LC}: LC oscillator signal amplitude
- η: Coupling factor between exciter and receive coil
- Θ: Instantaneous motor angle
- G_{MIXER}: gain due to the mixer
- G_{BPF}: gain due to the bandpass filter
- G_{LPF}: gain due to the lowpass filter

$$V_{OUT\_SIN} = \frac{1}{2} \times G \times V_{AMP\_LC} \times \eta \times \sin(\Theta) \quad (5)$$

where

- $Vout_{sin}$: Signal output at the end of sine path
- V_{AMP_LC}: LC oscillator signal amplitude
- η: Coupling factor between exciter and receive coil
- Θ: Instantaneous motor angle
- G: Total combined gain of the signal path

The cosine path can be modeled in the same way as sine path.

The total gain of the system is a combination of the gain control, mixer gain, and fixed gain. It can be modeled by 式 6:

$$G = G_{FIXED} \times G_{MIXER} \times G_{GC} \quad (6)$$

where

- G_{FIXED} is the fixed gain in the signal path, including G_{LPF} and G_{BPF}
  - G_{FIXED} = 43.2 for VCC = 5 V
  - G_{FIXED} = 28.8 for VCC = 3.3 V
- G_{MIXER} is the gain due to the mixer. The typical value is 0.637.
- G_{GC} is the variable gain in the signal path. This is either selected by the AGC or the Fixed Gain Control depending on the voltage on the AGC_EN pin.

8.3.3.2 Fixed Gain Control

To set the gain of the final gain stage, a voltage in the range of $V_{AGC\_EN\_MANUAL}$ must be applied to the AGC_EN pin. This gain setting will be set during the DIAGNOSTICS state. A change in the voltage on AGC_EN affects the AGC gain the next time the device enters the DIAGNOSTICS state, either during the next power up of the device or during fault recovery. The nominal value of minimum gain of this stage is 0.375 and the maximum gain is 60.375. The gain is implemented as linear in dB scale with 256 steps. This gain is rotation frequency dependent. For higher rotation speeds, the gain value will fall off. 式 7 shows the gain in linear scale is related to the voltage on AGC_EN pin as a percentage of VREG:

$$\text{Gain} = 0.375 + 0.759 \times \left(10^{\left(1.903 \times \left(\frac{\%VReg - 4.55}{90.9}\right)\right)} - 1 \right) \quad (7)$$

where

- Gain is the effective gain set by gain control block.
- %VREG is the voltage on AGC_EN pin expressed as percentage of voltage on the VREG pin.

The voltage applied on AGC_EN pin should fall within $V_{AGC\_EN\_MANUAL}$ range.

8.3.3.3 Automatic Gain Control

When the voltage on the AGC_EN pin is below $V_{AGC\_EN\_AUTO}$, the manual gain control function is disabled and the Automatic Gain Control (AGC) is enabled.

In AGC mode, the device will change the gain of the last stage of the signal processing block to keep the final output within an appropriate voltage range on VOUT. The AGC block uses the square root of the sum of the squared amplitudes of the two channels to sense amplitude of output signals and set gain selection. Both channels will have the same gain. This means that the AGC block will set the gain for sine and cosine channels such that the quantity AGC_TARGET as defined in 式 8 is within the ranges listed in *Specifications*.

$$\text{RADIUS} = \frac{\sqrt{(OUT1P - OUT1N)^2 + (OUT0P - OUT0N)^2}}{VCC} \quad (8)$$

where

- OUTxx: Voltage on the output pins
- VCC: Voltage on the VCC pin
- AGC_TARGET: Regulation target for the AGC block

The AGC sets the gain in the DIAGNOSTICS state and then dynamically regulates it in NORMAL state. There are two regions of regulation, the slow AGC regulation region and the fast AGC regulation region. This is shown in 図 8-3. The blue curve shows the ratio defined by 式 8 as percentage of VCC. If the ratio rises above AGC_FH or falls below AGC_FL, fast regulation becomes active, and the gain is changed by four gain codes every nominal value of 819.2 µs. If the ratio falls between AGC_SH and AGC_FH, or between AGC_FL and AGC_SL, slow regulation is active, and the gain is changed by one code approximately every 840mS. To allow for faster

settling of the output during power up in diagnostic state, the device changes gain by one code every 3.2 µs in slow AGC region and eight codes every 3.2 µs in the fast AGC region. The thresholds are listed in *Specifications*. The gain step size is constant in dB scale and is approximately equal to 0.15 dB. 図 8-3 shows the two cases: a fast change (for example, due to a transient), and a slow change due to lifetime drift.

The AGC block thus will try to compensate for changes in amplitude of the input signal or changes in VCC. If the ratio, after reaching AGC_TARGET, stays between AGC_SH and AGC_SL, then AGC does not react and does not change the gain. The AGC block engages if one of the thresholds is crossed, and it will try to change the output amplitudes such that the ratio reaches AGC_TARGET again. Hence, the No Gain Control region in 図 8-3 causes the AGC block to have some hysteresis.

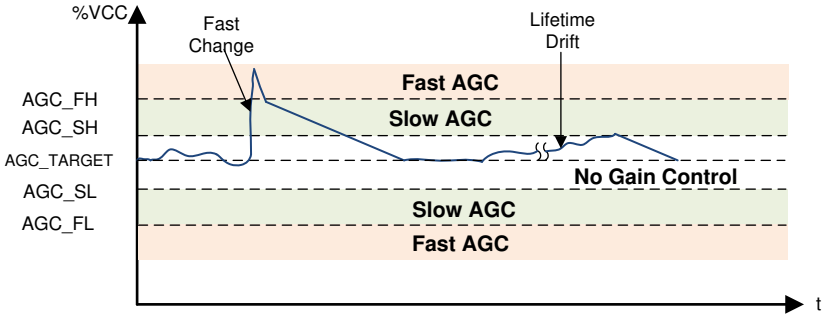


図 8-3. AGC Regulation Bands

8.3.4 Output Stage

The output stage consists of buffers that drive each of the outputs differentially and maintain the output common mode at V_{REF_OUT} as specified in *Specifications*. There are two output stages, one at the OUT0x pins and the other at the OUT1x pins, and each drive the pins in a push-pull manner. For a rotating input, one set of pins will represent the sine angle information and other set will represent cosine angle information. The output stages buffer the AGC output and outputs the final demodulated position information to be used by a microcontroller. The output stage is designed such that it can drive a large range of capacitive loads.

The output stage requires external capacitors as specified by C_{OUT} and pullup or pulldown resistors as specified by R_{PD_OUT} and R_{PU_OUT}. The OUTx pins enter a high impedance state in the case of a fault, so the pullup and pulldown resistors are used to pull the voltage out of range for detection by the MCU. See *External Diagnostics Required for Loss of VCC or GND* for details about external diagnostics required for loss of VCC or GND conditions.

There is a possibility that wires connecting to OUT0 and OUT1 pins can be routed outside the sensor module, so the output stage has both negative and high voltage protection to prevent the part from getting damaged in the event of shorts. The output stage also has out-of-range fault detection. The diagnostic coverage on output stage will also check if the output signal is being driven outside of the maximum allowable limit as defined in *Specifications* as shown in 図 8-4. In the event of a fault, the output stages are put in Hi-Z mode and external pullup and pulldown resistors will drive OUTx pins to maximum and minimum signaling a fault to the microcontroller. See *Diagnostics* for details.

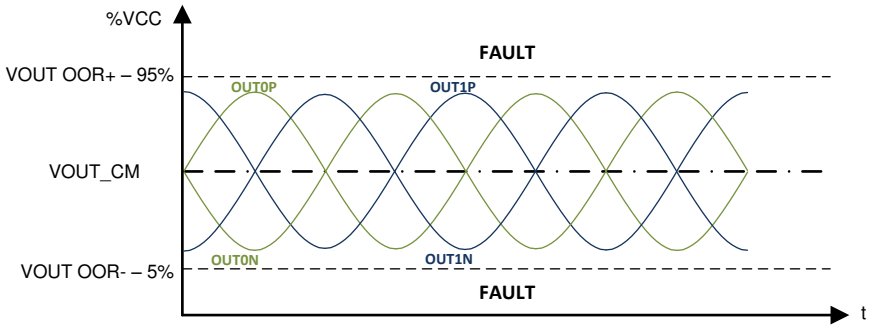


図 8-4. Out of Operation Fault Detection Range at the Output

注

The voltage at the OUTx pins is not ratiometric to VCC. In AGC mode, the calculated RADIUS in 式 8 value will change. Only if it crosses one of the threshold (depending on change magnitude of VCC), then the gain of AGC will be adjusted accordingly to bring the RADIUS value back to AGC_TARGET. In fixed-gain mode, the gain will not be adjusted even if VCC change by large magnitude.

8.3.5 Diagnostics

The LDC5072-Q1 is equipped with numerous diagnostics features to detect, monitor, and report failures that either existed before the power up or occurred during device operation. In the event of a failure, the LDC5072-Q1 is placed either in IDLE, DISABLED, or FAULT state (based on the failure nature), the LC Oscillator is turned off, the AFE is disabled, and the output pins are tri-stated, and consequently, are pulled up or down by external resistors. From the FAULT state, the LDC5072-Q1 returns to DIAGNOSTICS state if the fault condition is removed. From the DISABLED state, the LDC5072-Q1 is moved to IDLE state after a Power Cycle (see *Device Functional Modes*).

The LDC5072-Q1 tri-states its output to signal a fault. As shown in *Application and Implementation*, it is expected that a combination of pullup or pulldown resistors are added on OUTx pins at the termination site (that is, at the microcontroller). The values of these resistors are specified as R_{PU_OUT} and R_{PD_OUT} in *Specifications*. The resistors are generally pulled up to a supply (typically VCC) and pulled down to ground such that the ADC code on the MCU is out of the expected range. This will signal a fault to the microcontroller.

8.3.5.1 Undervoltage Diagnostics

The LDC5072-Q1 continuously monitors the VREG and DVDD voltage while in DIAGNOSTICS, NORMAL, FAULT, and DISABLED states. If the VREG or DVDD drops below the specified limits (see *Electrical Characteristics*), the LC Oscillator is turned off, the AFE is disabled, and the output pins are tri-stated if neither were done so yet. Upon voltage recovery, the device transitions to the IDLE state and initiates regular Power-On Reset.

8.3.5.2 Initialization Diagnostics

During power up in the DIAGNOSTICS state, the LDC5072-Q1 undergoes a number of self-diagnostics and checks (for fault thresholds refer to *Diagnostics* and for de-glitch times refer to *Switching Characteristics*):

1. EEPROM CRC check: the LDC5072-Q1 calculates the CRC value of the EEPROM register settings and compares it to the recorded expected CRC value. In case of FAULT, the LDC5072-Q1 transitions to the DISABLED state.
2. LBIST check: the LDC5072-Q1 undergoes automated self-testing pattern for the digital logic. In case of FAULT, the LDC5072-Q1 transitions to the DISABLED state.
3. ABIST check: the LDC5072-Q1 undergoes automated self-testing pattern for the fault-monitoring circuits. In case of FAULT, the LDC5072-Q1 transitions to the DISABLED state.
4. Sensor interface BIST check: the LDC5072-Q1 applies the automated test patterns to Sensor interface (LCIN, LCOUT, IN0P, IN0N, IN1P, and IN1N) pins to check that they are open or shorted to GND or battery. It

also checks if there is a short between the coils of the sensor and if any of the coils are open. The LDC5072-Q1 will also check if any impedance is present as specified by the $R_{AGC\_EN\_AUTO}$ or $R_{PU\_AGC\_EN}$ on the AGC_EN pin and check if the AGC_EN pin is not shorted to GND.

5. VREG cap loss check: the LDC5072-Q1 uses the VREG cap to compare the internal time constant with the external time constant (5-V VCC mode only). This check is only performed at power up and is not performed if the device transitions from FAULT state to DIAGNOSTICS state. The maximum capacitance on VREG pin that can trigger this fault is given by C_{LOSS_VREG}.
6. The LDC5072-Q1 enables the LC oscillator and checks that $V_{UVL\_AMP\_LC}$, $V_{OVH\_AMP\_LC}$, $V_{UVL\_CM\_LC}$, and $V_{OVH\_CM\_LC}$ faults disappear within $t_{LC\_FLT\_DT}$.
7. The LDC5072-Q1 enables the AFE, AGC, and Output stages in a staggered manner.
8. The LDC5072-Q1 the device resets all checks and faults for certain period of time to allow all internal signals to settle and then starts monitor faults
9. The LDC5072-Q1 transitions to the Normal state ensuring that t_{PRWR_ON} is met and no other faults are detected. In AUTO AGC mode, the LDC5072-Q1 also checks that the output of the AGC block is within AGC_Target. If the AGC block is not within AGC_Target, the devices transitions to the DISABLED state.

8.3.5.3 Normal State Diagnostics

During normal device operation, a number of parameters are continuously monitored

For the following parameters, if a fault condition is detected, the device is transferred to the FAULT state. Only if the fault condition is cleared then the part transitions to DIAGNOSTIC state (for fault thresholds refer to *Diagnostics* and for de-glitch times refer to *Switching Characteristics*):

- VCC overvoltage check: if the VCC voltage exceeds the V_{OVUTH_VCC}, fault condition is detected in the $t_{VCC\_FLT\_DT}$. This fault detection delay allows the LDC5072-Q1 to filter out short glitches on the VCC pin. Once the voltage drops below the V_{OVLTH_VCC}, the fault condition is cleared.
- VCC undervoltage check (active only in VCC = 5 V mode): if the VCC voltage falls below the VCC_{UVLTH}, fault condition is detected in the $t_{VCC\_FLT\_DT}$. This fault detection delay allows the LDC5072-Q1 to filter out short glitches on the VCC pin. Once the voltage rises above the V_{UVUTH_VCC}, the fault condition is cleared.
- VREG overvoltage check: if the VREG voltage exceeds the V_{OVUTH_VREG}, fault condition is detected in the $t_{VREG\_OV\_DT}$. This fault detection delay allows the LDC5072-Q1 to filter out short glitches on the VREG pin. Once the voltage drops below the V_{OVLTH_VREG}, the fault condition is cleared.
- Thermal Shutdown Check: If the temperature of the die increases and crosses T_{TSD_rise}, a fault condition is detected. Once the die temperature falls below T_{TSD_fall}, the fault condition is cleared.

For the following parameters, if a fault condition is detected, the device is transferred to the FAULT state and then to the DIAGNOSTICS state to attempt recovery and detect if the fault is still present. The zero-crossing mentioned in this section refers to crossing of the common voltage of a differential signal pair.

- LC oscillator frequency check: if the LC tank oscillation frequency exceeds the f_{FLTH_LC} or falls below the f_{FLTL_LC} parameter, fault condition is detected in the t_{FAULT_DT}. This fault detection delay allows the LDC5072-Q1 to filter out short glitches on the LC tank pins.
- LC Loop control check: checks for amplitude and common mode voltage loop of the LC oscillator by monitoring internal node voltages with a comparator. The fault condition de-gltiched for $t_{LC\_FLT\_DT}$.
- Output signal Out-Of-Range check: if the voltage on one of the four OUT pins exceeds the $V_{OOR_H_OUTx}$_PIN threshold, or falls below the $V_{OOR\_L\_OUTx}$ threshold parameter, fault condition is detected in the $t_{OUT\_OOR\_DT}$.
- Output signal voltage check: this diagnostic compares the states of the zero-crossing comparators of OUT pins with the corresponding zero-crossing comparators of the AGC block outputs. A valid rotational signal must be present for this check, and the detection time, will depend on the rotational speed of the motor.
- Output signal common mode check: this diagnostic detects the OUT0 and OUT1 pin pairs deviation from the expected common-mode voltage. If V_{OUT0P}+V_{OUT0N} is greater than the range defined by $V_{CM\_H\_OUTx\_PIN}$ and $V_{CM\_L\_OUTx\_PIN}$, the fault is reported with a de-glitch time of $t_{OUT\_CM\_DT}$.
- Output pin short check: detects fault condition if any of the two output pins (OUTx) are shorted. It compares the differential output of each channel to the corresponding internal output of the AGC block (or fixed gain block for fixed gain mode) and flags a fault condition if the difference is greater than $V_{OUTx\_SHRT\_CMP\_OFF}$. The fault signal is de-glitched for $t_{OUTx\_SHORT\_DT}$ before signaling a fault. During this de-glitch period, the OUTx pins are enabled even while being shorted.

- Frequency imbalance check: given a valid rotation signal, the device monitors that exactly 1 zero-crossing of the sine output occurs between two consecutive zero-crossings of the cosine output, and vice versa. A valid rotation signal detected using zero-crossing information must be present for this check to be enabled and detection time will depend on the rotational speed of the motor. For this fault to be detected two conditions must be met:
  - The device has detected 1KHz rotation frequency and the measured rotation frequency on both channels is less than 10KHz
  - The rotation frequency range condition is met for 10 consecutive cycles or 20 half cycles
- Phase imbalance check: the device checks that there is a time delay of at least $t_{MIN\_PH\_IMB}$ between the zero crossing of sine output and the following zero crossing of cosine output, and vice versa.
- Input signal out of range check (valid only for AGC mode): if the AGC gain code of $VAL_{AGC\_INP\_OOR\_H}$ or greater, or $VAL_{AGC\_INP\_OOR\_L}$ or less, is required to keep the OUT signals in the AGC target range (AGC_Target), the input signals are out of range, and fault is reported. This fault is de-glitched for $t_{AGC\_VAL\_DT}$.
- Input signal out of range check: if input signals during normal operation cross $V_{OOR\_x\_INx\_PIN}$ thresholds multiple times in an interval, or, stays constantly above $V_{OOR\_H\_INx\_PIN}$ or below $V_{OOR\_L\_INx\_PIN}$ for $t_{IN\_OOR\_DT}$, the input signals are out of range, and fault is reported. The DC fault, combination of any of input signaling a fault after individual de-glitch time, is further de-glitched for $t_{INx\_FLT\_DT}$.
- Input signal out of range check: if LPF output signals during normal operation cross $V_{OOR\_x\_INx\_LPF}$ thresholds multiple times in an interval, or, stay above $V_{OOR\_H\_INx\_LPF}$ or below $V_{OOR\_L\_INx\_LPF}$ for $t_{LPF\_OOR\_DT}$, the input signals are out of range, and fault is reported.

For the following parameters, if a fault condition is detected, the device is transferred to the DISABLED state and a recovery is attempted (See *DISABLED State*):

- Register CRC check: the LDC5072-Q1 calculates the CRC value of the Safety-critical register settings and compares the CRC value to the recorded expected CRC value. In case of FAULT, the LDC5072-Q1 transitions to the DISABLED state. This check is performed continuously.
- Critical registers redundancy check: the device checks the validity of the critical registers vs its redundant copy. In case of a discrepancy, the device immediately transitions to the DISABLED state
- TM0 state check: the device checks if the TM0 pin state was changed after its state was determined during Initialization diagnostics.
- TOUT state check: the device checks if the TOUT pin state was changed after its state was determined during Initialization diagnostics.
- AGC_EN toggle check: the device checks if the AGC_EN state was changed after its state was determined during Initialization diagnostics. This check has a de-glitch time of $t_{AGC\_EN\_TGL\_DT}$

8.3.5.4 Fault State Diagnostics

While in the Fault state, a number of parameters are continuously monitored.

For the following parameters, if a fault condition is detected, the device stays in FAULT state until and unless the fault condition is removed and then the device transitions to DIAGNOSTIC state:

- The VCC overvoltage check as described in *Normal State Diagnostics*.
- The VCC undervoltage check as described in *Normal State Diagnostics*.
- The VREG overvoltage check as described in *Normal State Diagnostics*.
- The thermal shutdown check as described in *Normal State Diagnostics*.

For the following parameters, if a fault condition is detected, the device is transferred to the DISABLED state and a recovery is attempted (see *DISABLED State*):

- The Critical registers redundancy check as described in *Normal State Diagnostics*.
- The TM0 state check as described in the *Normal State Diagnostics*.
- The TOUT state check as described in the *Normal State Diagnostics*.
- The AGC_EN toggle check as described in *Normal State Diagnostics*.

For all other faults, the device attempts recovery by transitioning to DIAGNOSTIC state while the OUTx pins remain in FAULT signaling state.

8.4 Device Functional Modes

The LDC5072-Q1 is driven by a state machine. The state machine is initialized upon power up, and the machine goes through the initial diagnostics routines. If the system functions normally, the device moves to a normal operational state and starts to drive the OUT pin to indicate angular information. In case of a fault, the device moves to the FAULT state, the LC oscillator driver is disabled, and the OUT pins are tri-stated to indicate fault condition until the FAULT condition is removed or the IC is power-cycled. Some critical faults will lead to the disabled state, which requires a power-cycle to recover.

図 8-5 shows the different device states. The management of faults is divided into four types of faults as shown in 表 8-1:

- Initialization faults: These faults occur during initialization and transitions the device to DISABLED state and the device indicates a fault at the OUTx pins.
- Run Time #1 faults: These faults are checked in NORMAL state and transition the device to FAULT state. For these type of faults, the device will try to recover from FAULT state when the fault condition is removed and by transitioning to the DIAGNOSTIC state.
- Run Time #2 faults: These faults are critical faults which are checked in NORMAL state and transition to DISABLED state. A recovery is attempted from this state as described in *DISABLED State*.
- Reset faults: These faults will put the part in reset and the device will power up again once the conditions causing the fault are cleared.

表 8-1. Diagnostic List

RESET FAULTS	INITIALIZATION FAULTS	RUN TIME FAULTS # 1	RUN TIME FAULTS # 2
VREG UNDER VOLTAGE CHECK	EE CRC CHECK	VCC OV/UV CHECK(1)	CRITICAL REGISTERS REDUNDANCY CHECK
DVDD UNDER VOLTAGE CHECK	LBIST CHECK	FREQUENCY CHECK	REGISTER CRC CHECK
	ABIST CHECK	LC OSCILLATOR VOLTAGE CHECK	TM0 PULL UP CHECK
	SENSOR INTERFAFE BIST CHECK	PHASE IMBALANCE CHECK	T0UT PULL UP CHECK
	VREG CAP LOSS CHECK	INPUT SIGNAL OUT OF RANGE CHECK	AGC_EN TOGGLE CHECK
	AGC_EN BIST CHECK	OUTPUT SIGNAL OUT OF RANGE CHECK	
		OUTPUT SIGNAL VOLTAGE CHECK	
		OUTPUT SIGNAL COMMON MODE CHECK	
		OUTPUT SHORT CHECK	
		FREQUENCY IMBALANCE CHECK	
		TSD CHECK(1)	
		VREG OV CHECK(1)	

(1) These faults force the device to stay in FAULT state and not allow attempt for recovery till the fault causing condition is removed.

図 8-5 shows the states and the transitions for the LDC5072-Q1. Following states are considered SAFE state where the device has detected a fault and indicates a fault making all the OUT pins high-impedance:

- IDLE
- FAULT
- DISABLED

In diagnostic state, the device indicates faults till all checks are complete and then drives the OUT pins to correct values.

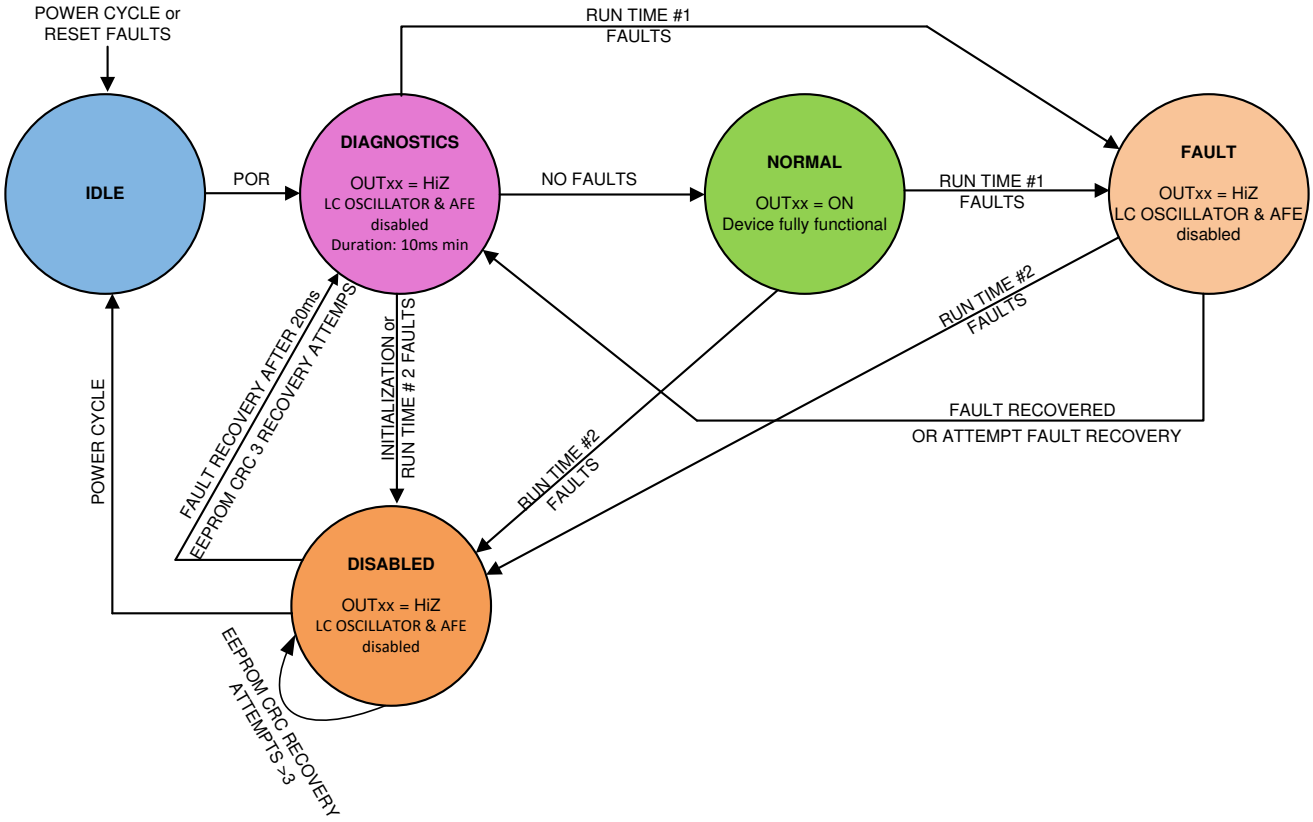


図 8-5. Device State Diagram

8.4.1 IDLE State

The LDC5072-Q1 enters the IDLE state once the VCC and VREG reach operational limits. Power-on Reset is triggered at that time and the device transitions to the DIAGNOSTICS state.

8.4.2 DIAGNOSTICS State

In the DIAGNOSTICS state, the LDC5072-Q1 undergoes a number of self-diagnostics and checks to ensure that the device is functioning as expected and that all sensors are properly connected. See *Diagnostics* for more information.

The device transitions to the DIAGNOSTICS state from one of the following:

- From IDLE state, upon completion of the POR.
- From FAULT state, if the forcing fault conditions are removed or to attempt recovery from non-forcing faults.
- From DISABLED state after 20 ms to attempt recovery. For EEPROM CRC error, the device will only attempt recovery 3 times.

The device transitions from the DIAGNOSTICS state to one of the following:

- NORMAL state, if all the checks are completed successfully.
- FAULT state, if certain fault conditions are present.
- DISABLED state, if certain fault conditions are present.

8.4.3 NORMAL State

The device enters NORMAL state after successful completion of the Diagnostics checks in the DIAGNOSTICS state. In normal state, the LDC5072-Q1 is fully functional and outputs valid signals at the OUT pins. These are the characteristics of the NORMAL state:

- The LC oscillator is enabled and both the oscillation frequency and amplitude are within the specified range.
- The Analog Front End is active and the frequencies of the input signals, amplitudes, and their phase relation are within the specified range.
- the AGC is fully functional and output signals are within the specified range in Auto AGC mode.
- The Output stage is active and OUT pin signals are within the specified range.
- The NORMAL state diagnostics is active and running.

The device transitions from the NORMAL state to one of the following:

- FAULT state, if certain fault conditions are detected.
- DISABLED state, if certain fault conditions are detected.

See *Diagnostics* for more information.

8.4.4 FAULT State

If certain faults are detected in the DIAGNOSTICS or NORMAL state, the device transitions to the FAULT state. These are the characteristics of the FAULT state:

- The LC oscillator is disabled.
- The Analog Front End is disabled.
- The Output stage is tri-stated and OUT pins are pulled up or down by external resistors to indicate the FAULT state.
- The FAULT state diagnostics is active and running.

The device transitions from the FAULT state to one of the following:

- DIAGNOSTICS state, to attempt recovery. For non-forcing faults this is required as the LC and signal path must be enabled to check for faults again. For non-forcing faults, the device stays in FAULT state till removed.
- DISABLED state, if certain fault conditions are detected.

See *Diagnostics* for more information.

8.4.5 DISABLED State

If certain faults are detected in the DIAGNOSTICS, NORMAL or FAULT state, the device transitions to the DISABLED state. These are the characteristics of the DISABLED state:

- The LC oscillator is disabled.
- The Analog Front End is disabled.
- The Output stage is tri-stated and OUT pins are pulled up or down by external resistors to indicate the FAULT state.

The device transitions from the DISABLED state to one of the following:

- Diagnostics state after 20ms to attempt recovery. For EEPROM CRC error, the device will only attempt recovery 3 times.
- The device transitions to the IDLE state upon power cycle.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

This device is intended to be used with an inductive sensor that couples an excitation coil with two receiver coils placed 90° apart. The sensor consists of a movable rotor (target) and a stationary stator (excitation and receiver coils) that allows the user to determine the angular position of the rotor with respect to the stator based on the amplitudes of the secondary coils. The device will filter and gain these signals, and will give Sine and Cosine representation of current angular position at the OUT pins. Next, these analog signals are typically converted to digital signal (by external ADCs or ADCs on board a MCU) and processed by the MCU or another processing unit to extract the angular position.

9.2 Typical Applications

There are two typical system configurations with this device: a 5-V input supply mode and a 3.3-V input supply mode. Additionally, two of these devices may be used in a double-channel architecture to allow for redundancy.

9.2.1 5-V Supply Mode

The primary input configuration of this device is to input a 5-V supply on the VCC pin.

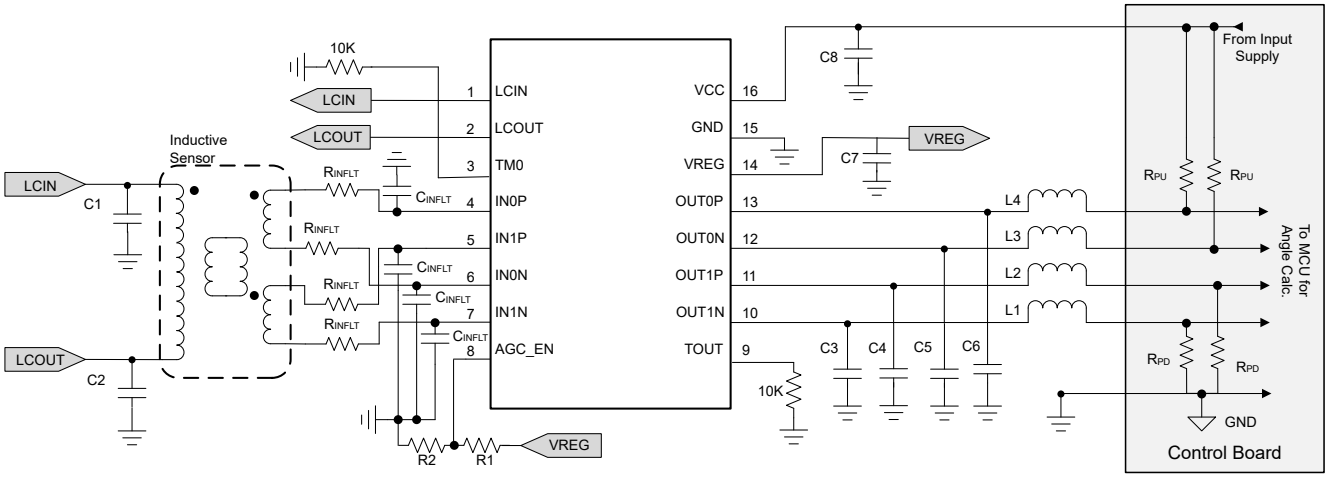


図 9-1. Application Schematic – 5-V Supply Mode

表 9-1. Recommended Components

SCHEMATIC COMPONENT	PARAMETRIC TABLE REFERENCE
C1, C2	C_{LC1},C_{LC2}
C3, C4, C5, C6	C_{OUT}
C7	C_{EXT_VREG}
C8	C_{EXT_VCC}
R1, R2	Sets V_{AGC_EN}. The minimum value for R2 is 1.5KΩ.
R_{INFLT}	Optional. For increasing robustness to electromagnetic susceptibility Suggested value is 120 Ω. Should be adapted to the application
C_{INFLT}	Optional. For increasing robustness to electromagnetic susceptibility Suggested value is 220 pF. Should be adapted to the application
L1, L2, L3, L4	Optional. For increasing robustness to electromagnetic susceptibility

表 9-1. Recommended Components (continued)

SCHEMATIC COMPONENT	PARAMETRIC TABLE REFERENCE
R_{PD}, R_{PU}	R_{PD_OUT}, R_{PU_OUT} ; Typically 10 KΩ Any combination of R_{PD_OUT}, R_{PU_OUT} can be used.

9.2.1.1 Design Requirements

表 9-2 lists the design requirements for this example.

表 9-2. Design Requirements

SCHEMATIC COMPONENT	PARAMETRIC TABLE REFERENCE
Maximum Speed of Motor	20,000 RPM
Number of Poles of Inductive Sensor	10
Short Circuit to Battery Possible	Yes
Gain Mode	Automatic Gain Control

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 VREG and VCC

A short circuit to battery is possible, therefore the VCC must be supplied by a 5-V rail. In this application, the VREG pin requires an external capacitor for regulation. The device will automatically detect the 5-V supply and turn the VREG LDO on for operation.

9.2.1.2.2 Output Capacitors

The maximum rotational speed seen by the LDC5072-Q1 is equal to the motor speed times the number of poles of the inductive sensor:

$$\text{Velocity}_{LDC} = \text{Velocity}_{Motor} \times n \tag{9}$$

where

- Velocity_{LDC} = maximum speed seen by LDC5072-Q1
- Velocity_{Motor} = maximum speed of motor
- n = number of poles of inductive sensor

Based on Velocity_{LDC}, choose C_{OUT} output by referring to graphs in *Typical Characteristics*. In this case, Velocity_{LDC} equals 200,000 RPM which is 3,333 Hz. The output capacitors selected should be can be easily 50 nF but less than 149 nF.

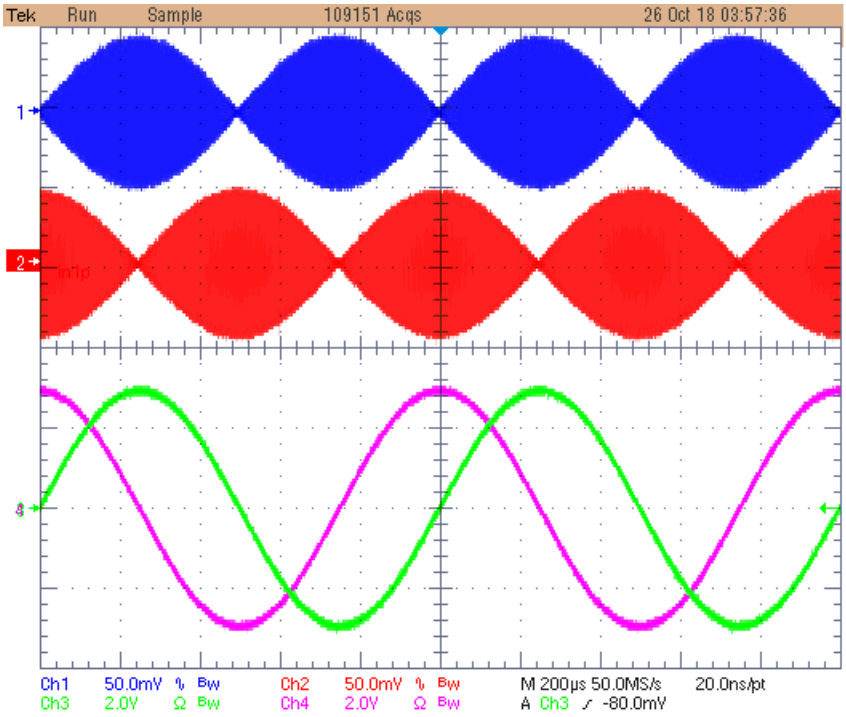
9.2.1.2.3 AGC Mode

Automatic gain control mode will automatically adjust the signal path gain. This helps to accommodate for variations in sensors as well as the mounting distance between the sensor and target.

To use AGC mode:

- R1 should be unpopulated
- R2 should be 1.5KΩ

9.2.1.3 Application Curve



CH1 = IN0P-IN0N

CH2 = IN1P-IN1N

CH3 = OUT0P-OUT0N

CH4 = OUT1P-OUT1N

図 9-2. INx and OUTx Signals at 1000-Hz Rotation Speed

9.2.2 3.3-V Supply Mode

Another configuration of this device is to input a 3.3-V supply on the VCC pin. In this case, the VREG pin must be shorted to the VCC pin externally. The device will automatically detect the 3.3-V supply and bypass the VREG LDO for operation. Refer to 表 9-1 for component values.

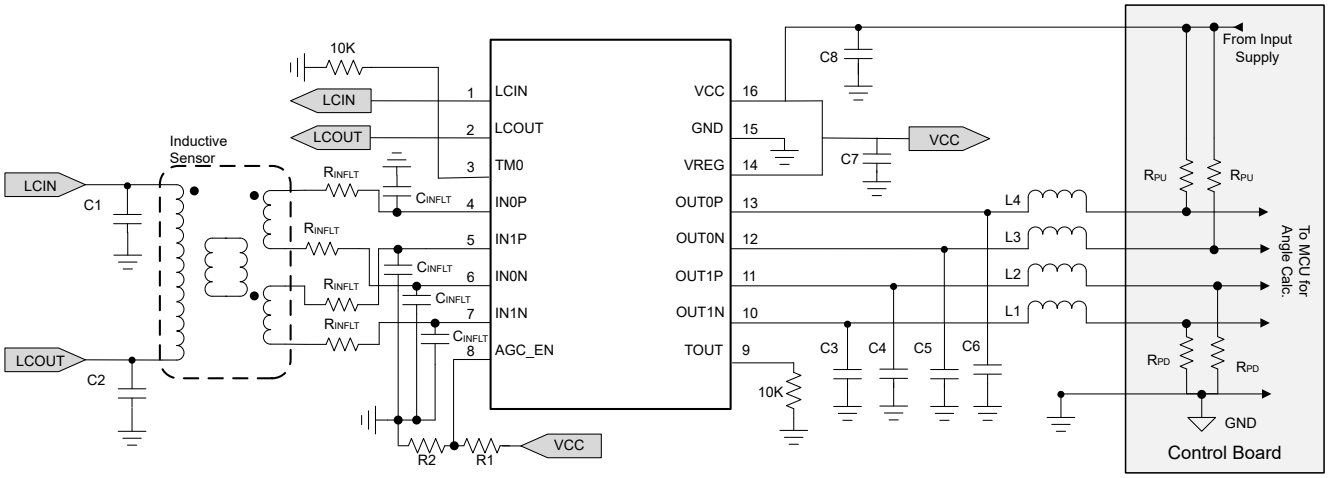


図 9-3. Application Schematic – 3.3-V Supply Mode

9.2.2.1 Design Requirements

表 9-3 lists the design requirements for this example.

表 9-3. Design Requirements

SCHEMATIC COMPONENT	PARAMETRIC TABLE REFERENCE
Maximum Speed of Motor	1,000 RPM
Number of Poles of Inductive Sensor	4
Short Circuit to Battery Possible	No
Gain Mode	Fixed Gain Mode
Coupling Coefficient Between Exciter and Sin/Cos Coils	0.02

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 VREG and VCC

In this application, VCC and VREG will both be supplied by an external 3.3-V power supply. This power rail should not be exposes to voltages greater than 5.5 V.

9.2.2.2.2 Output Capacitors

The method of selecting output capacitors is the same as in the first application. In this example, the output capacitors should be no more than 200 nF.

9.2.2.2.3 Fixed Gain Mode

Fixed gain mode might be chosen in cases where the variation in INx amplitudes between boards is sufficiently small and the air gap is well controlled. An advantage is that changes in OUTx amplitudes can be measured by the host MCU. This could lead to information about air gap variance. A disadvantage is that the signal path gain will not adjust due to variances, which could lead to saturation if the signal is too large, or increased error due to low SNR if the signal is too small.

To use fixed gain mode, first determine the maximum amplitude of the signal at the INx inputs. This is calculated by knowing the maximum coupling coefficient between the LC exciter coil and the Sin/Cos coils (see 式 10 and 式 11).

$$V_{AMP\_INx} = V_{AMP\_LC} \times \eta_{Coupling} \tag{10}$$

where

- V_{AMP_INx}= differential voltage on the INx pin
- V_{AMP_LC}= differential voltage on LCOUT
- $k_{coupling}$= coupling coefficient between exciter and sin/cos coils

$$G_{Desired} = \frac{V_{AMP\_OUTx}}{V_{AMP\_INx}} = \frac{V_{AMP\_OUTx}}{V_{AMP\_LC} \times \eta_{Coupling}} = \frac{2.0\ V}{2.5\ V \times 0.02} = 40 \tag{11}$$

where

- $G_{desired}$= gain setting for the system
- V_{AMP_OUTx}= Differential amplitude between OUTxP and OUTxN
- V_{AMP_INx}= Differential voltage on the INx pin

The single-ended OUTx voltages should stay within 10% to 90% of VREG. For this example, a differential amplitude of 2.0 V was chosen.

When the desired gain is known, the voltage to apply to the AGC_EN pin can be calculated by rearranging 式 7.

$$G_{GC} = \frac{G_{Desired}}{G_{MIXER} \times G_{FIXED}} = \frac{40}{0.637 \times 28.8} = 2.08 \tag{12}$$

$$\%VREG_{Desired} = \frac{90.9}{1.903} \times \log\left(\frac{G_{GC}}{0.4}\right) + 4.55 = 38.53\%VREG \tag{13}$$

From there, the pullup and pulldown resistors can be calculated to achieve $\%VREG_{Desired}$. These should be 0.1% tolerant resistors and the loading should not violate the $I_{LOAD\_REG\_EXT}$ specification.

Choose R2 = 10 kΩ

$$R_1 = \frac{R_2}{\%VREG_{Desired}} - R_2 = \frac{10000}{.3853} - 10000 = 15.95\ k\Omega \tag{14}$$

Finally, choose the closest resistor value and double check that the final gain will be within acceptable limits. In this case, choose R1 = 16.0 kΩ.

9.2.3 Redundancy Mode

In some applications, it is necessary to have redundancy with respect to the angle feedback information. One option for achieving redundancy is to have two independent sensors each with their own LDC5072-Q1 device. Alternatively, the system can be configured in a way that the sensor rotor is shared between two sets of excitation and receive coils with two LDC5072-Q1 devices. This configuration is possible because the structure of the LCIN and LCOUT pins prevent current from back-flowing into the device even when one device is in the FAULT state. This prevents the disabled device from loading the active device. All coils are drawn on the same PCB. Refer to 表 9-1 for component values.

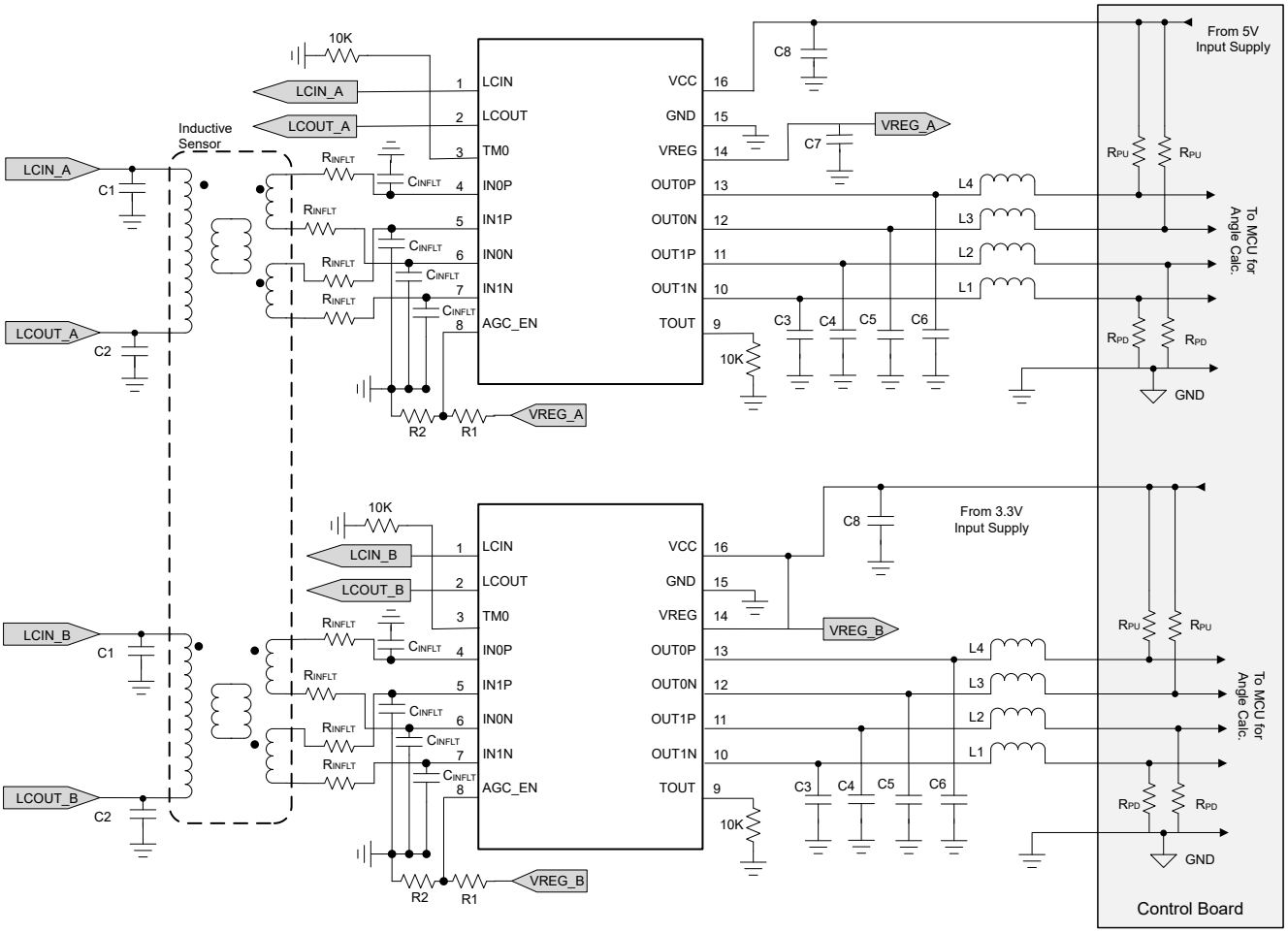


図 9-4. Application Schematic - Redundancy Mode

注

Both LDC5072-Q1 devices can be supplied by the same voltage, provided that system level functional safety requirements are satisfied.

9.2.4 Single-Ended Mode

In some scenarios, it may be desirable to connect to a single-ended ADC. This will reduce the number of wires leaving the LDC5072-Q1 sensor board, but it will reduce the dynamic range, SNR, and noise immunity. If it is possible to use the LDC5072-Q1 in differential mode, then that should be the first choice for the system designer. Refer to 表 9-1 for component values. If single-ended mode must be used, follow these guidelines:

- Typically, OUT0P and OUT1P will be the single-ended outputs used.
- Each differential pair must be loaded equally. This means that terminations must be added to the sensor board for OUT0N and OUT1N.
- If it is difficult to balance the loads due to the effects of the ADC, then the OUT0P and OUT1P outputs can be buffered before the ADC.

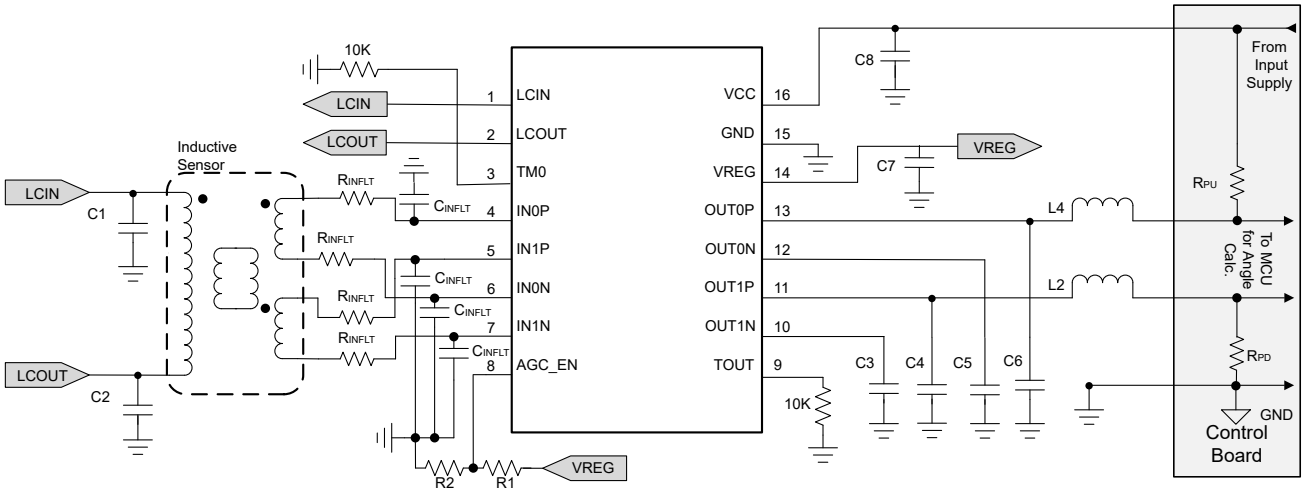


図 9-5. Single-Ended Configuration

9.2.5 External Diagnostics Required for Loss of VCC or GND

The robustness of the system can be improved by implementing simple checks in software. The primary reason for this is to help with the loss of VCC or loss of GND fault condition.

Fault detection is typically done by measuring when the OUTx pins enter a High-Z state. This is done by adding pullup and pulldown resistors on the controller board. The ADC then measures if the OUTx signals ever exceed $V_{OUT\_FLT\_HIGH}$ or are below $V_{OUT\_FLT\_LOW}$.

If a pullup resistor is used, a loss-of-VCC condition on the sensor board causes there to be a small leakage current (I_{OUT_NOVCC}) path into the OUTx pin. If a pulldown resistor is used, a loss of GND condition on the sensor board will have a leakage current path (I_{OUT_NOGND}) into OUTx pin. The leakage current value is controlled such that the OUTx pin voltages stay above $V_{OUT\_FLT\_HIGH}$ and below $V_{OUT\_FLT\_LOW}$. However if certain application conditions cause the OUTx pin voltage outside the fault thresholds, following options is recommended to ensure that the MCU recognizes that a fault has occurred:

- Use a combination of pullup and pulldown resistors. This way, a loss of ground or loss of VCC will always be detected by two of the four OUTx pins. For example, if a pulldown resistor is present, then a loss of VCC can be signaled with a voltage below $V_{OUT\_FLT\_LOW}$. If a pullup resistor is used, then a loss of GND can be signaled with a voltage about $V_{OUT\_FLT\_HIGH}$.
- Track the common-mode voltage of the OUT0x and OUT1x pairs. Normally the common mode will be half of VCC. A loss of VCC or GND is easily caught by using this method. This method does not work when using single-ended mode.

10 Power Supply Recommendations

The LDC5072-Q1 requires at most 22 mA from either a 5-V or 3.3-V source, not including loading due to the connected sensor coils. Also note that the analog output OUTx signals are scaled to VCC.

There are two modes of operation for the LDC5072-Q1.

10.1 Mode 1: VCC = 5 V, VREG = 3.3 V

In this mode of operation, VCC must be supplied with an external 5-V power supply. The LDC5072-Q1 then uses an internal LDO to generate the 3.3 V for VREG. The supply for VCC must stay within the range of 4.5 V to 5.6 V. VCC requires at least a 100-nF decoupling capacitor and VREG requires a capacitor within the range of the C_{EXT_VREG} parameter.

VCC is rated to withstand voltages between –15 V to 30 V. This might occur due to an incorrect connection in the cabling between the LDC5072-Q1 PCB and a controller board.

10.2 Mode 2: VCC = VREG = 3.3 V

In this mode of operation, VCC and VREG are supplied from the same 3.3-V power supply. VCC and VREG together require at least a 100-nF decoupling capacitor.

VREG is only rated from –0.3 V to 5.5 V. In this mode, the power rail to the LDC5072-Q1 cannot withstand a short circuit to a higher voltage source, such as a car battery.

11 Layout

11.1 Layout Guidelines

The designer requires at least a 2-layer PCB for the LDC5072-Q1. The device is designed such that one half of the device contains sensitive analog signals for the sensor coils (LCIN, LCOUT, and INxx), and the other half of the device contains signals that may leave the PCB (power, ground, and analog outputs).

The following lists the best practices for the PCB layout:

- Bypass capacitors should be placed close to the device pins.
- A ground plane layer can be placed below the LDC5072-Q1.
- Ideally, there should not be a ground layer beneath the sensor coils as it will impact the sensor response. A shielding layer, however, may be implemented to protect the sensor from interference of metal or EMI beneath the sensor. To minimize the impact to the sensor response, the shielding layer should be separated by as much distance from the bottom of the sensor as possible.
- LCIN, LCOUT, and the INX signal traces should be kept as short as possible between the LDC5072-Q1 device and the sensor coils.
- TI recommends that placeholder pads be accommodated in the layout for the R_{INFLT}, C_{FLT}, L1, L2, L3, and L4. These pads can be useful in debug during EMI/EMC testing and can save iteration of board layout.

11.2 Layout Example

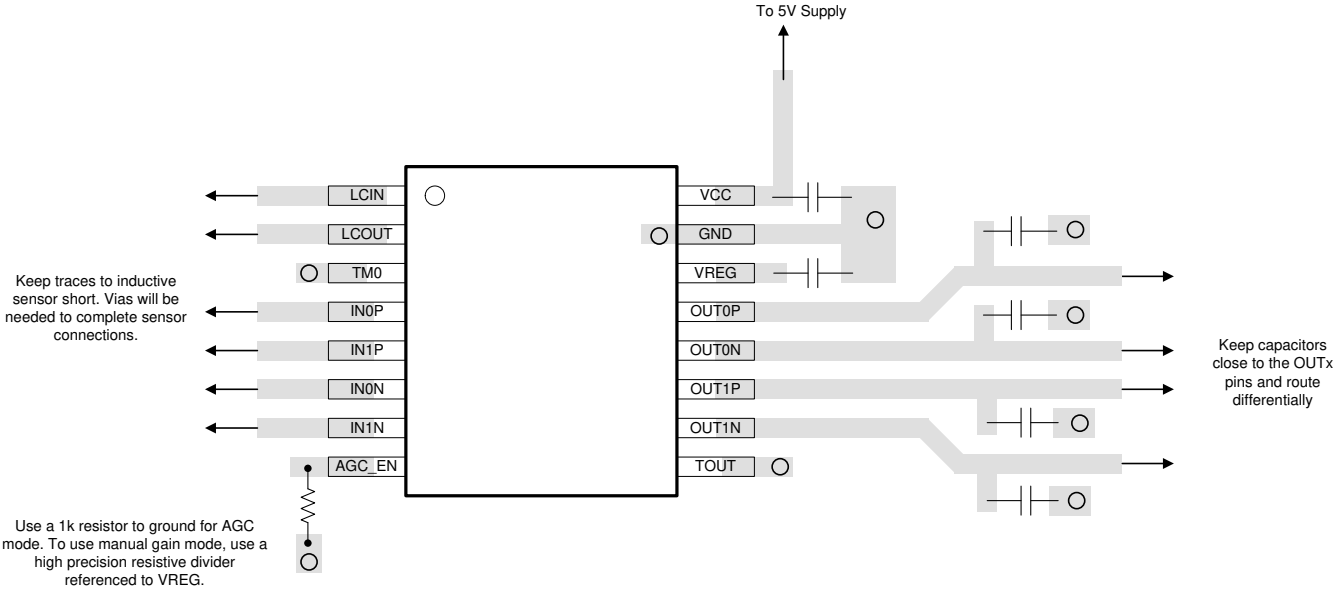


図 11-1. Layout Recommendation for the LDC5072-Q1

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC5072EPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 160	LDC5072	Samples
LDC5072EPWTQ1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 160	LDC5072	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

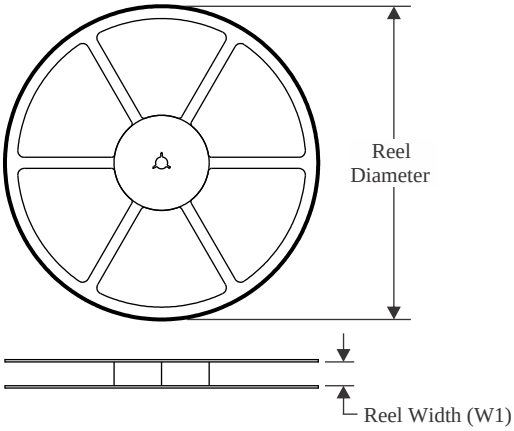
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

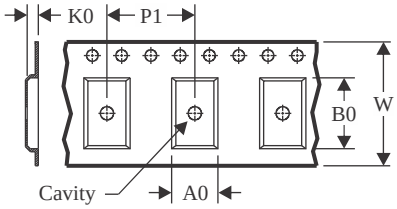
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

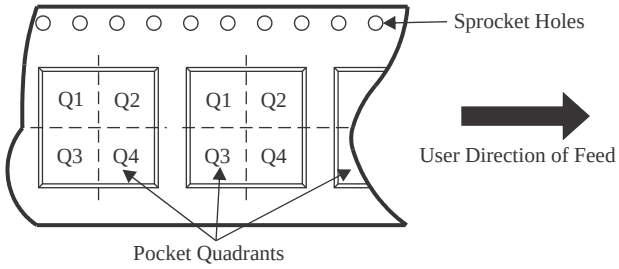


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

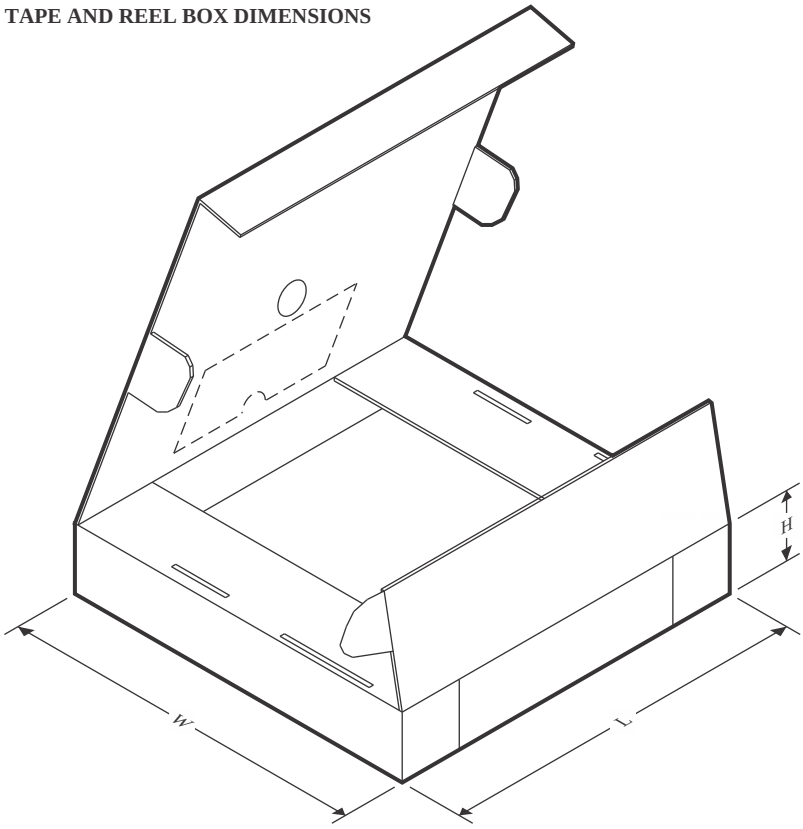
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC5072EPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

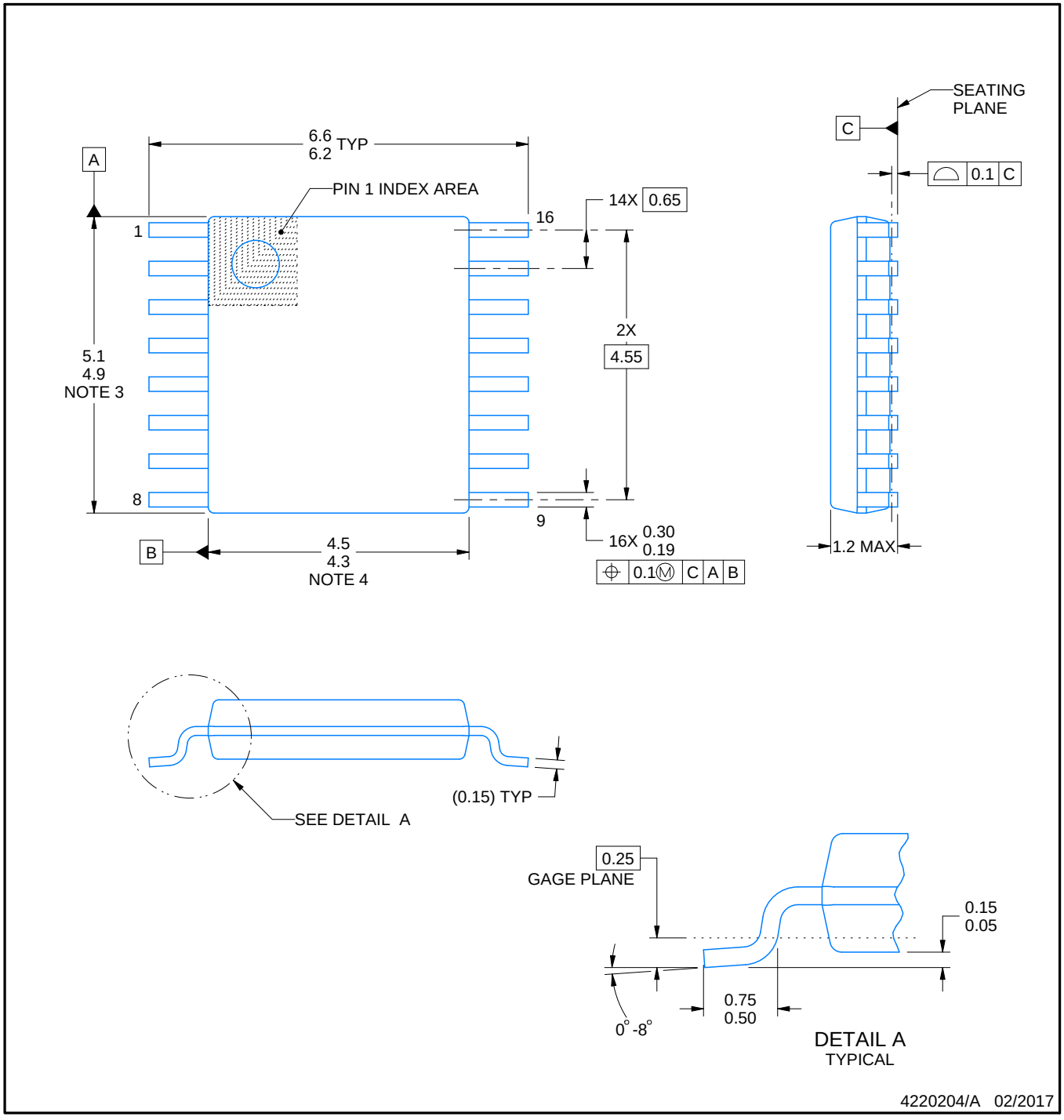
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC5072EPWRQ1	TSSOP	PW	16	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0016A

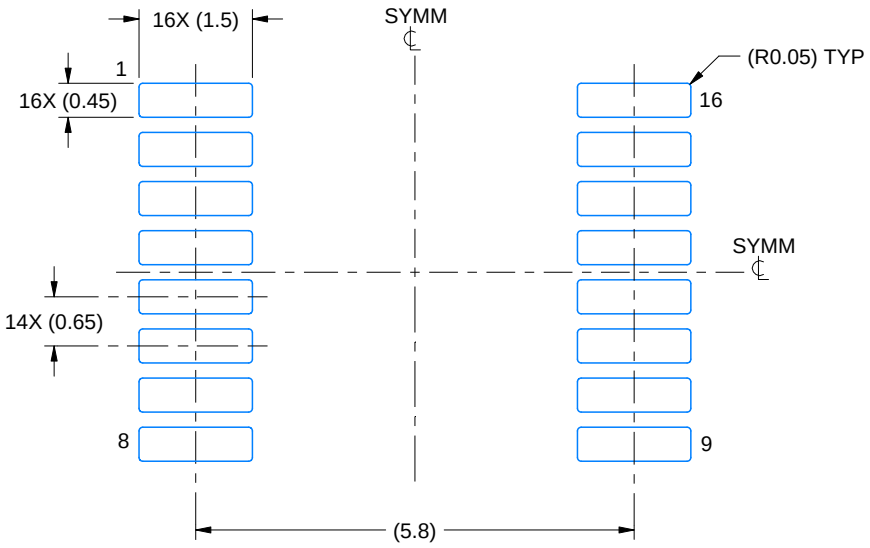
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

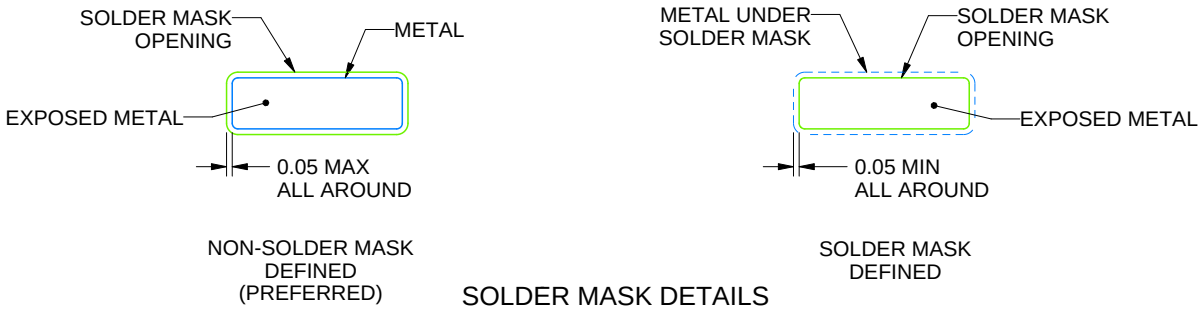


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

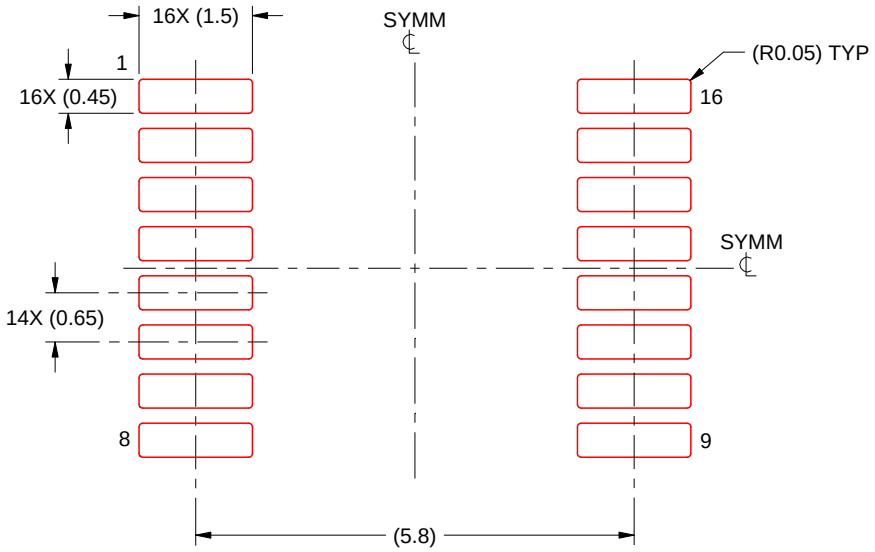


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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