LM193-MIL デュアル差動コンパレータ

1 特長

- 単一電源またはデュアル電源
- 広い範囲の電源電圧
  - 最大定格: 2V～36V
  - 30Vでテスト: V接尾辞なしのデバイス
  - 32Vでテスト: V接尾辞付きのデバイス
- 電源電圧に影響されない低い電源消費電流: コンパレータごとに0.4mA (標準値)
- 低い入力バイアス電流: 25nA (標準値)
- 低い入力オフセット電流: 3nA (標準値) (LM193)
- 低い入力オフセット電圧: 2mV (標準値)
- 同相入力電圧範囲にグランドが含まれる
- 差動入力電圧範囲が最大定格電源電圧と同じ: ±36V
- 低い出力飽和電圧
- TTL、MOS、CMOS互換出力
- MIL-PRF-38535準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。

  他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

2 アプリケーション

- 化学センサ/ガス・センサ
- デスクトップ PC
- モータ制御: AC誘導
- 重量計

3 概要

このデバイスは2つの独立した電圧コンパレータで構成され、広い範囲の電圧を持つ単一の電源で動作するよう設計されています。デュアル電源での動作も可能です。この場合、2つの電源の差が2V～36Vで、V_{CC}が入力同相電圧よりも1.5V以上高いことが条件です。消費電流は、電源電圧に依存しません。出力を他のオープン・コレクタ出力に接続し、ワイヤードAND関係が構成できます。

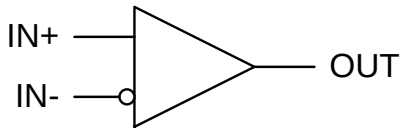
LM193-MILデバイスは、-55℃～+125℃で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM193-MIL	SOIC (8)	4.90mm×6.00mm
	CDIP (8)	10.00mm×7.00mm
	LCCC (20)	9.00mm×9.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



目次

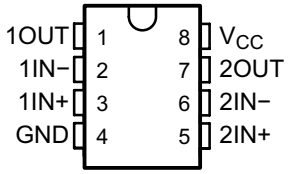
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

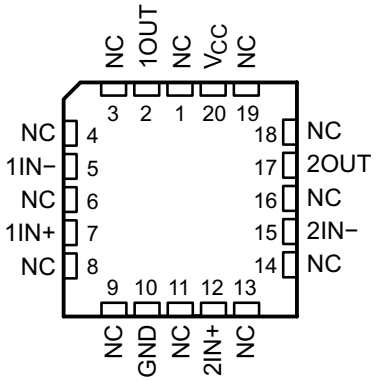
日付	改訂内容	注
2017年6月	*	初版

5 Pin Configuration and Functions

D, JG
8-Pin SOIC, CDIP
Top View



FK Package
20-Pin LCCC
Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, CDIP	LCCC		
1OUT	1	2	Output	Output pin of comparator 1
1IN–	2	5	Input	Negative input pin of comparator 1
1IN+	3	7	Input	Positive input pin of comparator 1
GND	4	10	—	Ground
2IN+	5	12	Input	Positive input pin of comparator 2
2IN-	6	15	Input	Negative input pin of comparator 2
2OUT	7	17	Output	Output pin of comparator 2
V_{CC}	8	20	—	Supply Pin
NC	—	1	N/A	No Connect (No Internal Connection)
		3		
		4		
		6		
		8		
		9		
		11		
		13		
		14		
		16		
		18		
		19		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			36	V
V_{ID}	Differential input voltage(3)			±36	V
V_I	Input voltage (either input)		–0.3	36	V
I_{IK}	Input current(4)			-50	mA
V_O	Output voltage			36	V
I_O	Output current			20	mA
	Duration of output short circuit to ground(5)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1.6 mm (1/16 in) from case for 60 s	JG package		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Input current flows thorough parasitic diode to ground and will turn on parasitic transistors that will increase ICC and may cause output to be incorrect. Normal operation resumes when input current is removed.
(5) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	non-V devices	2	30	V
		V devices	2	32	V
T_A	Operating temperature	LM193	–55	125	°C
		LM293, LM293A	–25	85	°C
		LM393, LM393A	0	70	°C
		LM2903, LM2903V, LM2903AV	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM193-MIL		UNIT
		JG (CDIP)	FK (LCCC)	
		8 PINS	20 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	5.61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LM193-MIL			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		25°C		2	5	mV
				Full range			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25	nA
				Full range			100	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–25	–100	nA
				Full range			–300	
V_{ICR}	Common-mode input-voltage range (2)			25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	25°C		0.1		nA
		V_{OH} = 30 V	V_{ID} = 1 V	Full range			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1	mA
			V_{CC} = 30 V	Full range			2.5	

(1) Full range (minimum or maximum) for LM193-MIL is –55°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2 V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF (1)(2)	100-mV input step with 5-mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.7 Typical Characteristics

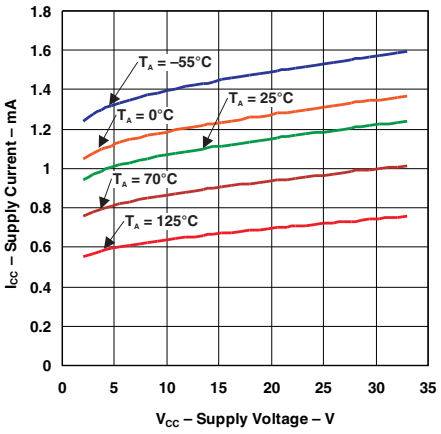


Figure 1. Supply Current vs Supply Voltage

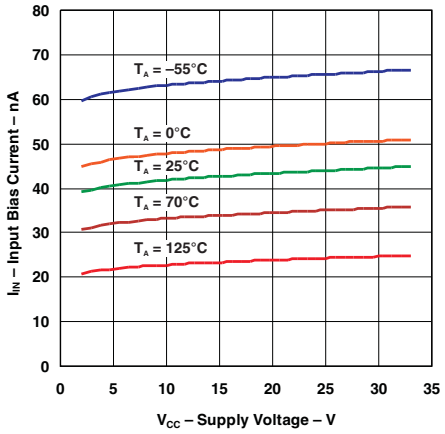


Figure 2. Input Bias Current vs Supply Voltage

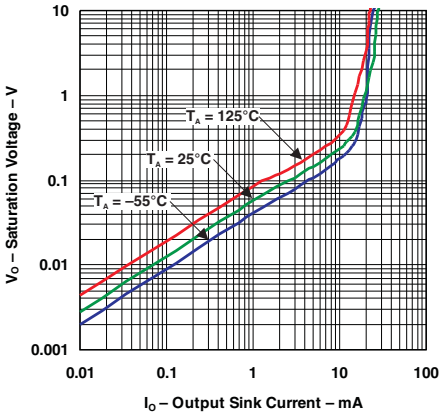


Figure 3. Output Saturation Voltage

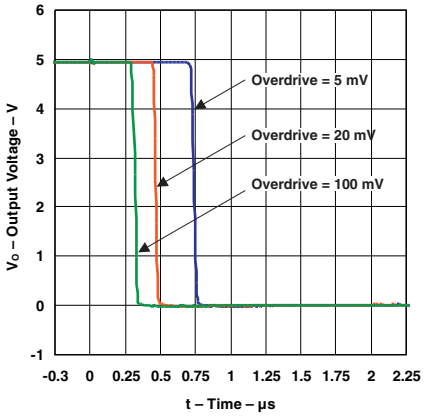


Figure 4. Response Time for Various Overdrives Negative Transition

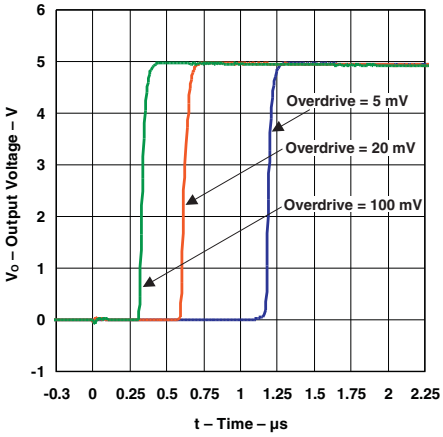


Figure 5. Response Time for Various Overdrives Positive Transition

7 Detailed Description

7.1 Overview

The dual comparator has the ability to operate up to absolute maximum of 36 V on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V to 36 V), low Iq and fast response of the device.

The open-drain output allows the user to configure the output's logic high voltage (V_{OH}) and can be used to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram

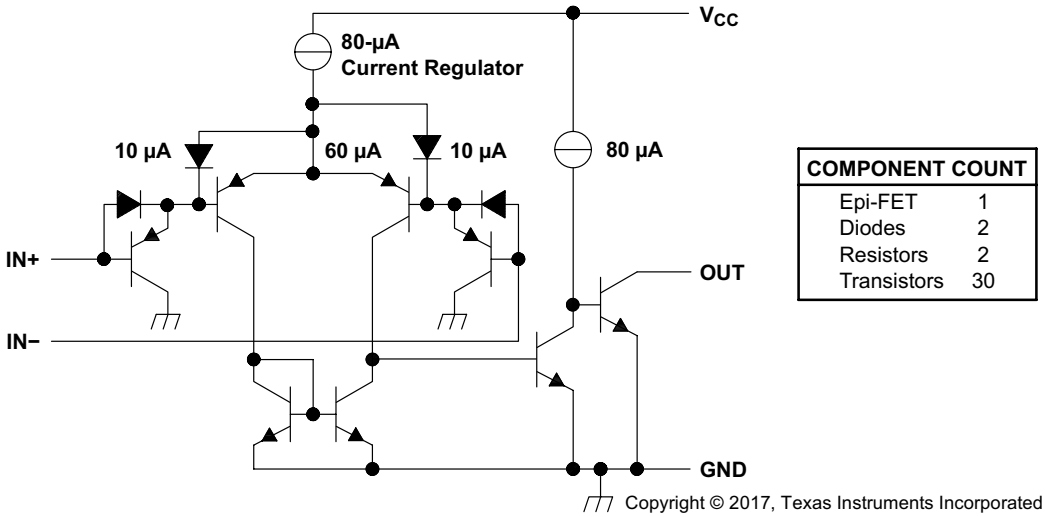


Figure 6. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to V_{CC}– 1.5 V input. Allow for V_{CC}– 2 V at cold temperature.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the negative input voltage is higher than the positive input voltage and the offset voltage. The VOL is resistive and will scale with the output current. See Figure 3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The device operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes this comaprator optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

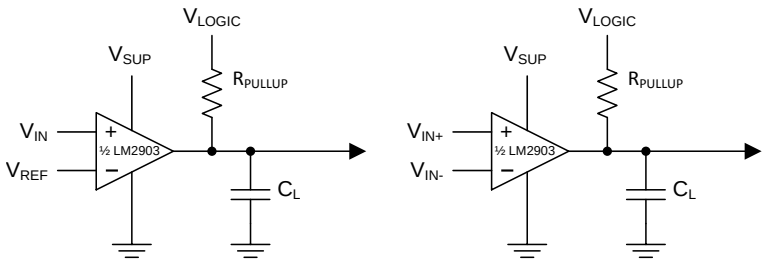


Figure 7. Single-Ended and Differential Comparator Configurations Using the LM2903

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-2 V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 µA to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using the device in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0 V to V_{CC}– 2.0 V. This limits the input voltage range to as high as V_{CC}– 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common-mode range:
   (a) If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   (b) If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 8 and Figure 9 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use *Typical Characteristics* to determine V_{OL} based on the output current.

The output current can also effect the transient response. See *Response Time* for more information.

8.2.2.4 Response Time

Response time is a function of input over drive. See *Application Curves* for typical response times. The rise and falls times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  – R_{CE} can be determine by taking the slope of *Typical Characteristics* in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

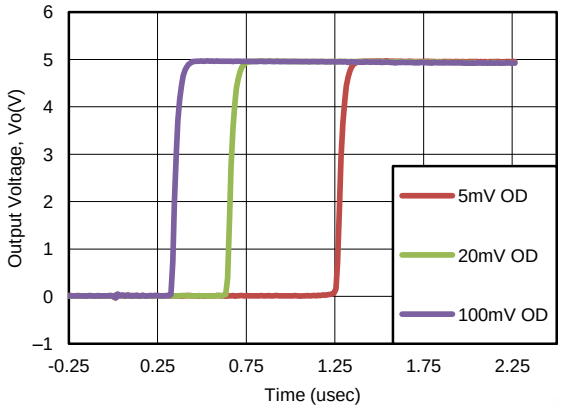


Figure 8. Response Time for Various Overdrives (Positive Transition)

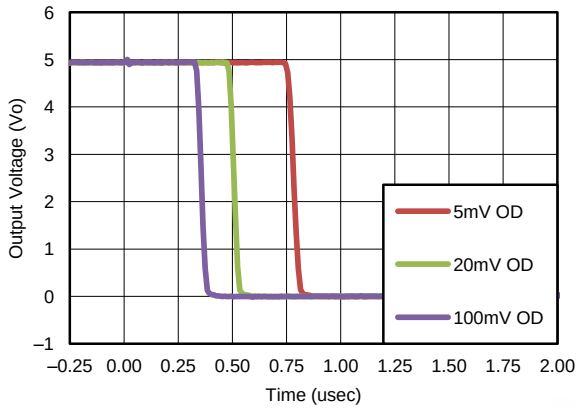


Figure 9. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the device's GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

10.2 Layout Example

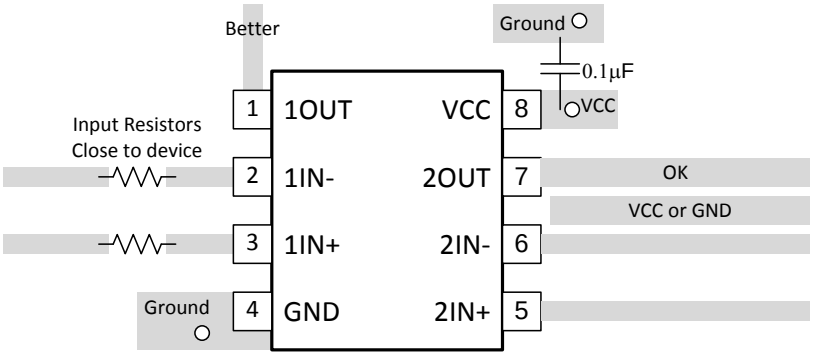


Figure 10. LM2903 Layout Example Used as an Example

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
LM193	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM293	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM293A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM393	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM393A	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM2903	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM2903V	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

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11.5 静電気放電に関する注意事項

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9452601Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9452601Q2A LM193FKB	Samples
5962-9452601QPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9452601QPA LM193	Samples
JM38510/11202BPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11202BPA	Samples
LM193FKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9452601Q2A LM193FKB	Samples
LM193JG	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM193JG	Samples
LM193JGB	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9452601QPA LM193	Samples
M38510/11202BPA	ACTIVE	CDIP	JG	8	50	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11202BPA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

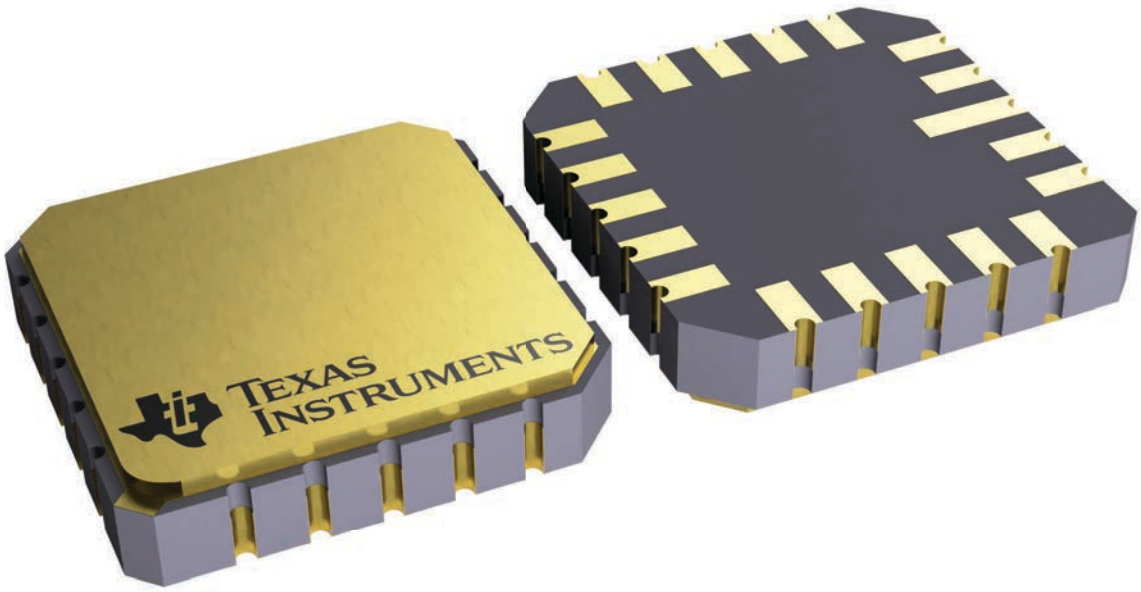
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



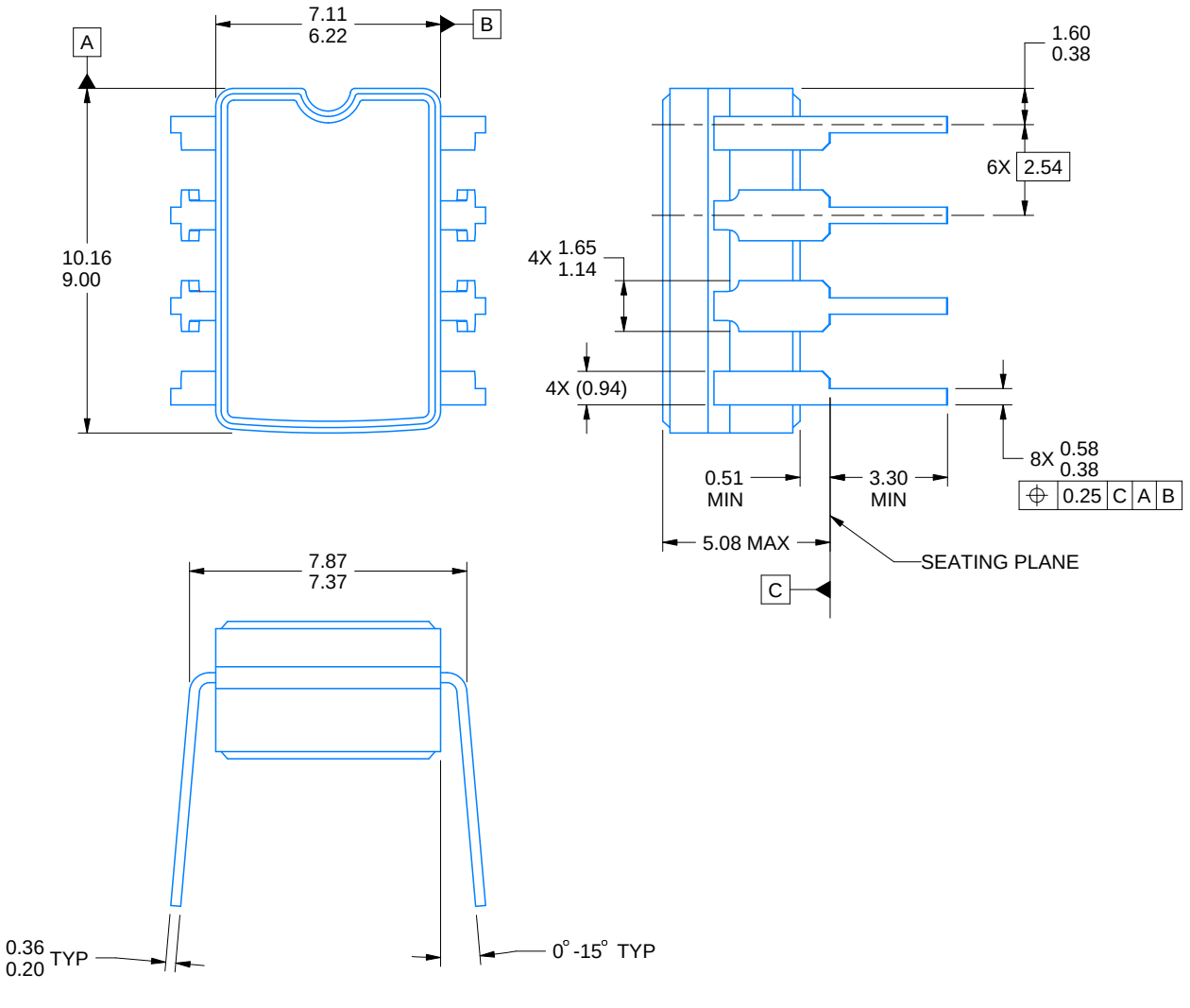
4229370VA\

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



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NOTES:

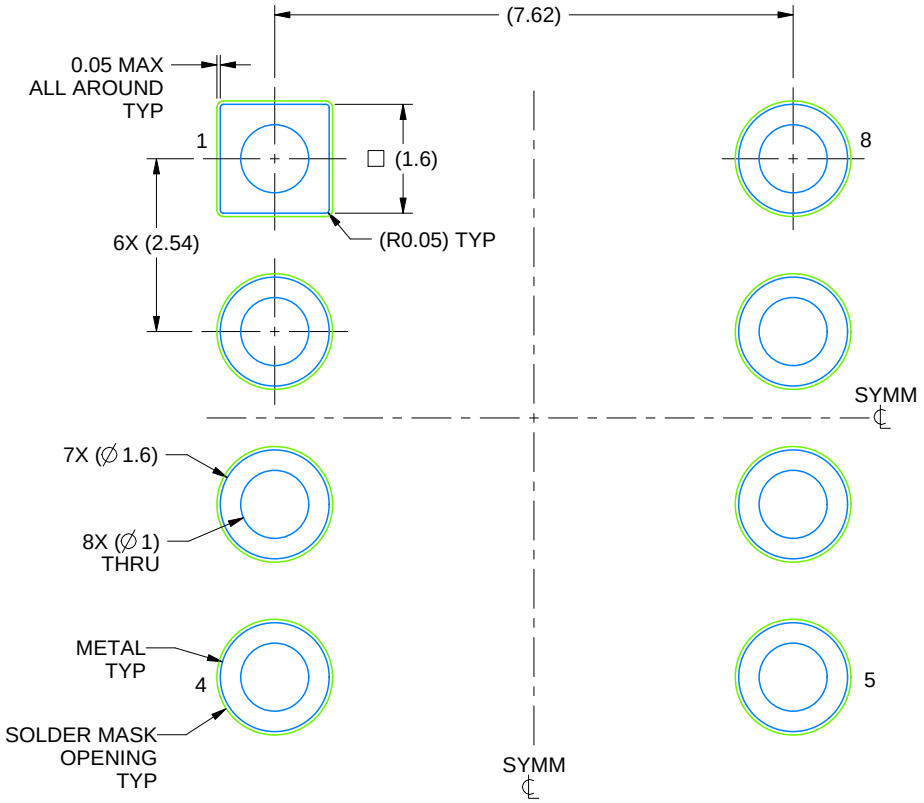
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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