LM25180 42V_{IN} の PSR フライバック DC/DC コンバータ、65V、1.5A のパワー MOSFET 搭載

1 特長

- 高信頼性の堅牢なアプリケーション用に設計
  - 4.5V～42V の広い入力電圧範囲
  - 絶縁バリアと交差する部品は 1 つだけの堅牢なソリューション
  - 総出力レギュレーション精度: ±1.5%
  - (オプション) V_{OUT} 温度補償
  - 6ms の内部ソフトスタート、プログラムも可能
  - 入力 UVLO およびサーマル・シャットダウン保護機能
  - ヒカップ・モード過電流フォルト保護
  - -40°C～+150°C の接合部温度範囲
- 統合によりソリューションのサイズとコストを低減
  - 65V、0.4Ωのパワー MOSFET を内蔵
  - V_{OUT}の レギュレーションにフォトカプラや変圧器の補助巻線が不要
  - ループ補償内蔵
  - CISPR 32 に適合する低 EMI での動作
- 高効率の PSR フライバック動作
  - 重負荷時の境界導通モード (BCM) での疑似共振スイッチング
  - 低い入力静止電流
  - 外部バイアス・オプションによる効率向上
  - シングルおよびマルチ出力の実装
- WEBENCH® Power Designer を使用して、カスタムのレギュレータ設計を作成

2 アプリケーション

- 絶縁型フィールド・トランスミッタおよびフィールド・アクチュエータ
- アナログ入力モジュール用マルチ出力レール
- モータ・ドライブ： IGBT ゲート・ドライブの電源
- ビルディング・オートメーション用 HVAC システム

3 概要

LM25180は1次側レギュレーション(PSR)のフライバック・コンバータで、4.5V～42Vの広い入力電圧範囲にわたって高い効率を実現します。絶縁出力電圧は1次側フライバック電圧からサンプリングされるため、出力電圧のレギュレーションを行うためにフォトカプラ、基準電圧、変圧器からの3次巻線を必要としません。高いレベルの統合により、絶縁バリアと交差する部品は 1 つだけで、単純で信頼性が高く、高密度の設計が実現されています。境界導通モード (BCM) スイッチングにより、小型の磁気的ソリューションと、±1.5% 以内の負荷およびライン・レギュレーション性能を実現できます。内蔵の65VパワーMOSFETは最大7Wの出力電力を供給でき、ライン過渡に対する余裕が拡大されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM25180	WSON (8)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

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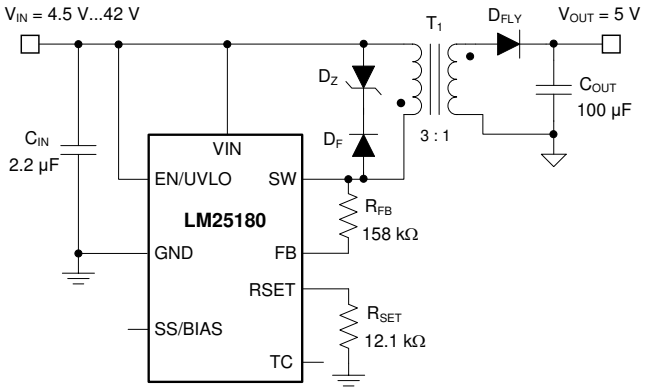
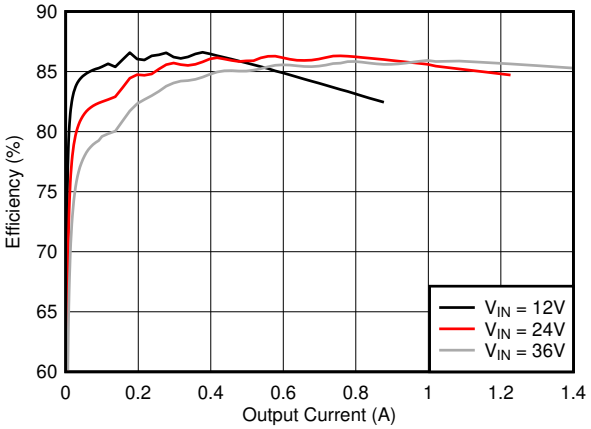
代表的なアプリケーション



標準的な効率、V_{OUT} = 5V



目次

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年11月発行のものから更新 **Page**

- Changed EC table specs for current limit ... 5
- 追加 note about failsafe current limit ... 15

5 概要（続き）

LM25180コンバータには、対象の最終機器に合わせて性能を最適化するオプション機能があるため、絶縁DC/DC電源の実装が簡単になります。出力電圧を1つの抵抗で設定でき、オプションの抵抗を使用するとフライバック・ダイオードの電圧降下の温度係数を打ち消して電圧精度を向上できます。追加機能として、内部的に固定または外部的にプログラム可能なソフトスタート、オプションの高効率用バイアス電源接続、可変ラインUVLO用のヒステリシス付き高精度イネーブル入力、ヒカップ・モード過負荷保護、自動復元機能付きのサーマル・シャットダウン保護機能があります。

LM25180フライバック・コンバータは、8ピン、4mm×4mm、0.8mmピン・ピッチの、熱的に強化されたWSONパッケージで供給されます。

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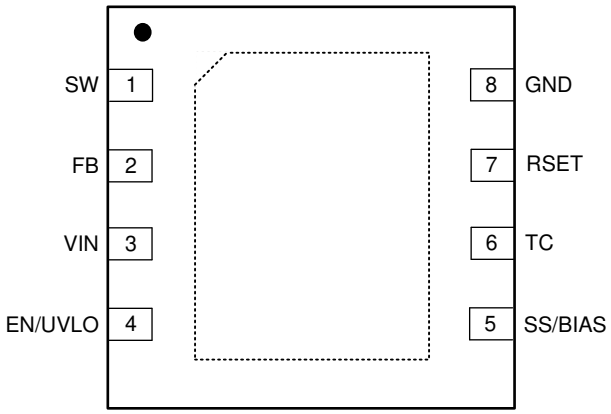
6 Pin Configuration and Functions

NGU Package
8-Pin WSON With Wettable Flanks
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	SW	P	Switch node that is internally connected to the drain of the N-channel power MOSFET. Connect to the primary-side switching terminal of the flyback transformer.
2	FB	I	Primary side feedback pin. Connect a resistor from FB to SW. The ratio of the FB resistor to the resistor at the RSET pin sets the output voltage.
3	VIN	P/I	Input supply connection. Source for internal bias regulators and input voltage sensing pin. Connect directly to the input supply of the converter with short, low impedance paths.
4	EN/UVLO	I	Enable input and undervoltage lockout (UVLO) programming pin. If the EN/UVLO voltage is below 1.1 V, the converter is in shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 1.1 V and below 1.5 V, the converter is in standby mode with the internal regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
5	SS/BIAS	I	Soft-start or bias input. Connect a capacitor from SS/BIAS to GND to adjust the output start-up time and input inrush current. If SS/BIAS is left open, the internal 6-ms soft-start timer is activated. Connect an external supply to SS/BIAS to supply bias to the internal voltage regulator and enable internal soft start.
6	TC	I	Temperature compensation pin. Tie a resistor from TC to RSET to compensate for the temperature coefficient of the forward voltage drop of the secondary diode, thus improving regulation at the secondary-side output.
7	RSET	I	Reference resistor tied to GND to set the reference current for FB. Connect a 12.1-kΩ resistor from RSET to GND.
8	GND	G	Analog and power ground. Ground connection of internal control circuits and power MOSFET.
-	DAP	G	Die attach pad. Connect to PCB ground plane.

(1) P = Power, G = Ground, I = Input, O = Output.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN to GND	–0.3	45	V
	EN/UVLO to GND	–0.3	45	
	TC to GND	–0.3	6	
	SS/BIAS to GND	–0.3	14	
	FB to GND	–0.3	45.3	
	FB to VIN	–0.3	0.3	
	RSET to GND	–0.3	3	
Output voltage	SW to GND	–1.5	70	V
	SW to GND (20-ns transient)	–3		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) CDM ESD Classification Level C4B	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage after turn on	4.5		42	V
V_{SW}	SW voltage			65	V
$V_{EN/UVLO}$	EN/UVLO voltage			42	V
$V_{SS/BIAS}$	SS/BIAS voltage			13	V
T_J	Operating junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		LM25180 NGU (WSON) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	41.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	34.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	19.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits aaply over the full –40°C to 150°C junction temperature range unless otherwise indicated. V_{IN} = 24 V and $V_{EN/UVLO}$ = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$ = 0 V		3		µA
I_{ACTIVE}	VIN active current	$V_{EN/UVLO}$ = 2.5 V, V_{RSET} = 1.8 V		260	350	µA
$I_{ACTIVE-BIAS}$	VIN current with BIAS connected	$V_{SS/BIAS}$ = 6 V		25	40	µA
$V_{SD-FALLING}$	Shutdown threshold	$V_{EN/UVLO}$ falling	0.3			V
ENABLE AND INPUT UVLO						
$V_{SD-RISING}$	Standby threshold	$V_{EN/UVLO}$ rising		0.8	1	V
$V_{UV-RISING}$	Enable threshold	$V_{EN/UVLO}$ rising	1.45	1.5	1.53	V
$V_{UV-HYST}$	Enable voltage hysteresis	$V_{EN/UVLO}$ falling	0.04	0.05		V
$I_{UV-HYST}$	Enable current hysteresis	$V_{EN/UVLO}$ = 1.6 V	4.2	5	5.5	µA
FEEDBACK						
I_{RSET}	RSET current	R_{RSET} = 12.1 kΩ		100		µA
V_{RSET}	RSET regulation voltage	R_{RSET} = 12.1 kΩ	1.191	1.21	1.224	V
$V_{FB-VIN1}$	FB to VIN voltage	I_{FB} = 80 µA	–40			mV
$V_{FB-VIN2}$	FB to VIN voltage	I_{FB} = 120 µA			40	mV
SWITCHING FREQUENCY						
F_{SW-MIN}	Minimum switching frequency			12		kHz
F_{SW-MAX}	Maximum switching frequency			350		kHz
t_{ON-MIN}	Minimum switch on-time			140		ns
DIODE THERMAL COMPENSATION						
V_{TC}	TC voltage	I_{TC} = ±10 µA, T_J = 25°C		1.2	1.27	V
POWER SWITCHES						
$R_{DS(on)}$	MOSFET on-state resistance	I_{SW} = 100 mA		0.4		Ω
SOFT-START AND BIAS						
I_{SS}	SS ext capacitor charging current			5		µA
t_{SS}	Internal SS time			6		ms
$V_{BIAS-UVLO-RISE}$	BIAS enable voltage	$V_{SS/BIAS}$ rising		5.5	5.75	V
$V_{BIAS-UVLO-HYST}$	BIAS UVLO hysteresis	$V_{SS/BIAS}$ falling		190		mV
CURRENT LIMIT						
$I_{SW-PEAK}$	Peak current limit threshold		1.23	1.5	1.73	A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			6		°C

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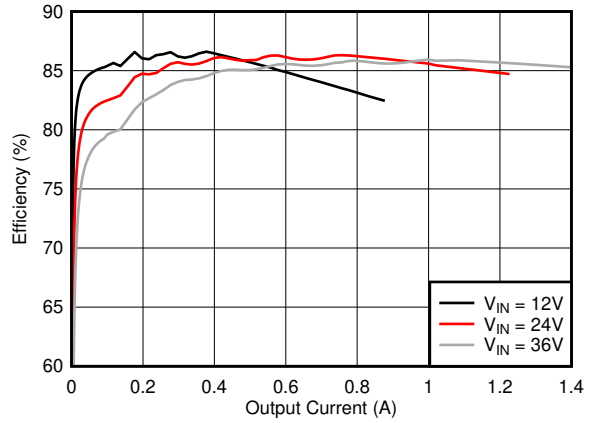
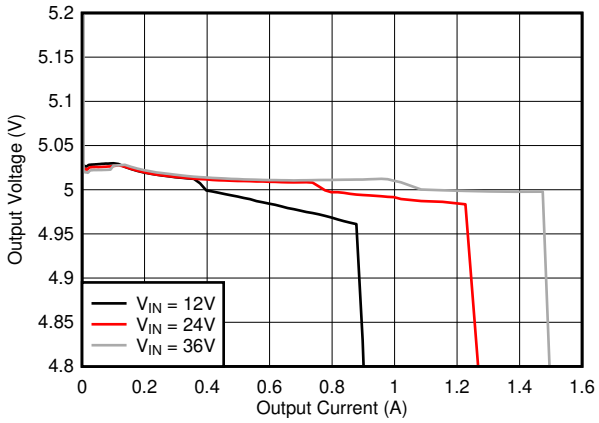
7.6 Typical Characteristics

V_{IN} = 24 V, $V_{EN/UVLO}$ = 2 V (unless otherwise stated).



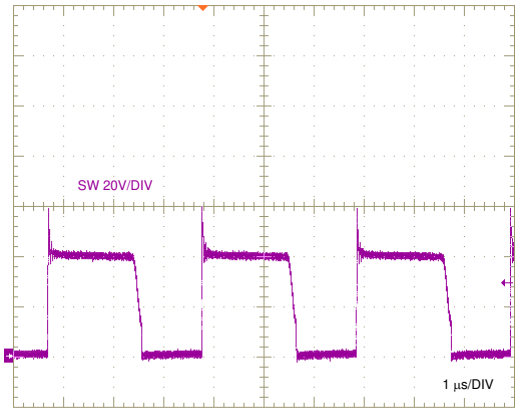
See 図 23

図 1. Efficiency vs. Load



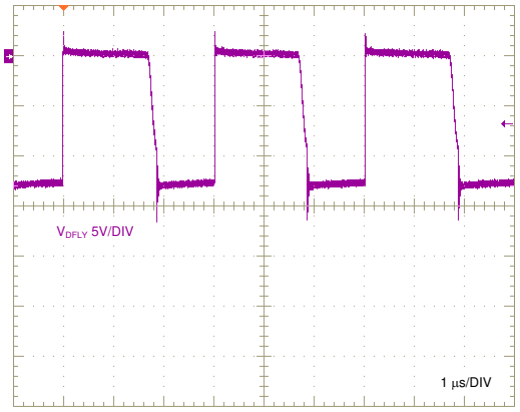
See 図 23

図 2. Output Voltage vs. Load



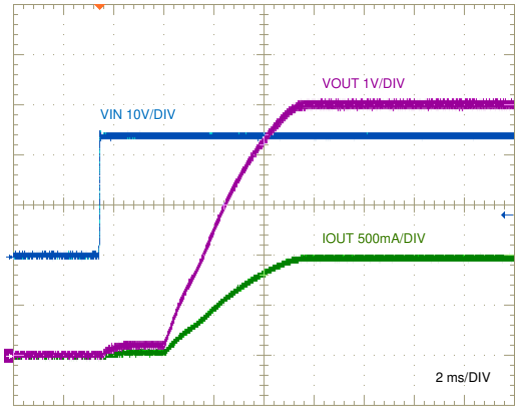
See 図 23 I_{OUT} = 1 A

図 3. Primary-side Switching Waveform in BCM



See 図 23 I_{OUT} = 1 A

図 4. Flyback Diode Switching Waveform in BCM



See 図 23

図 5. Startup Characteristic

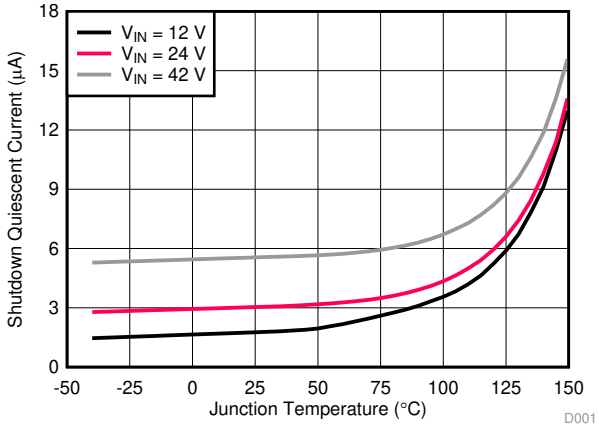


図 6. Shutdown Quiescent Current vs. Temperature

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Typical Characteristics (continued)

V_{IN} = 24 V, $V_{EN/UVLO}$ = 2 V (unless otherwise stated).

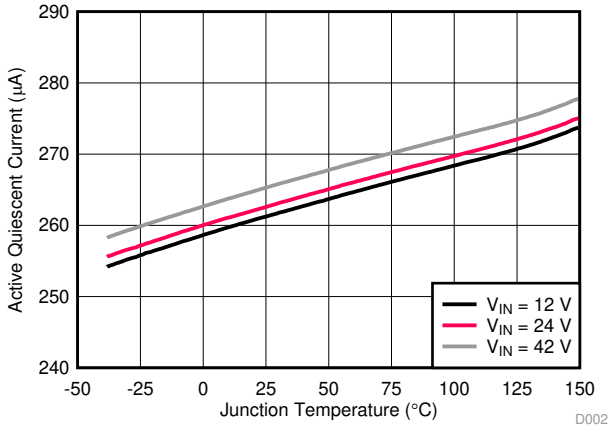
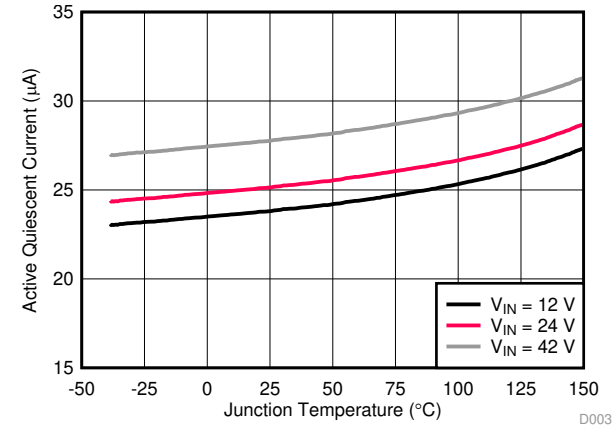


図 7. Active Quiescent Current vs. Temperature



$V_{SS/BIAS}$ = 6 V

図 8. Active Quiescent Current with BIAS vs. Temperature

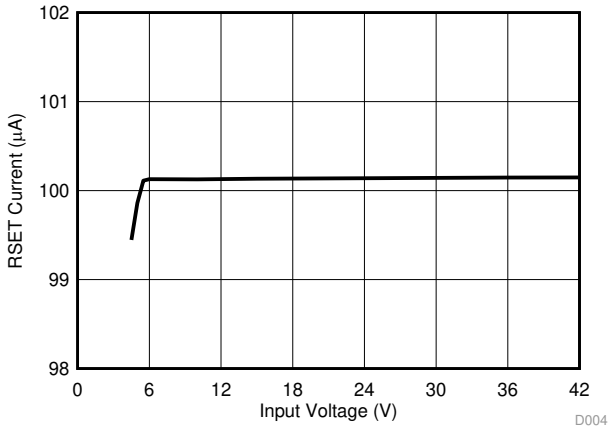


図 9. RSET Current vs. Input Voltage

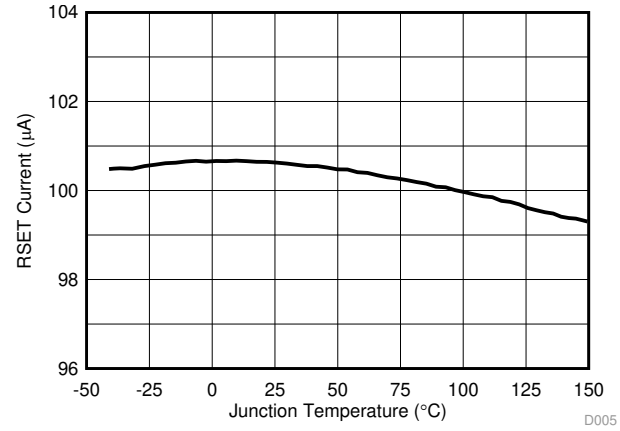


図 10. RSET Current vs. Temperature

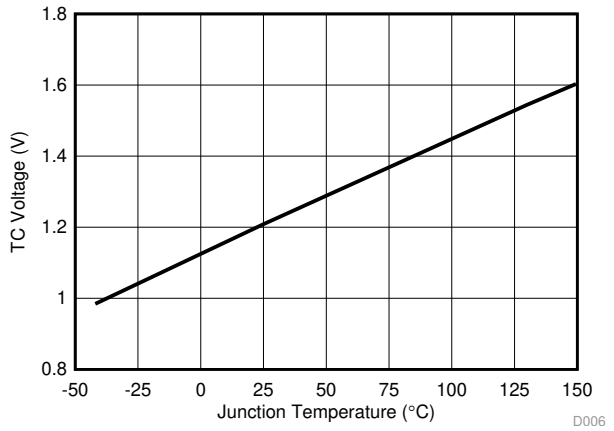


図 11. TC Voltage vs. Temperature

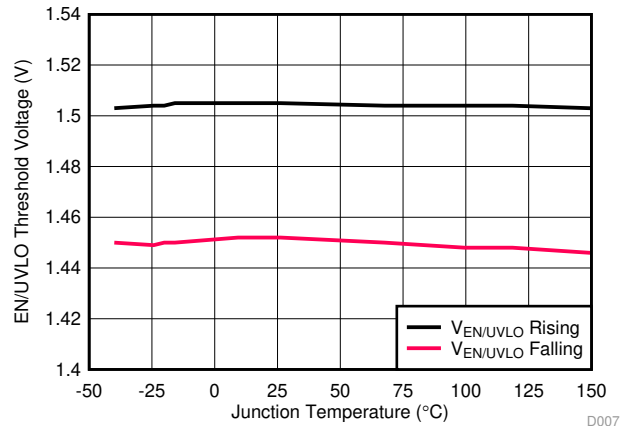


図 12. EN/UVLO Threshold Voltages vs. Temperature

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Typical Characteristics (continued)

V_{IN} = 24 V, $V_{EN/UVLO}$ = 2 V (unless otherwise stated).

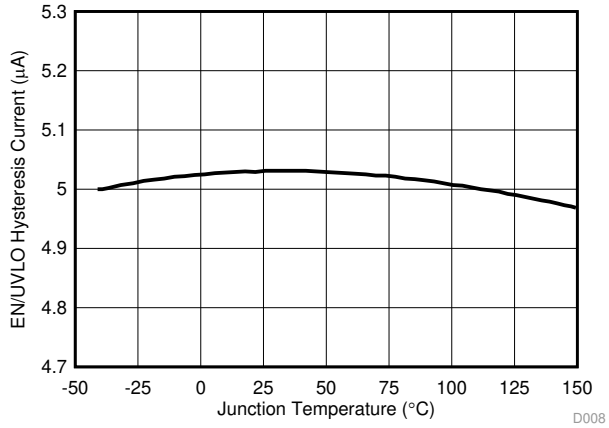

図 13. EN/UVLO Hysteresis Current vs. Temperature

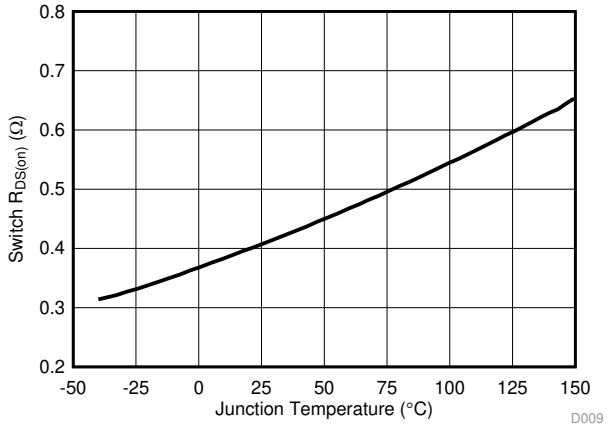

図 14. MOSFET $R_{DS(on)}$ vs. Temperature

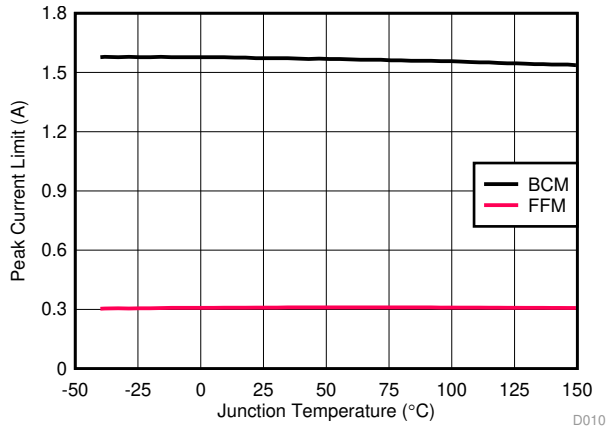

図 15. Switch Peak Current Limits vs. Temperature

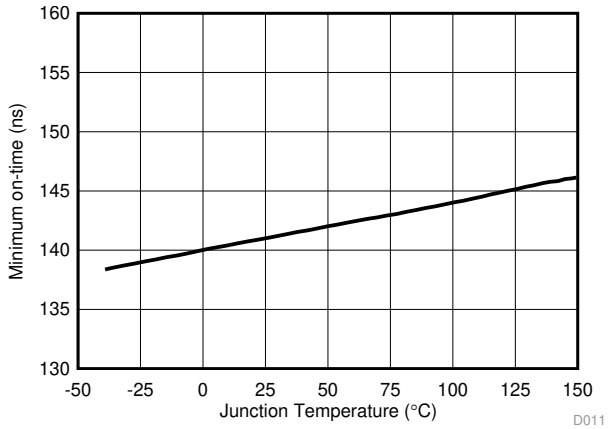

図 16. Minimum Switch On-Time vs. Temperature

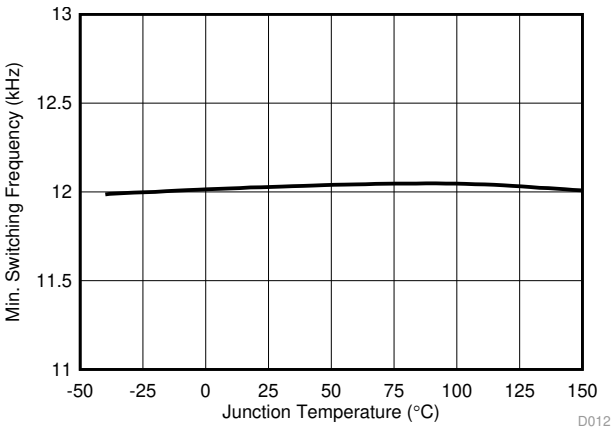

図 17. Minimum Switching Frequency vs. Temperature

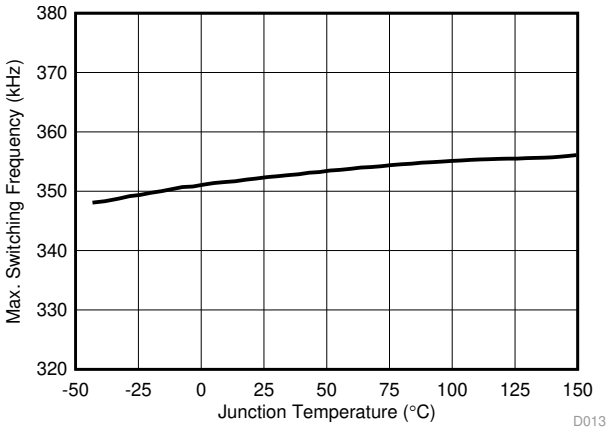

図 18. Maximum Switching Frequency vs. Temperature

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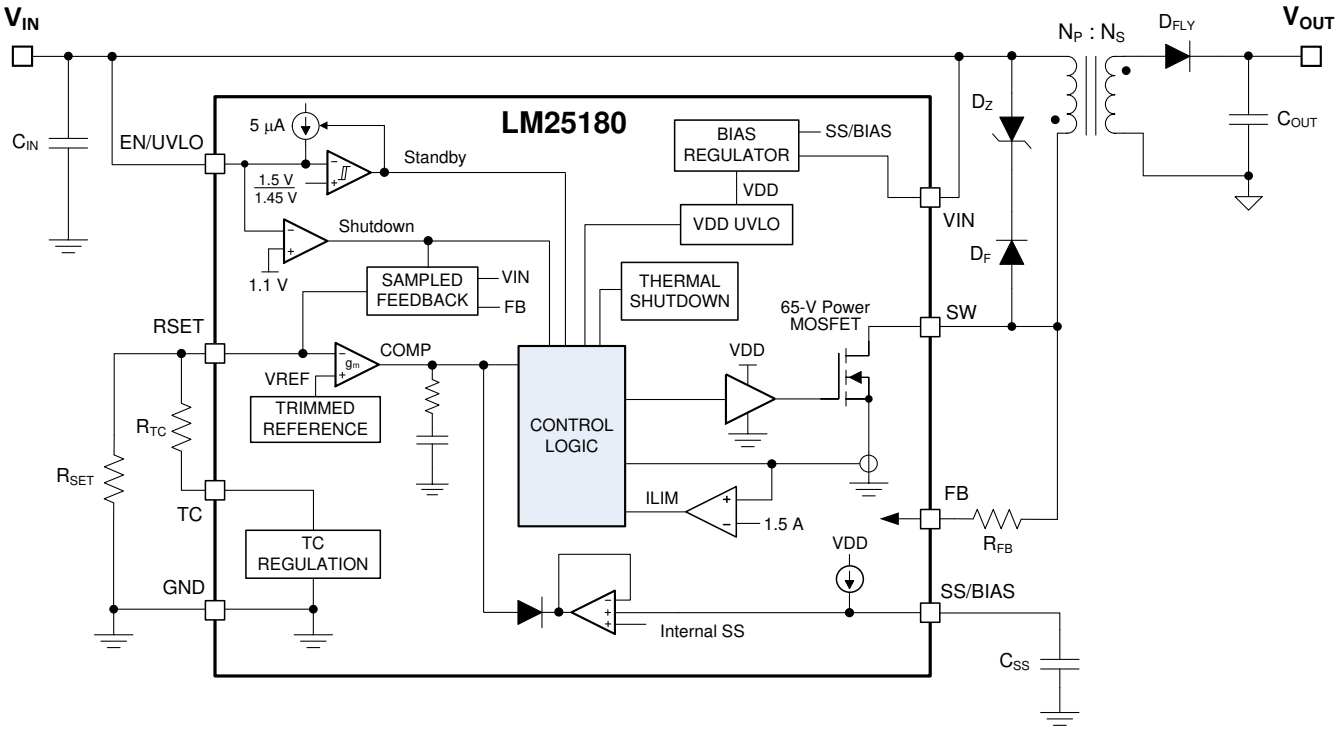
8 Detailed Description

8.1 Overview

The LM25180 primary-side regulated (PSR) flyback converter is a high-density, cost-effective solution for industrial systems requiring less than 7 W of isolated DC/DC power. This compact, easy-to-use flyback converter with low I_Q can be applied over a wide input voltage range from 4.5 V to 42 V, with operation down to 3.5 V after startup. Innovative frequency and current amplitude modulation enables high conversion efficiency across the entire load and line range. Primary-side regulation of the isolated output voltage using sampled values of the primary winding voltage eliminates the need for an opto-coupler or an auxiliary transformer winding for feedback. Regulation performance that rivals that of traditional opto-coupler solutions is achieved without the associated cost, solution size and reliability concerns. The LM25180 converter services a wide range of applications including IGBT-based motor drives, factory automation, and medical equipment.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Integrated Power MOSFET

The LM25180 is a flyback dc/dc converter with integrated 65-V, 1.5-A N-channel power MOSFET. During the MOSFET on-time, the transformer primary current increases from zero with slope V_{IN} / L_{MAG} (where L_{MAG} is the transformer primary-referred magnetizing inductance) while the output capacitor supplies the load current. When the high-side MOSFET is turned off by the control logic, the SW voltage V_{SW} swings up to approximately V_{IN} + (N_{PS} × V_{OUT}), where N_{PS} = N_P/N_S is the primary-to-secondary turns ratio of the transformer. The magnetizing current flows in the secondary side through the flyback diode, charging the output capacitor and supplying current to the load. Duty cycle D is defined as t_{ON} / t_{SW}, where t_{ON} is the MOSFET conduction time and t_{SW} is the switching period.

図 19 shows a typical schematic of the LM25180 PSR flyback circuit. Components denoted in red are optional depending on the application requirements.

Feature Description (continued)

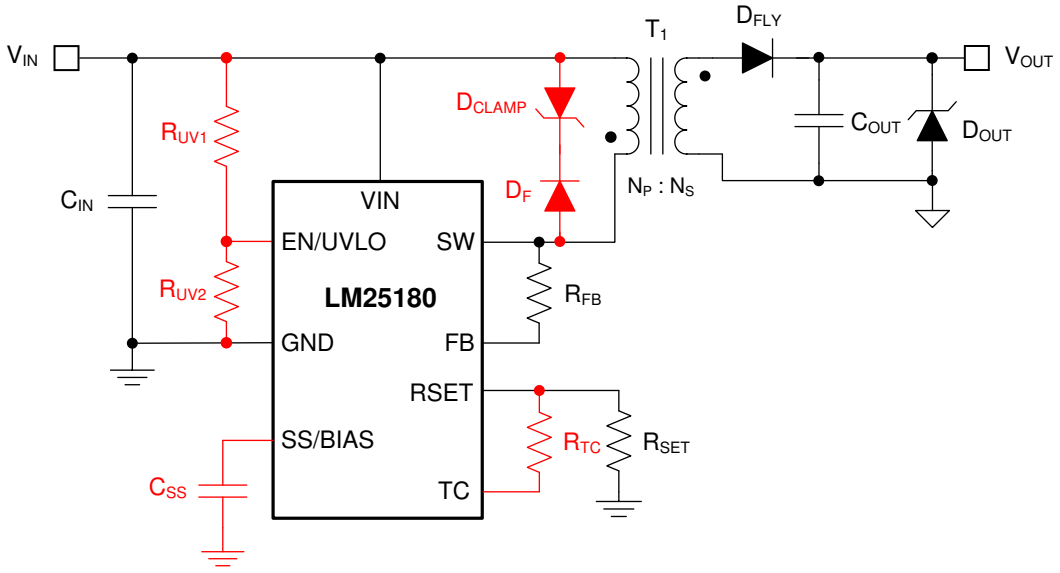


図 19. LM25180 Flyback Converter Schematic (Optional Components in Red)

8.3.2 PSR Flyback Modes of Operation

The LM25180 uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as illustrated in 図 20.

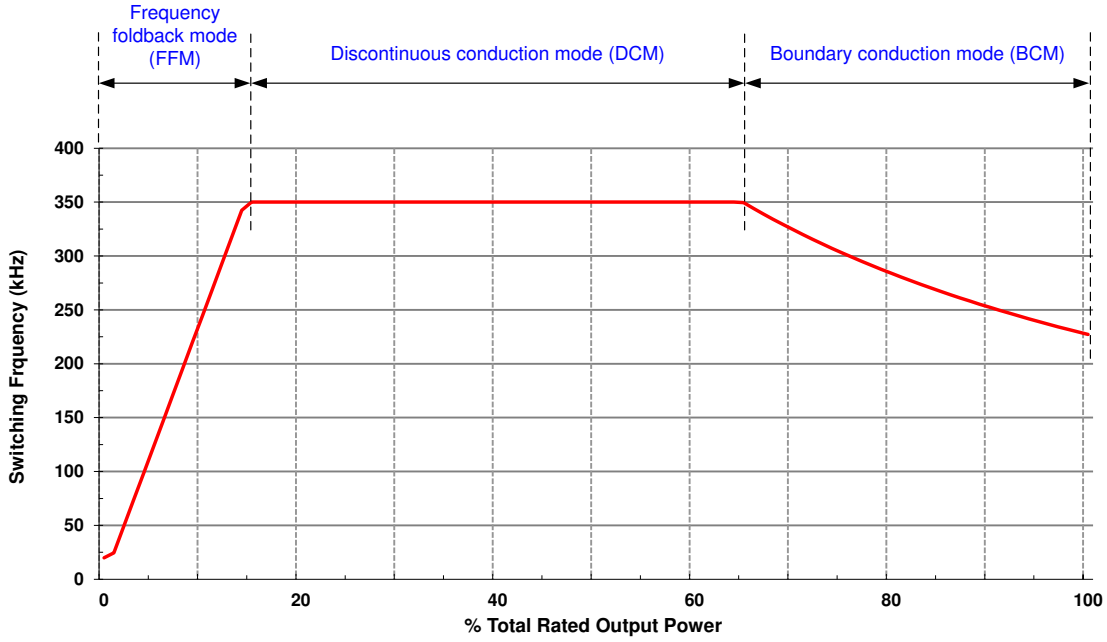


図 20. Three Modes of Operation Illustrated by Variation of Switching Frequency With Load

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Feature Description (continued)

The LM25180 operates in boundary conduction mode (BCM) at heavy loads. The power MOSFET turns on when the current in the secondary winding reaches zero, and the MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the frequency increases in order to maintain BCM operation. The duty cycle of the flyback converter is given 式 1, where V_D is the forward voltage drop of the flyback diode as its current approaches zero.

$$D_{BCM} = \frac{(V_{OUT} + V_D) \cdot N_{PS}}{V_{IN} + (V_{OUT} + V_D) \cdot N_{PS}} \tag{1}$$

The output power in BCM is given by 式 2, where the applicable switching frequency and peak primary current in BCM are specified by 式 3 and 式 4, respectively.

$$P_{OUT(BCM)} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(BCM)}^2}{2} \cdot F_{SW(BCM)} \tag{2}$$

$$F_{SW(BCM)} = \frac{1}{I_{PRI\text{-}PK(BCM)} \cdot \left(\frac{L_{MAG}}{V_{IN}} + \frac{L_{MAG}}{N_{PS} \cdot (V_{OUT} + V_D)} \right)} \tag{3}$$

$$I_{PRI\text{-}PK(BCM)} = \frac{2 \cdot (V_{OUT} + V_D) \cdot I_{OUT}}{V_{IN} \cdot D} \tag{4}$$

As the load decreases, the LM25180 clamps the maximum switching frequency to 350 kHz, and the converter enters discontinuous conduction mode (DCM). The power delivered to the output in DCM is proportional to the peak primary current squared as given by 式 5 and 式 6. Thus, as the load decreases, the peak current reduces to maintain regulation at 350-kHz switching frequency.

$$P_{OUT(DCM)} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(DCM)}^2}{2} \cdot F_{SW(DCM)} \tag{5}$$

$$I_{PRI\text{-}PK(DCM)} = \sqrt{\frac{2 \cdot I_{OUT} \cdot (V_{OUT} + V_D)}{L_{MAG} \cdot F_{SW(DCM)}}} \tag{6}$$

$$D_{DCM} = \frac{L_{MAG} \cdot I_{PRI\text{-}PK(DCM)} \cdot F_{SW(DCM)}}{V_{IN}} \tag{7}$$

At even lighter loads, the primary-side peak current set by the internal error amplifier decreases to a minimum level of 0.3 A, or 20% of its 1.5-A peak value, and the MOSFET off-time extends to maintain the output load requirement. The system operates in frequency foldback mode (FFM), and the switching frequency decreases as the load current is reduced. Other than a fault condition, the lowest frequency of operation of the LM25180 is 12 kHz, which sets a minimum load requirement of approximately 0.5% full load.

8.3.3 Setting the Output Voltage

To minimize output voltage regulation error, the LM25180 senses the reflected secondary voltage when the secondary current reaches zero. The feedback (FB) resistor, which is connected between SW and FB as shown in 図 19, is determined using 式 8, where R_{SET} is nominally 12.1 kΩ.

$$R_{FB} = (V_{OUT} + V_D) \cdot N_{PS} \cdot \frac{R_{SET}}{V_{REF}} \tag{8}$$

ADVANCE INFORMATION

Feature Description (continued)

8.3.3.1 Diode Thermal Compensation

The LM25180 employs a unique thermal compensation circuit that adjusts the feedback setpoint based on the thermal coefficient of the flyback diode's forward voltage drop. Even though the output voltage is measured when the secondary current is effectively zero, there is still a non-zero forward voltage drop associated with the flyback diode. Select the thermal compensation resistor using 式 9.

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \cdot \frac{3\,mV/°C}{TC_{Diode}} \quad (9)$$

The temperature coefficient of the diode voltage drop may not be explicitly provided in the diode datasheet, so the effective value can be estimated based on the measured output voltage shift over temperature when the TC resistor is not installed.

8.3.4 Control Loop Error Amplifier

The inputs of the error amplifier include a level-shifted version of the FB voltage and an internal 1.21-V reference set by the resistor at RSET. A type-2 internal compensation network stabilizes the converter. In BCM operation when the output voltage is in regulation, an on-time interval is initiated when the secondary current reaches zero. The power MOSFET is subsequently turned off when an amplified version of the peak primary current exceeds the error amplifier output.

8.3.5 Precision Enable

The precision EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis for application specific power-up and power-down requirements. EN/UVLO connects to a comparator with a 1.5-V reference voltage and 50-mV hysteresis. An external logic signal can be used to drive the EN/UVLO input to toggle the output on and off for system sequencing or protection. The simplest way to enable the LM25180 is to connect EN/UVLO directly to V_{IN}. This allows the LM25180 to start up when V_{IN} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in 図 21 to establish a precision UVLO level.

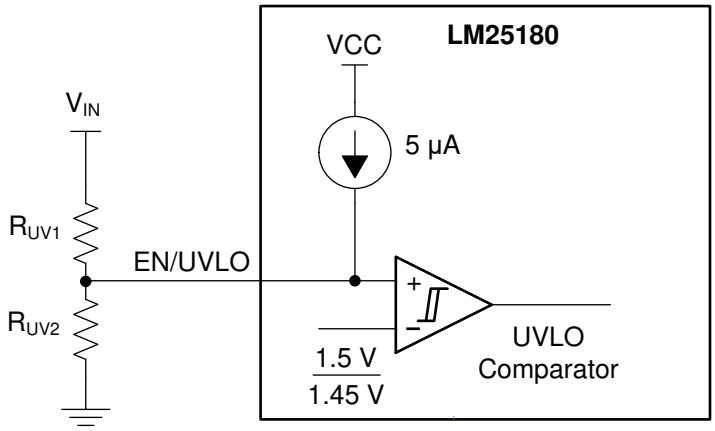

図 21. Programmable Input Voltage UVLO With Hysteresis

Use 式 10 and 式 11 to calculate the input UVLO voltages turn-on and turn-off voltages, respectively, where $V_{UV\text{-}RISING}$ and $V_{UV\text{-}FALLING}$ are the UVLO comparator thresholds and $I_{UV\text{-}HYST}$ is the hysteresis current.

$$V_{IN(on)} = V_{UV\text{-}RISING}\left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (10)$$

$$V_{IN(off)} = V_{UV\text{-}FALLING}\left(1 + \frac{R_{UV1}}{R_{UV2}}\right) - I_{UV\text{-}HYST} \cdot R_{UV2} \quad (11)$$

ADVANCE INFORMATION

Feature Description (continued)

The LM25180 also provides a low-I_Q shutdown mode when the EN/UVLO voltage is pulled below a base-emitter voltage drop (approximately 0.6 V at room temperature). If the EN/UVLO voltage is below this hard shutdown threshold, the internal LDO regulator powers off, and the internal bias-supply rail collapses, shutting down the bias currents of the LM25180. The LM25180 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision-enable thresholds.

8.3.6 Configurable Soft Start

The LM25180 has a flexible and easy-to-use soft-start control pin, SS/BIAS. The soft-start feature prevents inrush current impacting the LM25180 and the input supply when power is first applied. This is achieved by controlling the voltage at the output of the internal error amplifier. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable and adjustable start-up timing options include a 6-ms internally-fixed soft start and an externally-programmable soft start.

The simplest way to use the LM25180 is to leave SS/BIAS open. The LM25180 employs an internal soft-start control ramp and starts up to the regulated output voltage in 6 ms.

However, in applications with a large amount of output capacitance, higher V_{OUT} or other special requirements, the soft-start time can be extended by connecting an external capacitor C_{SS} from SS/BIAS to GND. A longer soft-start time further reduces the supply current needed to charge the output capacitors while sourcing the required load current. When the EN/UVLO voltage exceeds the UVLO rising threshold and a delay of 20 µs expires, an internal current source I_{SS} of 5 µA charges C_{SS} and generates a ramp to control the primary current amplitude. Calculate the soft-start capacitance for a desired soft-start time, t_{SS}, using 式 12.

$$C_{SS}\left[nF\right] = 5 \cdot t_{SS}\left[ms\right] \tag{12}$$

C_{SS} is discharged by an internal FET when switching is disabled by EN/UVLO or thermal shutdown.

8.3.7 External Bias Supply

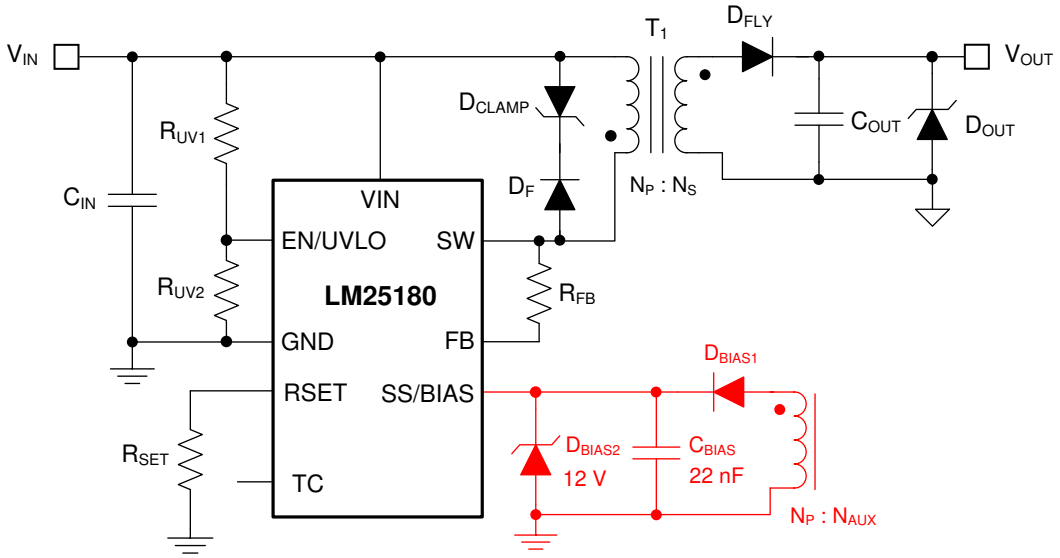

図 22. External Bias Supply Using Transformer Auxiliary Winding

The LM25180 has an external bias supply feature that reduces input quiescent current and increases efficiency. When the voltage at SS/BIAS exceeds a rising threshold of 5.5 V, bias power for the internal LDO regulator can be derived from an external voltage source or from a transformer auxiliary winding as shown in 図 22. With a bias supply connected, the LM25180 then uses its internal soft-start ramp to control the primary current during start-up.

ADVANCE INFORMATION

Feature Description (continued)

When using a transformer auxiliary winding for bias power, the total leakage current related to diodes D_{BIAS1} and D_{BIAS2} in 図 22 should be less than 1 µA across the full operating temperature range.

8.3.8 Minimum On-Time and Off-Time

When the internal power MOSFET is turned off, the leakage inductance of the transformer resonates with the SW node parasitic capacitance. The resultant ringing behavior can be excessive with large transformer leakage inductance and may corrupt the secondary zero-current detection. In order to prevent such a situation, a minimum switch off-time, designated as $t_{OFF-MIN}$, of maximum 450 ns is set internally to ensure proper functionality. This sets a lower limit for the transformer magnetizing inductance as discussed in Detailed Design Procedure.

Furthermore, noise effects as a result of power MOSFET turn-on can impact the internal current sense circuit measurement. To mitigate this effect, the LM25180 provides a blanking time after the MOSFET turns on. This blanking time forces a minimum on-time, t_{ON-MIN}, of 140 ns.

8.3.9 Overcurrent Protection

In case of an overcurrent condition on the isolated output(s), the output voltage drops lower than the regulation level since the maximum power delivered is limited by the peak current capability on the primary side. The peak primary current is maintained at 1.5 A (plus an amount related to the 100-ns propagation delay of the current limit comparator) until the output decreases to the secondary diode voltage drop to impact the reflected signal on the primary side. At this point, the LM25180 assumes the output cannot be recovered and re-calibrates its switching frequency to 9 kHz until the overload condition is removed. The LM25180 responds with similar behavior to an output short circuit condition.

For a given input voltage, 式 13 gives the maximum output current prior to the engagement of overcurrent protection. The typical threshold value for $I_{SW-PEAK}$ from Specifications is 1.5 A.

$$I_{OUT(max)} = \frac{I_{SW-PEAK}}{2 \cdot \left(\frac{V_{OUT} + V_D}{V_{IN}} + \frac{1}{N_{PS}} \right)} \quad (13)$$

A failsafe current limit set at 2.4A, or 1.6 times the nominal peak current limit, provides redundant fault protection in case of transformer short circuit or saturation effects. This initiates a 7.5ms hiccup interval after eight overcurrent events.

8.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 175°C to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the restarts when the junction temperature falls to 169°C.

ADVANCE INFORMATION

8.4 Device Functional Modes

8.4.1 Shutdown Mode

EN/UVLO facilitates ON and OFF control for the LM25180. When $V_{EN/UVLO}$ is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 3 μA at V_{IN} = 24 V. The LM25180 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below its UV threshold, the converter remains off.

8.4.2 Standby Mode

The internal bias rail LDO regulator has a lower enable threshold than the converter itself. When $V_{EN/UVLO}$ is above 0.6 V and below the precision-enable threshold (1.5 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal VCC is above its UV threshold. The switching action and voltage regulation are not enabled until $V_{EN/UVLO}$ rises above the precision enable threshold.

8.4.3 Active Mode

The LM25180 is in active mode when $V_{EN/UVLO}$ is above the precision-enable threshold and the internal bias rail is above its UV threshold. The LM25180 operates in one of three modes depending on the load current requirement:

1. Boundary conduction mode (BCM) at heavy loads.
2. Discontinuous conduction mode (DCM) at medium loads.
3. Frequency foldback mode (FFM) at light loads.

Refer to *PSR Flyback Modes of Operation* for more detail.

ADVANCE INFORMATION

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM25180 requires only a few external components to convert from a wide range of supply voltages to one or more isolated output rails. To expedite and streamline the process of designing of a LM25180-based converter, a comprehensive LM25180 quick-start calculator is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both single- and dual-output implementations using specific circuit design examples.

As mentioned previously, the LM25180 also integrates several optional features to meet system design requirements, including precision enable, input UVLO, programmable soft start, output voltage thermal compensation, and external bias supply connection. Each application incorporates these features as needed for a more comprehensive design.

The application circuits detailed in *Typical Applications* show LM25180 configuration options suitable for several application use cases. Refer to the *LM5180EVM-S05* and *LM5180EVM-DUAL* EVM user's guides for more detail.

9.2 Typical Applications

For step-by-step design procedures, circuit schematics, bill of materials, PCB files, simulation and test results of LM25180-powered implementations, refer to the *TI Designs* reference design library.

9.2.1 Design 1: Wide V_{IN}, Low I_Q PSR Flyback Converter Rated at 5 V, 1 A

The schematic diagram of a 5-V, 1-A PSR flyback converter is given in 図 23.

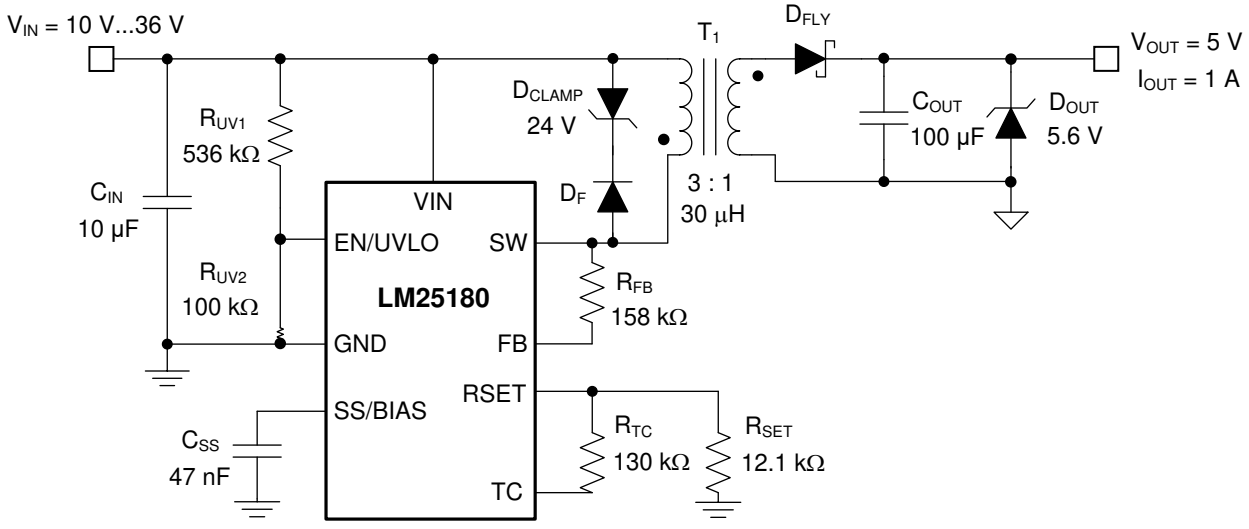

図 23. Schematic for Design 1 With $V_{IN(nom)}$ = 24 V, V_{OUT} = 5 V, I_{OUT} = 1 A

9.2.1.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 1.

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表 1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	10 V to 36 V
Input UVLO thresholds	9.5 V on, 6.5 V off
Output voltage	5 V
Rated load current, V_{IN} = 24 V	1 A
Output voltage regulation	±1.5%
Output voltage ripple	< 100 mV

The target full-load efficiency is 86% based on a nominal input voltage of 24 V and an isolated output voltage of 5 V. The LM25180 is chosen to deliver a fixed 5-V output voltage set by resistor R_{FB} connected between the SW and FB pins. The input voltage turn-on and turn-off thresholds are established by R_{UV1} and R_{UV2}. The required components are listed in 表 2.

表 2. List of Components for Design 1

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325AB7106KM-T
C_{OUT}	1	100 µF, 6.3 V, X7S, 1210, ceramic	Murata	GRM32EC70J107ME15
			Taiyo Yuden	JMK325AC7107MM-P
		100 µF, 6.3 V, X5R, 1210, ceramic	TDK	C3225X5R0J107M250AC
			Würth Electronik	885012109004
C_{SS}	1	47 nF, 16 V, X7R, 0402	Std	Std
D_{CLAMP}	1	Zener, 24 V, 1 W, PowerDI-123	DFLZ24-7	Diodes Inc.
D_F	1	Switching diode, 75 V, 0.25 A, SOD-323	CMDD4448	Central Semi
D_{FLY}	1	Schottky diode, 40 V, 2 A, SOD-123	FSV340FP	ONsemi
D_{OUT}	1	Zener, 5.6 V, 5%, SOD-523	BZX585-C5V6	Nexperia
R_{FB}	1	158 kΩ, 1%, 0402	Std	Std
R_{SET}	1	12.1 kΩ, 1%, 0402	Std	Std
R_{TC}	1	130 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	536 kΩ, 1%, 0603	Std	Std
R_{UV2}	1	100 kΩ, 1%, 0402	Std	Std
T_1	1	30 µH, 2 A, turns ratio 3 : 1, 9.3 × 10.2 mm	Coilcraft	YA8779-BLD
			Würth Electronik	750317605
		30 µH, 2.6 A, turns ratio 3 : 1, 12.5 × 15.5 mm	Sumida	12387-T151
		40 µH, 2 A, turns ratio 3 : 1, 13.3 × 15.2 mm	Würth Electronik	750313974
U_1	1	LM25180 PSR flyback converter, VSON-8	Texas Instruments	LM25180NGUR

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25180 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats

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- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the converter specifications using the LM25180 quick-start calculator.

9.2.1.2.3 Flyback Transformer – T_1

Choose a turns ratio based on an approximate 60% max duty cycle at minimum input voltage using 式 14, rounding up or down as needed.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.6}{1 - 0.6} \cdot \frac{10\,V}{5\,V + 0.3\,V} = 3 \tag{14}$$

Select a magnetizing inductance based on the minimum off-time constraint using 式 15. Choose a value of 30 µH with a saturation current of minimum 2 A for this application.

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \cdot N_{PS} \cdot t_{OFF\text{-}MIN}}{I_{PRI\text{-}PK(FFM)}} = \frac{(5\,V + 0.3\,V) \cdot 3 \cdot 450\,ns}{0.3\,A} = 23.9\,\mu H \tag{15}$$

Note that a higher magnetizing inductance provides a larger operating range for BCM and FFM, but the leakage inductance may increase based on a higher number of primary turns, N_P. The primary and secondary winding RMS currents are given by 式 16 and 式 17, respectively.

$$I_{PRI\text{-}RMS} = \sqrt{\frac{D}{3}} \cdot I_{PRI\text{-}PK} \tag{16}$$

$$I_{SEC\text{-}RMS} = \sqrt{\frac{2 \cdot I_{OUT} \cdot I_{PRI\text{-}PK} \cdot N_{PS}}{3}} \tag{17}$$

Find the maximum output current for a given turns ratio using 式 18, where the typical value for $I_{PRI\text{-}PK(max)}$ is the 1.5 A switch current peak threshold. Iterate by increasing the turns ratio if the output current capability is too low at minimum input voltage.

$$I_{OUT(max)} = \frac{I_{PRI\text{-}PK(max)}}{2 \cdot \left[\frac{V_{OUT} + V_D}{V_{IN}} + \frac{1}{N_{PS}} \right]} \tag{18}$$

9.2.1.2.4 Flyback Diode – D_{FLY}

The flyback diode reverse voltage is given by 式 19.

$$V_{D\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS}} + V_{OUT} = \frac{36\,V}{3} + 5\,V = 17\,V \tag{19}$$

Select a 40-V, 3-A Schottky diode for this application to account for inevitable diode voltage overshoot and ringing related to the resonance of transformer leakage inductance and diode parasitic capacitance. Connect an appropriate RC snubber circuit (for example, 100 Ω and 22 pF) across the flyback diode if needed.

In general, choose a flyback diode with current rating greater than the maximum peak secondary winding current of N_{PS}*$I_{PRI\text{-}PK(max)}$. As mentioned in Layout, place adequate copper at the cathode of the diode to improve its thermal performance and prevent overheating during high ambient temperature or overload conditions. Beware of the high leakage current typical of a Schottky diode at elevated operating temperatures.

9.2.1.2.5 Zener Clamp Circuit – D_F, D_{CLAMP}

Connect a diode-Zener clamping circuit across the primary winding to limit the peak switch-node voltage after MOSFET turn-off below the maximum level of 65 V, as given by 式 20.

ADVANCE INFORMATION

$$V_{DZ(clamp)} < V_{SW(max)} - V_{IN(max)} \tag{20}$$

Choosing the zener, D_{CLAMP}, with clamp voltage of approximately 1.5 times the reflected output voltage, as specified by 式 21, provides a balance between the maximum SW voltage excursion and the leakage inductance demagnetization time.

$$V_{DZ(clamp)} = 1.5 \cdot N_{PS} \cdot \left(V_{OUT} + V_D\right) = 1.5 \cdot 3 \cdot \left(5\,V + 0.3\,V\right) \approx 24\,V \tag{21}$$

Select an ultra-fast switching diode or Schottky diode for D_F with rated voltage greater than the maximum input voltage and with low forward recovery voltage drop.

9.2.1.2.6 Output Capacitor – C_{OUT}

The output capacitor determines the voltage ripple at the converter output, limits the voltage excursion during a load transient, and sets the dominant pole of the converter's small-signal response. For a flyback converter specifically, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function of load current and duty cycle.

Select an output capacitance using 式 22 to limit the ripple voltage amplitude to less than 1% of the output voltage at minimum input voltage.

$$C_{OUT} \geq \frac{I_{OUT(max)}}{\Delta V_{OUT}} \cdot \frac{L_{MAG} \cdot I_{PRI\text{-}PK(max)}}{V_{IN}} \tag{22}$$

Substituting the maximum load current at minimum input voltage from 式 18, transformer inductance, peak switch current and peak-to-peak ripple voltage specification gives C_{OUT} greater than 72 µF.

Mindful of the voltage coefficient of ceramic capacitors, select a 100-µF, 6.3-V capacitor in 1210 case size with X5R or better dielectric. 式 23 gives the output capacitor RMS ripple current.

$$I_{COUT\text{-}RMS} = I_{OUT} \cdot \sqrt{\frac{2 \cdot N_{PS} \cdot I_{PRI\text{-}PK}}{3 \cdot I_{OUT}} - 1} \tag{23}$$

9.2.1.2.7 Input Capacitor – C_{IN}

Select an input capacitance using 式 24 to limit the ripple voltage amplitude to less than 5% of the input voltage when operating at nominal input voltage.

$$C_{IN} \geq \frac{I_{PRI\text{-}PK} \cdot D \cdot \left(1 - \frac{D}{2}\right)^2}{2 \cdot F_{SW} \cdot \Delta V_{IN}} \tag{24}$$

Substituting the input current at full load, switching frequency, peak primary current and peak-to-peak ripple specification gives C_{IN} greater than 2 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 10-µF, 50-V ceramic input capacitor with X7R dielectric in 1210 case size. 式 25 gives the input capacitor RMS ripple current.

$$I_{CIN\text{-}RMS} = \frac{D \cdot I_{PRI\text{-}PK}}{2} \cdot \sqrt{\frac{4}{3 \cdot D} - 1} \tag{25}$$

9.2.1.2.8 Feedback Resistor – R_{FB}

Select a feedback resistor, designated R_{FB}, of 158 kΩ based on the secondary winding voltage at the end of the flyback conduction interval (the sum of the 5-V output voltage and the Schottky diode forward voltage drop) reflected by the transformer turns ratio of 3 : 1. The forward voltage drop of the flyback diode is 0.3 V as its current approaches zero.

$$R_{FB} = \frac{\left(V_{OUT} + V_D\right) \cdot N_{PS}}{0.1\,mA} = \frac{\left(5\,V + 0.3\,V\right) \cdot 3}{0.1\,mA} = 158\,k\Omega \tag{26}$$

ADVANCE INFORMATION

9.2.1.2.9 Thermal Compensation Resistor – R_{TC}

Select a resistor for output voltage thermal compensation, designated R_{TC}, based on 式 27.

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \cdot \frac{3\ mV/°C}{TC_{Diode}} = \frac{158\ k\Omega \cdot 3}{3 \cdot 1.2} = 130\ k\Omega \tag{27}$$

9.2.1.2.10 UVLO Resistors – R_{UV1}, R_{UV2}

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turn-on and turn-off thresholds of 9.5 V and 6.5 V, respectively, select the upper and lower UVLO resistors using the following expressions:

$$R_{UV1} = \frac{V_{IN(on)} \cdot \frac{V_{UV\text{-}FALLING}}{V_{UV\text{-}RISING}} - V_{IN(off)}}{I_{UV\text{-}HYST}} = \frac{9.5\ V \cdot \frac{1.45\ V}{1.5\ V} - 6.5\ V}{5\ \mu A} = 536 k\Omega \tag{28}$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{UV\text{-}RISING}}{V_{IN(on)} - V_{UV\text{-}RISING}} = 536\ k\Omega \cdot \frac{1.5\ V}{9.5\ V - 1.5\ V} = 100\ k\Omega \tag{29}$$

9.2.1.2.11 Soft-Start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on 式 12 to achieve a soft-start time of 9 ms.

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power Management* technical articles.

9.2.1.3 *Application Curves*

Unless otherwise stated, application performance curves were taken at T_A = 25°C.

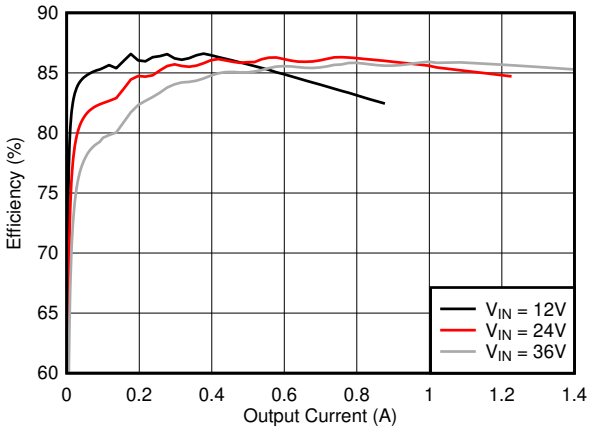


図 24. Efficiency (Linear Scale)

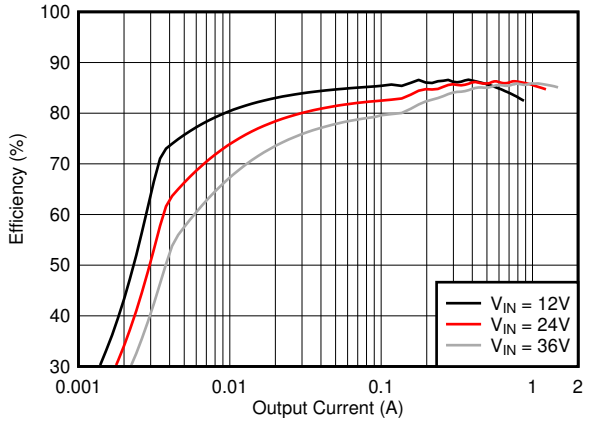


図 25. Efficiency (Log Scale)

ADVANCE INFORMATION

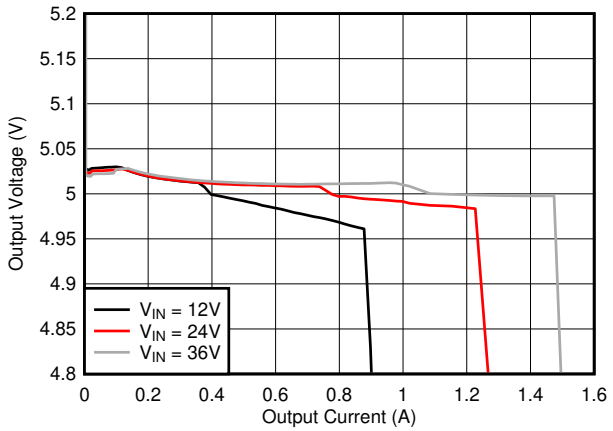


図 26. Load Regulation (Linear Scale)

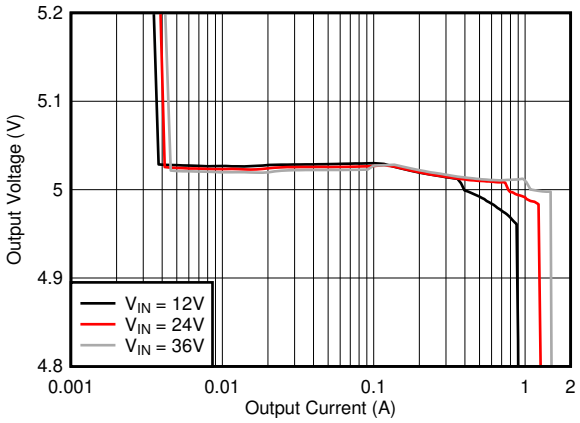
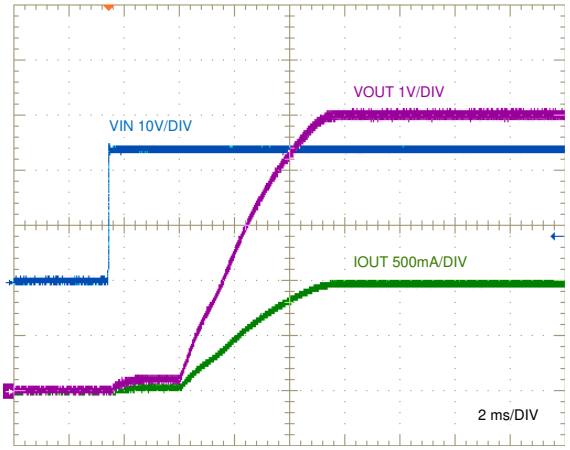
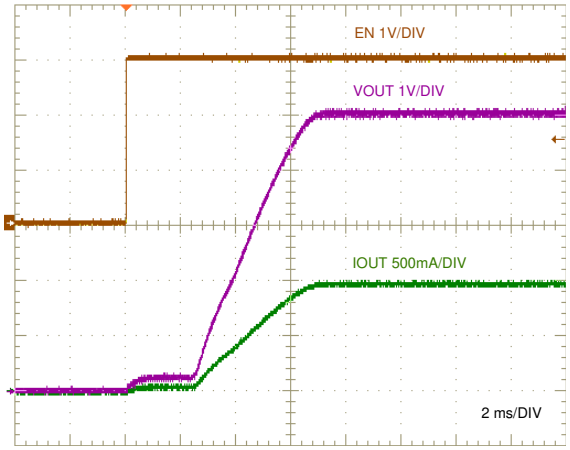


図 27. Load Regulation (Log Scale)



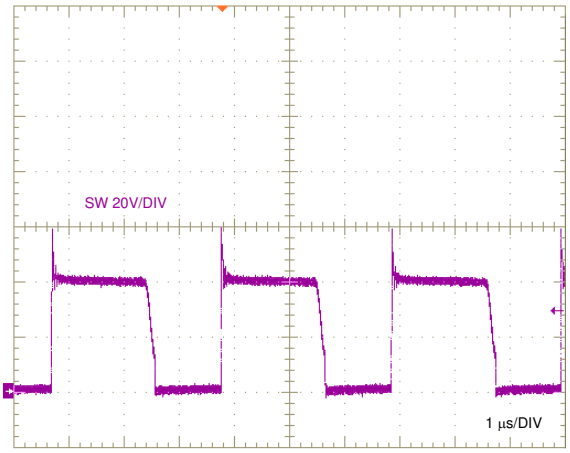
VIN stepped to 24 V　　5-Ω Load

図 28. Start-up Characteristic



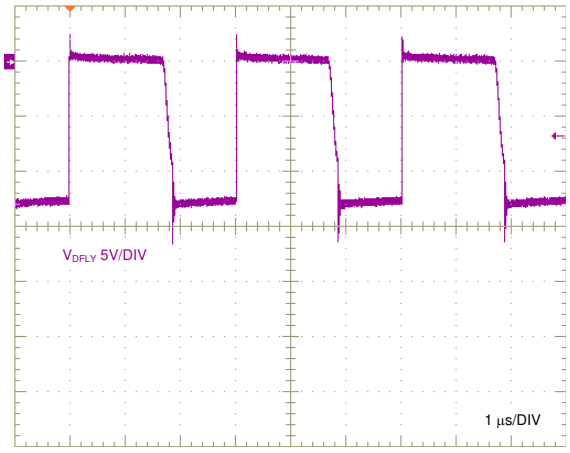
VIN = 24 V　　5-Ω Load

図 29. Enable ON Characteristic



VIN = 24 V　　IOUT = 1 A

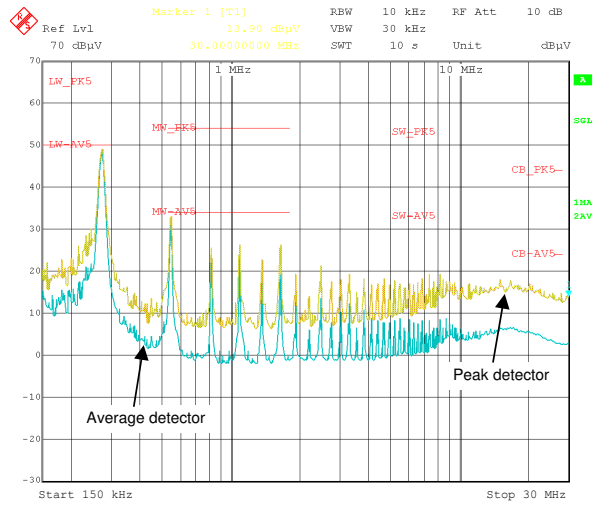
図 30. SW Node Voltage



VIN = 24 V　　IOUT = 1 A

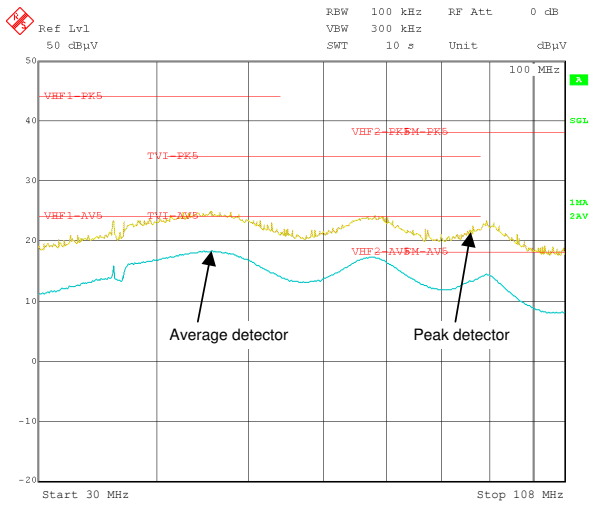
図 31. Flyback Diode Voltage

ADVANCE INFORMATION



V_{IN} = 24 V
I_{OUT} = 0.85 A
150 kHz to 30 MHz
L_{IN} = 4.7 µH
C_{IN} = 10 µF

図 32. CISPR 25 Class 5 Conducted EMI Plot



V_{IN} = 24 V
I_{OUT} = 0.85 A
30 MHz to 108 MHz
L_{IN} = 4.7 µH
C_{IN} = 10 µF

図 33. CISPR 25 Class 5 Conducted EMI Plot

ADVANCE INFORMATION

9.2.2 Design 2: PSR Flyback Converter With Dual Outputs of 15 V and –7.7 V at 200 mA

The schematic diagram of a dual-output flyback converter intended for isolated IGBT and SiC MOSFET gate drive power supply applications is given in 図 34.

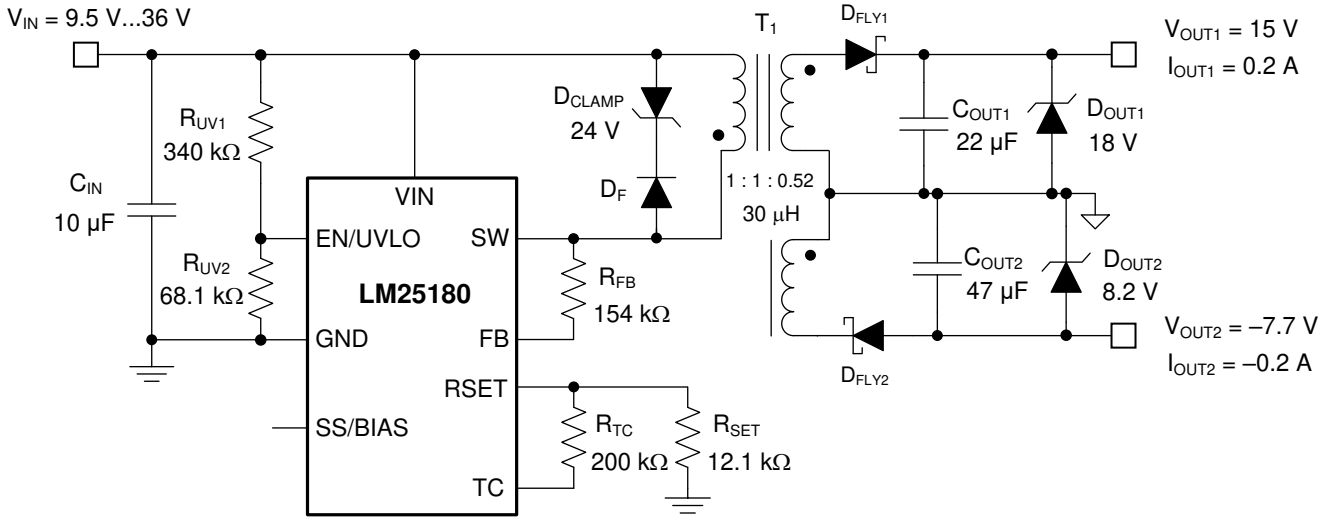


図 34. Schematic for Design 2 With $V_{IN(nom)}$ = 24 V, V_{OUT1} = 15 V, V_{OUT2} = –7.7 V, I_{OUT} = 200 mA

9.2.2.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 3.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	9.5 V to 36 V
Output 1 voltage and current	15 V, 0.2 A
Output 2 voltage and current	–7.7 V, –0.2 A
Input UVLO thresholds	9 V on, 7 V off
Output voltage regulation	±2%

The target full-load efficiency of this LM25180 design is 88% based on a nominal input voltage of 24 V and isolated output voltages of 15 V and –7.7 V sharing a common return. The selected flyback converter components are cited in 表 4, including multi-winding flyback transformer, input and output capacitors, rectifying diodes and flyback converter IC.

ADVANCE INFORMATION

表 4. List of Components for Design 2

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}	1	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325AB7106KM-T
C_{OUT1}	1	22 µF, 25 V, X7R, 1210, ceramic	TDK	C3225X7R1E226M
			Murata	GRM32ER71E226KE15L
			Taiyo Yuden	TMK325B7226MM-TR
C_{OUT2}	1	47 µF, 10 V, X7R, 1210, ceramic	TDK	C3225X7R1A476M
			Murata	GRM32ER71A476ME15L
			Taiyo Yuden	LMK325B7476MM-TR
D_{FLY1}	1	Schottky diode, 100 V, 1 A, PowerDI-123	DFLS1100-7	Diodes Inc.
D_{FLY2}	1	Schottky diode, 60 V, 1 A, PowerDI-123	DFLS160-7	Diodes Inc.
D_{CLAMP}	1	Zener, 24 V, 1 W, PowerDI-123	DFLZ24-7	Diodes Inc.
D_F	1	Switching diode, 75 V, 0.3 A, SOD323	1N4148WS	Diodes Inc.
D_{OUT1}	1	Zener, 18 V, 5%, SOD523	BZX585-C18	Nexperia
D_{OUT2}	1	Zener, 8.2 V, 2%, SOD523	BZX585-B8V2	Nexperia
R_{FB}	1	154 kΩ, 1%, 0402	Std	Std
R_{SET}	1	12.1 kΩ, 1%, 0402	Std	Std
R_{TC}	1	200 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	340 kΩ, 1%, 0603	Std	Std
R_{UV2}	1	68.1 kΩ, 1%, 0402	Std	Std
T_1	1	30 µH, 2 A, turns ratio 1 : 1: 0.52, 9 × 10 mm, SMT	Coilcraft	YA8916-BLD
			Würth Electronik	750317595
U_1	1	LM25180 PSR flyback converter, VSON-8	Texas Instruments	LM25180NGUR

9.2.2.2 Detailed Design Procedure

Using the LM25180 quick-start calculator, components are selected based on the flyback converter specifications.

9.2.2.2.1 Flyback Transformer – T_1

Set the turns ratio of the transformer secondary windings using 式 30, where N_{S1} and N_{S2} are the number of secondary turns for the respective outputs.

$$\frac{N_{S2}}{N_{S1}} = \frac{V_{OUT2} + V_{D2}}{V_{OUT1} + V_{D1}} = \frac{7.7\ V + 0.3\ V}{15\ V + 0.3\ V} = 0.52 \tag{30}$$

Choose a primary-secondary turns ratio for the 15-V output based on an approximate 60% max duty cycle at minimum input voltage using 式 31. The transformer turns ratio for both outputs is thus specified as 1 : 1 : 0.52.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.6}{1 - 0.6} \cdot \frac{9.5\,V}{15\,V + 0.3\,V} \approx 1 \tag{31}$$

Select a magnetizing inductance based on the minimum off-time constraint using 式 32. Choose a value of 30 µH with a saturation current of 2 A for this application.

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \cdot N_{PS} \cdot t_{OFF\text{-}MIN}}{I_{PRI\text{-}PK(FFM)}} = \frac{(15\,V + 0.35\,V) \cdot 1 \cdot 450\,ns}{0.3\,A} = 23.0\,\mu H \tag{32}$$

9.2.2.2.2 Flyback Diodes – D_{FLY1} and D_{FLY2}

The flyback diode reverse voltages for the positive and negative outputs are given respectively by 式 33 and 式 25.

ADVANCE INFORMATION

$$V_{D1\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS}} + V_{OUT1} = \frac{36\,V}{1} + 15\,V = 51V \tag{33}$$

$$V_{D2\text{-}REV} \geq \frac{V_{IN(max)}}{N_{PS}} + \left|V_{OUT2}\right| = 36\,V \cdot 0.52 + 7.7\,V = 26.4\,V \tag{34}$$

Choose 100-V, 1-A and 60-V, 1-A Schottky diodes for the positive and negative outputs, respectively, to allow some margin for inevitable voltage overshoot and ringing related to leakage inductance and diode capacitance. If needed, use a diode RC snubber circuit, for example 100 Ω and 22 pF, to mitigate such overshoot and ringing.

9.2.2.2.3 Input Capacitor – C_{IN}

The input capacitor, C_{IN}, filters the primary-side triangular current waveform. To prevent large ripple voltage, use a low-ESR ceramic input capacitor sized according to 式 24 for the RMS ripple current given by 式 25. In this design example, choose a 10-µF, 50-V ceramic input capacitor with X7R dielectric and 1210 footprint.

9.2.2.2.4 Feedback Resistor – R_{FB}

Install a 154-kΩ resistor from SW to FB based on an output voltage setpoint of 15 V (plus a flyback diode voltage drop) reflected to the primary by a transformer turns ratio of unity.

$$R_{FB} = \frac{\left(V_{OUT} + V_D\right) \cdot N_{PS}}{0.1\,mA} = \frac{\left(15\,V + 0.3\,V\right) \cdot 1}{0.1\,mA} = 154\,k\Omega \tag{35}$$

9.2.2.2.5 UVLO Resistors – R_{UV1}, R_{UV2}

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turn-on and turn-off thresholds of 9 V and 7 V, respectively, select the upper and lower UVLO resistors using 式 36 and 式 37.

$$R_{UV1} = \frac{V_{IN(on)} \cdot \frac{V_{UV\text{-}FALLING}}{V_{UV\text{-}RISING}} - V_{IN(off)}}{I_{UV\text{-}HYST}} = \frac{9\,V \cdot \frac{1.45\,V}{1.5\,V} - 7\,V}{5\,\mu A} = 340k\Omega \tag{36}$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{UV\text{-}RISING}}{V_{IN(on)} - V_{UV\text{-}RISING}} = 340\,k\Omega \cdot \frac{1.5\,V}{9\,V - 1.5\,V} = 68\,k\Omega \tag{37}$$

9.2.2.3 Application Curves

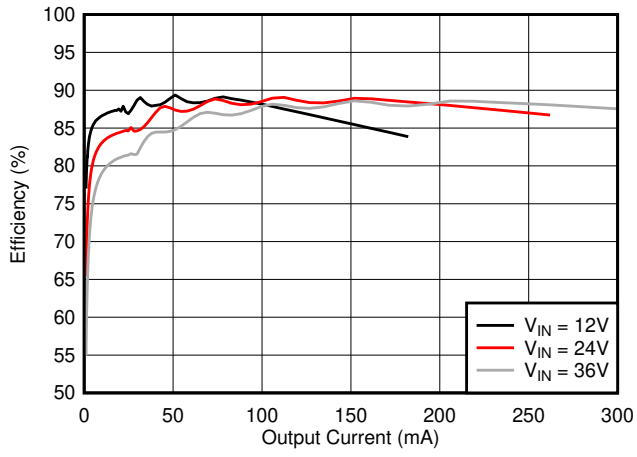


図 35. Efficiency (Linear Scale)

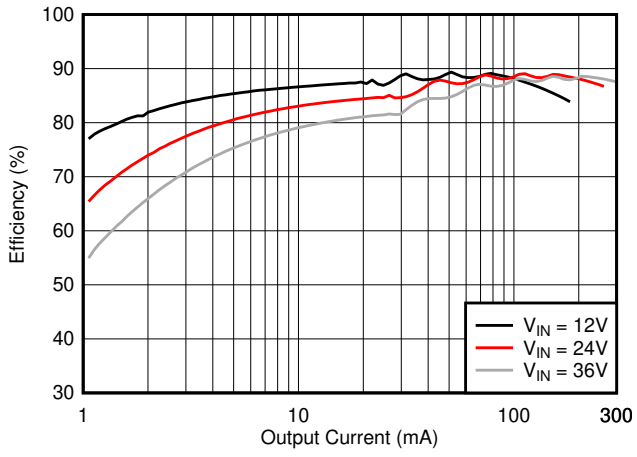
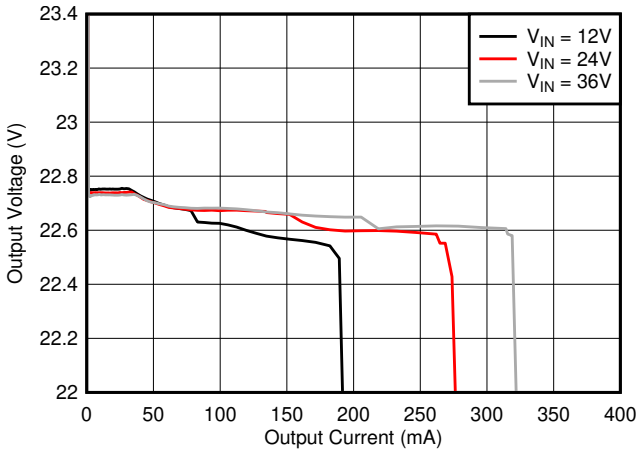


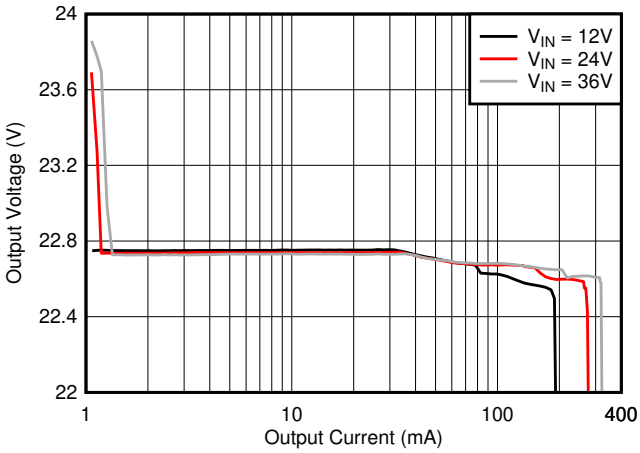
図 36. Efficiency (Log Scale)

ADVANCE INFORMATION



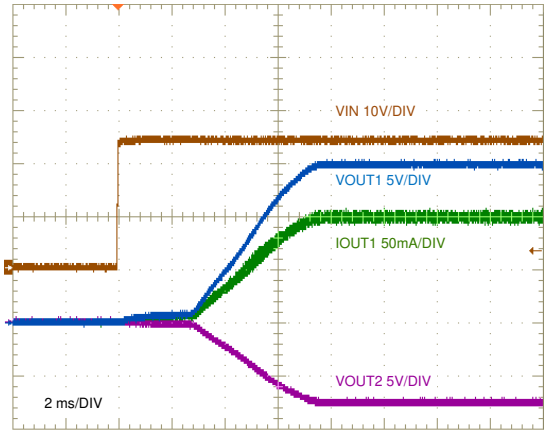
Total of V_{OUT1} and V_{OUT2}

図 37. Load Regulation (Linear Scale)



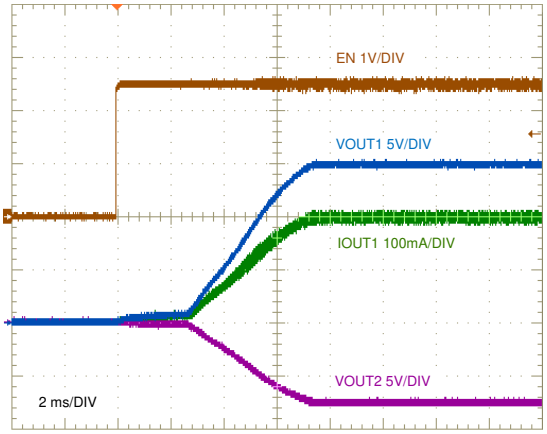
Total of V_{OUT1} and V_{OUT2}

図 38. Load Regulation (Log Scale)



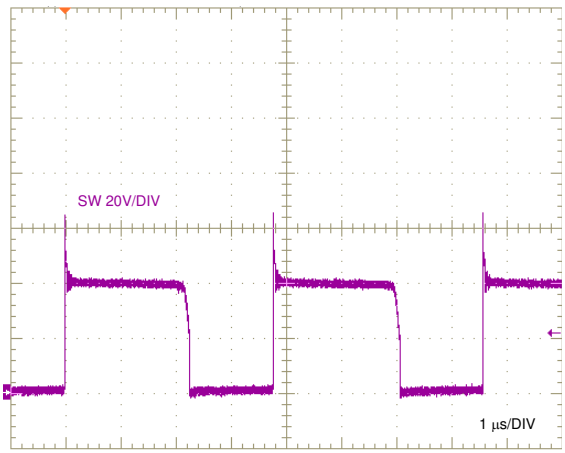
V_{IN} stepped to 24 V 75 Ω and 40 Ω Loads

図 39. Start-Up Characteristic



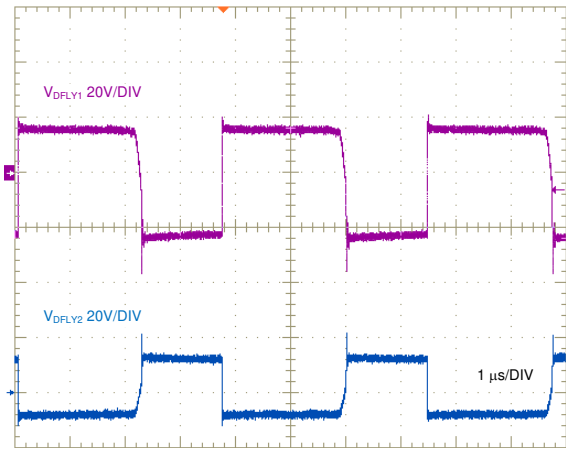
V_{IN} = 24 V 75 Ω and 40 Ω Loads

図 40. ENABLE ON Characteristic



V_{IN} = 24 V

図 41. SW Node Voltage, Full Load



V_{IN} = 24 V

図 42. Flyback Diode Voltages, Full Load

ADVANCE INFORMATION

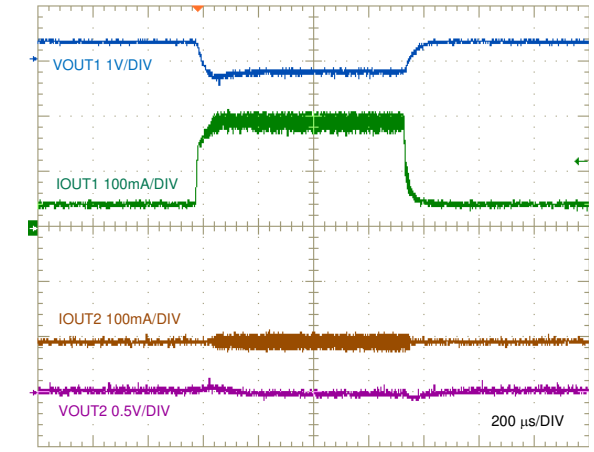


図 43. Output 1 Load Transient, 50 mA to 200 mA

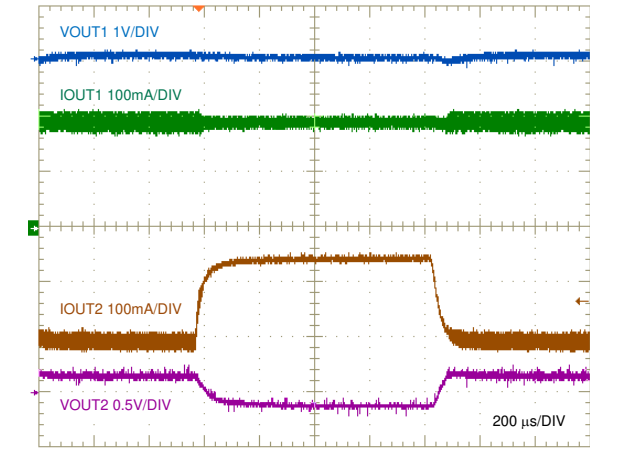


図 44. Output 2 Load Transient, 50 mA to 200 mA

ADVANCE INFORMATION

9.2.3 Design 3: PSR Flyback Converter With Stacked Dual Outputs of 24 V and 5 V

The schematic diagram of a dual-output flyback converter with high-voltage secondary stacked on the low-voltage secondary winding is given in 図 45. This configuration reduces the number of turns for the high-voltage output, resulting in lower secondary-to-secondary leakage inductance for improved output voltage cross regulation.

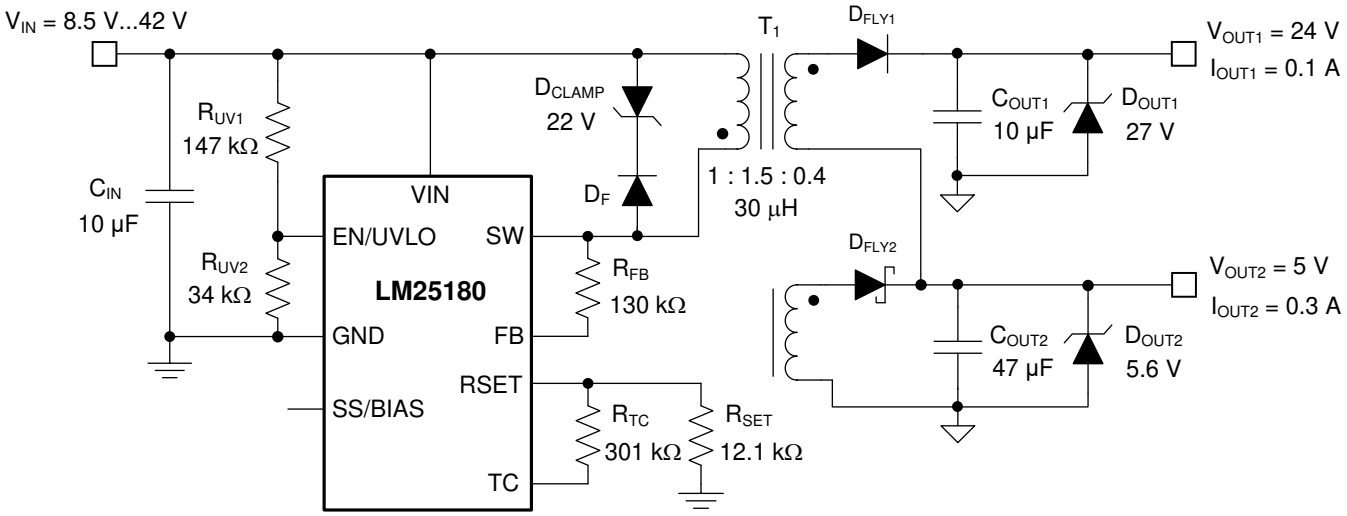


図 45. Schematic for Design 3 With $V_{IN(nom)}$ = 24 V, V_{OUT1} = 24 V, V_{OUT2} = 5 V

9.2.3.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in 表 5.

表 5. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	8.5 V to 42 V
Output 1 voltage and current	24 V, 0.1 A
Output 2 voltage and current	5 V, 0.3 A
Input UVLO thresholds	8 V on, 7 V off
Output voltage regulation	±2%

The target full-load efficiency of this LM25180 design is 88% based on a nominal input voltage of 24 V and isolated output voltages of 24 V and 5 V. The selected flyback converter components are cited in 表 6, including multi-winding flyback transformer, input and output capacitors, rectifying diodes, and converter IC.

ADVANCE INFORMATION

表 6. List of Components for Design 3

REF DES	QTY	SPECIFICATION	VENDOR	PART NUMBER
C_{IN}, C_{OUT1}	2	10 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325AB7106MM-T
		10 µF, 50 V, X7S, 1210, ceramic	TDK	C3225X7R1H106M
C_{OUT2}	1	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
D_{FLY1}	1	Switching diode, fast recovery, 200 V, 1 A, SOD-123	DFLU1200	Diodes Inc.
D_{FLY2}	1	Schottky diode, 40 V, 1 A, SOD-123	B140HW	Diodes Inc.
D_{CLAMP}	1	Zener, 22 V, 1 W, PowerDI-123	DFLZ22-7	Diodes Inc.
D_F	1	Switching diode, 75 V, 0.25 A, SOD-323	CMDD4448	Central Semi
D_{OUT1}	1	Zener, 27 V, 2%, SOD-523	BZX585-B27	Nexperia
D_{OUT2}	1	Zener, 5.6 V, 2%, SOD-523	BZX585-B5V6	Nexperia
R_{FB}	1	130 kΩ, 1%, 0402	Std	Std
R_{SET}	1	12.1 kΩ, 1%, 0402	Std	Std
R_{TC}	1	301 kΩ, 1%, 0402	Std	Std
R_{UV1}	1	147 kΩ, 1%, 0603	Std	Std
R_{UV2}	1	34 kΩ, 1%, 0402	Std	Std
T_1	1	30 µH, 2 A, turns ratio 1 : 1.5 : 0.4, 9 × 10 mm, SMT	Coilcraft	YA8864-BLD
		30 µH, 2 A, turns ratio 1 : 1 : 0.55, 9 × 10 mm, SMT	Coilcraft	YA8916-BLD
			Würth Electronik	750317595
U_1	1	LM25180 PSR flyback converter, VSON-8	Texas Instruments	LM25180NGUR

ADVANCE INFORMATION

9.2.3.2 Detailed Design Procedure

Components are selected based on the converter specifications using the LM25180 quick-start calculator. The design procedure is similar to that outlined for Designs 1 and 2 previously.

9.2.3.2.1 Flyback Transformer – T_1

The 24-V output is DC stacked on top of the 5-V output as they share a common return connection. This enables lower secondary-to-secondary leakage inductance for better cross regulation and also reduced rectifier diode reverse voltage stress. Choose a primary-secondary turns ratio for the effective 19-V secondary based on an approximate 60% max duty cycle at minimum input voltage using 式 38.

$$N_{PS} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.6}{1 - 0.6} \cdot \frac{8.5\,V}{19\,V + 0.3\,V} = 0.66 \tag{38}$$

Set the turns ratio of the transformer secondary windings using 式 39. The transformer turns ratio for both outputs is thus specified as 1 : 1.5 : 0.4.

$$\frac{N_{S2}}{N_{S1}} = \frac{V_{OUT2} + V_{D2}}{V_{OUT1} + V_{D1}} = \frac{5\ V + 0.3\ V}{19\ V + 0.3\ V} = 0.275 \tag{39}$$

Select a magnetizing inductance based on the minimum off-time constraint using 式 40. Choose a value of 30 µH with a saturation current of minimum 2 A for this application.

$$L_{MAG} \geq \frac{(V_{OUT1} + V_{D1}) \cdot N_{PS1} \cdot t_{OFF\text{-}MIN}}{I_{PRI\text{-}PK(FFM)}} = \frac{(19\,V + 0.35\,V) \cdot 0.66 \cdot 450\,ns}{0.3\,A} = 19.2\,\mu H \tag{40}$$

9.2.3.2.2 Feedback Resistor – R_{FB}

Install a 130-kΩ resistor from SW to FB based on the secondary winding voltage (the sum of the 5-V output voltage and the Schottky diode forward voltage drop) reflected by the relevant transformer turns ratio, which in this design is 1 : 0.4 or 2.5 : 1.

$$R_{FB} = \frac{(V_{OUT} + V_D) \cdot N_{PS}}{0.1\,mA} = \frac{(5\,V + 0.25\,V) \cdot 2.5}{0.1\,mA} = 130\ k\Omega \tag{41}$$

9.2.3.2.3 UVLO Resistors – R_{UV1}, R_{UV2}

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turn-on and turn-off thresholds of 8 V and 7 V, respectively, select the upper and lower UVLO resistors using the following expressions:

$$R_{UV1} = \frac{V_{IN(on)} \cdot \frac{V_{UV\text{-}FALLING}}{V_{UV\text{-}RISING}} - V_{IN(off)}}{I_{UV\text{-}HYST}} = \frac{8\ V \cdot \frac{1.45\ V}{1.5\ V} - 7\ V}{5\ \mu A} = 147 k\Omega \quad (42)$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{UV\text{-}RISING}}{V_{IN(on)} - V_{UV\text{-}RISING}} = 147\ k\Omega \cdot \frac{1.5\ V}{8\ V - 1.5\ V} = 34\ k\Omega \quad (43)$$

9.2.3.3 Application Curves

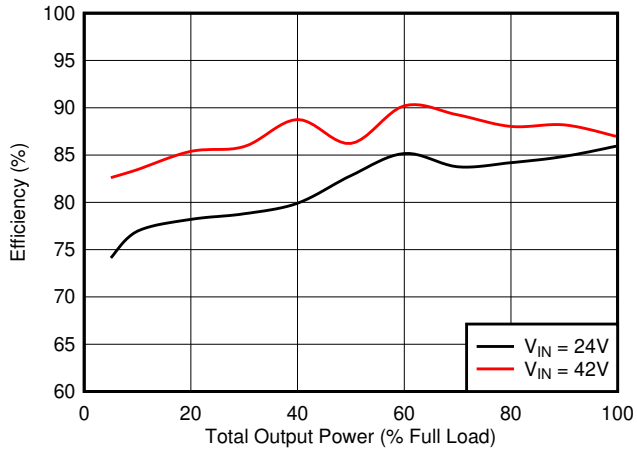


図 46. Efficiency

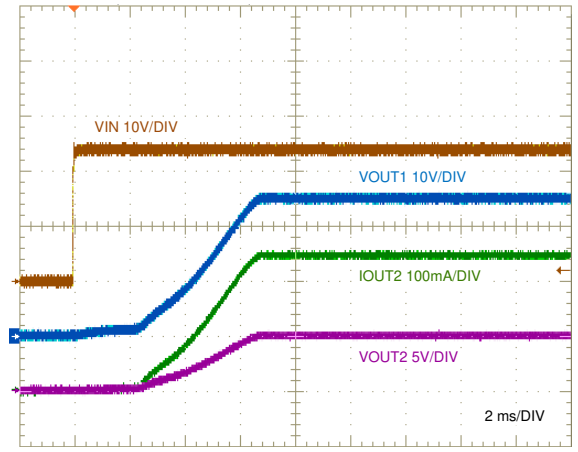


図 47. Start-Up Characteristic

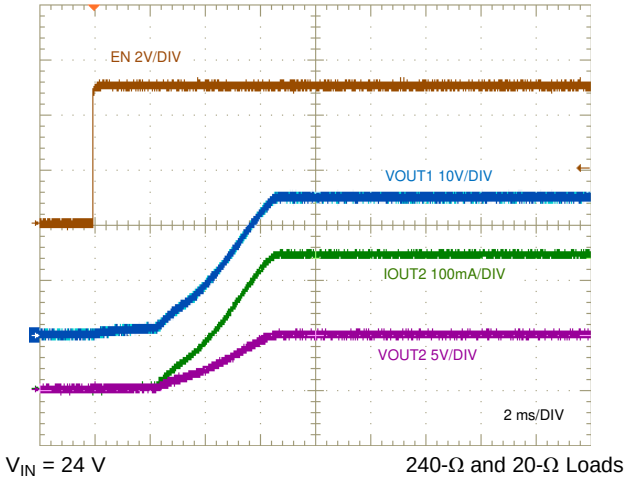


図 48. ENABLE ON Characteristic

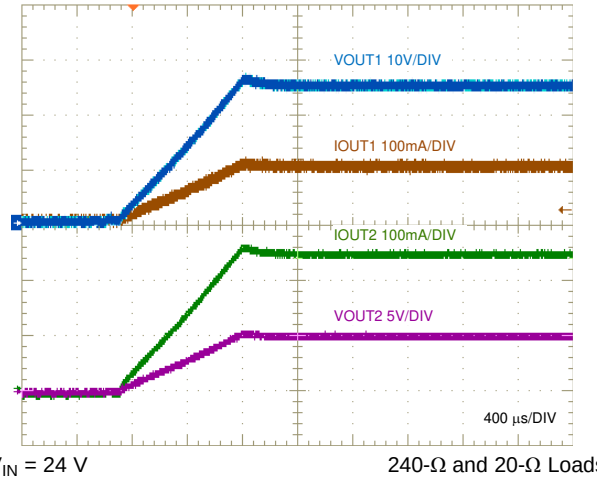
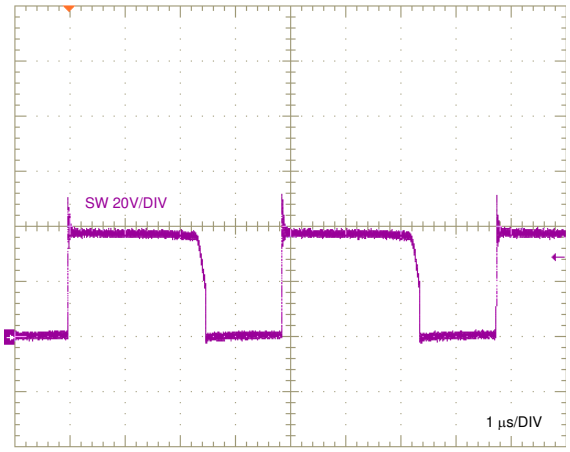


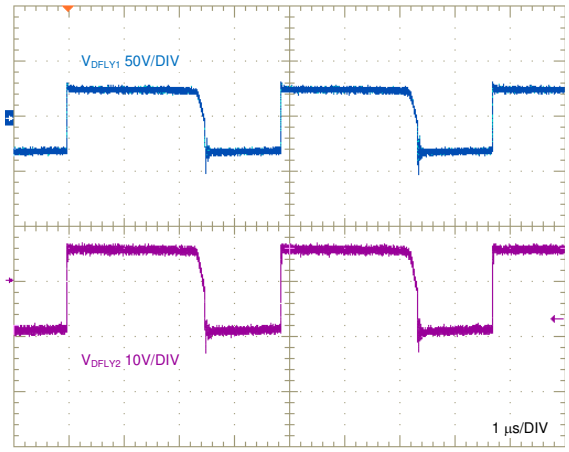
図 49. Recovery From Short Circuit

ADVANCE INFORMATION



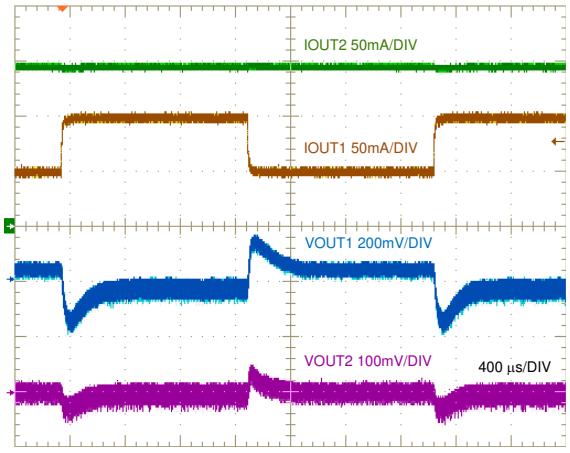
V_{IN} = 24 V

図 50. SW Node Voltage, Full Load



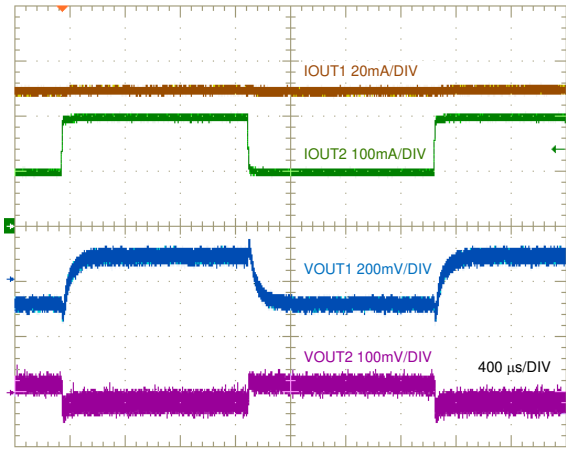
V_{IN} = 24 V

図 51. Flyback Diode Voltages, Full Load



V_{IN} = 24 V I_{OUT2} = 150 mA

図 52. Output 1 Load Transient, 50 mA to 100 mA



V_{IN} = 24 V I_{OUT1} = 50 mA

図 53. Output 2 Load Transient, 100 mA to 200 mA

ADVANCE INFORMATION

10 Power Supply Recommendations

The LM25180 flyback converter is designed to operate from a wide input voltage range from 4.5 V to 42 V. The characteristics of the input supply must be compatible with the Specifications. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with 式 44.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}$$

where

- η is the efficiency (44)

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients. A typical ESR of 0.25 Ω provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

ADVANCE INFORMATION

11 Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI. 図 54 and 図 55 provide layout examples for single-output and dual-output designs, respectively.

11.1 Layout Guidelines

PCB layout is a critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with transformer leakage inductance or parasitic capacitance to generate noise and EMI or degrade the power supply's performance.

1. Bypass the VIN pin to GND with a low-ESR ceramic capacitor, preferably of X7R or X7S dielectric. Place C_{IN} as close as possible to the LM25180 VIN and GND pins. Ground return paths for the input capacitor(s) must consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the transformer close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive e-field or capacitive coupling.
4. Minimize the loop area formed by the diode-Zener clamp circuit connections and the primary winding terminals of the transformer.
5. Minimize the loop area formed by the flyback rectifying diode, output capacitor and the secondary winding terminals of the transformer.
6. Connect adequate copper at the cathode of the flyback diode to prevent overheating during overload or high ambient temperature conditions.
7. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
8. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
9. Have a single-point ground connection to the plane. Route the return connections for the reference resistor, soft-start, and enable components directly to the GND pin. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
10. Make V_{IN+}, V_{OUT+} and ground bus connections short and wide. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
11. Minimize trace length to the FB pin. Locate the feedback resistor close to the FB pin.
12. Locate components R_{SET}, R_{TC} and C_{SS} as close as possible to their respective pins. Route with minimal trace lengths.
13. Place a capacitor between input and output return connections to route common-mode noise currents directly back to their source.
14. Provide adequate heatsinking for the LM25180 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed PAD to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. The connection to V_{OUT+} provides heatsinking for the flyback diode.

11.2 Layout Examples

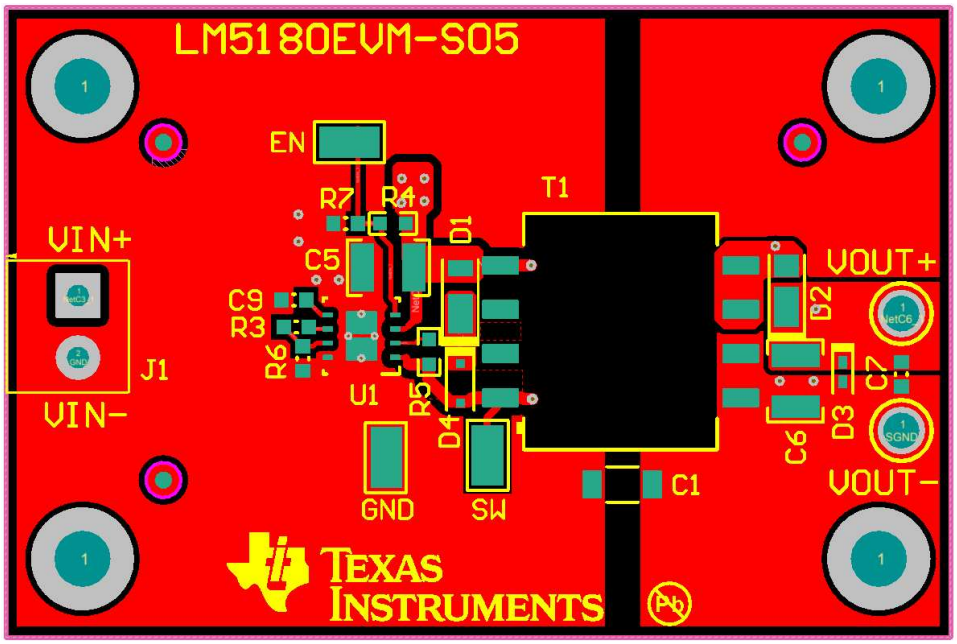


図 54. LM25180 Single-Output PCB Layout

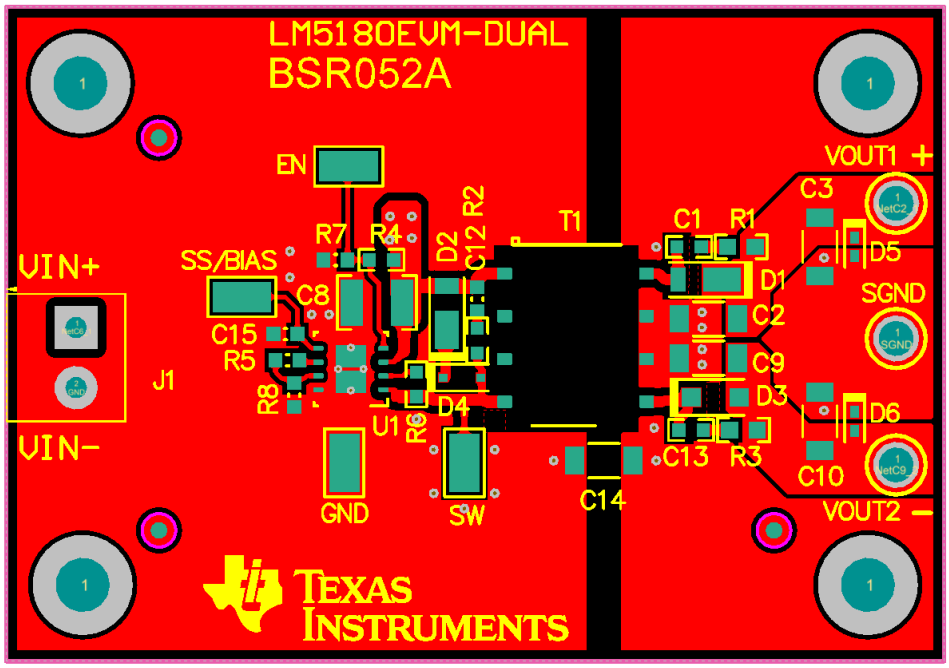


図 55. LM25180 Dual-Output PCB Layout

ADVANCE INFORMATION

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.1.2 開発サポート

開発サポートについては、以下を参照してください。

- LM25180 *クイックスタート・カリキュレータ*
- LM25180 *シミュレーション・モデル*
- TIのリファレンス・デザイン・ライブラリについては、TIDesignsを参照してください。
- TIのWEBENCH設計環境については、WEBENCH®デザイン・センターを参照してください。
- この製品の関連デバイスについては、LM5180 を参照してください。

12.1.3 WEBENCH® ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LM25180デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『LM5180EVM-S05 EVMユーザー・ガイド』*(SNVU592)
- *『LM5180EVM-DUAL EVMユーザー・ガイド』*(SNVU609)
- *『フライバックSMSP設計の詳細解説』*(SLUP261)
- *『フライバック変圧器の設計における効率とEMIの考慮事項』*(SLUP338)
- TI Designs
  - *スイッチ内蔵PSRフライバック・コントローラ搭載、絶縁型IGBTゲート・ドライブ向け電源のリファレンス・デザイン*
  - *サーボ・ドライブ向け、小型、高効率 24V 入力補助電源のリファレンス・デザイン*
  - *電源絶縁型超小型アナログ出力モジュールのリファレンス・デザイン*
  - *3 種類の IGBT/SiC 向けバイアス電源ソリューション搭載、HEV/EV トラクション・インバータ出力段のリファレンス・デザイン*
  - *IGBT/SiC ゲート・ドライバ向け、出力段搭載、4.5V～65V 入力、小型バイアス電源のリファレンス・デザイン*
- TIブログ
  - *「フライバック・コンバータ: 2つの出力が1つより適切な理由」*
  - *「サーバーPSU用の補助電源を選択するときの一般的な課題」*
  - *「限られた予算でPoE PDの効率を最大化する方法」*

ADVANCE INFORMATION

ドキュメントのサポート (continued)

- ホワイト・ペーパー
  - *『コストが重要で、要求の厳しいアプリケーション向けの広VIN、低EMI同期整流降圧回路の評価』*(SLYY104)
  - *『電源の伝導EMI仕様の概要』*(SLYY136)
  - *『電源の放射EMI仕様の概要』*(SLYY142)
- *『AN-2162: DC/DCコンバータから伝導されるEMIでの簡単な成功』*(SNVA489)
- *『車載用クランキング・シミュレータ・ユーザー・ガイド』*(SLVU984)
- *『新しい熱測定基準の使用』*(SBVA025)
- *『半導体とICパッケージの熱指標』*(SPRA953)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商標

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以下のページには、メカニカル、パッケージ、および注文の情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

ADVANCE INFORMATION

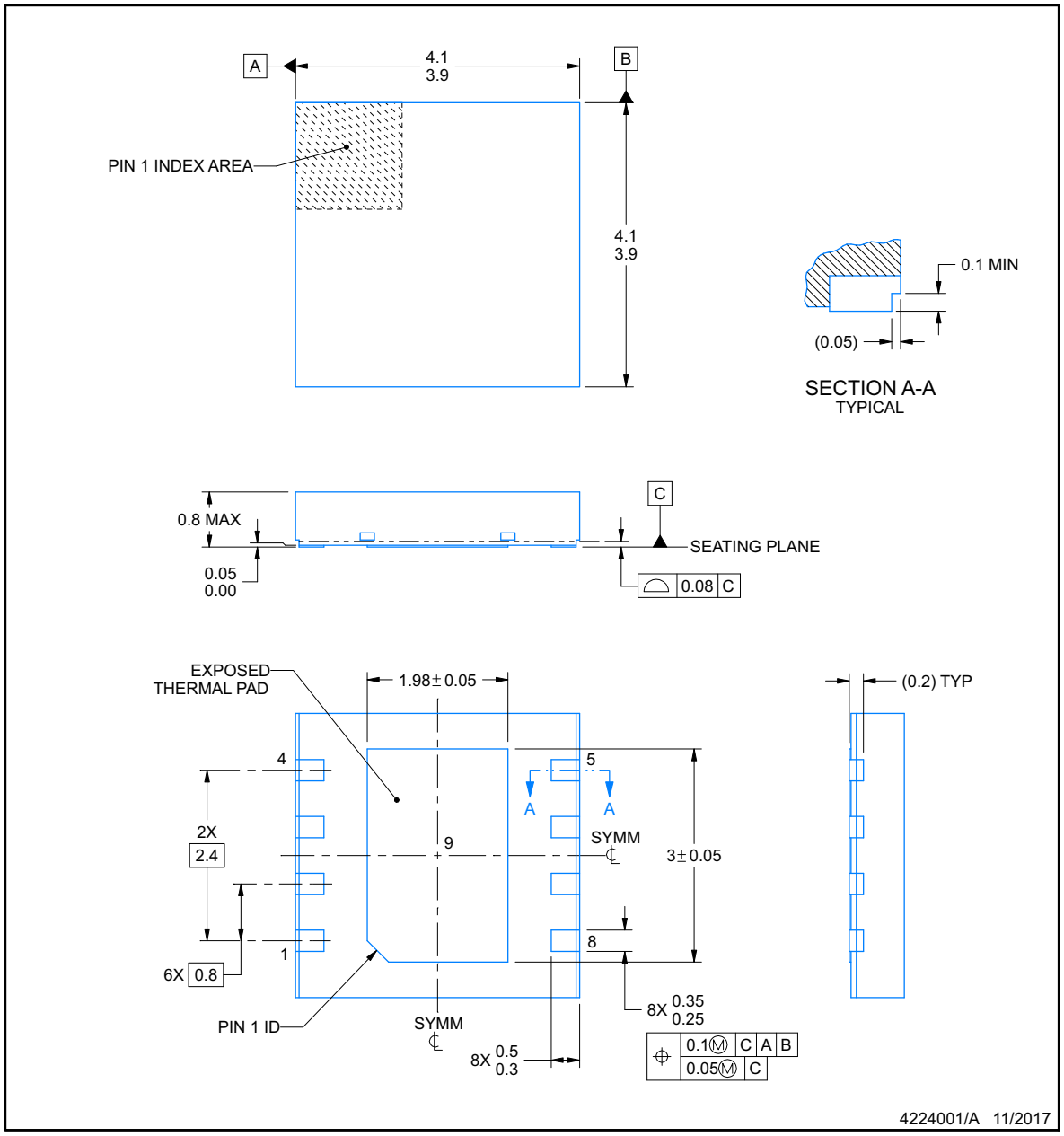
ADVANCE INFORMATION

PACKAGE OUTLINE

NGU0008C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

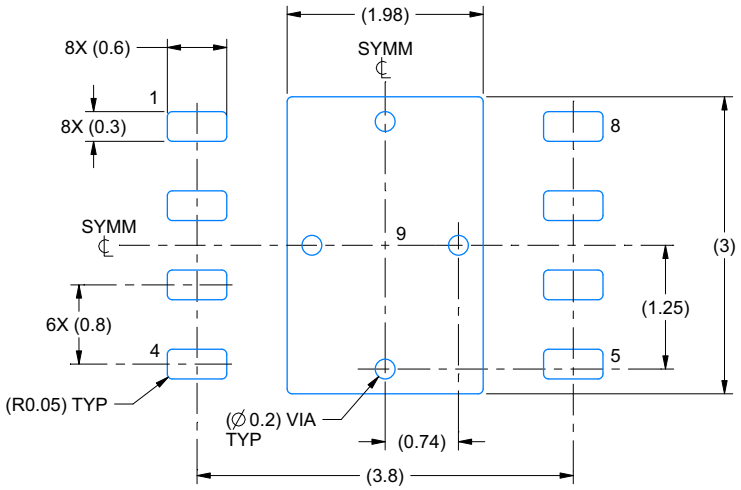
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

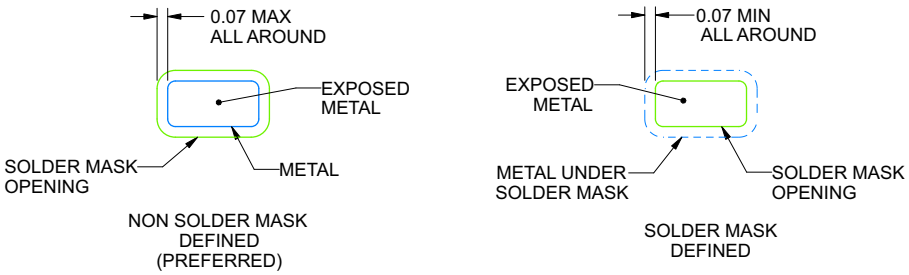
NGU0008C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4224001/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

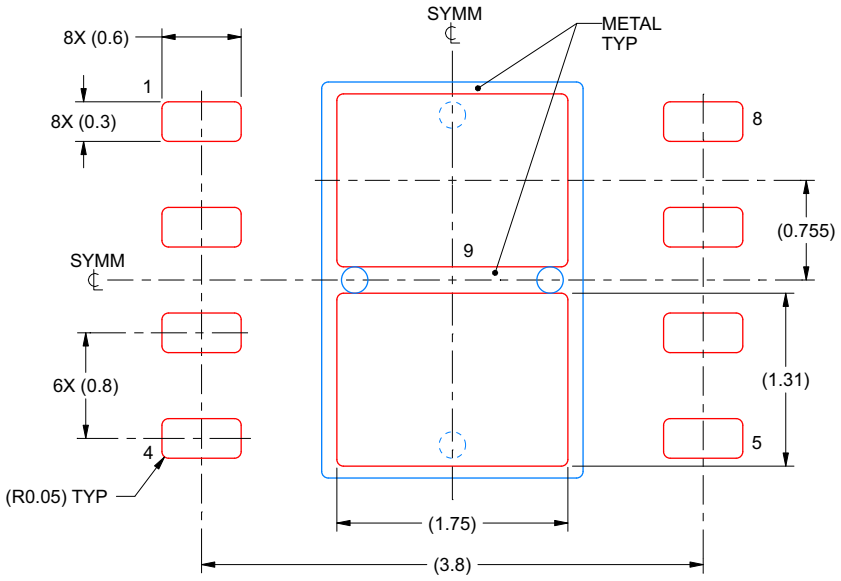
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

NGU0008C — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224001/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25180NGUR	ACTIVE	WSON	NGU	8	4500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM25180 NGU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

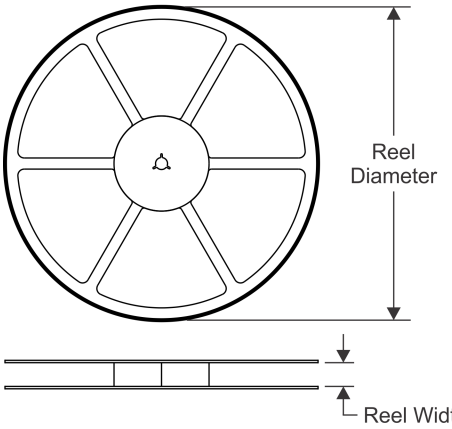
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

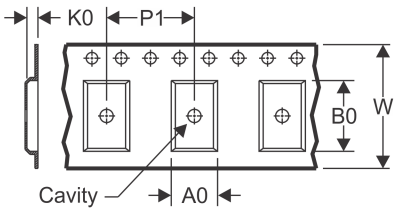
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

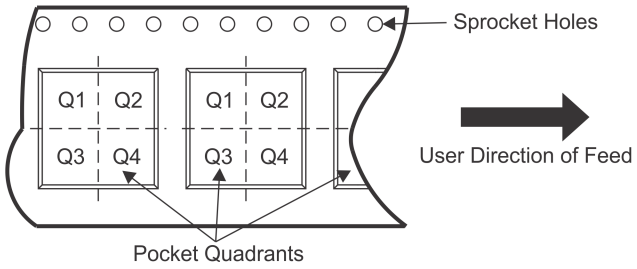


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

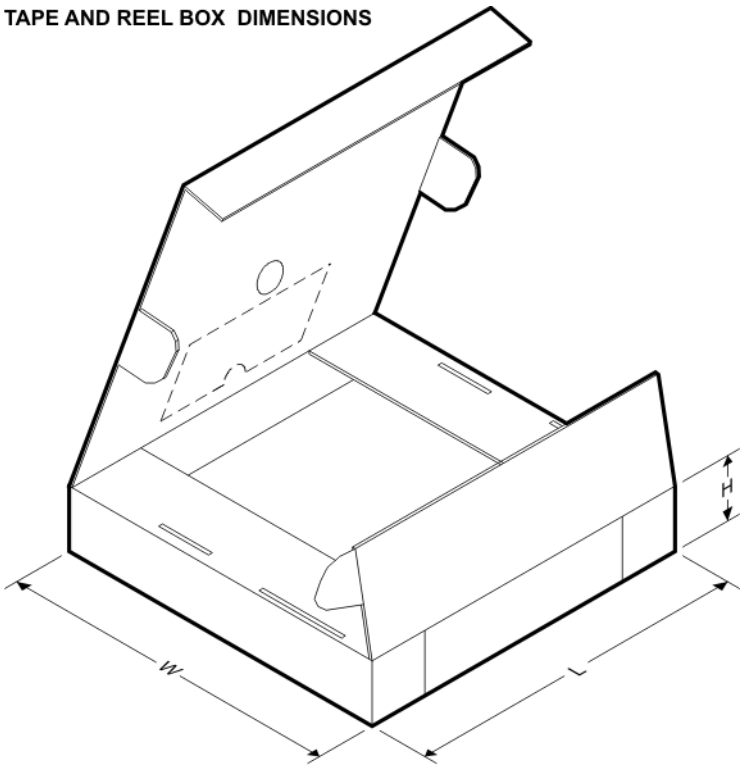
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25180NGUR	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

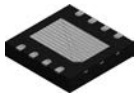
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25180NGUR	WSON	NGU	8	4500	367.0	367.0	38.0

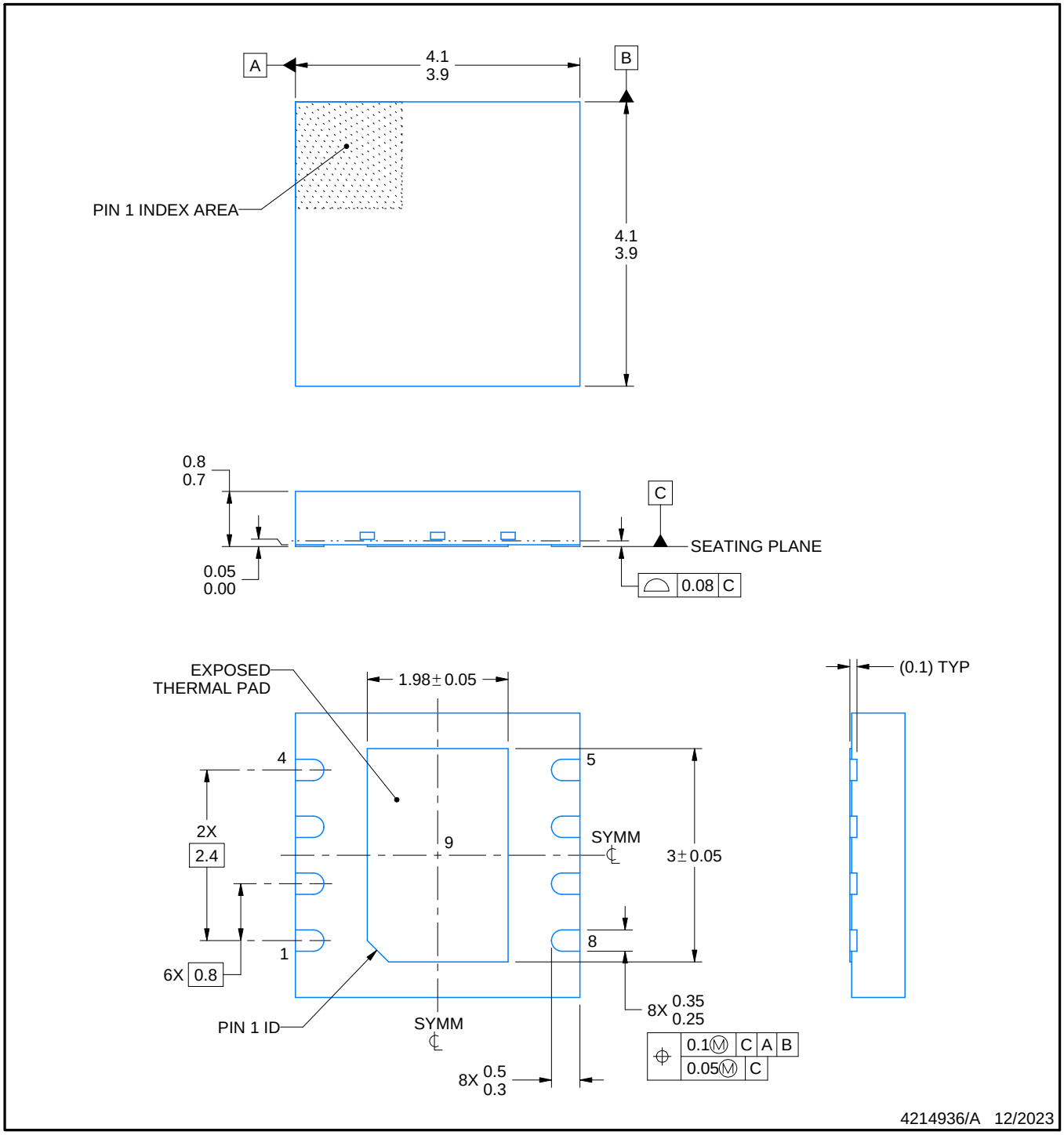
NGU0008B



PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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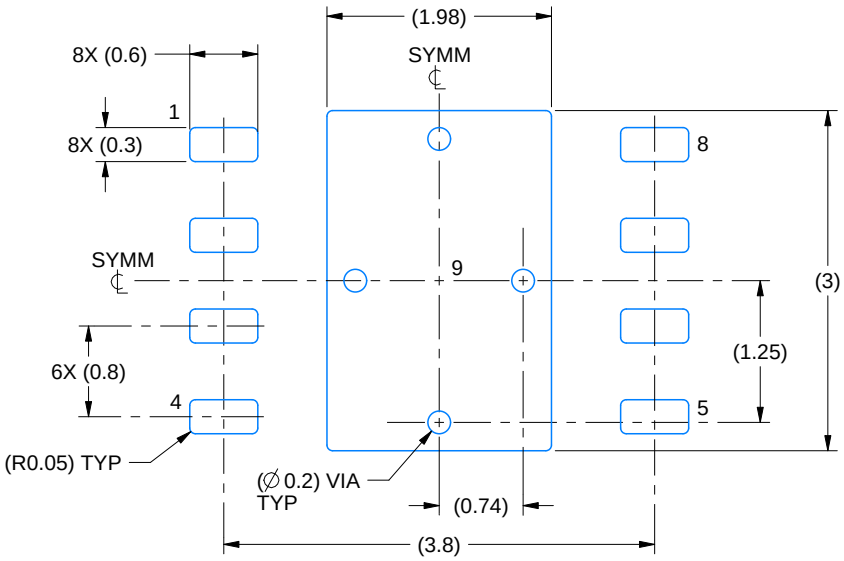
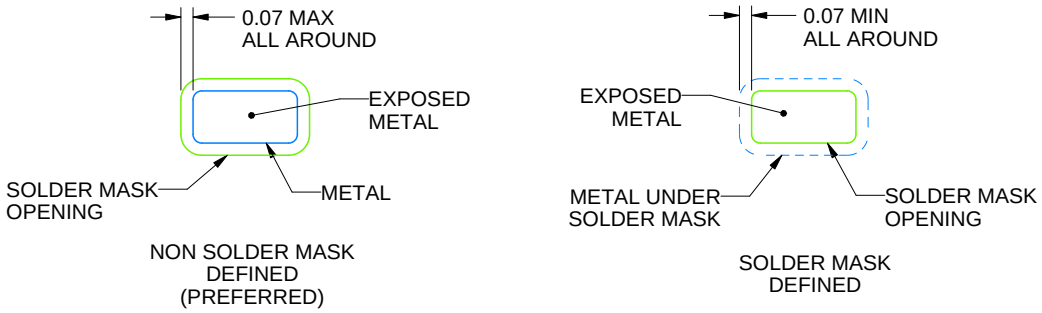


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

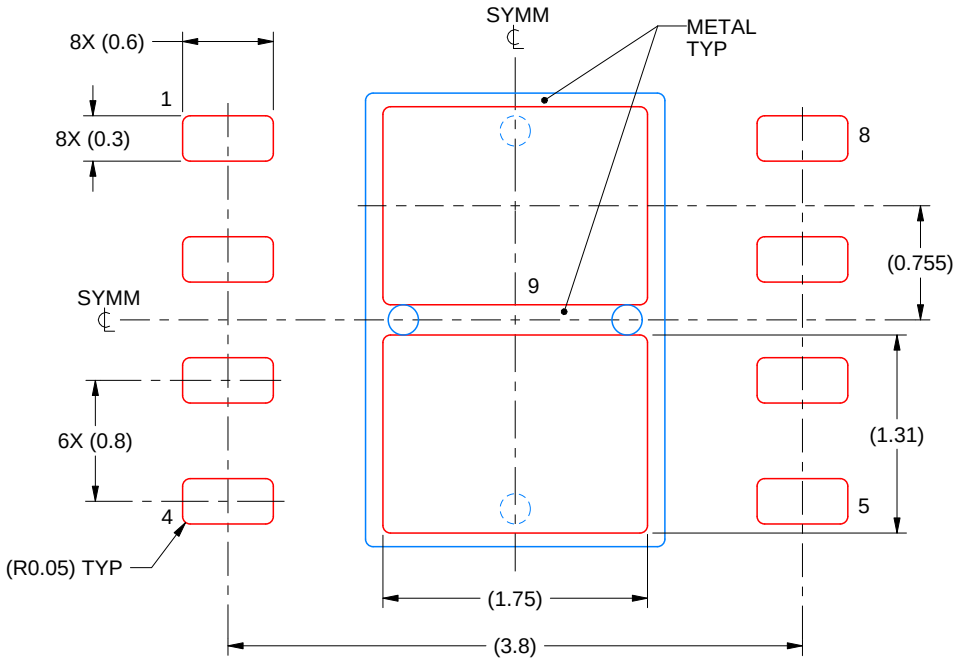


SOLDER MASK DETAILS

4214936/A 12/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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