

LM2623-Q1 ゲート付きオシレータ・ベースの車載用DC/DC昇圧コンバータ

1 特長

- 車載アプリケーション用にAEC-Q100認定済み:
 - デバイス温度グレード 1: -40°C ~ 125°C 周囲動作温度
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC4A
- 非常に広い負荷範囲で優れた効率を維持
- 非常に低い出力電圧リップル
- 最大2MHzのスイッチング周波数
- 0.9V ~ 14Vの動作電圧
- 1.1Vのスタートアップ電圧
- 出力電圧は1.24V ~ 14Vまで可変
- 0.17Ωの内蔵MOSFET
- 最高90%のレギュレータ効率
- 標準動作電流80μA (電源のV_{DD}ピンに対して)
- 低いシャットダウン電流(I_Q < 2.5μA)
- 4mmx4mmの熱的に強化されたWSONパッケージ・オプション

2 アプリケーション

- 車載用 カメラ
- 車載用 レーダー
- 車載用 GPS
- フラッシュ・メモリのプログラミング
- 白色LEDの駆動

3 概要

LM2623-Q1は、車載システム用の高効率の汎用昇圧型DC/DCスイッチング・レギュレータです。このデバイスは、0.9V ~ 14Vの入力電圧を受け付け、1.24V ~ 14Vのレギュレートされた出力電圧に変換します。

各種のアプリケーションに適合できるように、LM2623-Q1は設計者により出力電圧、動作周波数(300kHz ~ 2MHz)、デューティ・サイクル(17% ~ 90%)をプログラム可能で、最適な性能が得られます。選択された値は固定にも、入力電圧や入力と出力の電圧比に応じて変動するようにも設定できます。LM2623-Q1は非常に単純なオン/オフのレギュレーション・モードを使用し、広い動作範囲にわたって優れた効率と安定した動作を実現しています。このデバイスは通常、レギュレーションの限界に達したとき、スイッチング・サイクルをスキップしてレギュレートを行います(パルス幅変調(PFM))。

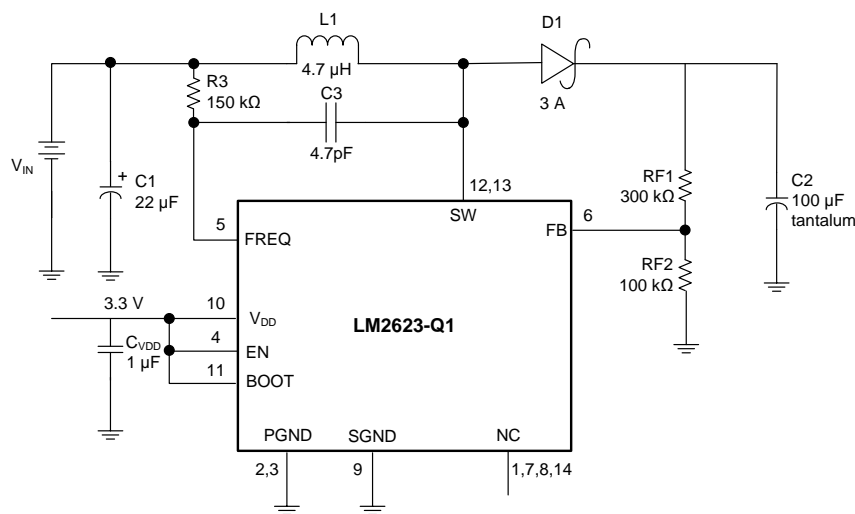
基板設計を最終的に確定する前に設計課題を解決する方法については、「[Non-Linear Effect](#)」および「[Choosing the Correct C3 Capacitor](#)」を参照してください。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
LM2623-Q1	WSON (14)	4.00mmx4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



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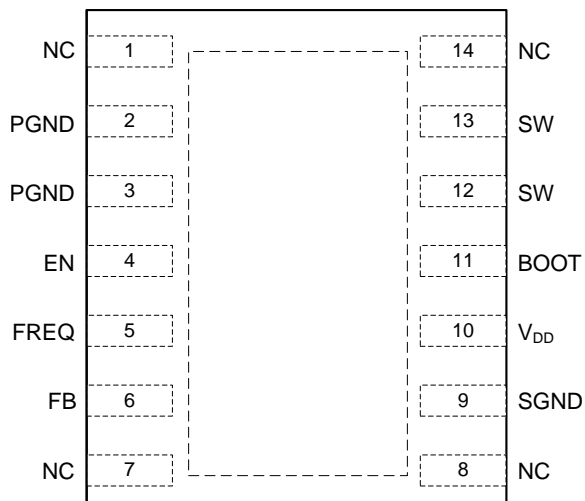
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年10月	*	初版

5 Pin Configuration and Functions

**NHL Package
14-Pin WSON
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No connect
2, 3	PGND	GND	Power ground (pins 2 and 3 <i>must</i> be shorted together)
4	EN	Digital	Active-low shutdown input
5	FREQ	Analog	Frequency adjust; connect an external resistor between this pin and a voltage source sets the switching frequency of the LM2623-Q1.
6	FB	Analog	Output voltage feedback
7	NC	—	No connect
8	NC	—	No connect
9	SGND	GND	Signal ground
10	V _{DD}	Power	Power supply for internal circuitry
11	BOOT	Analog	Bootstrap supply for the gate drive of internal MOSFET power switch
12, 13	SW	Analog	Drain of the internal MOSFET power switch (pins 12 and 13 <i>must</i> be shorted together)
14	NC	—	No connect
DAP	DAP	Thermal	Solder to board for enhanced thermal dissipation; must be electrically isolated/floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
Input pins	SW pin voltage	-0.5	14.5	V
	BOOT, VDD, EN, and FB pins	-0.5	10	V
	FREQ pin		100	μA
Power dissipation ($T_A = 25^\circ\text{C}$) ⁽³⁾			500	mW
T_{J_MAX} ⁽³⁾			150	°C
Storage temperature, T_{stg}		-55	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office / Distributors for availability and specifications.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{J_MAX} (maximum junction temperature), $R_{\theta JA}$ (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{D_MAX} = (T_{J_MAX} - T_A)/R_{\theta JA}$ or the number given in the Absolute Maximum Rating, whichever is lower.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	All pins except 12 and 13	±2000	V
		Pins 12 and 13	±1000	
	Charged device model (CDM), per AEC Q100-011		±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input pins	V_{DD} pin	3		5	V
	FB and EN pins	0		V_{DD}	V
	BOOT pin	0		10	V
Operating junction temperature range, T_J		-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM2623-Q1	UNIT
		NHL (WSON)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Limits apply for $T_J = 25^\circ\text{C}$ and $V_{DD} = V_{OUT} = 3.3\text{ V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
GENERAL						
V_{DD_ST}	Start-up supply voltage 25°C	$I_{LOAD} = 0\text{ mA}^{(1)}$		1.1	V	
V_{IN_OP}	Minimum operating supply voltage (once started)	$I_{LOAD} = 0\text{ mA}$		0.65	V	
V_{FB}	FB pin voltage			1.24	V	
		-40°C to 85°C		1.2028		1.2772
		-40°C to 125°C		1.2028		1.2772
V_{OUT_MAX}	Maximum output voltage			14	V	
η	Efficiency	$V_{IN} = 3.6\text{ V}; V_{OUT} = 5\text{ V}, I_{LOAD} = 500\text{ mA}$		87%		
		$V_{IN} = 2.5\text{ V}; V_{OUT} = 3.3\text{ V}, I_{LOAD} = 200\text{ mA}$		87%		
D	Switch duty cycle			17%		
I_{DD}	Operating quiescent current ⁽²⁾	FB pin > 1.3 V, EN pin at V_{DD}		80	μA	
		FB pin > 1.3 V, EN pin at V_{DD} , -40°C to 85°C		110		
		FB pin > 1.3 V, EN pin at V_{DD} , -40°C to 125°C		110		
I_{SD}	Shutdown quiescent current ⁽³⁾	V_{DD} , BOOT, and SW pins at 5 V, EN pin < 200 mV		0.01	μA	
		V_{DD} , BOOT, and SW pins at 5 V, EN pin < 200 mV, -40°C to 85°C		2.5		
		V_{DD} , BOOT, and SW pins at 5 V, EN pin < 200 mV, -40°C to 125°C		2.5		
I_{CL}	Switch peak current limit	2.2	2.85		A	
R_{DSON}	MOSFET switch on resistance			0.17	Ω	
		-40°C to 85°C		0.26		
		-40°C to 125°		0.26		
ENABLE SECTION						
V_{EN_LO}	EN pin voltage low ⁽⁴⁾	-40°C to 85°C		$0.15 V_{DD}$	V	
		-40°C to 125°C		$0.15 V_{DD}$		
V_{EN_HI}	EN pin voltage high ⁽⁴⁾	-40°C to 85°C		$0.7 V_{DD}$	V	
		-40°C to 125°C		$0.7 V_{DD}$		

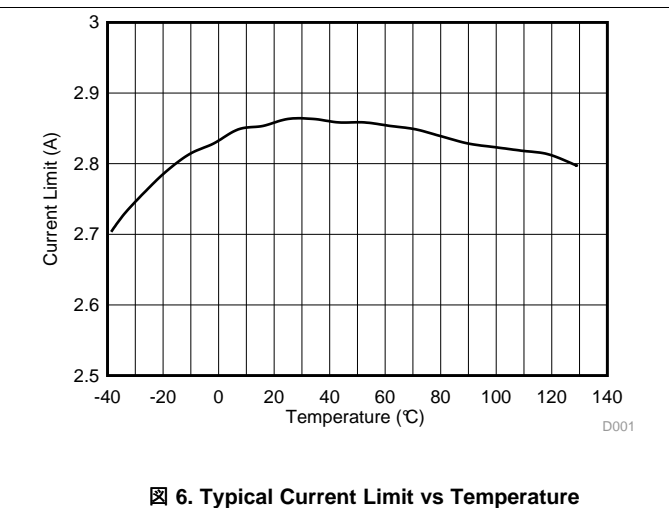
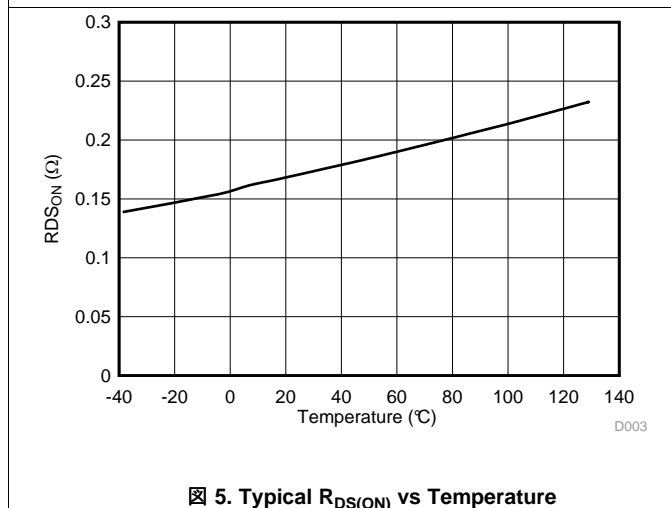
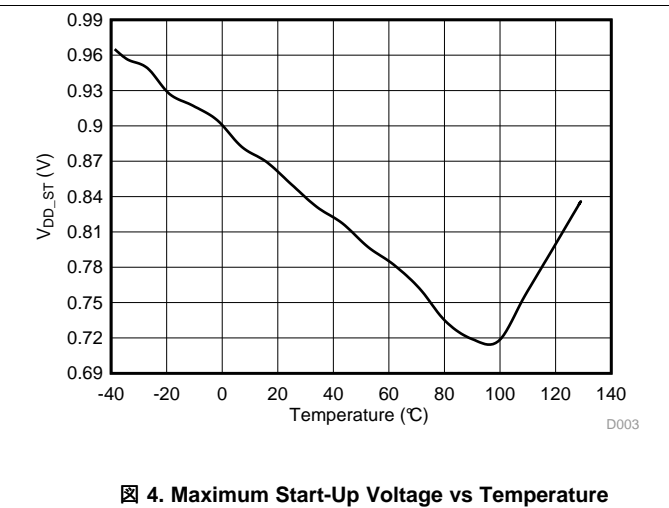
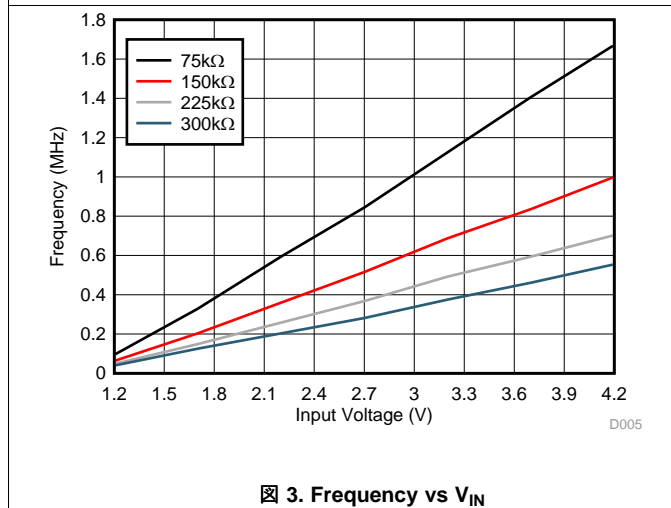
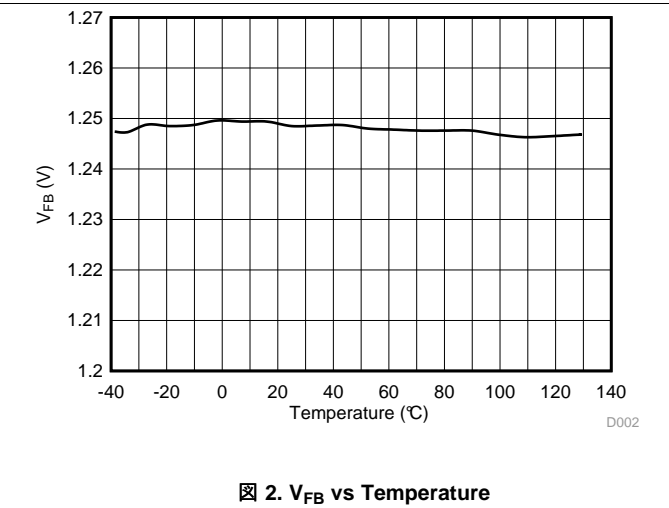
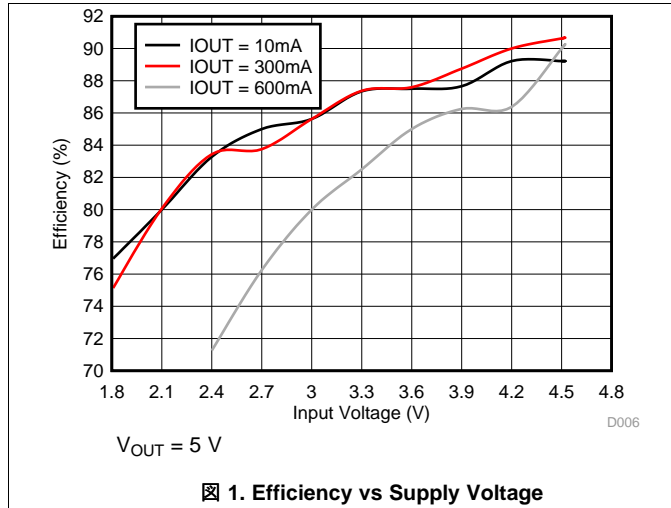
(1) V_{DD} tied to BOOT and EN pins. Frequency pin tied to V_{DD} through 121-K Ω resistor. $V_{DD_ST} = V_{DD}$ when start-up occurs. V_{IN} is $V_{DD} + D1$ voltage (usually 10 mV to 50 mV at start-up).

(2) This is the current into the V_{DD} pin.

(3) This is the total current into pins V_{DD} , BOOT, SW, and FREQ.

(4) When the EN pin is below V_{EN_LO} , the regulator is shut down; when it is above V_{EN_HI} , the regulator is operating.

6.6 Typical Characteristics



Typical Characteristics (continued)

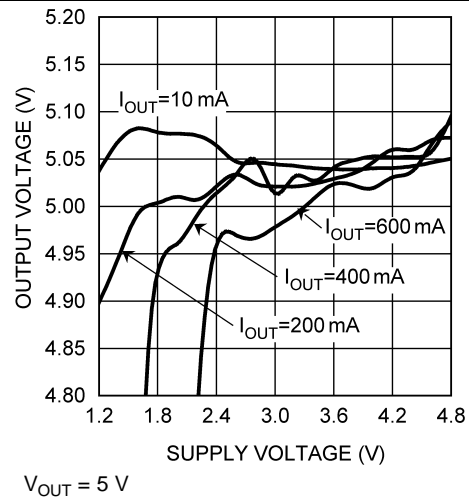


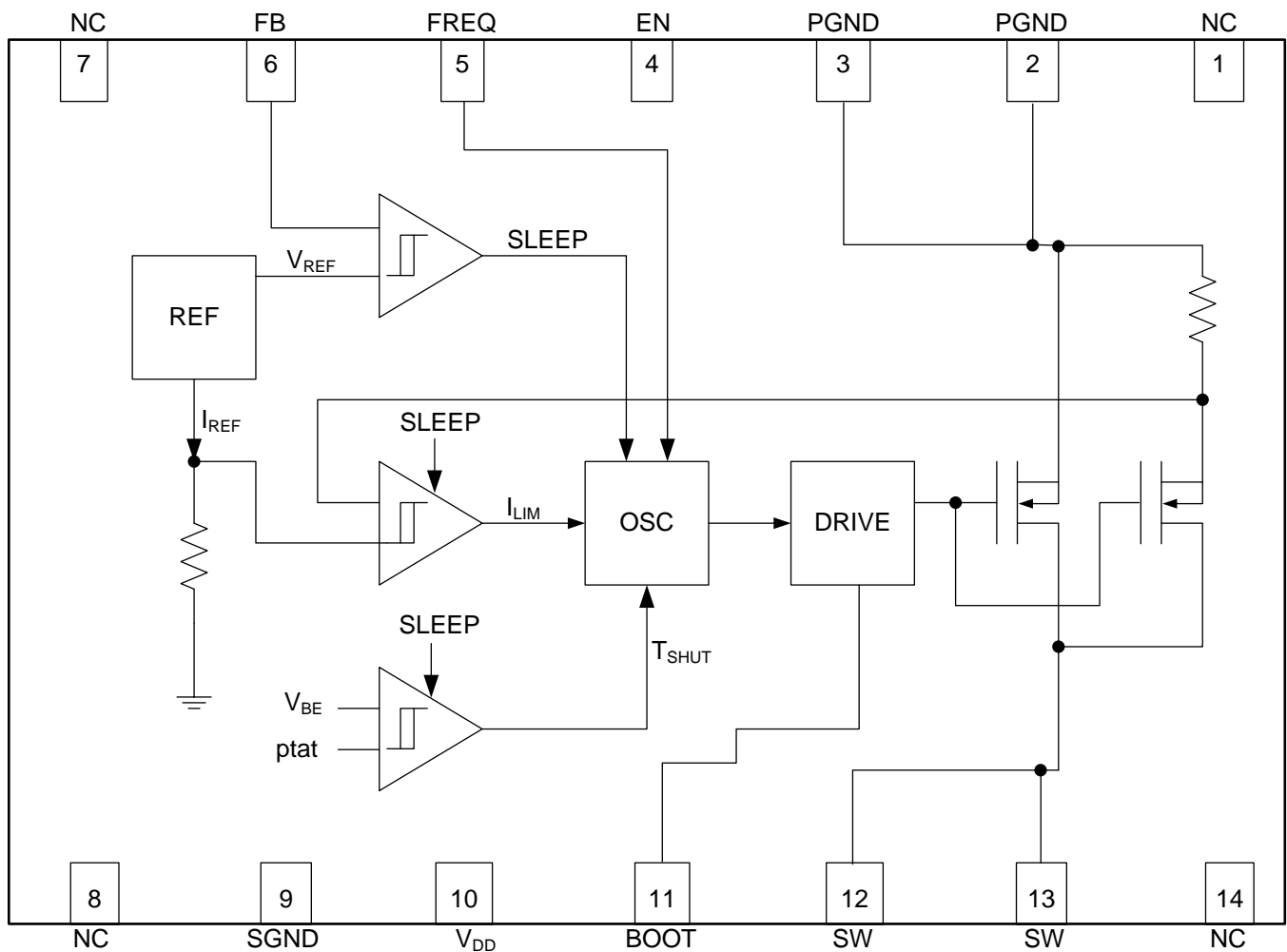
Figure 7. Output Voltage vs Supply Voltage

7 Detailed Description

7.1 Overview

The LM2623-Q1 device is designed to provide step-up DC-DC voltage regulation in battery-powered and low-input voltage systems. The device combines a step-up switching regulator, N-channel power MOSFET, built-in current limit, thermal limit, and voltage reference in a single 14-pin WSON package (see [Functional Block Diagram](#)). The switching DC-DC regulator boosts an input voltage between 0.9 V and 14 V to a regulated output voltage between 1.24 V and 14 V. The LM2623-Q1 starts from a low 1.1-V input and remains operational down to below 0.9 V. A high-efficiency gated-oscillator topology offers an output of up to 2 A at low step-up ratios.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Gated Oscillator Control Scheme

The on/off regulation mode of the LM2623-Q1, along with its ultra-low quiescent current, results in good efficiency over a very wide load range. The internal oscillator frequency can be programmed using an external resistor to be constant or vary with the battery voltage. Adding a capacitor to program the frequency allows the designer to adjust the duty cycle and optimize it for the application. Adding a resistor in addition to the capacitor allows the duty cycle to dynamically compensate for changes to the input/output voltage ratio. This is called a *ratio-adaptive gated-oscillator circuit*. See the [Typical Application](#) for a sample application circuit. Using the correct RC components to adjust the oscillator allows the device to run with low ripple and high efficiency over a wide range of loads and input/output voltages.

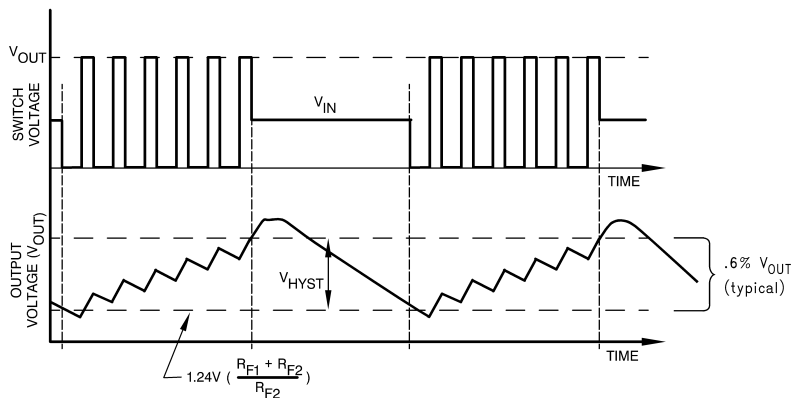


图 8. Typical Step-Up Regulator Waveforms

7.3.2 Cycle-To-Cycle PFM

When the load does not vary over a wide range, ratio adaptive circuit techniques can be used to achieve cycle to cycle PFM regulation and lower ripple (or smaller output capacitors). The key to success is matching the duty cycle of the circuit closely to what is required by the input-to-output voltage ratio. This ratio then must be dynamically adjusted for input voltage changes (usually caused by batteries running down). The chosen ratio must allow most of the energy in each switching cycle to be delivered to the load and only a small amount to be stored. When the regulation limit is reached, the overshoot is small, and the system settles at an equilibrium point where it adjusts the off time in each switching cycle to meet the current requirements of the load. The off-time adjustment is done by exceeding the regulation limit during each switching cycle and waiting until the voltage drops below the limit again to start the next switching cycle. The current in the coil never goes to zero like it frequently does in the hysteretic operating mode of circuits with wide load variations or duty cycles that are not matched to the input/output voltage ratio. Optimizing the duty cycle for a given set of input/output voltages conditions can be done by referencing the circuit values in [AN-1221 LM2623 General Purpose, Boost Converter Circuit](#).

7.3.3 Shutdown

The LM2623-Q1 features a shutdown mode that reduces the quiescent current to less than an ensured 2.5 μA over temperature. This extends the life of the battery in battery-powered applications. During shutdown, all feedback and control circuitry is turned off. The output voltage of the regulator drops to one diode drop below the input voltage. Entry into the shutdown mode is controlled by the active-low logic input pin EN (pin 4). When the logic input to this pin is pulled below 0.15 V_{DD} , the device goes into shutdown mode. The logic input to this pin must be above 0.7 V_{DD} for the device to work in normal step-up mode. If EN is pulled above 0.7 V_{DD} the SW pin switches continuously for experimentally tested 5 μs period, regardless of the output voltage. Once this time period is expired the feedback and gated oscillator scheme take over to regulate the output voltage.

Feature Description (continued)

7.3.4 Internal Current Limit and Thermal Protection

An internal cycle-by-cycle current limit serves as a protection feature. This is set high enough (2.85 A typical, approximately 4 A maximum) so it does not come into effect during normal operating conditions. An internal thermal protection circuit disables the MOSFET power switch when the junction temperature (T_J) exceeds about 160°C. The switch is re-enabled when T_J drops below approximately 135°C.

7.4 Device Functional Modes

7.4.1 Pulse Frequency Modulation (PFM)

Pulse frequency modulation is typically accomplished by switching continuously until the voltage limit is reached and skipping cycles after that to just maintain it. This results in a somewhat hysteretic mode of operation. The coil stores more energy each cycle as the current ramps up to high levels. When the voltage limit is reached, the system usually overshoots to a higher voltage than required, due to the stored energy in the coil (see [Figure 8](#)). The system also undershoots somewhat when it starts switching again because it has depleted all the stored energy in the coil and must store more energy to reach equilibrium with the load. Larger output capacitors and smaller inductors reduce the ripple in these situations. The frequency being filtered, however, is not the basic switching frequency. It is a lower frequency determined by the load, the input/output voltage and the circuit parameters. This mode of operation is useful in situations where the load variation is significant. Power-managed computer systems, for instance, may vary from zero to full load while the system is on, and this is usually the preferred regulation mode for such systems.

7.4.2 Low Voltage Start-Up

The LM2623-Q1 can start up from voltages as low as 1.1 V. On start-up, the control circuitry switches the N-channel MOSFET continuously until the output reaches 3 V. After this output voltage is reached, the normal step-up regulator feedback and gated oscillator control scheme take over. Once the device is in regulation, it can operate down to 0.9 V input, because the internal power for the device can be boot-strapped from the output using the V_{DD} pin.

8 Applications and Implementation

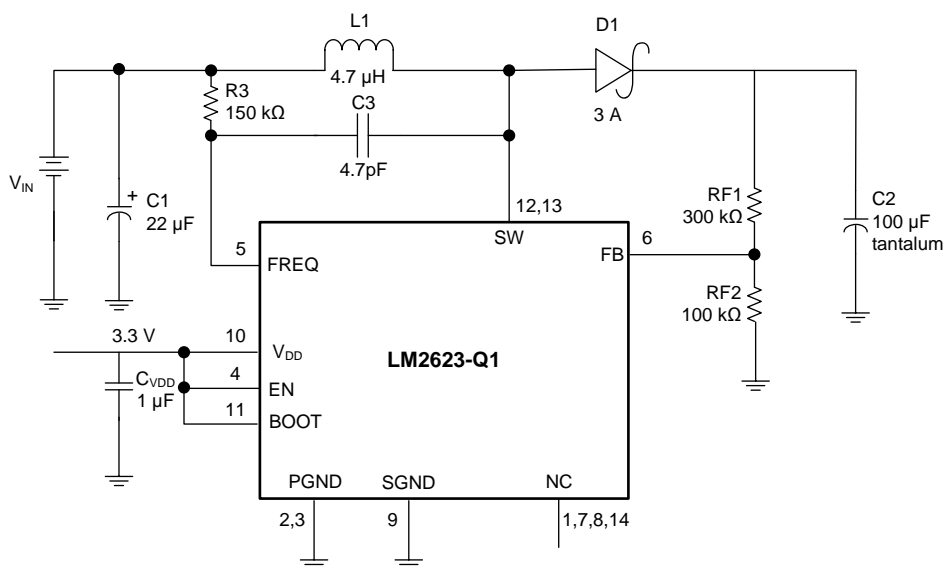
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2623-Q1 is suitable for automotive applications, and supports shutdown mode for low quiescent current when EN input is low. Output voltage level can be adjusted by changing feedback resistor divider values from 1.24-V to 14-V range. The maximum switching frequency is 2MHz.

8.2 Typical Application



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图 9. LM2623-Q1 Typical Application

8.2.1 Design Requirements

The LM2623-Q1 allows the designer to vary output voltage, operating frequency and duty cycle to optimize device performance (see [Detailed Design Procedure](#) for details).

For typical boost-converter applications, use the parameters listed in 表 1.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	0.9 V to 14 V
Output voltage	1.24 V to 14 V (adjustable)
Output current	2 A (maximum)

8.2.2 Detailed Design Procedure

8.2.2.1 Non-Linear Effect

The LM2623-Q1 takes advantage of a non-linear effect, allowing for the duty cycle to be programmable. C3 in [Figure 9](#) allows for the duty cycle to be programmable.

8.2.2.2 Choosing the Correct C3 Capacitor

The duty cycle of the internal oscillator is programmable with the C3 capacitor. Choosing the correct C3 capacitor to obtain the appropriate duty cycle for a particular application circuit is a trial-and-error process. The non-linear effect that C3 produces is dependent on the input voltage and output voltage values. The correct C3 capacitor for specific input and output voltage values cannot be calculated. Choosing the correct C3 capacitance is best done by trial and error, in conjunction with the checking of the inductor peak current to make sure it is not too close to the current limit of the device. As the C3 capacitor value increases, so does the duty cycle; conversely, as the C3 capacitor value decreases, the duty cycle decreases. An incorrect choice of the C3 capacitor can result in the device prematurely tripping the current limit and/or double pulsing, which could lead to the output voltage not being stable. Optimizing the duty cycle for a given set of input/output voltages conditions can be done by referencing the component values in [AN-1221 LM2623 General Purpose, Boost Converter Circuit](#).

8.2.2.3 Setting the Output Voltage

The output voltage of the step-up regulator can be set by connecting a feedback resistive divider made of R_{F1} and R_{F2}. The resistor values are selected as follows:

$$R_{F1} = R_{F2} \times [(V_{OUT} / 1.24) - 1] \quad (1)$$

A value of 50 kΩ to 100 kΩ is suggested for R_{F2}. R_{F1} can be selected using [Equation 1](#).

8.2.2.4 V_{DD} Supply

The V_{DD} supply must be between 3 V to 5 V for the LM2623-Q1 device. This voltage can be bootstrapped from a much lower input voltage by simply connecting the V_{DD} pin to V_{OUT}. In the event that the V_{DD} supply voltage is not a low-ripple voltage source (less than 200 mV), it may be advisable to use an RC filter to clean it up. Excessive ripple on V_{DD} may reduce the efficiency.

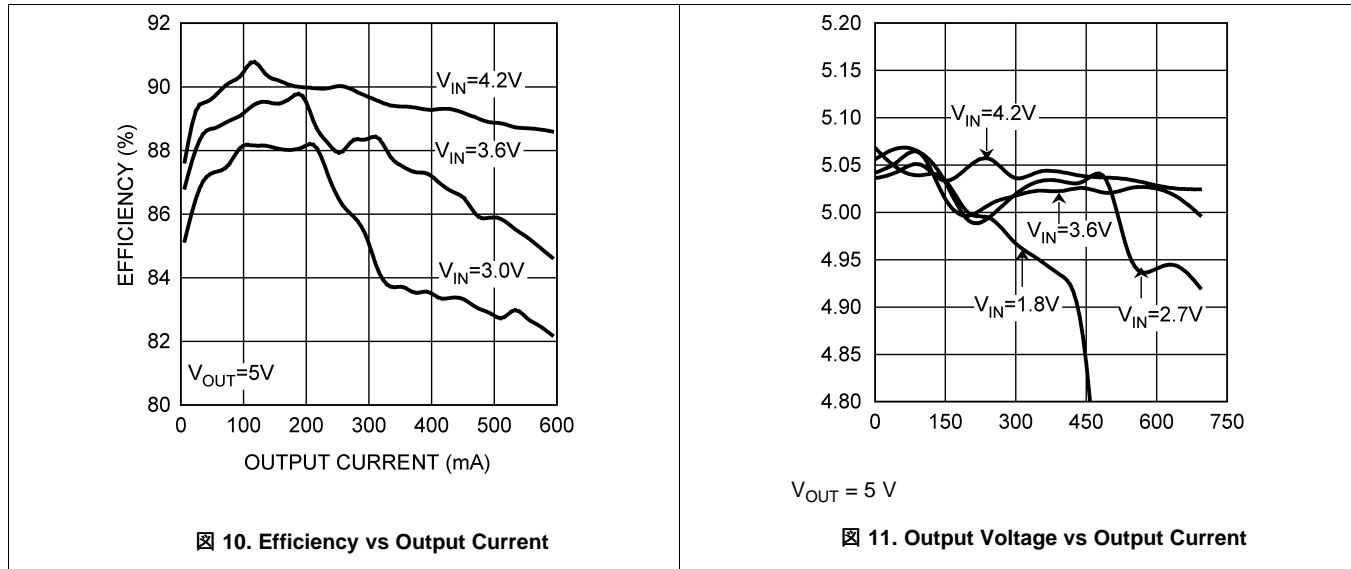
8.2.2.5 Setting the Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor (R3) connected between V_{IN} and the FREQ pin. See [Figure 3](#) in the [Typical Characteristics](#) for choosing the R3 value to achieve the desired switching frequency. A high switching frequency allows the use of very small surface mount inductors and capacitors and results in a very small solution size. TI recommends a switching frequency between 300 kHz and 2 MHz.

8.2.2.6 Output Diode Selection

Use a Schottky diode for the output diode. The forward current rating of the diode must be higher than the peak input current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

8.2.3 Application Curves




9 Power Supply Recommendations

The LM2623-Q1 can start up from voltages as low as 1.1 V. On start-up, the control circuitry switches the N-channel MOSFET continuously until the output reaches 3 V. After this output voltage is reached, the normal step-up regulator feedback and gated oscillator control scheme take over. Once the device is in regulation, it can operate down to below 0.9 V input, because the internal power for the device can be boot-strapped from the output using the V_{DD} pin.

10 Layout

10.1 Layout Guidelines

 **12** follows proper layout guidelines — use as a guide for laying out the LM2623-Q1 circuit. The LM2623-Q1 inductive boost converter sees a high switched voltage at the SW pin and a step current through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling ($I = C \times dV/dt$). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW and BOOST pins due to parasitic inductance in the step current conducting path ($V = L \times di/dt$). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise.

[Boost Output Capacitor Placement](#), [Schottky Diode Placement](#), and [Boost Input / \$V_{DD}\$ Capacitor Placement](#) detail the main (layout sensitive) areas of the LM2623-Q1 inductive boost converter in order of decreasing importance:

10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path, it experiences a high-current step from 0 A to the peak inductor current each time the switch turns off, and the Schottky diode turns on. Any inductance along this series path from the diodes cathode, through C_{OUT} , and back into the LM2623-Q1 GND pin contributes to voltage spikes at SW. These spikes can potentially overvoltage the SW and BOOST pins, or feed through to GND. To avoid this, C_{OUT+} must be connected as close as possible to the cathode of the Schottky diode, and C_{OUT-} must be connected as close as possible to the LM2623-Q1 GND bumps. The best placement for C_{OUT} is on the same layer as the LM2623-Q1 to avoid any vias that can add excessive series inductance.

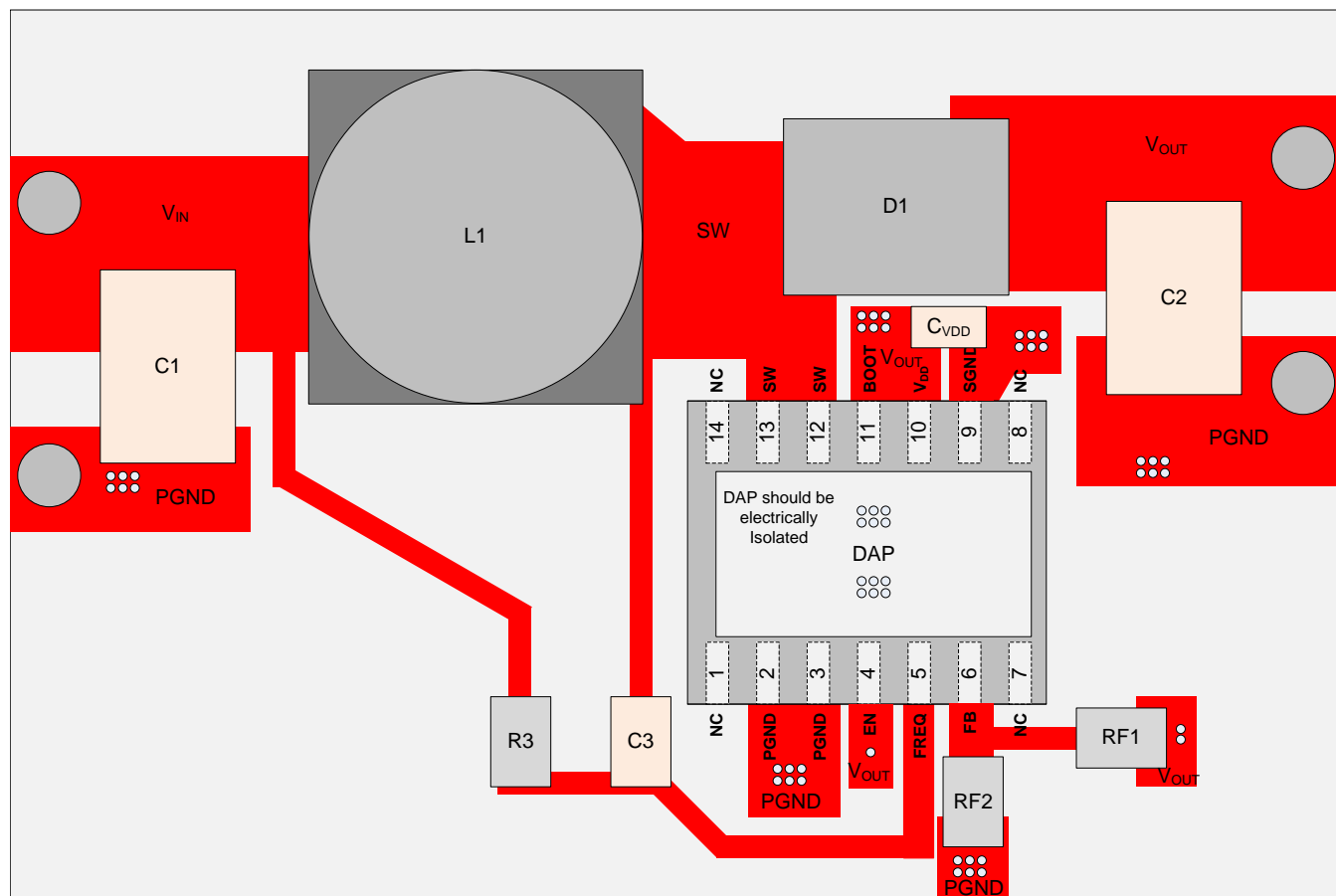
10.1.2 Schottky Diode Placement

In the LM2623-Q1 device boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode detects a high-current step from 0 A to the peak inductor current each time the switch turns off, and the diode turns on. Any inductance in series with the diode causes a voltage spike at SW. This can potentially overvoltage the SW pin, or feed through to VOUT and through the output capacitor, into GND. Connecting the anode of the diode as close as possible to the SW pin, and connecting the cathode of the diode as close as possible to C_{OUT} reduces the parasitic inductance and minimizes these voltage spikes.

10.1.3 Boost Input / V_{DD} Capacitor Placement

The LM2623-Q1 input capacitor filters the inductor current ripple and the internal MOSFET driver currents. The inductor current ripple can add input voltage ripple due to any series resistance in the input power path. The MOSFET driver currents can add voltage spikes on the input due to the inductance in series with the V_{IN}/V_{DD} and the input capacitor. Place the input capacitor close to the inductor and minimize the current-loop area. Close placement of the V_{DD} capacitor to the V_{DD} and GND pins is critical because any series inductance can create voltage spikes that could appear on the V_{IN}/V_{DD} supply line.

10.2 Layout Example



12. LM2623-Q1 Layout Example

10.3 WSON Package Devices

The LM2623-Q1 is offered in the 14-pin WSON surface mount package — for details of the thermal performance as well as mounting and soldering specifications, refer to [Leadless Leadframe Package \(LLP\)](#).

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- 『AN-1187 リードレス・リードフレーム・パッケージ(LLP)』
- 『AN-1221 LM2623汎用昇圧コンバータ回路』
- 『AN-1258 LM2623昇圧コンバータ - 単純な電源』

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2623QNHLRQ1	ACTIVE	WSON	NHL	14	4500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2623Q1	Samples
LM2623QNHLTQ1	ACTIVE	WSON	NHL	14	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2623Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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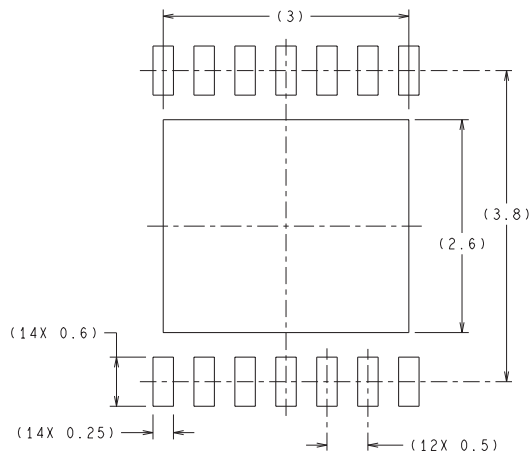
OTHER QUALIFIED VERSIONS OF LM2623-Q1 :

- Catalog : [LM2623](#)

NOTE: Qualified Version Definitions:

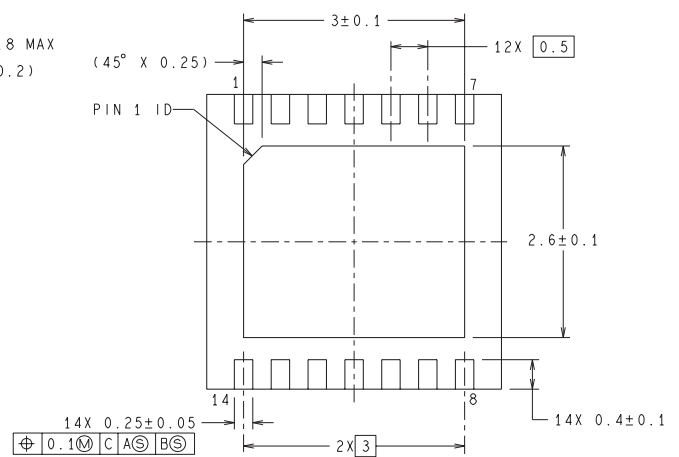
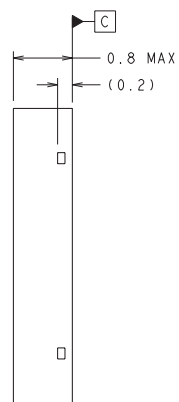
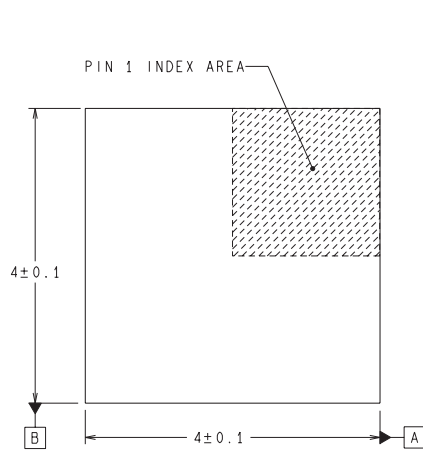
- Catalog - TI's standard catalog product

NHL0014B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDA14B (Rev A)

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