LM2733 SOT-23 パッケージ、40V FET スイッチ内蔵 0.6/1.6MHz 昇圧型コンバータ

1 特長

- 40V の DMOS FET スイッチ
- 1.6MHz (「X」)、0.6MHz (「Y」) のスイッチング周波数
- 低 $R_{DS(ON)}$ の DMOS FET
- 最大 1A のスイッチング電流
- 広い入力電圧範囲：2.7V～14V
- 低いシャットダウン時電流：1μA 未満
- 5 ピン SOT-23 パッケージ
- 小型コンデンサおよびインダクタを使用
- サイクル単位の電流制限
- 内部補償

2 アプリケーション

- 白色 LED 用電流源
- PDA、パームトップ・コンピュータ
- デジタル・カメラ
- 携帯電話、ゲーム機
- ローカル昇圧レギュレータ

3 概要

LM2733 スイッチング・レギュレータは、1.6MHz (「X」オプション) と 600kHz (「Y」オプション) の固定周波数で動作する電流モード昇圧型コンバータです。

内蔵の 1A スイッチの電力損失を最小限にすることで可能になった SOT-23 パッケージの使用と、小型インダクタおよびコンデンサの使用により、業界で最高の電力密度を実現しています。これらのソリューションは 40V のスイッチを内蔵しているため、16V 以上の電圧への昇圧に理想的です。

これらの製品は、静止電流の低減とバッテリー駆動時間の延長に使用できるロジック・レベルのシャットダウン・ピンを備えています。

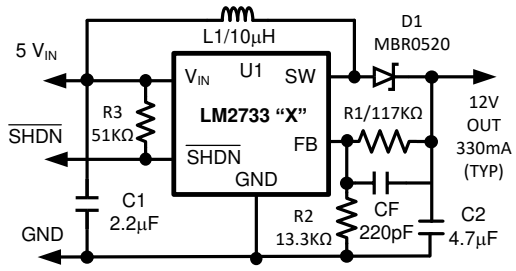
サイクル単位の電流制限とサーマル・シャットダウンによる保護機能を備えています。補償機能を内蔵しているため、設計が簡単であり、部品数を減らせます。

製品情報(1)

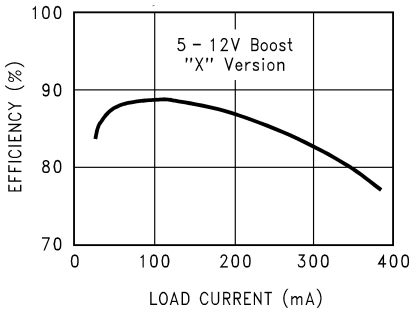
型番	パッケージ	本体サイズ(公称)
LM2733	SOT-23 (5)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



効率と負荷電流との関係



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (December 2014) から **Revision G** に変更 **Page**

- コネクタの配線の誤記を訂正するために「代表的なアプリケーション回路」の図を 変更 ... 1

Revision E (April 2013) から **Revision F** に変更 **Page**

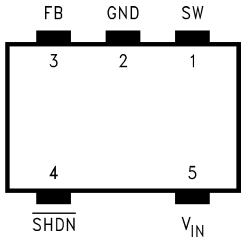
- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1

Revision D (April 2013) から **Revision E** に変更 **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 11

5 Pin Configuration and Functions

5-Pin DBV
SOT-23 Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1	O	Drain of the internal FET switch.
GND	2	GND	Analog and power ground.
FB	3	I	Feedback point that connects to external resistive divider.
$\overline{SHDN}$	4	I	Shutdown control input. Connect to V_{IN} if this feature is not used.
V_{IN}	5	I	Analog and power input.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

	MIN	MAX	UNIT
Input supply voltage (VIN)	−0.4	14.5	V
FB pin voltage	−0.4	6	V
SW pin voltage	−0.4	40	V
$\overline{SHDN}$ pin voltage	−0.4	V_{IN} + 0.3	V
Power dissipation(3)	Internally Limited		
Lead temperature (soldering, 5 sec.)		300	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of the limits set forth under the operating ratings which specify the intended range of operating conditions.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation which can be safely dissipated for any application is a function of the maximum junction temperature, $T_J(MAX)$ = 125°C, the junction-to-ambient thermal resistance for the SOT-23 package, $R_{\theta J\text{-}A}$ = 210°C/W, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature for designs using this device can be calculated using the formula: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{265}$ If power dissipation exceeds the maximum specified above, the internal thermal protection circuitry protects the device by reducing the output voltage as required to maintain a safe junction temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input supply voltage (VIN)	2.7	14	V
$\overline{SHDN}$ pin voltage	0	V_{IN}	V
Junction temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2733 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*SPRA953 application report.

6.5 Electrical Characteristics

Unless otherwise specified: V_{IN} = 5 V, V_{SHDN} = 5 V, I_L = 0 A, T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{IN}	Input voltage	−40°C ≤ T_J ≤ +125°C	2.7		14	V
I_{SW}	Switch current limit	See[3]	1	1.5		A
R_{DS}(ON)	Switch ON resistance	I_{SW} = 100 mA		500	650	mΩ
$SHDN_{TH}$	Shutdown threshold	Device ON, −40°C ≤ T_J ≤ +125°C	1.5			V
		Device OFF, −40°C ≤ T_J ≤ +125°C			0.50	
I_{SHDN}	Shutdown pin bias current	V_{SHDN} = 0		0		µA
		V_{SHDN} = 5 V		0		
		V_{SHDN} = 5 V, −40°C ≤ T_J ≤ +125°C			2	
V_{FB}	Feedback pin reference voltage	V_{IN} = 3 V		1.230		V
		V_{IN} = 3 V, −40°C ≤ T_J ≤ +125°C	1.205		1.255	
I_{FB}	Feedback pin bias current	V_{FB} = 1.23 V		60		nA
I_Q	Quiescent current	V_{SHDN} = 5 V, Switching "X"		2.1		mA
		V_{SHDN} = 5 V, Switching "X", −40°C ≤ T_J ≤ +125°C			3	
		V_{SHDN} = 5 V, Switching "Y"		1.1		
		V_{SHDN} = 5 V, Switching "Y", −40°C ≤ T_J ≤ +125°C			2	
		V_{SHDN} = 5 V, Not Switching		400		µA
		V_{SHDN} = 5 V, Not Switching, −40°C ≤ T_J ≤ +125°C			500	
		V_{SHDN} = 0		0.024	1	
$\Delta V_{FB}/\Delta V_{IN}$	FB voltage line regulation	2.7 V ≤ V_{IN} ≤ 14 V		0.02		%/V

(1) Limits are specified by testing, statistical correlation, or design.
(2) Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.
(3) Switch current limit is dependent on duty cycle (see *Typical Characteristics*). Limits shown are for duty cycles ≤ 50%.

Electrical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, V_{SHDN} = 5 V, I_L = 0 A, T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
F_{SW}	Switching frequency	"X" Option		1.6		MHz
		"X" Option, −40°C ≤ T_J ≤ +125°C	1.15		1.85	
		"Y" Option		0.60		
		"Y" Option, −40°C ≤ T_J ≤ +125°C	0.40		0.8	
D_{MAX}	Maximum duty cycle	"X" Option		93%		
		"X" Option, −40°C ≤ T_J ≤ +125°C	87%			
		"Y" Option		96%		
		"Y" Option, −40°C ≤ T_J ≤ +125°C	93%			
I_L	Switch leakage	Not Switching V_{SW} = 5 V			1	µA

6.6 Typical Characteristics

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin is tied to V_{IN}.

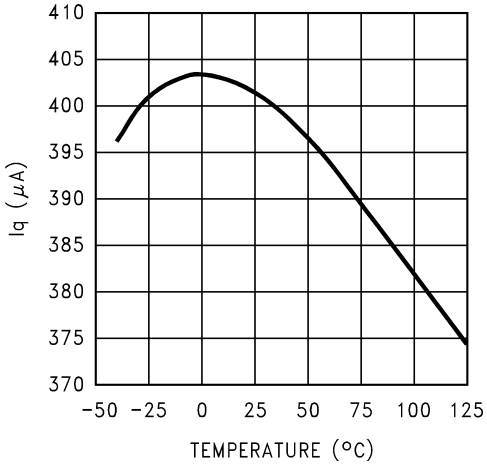


Figure 1. Iq V_{IN} (Active) vs Temperature - "X"

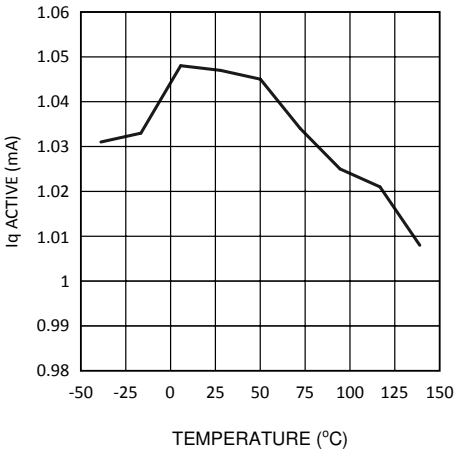


Figure 2. Iq V_{IN} (Active) vs Temperature - "Y"

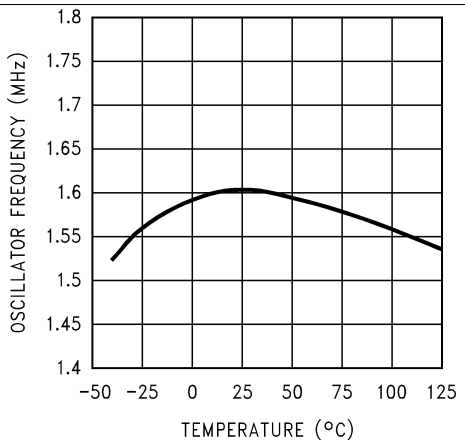


Figure 3. Oscillator Frequency vs Temperature - "X"

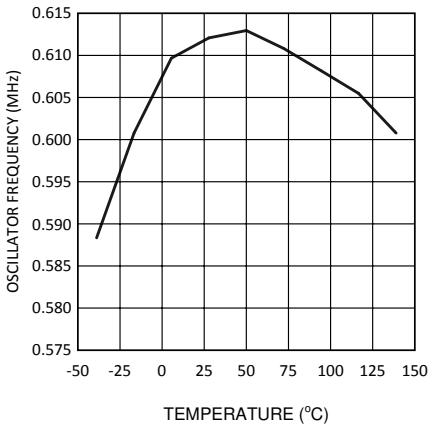


Figure 4. Oscillator Frequency vs Temperature - "Y"

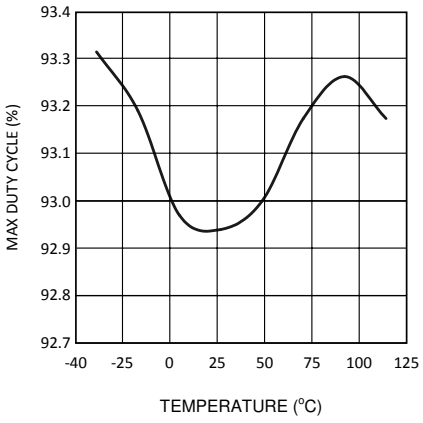


Figure 5. Max. Duty Cycle vs Temperature - "X"

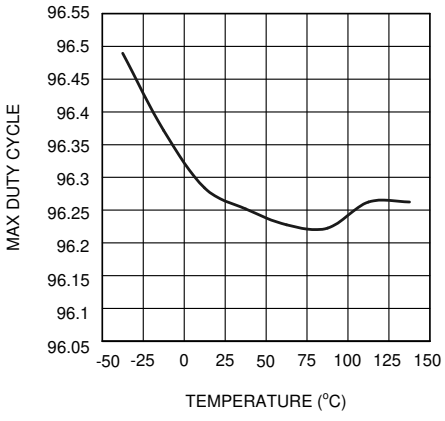


Figure 6. Max. Duty Cycle vs Temperature - "Y"

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin is tied to V_{IN}.

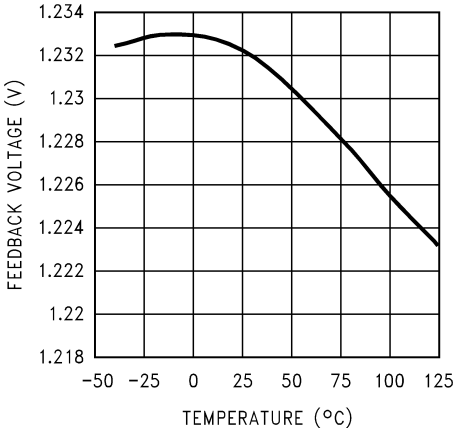


Figure 7. Feedback Voltage vs Temperature

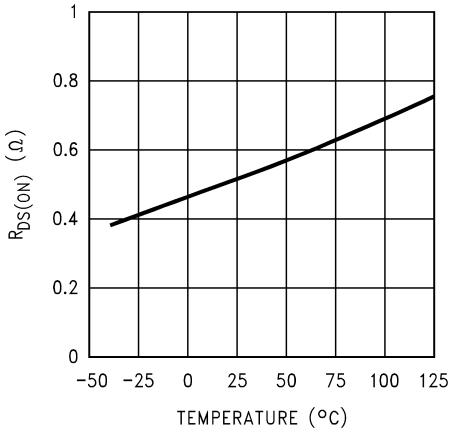


Figure 8. R_{DS}(ON) vs Temperature

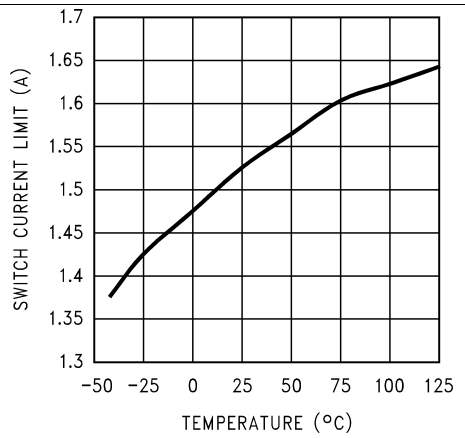


Figure 9. Current Limit vs Temperature

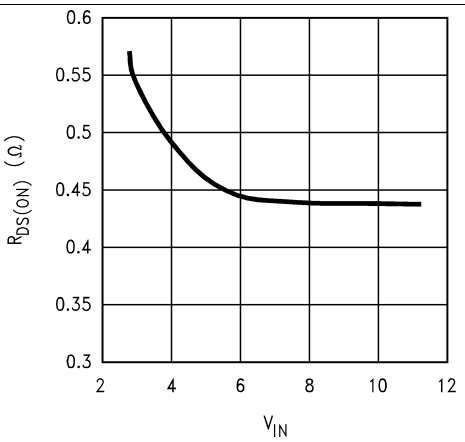


Figure 10. $R_{DS(ON)}$ vs V_{IN}

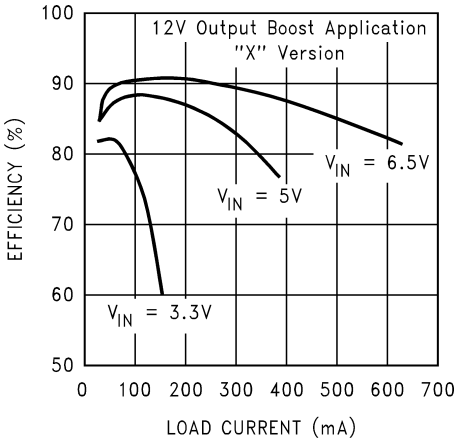


Figure 11. Efficiency vs Load Current (V_{OUT} = 12 V) - "X"

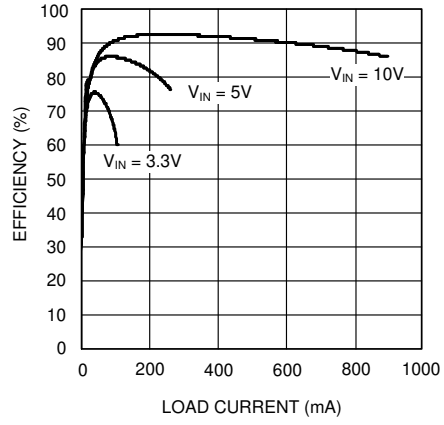


Figure 12. Efficiency vs Load Current (V_{OUT} = 15 V) - "X"

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin is tied to V_{IN}.

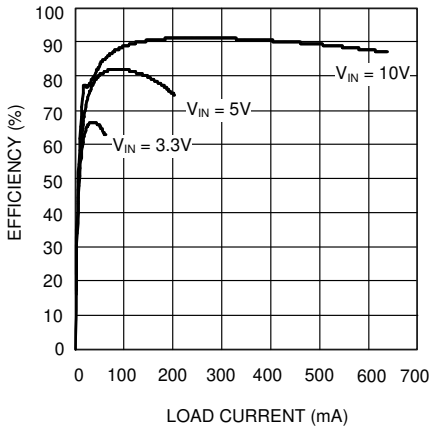


Figure 13. Efficiency vs Load Current (V_{OUT} = 20 V) - "X"

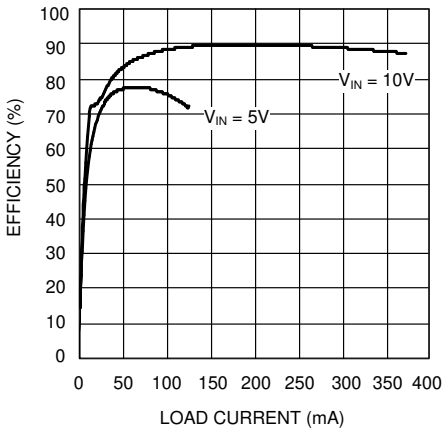


Figure 14. Efficiency vs Load Current (V_{OUT} = 25 V) - "X"

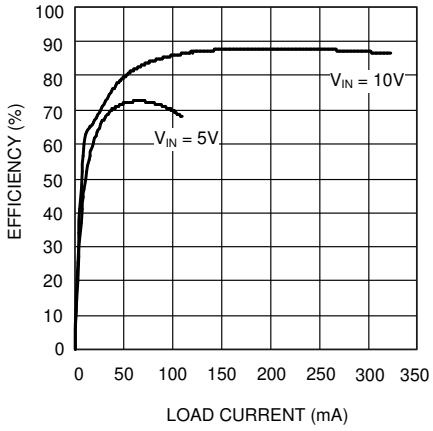


Figure 15. Efficiency vs Load Current (V_{OUT} = 30 V) - "X"

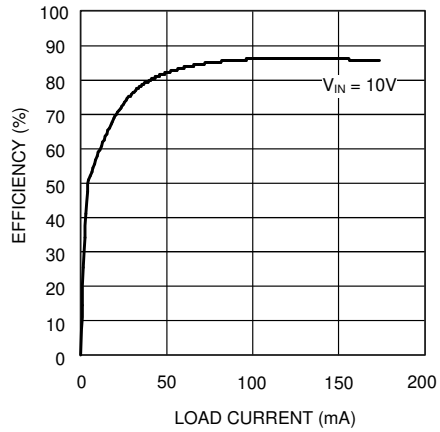


Figure 16. Efficiency vs Load Current (V_{OUT} = 35 V) - "X"

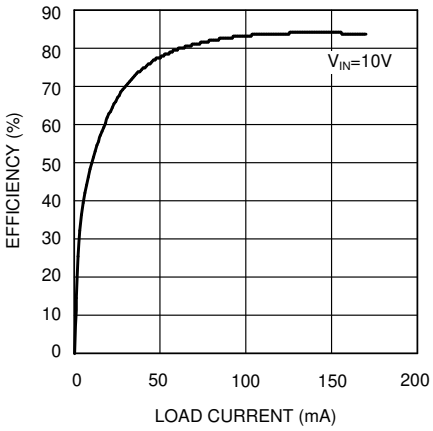


Figure 17. Efficiency vs Load Current (V_{OUT} = 40 V) - "X"

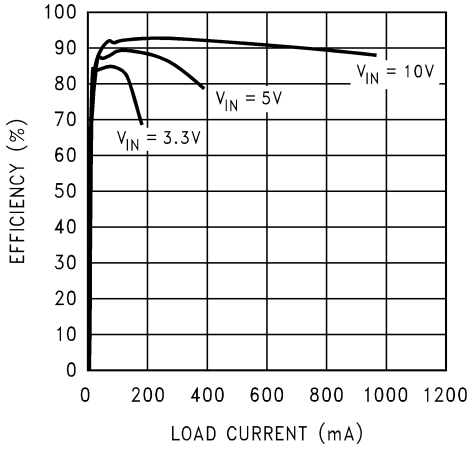


Figure 18. Efficiency vs Load (V_{OUT} = 15 V) - "Y"

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin is tied to V_{IN}.

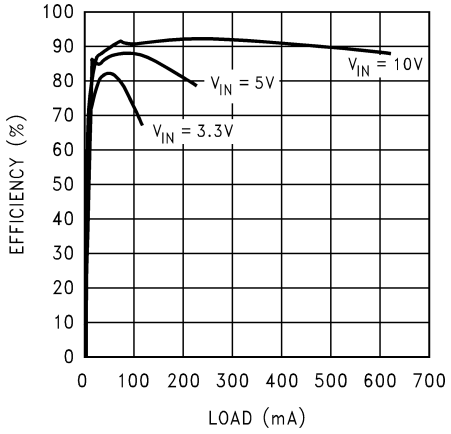


Figure 19. Efficiency vs Load (V_{OUT} = 20 V) - "Y"

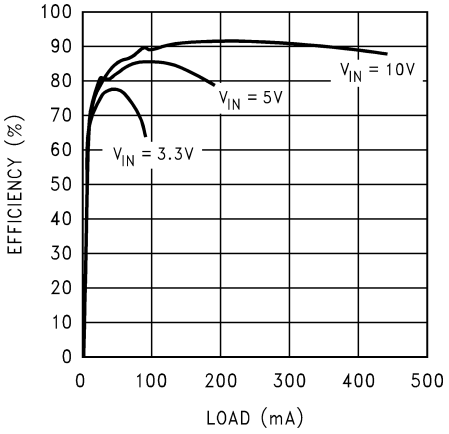


Figure 20. Efficiency vs Load (V_{OUT} = 25 V) - "Y"

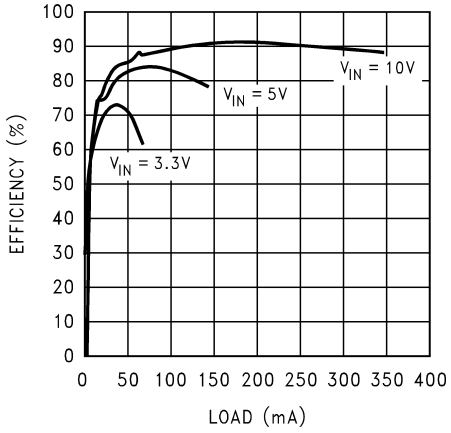


Figure 21. Efficiency vs Load (V_{OUT} = 30 V) - "Y"

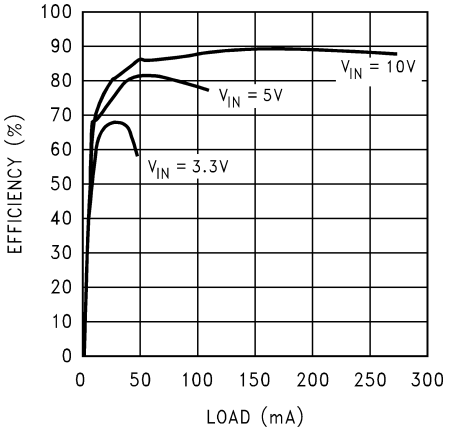


Figure 22. Efficiency vs Load (V_{OUT} = 35 V) - "Y"

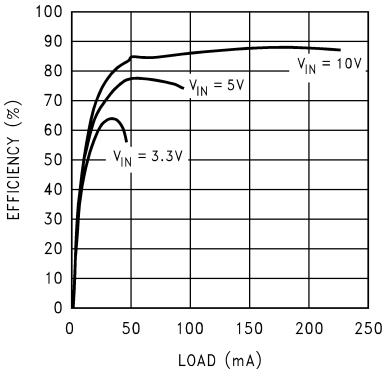


Figure 23. Efficiency vs Load (V_{OUT} = 40 V) - "Y"

7 Detailed Description

7.1 Overview

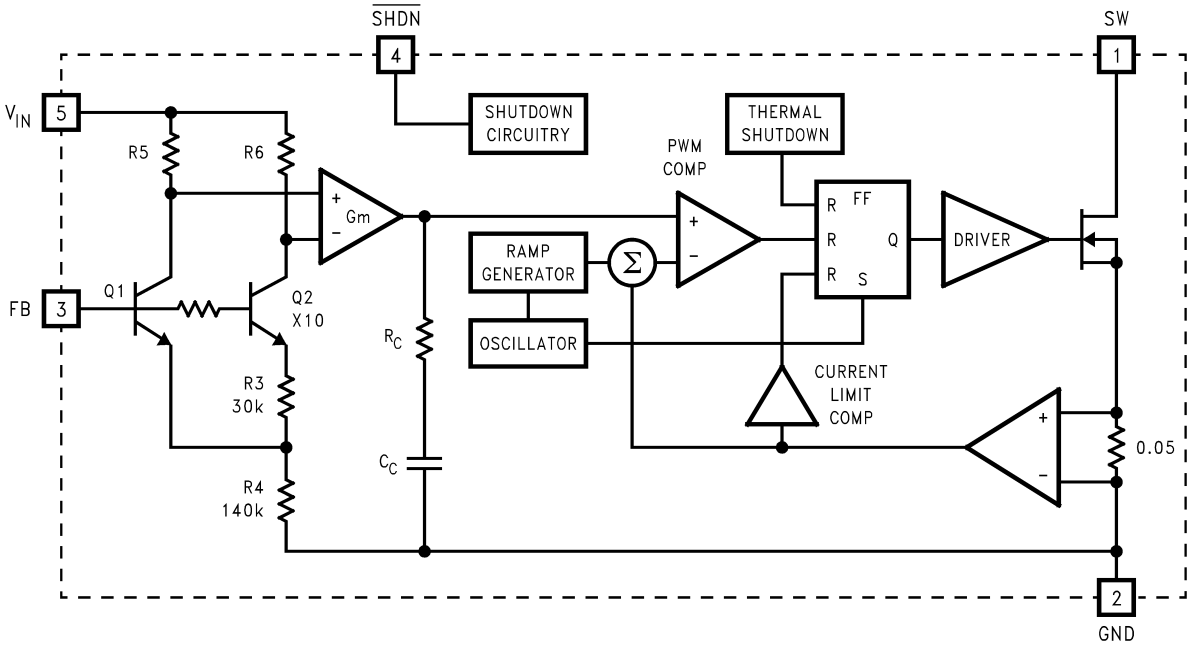
The LM2733 device is a switching converter IC that operates at a fixed frequency (0.6 or 1.6 MHz) using current-mode control for fast transient response over a wide input voltage range and incorporate pulse-by-pulse current limiting protection. Because this is current mode control, a 50 mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Since the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output volatge in regulation.

Q1 and Q2 along with R3 - R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 and Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node "multiplied up" by the ratio of the output resistive divider.

The current limit comparator feeds directly into the flip-flop, that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminated until the next clock pulse. The current limit input terminates the pulse regardless of the status of the output of the PWM comparator.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Switching Frequency

The LM2733 device is provided with two switching frequencies: the “X” version is typically 1.6 MHz, while the “Y” version is typically 600 kHz. The best frequency for a specific application must be determined based on the tradeoffs involved. See *Switching Frequency* in the *Detailed Design Procedure* section.

7.4 Device Functional Modes

7.4.1 Shutdown Pin Operation

The device is turned off by pulling the shutdown pin low. If this function is not going to be used, tie the pin directly to V_{IN}. If the SHDN function is needed, a pullup resistor must be used to V_{IN} (approximately 50 k to 100 kΩ recommended). The SHDN pin must not be left unterminated.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2733 device is a high frequency switching boost regulator that offers small size and high power conversion efficiency. The "X" version of the part operates at 1.6 MHz switching frequency and the "Y" version at 600 kHz.

The LM2733 device targets applications with high output voltages and uses a high voltage FET allowing switch currents up to 1 A. The LM2731 device is similar to the LM2733 device but has a lower voltage FET allowing switch currents up to 1.8 A.

8.2 Typical Application

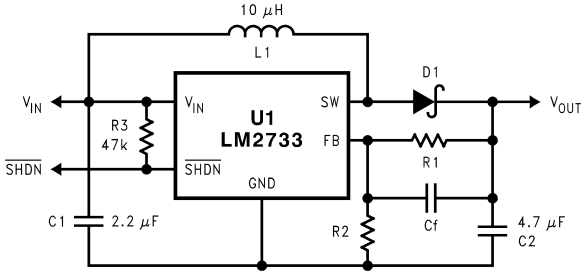


Figure 24. Basic Application Circuit

8.2.1 Design Requirements

Table 1. Circuit Configurations

COMPONENT	LM2733-X	LM2733-X	LM2733-Y
	LOW VOLTAGE 5-12 V 330 mA typical	HIGH VOLTAGE 20 V 170 mA typical	HIGH VOLTAGE 30 V 110 mA typical
R1	117 K	205 K	309 K
R2	13.3 K	13.3 K	13.3 K
Cf	220 pF	120 pF	82 pF
D1	MBR0520	MBR0530	MBR0540

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the External Capacitors

The best capacitors for use with the LM2733 device are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high frequency switching converters.

When selecting a ceramic capacitor, use only X5R and X7R dielectric types. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden, AVX, and Murata.

8.2.2.2 Selecting the Output Capacitor

A single ceramic capacitor of value 4.7 µF to 10 µF provides sufficient output capacitance for most applications. For output voltages below 10 V, a 10-µF capacitance is required. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used in parallel with the ceramics. Aluminum electrolytics with ultra-low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical AI electrolytic capacitors are not suitable for switching frequencies above 500 kHz due to significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

8.2.2.3 Selecting the Input Capacitor

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. TI recommends a nominal value of 2.2 µF, but larger values can be used. Because this capacitor reduces the amount of voltage ripple detected at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

8.2.2.4 Feedforward Compensation

Although internally compensated, the feedforward capacitor Cf is required for stability (see Figure 24). Adding this capacitor puts a zero in the loop response of the converter. Without it, the regulator loop can oscillate. The recommended frequency for the zero fz is approximately 8 kHz. Cf can be calculated using the formula:

$$Cf = 1 / (2 \times \pi \times R1 \times fz) \quad (1)$$

8.2.2.5 Selecting Diodes

The external diode used in the typical application should be a Schottky diode. If the switch voltage is less than 15 V, a 20-V diode such as the MBR0520 is recommended. If the switch voltage is between 15 V and 25 V, TI recommends a 30-V diode such as the MBR0530. If the switch voltage exceeds 25 V, a 40-V diode such as the MBR0540 should be used.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5 A. For applications exceeding 0.5 A average but less than 1 A, a Microsemi UPS5817 can be used.

8.2.2.6 Setting the Output Voltage

The output voltage is set using the external resistors R1 and R2 (see Figure 24). A value of approximately 13.3 kΩ is recommended for R2 to establish a divider current of approximately 92 µA. R1 is calculated using the formula:

$$R1 = R2 \times (V_{OUT}/1.23 - 1) \quad (2)$$

8.2.2.7 Switching Frequency

The device options provide for two fixed frequency operating conditions 1.6 MHz, and 600 kHz. Chose the operating frequency required noting the following trade-offs:

Higher switching frequency means the inductors and capacitors can be made smaller and cheaper for a given output voltage and current. The down side is that efficiency is slightly lower because the fixed switching losses occur more frequently and become a larger percentage of total power loss. EMI is typically worse at higher switching frequencies because more EMI energy will be seen in the higher frequency spectrum where most circuits are more sensitive to such interference.

8.2.2.8 Duty Cycle

The maximum duty cycle of the switching regulator determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

$$\text{Duty Cycle} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{V_{OUT} + V_{DIODE} - V_{SW}} \quad (3)$$

This applies for continuous mode operation.

The equation shown for calculating duty cycle incorporates terms for the FET switch voltage and diode forward voltage. The actual duty cycle measured in operation will also be affected slightly by other power losses in the circuit such as wire losses in the inductor, switching losses, and capacitor ripple current losses from self-heating. Therefore, the actual (effective) duty cycle measured may be slightly higher than calculated to compensate for these power losses. A good approximation for effective duty cycle is :

$$DC\ (eff) = (1 - Efficiency \times (V_{IN}/V_{OUT})) \quad (4)$$

Where the efficiency can be approximated from the curves provided.

8.2.2.9 Inductance Value

The first question we are usually asked is: “How small can I make the inductor?” (because they are the largest sized component and usually the most costly). The answer is not simple and involves tradeoffs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L/2 \times (Ip)^2 \quad (5)$$

Where “Ip” is the peak inductor current. An important point to observe is that the LM2733 device will limit its switch current based on peak current. This means that since Ip (maximum) is fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays “continuous” over a wider load current range.

To better understand these tradeoffs, a typical application circuit (5V to 12V boost with a 10 µH inductor) will be analyzed. We will assume:

V_{IN} = 5 V, V_{OUT} = 12 V, V_{DIODE} = 0.5 V, V_{SW} = 0.5 V

Since the frequency is 1.6 MHz (nominal), the period is approximately 0.625 µs. The duty cycle will be 62.5%, which means the ON time of the switch is 0.390 µs. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5 V.

Using the equation:

$$V = L\ (di/dt) \quad (6)$$

We can then calculate the di/dt rate of the inductor which is found to be 0.45 A/µs during the ON time. Using these facts, we can then show what the inductor current will look like during operation:

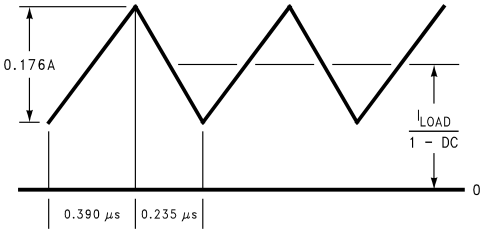


Figure 25. 10-µH Inductor Current, 5-V – 12-V Boost (LM2733X)

During the 0.390 µs ON time, the inductor current ramps up 0.176 A and ramps down an equal amount during the OFF time. This is defined as the inductor “ripple current”. It can also be seen that if the load current drops to about 33 mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.

8.2.2.10 Maximum Switch Current

The maximum FET swtch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in the graphs below which show both the typical and specified values of switch current for both the "X" and "Y" versions as a function of effective (actual) duty cycle:

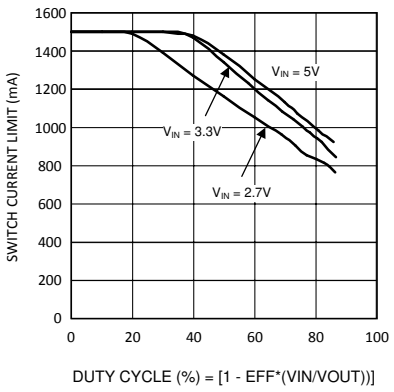


Figure 26. Switch Current Limit vs Duty Cycle - "X"

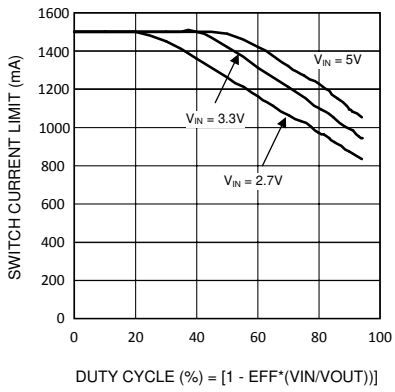


Figure 27. Switch Current Limit vs Duty Cycle - "Y"

8.2.2.11 Calculating Load Current

As shown in the figure which depicts inductor current, the load current is related to the average inductor current by the relation:

$$I_{LOAD} = I_{IND}(AVG) \times (1 - DC) \quad (7)$$

Where "DC" is the duty cycle of the application. The switch current can be found by:

$$I_{SW} = I_{IND}(AVG) + ½ (I_{RIPPLE}) \quad (8)$$

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{IN}-V_{SW}) / (f \times L) \quad (9)$$

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

$$I_{LOAD}(max) = (1 - DC) \times \left(I_{SW}(max) - \frac{DC\,(V_{IN} - V_{SW})}{2fL}\right) \quad (10)$$

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode. For actual load current in typical applications, we took bench data for various input and output voltages for both the "X" and "Y" versions of the LM2733 device and displayed the maximum load current available for a typical device in graph form:

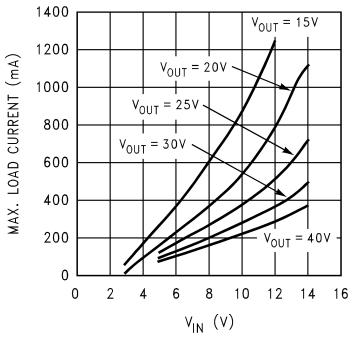


Figure 28. Max. Load Current vs V_{IN} - "X"

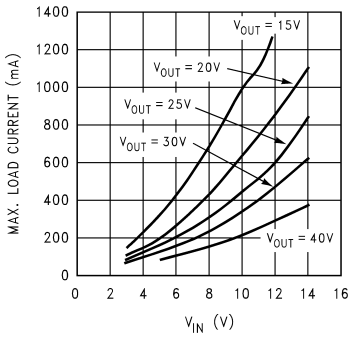


Figure 29. Max. Load Current vs V_{IN} - "Y"

8.2.2.12 Design Parameters V_{SW} and I_{SW}

The value of the FET "ON" voltage (referred to as V_{SW} in the equations) is dependent on load current. A good approximation can be obtained by multiplying the "ON Resistance" of the FET times the average inductor current.

FET on resistance increases at V_{IN} values below 5 V, since the internal N-FET has less gate voltage in this input voltage range (see *Typical Characteristics*). Above V_{IN} = 5 V, the FET gate voltage is internally clamped to 5 V.

The maximum peak switch current the device can deliver is dependent on duty cycle. The minimum value is specified to be > 1 A at duty cycle below 50%. For higher duty cycles, see *Typical Characteristics*.

8.2.2.13 Thermal Considerations

At higher duty cycles, the increased ON time of the FET means the maximum output current will be determined by power dissipation within the LM2733 FET switch. The switch power dissipation from ON-state conduction is calculated by:

$$P_{(SW)} = DC \times I_{IND}(AVE)^2 \times R_{DS}ON \quad (11)$$

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

8.2.2.14 Minimum Inductance

In some applications where the maximum load current is relatively small, it may be advantageous to use the smallest possible inductance value for cost and size savings. The converter will operate in discontinuous mode in such a case.

The minimum inductance should be selected such that the inductor (switch) current peak on each cycle does not reach the 1-A current limit maximum. To understand how to do this, an example will be presented.

In the example, the LM2733X will be used (nominal switching frequency 1.6 MHz, minimum switching frequency 1.15 MHz). This means the maximum cycle period is the reciprocal of the minimum frequency:

$$T_{ON(max)} = 1/1.15M = 0.870\ \mu s \quad (12)$$

We will assume the input voltage is 5 V, V_{OUT} = 12 V, V_{SW} = 0.2 V, V_{DIODE} = 0.3 V. The duty cycle is:

Duty Cycle = 60.3%

Therefore, the maximum switch ON time is 0.524 µs. An inductor should be selected with enough inductance to prevent the switch current from reaching 1A in the 0.524 µs ON time interval (see below):

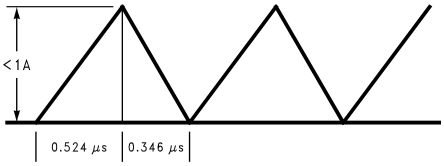


Figure 30. Discontinuous Design, 5V–12V Boost (LM2733X)

The voltage across the inductor during ON time is 4.8V. Minimum inductance value is found by:

$$V = L \times dI/dt,\ L = V \times (dt/dI) = 4.8\ (0.524\mu/1) = 2.5\ \mu H \quad (13)$$

In this case, a 2.7 µH inductor could be used assuming it provided at least that much inductance up to the 1A current value. This same analysis can be used to find the minimum inductance for any boost application. Using the slower switching “Y” version requires a higher amount of minimum inductance because of the longer switching period.

8.2.2.15 Inductor Suppliers

Some of the recommended suppliers of inductors for this product include, but not limited to are Sumida, Coilcraft, Panasonic, TDK and Murata. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

8.2.3 Application Curves

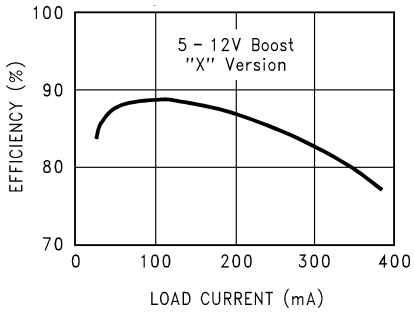


Figure 31. Efficiency vs. Load Current (5-12V, X-version)

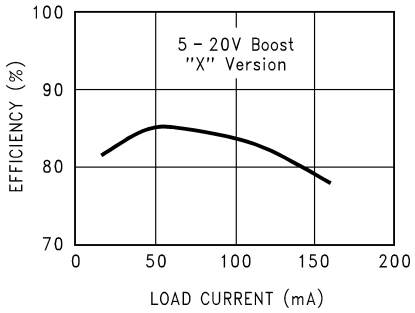


Figure 32. Efficiency vs. Load Current (5-20V X-version)

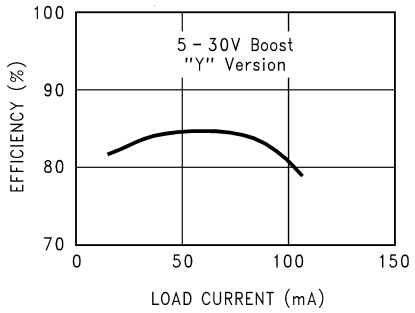


Figure 33. Efficiency vs. Load Current (5 - 30V Y-version)

9 Power Supply Recommendations

The device input voltage range is 2.7 V to 14 V.

The voltage on the shutdown pin should not exceed the voltage on the VIN pin. For applications that do not require a shutdown function the shutdown pin may be connected to the VIN pin. In this case a 47-KΩ resistor is recommended to be connected between these pins.

10 Layout

10.1 Layout Guidelines

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM2733 device. It is recommended that a 4-layer PCB be used so that internal ground planes are available.

Some additional guidelines to be observed:

1. Keep the path between L1, D1, and C2 extremely short. Parasitic trace inductance in series with D1 and C2 will increase noise and ringing.
2. The feedback components R1, R2 and CF must be kept close to the FB pin of U1 to prevent noise injection on the FB pin trace.
3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of U1, as well as the negative sides of capacitors C1 and C2.

10.2 Layout Example

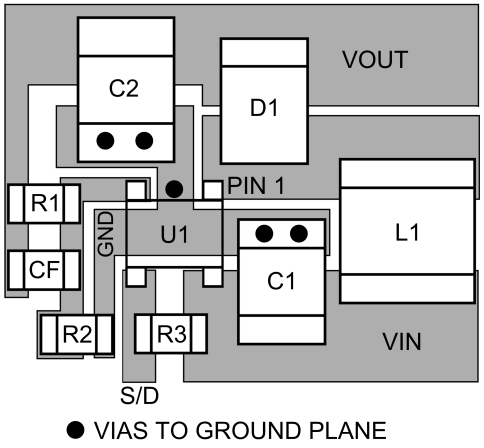


Figure 34. Recommended PCB Component Layout

11 デバイスおよびドキュメントのサポート

11.1 商標

All trademarks are the property of their respective owners.

11.2 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2733XMF	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	S52A	
LM2733XMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S52A	Samples
LM2733XMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S52A	Samples
LM2733YMF	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	S52B	
LM2733YMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S52B	Samples
LM2733YMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S52B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

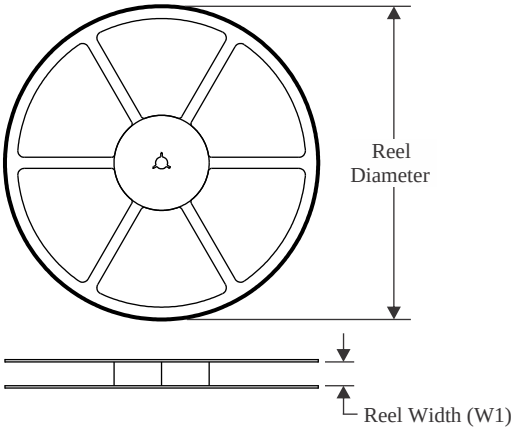
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

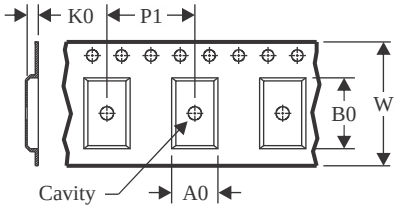
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

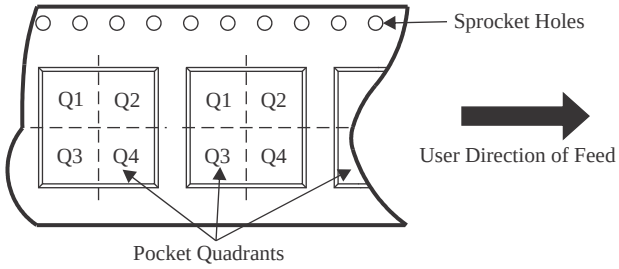


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

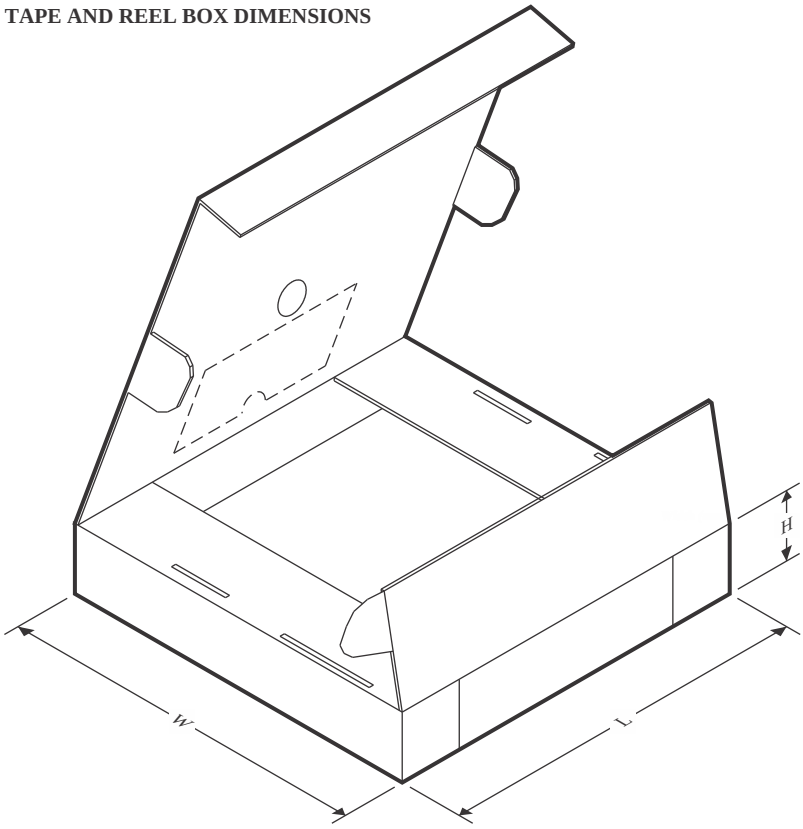
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2733XMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2733XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2733XMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2733YMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2733YMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2733YMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

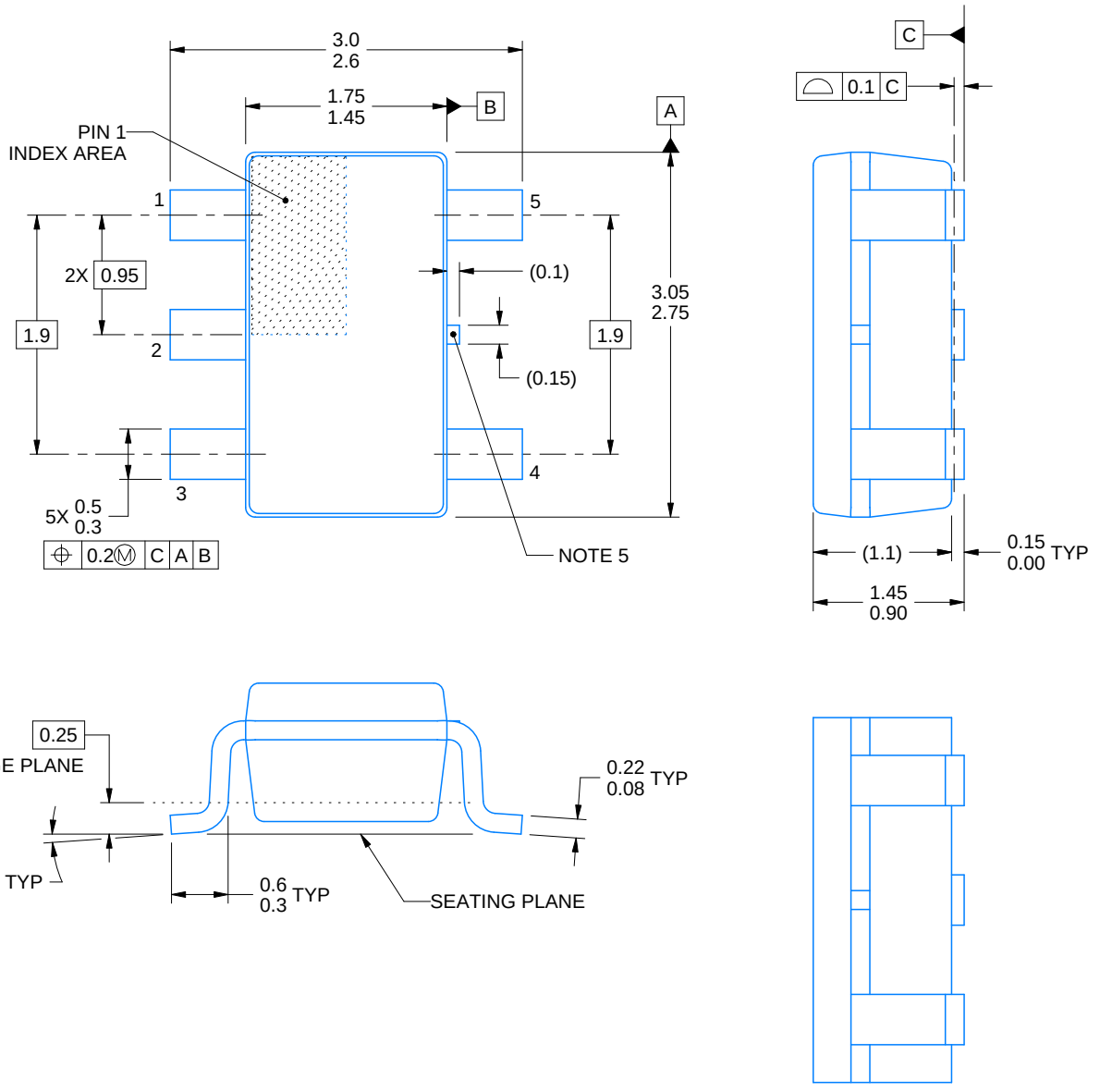
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2733XMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2733XMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2733XMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2733YMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2733YMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2733YMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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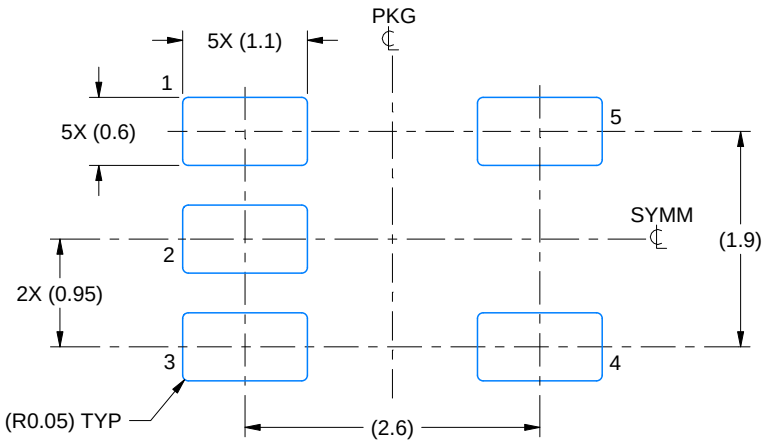
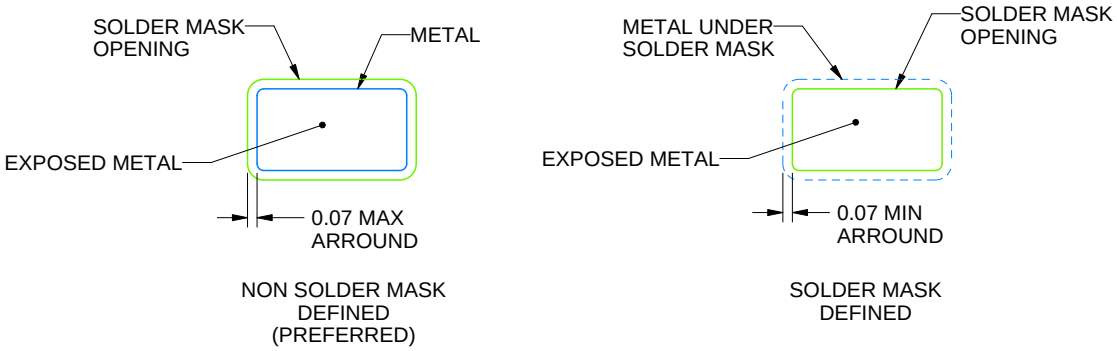
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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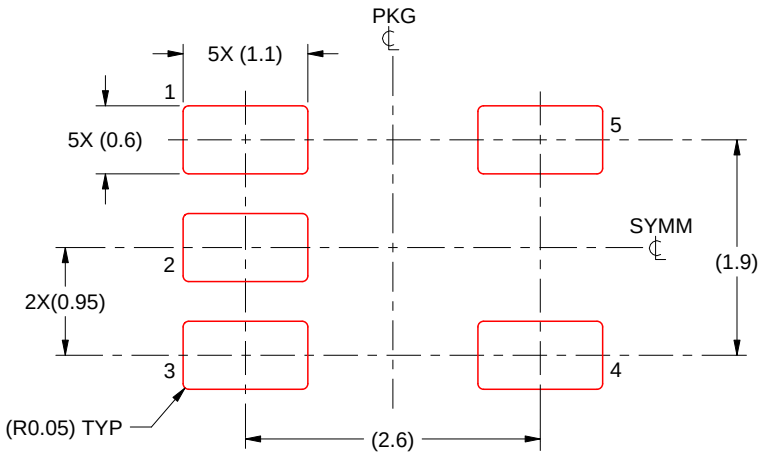
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265