LM3489x ヒステリシス制御PFET降圧コントローラ、イネーブル・ピン付

1 特長

- 車載用部品として認定済み
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード1: 動作時周囲温度範囲 −40°C～125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC5
- 使いやすい制御方式
- 制御ループ補償が不要
- 4.5V～35Vの広い入力電圧範囲
- 可変出力範囲: 1.239V～V_{IN}
- 高い効率: 93%
- ±1.3% (全温度範囲で±2%)の内部基準電圧
- 100%デューティ・サイクルでの動作
- 1MHzを超える最大動作周波数
- 電流制限保護
- 専用のイネーブル・ピン(無接続でオン)
- シャットダウン・モードでわずか7µAの消費電流
- 8ピンのVSSOPパッケージ

2 アプリケーション

- セットトップ·ボックス
- DSLまたはケーブル・モデム
- PC/IA
- Auto PC
- TFTモニタ
- バッテリ駆動の携帯用アプリケーション
- 分散電源システム
- 常時オンの電源
- 大電力のLEDドライバ
- 車載

3 概要

LM3489デバイスは高効率のPFETスイッチング・レギュレータ・コントローラであり、広範なアプリケーション向けの小型でコスト効率の優れたスイッチング降圧レギュレータを迅速かつ簡単に開発するため使用できます。ヒステリシス制御アーキテクチャにより、制御ループ安定性の懸念なしに、広範な外部部品を使用して単純な設計を行えます。また、PFETアーキテクチャにより、部品点数の削減、超低ドロップアウト、100%デューティ・サイクル動作を実現しています。さらに、軽負荷時に出力リップルが増大しない高効率動作も特長です。専用のイネーブル・ピンによりシャットダウン・モードへ移行し、消費電流がわずか7µAに低下します。イネーブル・ピンを無接続にすると、デフォルトでオンになります。

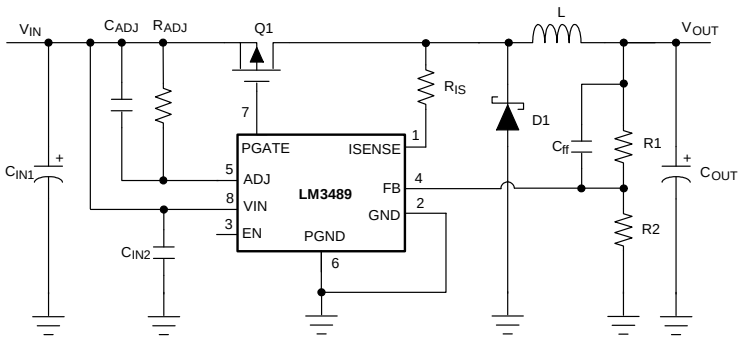
PFETの$R_{DS(ON)}$の両端で電圧を測定することにより電流制限保護を実装できるため、検出抵抗は必要ありません。必要なら、検出抵抗を使用して、電流制限の精度を向上することもできます。サイクル単位の電流制限は単一の抵抗で設定可能なため、広い範囲の出力電流で安全な動作を保証できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM3489 LM3489-Q1	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション回路



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (February 2013) から **Revision C** に変更 **Page**

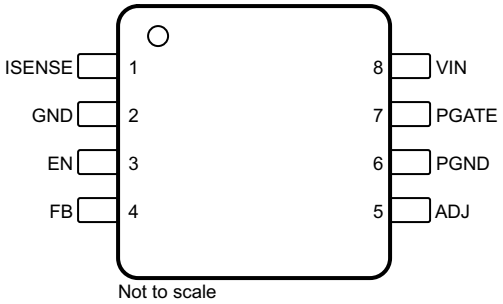
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「*特長*」にAEC-Q100認定の箇条書き項目を追加 ... 1
- Deleted Lead temperature (Vapor phase and Infrared maximums) ... 4
- Added *Thermal Information* table ... 5

Revision A (February 2013) から **Revision B** に変更 **Page**

- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ISENSE	I	The current sense input pin. This pin must be connected to the PFET drain terminal directly or through a series resistor up to 600 Ω for 28 V > VIN > 35 V.
2	GND	—	Signal ground
3	EN	I	Enable pin. Connect EN pin to ground to shutdown the part or float to enable operation (Internally pulled high). This pin can also be used to perform UVLO function.
4	FB	I	The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.
5	ADJ	I	Current limit threshold adjustment. Connected to an internal 5.5-µA current source. A resistor is connected between this pin and VIN. The voltage across this resistor is compared with the ISENSE pin voltage to determine if an overcurrent condition has occurred.
6	PGND	—	Power ground
7	PGATE	O	Gate drive output for the external PFET. PGATE swings between VIN and VIN 5-V.
8	VIN	I	Power supply input pin

6 Specifications

6.1 Absolute Maximum Ratings

See (1).

	MIN	MAX	UNIT
VIN voltage	–0.3	36	V
PGATE voltage	–0.3	36	V
FB voltage	–0.3	5	V
ISENSE voltage	–1	36	V
	–1 (<100 ns)		
ADJ voltage	–0.3	36	V
EN voltage(2)	–0.3	6	V
Power dissipation, T_A = 25°C(3)		417	mW
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is internally pulled high and clamped at 8 V (typical). The absolute maximum and operating maximum rating specifies the input level allowed for an external voltage source applied to this pin without triggering the internal clamp with margin.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, $R_{\theta JA}$ and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D = (T_J - T_A) / R_{\theta JA}$. Exceeding the maximum allowable power dissipation will lead to excessive die temperature.

6.2 ESD Ratings: LM3489

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LM3489-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply voltage		4.5	35	V
	EN voltage(1)			5.5	V
T_J	Operating junction temperature(2)	LM3489	–40	125	°C
		LM3489-Q1	–40	150	°C

(1) This pin is internally pulled high and clamped at 8 V (typical). The absolute maximum and operating maximum rating specifies the input level allowed for an external voltage source applied to this pin without triggering the internal clamp with margin.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.5 Thermal Information

THERMAL METRIC[1]		LM3489 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C for the LM3489 and LM3489-Q1. VIN = 12 V, $V_{ISNS} = V_{IN} - 1$ V, and V_{ADJ} = VIN − 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown input supply current	EN = 0 V		7	15	µA
V_{EN}	Enable threshold voltage	Enable rising	1.15	1.5	1.85	V
V_{EN_HYST}	Enable threshold hysteresis			130		mV
I_Q	Quiescent current at ground pin	FB = 1.5 V (not switching)		280	400	µA
V_{FB}	Feedback voltage[1]		1.214	1.239	1.264	V
V_{HYST}	Comparator hysteresis			10	20	mV
V_{CL_OFFSET}	Current limit comparator offset	V_{FB} = 1 V	–20	0	20	mV
I_{CL_ADJ}	Current limit ADJ current source	V_{FB} = 1.5 V	3	5.5	7	µA
T_{CL}	Current limit one-shot off-time	V_{ADJ} = 11.5 V, V_{ISNS} = 11 V, V_{FB} = 1 V	6	9	14	µs
R_{PGATE}	Driver resistance	Source, I_{SOURCE} = 100 mA		5.5		Ω
		Sink, I_{SINK} = 100 mA		8.5		
I_{PGATE}	Driver output current	Source, V_{IN} = 7 V, PGATE = 3.5 V		0.44		A
		Sink, V_{IN} = 7 V, PGATE = 3.5 V		0.1		
I_{FB}	FB pin bias current[2]	V_{FB} = 1 V		300	750	nA
T_{ONMIN_NOR}	Minimum ON time in normal operation	$V_{ISNS} = V_{ADJ}$ + 0.1 V, C_{load} on OUT = 1000 pF[3]		100		ns
T_{ONMIN_CL}	Minimum ON time in current limit	$V_{ISNS} = V_{ADJ}$ – 0.1 V, V_{FB} = 1 V, C_{load} on OUT = 1000 pF[3]		200		ns
$\%V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	4.5 V ≤ V_{IN} ≤ 35 V		0.01%		V

(1) The V_{FB} is the trip voltage at the FB pin when PGATE switches from high to low.
(2) Bias current flows out from the FB pin.
(3) A 1000-pF capacitor is connected between V_{IN} and PGATE.

6.7 Typical Characteristics

At T_A = 25°C and applicable to both LM3489 and LM3489-Q1 at V_{IN} = 12 V with configuration in *Detailed Description* (unless otherwise noted).

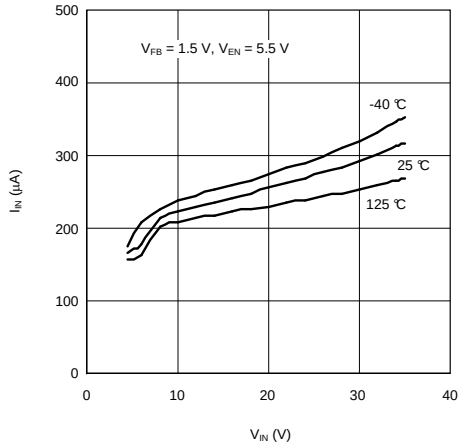


Figure 1. Quiescent Current vs Input Voltage

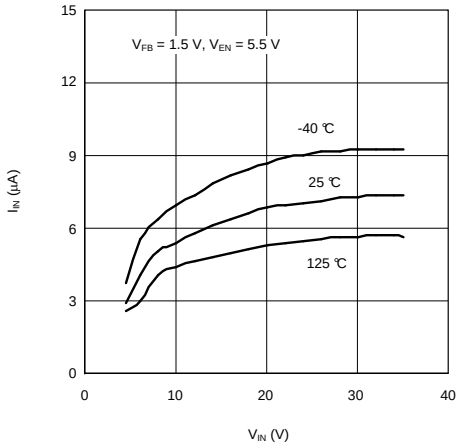


Figure 2. Shutdown Current vs Input Voltage

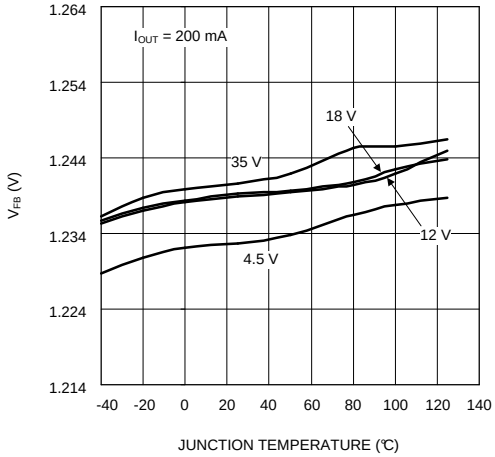


Figure 3. Feedback Voltage vs Temperature

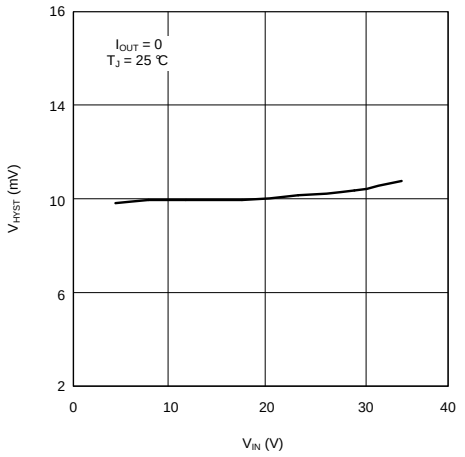


Figure 4. Feedback Voltage Hysteresis vs Input Voltage

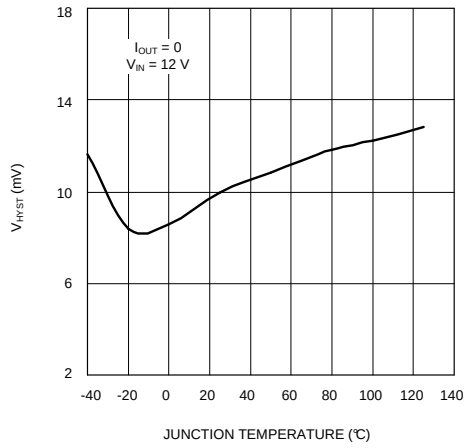


Figure 5. Feedback Voltage Hysteresis vs Temperature

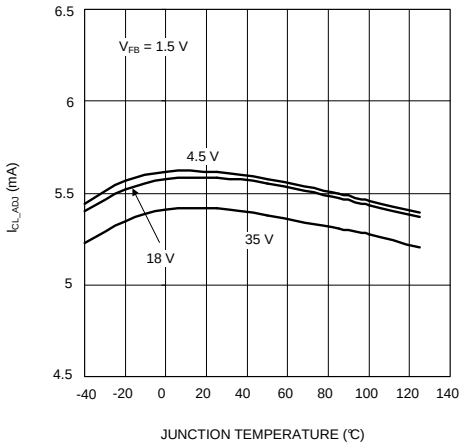


Figure 6. Current Limit ADJ Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C and applicable to both LM3489 and LM3489-Q1 at V_{IN} = 12 V with configuration in *Detailed Description* (unless otherwise noted).

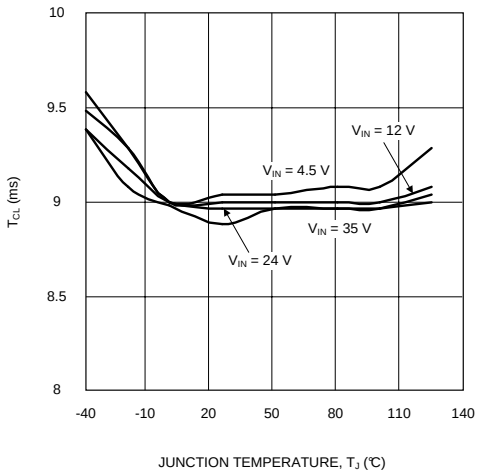


Figure 7. Current Limit One Shot OFF Time vs Temperature

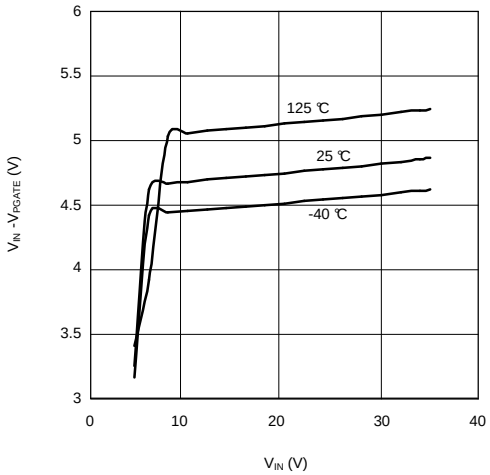


Figure 8. V_{IN} – V_{PGATE} vs V_{IN}

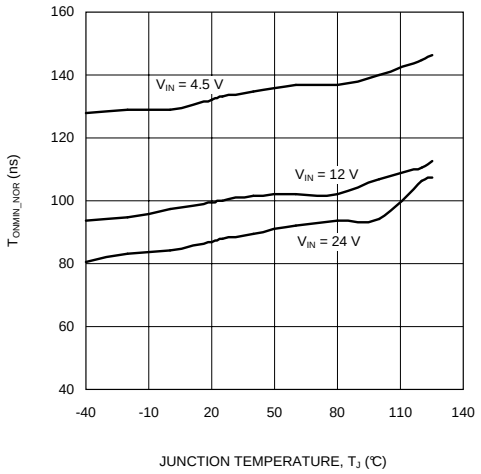


Figure 9. Minimum ON Time vs Temperature (Normal Operation)

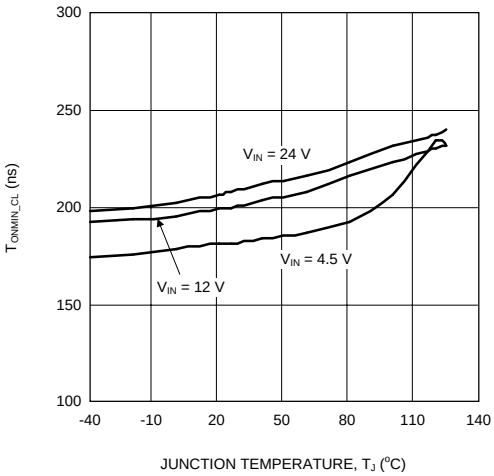


Figure 10. Minimum ON Time vs Temperature (Current Limit)

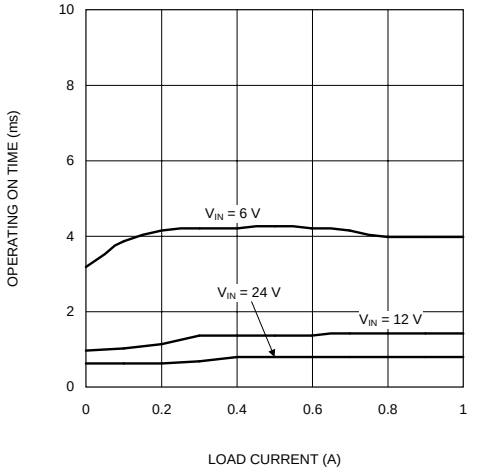


Figure 11. Operating ON Time vs Load Current

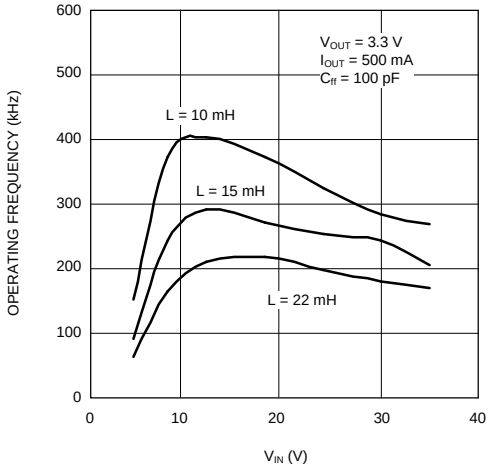
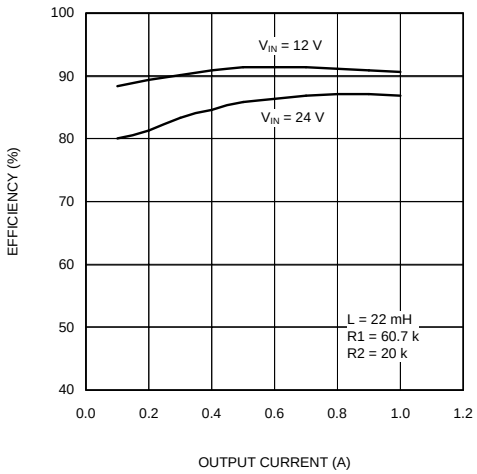


Figure 12. Operating Frequency vs Input Voltage

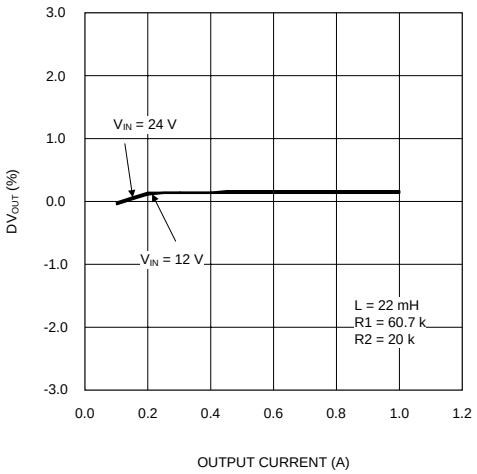
Typical Characteristics (continued)

At T_A = 25°C and applicable to both LM3489 and LM3489-Q1 at V_{IN} = 12 V with configuration in *Detailed Description* (unless otherwise noted).



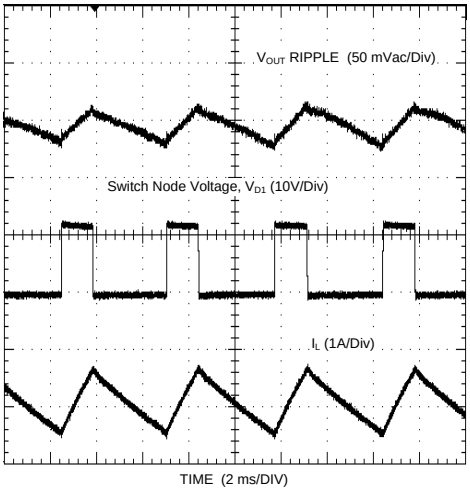
V_{OUT} = 5 V, L = 22 µH

Figure 13. Efficiency vs Load Current



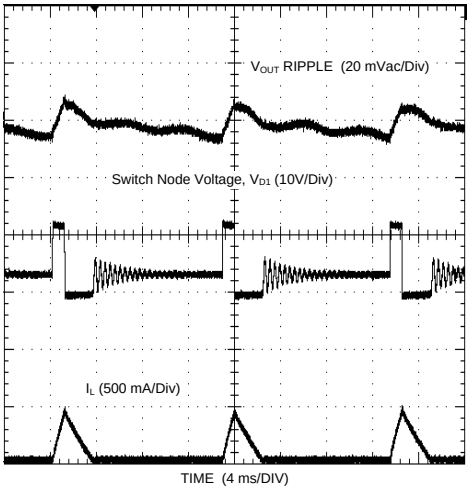
V_{OUT} = 5 V, L = 22 µH

Figure 14. V_{OUT} Regulation vs Load Current



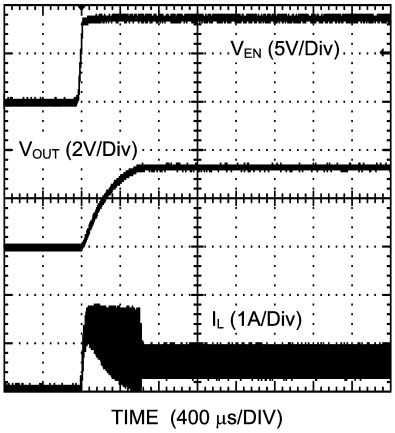
V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA

Figure 15. Continuous Mode Operation



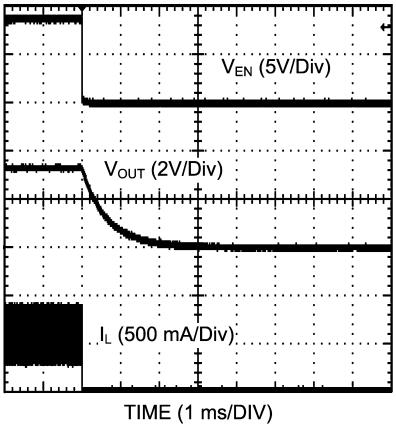
V_{IN} = 12 V, V_{OUT} =3.3 V, I_{OUT} = 50 mA

Figure 16. Discontinuous Mode Operation



V_{OUT} = 3.3 V, 500 mA loaded

Figure 17. Enable Transient



V_{OUT} = 3.3 V, 500 mA loaded

Figure 18. Shutdown Transient

7 Detailed Description

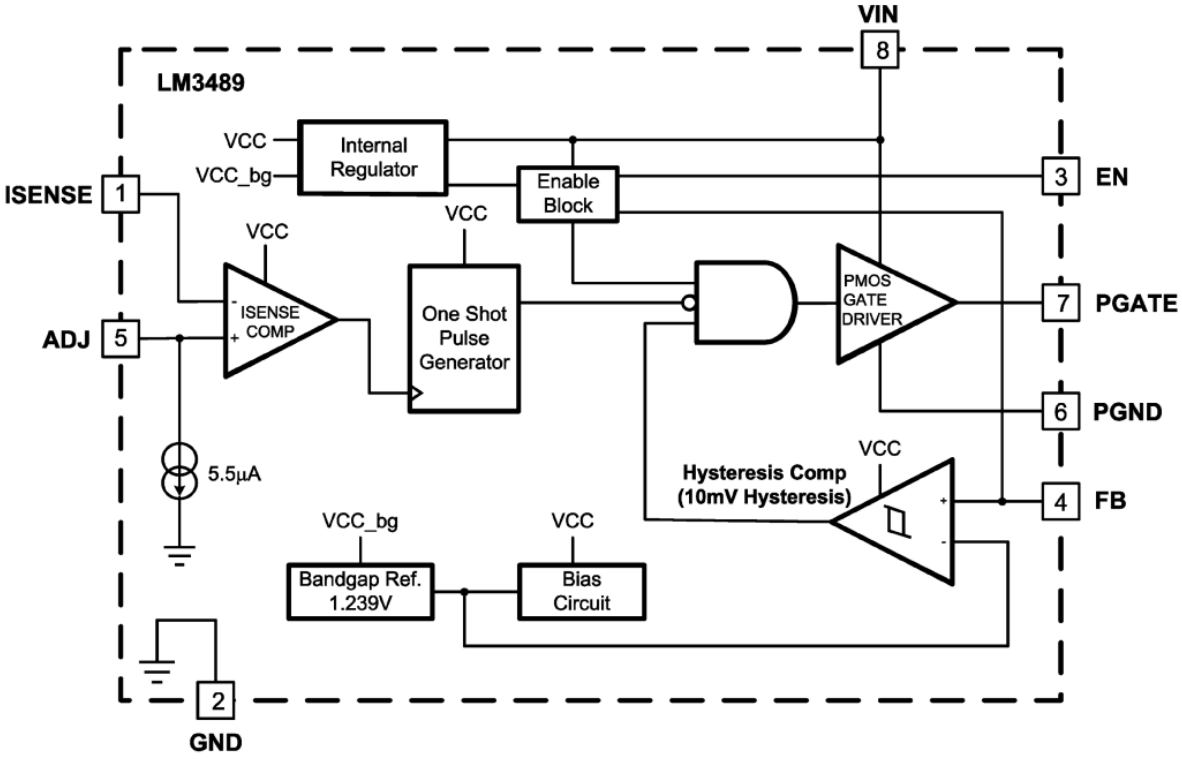
7.1 Overview

The LM3489 is a buck (step-down) DC-DC controller that uses a hysteretic control scheme. The control comparator is designed with approximately 10 mV of hysteresis. In response to the voltage at the FB pin, the gate drive (PGATE pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9 µs.

Hysteretic control does not require an internal oscillator. Switching frequency depends on the external components and operating conditions. The operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

The output voltage can be programmed by two external resistors. The output can be set in a wide range from 1.239 V (typical) to V_{IN}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit

When the FB input to the control comparator falls below the reference voltage (1.239 V), the output of the comparator switches to a low state. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET. With the PFET on, the input supply charges C_{OUT} and supplies current to the load through the series path through the PFET and the inductor. Current through the Inductor ramps up linearly and the output voltage increases. As the FB voltage reaches the upper threshold, which is the internal reference voltage plus 10 mV, the output of the comparator changes from low to high, and the PGATE responds by turning the PFET off. As the PFET turns off, the inductor voltage reverses, the catch diode turns on, and the current through the inductor ramps down. Then, as the output voltage reaches the internal reference voltage again, the next cycle starts.

Feature Description (continued)

The LM3489 operates in discontinuous conduction mode at light-load current or continuous conduction mode at heavy-load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak then ramps down to zero. The next cycle starts when the FB voltage reaches the reference voltage. Until then, the inductor current remains zero and the output capacitor supplies the load. The operating frequency is lower and switching losses reduced. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

The output voltage (V_{OUT}) can be programmed by 2 external resistors. It can be calculated with Equation 1.

$$V_{OUT} = 1.239 \times (R1 + R2) / R2 \quad (1)$$

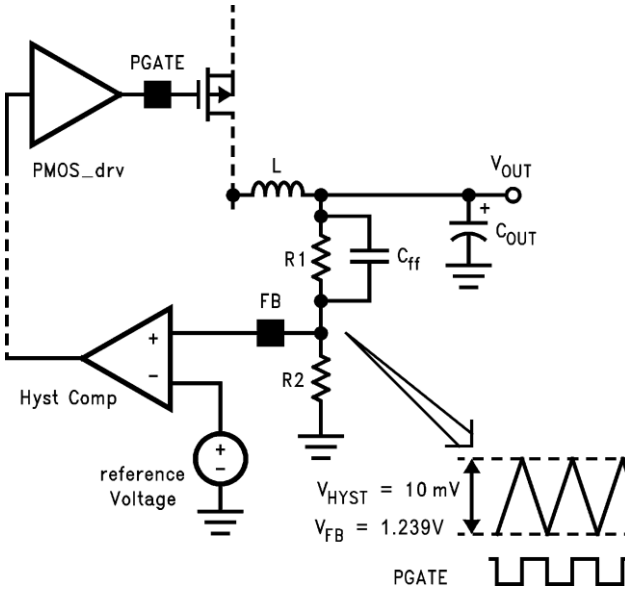


Figure 19. Hysteretic Window

The minimum output voltage ripple (V_{OUT_PP}) can be calculated in the same way with Equation 2.

$$V_{OUT\_PP} = V_{HYST} (R1 + R2) / R2 \quad (2)$$

For example, with V_{OUT} set to 3.3 V, V_{OUT_PP} is 26.6 mV in Equation 3.

$$V_{OUT\_PP} = 0.01 \times (33k + 20k) / 20k = 0.0266 \text{ V} \quad (3)$$

Operating frequency (F) is determined by knowing the input voltage, output voltage, inductor, V_{HYST}, ESR (Equivalent Series Resistance) of output capacitor, and the delay. It can be approximately calculated using Equation 4.

$$F = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT}) \times ESR}{(V_{HYST} \times \alpha \times L) + (V_{IN} \times delay \times ESR)}$$

where

- α: (R1 + R2) / R2 (4)

7.3.1.1 Delay

It includes the LM3489 propagation delay time and the PFET delay time. The propagation delay is 90 ns typically (see Figure 20).

Feature Description (continued)

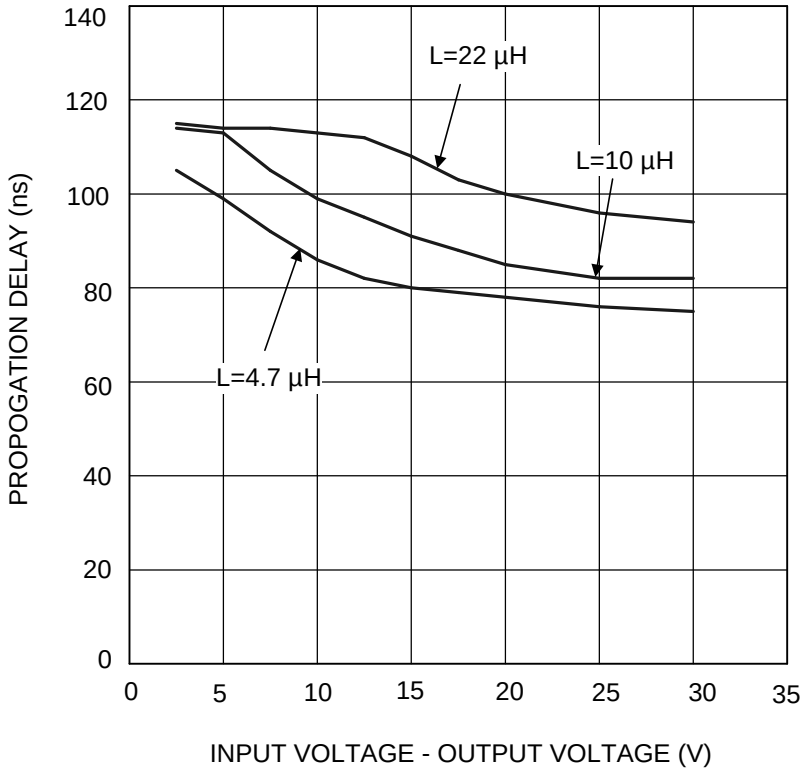


Figure 20. Propagation Delay

The operating frequency and output ripple voltage can also be significantly influenced by the speed up capacitor (Cff). Cff is connected in parallel with the high side feedback resistor, R1. The location of this capacitor is similar to where a phase lead capacitor would be located in a PWM control scheme. However it's effect on hysteretic operation is much different. Cff effectively shorts out R1 at the switching frequency and applies the full output ripple to the FB pin without dividing by the R2/R1 ratio. The end result is a reduction in output ripple and an increase in operating frequency. When adding Cff, calculate the formula above with α = 1. The value of Cff depend on the desired operating frequency and the value of R2. A good starting point is 470-pF ceramic at 100-kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 2.5 V, the effect of Cff will decrease significantly.

7.3.2 Current Limit Operation

The LM3489 has a cycle-by-cycle current limit. Current limit is sensed across the V_{DS} of the PFET or across an additional sense resistor. When current limit is activated, the LM3489 turns off the external PFET for a period of 9 µs (typical). The current limit is adjusted by an external resistor, R_{ADJ}.

The current limit circuit is composed of the ISENSE comparator and the one-shot pulse generator. The positive input of the ISENSE comparator is the ADJ pin. An internal 5.5-µA current sink creates a voltage across the external R_{ADJ} resistor. This voltage is compared to the voltage across the PFET or sense resistor. The ADJ voltage can be calculated with Equation 5.

$$V_{ADJ} = V_{IN} - (R_{ADJ} \times 3\ \mu A)$$

where

- 3 µA is the minimum $I_{CL\text{-}ADJ}$ value (5)

The negative input of the ISENSE comparator is the ISENSE pin that must be connected to the drain of the external PFET. The inductor current is determined by sensing the V_{DS}. It can be calculated with Equation 6.

$$V_{ISENSE} = V_{IN} - (R_{DSON} \times I_{IND\_PEAK}) = V_{IN} - V_{DS} \quad (6)$$

Feature Description (continued)

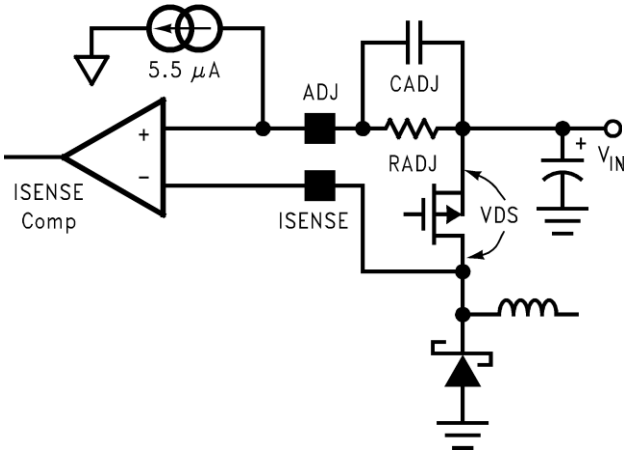


Figure 21. Current Sensing by V_{DS}

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the I_{SENSE} pin. The ISENSE comparator triggers the 9-µs one-shot pulse generator forcing the driver to turn the PFET off. The driver turns the PFET back on after 9 µs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, C_{ADJ}, must be placed as shown in Figure 21. C_{ADJ} filters unwanted noise so that the ISENSE comparator will not be accidentally triggered. A value of 100 pF to 1 nF is recommended in most applications. Higher values can be used to create a soft-start function (see *Start Up*).

The current limit comparator has approximately 100 ns of blanking time. This ensures that the PFET is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some PFETs may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100 ns. Under low duty cycle operation, the maximum operating frequency is limited by this minimum on-time.

During current limit operation, the output voltage drops significantly as does operating frequency. As the load current is reduced, the output returns to the programmed voltage. However, there is a current limit foldback phenomenon inherent in this current limit architecture (see Figure 22).

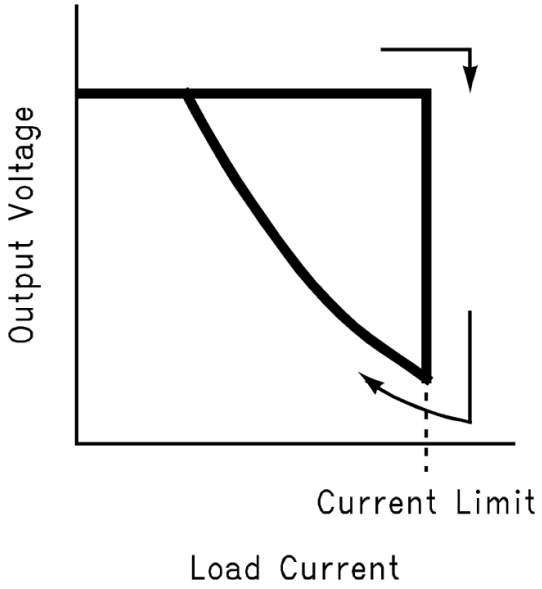


Figure 22. Current Limit Foldback Phenomenon

Feature Description (continued)

At high input voltages (> 28 V) increased undershoot at the switch node can cause an increase in the current limit threshold. To avoid this problem, a low Vf Schottky catch diode must be used (see *Catch Diode Selection (D1)*). Additionally, a resistor can be placed between the ISENSE pin and the switch node. Any value in the range of 220 Ω to 600 Ω is recommended.

7.3.3 Start Up

The current limit circuit is active during start-up. During start-up, the PFET stays on until either the current limit or the feedback comparator is tripped

If the current limit comparator is tripped first, then take the the foldback characteristic into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up.

One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance (C_{ADJ}) in parallel with R_{ADJ} results in a soft-start characteristic. C_{ADJ} and R_{ADJ} create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using this technique. There is example start-up plot for C_{ADJ} equal to 1 nF in *Typical Characteristics*. Lower values for C_{ADJ} will have little to no effect on soft-start.

7.3.4 External Sense Resistor

The V_{DS} of a PFET tends to vary significantly over temperature. This will result an equivalent variation in current limit. To improve current limit accuracy, an external sense resistor can be connected from V_{IN} to the source of the PFET, as shown in Figure 23. The current sense resistor, R_{CS} must have value comparable with R_{DSON} of the PFET used, typically in the range of 50 mΩ to 200 mΩ. Equation 6 in *Current Limit Operation* can be used by replacing the R_{DSON} with R_{CS}.

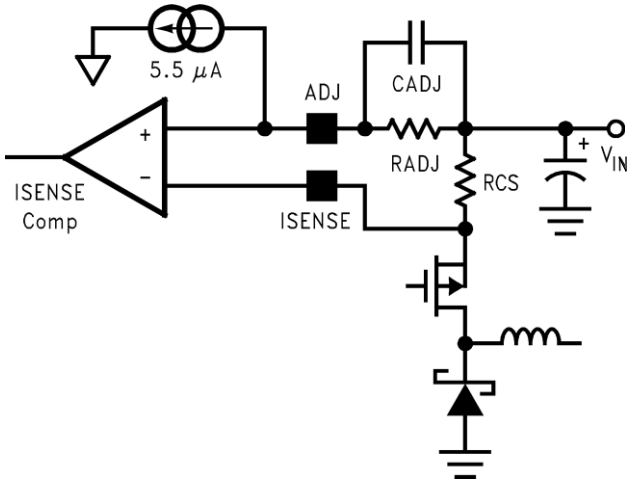


Figure 23. Current Sensing by External Resistor

7.3.5 PGATE

When switching, the PGATE pin swings from VIN (off) to some voltage below VIN (on). How far the PGATE will swing depends on several factors including the capacitance, on-time, and input voltage.

PGATE voltage swing will increase with decreasing gate capacitance. Although PGATE voltage will typically be around VIN-5V, with very small gate capacitances, this value can increase to a typical maximum of VIN-8.3 V.

Additionally, PGATE swing voltage will increase as on-time increases. During long on-times, such as when operating at 100% duty cycle, the PGATE voltage will eventually fall to its maximum voltage of VIN-8.3 V (typical) regardless of the PFET gate capacitance.

The PGATE voltage will not fall below 0.4 V (typical). Therefore, when the input voltage falls below approximately 9 V, the PGATE swing voltage range is reduced. At an input voltage of 7 V, for instance, PGATE will swing from 7 V to a minimum of 0.4 V.

Feature Description (continued)

7.3.6 Adjustable UVLO

The undervoltage lockout (UVLO) function can be implemented as shown in Figure 24. By incorporating the feature of the internal enable threshold, the lockout level can be programmed through an external potential divider formed with R3 and R4. The input voltage information is detected and compared with the enable threshold and the device operation is inhibited when V_{IN} drops below the preset UVLO level. The UVLO and hysteresis voltage can be calculated with Equation 7 and Equation 8.

$$V_{IN(UVLO)} = V_{EN}\left(1+\frac{R4}{R3}\right) \quad (7)$$

$$V_{IN(UVLO\_HYST)} = V_{EN\_HYST}\times\left(1+\frac{R4}{R3}\right) \quad (8)$$

where

- V_{EN} is the enable rising threshold voltage
- V_{EN_HYST} is the enable threshold hysteresis

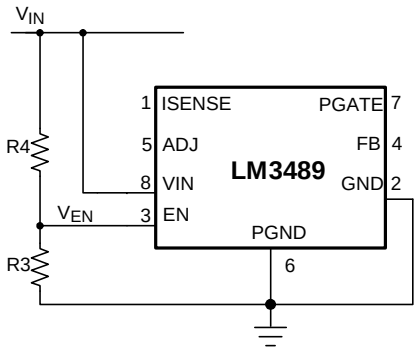


Figure 24. Adjustable UVLO

7.4 Device Functional Mode

7.4.1 Device Enable and Shutdown

The LM3489 can be remotely shutdown by forcing the enable pin to ground. With EN pin grounded, the internal blocks other than the enable logic are deactivated and the shutdown current of the device is lowered to only 7 µA (typical). Releasing the EN pin allows for normal operation to resume. The EN pin is internally pulled high with the voltage clamped at 8 V typical. For normal operation, this pin must be left open. In case an external voltage source is applied to this pin for enable control, the applied voltage must not exceed the maximum operating voltage level specified in this datasheet (that is 5.5 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Hysteretic control is a simple control scheme. However the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, V_{IN}, or Cff is changed, there is a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and C_{OUT} ESR.

8.2 Typical Application

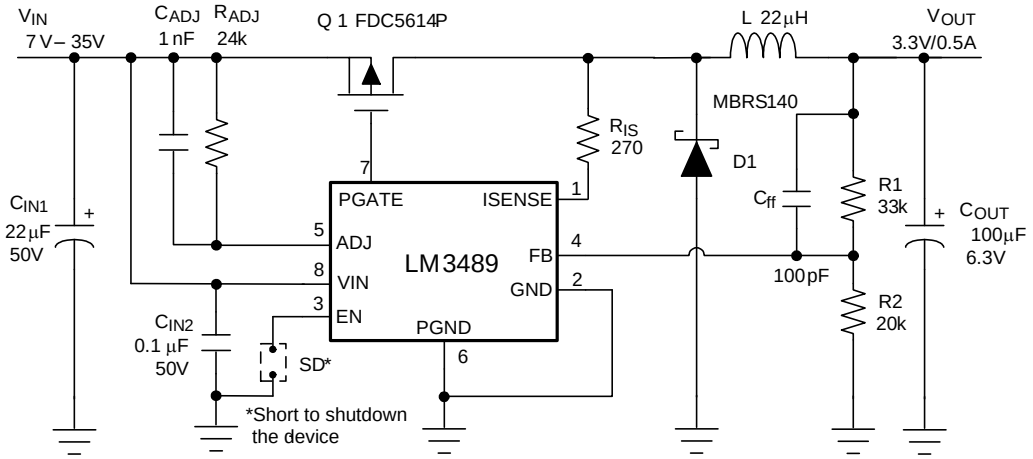


Figure 25. Typical Application Schematic for VOUT = 3.3 V, 500 mA

8.2.1 Design Requirements

The important parameters for the inductor are the inductance and the current rating. The LM3489 operates over a wide frequency range and can use a wide range of inductance values. A rule of thumb is to use the equations used for Simple Switchers®. The equations for inductor ripple (Δi) as a function of output current (I_{OUT}) depend on I_{out}:

For $I_{out} < 2$ A, $\Delta i \leq I_{out} \times I_{out}^{-0.366726}$.

For $I_{out} > 2$ A, $\Delta i \leq I_{out} \times 0.3$.

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection (L)

The inductance can be calculated with Equation 9 and Equation 10 based upon the desired operating frequency.

$$L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\Delta i} \times \frac{D}{f} \quad (9)$$

Typical Application (continued)

$$I_{pk} = \left(I_{OUT} + \frac{\Delta i}{2}\right) \times 1.1$$

where

- D is the duty cycle
- V_D is the diode forward voltage
- V_{DS} is the voltage drop across the PFET

(10)

The inductor must be rated with Equation 11.

$$I_{pk} = \left(I_{OUT} + \frac{\Delta i}{2}\right) \times 1.1$$

(11)

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the inductor ESR that contribute to the steady-state power loss due to current flowing through the inductor.

8.2.2.2 Output Capacitor Selection (C_{OUT})

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the V_{HYST} sets the first-order value of this ripple. As ESR is increased with a given inductance, operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common desire of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low-value resistor must be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provides highly accurate control over the output voltage ripple. Other types capacitor, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, and Nichicon *NA* series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

8.2.2.3 Input Capacitor Selection (C_{IN})

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage derating. For high-input voltage applications, low-ESR electrolytic, Nichicon *UD* series or the Panasonic *FK* series are available. The RMS current in the input capacitor can be calculated with Equation 12.

$$I_{RSM\_CIN} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

(12)

The input capacitor power dissipation can be calculated with Equation 13.

$$P_{D(CIN)} = I_{RMS\_CIN}^2 \times ESR_{CIN}$$

(13)

The input capacitor must be able to handle the RMS current and the dissipation. Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low-ESR, high-performance capacitor such as OS-CON or Tantalum. The capacitance value must be selected such that the ripple voltage created by the switch current pulses is less than 10% of the total DC voltage across the capacitor.

For high VIN conditions (> 28 V), the fast switching, high swing of the internal gate drive introduces unwanted disturbance to the VIN rail and the current limit function can be affected. To eliminate this potential problem, a high-quality ceramic capacitor of 0.1 µF is recommended to filter out the internal disturbance at the VIN pin. This capacitor must be placed right next to the VIN pin for best performance.

Typical Application (continued)

8.2.2.4 Programming the Current Limit (R_{ADJ})

The current limit is determined with Equation 14 by connecting a resistor (R_{ADJ}) between input voltage and the ADJ pin, pin 5.

$$R_{ADJ} = I_{IND\_PEAK} \times \frac{R_{DSON}}{I_{CL\_ADJ}}$$

where

- R_{DSON} is Drain-Source ON resistance of the external PFET
- I_{CL_ADJ} is 3 µA minimum
- $I_{IND\_PEAK} = I_{LOAD} + I_{RIPPLE} / 2$ (14)

Using the minimum value for I_{CL_ADJ} (3 µA) ensures that the current limit threshold is set higher than the peak inductor current.

The R_{ADJ} value must be selected to ensure that the voltage at the ADJ pin does not fall below 3.5 V. With this in mind, $R_{ADJ\_MAX} = (V_{IN} – 3.5) / 7$ µA. If a larger R_{ADJ} value is needed to set the desired current limit, either use a PFET with a lower R_{DSON} or use a current sense resistor as shown in Figure 23.

The current limit function can be disabled by connecting the ADJ pin to ground and ISENSE to VIN.

8.2.2.5 Catch Diode Selection (D1)

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated with Equation 15.

$$I_{D\_AVE} = I_{OUT} \times (1 – D) \quad (15)$$

The off-state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a Schottky diode is recommended. In low-output voltage applications, a low forward voltage provides improved efficiency. For high-temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

8.2.2.6 P-Channel MOSFET Selection (Q1)

The important parameters for the PFET are the maximum Drain-Source voltage (V_{DS}), the ON resistance (R_{DSON}), Current rating, and the input capacitance.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage.

PFET drain current, Id, must be rated higher than the peak inductor current, $I_{IND\text{-}PEAK}$.

Depending on operating conditions, the PGATE voltage may fall as low as V_{IN} – 8.3 V. Therefore, a PFET must be selected with a V_{GS} maximum rating greater than the maximum PGATE swing voltage.

As input voltage decreases below 9 V, PGATE swing voltage may also decrease. At 5-V input the PGATE will swing from V_{IN} to V_{IN} – 4.6 V. To ensure that the PFET turns on quickly and completely, a low threshold PFET must be used when the input voltage is less than 7 V.

Total power loss in the FET can be approximated using Equation 16.

$$PD_{switch} = R_{DSON} \times I_{OUT}^2 \times D + F \times I_{OUT} \times V_{IN} \times (t_{on} + t_{off}) / 2$$

where

- t_{on} is the FET turn on time
- t_{off} is the FET turn off time (16)

A value of 10 ns to 20 ns is typical for t_{on} and t_{off}.

A PFET must be selected with a turnon rise time of less than 100 ns. Slower rise times will degrade efficiency, can cause false current limiting, and in extreme cases may cause abnormal spiking at the PGATE pin.

Typical Application (continued)

The R_{DSON} is used in determining the current limit resistor value, R_{ADJ}. Note that the R_{DSON} has a positive temperature coefficient. At 100°C, the R_{DSON} may be as much as 150% higher than the 25°C value. This increase in R_{DSON} must be considered when determining R_{ADJ} in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature.

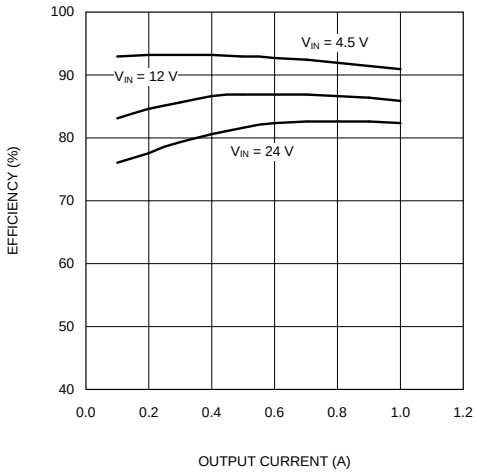
Keeping the gate capacitance below 2000 pF is recommended to keep switching losses and transition times low. This will also help keep the PFET drive current low, which will improve efficiency and lower the power dissipation within the controller.

As gate capacitance increases, operating frequency must be reduced and as gate capacitance decreases operating frequency can be increased.

8.2.2.7 Interfacing With the Enable Pin

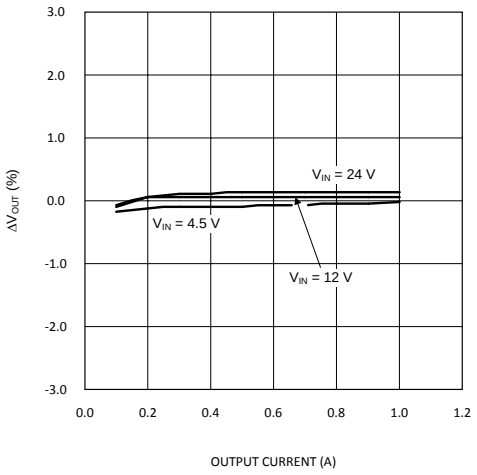
The enable pin is internally pulled high with clamping at 8 V typical. For normal operation this pin must be left open. To disable the device, the enable pin must be connected to ground externally. If an external voltage source is applied to this pin for enable control, the applied voltage must not exceed the maximum operating voltage level specified in this datasheet, that is 5.5 V. For most applications, an open-drain or open-collector transistor can be used to short this pin to ground to shutdown the device .

8.2.3 Application Curves



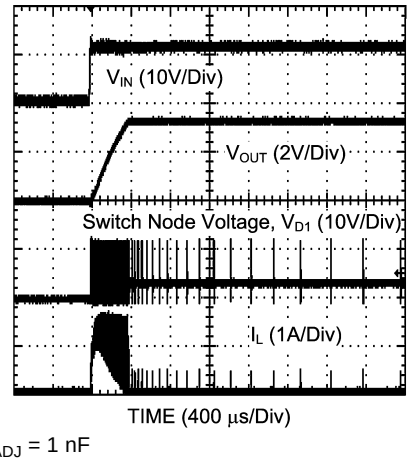
V_{OUT} = 3.3 V, L = 22 µH

Figure 26. Efficiency vs Load Current



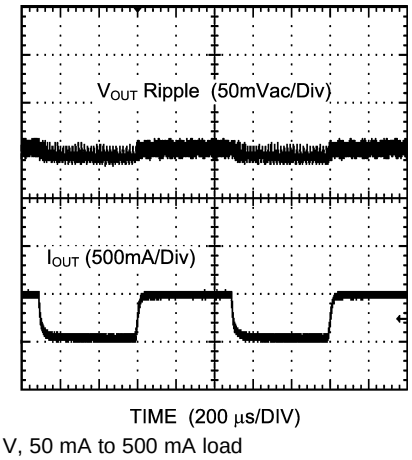
V_{OUT} = 3.3 V, L = 22 µH

Figure 27. V_{OUT} Regulation vs Load Current



No load, C_{ADJ} = 1 nF

Figure 28. Power Up



V_{OUT} = 3.3 V, 50 mA to 500 mA load

Figure 29. Load Transient

9 Power Supply Recommendations

This device is designed to operate over a recommended input voltage supply range of 4.5 V to 35 V. The input supply must be well regulated. If the input supply is located far from the LM3485 EVM and needs a long power supply cable to connect, an additional bulk capacitor may be required. An electrolytic capacitor with a value of 47 µF can be used typically.

As mentioned in *Current Limit Operation*, at higher input voltages (> 28 V) an increased negative SW transient spike at the switch node can lead to an increase in the current limit threshold due to the formation of the parasitic NPN connection between the ISENSE pin, the internal substrate and the ADJ pin . To avoid this issue, a Schottky catch diode with lower forward voltage drop must be used. In addition to that, a resistor must be placed between the ISENSE pin and the external switch node. A resistor value in the range of 220 Ω to 600 Ω is recommended.

10 Layout

10.1 Layout Guidelines

The PCB layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and generate EMI problems. For minimal inductance, the wires indicated by heavy lines in schematic diagram must be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the catch diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor and FET drain must be kept short. This node is one of the main sources for radiated EMI since it sees a large AC voltage at the switching frequency. It is always a good practice to use a ground plane in the design, particularly for high-current applications.

The two ground pins, PGND and GND, must be connected by as short a trace as possible. They can be connected underneath the device. These pins are resistively connected internally by approximately 50 Ω. The ground pins must be tied to the ground plane, or to a large ground trace in close proximity to both the FB divider and C_{OUT} grounds.

The gate pin of the external PFET must be placed close to the PGATE pin. However, if a very small FET is used, a resistor may be required between PGATE pin and the gate of the PFET to reduce high-frequency ringing. Because this resistor will slow down the PFET's rise time, the current limit blanking time must be taken into consideration (see *Current Limit Operation*). The feedback voltage signal line can be sensitive to noise. Avoid inductive coupling with the inductor or the switching node. The FB trace must be kept away from those areas. Also, the orientation of the inductor can contribute un-wanted noise coupling to the FB path. If noise problems are observed it may be worth trying a different orientation of the inductor and select the best for final component placement.

10.2 Layout Examples

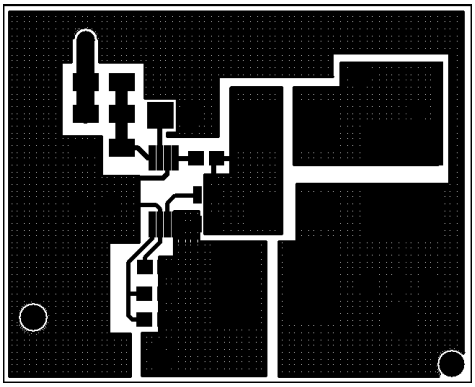


Figure 30. LM3489 EVM PCB Top Layer Layout

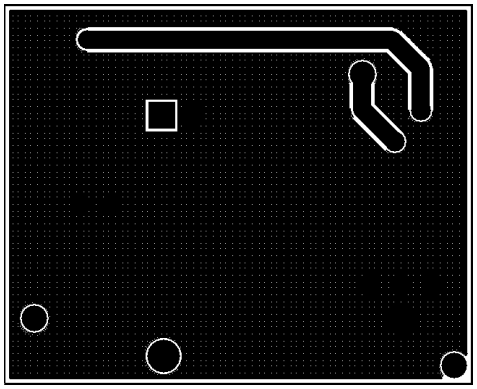


Figure 31. LM3489 EVM PCB Bottom Layer Layout

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LM3489	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LM3489-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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11.6 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3489MM	LIFEBUY	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	SKSB	
LM3489MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	SKSB	Samples
LM3489MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	SKSB	Samples
LM3489QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STEB	Samples
LM3489QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STEB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM3489, LM3489-Q1 :

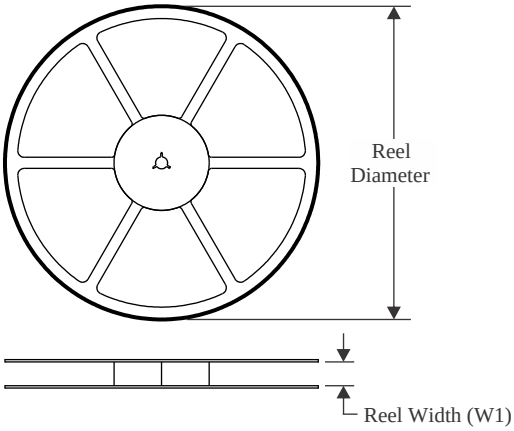
- Catalog : LM3489
- Automotive : LM3489-Q1

NOTE: Qualified Version Definitions:

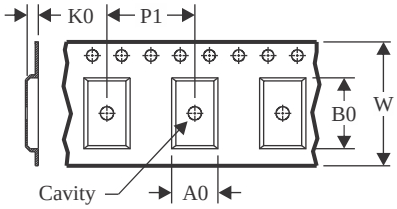
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

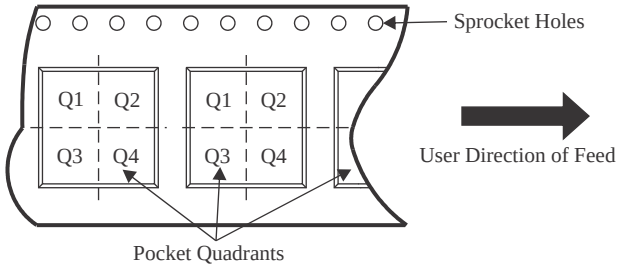


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

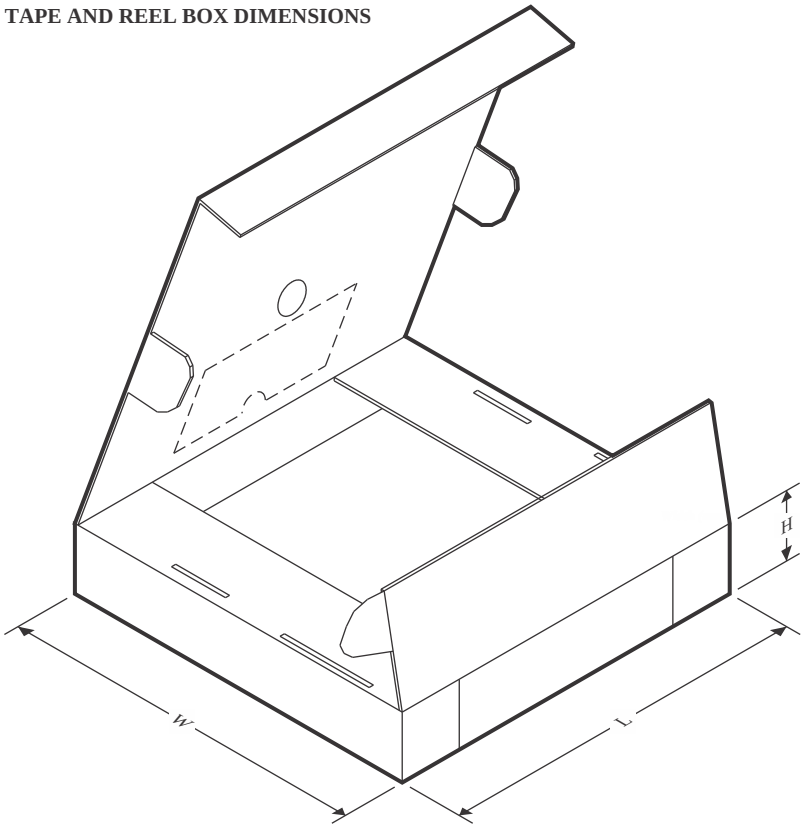
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3489MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

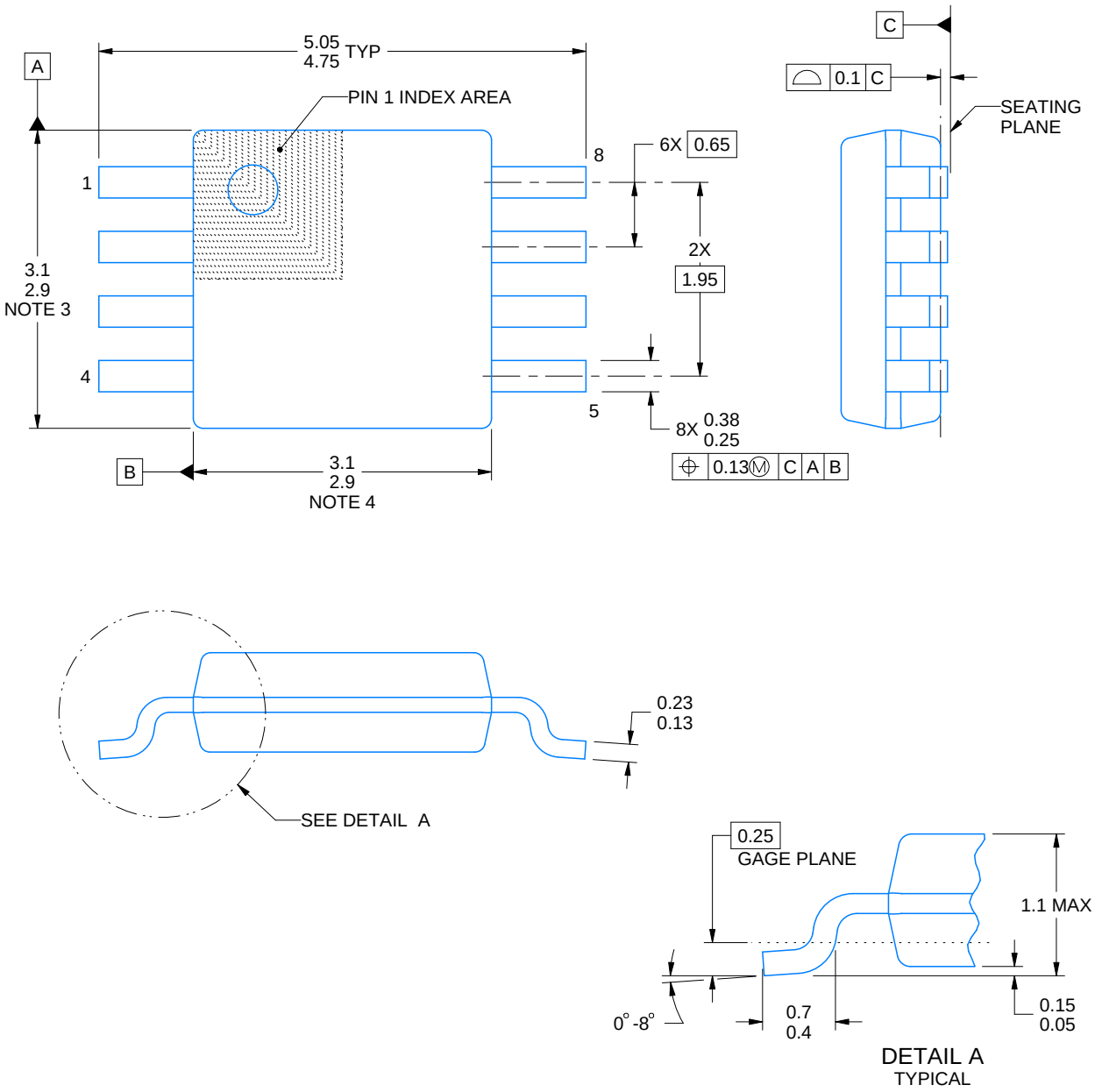
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3489MM	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3489MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3489MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3489QMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3489QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

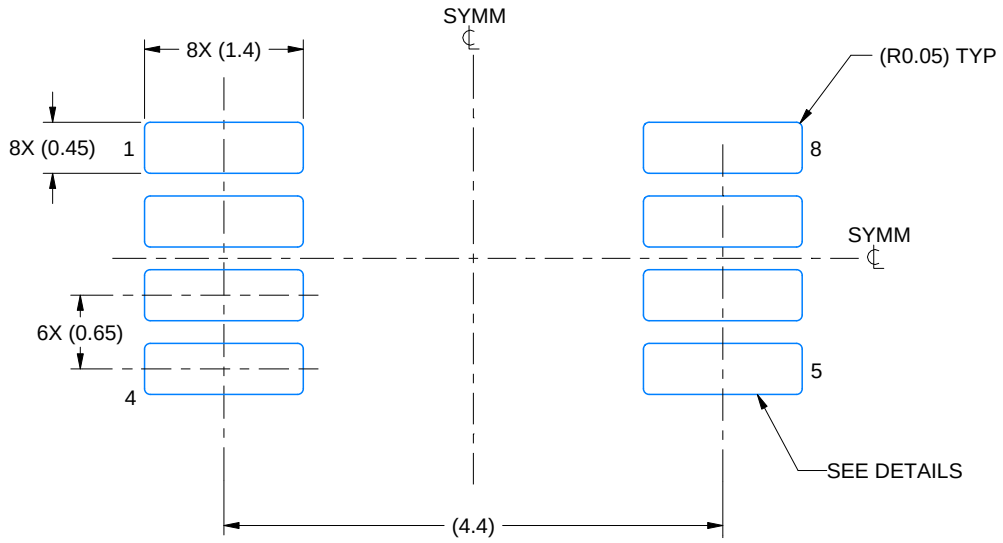
SMALL OUTLINE PACKAGE



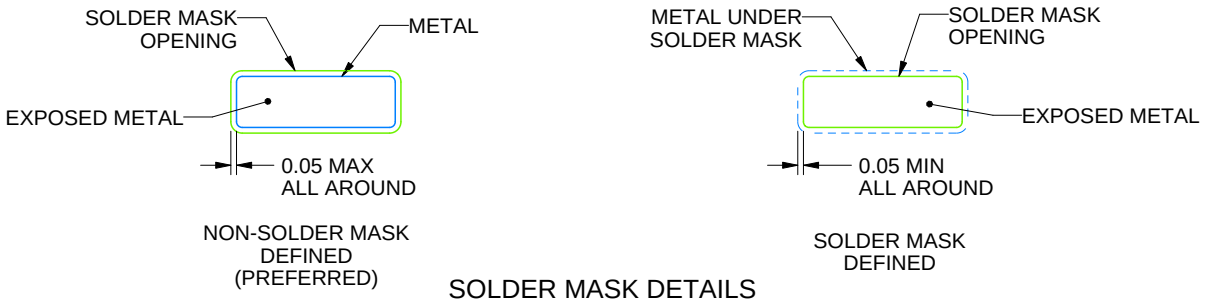
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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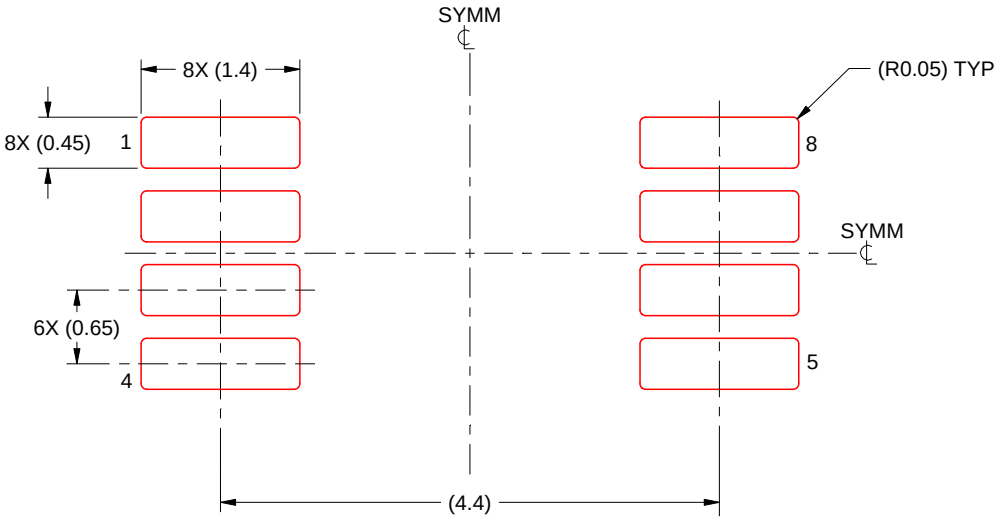
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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