LM3632A Single-Chip Backlight With Bias Power and 1.5-A Flash LED Driver

1 Features

- Drives up to Two Strings of Typically Eight LEDs in Series
  - Integrated Backlight Boost with 29-V Maximum Output Voltage
  - Two Low-Side Constant-Current LED Drivers with 25-mA Maximum Output Current
- Backlight Efficiency Up to 90%
- 11-Bit Exponential or Linear Dimming
- External PWM Input for CABC Backlight Operation
- LCD Bias Efficiency > 85%
- Programmable Positive LCD bias, 4-V to 6-V, 50-mA Maximum Output Current
- Programmable Negative LCD bias, –4-V to –6-V, 50-mA Maximum Output Current
- 1.5-A Flash LED Boost
- Flash Efficiency > 85%
- 2.7-V to 5-V Input Voltage Range

2 Applications

- Smart Phone LCD Backlighting and Bias
- Small Tablet LCD Backlighting and Bias

3 Description

The LM3632A integrates the WLED drivers for both the backlight of the LCD panel and the camera flash along with the bias power for the LCD panel into one device. The device has all the safety features required in LED drivers with up to 90% efficiency and bias positive/negative power rails achieving 1.5% accuracy. Capable of driving up to 16 backlight LEDs, the device is ideal for small- to medium-size displays. A 1.5-A constant-current LED driver powered by a synchronous boost converter can be used for flash applications. The high-side flash current source allows for grounded cathode LED operation.

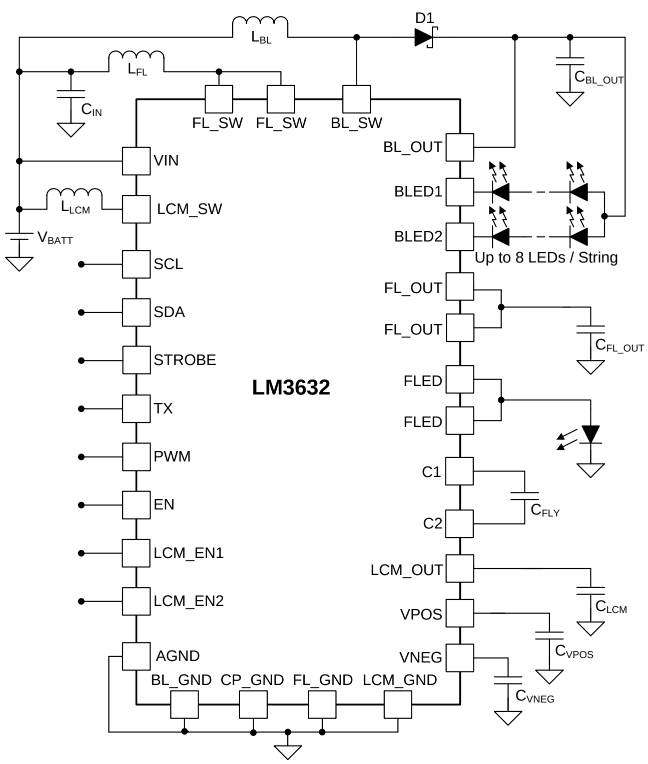
A high level of integration and programmability allows the LM3632A to address a variety of applications without the need for hardware changes.

Device Information(1)

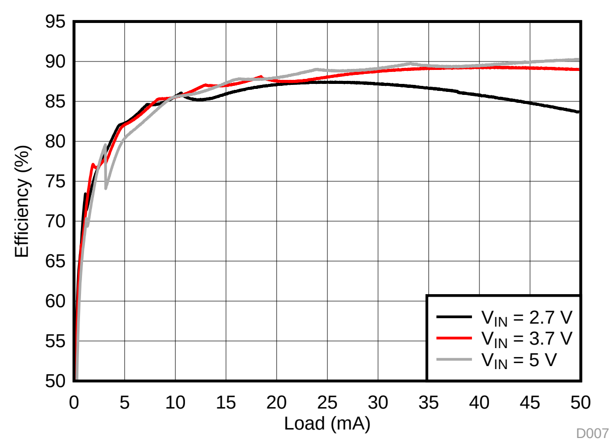
PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3632A	DSBGA (30)	2.47 mm x 2.07 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Backlight Efficiency, 2P7S



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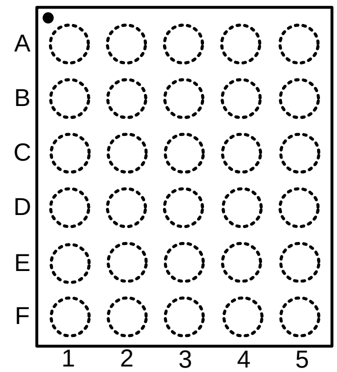
4 Revision History

Changes from Original (April 2015) to Revision A — **Page**

- Added 3 additional graphs for Iq shutdown and standby ... 12
- Added "It is recommended that V_{IN} has risen above 2.7 V before setting EN HIGH and that the EN pin is not forced low while the VNEG output is enabled or before the VNEG output is discharged." to end of *EN Input* subsection. ... 27
- Added *Community Resources* ... 56

5 Pin Configuration and Functions

YFF Package
30-Pin DSBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VPOS	O	Positive LDO output for LCM bias power
A2	LCM_OUT	O	LCM bias boost output voltage
A3	LCM_SW	O	LCM bias boost switch connection
A4	BL_GND	-	Backlight boost ground connection
A5	BL_SW	O	Backlight boost switch connection
B1	LCM_EN2	I	Enable for inverting charge pump output; 300-kΩ internal pulldown resistor between LCM_EN2 and GND.
B2	LCM_EN1	I	Enable for positive LDO output; 300-kΩ internal pulldown resistor between LCM_EN1 and GND.
B3	EN	I	Active high chip enable; 300-kΩ internal pulldown resistor between EN and GND.
B4	LCM_GND	-	LCM bias boost ground connection
B5	BL_OUT	O	Backlight boost output voltage
C1	C1	O	Inverting charge pump flying capacitor positive connection
C2	SDA	I/O	Serial data connection for I^2C- compatible interface
C3	TX	I	Flash interrupt input; 300-kΩ internal pulldown resistor between TX and GND.
C4	AGND	-	Analog ground connection
C5	BLED1	O	Input pin to internal LED current sink 1
D1	CP_GND	-	Inverting charge pump ground connection
D2	SCL	I	Serial clock connection for I^2C- compatible interface
D3	STROBE	I	Flash enable input; 300-kΩ internal pulldown resistor between STROBE and GND.
D4	PWM	I	PWM input for CABC current control; 300-kΩ internal pulldown resistor between PWM and GND.
D5	BLED2	O	Input pin to internal LED current sink 2
E1	C2	O	Inverting charge pump flying capacitor negative connection
E2	FLED	O	High-side current source output for flash LED
E3	FL_OUT	O	Flash boost output voltage
E4	FL_SW	O	Flash boost switch connection
E5	VIN	I	Input voltage connection
F1	VNEG	O	Inverting charge pump output voltage
F2	FLED	O	High-side current source output for flash LED
F3	FL_OUT	O	Flash boost output voltage
F4	FL_SW	O	Flash boost switch connection
F5	FL_GND	-	Flash boost ground connection

6 Specifications

6.1 Absolute Maximum Ratings[1]

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage on VIN, FL_SW, FL_OUT, FLED, EN, LCM_EN1, LCM_EN2, PWM, STROBE, TX, SCL, SDA	–0.3	6	V
Voltage on LCM_SW, LCM_OUT, VPOS, C1	–0.3	7	V
Voltage on VNEG, C2	–7	0.3	V
Voltage on BL_SW, BL_VOUT, BLED1, BLED2	–0.3	30	V
Continuous power dissipation		Internally limited	
Maximum junction temperature, $T_{J(MAX)}$		150	°C
Storage temperature, T_{stg}	–45	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

	MIN	MAX	UNIT
Input voltage, V_{IN}	2.7	5	V
Operating ambient temperature, T_A [1]	–40	85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC[1]		LM3632A YFF (DSBGA) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.6	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.7 V, V_{VPOS} = 5.5 V, V_{VNEG} = –5.4 V, V_{LCM_OUT} = 6 V.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION							
I_{SD}	Shutdown current	EN = 0			1	4	µA
I_Q	Quiescent current, device not switching	EN = V_{IN}, LCD bias boost disabled			2	10	µA
I_{LCD_EN}		LCD bias boost enabled, no-load			0.5		mA
DEVICE PROTECTION							
TSD	Thermal shutdown				140		°C
BACKLIGHT LED CURRENT SINKS							
I_{LED_MAX}	Maximum output current in BLED1/2	2.7 V ≤ V_{IN} ≤ 5 V, linear or exponential mode			25		mA
I_{LED_MIN}	Minimum output current in BLED1/2	2.7 V ≤ V_{IN} ≤ 5 V, linear or exponential mode			50		µA
I_{ACCU}	LED current accuracy(1)	2.7 V ≤ V_{IN} ≤ 5 V, 50 µA ≤ I_{LED} ≤ 25 mA, linear or exponential mode		-3%	0.1%	3%	
I_{MATCH}	LED1 to LED2 current matching(1)	2.7 V ≤ V_{IN} ≤ 5 V, 300 µA ≤ I_{LED} ≤ 25 mA, linear or exponential mode		-2%	0.1%	2%	
BACKLIGHT BOOST CONVERTER							
V_{OVP_BL}	Backlight boost output overvoltage protection	2.7 V ≤ V_{IN} ≤ 5 V, 29 V option		28	28.75	29.5	V
Efficiency	Typical efficiency(2)	I_{LED} = 5 mA/string, V_{IN} = 3.7 V (2 x 7 LEDs), (P_{OUT}/P_{IN})			87%		
V_{HR}	Regulated current sink headroom voltage	I_{LED} = 25 mA			250		mV
		I_{LED} = 5 mA			100		mV
V_{HR_MIN}	Current sink minimum headroom voltage	I_{LED} = 95% of nominal, I_{LED} = 5 mA			30		mV
R_{DSON}	NMOS switch on resistance	I_{SW} = 100 mA			0.25		Ω
I_{CL}	NMOS switch current limit	2.7 V ≤ V_{IN} ≤ 5 V		900	1000	1100	mA
$f_{SW\_BLBOOST}$	Switching frequency	2.7 V ≤ V_{IN} ≤ 5 V	500-kHz mode	450	500	550	kHz
			1-MHz mode	900	1000	1100	kHz
D_{MAX}	Maximum duty cycle				94%		
LCM BIAS BOOST CONVERTER							
V_{OVP_LCM}	LCM bias boost output overvoltage protection	2.7 V ≤ V_{IN} ≤ 5 V			7		V
f_{SW_LCMBST}	Switching frequency (3)	2.7 V ≤ V_{IN} ≤ 5 V			2500		kHz
V_{LCM_OUT}	Bias boost output voltage range			4.5		6.4	V
	Output voltage step size				50		mV
	Peak-to-peak ripple voltage (3)	I_{LOAD} = 5 mA & 50 mA, C_{BST} = 10 µF			50		mVpp
	LCM_OUT line transient response (3)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz, 12.5 % duty, I_{LOAD} = 5 mA, C_{IN} = 10 µF		–50	±25	50	mV
	LCM_OUT load transient response (3)	Load current step 0 mA to 100 mA, $T_{RISE/FALL}$ = 100 mA/µs, C_{IN} = 10 µF		–150		150	mV
I_{CL_LCMBST}	Valley current limit				1000		mA

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the device (BLED1 and BLED2), the following is determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of both outputs (AVG). Matching number is calculated: $(I_{LED1} – I_{LED2})/(I_{LED1} + I_{LED2})$. The typical specification provided is the most likely norm of the matching figure of all parts. Note that some manufacturers have different definitions in use.
(2) Typical value only for information.
(3) Limits set by characterization and/or simulation only.

Electrical Characteristics (continued)

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.7 V, V_{VPOS} = 5.5 V, V_{VNEG} = –5.4 V, V_{LCM_OUT} = 6 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_LCMBST}	High-side MOSFET on resistance	V_{IN} = V_{GS} = 5 V, T_A = 25°C		170		mΩ
	Low-side MOSFET on Resistance	V_{IN} = V_{GS} = 5 V, T_A = 25°C		290		mΩ
EFF_{LCMBST}	Efficiency (2)	V_{LCM_OUT} = 6 V, 5 mA < I_{LCMBST} < 100 mA		92%		
t_{ST_LCMBST}	Start-up time (LCM_OUT), V_{LCM_OUT} = 10% to 90% (3)	C_{LCM_BST} = 10 µF			1000	µs
DISPLAY BIAS POSITIVE OUTPUT (VPOS)						
V_{VPOS}	Programmable output voltage range		4		6	V
	Output voltage step size			50		mV
	Output voltage accuracy	Output voltage = 5.4 V	–1.5%		1.5%	
	VPOS line transient response (3)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz, I_{LOAD} = 25 mA, C_{IN} = 10 µF	–50		50	mV
	VPOS load transient response (3)	0 to 50 mA load transient, C_{VPOS} = 10 µF	–50		50	mV
	DC load regulation (3)	0 mA ≤ I_{VPOS} ≤ 50 mA			20	mV
I_{MAX_VPOS}	Maximum output current			50		mA
I_{CL_VPOS}	Output current limit			80		mA
$I_{RUSH\_PK\_VPOS}$	Peak start-up inrush current (3)	V_{LCM_OUT} = 6.3 V, V_{POS} = 5.8 V, C_{VPOS} = 10 µF			250	mA
V_{DO_VPOS}	VPOS dropout voltage (4)	I_{VPOS} = 50 mA, V_{VPOS} = 5.5 V			100	mV
t_{ST_VPOS}	Start-up time VPOS, V_{VPOS} = 10% to 90% (3)	C_{VPOS} = 10 µF, 500-µs setting		500		µs
		C_{VPOS} = 10 µF, 800-µs setting		800		µs
R_{PD_VPOS}	Output pull-down resistor (VPOS)	VPOS disabled	30	80	110	Ω
DISPLAY BIAS NEGATIVE OUTPUT (VNEG)						
V_{OVP_VNEG}	LCM bias negative charge-pump output overvoltage protection	Below V_{VNEG} output voltage target		–250		mV
V_{SHORT_VNEG}	LCM bias negative charge-pump output short circuit protection	VNEG to CP_GND		–750		mV
V_{VNEG}	Programmable output voltage range		–6		–4	V
	Output voltage step size			50		mV
	Output accuracy	Output voltage = –5.4 V	–1.5%		1.5%	
	Peak-to-peak ripple voltage (3)	I_{LOAD} = 5 mA & 50 mA, C_{VNEG} = 10 µF		60		mVpp
	VNEG line transient response (3)	V_{IN} + 500 mVp-p AC square wave, 100 mV/µs 200 Hz, 12.5% duty at 5 mA	–50	±25	50	mV
	VNEG load transient response (3)	0 to 50 mA load transient, $T_{RISE/FALL}$ = 1 µs, C_{VNEG} = 10 µF			100	mV
	Efficiency (2)	V_{IN} = 3.7 V, V_{LCM_OUT} = 5.8 V, V_{VNEG} = –5.4 V, I_{VNEG} > 5 mA		92%		
I_{MAX_VNEG}	Maximum output current (3)	V_{IN} = 3.7 V, V_{LCM_OUT} = 5.8 V, V_{VNEG} = –5.4 V		50		mA
I_{CL_VNEG}	Output current limit (3)			75		mA

(4) V_{IN_VPOS} – V_{VPOS} when V_{VPOS} has dropped 100 mV below target.

Electrical Characteristics (continued)

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.7 V, V_{VPOS} = 5.5 V, V_{VNEG} = –5.4 V, V_{LCM_OUT} = 6 V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_VNEG}	Charge FET pump on resistance	Q1		350		mΩ
		Q2		400		
		Q3		400		
t_{ST_VNEG}	Start-up time (V_{VNEG}), V_{VNEG} = 10% to 90%(3)	V_{VNEG} = –6 V, C_{VNEG} = 10 µF		1		ms
R_{PU_VNEG}	Output pullup resistor, VNEG(3)	VNEG Disabled, V_{LCM_OUT} > 4.8 V		20	40	Ω
FLASH DRIVER BOOST						
I_{LED}	Current source accuracy	1.5-A flash, V_{FL_OUT} = 4 V	1.4	1.5	1.6	A
V_{OVP}	Output overvoltage protection trip point	ON threshold	4.85	5	5.1	V
		OFF threshold	4.75	4.9	5	
V_{HR}	Current source regulation voltage	1.5-A flash, V_{FL_OUT} = 4 V		275		mV
I_{CL}	Switch current limit		2.45	2.8	3.15	A
			1.65	1.9	2.15	
R_{NMOS}	NMOS switch on resistance	I_{NMOS} = 1 A		80		mΩ
R_{PMOS}	PMOS switch on resistance	I_{PMOS} = 1 A		100		
V_{VINM}	Input voltage monitor trip threshold		2.76	2.9	3.04	V
LOGIC INPUTS (PWM, EN, LCM_EN1, LCM_EN2, SCL, SDA, TX, STROBE)						
V_{IL}	Input logic low		0		0.4	V
V_{IH}	Input logic high		1.2		V_{IN}	V
LOGIC OUTPUTS (SDA)						
V_{OL}	Output logic low	2.7 V ≤ V_{IN} ≤ 5 V, I_{OL} = 3 mA	0		0.4	V
PWM INPUT						
f_{PWM_INPUT}	PWM input frequency(2)		100		20000	Hz
	Minimum PWM ON/OFF time(3)	PWM sampling frequency = 1 MHz	6			µs
		PWM sampling frequency = 4 MHz	1.5			
	PWM timeout(3)	PWM sampling frequency = 1 MHz		25		ms
		PWM sampling frequency = 4 MHz		3		

6.6 I²C Timing Requirements (SDA, SCL) (1)

Over operating free-air temperature range (unless otherwise noted)(see Figure 1).

		MIN	NOM	MAX	UNIT
f_{SCL}	Clock frequency			400	kHz
1	Hold time (repeated) START condition	0.6			µs
2	Clock low time	1.3			µs
3	Clock high time	600			ns
4	Set-up time for a repeated START condition	600			ns
5	Data hold time	50			ns
6	Data set-up time	100			ns
7	Rise time of SDA and SCL	$20 + 0.1C_b$		300	ns
8	Fall time of SDA and SCL	$15 + 0.1C_b$		300	ns
9	Set-Up time between a STOP and a START condition	1.3			µs
C_b	Capacitive load for each bus line	10		200	pF

(1) Limits set by characterization and/or simulation only.

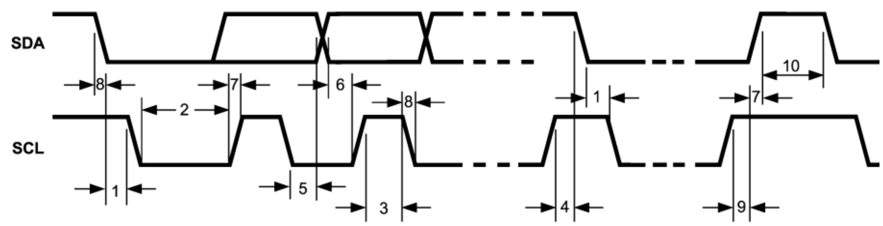


Figure 1. I²C Timing Parameters

6.7 Typical Characteristics

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

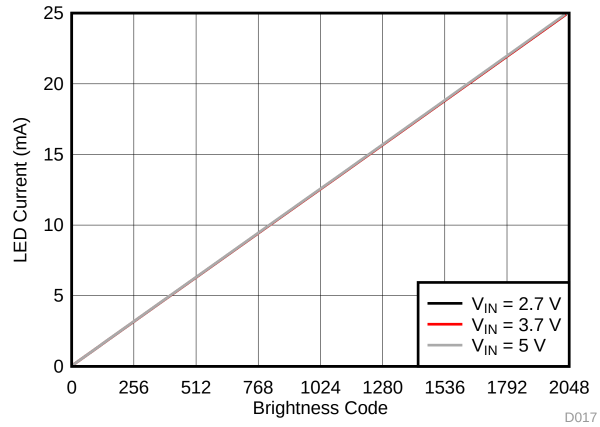


Figure 2. Backlight LED Current, Linear Control

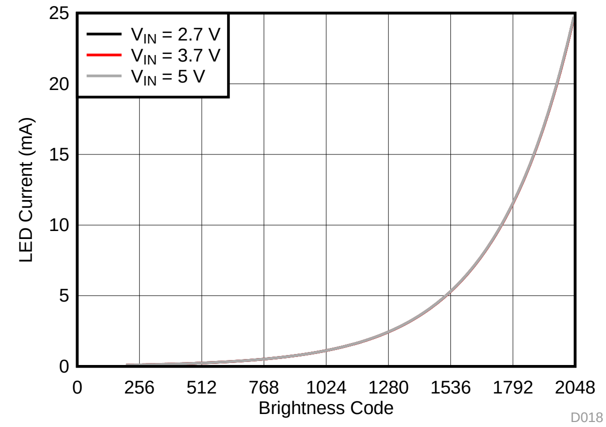
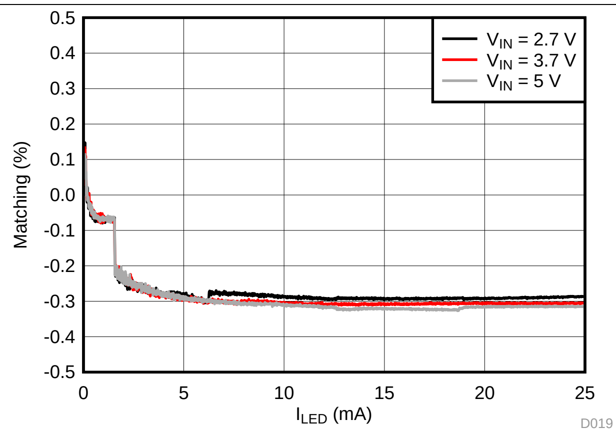
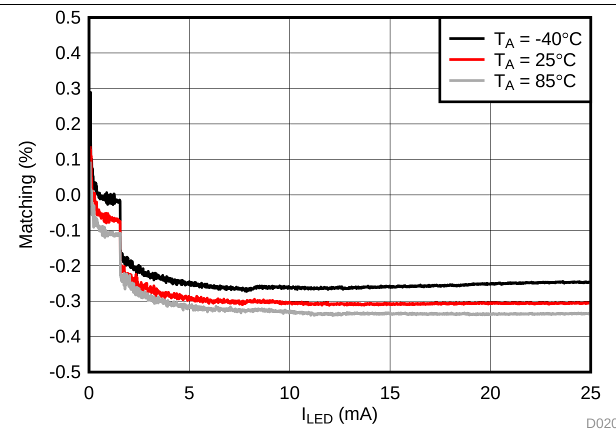


Figure 3. Backlight LED Current, Exponential Control



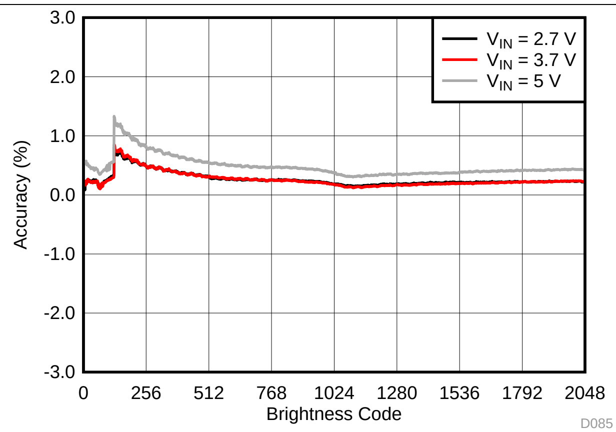
2p6s LEDs

Figure 4. Backlight LED Current Matching



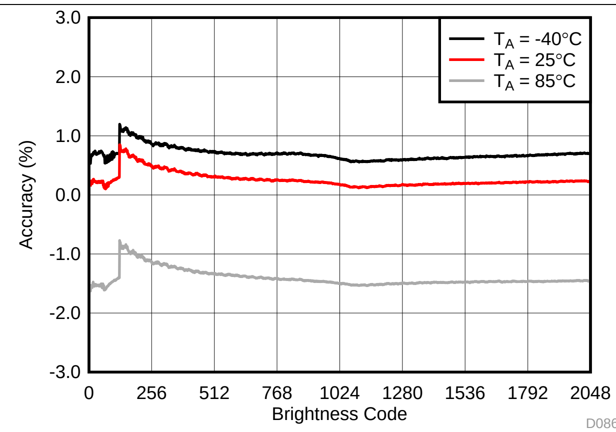
2p6s LEDs

Figure 5. Backlight LED Current Matching



2p6s LEDs

Figure 6. Backlight LED Current Accuracy



2p6s LEDs

Figure 7. Backlight LED Current Accuracy

Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

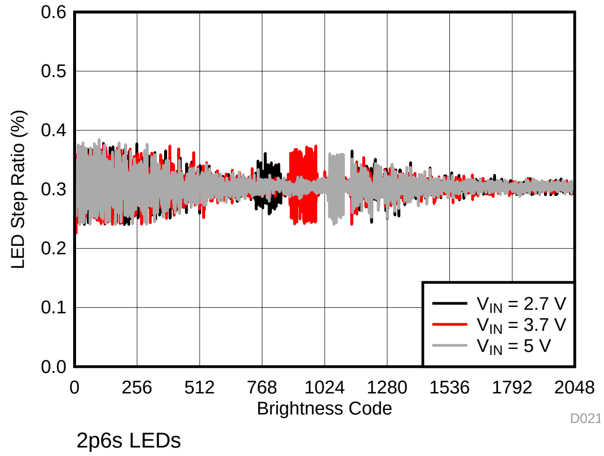


Figure 8. Backlight LED Current-Step Ratio

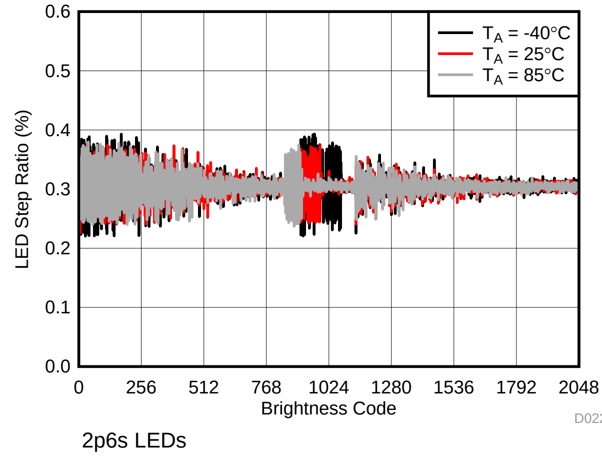


Figure 9. Backlight LED Current-Step Ratio

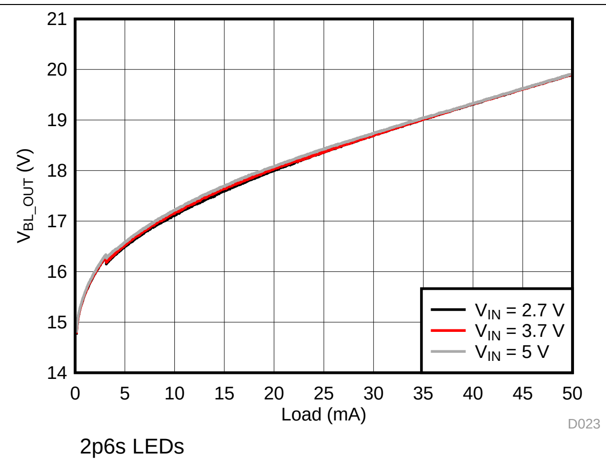


Figure 10. Backlight Boost Voltage

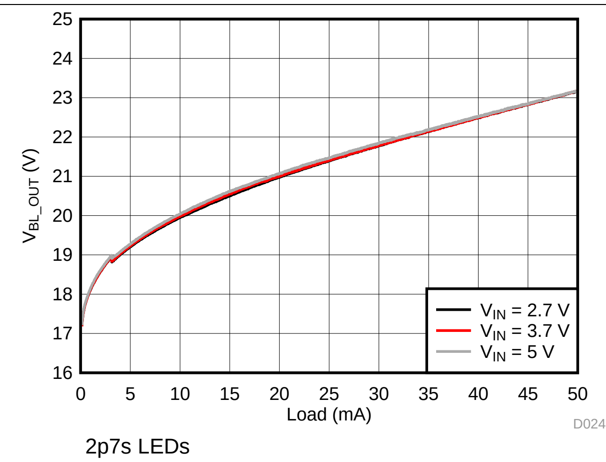


Figure 11. Backlight Boost Voltage

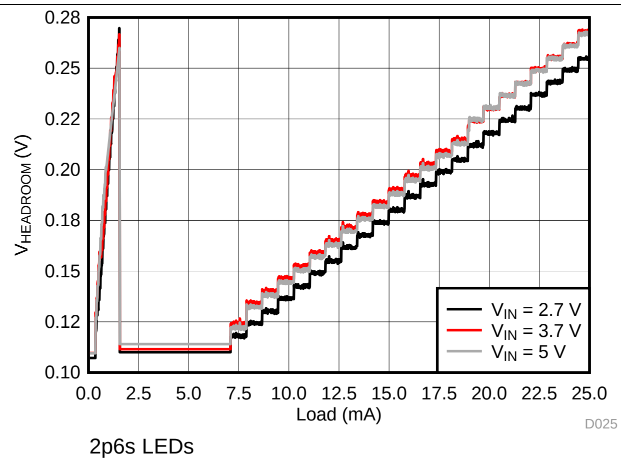


Figure 12. Backlight Headroom Voltage

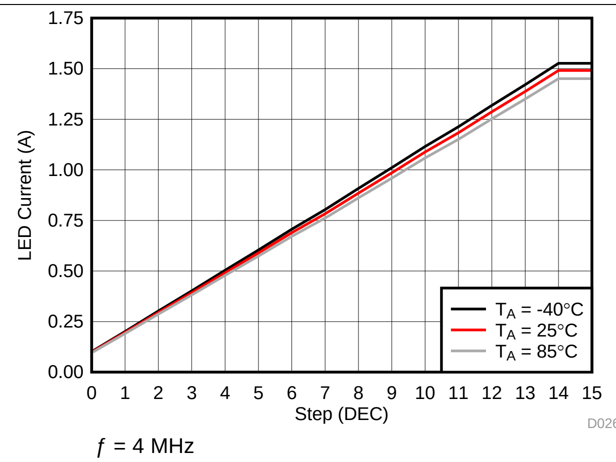
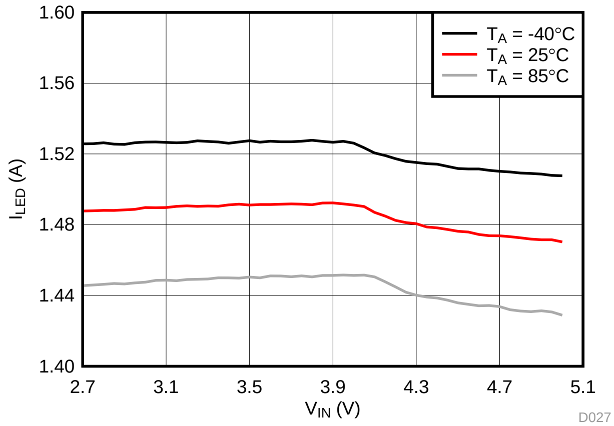


Figure 13. Flash LED Current

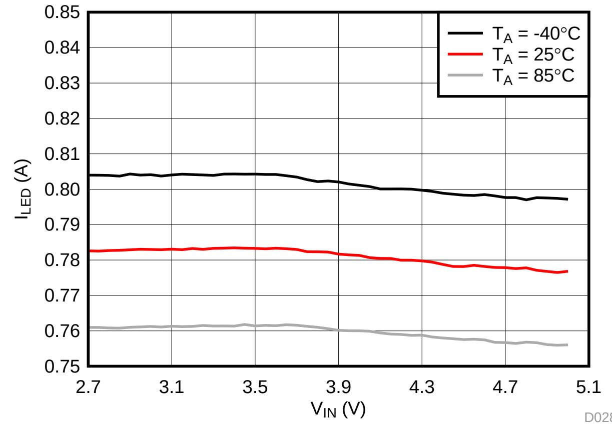
Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.



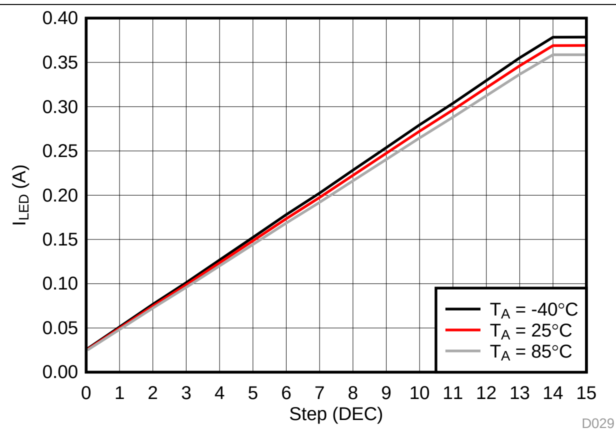
I_{FLED} = 1.5 A *f* = 4 MHz

Figure 14. Flash LED Current



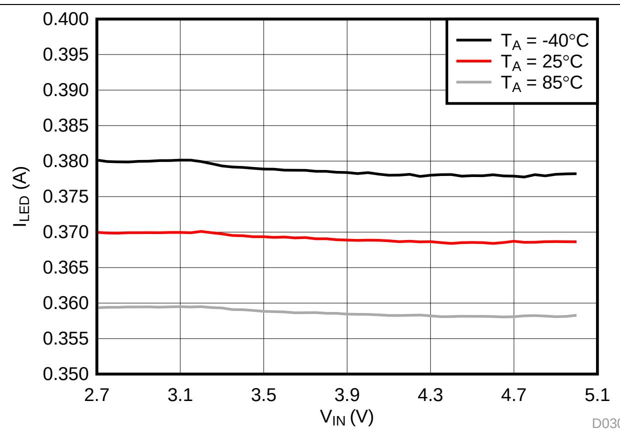
I_{FLED} = 0.8 A f = 4 MHz

Figure 15. Flash LED Current



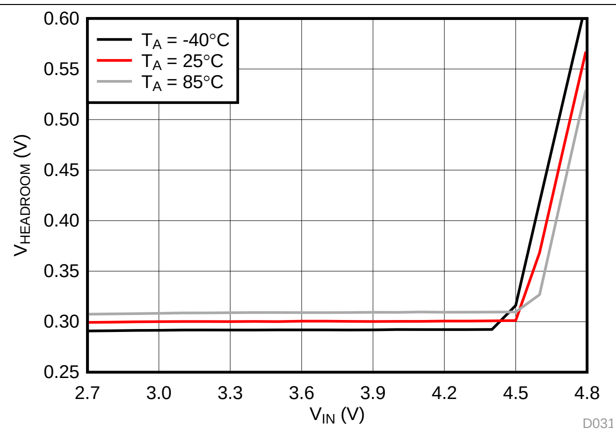
f = 4MHz

Figure 16. Torch LED Current



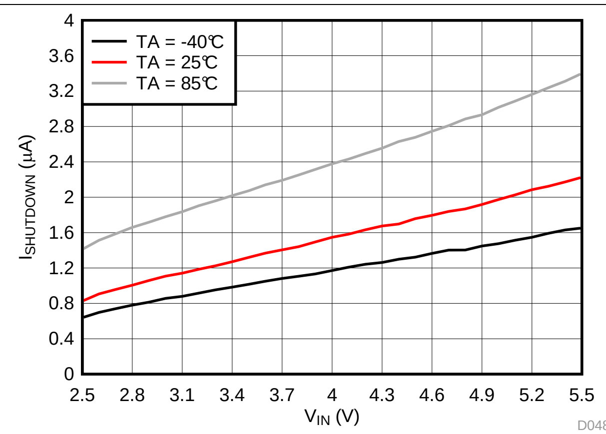
I_{FLED} = 375 mA *f* = 4 MHz

Figure 17. Torch LED Current



I_{FLED} = 1.5 A *f* = 4 MHz V_{FLED} = 4 V

Figure 18. Flash Headroom Voltage



V_{EN} = 0 V I2C = 0 V

Figure 19. Iq Shutdown

Typical Characteristics (continued)

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted.

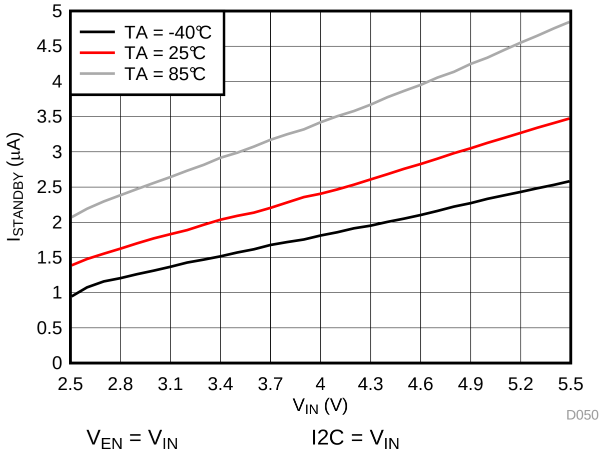


Figure 20. Iq Standby

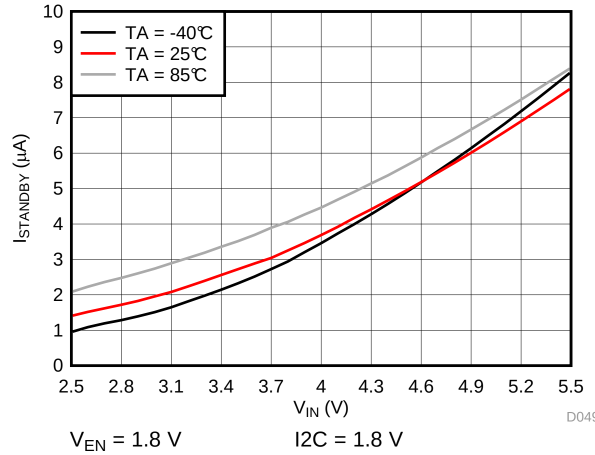


Figure 21. Iq Standby

7 Detailed Description

7.1 Overview

The LM3632A is a single-chip complete backlight, LCM power and flash solution. The device operates over the 2.7-V to 5-V input voltage range.

The LM3632A can drive up to two LED strings with up to 8 LEDs each (up to 28 V typical), with a maximum of 25 mA per string. The power for the LED strings comes from a integrated asynchronous backlight boost converter with two selectable switching frequencies to optimize performance or solution area. LED current is regulated by two low-headroom current sinks. Automatic voltage scaling adjusts the output voltage of the backlight boost converter to minimize the LED driver headroom voltage. The 11-bit LED current is set via an I^2C interface, via a logic level PWM input, or a combination of both.

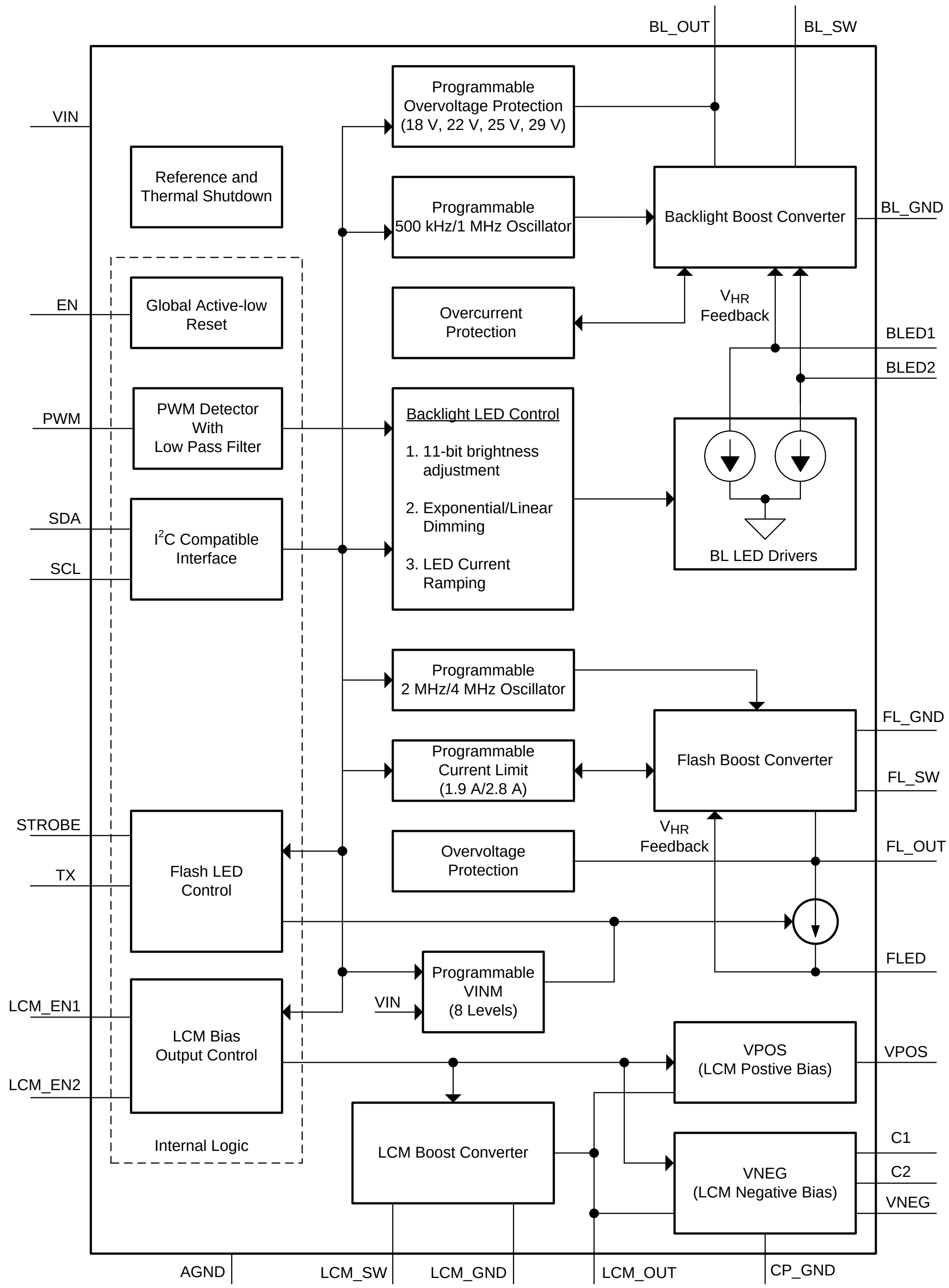
The LCM bias power portion of the LM3632A consists of a synchronous LCM bias boost converter, inverting charge pump, and an integrated LDO. The LCM positive bias voltage V_{POS} (up to 6 V) is post-regulated from the LCM bias boost converter output voltage. The LCM negative bias voltage V_{NEG} (down to –6 V) is generated from the LCM bias boost converter output using a regulated inverting charge pump.

The flash driver consists of a synchronous boost converter and a 1.5-A constant current LED driver. The high-side current source allows for grounded cathode LED operation providing flash current up to 1.5 A. An adaptive regulation method ensures the current source remains in regulation and maximizes efficiency.

The LM3632A flexible control interface consists of an EN active low reset input, LCM_EN1 and LCM_EN2 inputs for V_{POS} and V_{NEG} enable control, PWM input for content adaptive backlight control (CABC), a TX flash interrupt input, and an I^2C-compatible interface.

Additionally, there are two flag registers with flag and status bits. The user can read back these registers and determine if a fault or warning message has been generated.

7.2 Functional Block Diagram



7.3 Features Description

7.3.1 Backlight

The backlight is enabled if the BL_EN bit (bit[0] in reg[0x0A]) is set to ‘1’, at least one of the backlight sink outputs is enabled (bit[3] and/or bit[4] in reg[0x0A]), and the brightness value is different than 0. When the brightness value is 0 or the BL_EN bit is ‘0’, the backlight is disabled.

7.3.1.1 Brightness Control

Brightness can be controlled either by the I^2C brightness register or a combination of the external PWM control and the I^2C brightness register. The backlight truth table is shown in Table 1.

When controlling brightness through I^2C, registers 0x04 and 0x05 are used. Registers 0x04 and 0x05 hold the 11-bit brightness data. Register 0x04 contains the 3 LSBs, and register 0x05 contains the 8 MSBs. The LED current transitions to the new level after a write is done to register 0x05.

When controlling brightness through I^2C, setting the brightness value to '0' shuts down the backlight. When controlling the brightness with PWM input, if PWM input is low for a certain period of time (25 ms typ.), the backlight shuts down. When using the combination of a PWM input and the I^2C register, either option shuts down the backlight.

Table 1. Backlight Truth Table

EN PIN	BL_EN 0x0A[0]	BLED1_EN 0x0A[4]	BLED2_EN 0x0A[3]	PWM_EN 0x09[6]	ACTION
0	X	X	X	X	Shutdown
1	0	X	X	X	Standby
1	1	0	0	X	Bias enable
1	1	1	0	0	BLED1 ramp to target current
1	1	0	1	0	BLED1 & BLED2 ramp-to-target current
1	1	1	1	0	BLED1 & BLED2 ramp-to-target current
1	1	1	0	1	BLED1 ramp to (target current × PWM duty cycle)
1	1	0	1	1	BLED1 & BLED2 ramp to (target current × PWM duty cycle)
1	1	1	1	1	BLED1 & BLED2 ramp to (target current × PWM duty cycle)

7.3.1.1.1 LED Current with PWM Disabled

When LED brightness is controlled from the I^2C brightness registers, the 11-bit brightness data directly controls the LED current in BLED1 and BLED2. LED mapping can be selected as either linear or exponential. When this mode is selected, setting the PWM input to 0 does not disable the backlight.

With exponential mapping the 11-bit code-to-current response is approximated by the equation:

$$I_{LED} = 50\ \mu A \times 1.003040572^{I2C\ BRGT\ CODE}\ \text{(for codes > 0)} \quad (1)$$

Equation 1 is valid for I^2C brightness codes between 1 and 2047. Code 0 disables the backlight. The Code-to-LED current response realizes a 0.304% change in LED current per LSB of brightness code.

Figure 22 and Figure 23 detail the exponential response of the LED current vs. brightness code. Figure 22 shows the response on a linear Y axis while Figure 23 shows the response on a log Y axis to show the low current levels at the lower codes.

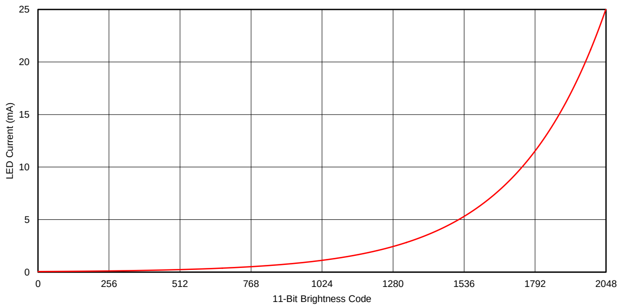


Figure 22. Exponential Response of LED Current vs Brightness Code

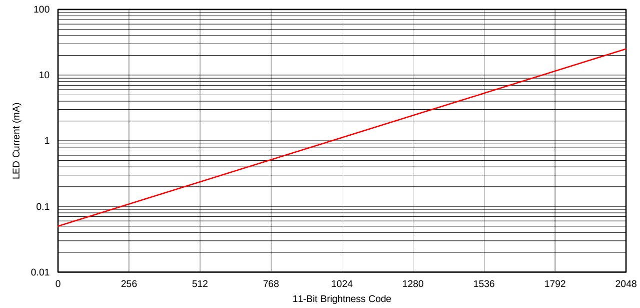


Figure 23. Response of LED Current vs Brightness Code on a Log Y Axis

With linear mapping the 11-bit code to current response is approximated by the equation:

$$I_{LED} = 37.8055\ \mu A + 12.1945\ \mu A \times \text{I2C BRGT CODE (for codes > 0)} \quad (2)$$

Equation 2 is valid for codes between 1 and 2047. Code 0 disables the backlight.

7.3.1.1.2 LED Current with PWM Enabled

When LED brightness is controlled with the combination of I^2C register and the PWM duty cycle, the multiplication result of I^2C register value and PWM duty cycle controls the LED current in BLED1 and BLED2. LED mapping can be selected as either linear or exponential.

With exponential mapping the multiplication result-to-current response is approximated by the equation:

$$I_{LED} = 50\ \mu A \times 1.003040572^{\text{I2C BRGT CODE} \times \text{PWM D/C}} \quad (3)$$

Equation 3 is valid for brightness values other than 0. Brightness value 0 (PWM D/C or I2C BRGT CODE) disables the backlight.

With linear mapping the PWM duty cycle-to-current response is approximated by the equation:

$$I_{LED} = 37.8055\ \mu A + (12.1945\ \mu A \times \text{I2C BRGT CODE} \times \text{PWM D/C}) \quad (4)$$

Equation 4 is valid for brightness values other than 0. Brightness value 0 (PWM D/C or I2C BRGT CODE) disables the backlight.

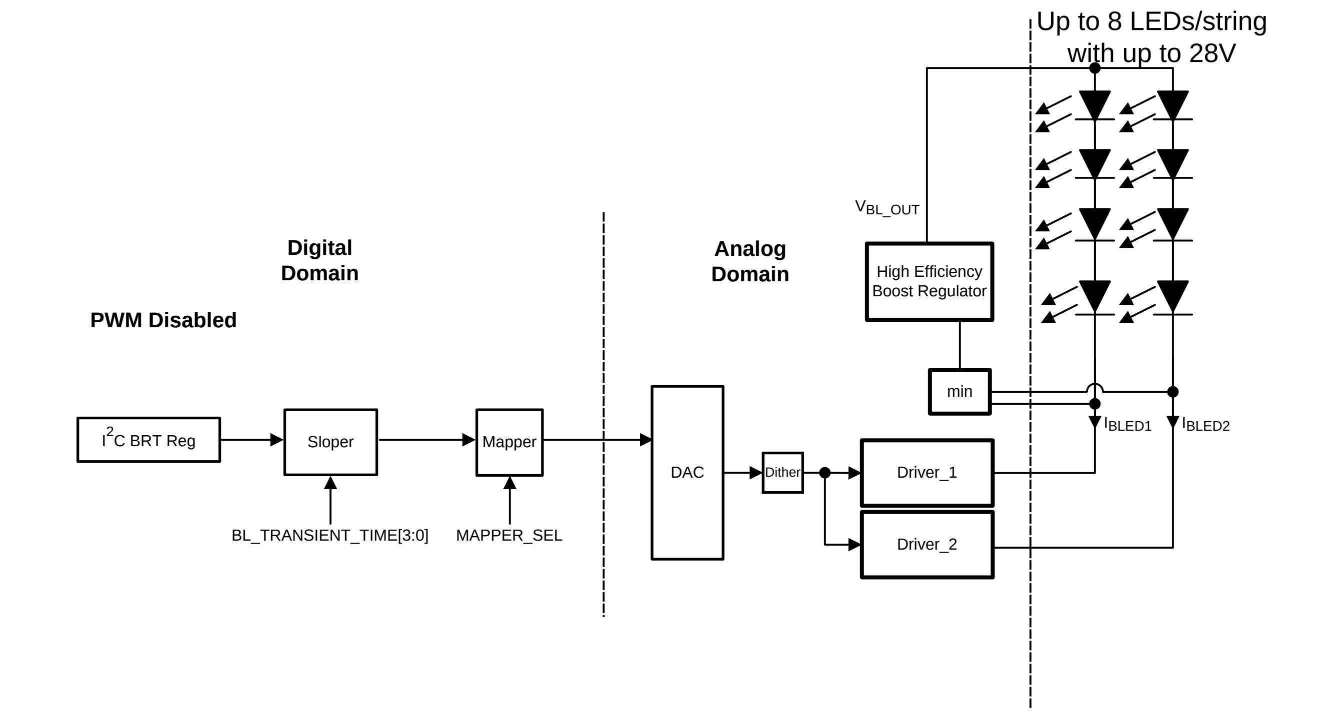


Figure 24. Brightness Control with PWM Bit Disabled

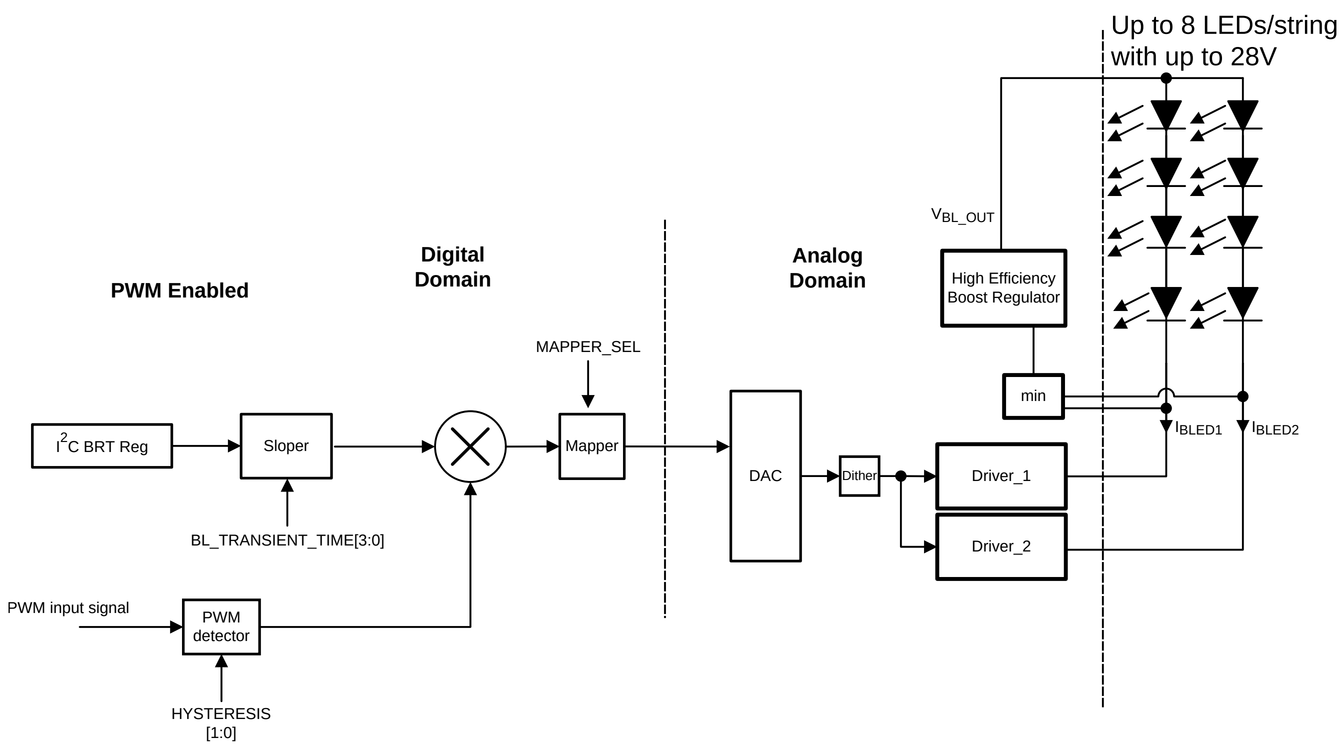


Figure 25. Brightness Control with PWM Bit Enabled

7.3.1.2 Sloper

The sloper smooths the transition from one brightness value to another. Slope time can be adjusted from 0 ms to 8000 ms with BL_TRANS[3:0] bits (see Table 9 for details). Transient time is used for sloping up and down. Transient time always remains the same regardless of the amount of change in brightness.

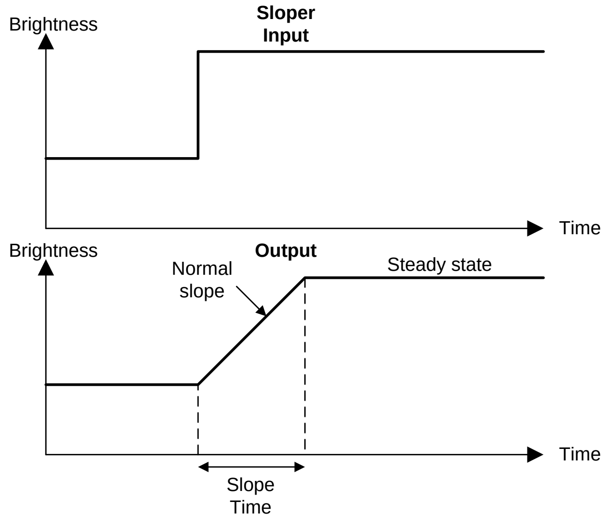


Figure 26. Sloper

7.3.1.3 Mapper

The mapper block maps the digital word set for the LED driver into current code. The user can select whether the mapping is exponential or linear with the BLED_MAP bit, register 0x02 bit[4].

Exponential control is tailored to the response of the human eye such that the perceived change in brightness during ramp up or ramp down is linear.

7.3.1.4 PWM Input

The PWM detector block measures the duty cycle in the PWM pin. The PWM period is measured from the rising edge to the next rising edge. PWM polarity can be changed with bit PWM_CONFIG, register 0x02 bit[3]. The sample rate for the PWM input can be set to 1 MHz or 4 MHz with bit PWM_FREQ, register 0x03 bit[2]. The choice of sample rate depends on three factors:

1. Required PWM resolution (input duty cycle to brightness code, with 11 bits max)
2. PWM input frequency
3. Efficiency

The PWM input block timeout is 25 ms for 1-MHz sampling frequency and 3 ms for 4-MHz sampling frequency, measured from the last rising edge. This should be taken into account for 0% and 100% brightness settings (for setting 100% brightness, the high level of PWM input signal should be greater than the PWM input timeout) and for selecting the minimum PWM input signal frequency.

7.3.1.5 PWM Minimum On/Off Time

The minimum PWM input signal allowed for low and high pulse width is 6 µs for 1-MHz sampling frequency and 1.5 µs for 4-MHz sampling frequency. This should be taken into account when selecting the PWM input signal frequency and maximum or minimum duty cycle. For example, if the PWM input signal frequency is 2 kHz (500 µs) and the 4-MHz sampling frequency is used, the maximum allowed on-time is: (500 – 1.5) µs = 498.5 µs. The maximum duty cycle allowed is 100 × (498.5/500) = 99.7%. By comparison, following similar calculations, with a PWM input signal frequency of 20 kHz the maximum allowed duty cycle is 97%.

NOTE

If the Minimum Off Time requirement is violated, there may be a range of duty cycle values in which flickering of the LEDs may occur or the LEDs may turn off completely. As the duty cycle increases farther and approaches 100%, the LEDs will turn on at full brightness level. This is due to the algorithm used by the device to detect 100% duty cycle in conjunction with the minimum low pulse width requirement discussed in this section. To avoid LED flickering and/or the LEDs turning off at high PWM duty cycles, the PWM Minimum On/Off Time requirement should be met.

7.3.1.6 PWM Resolution and Input Frequency Range

The PWM input resolution depends on the input signal frequency. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code, the input PWM duty cycle must be ≥ 11 bits, and the PWM sample period ($1/f_{SAMPLE}$) must be smaller than the minimum PWM input pulse width. Figure 27 shows the possible brightness code resolutions based on the input PWM frequency. The minimum recommended PWM frequency is 100 Hz, and maximum recommended PWM frequency is 20 kHz.

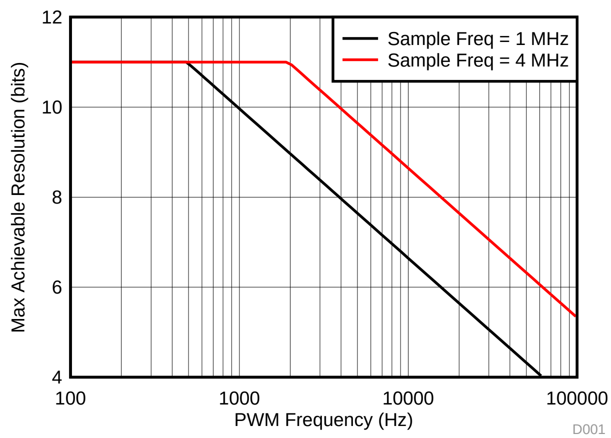


Figure 27. PWM Resolution and PWM Input Frequency

7.3.1.7 PWM Hysteresis

To prevent jitter in the input PWM signal from feeding through the PWM path and causing oscillations in the LED current, the LM3632A offers 4 programmable PWM hysteresis settings. Hysteresis works by forcing a specific number of 11-bit LSB code transitions to occur in the input duty cycle before the LED current changes. Table 9 describes the hysteresis. Hysteresis only applies during the change in direction of brightness currents. Once the change in direction has taken place, the PWM input must overcome the required LSB(s) of the hysteresis setting before the brightness change takes effect. Once the initial hysteresis has been overcome and the direction in brightness change remains the same, the PWM-to-current response changes with no hysteresis. Hysteresis is selected with the PWM_HYST bits, register 0x03 bits[1:0]. Changing the hysteresis value is recommended when PWM input frequency increases.

7.3.1.8 PWM Timeout

The LM3632A PWM timeout feature turns off the backlight boost output when the PWM input is enabled and there is no PWM pulse detected. The timeout duration depends on the PWM sample rate setting and defines the minimum supported PWM input frequency. Table 2 summarizes the sample rate, timeout, and minimum supported PWM frequency.

Table 2. PWM Timeout and Minimum Supported PWM Frequency vs PWM Sample Rate

SAMPLE RATE	TIMEOUT	MINIMUM SUPPORTED PWM FREQUENCY
1 MHz	25 msec	48 Hz
4 MHz	3 msec	400 Hz

7.3.1.9 Backlight Boost Converter

The high voltage required by the LED strings is generated with an asynchronous backlight boost converter. An adaptive voltage control loop automatically adjusts the output voltage based on the voltage over the LED drivers BLED1 and BLED2.

The LM3632A has two switching frequency modes, 500 kHz and 1 MHz. These are set via the BL_FREQ Select bit, register 0x03 bit[7]. Operation in low-frequency mode results in better efficiency at lighter load currents due to the decreased switching losses. Operation in high-frequency mode gives better efficiency at higher load currents due to the reduced inductor current ripple and the resulting lower conduction losses in the MOSFETs and inductor.

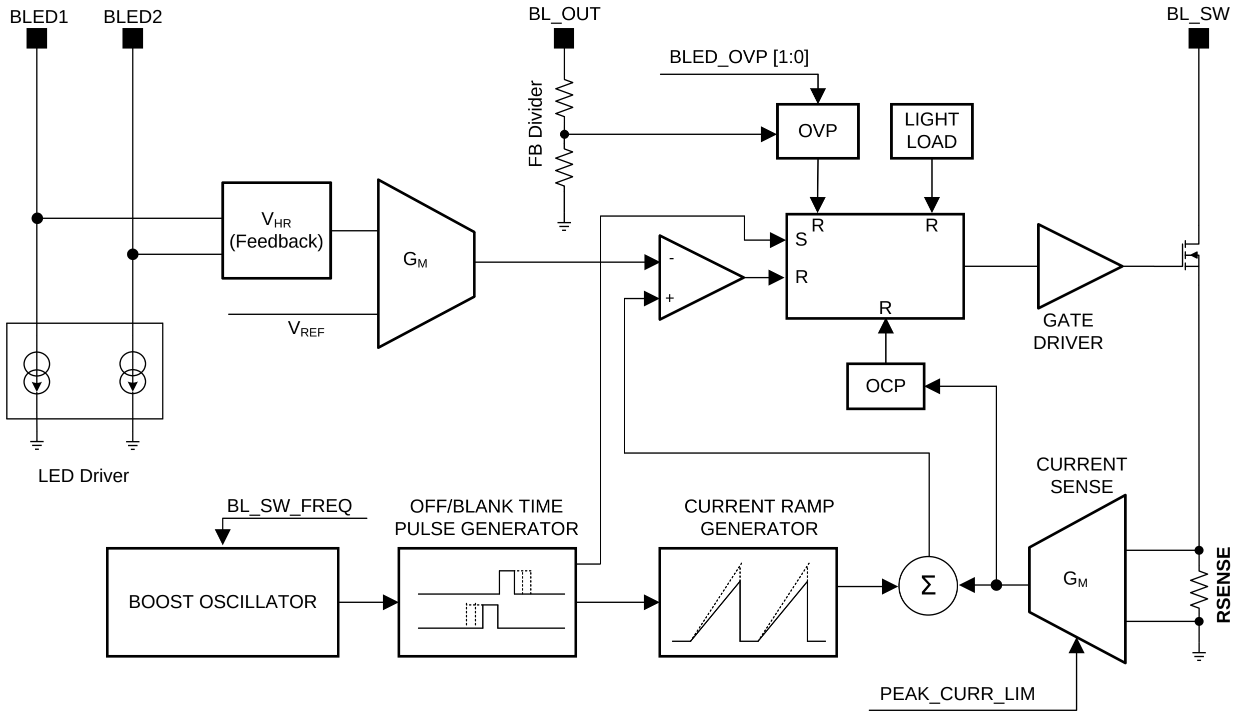


Figure 28. Backlight Boost Block Diagram

7.3.1.9.1 Headroom Voltage

In order to optimize efficiency, the LED driver-regulated headroom voltage (V_{HR}) changes with the programmed LED current. This allows for increased solution efficiency as the dropout voltage of the LED driver changes. Furthermore, in order to ensure that both current sinks remain in regulation when there is a mismatch in string voltages, the minimum headroom voltage between V_{BLED1} and V_{BLED2} becomes the regulation point for the boost converter. For example, if the LEDs connected to BLED1 require 25 V at the programmed current, and the LEDs connected to BLED2 require 25.5 V at the programmed current, the voltage at BLED1 is V_{HR} + 0.5 V, and the voltage at BLED2 is V_{HR}. In other words, the cathode of the highest voltage LED string becomes the boost output regulation point.

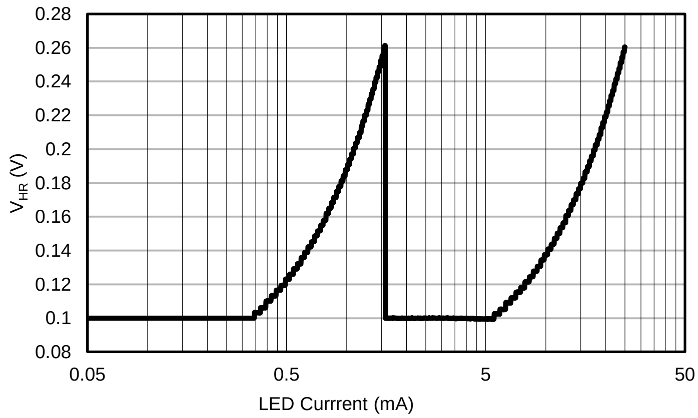


Figure 29. Regulated Headroom vs LED Current

7.3.1.9.2 Backlight Protection and Faults

7.3.1.9.2.1 Overvoltage Protection (OVP) and Open-Load Fault Protection

The LM3632A provides an OVP that monitors the LED boost output voltage (V_{BL_OUT}) and protects BL_OUT and BL_SW from exceeding safe operating voltages. The OVP threshold can be set to 18 V, 22 V, 25 V or 29 V with register 0x02 bits[7:5]. Once an OVP event has been detected, the BL_OVP flag is set in the Flags1 register, and the subsequent behavior depends on the state of bit BL_OVP_SET in the Enable Register: If BL_OVP_SET is set to '0', as soon as V_{BL_OUT} falls below the backlight OVP threshold, the LM3632A begins switching again. If BL_OVP_SET is set to '1' and the device detects three occurrences of V_{BL_OUT} > V_{OVP_BL} while any of the enabled current sink headroom voltages drops below 40 mV, the BL_OVP flag is set, the Backlight Enable bit is cleared, and the LM3632A enters standby mode. When the device is shut down due to a BL_OVP fault the Flags1 register must be read back before the device can be reenabled.

7.3.1.9.2.2 Overcurrent Protection (OCP) and Overcurrent Protection Flag

The LM3632A has an OCP threshold of 1 A. The OCP threshold is a cycle-by-cycle current limit detected in the low-side NFET. Once the threshold is reached, the NFET turns off for the remainder of the switching period. If enough overcurrent events occur, the BL_OCP flag (register 0x10 bit[0]) is set. The flag can be cleared upon a readback of register 0x10. To avoid transient conditions from inadvertently setting the BL_OCP flag, a pulse density counter monitors BL_OCP events over a 128-µs time window. If 8 consecutive 128-µs windows of at least 2 OCP events are detected, the BL_OCP flag is set.

7.3.2 LCM Bias

7.3.2.1 Display Bias Boost Converter (V_{VPOS}, V_{VNEG})

A single high-efficiency boost converter provides a positive voltage rail, V_{LCM_OUT}, which serves as the power rail for the LCM VPOS and VNEG outputs.

- The V_{VPOS} output LDO has a programmable range from 4 V up to 6 V with 50-mV steps and can supply up to 50 mA.
- The V_{VNEG} output is generated from a regulated, inverting charge pump and has an adjustable range of –6 V up to –4 V with 50-mV steps and a maximum load of 50 mA.

Boost voltage also has a programmable range from 4.5 V up to 6.4 V with 50-mV steps. Please refer to Table 19, Table 20 and Table 21 for V_{LCM_OUT}, V_{VPOS} and V_{VNEG} voltage settings. When selecting a suitable boost-output voltage, the following estimation can be used: $V_{LCM\_OUT} = \max(V_{VPOS}, |V_{VNEG}|) + V_{HR}$, where V_{HR} = 300 mV for lower currents and 400 mV for higher currents. When the device input voltage (V_{IN}) is greater than the programmed LCM boost output voltage, the boost voltage goes to V_{IN} + 100 mV. V_{VPOS}, and V_{VNEG} voltage settings cannot be changed while they are enabled. While the V_{LCM_OUT} target changes immediately upon a register write, V_{VPOS} and V_{VNEG} register setting targets take effect only after the outputs are disabled and re-enabled.

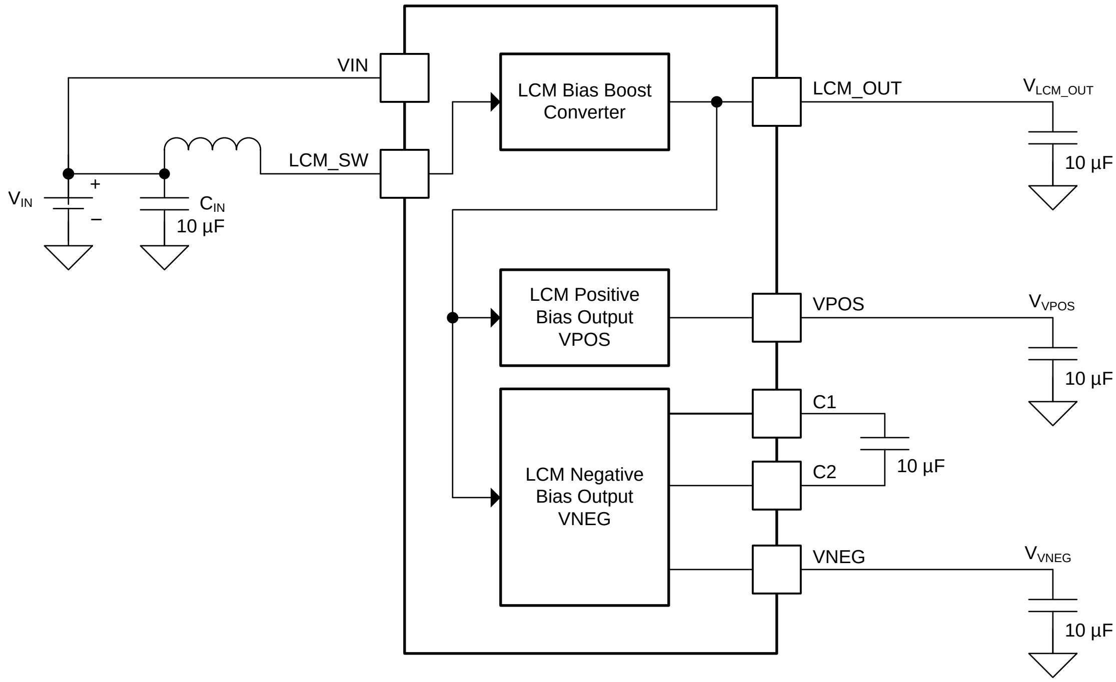


Figure 30. LCM Boost Block Diagram

The LCM Bias outputs can be controlled either by pins LCM_EN1 and LCM_EN2 or register bits VPOS_EN and VNEG_EN, register 0x0C bits[2:1]. Setting bit EXT_EN, register 0x0C bit[0], to '0' allows pins LCM_EN1 and LCM_EN2 to control VPOS and VNEG, respectively, while setting this bit to '1' yields control to bits VPOS_EN and VNEG_EN. Refer to Table 3 for LCM bias control information.

Table 3. LCM Bias Truth Table

EN PIN	LCM_EN2 PIN	LCM_EN1 PIN	EXT_EN 0x0C[0]	VNEG_EN 0x0C[1]	VPOS_EN 0x0C[2]	AUTO_SEQ 0x0C[5]	WAKE-UP 0x0C[7]	ACTION
0	X	X	X	X	X	X	X	Shutdown
1	0	0	1	X	X	X	0	Standby
1	0	1	1	X	X	X	0	External VPOS
1	1	0	1	X	X	X	0	External VNEG
1	1	1	1	X	X	0	0	External VPOS and VNEG Independent
1	1	1	1	X	X	1	0	External VPOS and VNEG Auto Sequence
1	X	X	0	0	0	X	0	Standby
1	X	X	0	0	1	X	0	I^2C VPOS
1	X	X	0	1	0	X	0	I^2C VNEG
1	X	X	0	1	1	0	0	I^2C VPOS and VNEG Independent
1	X	X	0	1	1	1	0	I^2C VPOS and VNEG Auto Sequence
1	0	X	X	X	X	X	1	Standby
1	1	X	X	0	0	X	1	Standby
1	1	X	X	0	1	X	1	Wake-up VPOS
1	1	X	X	1	0	X	1	Wake-up VNEG
1	1	X	X	1	1	X	1	Wake-up VPOS and VNEG

7.3.2.2 Auto Sequence Mode

If this mode is selected the LM3632A controls the turn-on and turn-off of VPOS and VNEG as shown in Figure 31.

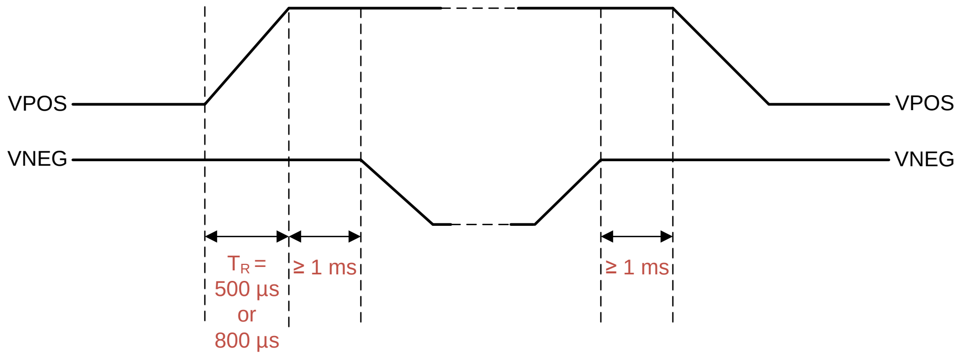


Figure 31. Auto Sequence Timing

7.3.2.3 Wake-up Mode

If Wake-up mode is selected the LM3632A allows on/off control of both VPOS and VNEG with only one external pin (LCM_EN2). Any combination of VPOS, VNEG, or both can be turned on based on the state of bits VPOS_EN and VNEG_EN in register 0x0C. In this mode the internal shutdown timing of the VPOS and VNEG blocks is modified to allow for lower quiescent current in standby mode, therefore reducing the average current consumption during a sequence of on/off events.

7.3.2.4 Active Discharge

An optional active discharge is available for the VPOS and VNEG output rails. An internal switch resistance for this discharge function is implemented on each output rail. The VPOS active discharge function is enabled with register 0x0C bit[4] and the VNEG active discharge with register 0x0C bit[3].

NOTE

To avoid an unsafe operating condition when the active discharge function is enabled, a minimum delay of 1 millisecond needs to be maintained between disabling and re-enabling of the VNEG output.

7.3.2.5 LCM Bias Protection and Faults

The LCM Bias block of the LM3632A provides four protection mechanisms in order to prevent damage to the device. Note that none of these have any effect on backlight or flash operation.

7.3.2.5.1 LCM Overvoltage Protection

The LM3632A provides OVP that monitors the LCM Bias boost output voltage (V_{LCM_OUT}) and protects LCM_OUT and LCM_SW from exceeding safe operating voltages. The OVP threshold is set to 7 V (typical). If an LCM Bias overvoltage condition is detected, the LCM_OVP flag, register 0x10 bit[5], is set. The flag can be cleared with an I^2C read back of the register. An LCM OVP condition will not cause the LCM Bias to shut down; it is a report-only flag.

7.3.2.5.2 VNEG Overvoltage Protection

If the charge-pump voltage goes 250 mV (typical) below its target set-point, the LM3632A provides a mechanism for preventing the voltage from increasing even further and damaging the device and sets the VNEG_OVP flag, register 0x10 bit[4]. The flag can be cleared with an I^2C readback of the register. A VNEG OVP condition will not cause the charge pump to shut down; it is a report-only flag.

NOTE

The VNEG_OVP flag may get set during VNEG start-up under light load and low VNEG voltage settings due to VNEG voltage undershoot. After the flag is cleared via register read back, the LM3632A detects VNEG OVP conditions properly.

7.3.2.5.3 VPOS Short Circuit Protection

If the current at VPOS exceeds 80 mA (typical), the LM3632A sets the VPOS_SHORT flag, register 0x10 bit[3]. A readback of register 0x10 is required to clear the flag. A VPOS_SHORT condition will not cause the LCM Bias to shut down; it is a report-only flag.

7.3.2.5.4 VNEG Short Circuit Protection

If the voltage at VNEG goes within 750 mV (typical) from ground, the LM3632A sets the VNEG_SHORT flag, register 0x10 bit[2]. A readback of register 0x10 is required to clear the flag. A VNEG_SHORT condition will not cause the LCM Bias to shut down; it is a report-only flag.

7.3.3 Flash

7.3.3.1 Flash Boost Converter

The LM3632A incorporates a high-efficiency synchronous current-mode PWM boost converter that switches and boosts the output to maintain at least V_{HR} across the flash current source (FLED) over the 2.7-V to 5.5-V input voltage range. The flash boost has two switching frequency modes, 2-MHz and 4-MHz. These are set via the FL_FREQ Select bits, register 0x07 bits[7:6].

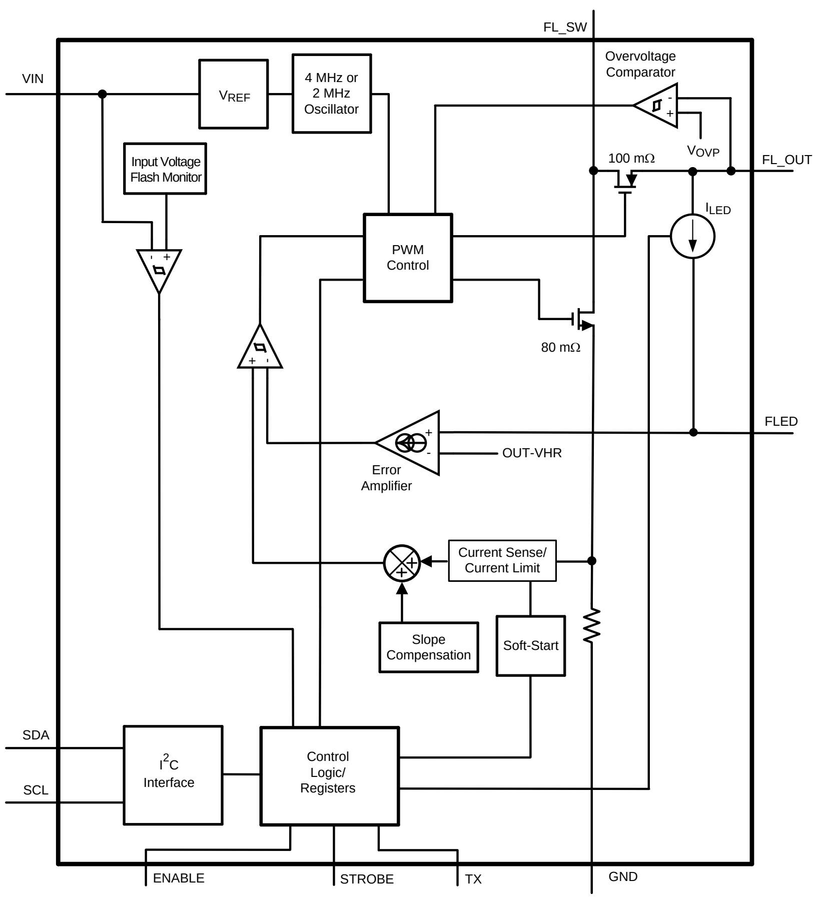


Figure 32. Flash Boost Block Diagram

7.3.3.2 Start-Up (Enabling The Device)

The flash LED output (FLED) can be enabled in flash or torch mode with the Enable Register and the STROBE pin. The state of bit STROBE_EN, register 0x09 bit[4], determines if the FLED output is enabled by bit[1] of register 0x0A or the STROBE pin. Table 4 contains the details for flash operation control. While a positive edge is required at the STROBE pin in order to initiate a Torch or Flash event, the STROBE pin is level sensitive. That means that the event is terminated as soon as the STROBE pin transitions low.

Table 4. Flash Truth Table

EN PIN	STROBE_EN 0x09[4]	STROBE PIN	FLASH_EN 0x0A[1]	FLASH_MODE 0x0A[2]	ACTION
0	X	X	X	X	Shutdown
1	0	X	0	X	Standby
1	0	X	1	0	Int Torch
1	0	X	1	1	Int Flash
1	1	0	0	X	Standby
1	1	0	1	X	Standby
1	1	pos edge	0	X	Standby
1	1	pos edge	1	0	Ext Torch
1	1	pos edge	1	1	Ext Flash

On start-up, when V_{OUT} is less than V_{IN} the internal synchronous PFET turns on as a current source and delivers 200 mA (typical) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typical) the current source turns on. At turn-on the current source steps through each flash or torch level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the V_{IN} supply.

7.3.3.3 Pass Mode

The LM3632A flash boost starts up in pass mode and stays there until boost mode is needed to maintain regulation. If the voltage difference between V_{FL_OUT} and V_{FLED} falls below V_{HR}, the device switches to boost mode. In pass mode the boost converter does not switch, and the synchronous PFET turns fully on bringing V_{FL_OUT} up to $V_{IN} - I_{FLED} \times$ RPMOS. In pass mode the inductor current is not limited by the peak current limit.

7.3.3.4 Flash Mode

In flash mode, the LED current source (FLED) provides 15 target current levels from 100 mA to 1500 mA in 100 mA increments. The flash currents are adjusted via register 0x06 (see Table 12 for details). Once the flash sequence is activated the current source (FLED) ramps up to the programmed flash current by stepping through all current steps until the programmed current is reached. The headroom in the current source is regulated to provide 100 mA to 1.5 A to the output. Whether the device is enabled in flash mode through the Enable Register or through the STROBE pin, the Flash Enable bit in the Enable Register is cleared at the completion of the flash event and needs to be re-written in order to perform the next internal or external flash event.

7.3.3.5 Torch Mode

In torch mode, the LED current source (FLED) provides 15 target current levels from 25 mA to 375 mA in 25-mA increments. The torch currents are adjusted via register 0x06 (see Table 12 for details). Once the torch sequence is activated the current source (FLED) ramps up to the programmed Torch current by stepping through all current steps until the programmed current is reached. Torch mode is not affected by Flash Timeout or by a TX Interrupt event.

7.3.3.6 Power Amplifier Synchronization (TX)

The TX pin is a Power Amplifier Synchronization input. This is designed to reduce the flash FLED current and thus limit the battery current during high battery-current conditions such as PA transmit events. When the LM3632A is engaged in a flash event, and the TX pin is pulled high, the FLED current is forced into torch mode at the programmed torch current setting. If the TX pin is then pulled low before the flash pulse terminates, the FLED current returns to the previous flash current level. At the end of the flash time-out, whether the TX pin is high or low, the FLED current is turned off.

7.3.3.7 VIN Monitor

The LM3632A has the ability to adjust the flash current based upon the voltage level present at the VIN pin. The adjustable VINM threshold ranges from 2.6 V to 3.3 V in 100-mV steps. The Flags1 Register (0x0B) has the fault flag set when the input voltage crosses the VINM value. Additionally, the VINM threshold sets the input voltage boundary that forces the device to either transition into torch mode at the programmed torch current setting or turn off the FLED current for the remaining flash duration. This decision is made based on the status of bit VINM_MODE, register 0x09 bit[1]. In order to re-enable the LM3632A in torch or flash mode the VINM flag has to be cleared. If the VINM flag is tripped during flash current ramp-up, and VINM mode is set to torch, the FLED current is reduced not to the torch current setting but to the same percentage of the last flash current that was reached during fash current ramp-up. For example, if the flash current setting is 1 A, the torch current setting is 100 mA and the maximum flash current that was reached before the VINM threshold was crossed is 700 mA, the device will transition the flash current to 70 mA (70% of 100 mA).

7.3.3.8 Flash Fault Protections

7.3.3.8.1 Fault Operation

If the LM3632A enters a fault condition during flash, the device sets the appropriate flag in the Flags1 and Flags2 Registers (0x0B and 0x10) and places the flash block into standby by clearing the FLASH_EN bit in the Enable Register. The flash block remains in shutdown until an I^2C read of the Flag Registers is completed. Upon clearing the flags/faults, flash can be restarted. If the fault is still present, the LM3632A re-enters the fault state and enters standby again. Flash faults have no effect on Backlight or LCM control.

7.3.3.8.2 Flash Time-Out

The Flash Time-Out period sets the amount of time that the Flash Current is being sourced from the current source (FLED). The LM3632A has 32 timeout levels ranging from 32 ms to 1024 ms (see Table 13 for more detail). Once a flash event is completed, the FTO flag in Flags1 register (register 0x0B bit[1]) is set. If a flash event is activated via the STROBE pin and STROBE transitions low after the end of the programmed flash timeout, the flash event is terminated at the programmed flash timeout, and the FTO flag is set. If the STROBE pin transitions low before the end of the programmed flash timeout, the flash event is terminated, and the FTO flag is not set.

7.3.3.8.3 Overvoltage Protection (OVP)

The flash output voltage is limited to typically 4.9 V (see V_{OVP} Spec in *Electrical Characteristics*). In situations such as an open FLED, the LM3632A tries to raise the output voltage in order to keep the FLED current at its target value. When V_{FL_OUT} reaches 4.9 V (typical), the overvoltage comparator trips and turns off the internal NFET. When V_{FL_OUT} falls below the V_{OVP} Off threshold, the LM3632A begins switching again. The Flash Enable bit is cleared, and the FLASH_OVP flag is set, when an OVP condition is present for three rising OVP edges. This prevents momentary OVP events from forcing the device to shut down.

7.3.3.8.4 Current Limit

The LM3632A features two selectable flash inductor current limits that are programmable through the I^2C-compatible interface. When the inductor current limit is reached, the device terminates the charging phase of the switching cycle. Switching resumes at the start of the next switching period. If the overcurrent condition persists, the device operates continuously in current limit. Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in pass mode (current does not flow through the NMOS in pass mode). In boost mode or pass mode if V_{FL_OUT} falls below 2.3 V, the device stops switching, and the PFET operates as a current source limiting the current to 200 mA. This prevents damage to the LM3632A and excessive current draw from the battery during output short-circuit conditions. The Flash Enable bit is not cleared upon a current limit event, but the FLASH_OCP flag (register 0x10 bit[1]) is set.

7.3.3.8.5 FLED and/or FL_OUT Short Fault

The FLED short flag (FLED_SHORT) reads back a '1' if the device is active in flash or torch mode and the FLED output experiences a short condition. The flash output short flag (FOUT_SHORT) reads back a '1' if the device is active in flash or torch mode and the flash boost output experiences a short condition. A FLED short condition is determined if the voltage at FLED goes below 500 mV (typical) while the device is in torch or flash mode. There is a deglitch time of 256 µs before the LED Short flag is valid and a deglitch time of 2.048 ms before the FL_OUT Short flag is valid. The FLED Short Fault can only be reset to '0' by removing power to the LM3632A, setting EN to '0', setting the SW RESET bit to a '1', or by reading back the Flags1 Register (0x0B on device). The Flash Enable bit is cleared upon a FLED and/or FL_OUT short fault.

7.3.4 Software RESET

Bit[7] (SWR_RESET) of the Enable Register (0x0A) is a software reset bit. Writing an '1' to this bit resets all I^2C register values to their default values. Once the LM3632A has finished resetting all registers, it auto-clears the SWR_RESET bit.

7.3.5 EN Input

The EN pin is a global hardware enable for the LM3632A. This pin must be pulled to logic HIGH to enable the device and the I^2C-compatible interface. There is a 300-kΩ internal resistor between EN and GND. When this pin is at logic LOW, the LM3632A is placed in shutdown, the I^2C-compatible interface is disabled, and the internal registers are reset to their default state. It is recommended that V_{IN} has risen above 2.7 V before setting EN HIGH and that the EN pin is not forced low while the VNEG output is enabled or before the VNEG output is discharged.

7.3.6 Thermal Shutdown (TSD)

The LM3632A has TSD protection which shuts down the backlight boost, both backlight current sinks, LCM Bias Boost and outputs, inverting charge pump, flash boost, and flash current source when the die temperature reaches or exceeds 140°C (typical). The I^2C interface remains active during a TSD event. If a TSD fault occurs the TSD fault is set, register 0x0B bit[0]. The fault is cleared by an I^2C read of register 0x0B or by toggling the EN pin.

7.4 Device Functional Modes

7.4.1 Modes of Operation

Shutdown: The LM3632A is in shutdown when the EN pin is low.

Standby: After the EN pin is set high the LM3632A goes into standby mode. In standby mode, I^2C writes are allowed but references, bias currents, the oscillator, LCM powers, backlight and flash are all disabled, to keep the quiescent supply current low (2 µA typ.).

Normal mode: All three main blocks of the LM3632A are independently controlled. For enabling each of the blocks in all available modes, see Table 1, Table 3, and Table 4 .

7.5 Programming

7.5.1 I^2C-Compatible Serial Bus Interface

7.5.1.1 Interface Bus Overview

The I^2C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines should be connected to a positive supply via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave, depending whether it generates or receives the serial clock (SCL).

Programming (continued)

7.5.1.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

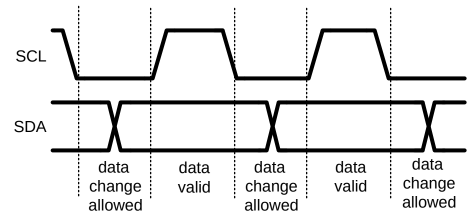


Figure 33. Data Validity

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software), and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

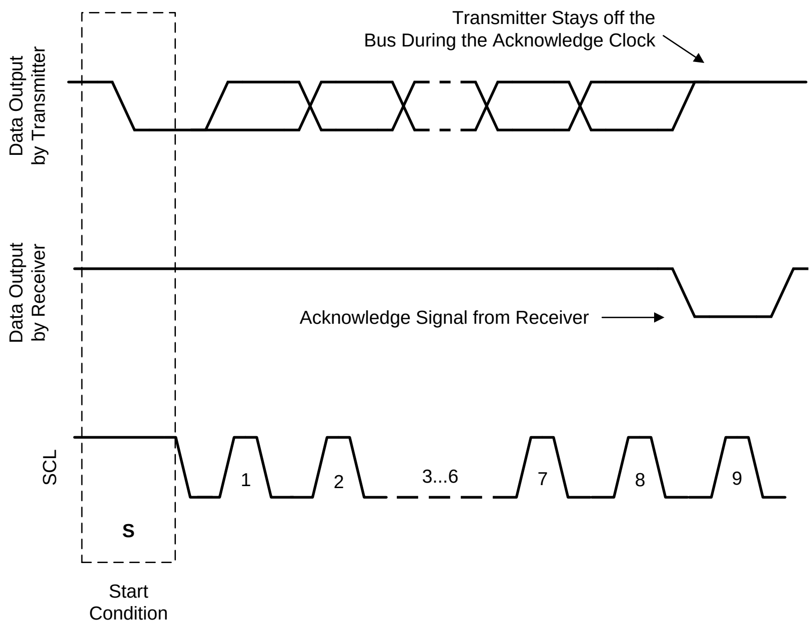


Figure 34. Acknowledge Signal

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy, and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

Programming (continued)

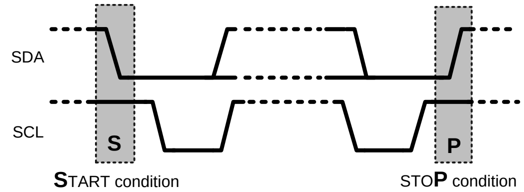


Figure 35. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

7.5.1.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

7.5.1.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

7.5.1.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LM3632A operates as a slave device with the 7-bit address. If an 8-bit address is used for programming, the 8th bit is '1' for read and '0' for write. The 7-bit address for the device is 0x11.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address. The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

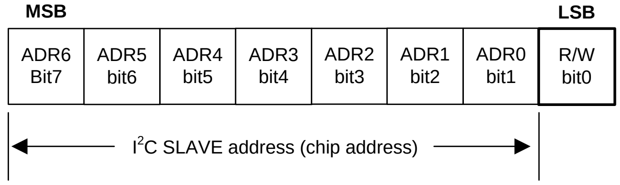


Figure 36. I^{2}C Device Address

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).

Programming (continued)

- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 5. I²C Data Read/Write(1)

	ADDRESS MODE
Data Read	<Start Condition> <Slave Address><r/w =0>[Ack] <Register Addr>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ...additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr>[Ack] <Register Data>[Ack] ...additional writes to subsequent register address possible <Stop Condition>

(1) < > = Data from master, [ ] = Data from slave

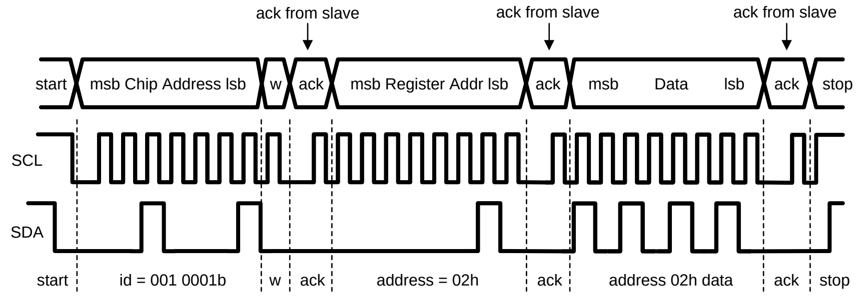


Figure 37. Register Write Format

When a READ function is to be accomplished, a WRITE function must precede the READ function, as show in the Read Cycle waveform.

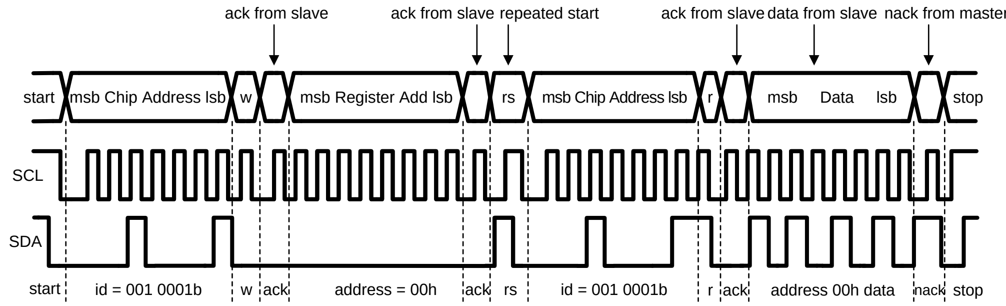


Figure 38. Register Read Format

NOTE

w = write (SDA = 0), r = read (SDA = 1), ack = acknowledge (SDA pulled down by either master or slave), rs = repeated start id = 7-bit chip address

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7.6 Register Maps

Table 6. Register Default Values

I^2C Address	Register Name	Read/Write	Power On/Reset Value
0x01	Revision Register	R	0x09
0x02	Backlight Configuration1 Register	R/W	0x30
0x03	Backlight Configuration2 Register	R/W	0x0D
0x04	LED Brightness LSB Register	R/W	0x07
0x05	LED Brightness MSB Register	R/W	0xFF
0x06	Flash/Torch Current Register	R/W	0x3E
0x07	Flash Configuration Register	R/W	0x2F
0x08	VIN Monitor Register	R/W	0x03
0x09	I/O Control Register	R/W	0x00
0x0A	Enable Register	R/W	0x00
0x0B	Flags1 Register	R	0x00
0x0C	Display Bias Configuration Register	R/W	0x18
0x0D	LCM Boost Bias Register	R/W	0x1E
0x0E	VPOS Bias Register	R/W	0x1E
0x0F	VNEG Bias Register	R/W	0x1C
0x10	Flags2 Register	R	0x00

7.6.1 Revision (Address = 0x01) [reset = 0x09]

Figure 39. Revision Register

7	6	5	4	3	2	1	0
DEV_REV[5]	DEV_REV[4]	DEV_REV[3]	DEV_REV[2]	DEV_REV[1]	DEV_REV[0]	VENDOR[1]	VENDOR[0]
R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	DEV_REV[6:0]	R	000010	
1-0	VENDOR[1:0]	R	01	

7.6.2 Backlight Configuration1 (Address = 0x02) [reset = 0x30]

Figure 40. Backlight Configuration1 Register

7	6	5	4	3	2	1	0
BLED_OVP[2]	BLED_OVP[1]	BLED_OVP[0]	BLED_MAP	PWM_CONFIG	Reserved		
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Backlight Configuration1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	BLED_OVP	R/W	001	Backlight OVP level select 000: 18 V 001: 22 V (Default) 010: 25 V 011: 29 V Note: Codes 100 to 111 also map to 29 V
4	BLED_MAP	R/W	1	Sets the backlight LED mapping mode 0: Exponential 1: Linear (Default)

Table 8. Backlight Configuration1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PWM_CONFIG	R/W	0	Sets the polarity of the PWM input signal 0: Active High PWM Input (default) 1: Active Low PWM Input
2-0	Reserved			

7.6.3 Backlight Configuration2 (Address = 0x03) [reset = 0x0D]

Figure 41. Backlight Configuration2 Register

7	6	5	4	3	2	1	0
BL_FREQ	BL_TRANS[3]	BL_TRANS[2]	BL_TRANS[1]	BL_TRANS[0]	PWM_FREQ	PWM_HYST[1]	PWM_HYST[0]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Backlight Configuration2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BL_FREQ	R/W	0	Sets the backlight boost switch frequency 0: 500 kHz (Default) 1: 1 MHz
6-3	BL_TRANS[3:0]	R/W	001	Controls backlight LED ramping time. The transient time is a constant time that the backlight takes to transition from an existing programmed code to a new programmed code. 0000: 0 0001: 500 µs (Default) 0010: 750 µs 0011: 1 ms 0100: 2 ms 0101: 5 ms 0110: 10 ms 0111: 20 ms 1000: 50 ms 1001: 100 ms 1010: 250 ms 1011: 800 ms 1100: 1 s 1101: 2 s 1110: 4 s 1111: 8 s
2	PWM_FREQ	R/W	1	Sets PWM sampling frequency 0: 1 MHz 1: 4 MHz (Default)
1-0	PWM_HYST[1:0]	R/W	01	Sets the minimum change in PWM input duty cycle that results in a change of backlight LED brightness level 00: 1 bit 01: 2 bits (Default) 10: 4 bits 11: 6 bits

7.6.4 Backlight Brightness LSB (Address = 0x04) [reset = 0x07]

Figure 42. Backlight Brightness LSB Register

7	6	5	4	3	2	1	0
Reserved					BL_BRT_ LSB[2]	BL_BRT_ LSB[1]	BL_BRT_ LSB[0]
					R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Backlight Brightness LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved			
2-0	BL_BRT_LSB[2:0]	R/W	111	Lower 3 bits (LSB's) of brightness code. Concatenated with brightness bits in Register 0x05 (MSB).

7.6.5 Backlight Brightness MSB (Address = 0x05) [reset = 0xFF]

Figure 43. Backlight Brightness MSB Register

7	6	5	4	3	2	1	0
BL_BRT_ MSB[7]	BL_BRT_ MSB[6]	BL_BRT_ MSB[5]	BL_BRT_ MSB[4]	BL_BRT_ MSB[3]	BL_BRT_ MSB[2]	BL_BRT_ MSB[1]	BL_BRT_ MSB[0]
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Backlight Brightness MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BL_BRT_MSB[7:0]	R/W	11111111	Upper 8 bits (MSB's) of backlight brightness code. Concatenated with brightness bits in Register 0x04 (LSB). With linear mapping the 11-bit code to current response is approximated by the equation: I_{LED}=37.8055µA+12.1945µA×I2C_BRGT_CODE (for codes > 0). With exponential mapping the 11-bit code-to-current response is approximated by the equation: I_{LED}=50µA×$1.003040572^{I2C\_BRGT\_CODE}$ (for codes > 0). These equations are valid for I2C brightness codes between 1 and 2047. Code 0 disables the backlight.

7.6.6 Flash/Torch Current (Address = 0x06) [reset = 0x3E]

Figure 44. Flash/Torch Current Register

7	6	5	4	3	2	1	0
TORCH_ BRT[3]	TORCH_ BRT[2]	TORCH_ BRT[1]	TORCH_ BRT[0]	FLASH_ BRT[3]	FLASH_ BRT[2]	FLASH_ BRT[1]	FLASH_ BRT[0]
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Flash/Torch Current Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TORCH_BRT[3:0]	R/W	0011	Sets torch mode current level (25 mA per step) 0000: 25 mA 0001: 50 mA 0010: 75 mA 0011: 100 mA (Default) .... 1101: 350 mA 1110: 375 mA Note: Code 1111 also maps to 375 mA
3-0	FLASH_BRT[3:0]	R/W	1110	Sets flash mode current level (100 mA per step) 0000: 100 mA 0001: 200 mA 0010: 300 mA 0011: 400 mA .... 1101: 1.4 A 1110: 1.5 A (Default) Note: Code 1111 also maps to 1.5 A

7.6.7 Flash Configuration (Address = 0x07) [reset = 0x2F]

Figure 45. Flash Configuration Register

7	6	5	4	3	2	1	0
FL_FREQ[1]	FL_FREQ[0]	FL_ILIMIT	FTO[4]	FTO[3]	FTO[2]	FTO[1]	FTO[0]
R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Flash Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FL_FREQ[1:0]	R/W	00	Sets the flash boost switch frequency 00: 4 MHz (Default) 01: 2 MHz Note: Codes 10 and 11 also map to 2 MHz
5	FL_ILIMIT	R/W	1	Selects the switch current limit level for flash boost 0: 1.9 A 1: 2.8 A (Default)
4-0	FTO[4:0]	R/W	01111	Selects the flash timeout duration (32 ms per step) 00000: 32 ms 00001: 64 ms 00010: 96 ms 00011: 128 ms .... 01110: 480 ms 01111: 512 ms (Default) 10000: 544 ms .... 11110: 992 ms 11111: 1024 ms

7.6.8 VIN Monitor (Address = 0x08) [reset = 0x03]

Figure 46. VIN Monitor Register

7	6	5	4	3	2	1	0
Reserved					VINM[2]	VINM[1]	VINM[0]
					R/W-0	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. VIN Monitor Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved			
2-0	VINM[2:0]	R/W	011	This field sets the VIN Monitor threshold level 000: 2.6 V 001: 2.7 V 010: 2.8 V 011: 2.9 V (Default) 100: 3 V 101: 3.1 V 110: 3.2 V 111: 3.3 V

7.6.9 I/O Control (Address = 0x09) [reset = 0x00]

Figure 47. I/O Control Register

7	6	5	4	3	2	1	0
Reserved	PWM_EN	Reserved	STROBE_EN	Reserved	TX_EN	VINM_MODE	VINM_EN
	R/W-0		R/W-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. I/O Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			
6	PWM_EN	R/W	0	This bit enables and disables the PWM input pin. If enabled, the backlight LED current ramps up to Target_Current*PWM_Duty_Cycle. If disabled, the PWM input is ignored. 0: PWM disabled (Default) 1: PWM enabled
5	Reserved			
4	STROBE_EN	R/W	0	Hardware flash enable 0: STROBE disabled (Default) 1: STROBE enabled
3	Reserved			
2	TX_EN	R/W	0	Flash Interrupt mode enable 0: TX disabled (Default) 1: TX enabled
1	VINM_MODE	R/W	0	Selects the VIN Monitor current reduction level 0: Flash driver returns to standby mode (Default) 1: Flash current reduced to programmed Torch current level
0	VINM_EN	R/W	0	Set this bit to enable VIN Monitor function 0: Disabled (Default) 1: Enabled

7.6.10 Enable (Address = 0x0A) [reset = 0x00]

Figure 48. Enable Register

7	6	5	4	3	2	1	0
SWR_RESET	Reserved	BL_OVP_SET	BLED1_EN	BLED1/2_EN	FLASH_MODE	FLASH_EN	BL_EN
R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWR_RESET	R/W	0	Setting this bit resets all registers to their default values. Bit auto-clears (returns to "0" upon device reset).
6	Reserved	R/W	0	
5	BL_OVP_SET	R/W	0	0: Reports flag if OVP condition detected, but no action taken (Default) 1: OVP causes shutdown
4	BLED1_EN	R/W	0	Backlight sink 1 enable only 0: Disabled (Default) 1: Enabled
3	BLED1/2_EN	R/W	0	Backlight sink 1 and sink 2 enable. Has priority over bit[4] (BLED1_EN). 0: Backlight sink 2 disabled, backlight sink 1 status depends on BLED1_EN bit status (Default) 1: Backlight sink 1 and sink 2 enabled regardless of BLED1_EN bit status
2	FLASH_MODE	R/W	0	Selects Torch or Flash mode for flash LED output 0: Torch (Default) 1: Flash
1	FLASH_EN	R/W	0	Flash LED output enable 0: Disabled (Default) 1: Enabled
0	BL_EN	R/W	0	Backlight output enable 0: Disabled (Default) 1: Enabled

7.6.11 Flags1 (Address = 0x0B) [reset = 0x00]

Figure 49. Flags1 Register

7	6	5	4	3	2	1	0
BL_OVP	FLASH_OVP	FOUT_SHORT	VINM	TX	FLED_SHORT	FTO	TSD
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Flags1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BL_OVP	R	0	Backlight overvoltage protection fault or flag
6	FLASH_OVP	R	0	Flash overvoltage protection fault or flag
5	FOUT_SHORT	R	0	Flash output short fault
4	VINM	R	0	VINM fault or flag
3	TX	R	0	TX Interrupt flag
2	FLED_SHORT	R	0	Flash LED short fault
1	FTO	R	0	Flash timeout flag
0	TSD	R	0	Thermal shutdown fault

7.6.12 Display Bias Configuration (Address = 0x0C) [reset = 0x18]

Figure 50. Display Bias Configuration Register

7	6	5	4	3	2	1	0
WAKE-UP	VPOS_TRANS	AUTOSEQ	VPOS_DISCH	VNEG_DISCH	VPOS_EN	VNEG_EN	EXT_EN
			R/W-1	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Display Bias Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE-UP	R/W	0	Enables wake-up mode 0: Wake-up mode disabled (Default) 1: Wake-up mode enabled
6	VPOS_TRANS	R/W	0	Controls positive display bias voltage (LDO) ramping time 0: 800 µs (Default) 1: 500 µs
5	AUTOSEQ	R/W	0	Enables Auto-sequence 0: Auto-sequence disabled (Default) 1: Auto-sequence enabled
4	VPOS_DISCH	R/W	1	Positive display bias voltage (LDO) active discharge selection 0: Not discharged 1: Active discharge (Default)
3	VNEG_DISCH	R/W	1	Negative display bias voltage (inverting charge pump) active discharge selection 0: Not discharged 1: Active discharge (Default)
2	VPOS_EN	R/W	0	Positive display bias (LDO) enable 0: Disabled (Default) 1: Enabled
1	VNEG_EN	R/W	0	Negative display bias (inverting charge pump) enable 0: Disabled (Default) 1: Enabled
0	EXT_EN	R/W	0	Setting this bit activates pins LCM_EN1 and LCM_EN2 to enable VPOS and VNEG, respectively 0: VPOS and VNEG can only be enabled via bit VPOS_EN and VNEG_EN, respectively (Default) 1: VPOS and VNEG can only be enabled via pin LCM_EN1 and LCM_EN2, respectively

7.6.13 LCM Boost Bias (Address = 0x0D) [reset = 0x1E]

Figure 51. LCM Boost Bias Register

7	6	5	4	3	2	1	0
Reserved		LCM_VBST[5]	LCM_VBST[4]	LCM_VBST[3]	LCM_VBST[2]	LCM_VBST[1]	LCM_VBST[0]
		R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. LCM Boost Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			
5-0	LCM_VBST[5:0]	R/W	011110	Sets the LCM Boost Voltage (50 mV per step) 000000: 4.5 V 000001: 4.55 V 000010: 4.6 V .... 011101: 5.95 V 011110: 6 V (Default) 011111: 6.05 V .... 100101: 6.35 V 100110: 6.4 V Note: Codes 100111 to 111111 map to 6.4V

7.6.14 VPOS Bias (Address = 0x0E) [reset = 0x1E]

Figure 52. VPOS Bias Register

7	6	5	4	3	2	1	0
Reserved		VPOS[5]	VPOS[4]	VPOS[3]	VPOS[2]	VPOS[1]	VPOS[0]
		R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. VPOS Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			
5-0	VPOS[5:0]	R/W	011110	Sets the Positive Display Bias (LDO) Voltage (50 mV per step) 000000: 4 V 000001: 4.05 V 000010: 4.1 V .... 011101: 5.45 V 011110: 5.5 V (Default) 011111: 5.55 V .... 100111: 5.95 V 101000: 6 V Note: Codes 101001 to 111111 map to 6 V

7.6.15 VNEG Bias (Address = 0x0F) [reset = 0x1C]

Figure 53. VNEG Bias Register

7	6	5	4	3	2	1	0
Reserved		VNEG[5]	VNEG[4]	VNEG[3]	VNEG[2]	VNEG[1]	VNEG[0]
		R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. VNEG Bias Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			
5-0	VNEG[5:0]	R/W	011100	Sets the Negative Display Bias (inverting charge pump) Voltage (–50 mV per step) 000000: –4 V 000001: –4.05 V 000010: -4.1 V .... 011011: –5.35 V 011100: –5.4 V (Default) 011101: –5.45 V .... 100111: –5.95 V 101000: –6 V Note: Codes 101001 to 111111 map to –6 V

7.6.16 Flags2 (Address = 0x10) [reset = 0x00]

Figure 54. Flags2 Register

7	6	5	4	3	2	1	0
Reserved		LCM_OVP	VNEG_OVP	VPOS_SHORT	VNEG_SHORT	FLASH_OCP	BL_OCP
		R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Flags2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved			
5	LCM_OVP	R	0	LCM boost overvoltage protection flag
4	VNEG_OVP	R	0	VNEG overvoltage protection flag
3	VPOS_SHORT	R	0	VPOS short circuit protection flag
2	VNEG_SHORT	R	0	VNEG short circuit protection flag
1	FLASH_OCP	R	0	Flash boost output overcurrent protection flag
0	BL_OCP	R	0	Backlight boost overcurrent protection flag

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3632A integrates an LCD backlight driver, LCM positive and negative bias voltage supplies, and a flash driver into a single device. The backlight boost converter generates the high voltage required for the LEDs. The device can drive one or two LED strings with 4 to 8 white LEDs per string. Positive and negative bias voltages are post-regulated from the LCM bias boost output voltage. The flash driver can supply constant current of up to a 1.5 A to the LED output. All three functions are independent of each other and can be enabled using their own dedicated controls.

8.2 Typical Application

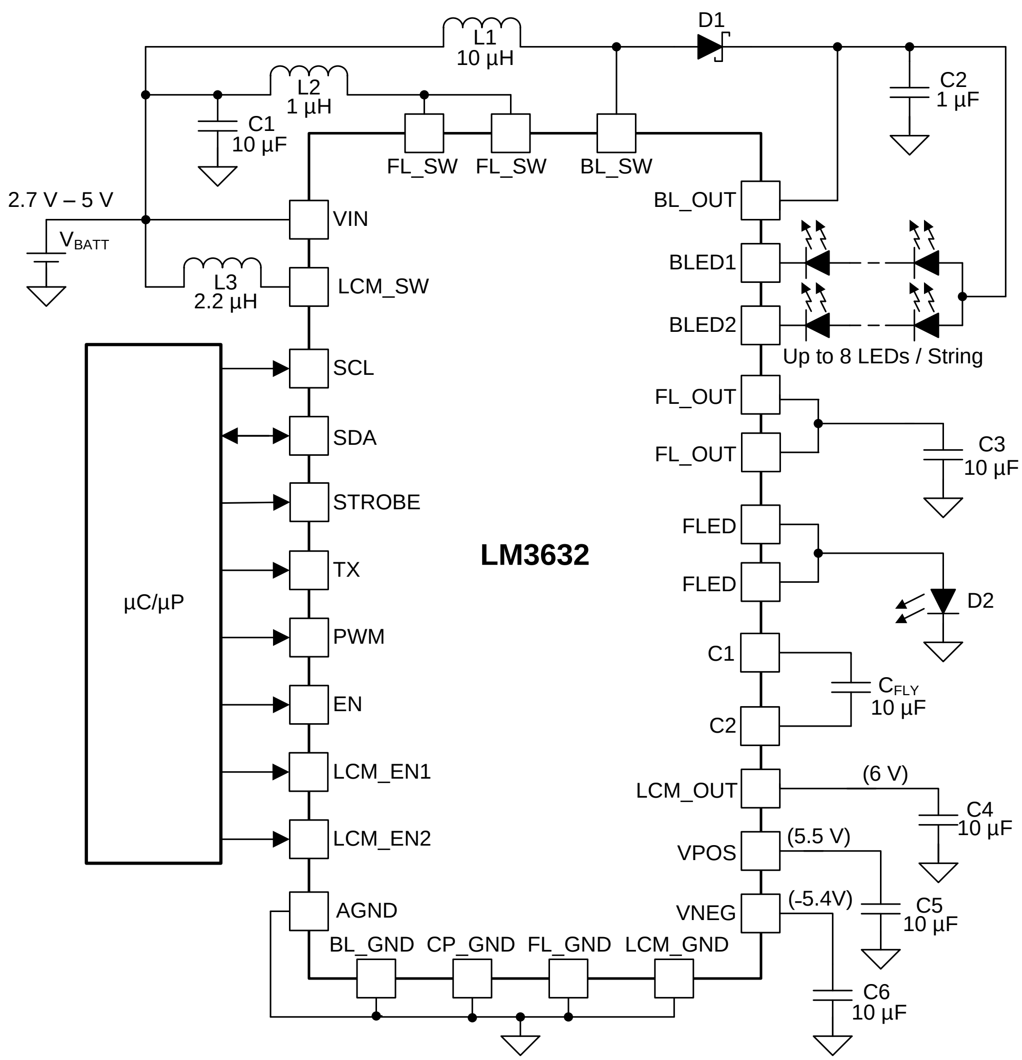


Figure 55. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Example requirements are shown below:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 4.5 V (single Li-Ion cell battery)
Brightness control	I^2C Register
Backlight LED configuration	2 parallel, 6 series
Backlight LED current	max 25 mA / string
Backlight boost maximum voltage	29 V
Backlight boost SW frequency	1 MHz
Backlight boost inductor	10 µH, 1-A saturation current
LCM boost output voltage	6 V
V_{VNEG} output voltage	–5.4 V
V_{VPOS} output voltage	5.5 V
Flash LED current	1.5 A
Torch LED current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 External Components

Table 23 shows examples of external components for the LM3632A. Boost converter output capacitors can be replaced with dual output capacitors of lower capacitance as long as the minimum effective capacitance requirement is met. DC bias effect of the ceramic capacitors must be taken into consideration when choosing the output capacitors. This is especially true for the high output-voltage backlight-boost converter.

Table 23. Recommended External Components

DESIGNATOR (Figure 55)	DESCRIPTION	VALUE	EXAMPLE
C1, C3, C4, C5, C6	Ceramic capacitor	10 µF, 10 V	C1608X5R0J106M
C2	Ceramic capacitor	1 µF, 35 V	C2012X7R1H105K125AB
L1	Inductor	10 µH, 1 A	VLF403212MT- 100M
L2	Inductor	1 µH, 2.8 A	DFE201610P-1R0M
L3	Inductor	2.2 µH, 1 A	VLS201612ET-2R2M
D1	Schottky diode	30 V, 500 mA	NSR0530P2T5G

8.2.2.2 Inductor Selection

Both of the LM3632A boost converters are internally compensated. The compensation parameters are designed for the inductance values listed on Table 23. Effective inductance of the inductors should be ±20%.

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of the application should be requested from the manufacturer. The saturation current should be greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. When the boost device is boosting ($V_{OUT} > V_{IN}$) the inductor is one of the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important, especially for the flash and LCM Bias converters. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the LM3632A are greater than I_{PEAK} in Equation 5:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{5}$$

See detailed information in "Understanding Boost Power Stages in Switch Mode Power Supplies" http://focus.ti.com/lit/an/slva061/slva061.pdf. "Power Stage Designer™ Tools" can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

8.2.2.3 Boost Output Capacitor Selection

At least an 1-µF capacitor is recommended for the backlight boost converter output capacitor. A high-quality ceramic type X5R or X7R is recommended. Voltage rating must be greater than the maximum output voltage that is used. The effective output capacitance should always remain higher than 0.4 µF for stable operation.

For the LCM bias boost output a high-quality 10-µF ceramic type X5R or X7R capacitor is recommended. Voltage rating must be greater than the maximum output voltage that is used.

The flash driver is designed to operate with a 10-µF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter's on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

The DC-bias effect of the capacitors must be taken into consideration when selecting the output capacitors. The effective capacitance of a ceramic capacitor can drop down to less than 10% with maximum rated DC bias voltage. Note that with a same voltage applied, the capacitors with higher voltage rating suffer less from the DC-bias effect than capacitors with lower voltage rating.

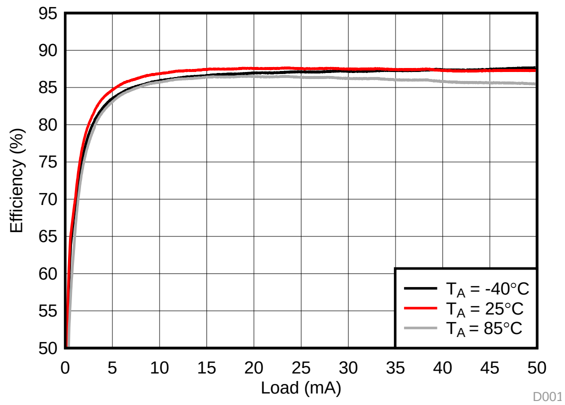
8.2.2.4 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3632A boost converters and reduce noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In Figure 55 a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the LM3632A input (VIN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents.

8.2.3 Application Curves

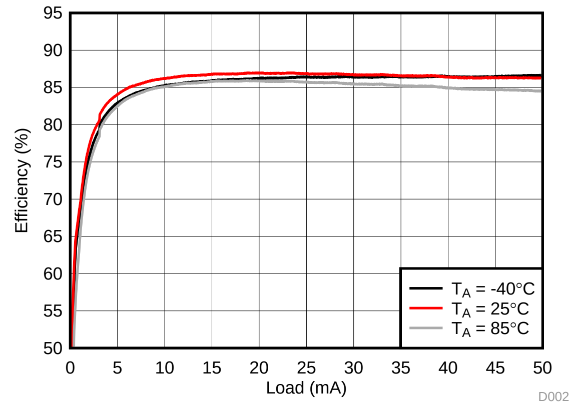
8.2.3.1 Backlight Curves

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Backlight System Efficiency is defined as PLED / PIN, where PLED is actual power consumed in backlight LEDs.



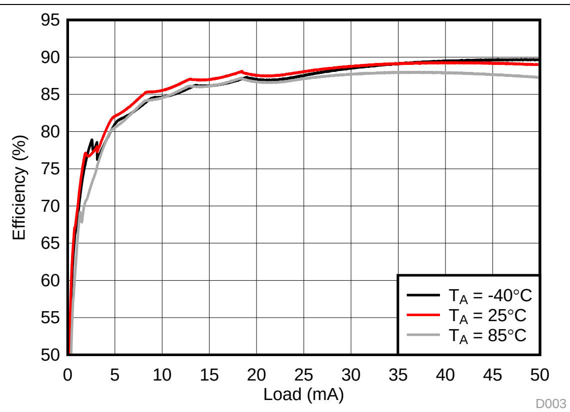
2p7s LEDs *f* = 500 kHz

Figure 56. Backlight Boost Efficiency



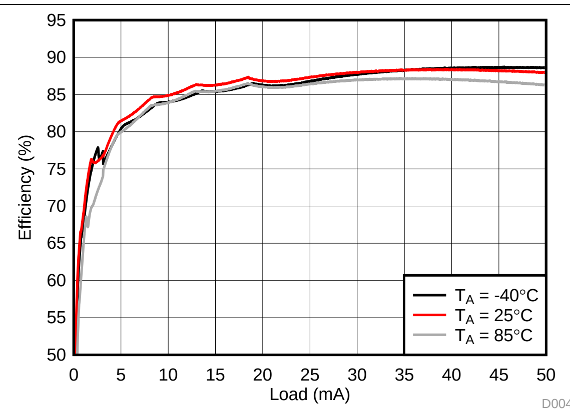
2p7s LEDs *f* = 500 kHz

Figure 57. Backlight System Efficiency



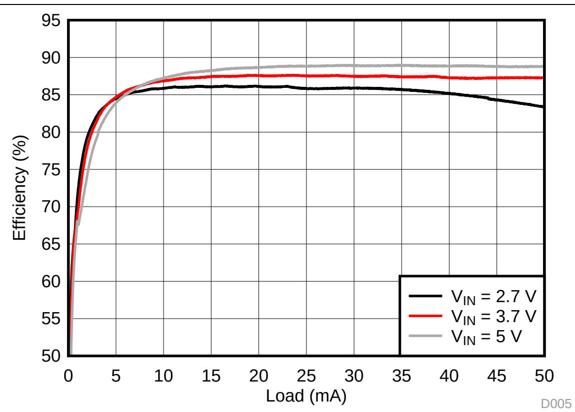
2p7s LEDs *f* = 1 MHz

Figure 58. Backlight Boost Efficiency



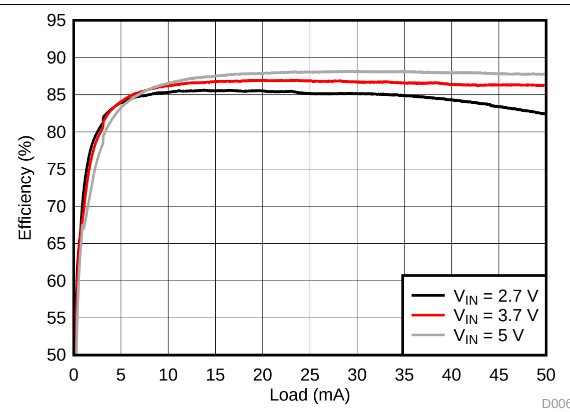
2p7s LEDs *f* = 1 MHz

Figure 59. Backlight System Efficiency



2p7s LEDs *f* = 500 kHz

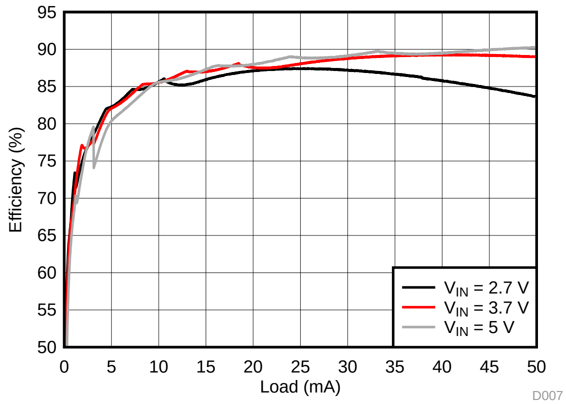
Figure 60. Backlight Boost Efficiency



2p7s LEDs *f* = 500 kHz

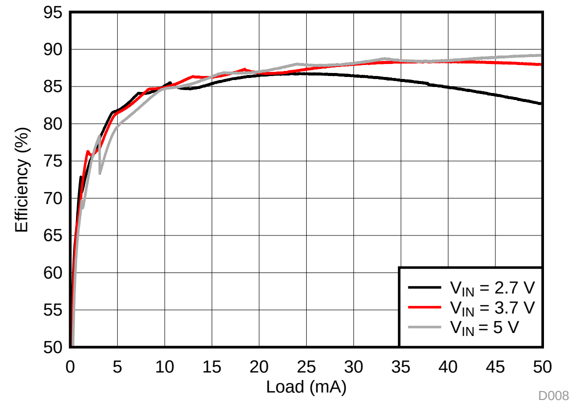
Figure 61. Backlight System Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Backlight System Efficiency is defined as PLED / PIN, where PLED is actual power consumed in backlight LEDs.



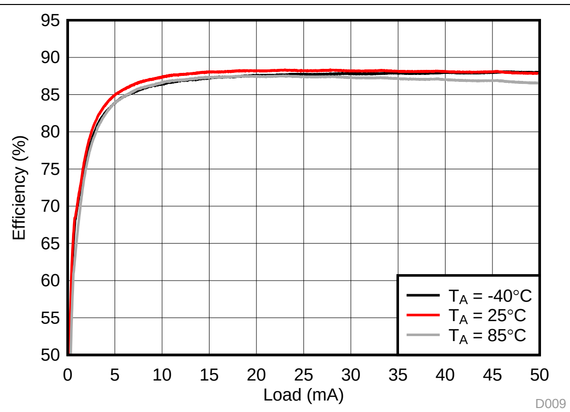
2p7s LEDs *f* = 1 MHz

Figure 62. Backlight Boost Efficiency



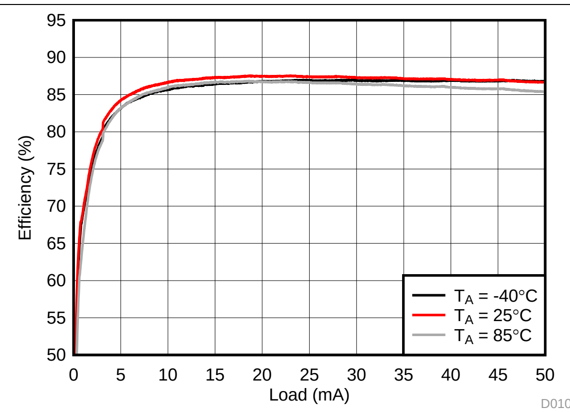
2p7s LEDs *f* = 1 MHz

Figure 63. Backlight System Efficiency



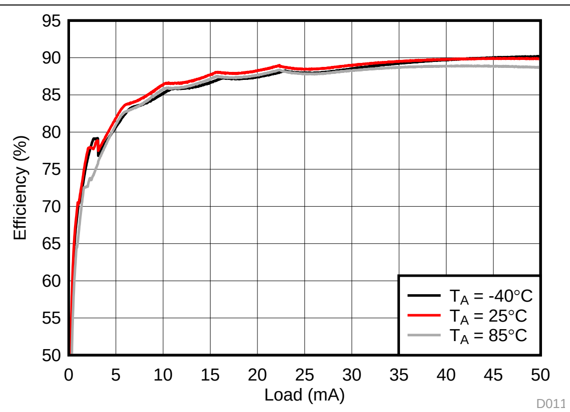
2p6s LEDs *f* = 500 kHz

Figure 64. Backlight Boost Efficiency



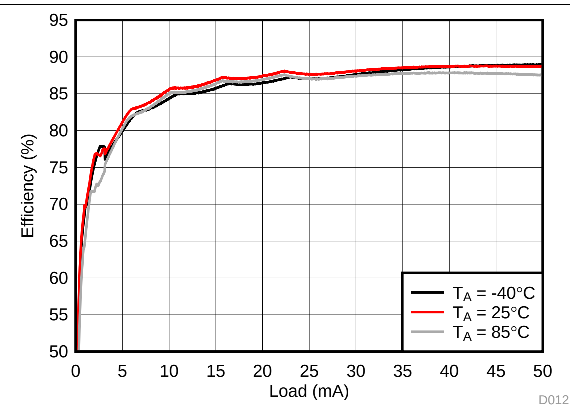
2p6s LEDs *f* = 500 kHz

Figure 65. Backlight System Efficiency



2p6s LEDs *f* = 1 MHz

Figure 66. Backlight Boost Efficiency



2p6s LEDs *f* = 1 MHz

Figure 67. Backlight System Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Backlight System Efficiency is defined as PLED / PIN, where PLED is actual power consumed in backlight LEDs.

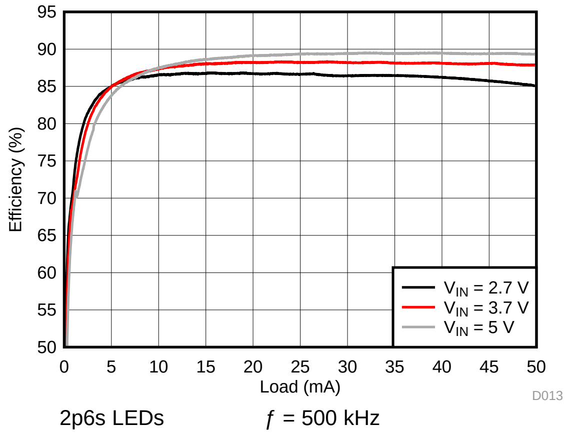


Figure 68. Backlight Boost Efficiency

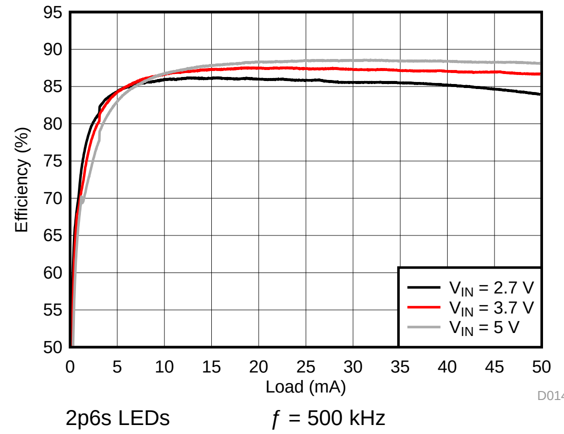


Figure 69. Backlight System Efficiency

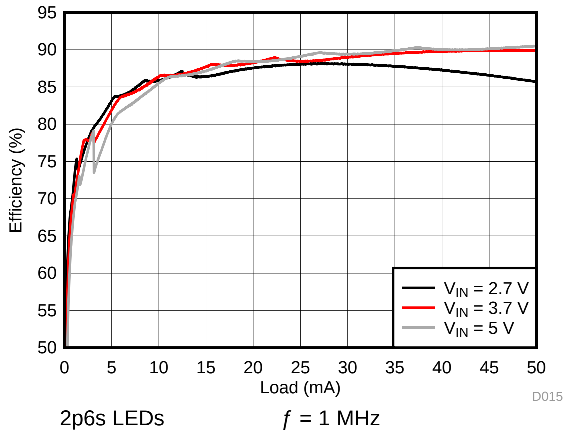


Figure 70. Backlight Boost Efficiency

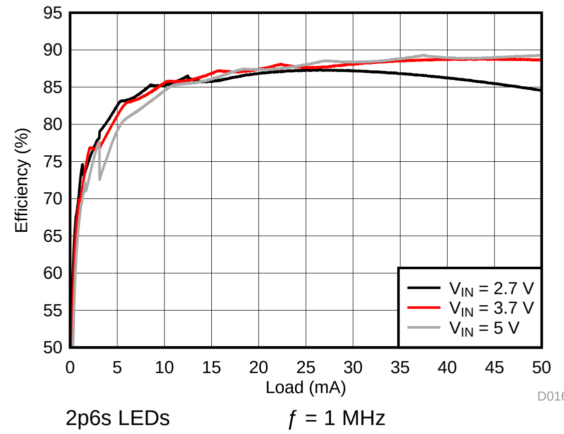


Figure 71. Backlight System Efficiency

8.2.3.2 LCM Bias Curves

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.

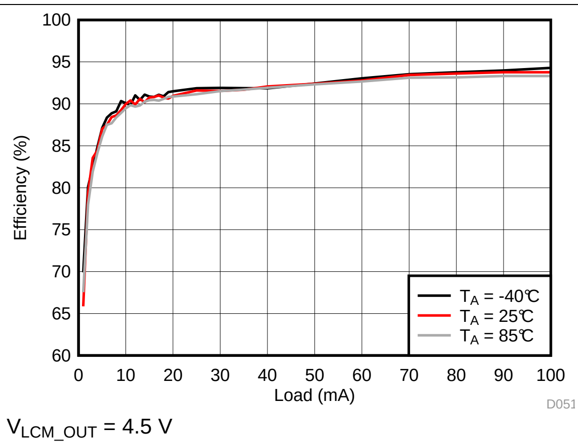


Figure 72. LCM Boost Efficiency

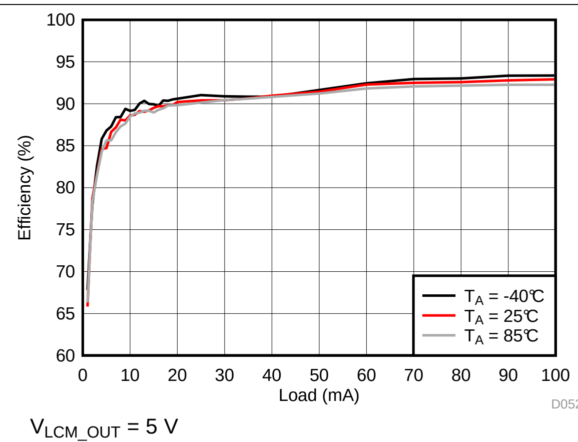
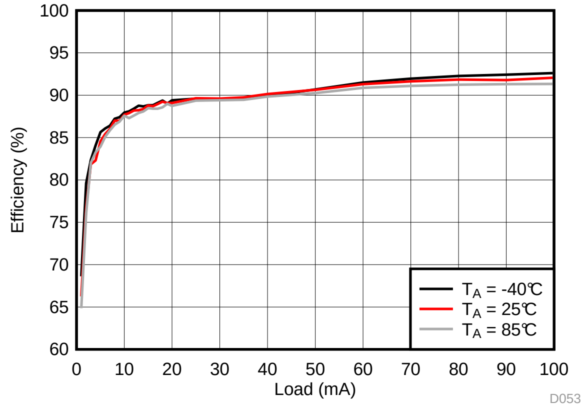


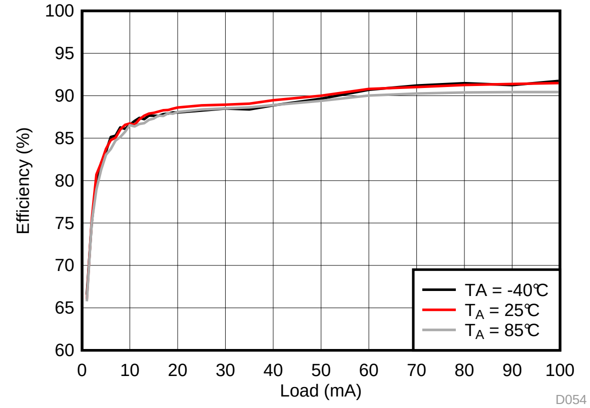
Figure 73. LCM Boost Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



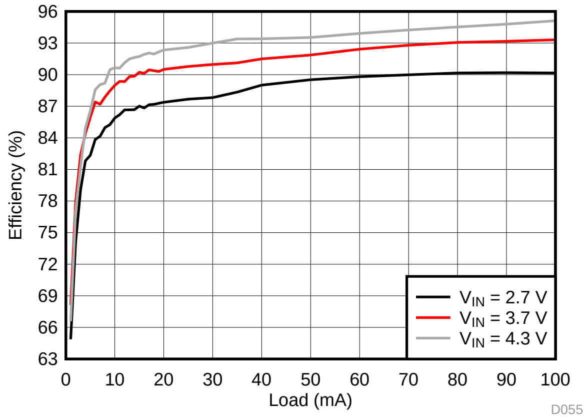
V_{LCM_OUT} = 5.5 V

Figure 74. LCM Boost Efficiency



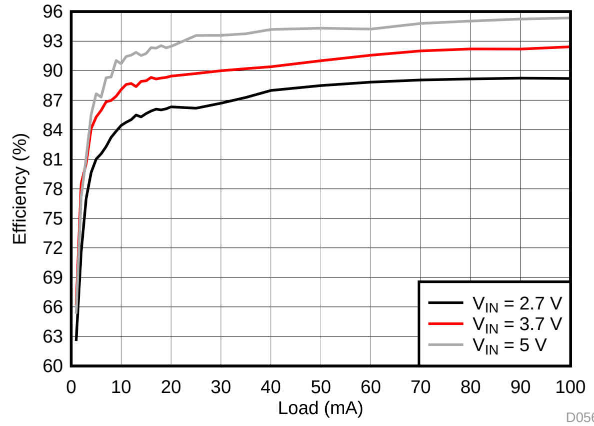
V_{LCM_OUT} = 6 V

Figure 75. LCM Boost Efficiency



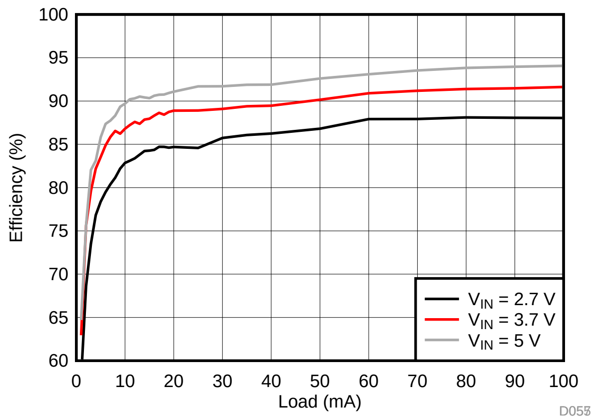
V_{LCM_OUT} = 4.8 V

Figure 76. LCM Boost Efficiency



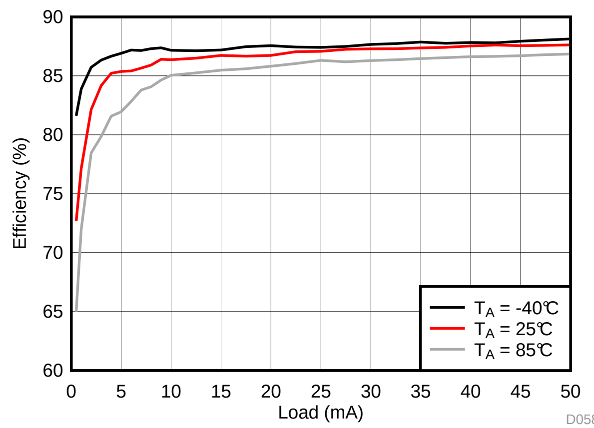
V_{LCM_OUT} = 5.3 V

Figure 77. LCM Boost Efficiency



V_{LCM_OUT} = 5.9 V

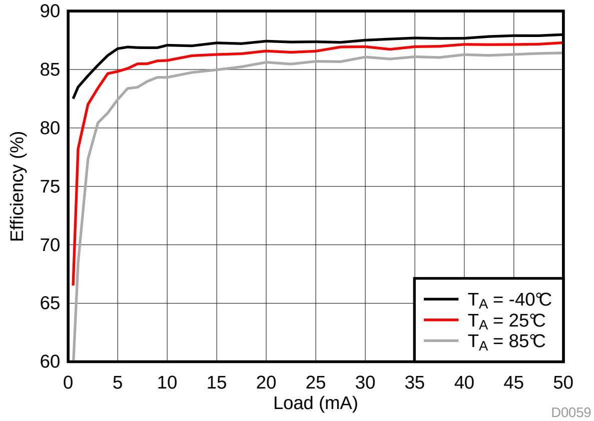
Figure 78. LCM Boost Efficiency



V_{VPOS} = 4.5 V V_{LCM_OUT} = 4.9 V

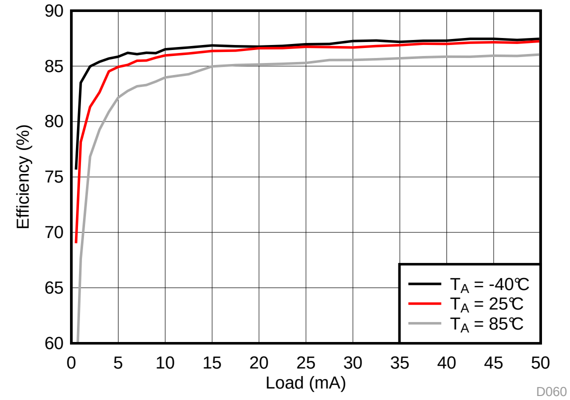
Figure 79. VPOS Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



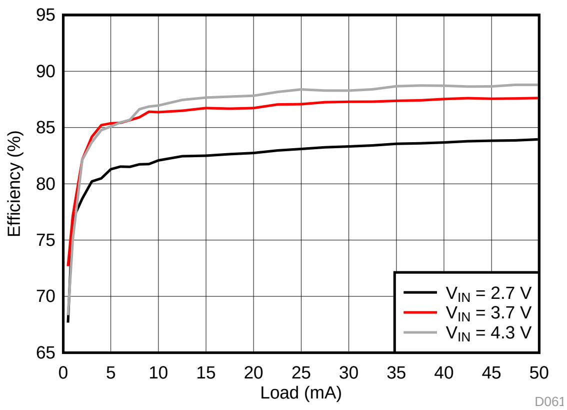
V_{VPOS} = 5 V V_{LCM_OUT} = 5.4 V

Figure 80. VPOS Efficiency



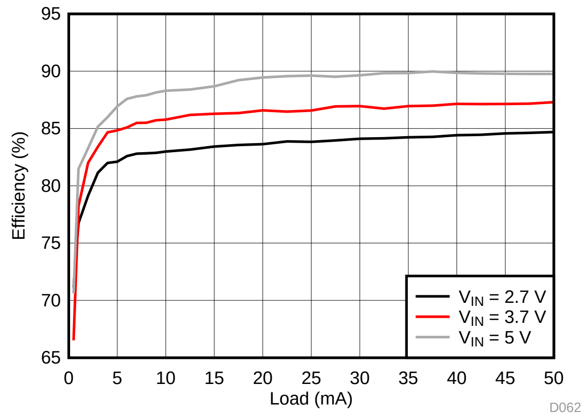
V_{VPOS} = 5.5 V V_{LCM_OUT} = 5.9 V

Figure 81. VPOS Efficiency



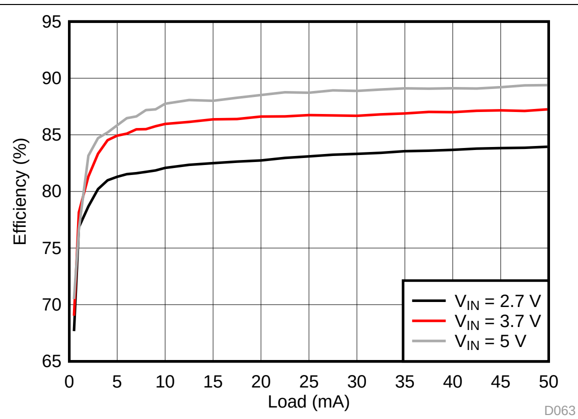
V_{VPOS} = 4.5 V V_{LCM_OUT} = 4.9 V

Figure 82. VPOS Efficiency



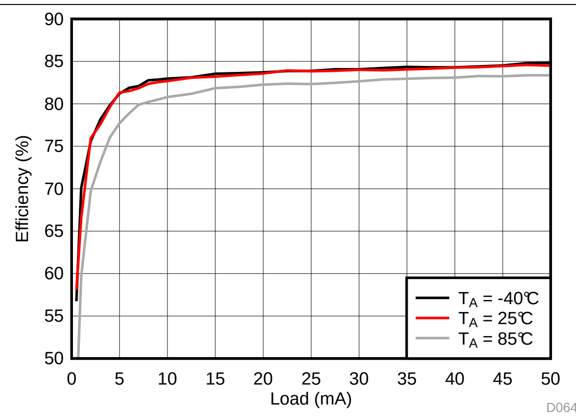
V_{VPOS} = 5 V V_{LCM_OUT} = 5.4 V

Figure 83. VPOS Efficiency



V_{VPOS} = 5.5 V V_{LCM_OUT} = 5.9 V

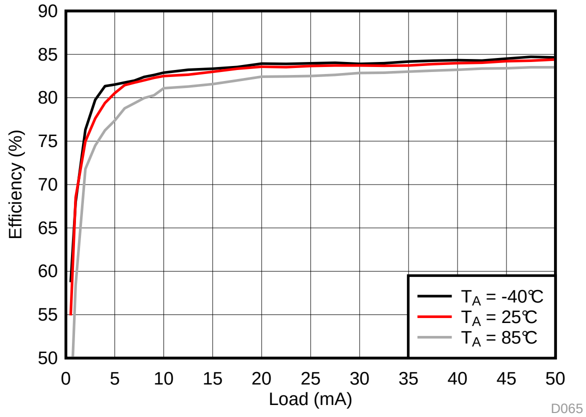
Figure 84. VPOS Efficiency



V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.9 V

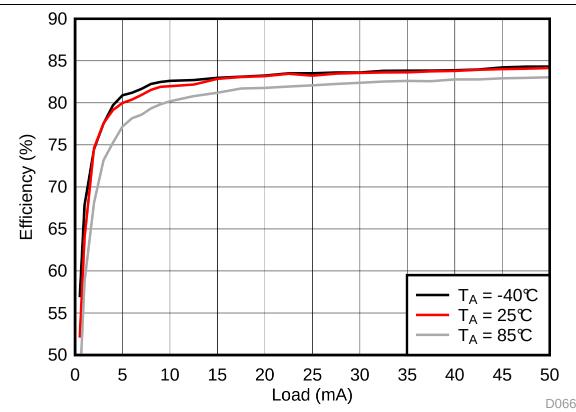
Figure 85. VNEG Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



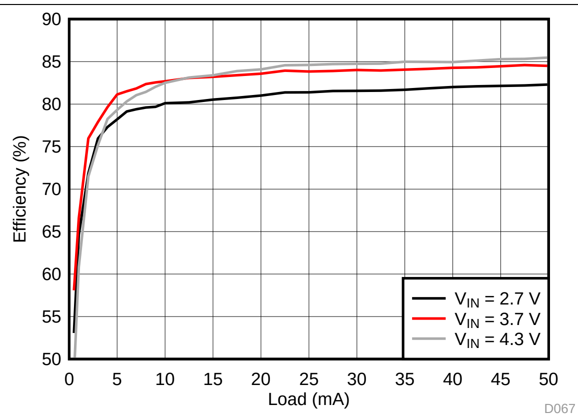
V_{VNEG} = –5 V V_{LCM_OUT} = 5.4 V

Figure 86. VNEG Efficiency



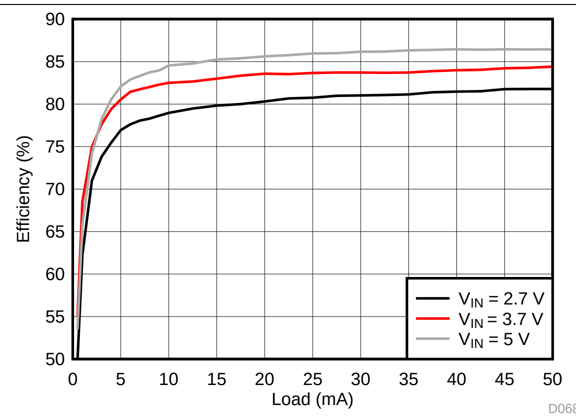
V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.9 V

Figure 87. VNEG Efficiency



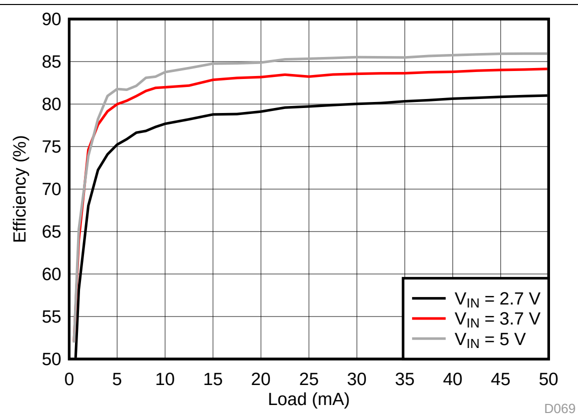
V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.9 V

Figure 88. VNEG Efficiency



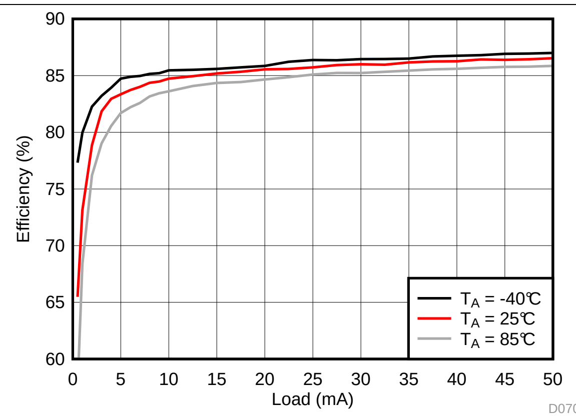
V_{VNEG} = –5 V V_{LCM_OUT} = 5.4 V

Figure 89. VNEG Efficiency



V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.9 V

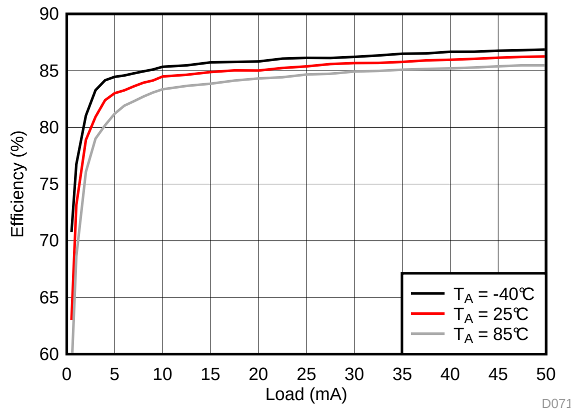
Figure 90. VNEG Efficiency



V_{VPOS} = 4.5 V V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.9 V

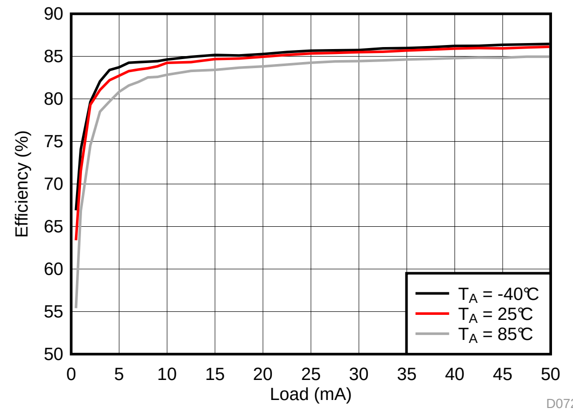
Figure 91. VPOS/VNEG Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



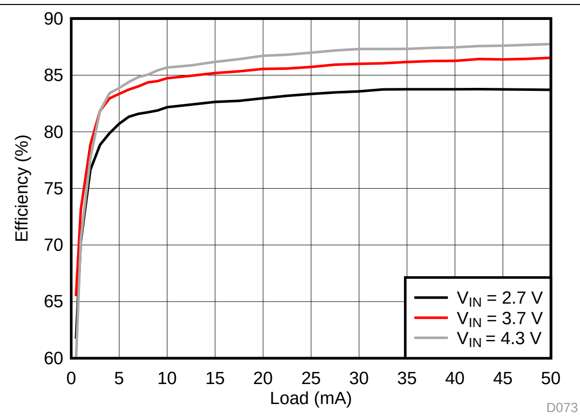
V_{VPOS} = 5 V V_{VNEG} = –5 V V_{LCM_OUT} = 5.4 V

Figure 92. VPOS/VNEG Efficiency



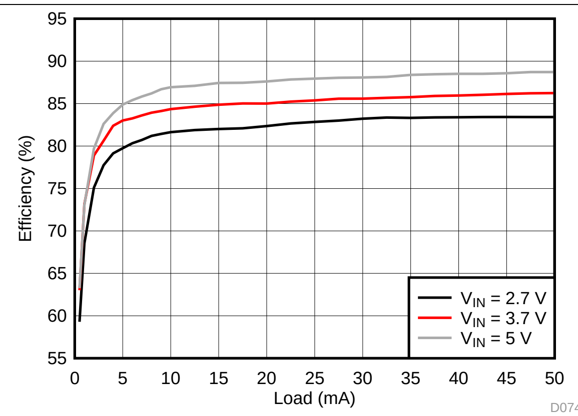
V_{VPOS}= 5.5 V V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.9 V

Figure 93. VPOS/VNEG Efficiency



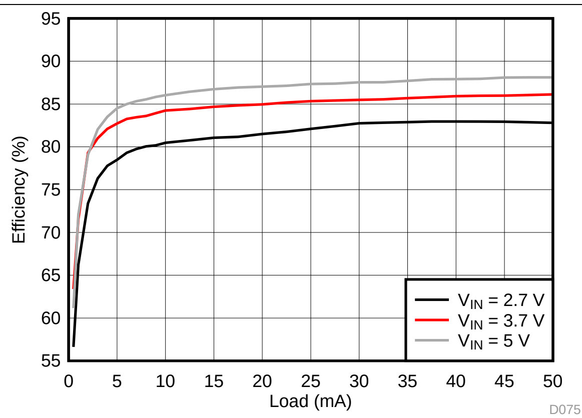
V_{VPOS} = 4.5 V V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.9 V

Figure 94. VPOS/VNEG Efficiency



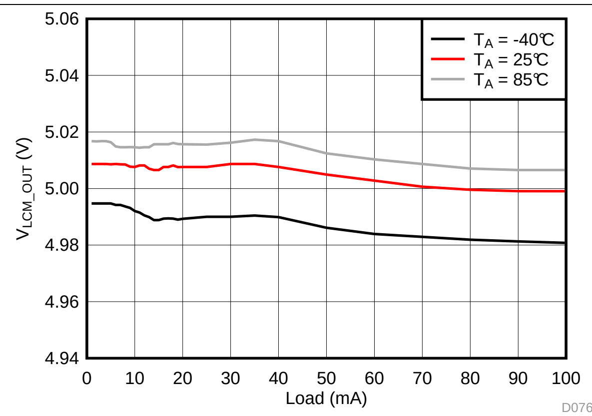
V_{VPOS} = 5 V V_{VNEG} = –5 V V_{LCM_OUT} = 5.4 V

Figure 95. VPOS/VNEG Efficiency



V_{VPOS} = 5.5 V V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.9 V

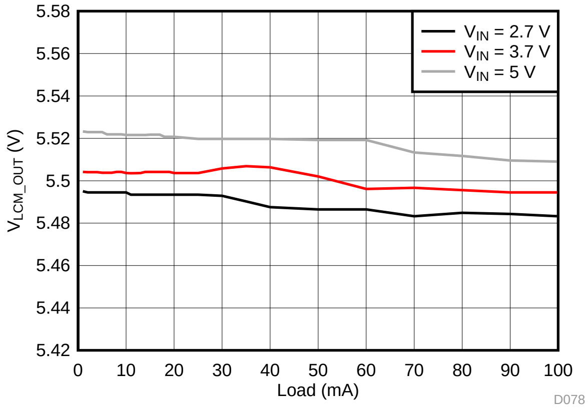
Figure 96. VPOS/VNEG Efficiency



V_{LCM_OUT} = 5 V

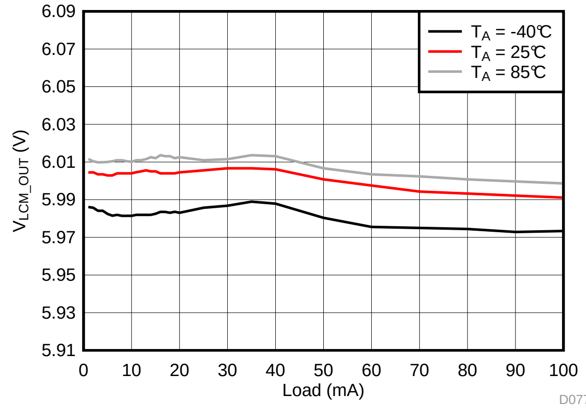
Figure 97. V_{LCM_OUT} Load Regulation

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



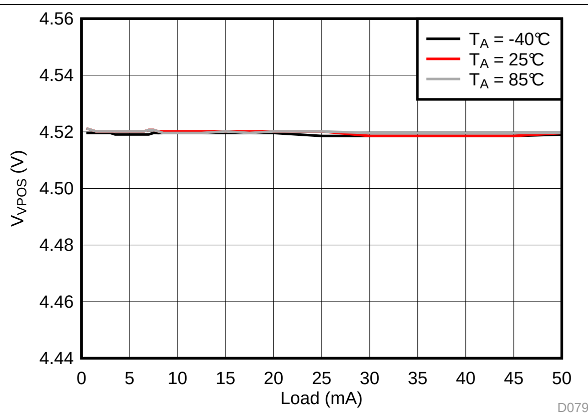
V_{LCM_OUT} = 5.5 V

Figure 98. V_{LCM_OUT} Load Regulation



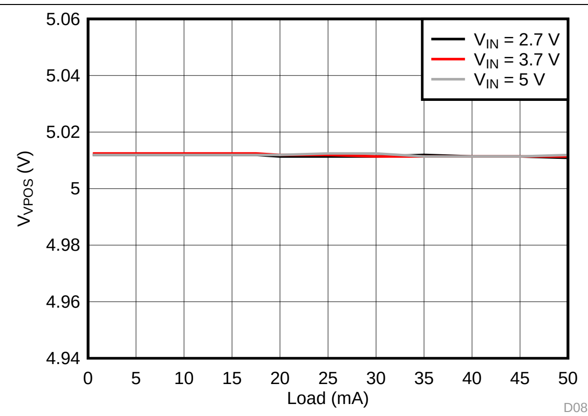
V_{LCM_OUT} = 6 V

Figure 99. V_{LCM_OUT} Load Regulation



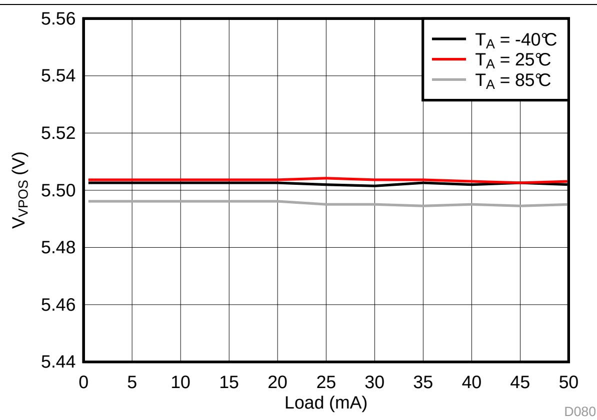
V_{VPOS} = 4.5 V V_{LCM_OUT} = 4.9 V

Figure 100. V_{VPOS} Load Regulation



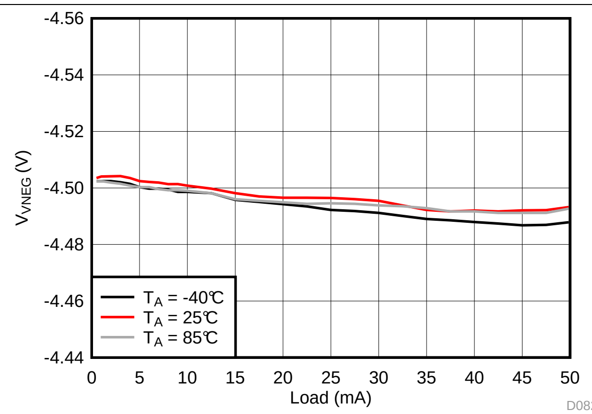
V_{VPOS} = 5 V V_{LCM_OUT} = 5.4 V

Figure 101. V_{VPOS} Load Regulation



V_{VPOS} = 5.5 V V_{LCM_OUT} = 5.9 V

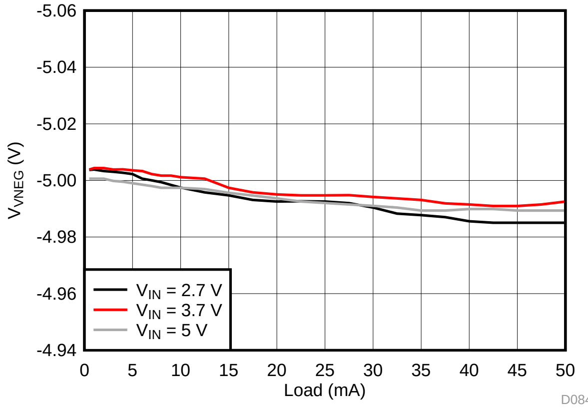
Figure 102. V_{VPOS} Load Regulation



V_{VNEG} = –4.5 V V_{LCM_OUT} = 4.9 V

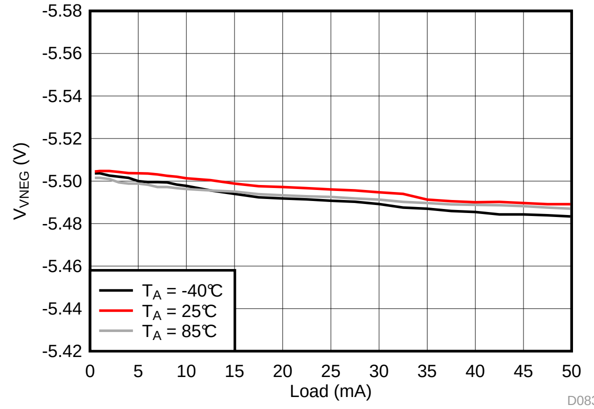
Figure 103. V_{VNEG} Load Regulation

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. VPOS, VNEG and VPOS/VNEG Efficiency is defined as POUT / PIN, where POUT is actual power consumed in VPOS, VNEG and (VPOS + VNEG) outputs, respectively.



V_{VNEG} = –5 V V_{LCM_OUT} = 5.4 V

Figure 104. V_{VNEG} Load Regulation

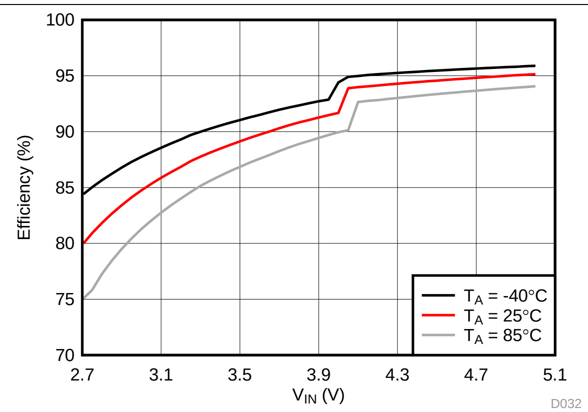


V_{VNEG} = –5.5 V V_{LCM_OUT} = 5.9 V

Figure 105. V_{VNEG} Load Regulation

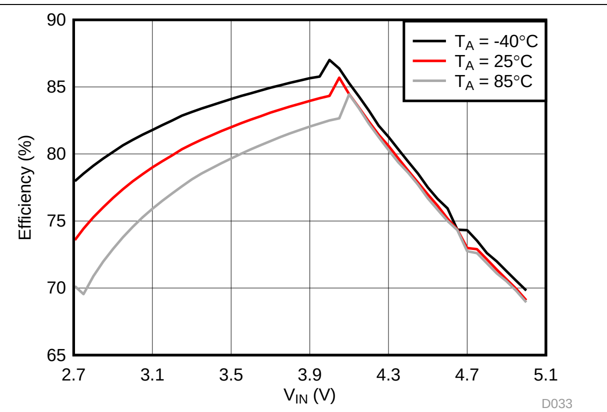
8.2.3.3 Flash Curves

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Flash System Efficiency defined as PLED / PIN, where PLED is actual power consumed in flash LED.



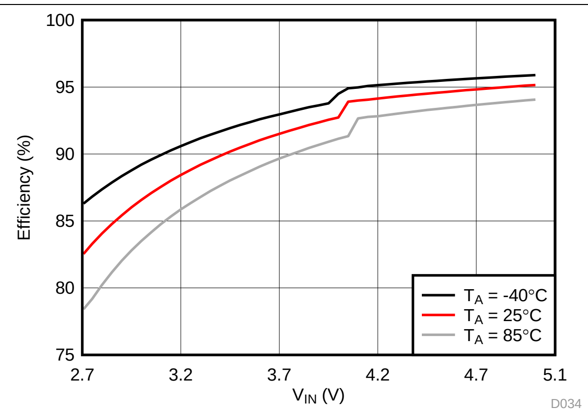
I_{FLED} = 1.5 A f = 4 MHz V_{FLED} = 3.5 V

Figure 106. Flash Boost Efficiency



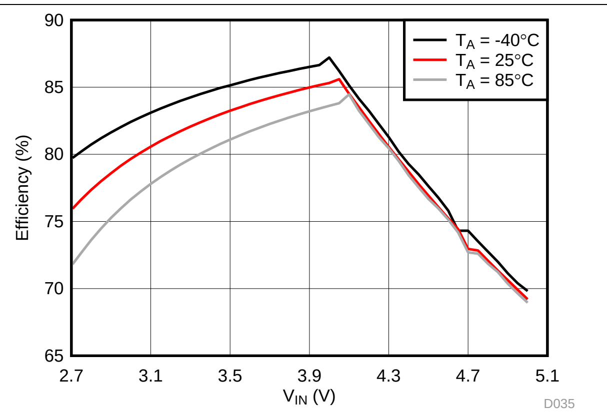
I_{FLED} = 1.5 A f = 4 MHz V_{FLED} = 3.5 V

Figure 107. Flash System Efficiency



I_{FLED} = 1.5 A f = 2 MHz V_{FLED} = 3.5 V

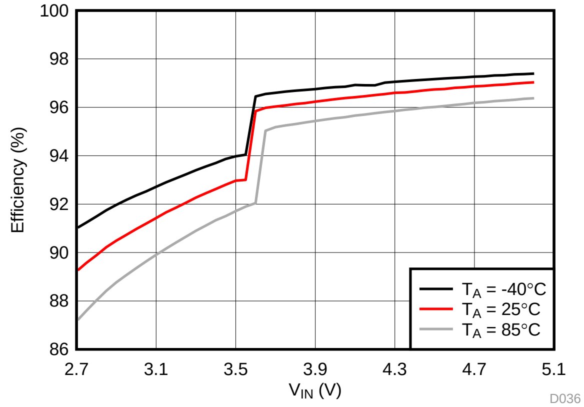
Figure 108. Flash Boost Efficiency



I_{FLED} = 1.5 A f = 2 MHz V_{FLED} = 3.5 V

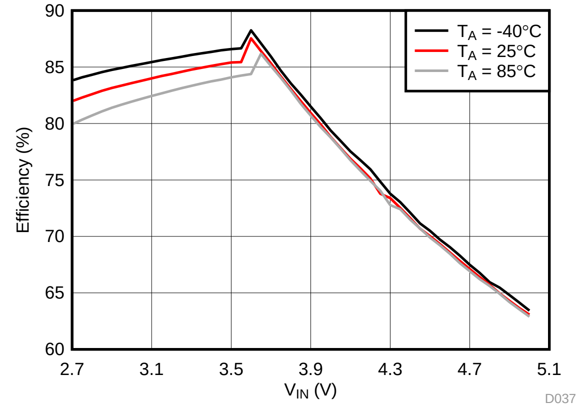
Figure 109. Flash System Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Flash System Efficiency defined as PLED / PIN, where PLED is actual power consumed in flash LED.



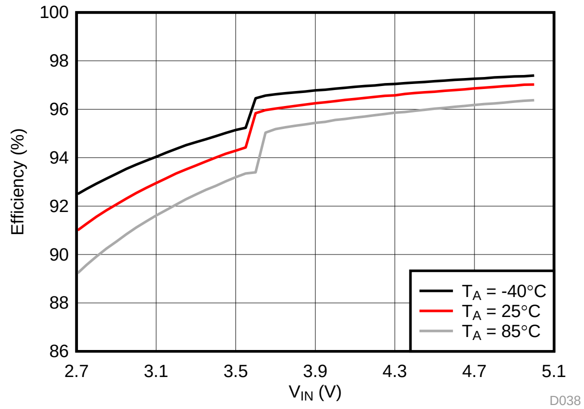
I_{FLED} = 0.8 A f = 4 MHz V_{FLED} = 3.2 V

Figure 110. Flash Boost Efficiency



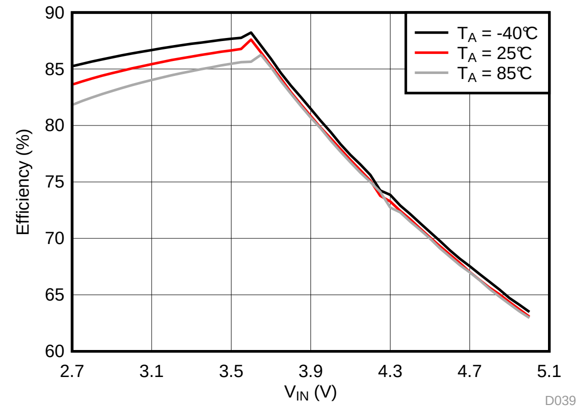
I_{FLED} = 0.8 A f = 4 MHz V_{FLED} = 3.2 V

Figure 111. Flash System Efficiency



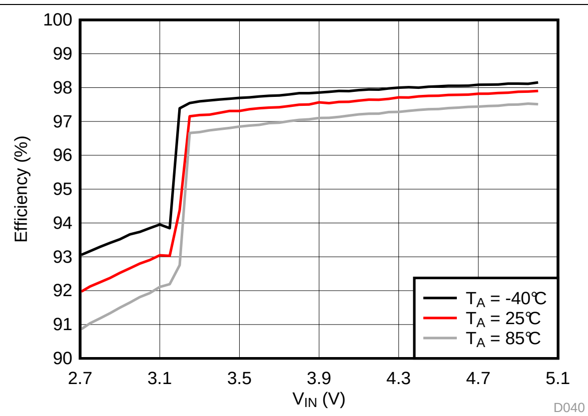
I_{FLED} = 0.8 A f = 2 MHz V_{FLED} = 3.2 V

Figure 112. Flash Boost Efficiency



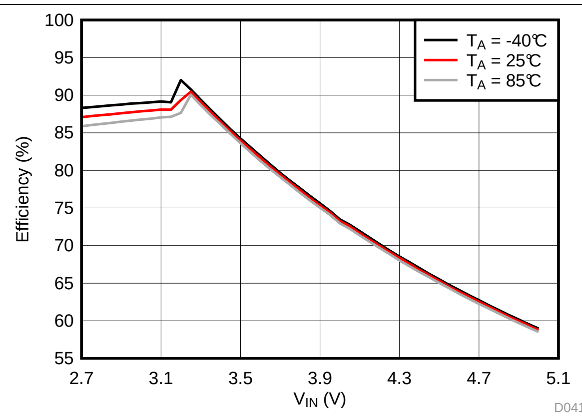
I_{FLED} = 0.8 A f = 2 MHz V_{FLED} = 3.2 V

Figure 113. Flash System Efficiency



I_{FLED} = 375 mA f = 4 MHz V_{FLED} = 3 V

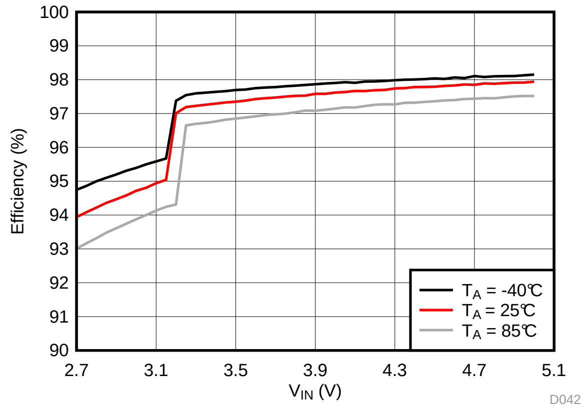
Figure 114. Torch Boost Efficiency



I_{FLED} = 375 mA f = 4 MHz V_{FLED} = 3 V

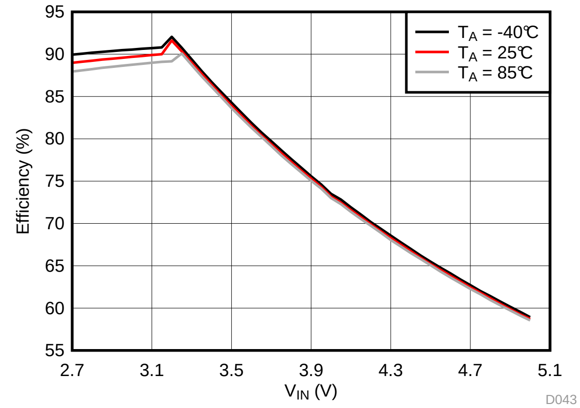
Figure 115. Torch System Efficiency

Ambient temperature is 25°C and V_{IN} is 3.7 V unless otherwise noted. Flash System Efficiency defined as PLED / PIN, where PLED is actual power consumed in flash LED.



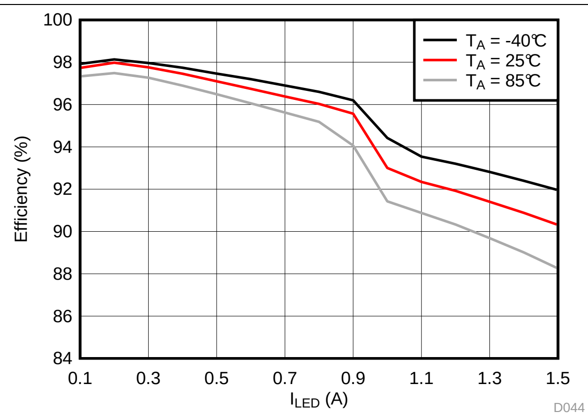
I_{FLED} = 375 mA *f* = 4 MHz V_{FLED} = 3 V

Figure 116. Torch Boost Efficiency



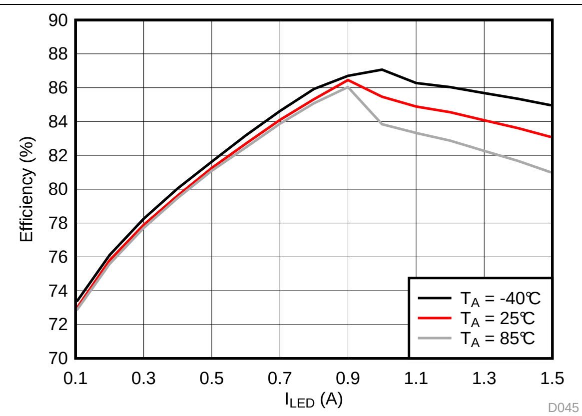
I_{FLED} = 375 mA *f* = 2 MHz V_{FLED} = 3 V

Figure 117. Torch System Efficiency



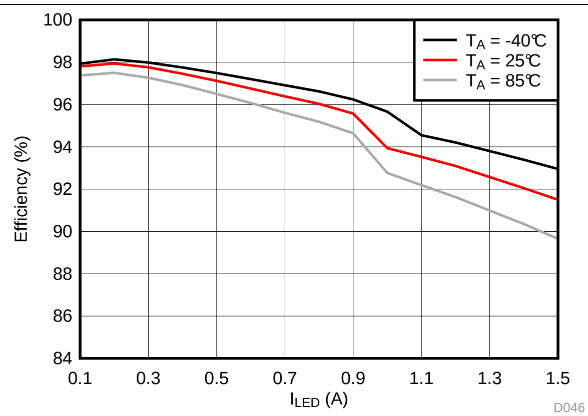
f = 4 MHz

Figure 118. Flash Boost Efficiency



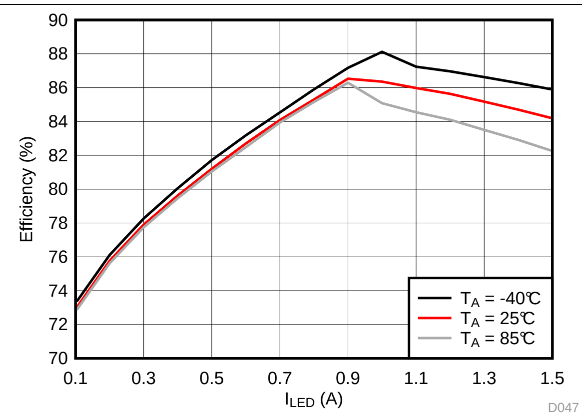
f = 4 MHz

Figure 119. Flash System Efficiency



f = 2 MHz

Figure 120. Flash Boost Efficiency



f = 2 MHz

Figure 121. Flash System Efficiency

9 Power Supply Recommendations

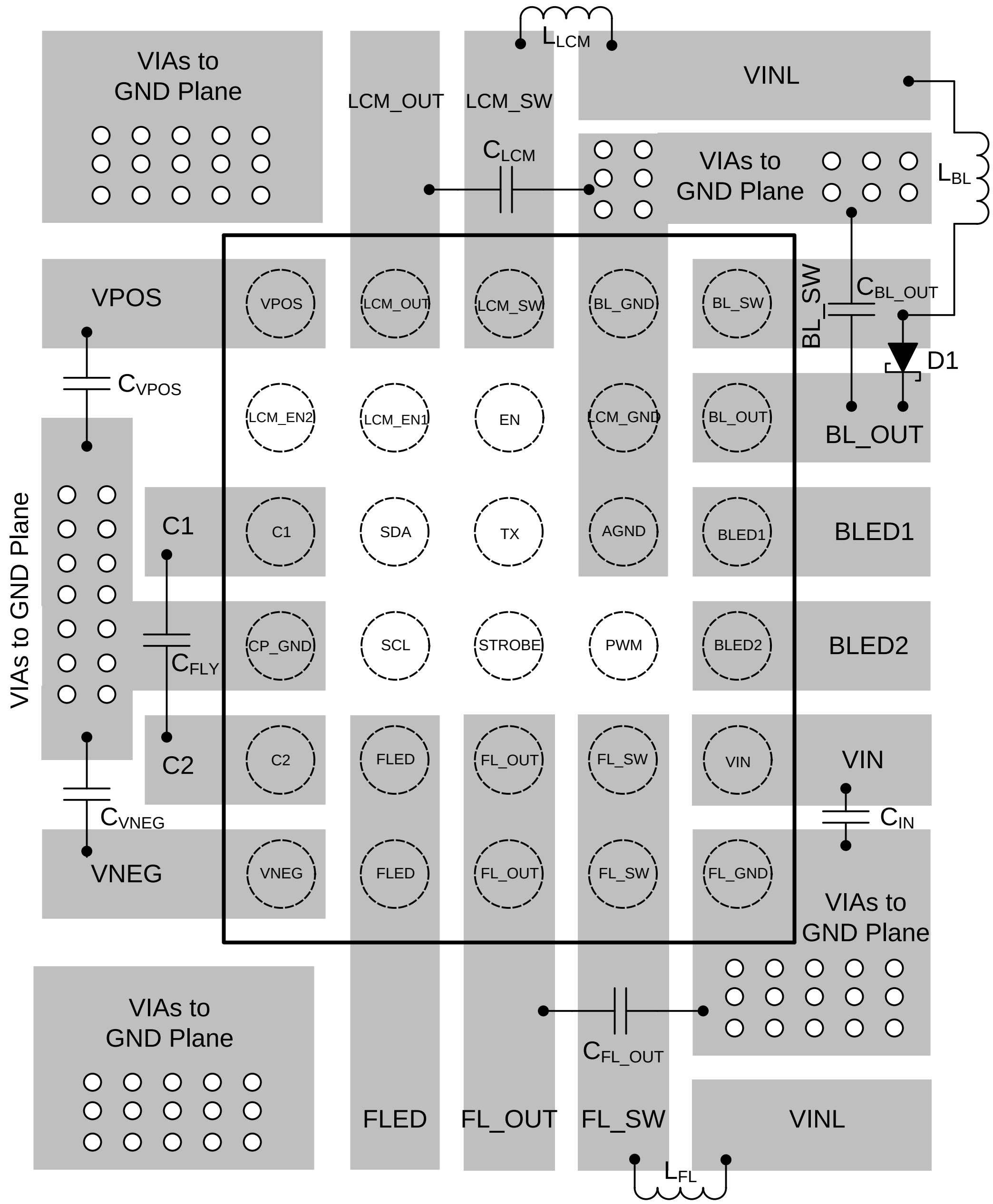
The LM3632A is designed to operate from an input voltage supply range between 2.7 V and 5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM3632A additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- Place the boost converters output capacitors as close to the output voltage and GND pins as possible.
- Minimize the boost converter switching loops by placing the input capacitors and inductors close to GND and switch pins.
- If possible, route the switching loops on top layer only. For best efficiency, try to minimize copper on the switch node to minimize switch pin parasitic capacitance while preserving adequate routing width.
- VIN input voltage pin needs to be bypassed to ground with a low-ESR bypass capacitor. Place the capacitor as close to VIN pin as possible.
- Place the output capacitor of the LDO as close to the output pins as possible. Also place the charge pump flying capacitor and output capacitor close to their respective pins.
- Terminate the Flash LED cathode directly to the Flash GND pin of the LM3632A. If possible, route the LED return with a dedicated path so as to keep the high amplitude LED current out of the GND plane.
- Route the internal pins on the second layer. Use offset micro vias to go from top layer to mid-layer1. Avoid routing the signal traces directly under the switching loops of the boost converters.

10.2 Layout Example



11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note AN1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

Understanding Boost Power Stages in Switch Mode Power Supplies,

http://focus.ti.com/lit/an/slva061/slva061.pdf.

Power Stage Designer™ Tools, http://www.ti.com/tool/powerstage-designer.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3632AYFFR	ACTIVE	DSBGA	YFF	30	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3632A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

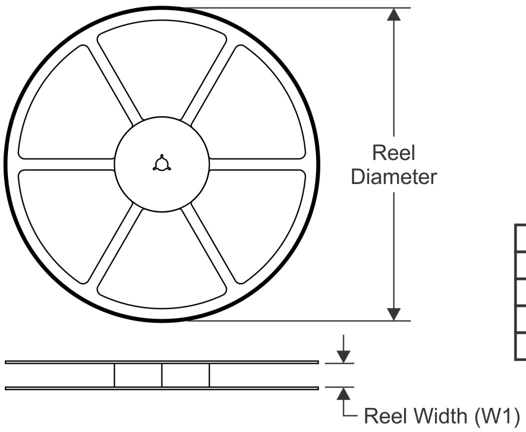
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

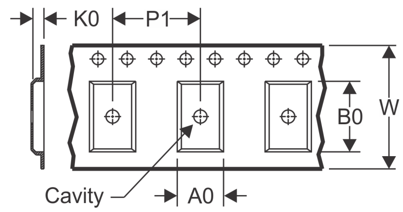
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

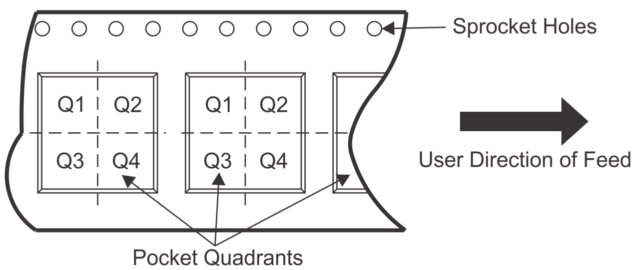


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

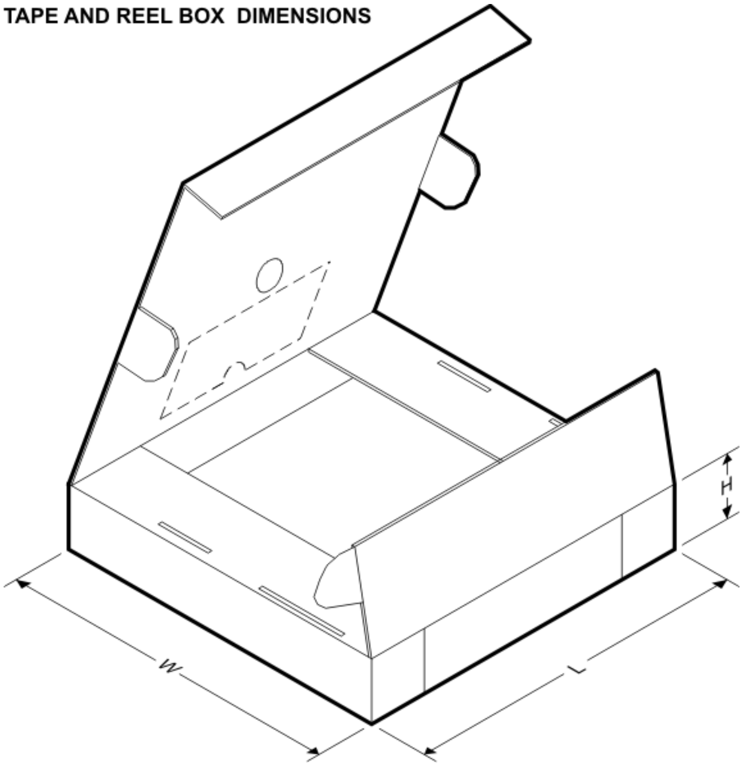
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

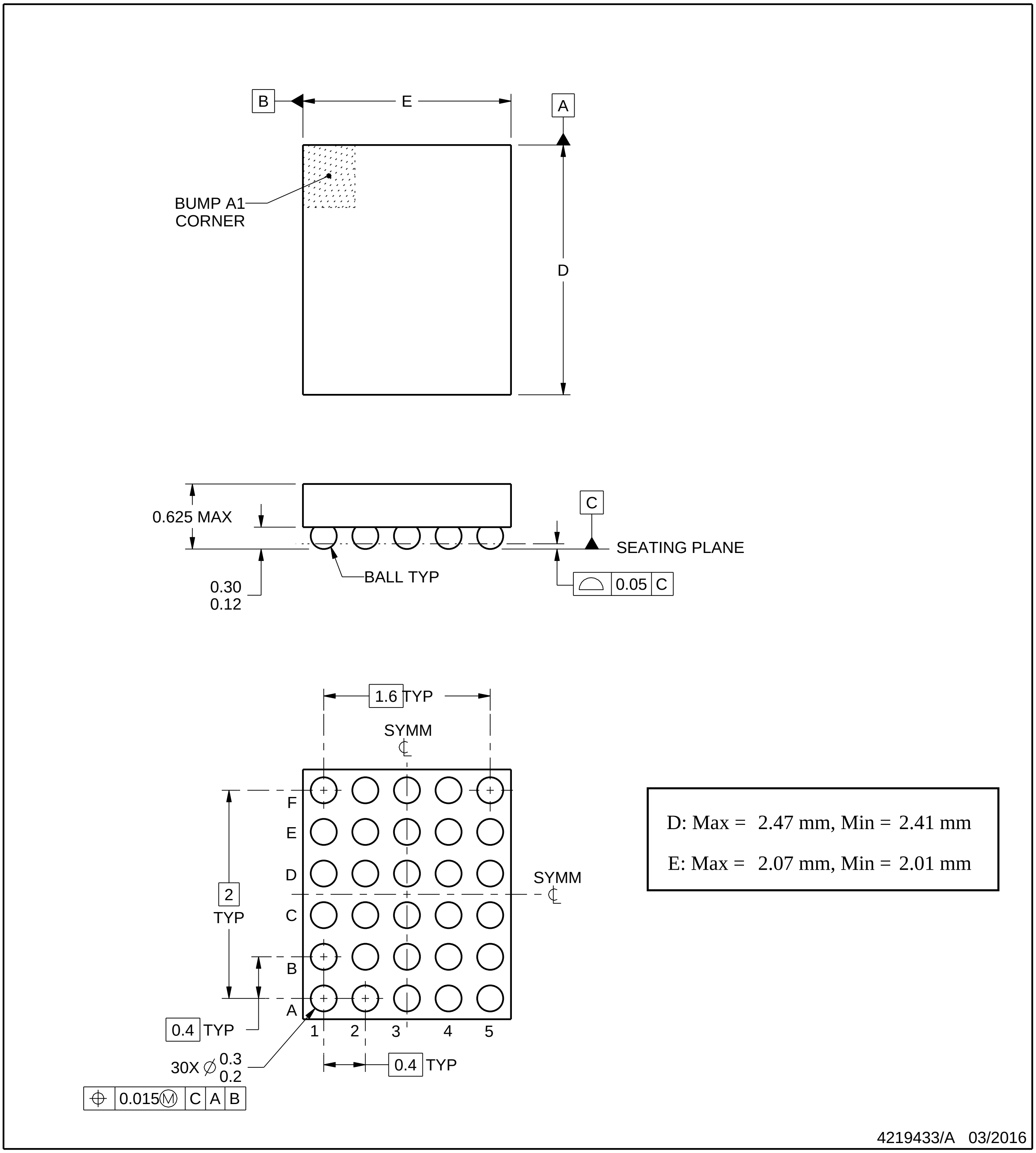
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3632AYFFR	DSBGA	YFF	30	3000	180.0	8.4	2.26	2.74	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



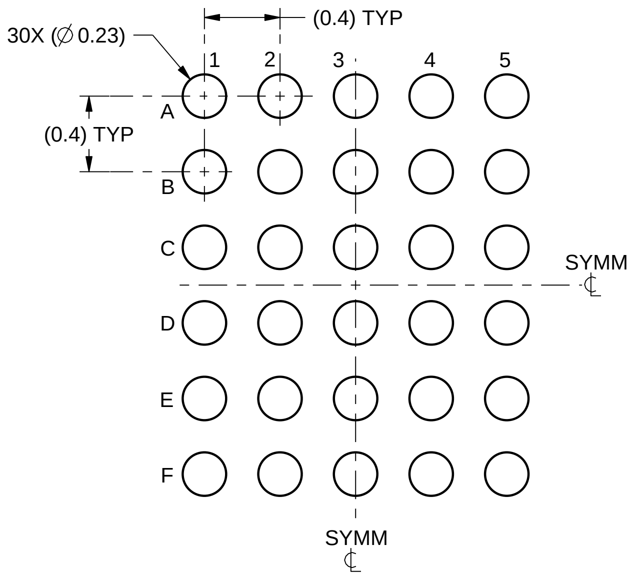
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3632AYFFR	DSBGA	YFF	30	3000	182.0	182.0	20.0

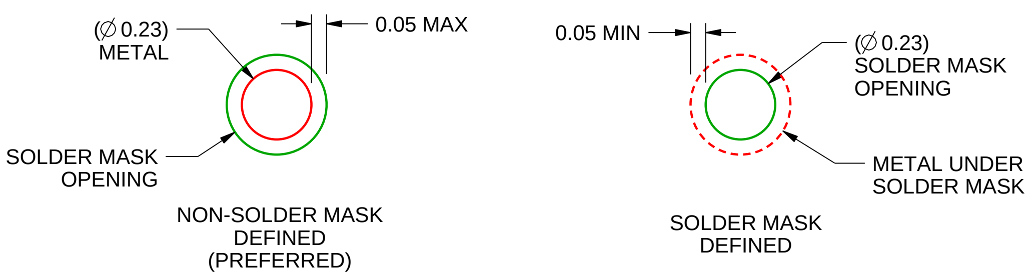


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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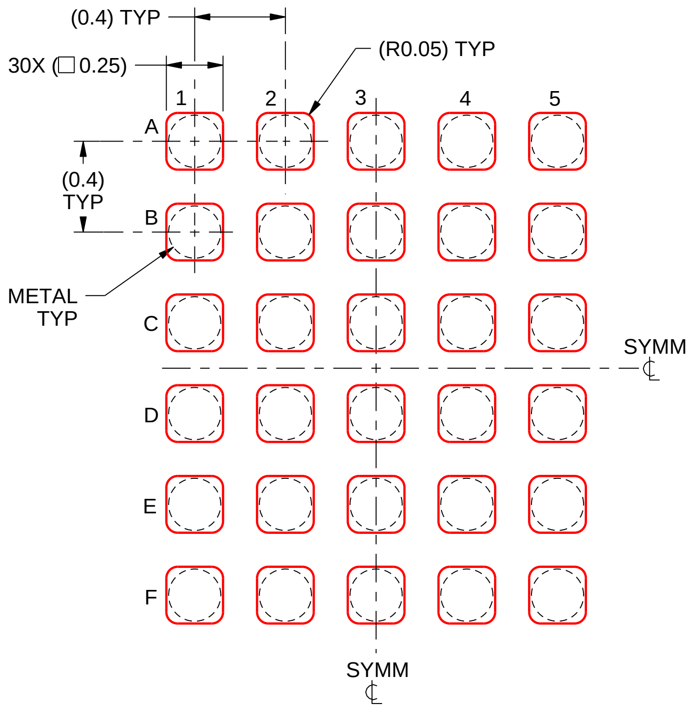
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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