TEXAS INSTRUMENTS
LM51231-Q1
JAJSNE2 – OCTOBER 2022

LM51231-Q1 2.2MHz 広入力電圧範囲 (VIN)、同期整流昇圧コントローラ、VOUT トラッキング搭載

1 特長

- 車載アプリケーション向けの AEC-Q100 認証取得済み
  - 温度グレード 1:-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載用バッテリ駆動アプリケーションの広い動作範囲に適合
  - 3.8V～42V の入力動作範囲
  - VOUT を 5V～20V または 15V～57V に動的にプログラム可能
  - BIAS ≧ 3.8V のときの最小昇圧入力電圧 0.8V
  - V_{SUPPLY} > V_{LOAD} のときバイパス動作
- BIAS シャットダウン時電流:3μA 未満
- 小さなソリューション・サイズ
  - 最大スイッチング周波数:2.2MHz
  - ブート・ダイオード内蔵
  - ウェッタブル・フランク付き QFN-20
- EMI の低減、AM 帯域干渉とクロストークの防止
  - クロック同期 (オプション)
  - スイッチング周波数:100kHz～2.2MHz
  - スイッチング・モードを選択可能 (FPWM、ダイオード・エミュレーション)
  - プログラム可能な拡散スペクトラム (オプション)
  - リードレス・パッケージ
- プログラマビリティとフレキシビリティ
  - 動的な V_{OUT} トラッキング
  - 動的なスイッチング周波数のプログラミング
  - DCR インダクタ電流センシングをサポート
  - 入力電圧 UVLO を設定可能
  - 調整可能なソフト・スタート
  - アダプティブ・デッドタイム制御
  - PGOOD インジケータ
- 保護機能内蔵
  - サイクル単位のピーク電流制限 (V_{SUPPLY} の全範囲で一定)
  - 過電圧保護
  - HB-SW 短絡保護
  - サーマル・シャットダウン

2 アプリケーション

- トラッキング機能付き車載用オーディオ電源
- 車載用 LED バイアス電源

3 概要

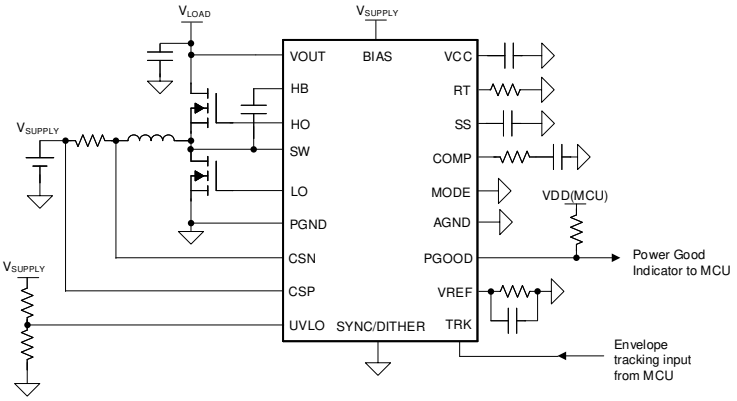
LM51231-Q1 デバイスは、広い入力電圧範囲に対応した同期整流昇圧コントローラであり、ピーク電流モード制御を採用しています。本デバイスの広い入力範囲は、自動車のコールド・クランクとロード・ダンプに対応します。BIAS が 3.8V 以上の場合、最小入力電圧を 0.8V まで下げることができます。出力電圧は、トラッキング機能を使うことで動的にプログラムできます。V_{SUPPLY} > V_{LOAD} になると自動的にバイパス・モード動作に入り、ハイサイド MOSFET のボディ・ダイオードの電圧降下を解消できます。スイッチング周波数は、外付けの抵抗により 100kHz～2.2MHz の範囲で動的にプログラム可能です。2.2MHz でのスイッチングにより、AM 帯域との干渉が最小化され、ソリューション・サイズの小型化と、高速な過渡応答を実現できます。

ピーク電流制限 (V_{SUPPLY} の全範囲にわたって一定)、過電圧保護、サーマル・シャットダウンなどの保護機能が内蔵されています。外部クロック同期、プログラム可能なスペクトラム拡散変調、最小限の寄生容量でのリードレス・パッケージは、EMI の低減とクロストークの回避に役立ちます。その他の機能として、ライン UVLO、FPWM、ダイオード・エミュレーション、DCR インダクタ電流センシング、プログラム可能なソフトスタート、パワー・グッド・インジケータがあります。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM51231-Q1	QFN (20)	3.5mm × 3.5mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2022	*	Initial release

5 Pin Configuration and Functions

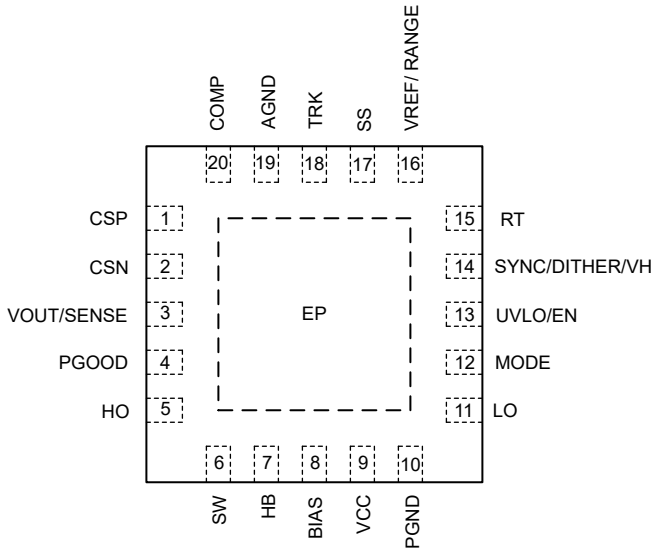


図 5-1. 20-Pin QFN with Wettable Flanks RGR Package (Top View)

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	CSP	I	Current sense amplifier input. The pin operates as the positive input pin.
2	CSN	I	Current sense amplifier input. The pin operates as the negative input pin.
3	VOUT/SENSE	I	Output voltage sensing pin. An internal feedback resistor voltage divider is connected from the pin to AGND. Connect a 0.1-µF local VOUT capacitor from the pin to ground.
			High-side MOSFET drain voltage sensing pin. Connect the pin to the drain of the high-side MOSFET through a short, low inductance path.
4	PGOOD	O	Power-good indicator with open-drain output stage. The pin is grounded when the output voltage is less than the undervoltage threshold. The pin can be left floating if not used.
5	HO	O	High-side gate driver output. Connect directly to the gate of the high-side N-channel MOSFET through a short, low inductance path.
6	SW	P	Switching node connection and the high-side MOSFET source voltage sensing pin. Connect directly to the source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET through a short, low inductance path. Connect to PGND for non-synchronous boost configuration.
7	HB	P	High-side driver supply for bootstrap gate drive. Boot diode is internally connected from VCC to the pin. Connect a 0.1-µF capacitor between the pin and SW. Connect to VCC for non-synchronous boost configuration.
8	BIAS	P	Supply voltage input to the VCC regulator. Connect a 1-µF local BIAS capacitor from the pin to ground.
9	VCC	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET drivers. Connect a 4.7-µF capacitor between the pin and PGND.
10	PGND	G	Power ground pin. Connect directly to the source of the low-side N-channel MOSFET and the power ground plane through a short, low inductance path.
11	LO	O	Low-side gate driver output. Connect directly to the gate of the low-side N-channel MOSFET through a short, low inductance path.
12	MODE	I	Device switching mode (FPWM or diode emulation) selection pin. The device is configured to diode emulation if the pin is open or if a resistor that is greater than 500 kΩ is connected from the pin to AGND or is less than 0.4 V during initial power-on. The device is configured to FPWM mode by connecting the pin to VCC or if the pin voltage is greater than 2.0 V during power-on. The switching mode can be dynamically programmed between the FPWM and the DE mode during operation.

表 5-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
13	UVLO/EN	I	Enable pin. The pin enables/disables the device. If the pin is less than 0.35 V, the device shuts down. The pin must be raised above 0.65 V to enable the device.
			Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting the pin to the supply voltage through a resistor voltage divider. The low-side UVLO resistor must be connected to AGND. Connect to BIAS if not used.
14	SYNC/DITHER/VH	I/O	Synchronization clock input. The internal oscillator can be synchronized to an external clock during operation. Connect to AGND if not used.
			Clock dithering/spread spectrum modulation frequency programming pin. If a capacitor is connected between the pin and AGND, the clock dithering/spread spectrum function is activated. During the dithering operation, the capacitor is charged and discharged with an internal 20-µA current source/sink. As the voltage on the pin ramps up and down, the oscillator frequency is modulated between –6% and +5% of the nominal frequency set by the RT resistor. The clock dithering/spread spectrum can be deactivated during operation by pulling down the pin to ground.
			VCC hold pin. If the pin is greater than 2.0 V, the device holds the VCC pin voltage when the EN pin is grounded, which helps to restart fast without reconfiguration.
15	RT	I	Switching frequency setting pin. If no external clock is applied to the SYNC pin, the switching frequency is programmed by a single resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
16	VREF/RANGE	I/O	1.0-V internal reference voltage output. Connect a 470-pF capacitor from the pin to AGND. The V_{OUT} regulation target can be programmed by connecting a resistor voltage divider from the pin to TRK. The resistance from the pin to AGND must be always greater than 20 kΩ if used. Connect the low-side resistor of the divider to AGND.
			V_{OUT} range selection pin. Lower V_{OUT} range (5 V to 20 V) is selected if the resistance from the pin to AGND is in the range of 75 kΩ and 100 kΩ during initial power-on. Upper VOUT range (15 V to 57 V) is selected if the resistance from the pin to AGND is in the range of 20 kΩ and 35 kΩ during initial power-on. Boost converter output voltage can be dynamically programmed within the pre-programmed range. The accuracy of the output voltage regulation is specified within the selected range.
17	SS	I/O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
18	TRK	I	Output regulation target programming pin. The V_{OUT} regulation target can be programmed by connecting the pin to VREF through a resistor voltage divider or by controlling the pin voltage directly from a D/A. The recommended operating range of the pin is from 0.25 V to 1.0 V.
19	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
20	COMP	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
-	EP		Exposed pad of the package. The EP must be soldered to a large analog ground plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	MAX	UNIT
Input(2)	BIAS to AGND	–0.3	50	V
	UVLO to AGND	–0.3	BIAS + 0.3	
	CSP to AGND	–0.3	50	
	CSP to CSN	–0.3	0.3	
	VOUT to AGND	–0.3	65	
	HB to AGND	–0.3	65	
	HB to SW	–0.3	5.8(3)	
	SW to AGND	-0.3	60	
	SW to AGND (50ns)	–1		
	MODE, SYNC, TRK to AGND	–0.3	5.5	
	PGOOD to AGND	–0.3	VOUT + 0.3	
	RT to AGND	–0.3	2.5	
	PGND to AGND	–0.3	0.3	
Output(2)	VCC to AGND	–0.3	5.8(3)	V
	HO to SW (50ns)	–1		
	LO to PGND (50ns)	–1		
	VREF, SS, COMP to AGND(4)	–0.3	5.5	
Operating junction temperature, T_J (5)		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) It is not allowed to apply an external voltage directly to VREF, COMP, SS, RT, LO, HO pins.
(3) Operating lifetime is de-rated when the pin voltage is greater than 5.5V.
(4) Maximum VREF pin sourcing current is 50uA.
(5) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
$V_{SUPPLY(BOOST)}$	Boost Converter Input (when BIAS ≥ 3.8V)	0.8		42	V
$V_{LOAD(BOOST)}$	Boost Converter Output	5		57	
V_{BIAS}	BIAS Input	3.8		42	
V_{UVLO}	UVLO Input	0		42	
V_{CSP}, V_{CSN}	Current Sense Input	0.8		42	
V_{VOUT}	Boost Output Sense	5		57	
V_{TRK}	TRK Input	0.25		1(3)	
V_{SYNC}	Synchronization Pulse Input	0		5.25	
f_{SW}	Typical Switching Frequency	100		2200	kHz
f_{SYNC}	Synchronization Pulse Frequency	200		2200	
T_J	Operating Junction Temperature(2)	–40		150	°C

(1) Recommended Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(3) The maximum TRK pin voltage is limited to 0.95V when upper VOUT range is selected.

6.4 Thermal Information

THERMAL METRIC(1)		LM5123-Q1 RGR(QFN) 20 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	43.3	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
R_{qJB}	Junction-to-board thermal resistance	17.8	°C/W
y_{JT}	Junction-to-top characterization parameter	0.8	°C/W
y_{JB}	Junction-to-board characterization parameter	17.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, , R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT(BIAS, VCC, VOUT)						
$I_{BIAS-SD}$	BIAS current in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V		2.5	5	µA
$I_{BIAS-ACTIVE}$	BIAS current in active (Non-switching, VCC is supplied by BIAS)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V		1.22	1.52	mA
$I_{BIAS-BYP}$	BIAS current in bypass mode	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V		1.22	1.52	mA
$I_{VOUT-SD}$	VOUT current in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V			1	µA
$I_{VOUT-BYP-DE}$	VOUT current in bypass mode	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{VOUT} = 12 V, MODE = GND		100	115	µA
$I_{VOUT-BYP-FPWM}$	VOUT current in bypass mode	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, V_{VOUT} = 12 V, MODE = VCC		240	276	µA

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, , R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VOUT-ACTIVE}$	VOUT current in active (Non-switching) (DE mode)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = GND		90	105	µA
	VOUT current in active (Non-switching), (FPWM)	V_{UVLO} = 2.5 V, V_{TRK} = 0.6 V, MODE = VCC		240	276	µA
$I_{BATTERY-SD}$	Battery drain in shutdown	V_{UVLO} = 0 V, V_{OUT} = 11.3 V		2.5	5	µA
$I_{BATTERY-DE}$	Battery drain in bypass mode (DE mode)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, MODE = GND		1.44	1.59	mA
$I_{BATTERY-FPWM}$	Battery drain in bypass mode (FPWM)	V_{UVLO} = 2.5 V, V_{TRK} = 0.25 V, MODE = VCC		1.58	1.74	mA
ENABLE, UVLO						
$V_{EN-RISING}$	Enable threshold	EN rising	0.45	0.55	0.65	V
$V_{EN-FALLING}$	Enable threshold	EN falling	0.35	0.45	0.55	V
V_{EN-HYS}	Enable hysteresis	EN falling	55	90	130	mV
$I_{UVLO-HYS}$	UVLO pull-down hysteresis current	V_{UVLO} = 0.7 V	8	10	12	µA
$V_{UVLO-RISING}$	UVLO threshold	UVLO rising	1.05	1.1	1.15	V
$V_{UVLO-FALLING}$	UVLO threshold	UVLO falling	1.025	1.075	1.125	V
$V_{UVLO-HYS}$	UVLO hysteresis	UVLO falling		25		mV
SYNC/DITHER/VH						
$V_{SYNC-RISING}$	SYNC threshold/SYNC detection threshold	SYNC rising			2	V
$V_{SYNC-FALLING}$	SYNC threshold	SYNC falling	0.4			V
	Minimum SYNC pull up pulse width				100	ns
I_{DITHER}	Dither source/sink current		16	21	26	µA
Δf_{SW1}	f_{SW} Modulation (Upper Limit)			5%		
Δf_{SW2}	f_{SW} Modulation (Lower Limit)			-6%		
$V_{DITHER-FALLING}$	Dither disable threshold		0.65	0.75	0.85	V
VCC						
$V_{VCC-REG1}$	VCC regulation	I_{VCC} = 100 mA	4.75	5	5.25	V
$V_{VCC-REG2}$	VCC regulation	No load	4.75	5	5.25	V
$V_{VCC-REG3}$	VCC regulation during dropout	V_{BIAS} = 3.8V, I_{VCC} = 100 mA	3.45			V
$V_{VCC-UVLO-RISING}$	VCC UVLO threshold	VCC rising	3.55	3.65	3.75	V
$V_{VCC-UVLO-FALLING}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V
I_{VCC-CL}	VCC sourcing current limit	V_{VCC} = 4 V	100			mA
CONFIGURATION (MODE)						
$V_{MODE-RISING}$	FPWM mode threshold	MODE rising			2.0	V
$V_{MODE-FALLING}$	Diode emulation mode threshold	MODE falling	0.4			V
RT						
V_{RT}	RT regulation			0.5		V
VREF, TRK, VOUT						
V_{REF}	VREF regulation target		0.99	1	1.005	V
$V_{OUT-REG}$	VOUT regulation target1 with resistor divider (lower VOUT range)	VREF resistor divider to make V_{TRK} = 0.25 V, R_{VREF} = 65 kΩ	4.915	5	5.085	V

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, , R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT-REG}$	VOUT regulation target2 with resistor divider (lower VOUT range)	VREF resistor divider to make V_{TRK} = 0.5 V, R_{VREF} = 65 kΩ	9.9	10	10.1	V
$V_{OUT-REG}$	VOUT regulation target3 with resistor divider (lower VOUT range)	VREF resistor divider to make V_{TRK} = 1.0 V, R_{VREF} = 65 kΩ	19.8	20	20.2	V
$V_{OUT-REG}$	VOUT regulation target4 with resistor divider (upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.25 V, R_{VREF} = 35 kΩ	14.74	15	15.24	V
$V_{OUT-REG}$	VOUT regulation target5 with resistor divider (upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.5 V, R_{VREF} = 35 kΩ	29.7	30	30.3	V
$V_{OUT-REG}$	VOUT regulation target6 with resistor divider (upper VOUT range)	VREF resistor divider to make V_{TRK} = 0.95 V, R_{VREF} = 35 kΩ	56.43	57	57.57	V
$V_{OUT-REG}$	VOUT regulation target1 using TRK (lower VOUT range)	V_{TRK} = 0.25 V, R_{VREF} = 65 kΩ	4.91	5	5.09	V
$V_{OUT-REG}$	VOUT regulation target2 using TRK (lower VOUT range)	V_{TRK} = 0.5 V, R_{VREF} = 65 kΩ	9.88	10	10.11	V
$V_{OUT-REG}$	VOUT regulation target3 using TRK (lower VOUT range)	V_{TRK} = 1.0 V, R_{VREF} = 65 kΩ	19.8	20	20.2	V
$V_{OUT-REG}$	VOUT regulation target4 using TRK (upper VOUT range)	V_{TRK} = 0.25 V, R_{VREF} = 35 kΩ	14.71	15	15.25	V
$V_{OUT-REG}$	VOUT regulation target5 using TRK (upper VOUT range)	V_{TRK} = 0.5 V, R_{VREF} = 35 kΩ	29.6	30	30.3	V
$V_{OUT-REG}$	VOUT regulation target6 using TRK (upper VOUT range)	V_{TRK} = 0.95 V, R_{VREF} = 35 kΩ	56.45	57	57.5	V
I_{TRK}	TRK bias current				1	µA
SOFT START, DE to FPWM TRANSITION						
I_{SS}	Soft-start current		17	20	23	µA
$V_{SS-DONE}$	MODE transition start	SS rising	1.3	1.5	1.7	V
R_{SS}	SS pull-down switch R_{DSON}			30	70	Ω
V_{SS-DIS}	SS discharge detection threshold		30	50	75	mV
V_{SS-FB}	internal SS to FB clamp	V_{FB}=0V		55	75	mV
CURRENT SENSE (CSP, CSN, SW, SENSE)						
V_{SLOPE}	Peak slope compensation amplitude	R_T = 220 kΩ, Referenced to CS input		45		mV
A_{CS}	Current sense amplifier gain	CSP=3.0V		10		V/V
	Current sense amplifier gain	CSP=1.5V		10		V/V
V_{CLTH}	Positive peak current limit threshold (CSP-CSN)	CSP=3.0V, MODE = GND	52	60	68	mV
	Positive peak current limit threshold (CSP-CSN)	CSP=1.5V, MODE = GND	51	60	72	mV
V_{ZCD-DE}	ZCD threshold (SW-SENSE)	MODE = GND		4		mV
$V_{I-NEG-FPWM}$	Negative current limit threshold (SW-SENSE)	MODE = VCC		–150		mV
V_{CS-FWD}	Forward current threshold voltage to enter bypass mode (CSP-CSN)	V_{ULVO} = 2.5 V, V_{TRK} = 0.25 V	2	6	10	mV
$V_{ZCD-BYP}$	Zero cross detection in bypass mode (DE mode) (SW-SENSE)	V_{ULVO} = 2.5 V, V_{TRK} = 0.25 V, MODE = GND		-5		mV

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, , R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I-NEG-BYP}$	Negative current limit in bypass mode (FPWM) (SW-SENSE)	V_{ULVO} = 2.5 V, V_{TRK} = 0.25 V, MODE = VCC		-150		mV
I_{CSN}	CSN bias current				1	µA
I_{CSP}	CSP bias current			110		µA
BOOT FAULT PROTECTION (HB)						
	Maximum replenish pulse cycles			4		cycles
	Replenish off cycles			12		cycles
	Number of sets to enter hiccup mode protection			4		sets
	Off-cycle during hiccup mode off			512		cycles
ERROR AMPLIFIER (COMP)						
Gm	Transconductance			1		mA/V
$I_{SOURCE-MAX}$	Maximum COMP sourcing current	V_{COMP}=0V	95			µA
$I_{SINK-MAX}$	Maximum COMP sinking current	V_{COMP}=1.8V	90			µA
$V_{CLAMP-MAX}$	COMP maximum clamp voltage	COMP rising	2.05	2.4	2.8	V
$V_{CLAMP-MIN}$	COMP minimum clamp voltage	COMP falling		0.65		V
PULSE WIDTH MODULATION (PWM)						
f_{SW1}	Switching frequency	R_T = 220 kΩ	85	100	115	kHz
f_{SW2}	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
t_{ON-MIN}	Minimum controllable on-time	R_T = 9.09 kΩ	14	20	50	ns
$t_{OFF-MIN}$	Minimum forced off-time	R_T = 9.09 kΩ	70	95	115	ns
D_{MAX1}	Maximum duty cycle limit	R_T = 220kΩ	90%	94%	98%	
D_{MAX2}	Maximum duty cycle limit	R_T = 9.09 kΩ	75%	80%	83%	
PGOOD, OVP						
$V_{OVTH-RISING}$	Overvoltage threshold (OVP threshold)	VOUT rising (referenced to $V_{OUT-REG}$)	108.5%	110%	113.5%	
$V_{OVTH-FALLING}$	Overvoltage threshold (OVP threshold)	VOUT falling (referenced to $V_{OUT-REG}$)	100.5%	103%	105.5%	
$V_{OVTH-DLY}$	Delay before entering bypass mode			30		us
$V_{UVTH-RISING}$	Undervoltage threshold (PGOOD threshold)	VOUT rising (referenced to $V_{OUT-REG}$)	91.5%	94%	98%	
$V_{UVTH-FALLING}$	Undervoltage threshold (PGOOD threshold)	VOUT falling (referenced to $V_{OUT-REG}$)	89.5%	92%	95.5%	
	UV comparator deglitch filter	Rising edge		26		µs
	UV comparator deglitch filter	Falling edge		21		µs
R_{PGOOD}	PGOOD pull-down switch R_{DSON}			90	180	Ω
	Minimum BIAS for valid PGOOD				2.5	V
MOSFET DRIVER						
	High-state voltage drop (HO driver)	100mA sinking		0.08	0.15	V
	Low-state voltage drop (HO driver)	100mA sourcing		0.04	0.1	V
	High-state voltage drop (LO driver)	100mA sinking		0.08	0.17	V

6.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 125 °C. Unless otherwise stated, V_{BIAS} = 12 V, V_{VOUT} = 12 V, R_T = 9.09 kΩ, , R_{VREF} = 65 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low-state voltage drop (LO driver)	100mA sourcing		0.04	0.1	V
$V_{HB-UVLO}$	HB-SW UVLO threshold	HB-SW falling	2.2	2.5	3.0	V
t_{DHL}	HO off to LO on deadtime			20		ns
t_{DLH}	LO off to HO on deadtime			22		ns
	HB diode resistance			1.2		Ω
I_{CP}	HB charge pump current	BIAS=3.8V	30	55		µA
THERMAL SHUTDOWN						
$T_{TSD-RISING}$	Thermal shutdown threshold	Temperature rising		175		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis			15		°C

6.6 Typical Characteristics

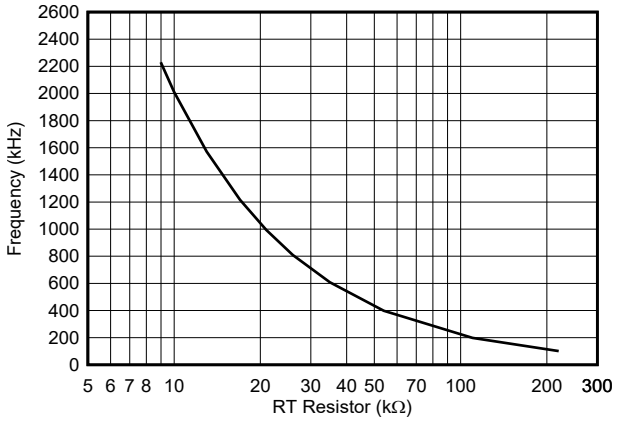


図 6-1. Frequency vs RT Resistance

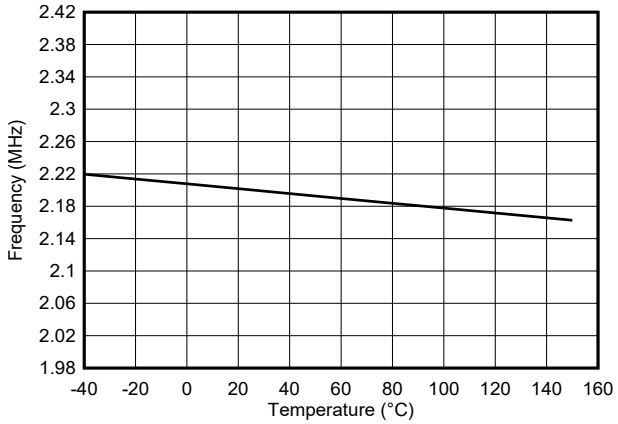


図 6-2. RT Frequency vs Temperature (RT = 9.09 kΩ, f_{SW} = 2.2 MHz)

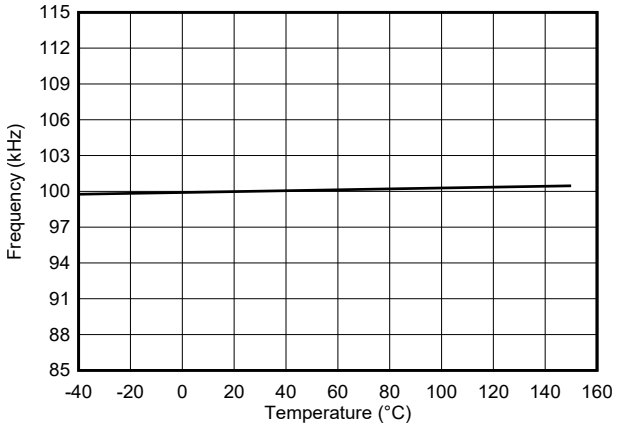


図 6-3. RT Frequency vs Temperature (RT = 220 kΩ, f_{SW} = 100 kHz)

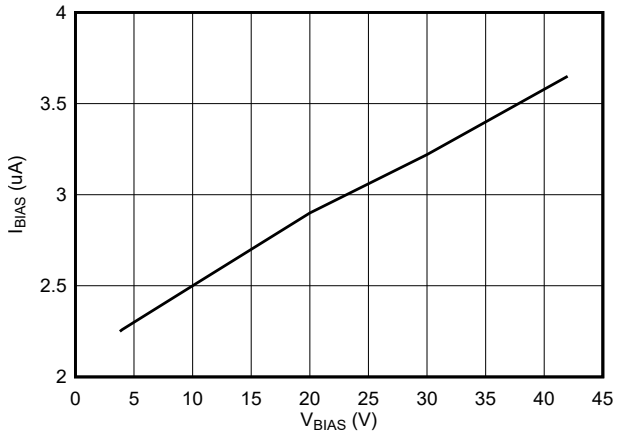


図 6-4. V_{BIAS} vs I_{BIAS} (shutdown mode)

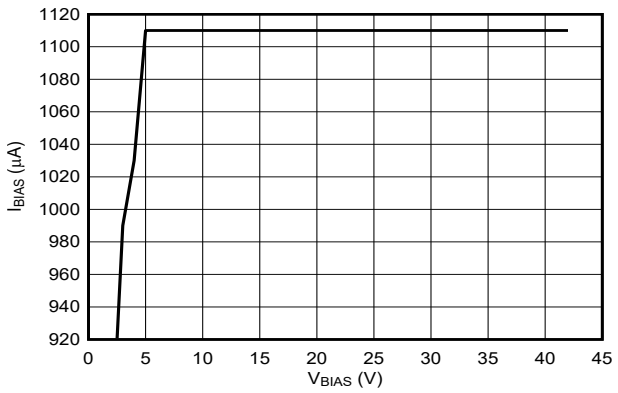


図 6-5. V_{BIAS} vs I_{BIAS} (active mode)

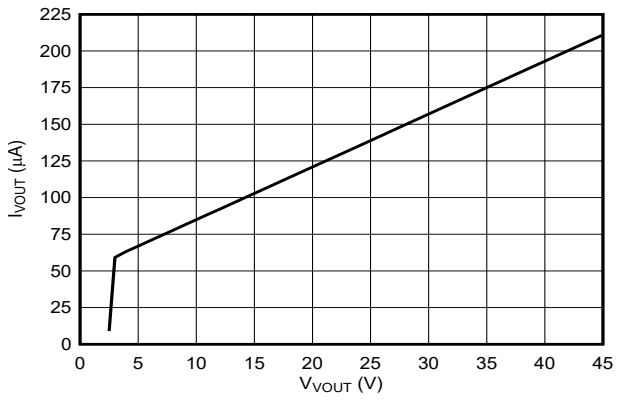


図 6-6. Bypass DEM

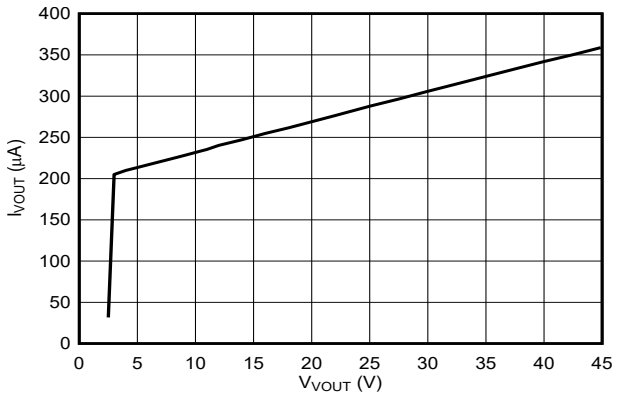


図 6-7. V_{VOUT} vs I_{VOUT} (bypass mode)

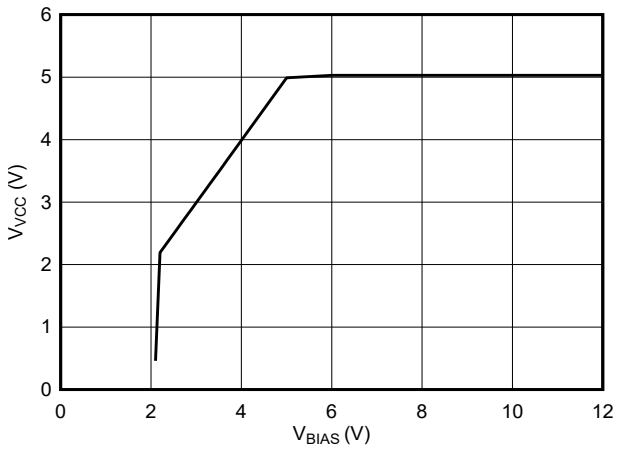


図 6-8. V_{BIAS} vs V_{VCC}

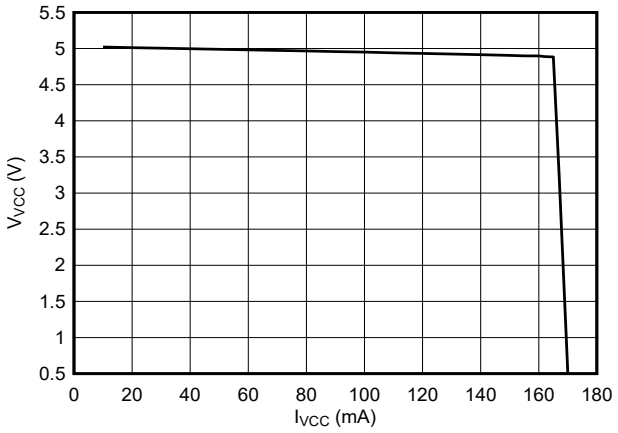


図 6-9. V_{VCC} vs I_{VCC}

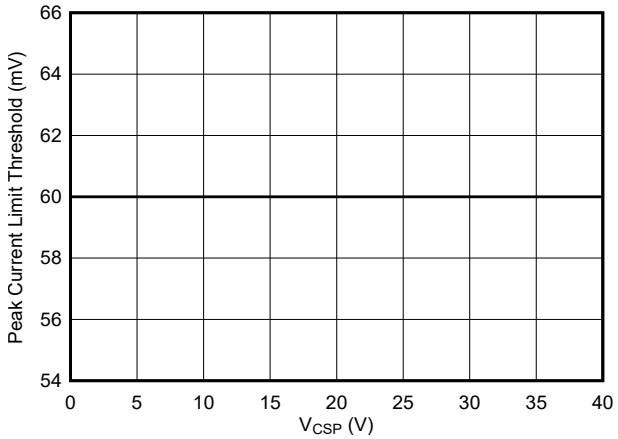


図 6-10. Peak current limit threshold V_{CLTH} vs V_{CSP}

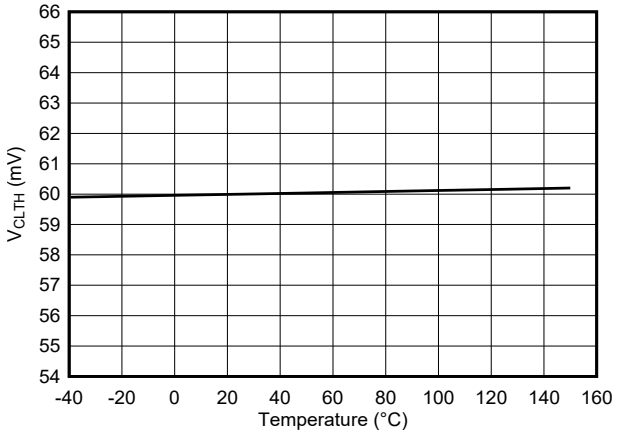


図 6-11. Peak current limit threshold V_{CLTH} vs Temperature, V_{CSP} = 3 V

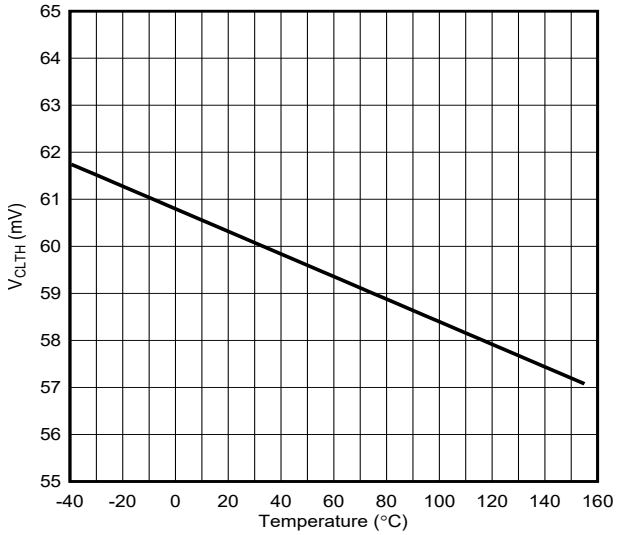


図 6-12. Bypass forward current threshold, V_{CS-FWD} vs Temperature , V_{CSP} = 3 V

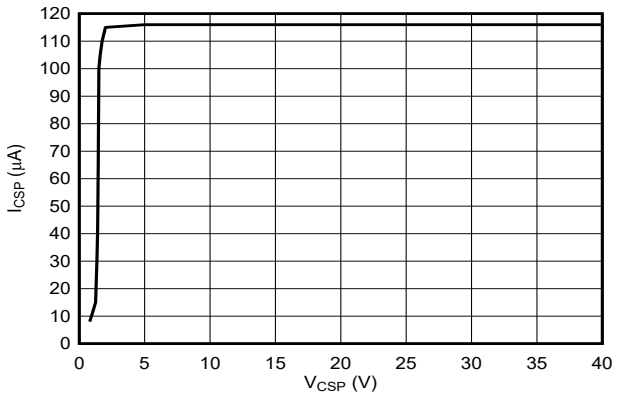


図 6-13. I_{CSP} vs V_{CSP} (active mode)

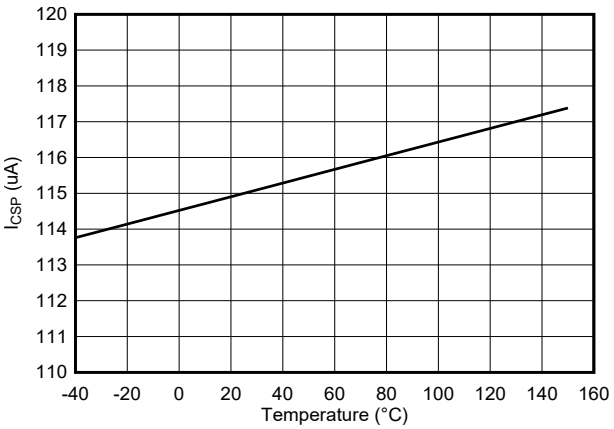


図 6-14. I_{CSP} vs temperature (active mode) V_{CSP} = 3 V

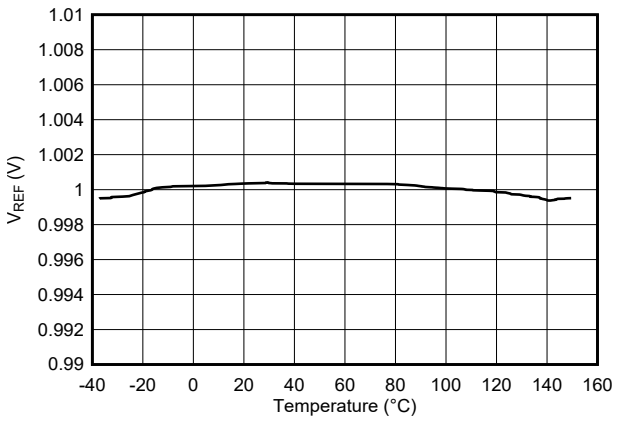


図 6-15. V_{REF} vs Temperature

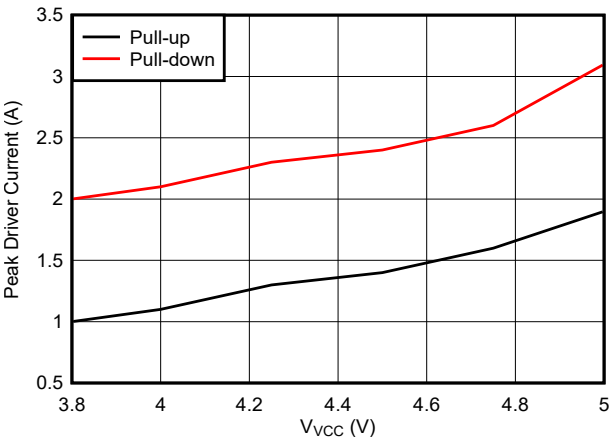


図 6-16. V_{VCC} vs Peak Driver Current

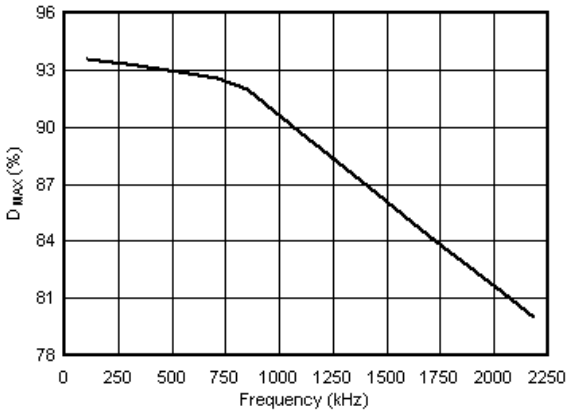


図 6-17. DMAX vs Switching Frequency

7 Detailed Description

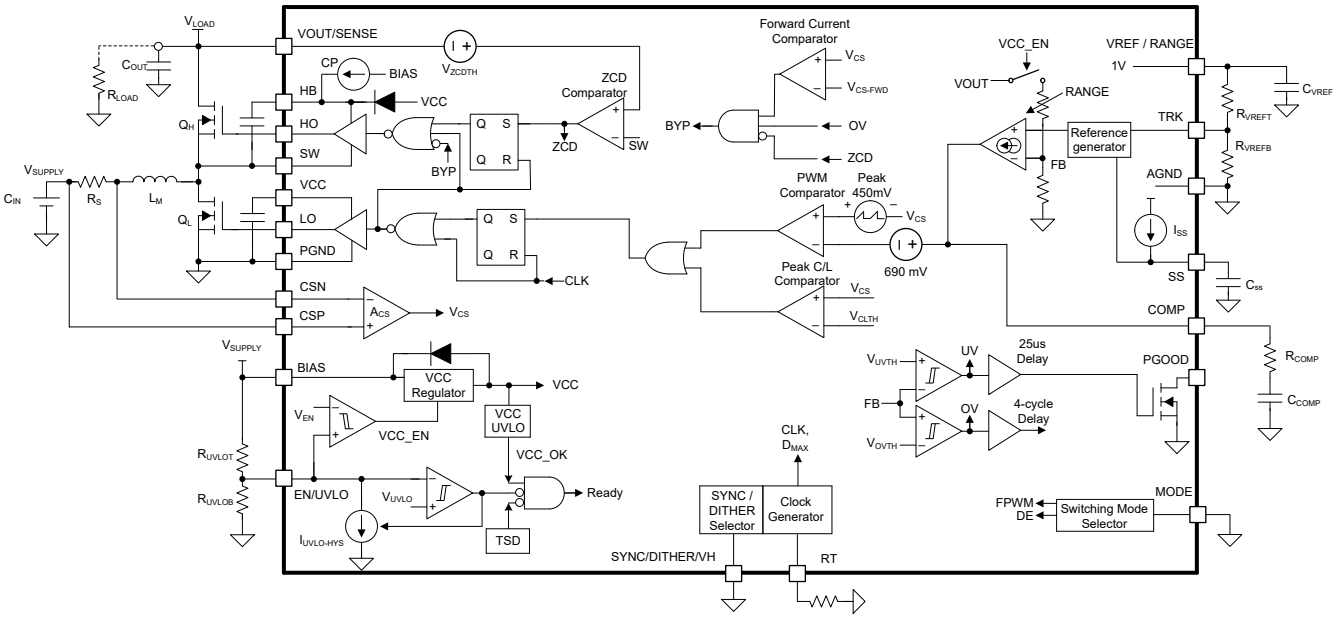
7.1 Overview

The LM51231-Q1 device is a wide input range synchronous boost controller that employs peak current mode control. The output voltage can be dynamically programmed by using the tracking function on the TRK pin. Bypass mode operation is automatically entered when the supply voltage is greater than the boost output regulation target. Bypass mode eliminates the need for an external bypass switch, by driving the high-side MOSFET at 100% duty cycle, decreasing the power dissipation by eliminating the high-side body diode voltage drop.

The device's wide input range supports automotive cold-crank and load dump. The minimum input voltage can be as low as 0.8 V when BIAS is equal to or greater than 3.8 V. The switching frequency is dynamically programmed with an external resistor from 100 kHz to 2.2 MHz. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response. Controller architecture simplifies thermal management at harsh ambient temperature conditions when compared to converter architectures.

The device has built-in protection features such as peak current limit, which is constant over input voltage, overvoltage protection, and thermal shutdown. External clock synchronization, programmable spread spectrum modulation, and a lead-less package with minimal parasitic, help reduce EMI and avoid cross talk. Additional features include line UVLO, FPWM, diode emulation, DCR inductor current sensing, programmable soft start, and a power-good indicator.

7.2 Functional Block Diagram



7.3 Feature Description

注

Read through セクション 7.4 before reading the feature description of the device. It is recommended to understand which device functional modes and what type of light load switching modes are supported by the device.

The parameters or thresholds values mentioned in this section are reference values unless otherwise specified. Refer to the セクション 6.5 to find the minimum, maximum, and typical values.

7.3.1 Device Enable/Disable (EN, VH Pin)

The device shuts down when EN is less than the EN threshold (V_{EN}) and VH is less than the SYNC threshold (V_{SYNC}). The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}. The VH pin provides a 40-µs internal delay before the device shuts down.

The device provides a 33-kΩ internal EN pulldown resistor to prevent a false turnon when the pin is floating. The EN pulldown resistor is connected to ground during the device configuration time or when the device shuts down. If the device configuration is finished and VH is greater than V_{SYNC}, EN hysteresis is accomplished by disconnecting/connecting the resistor when EN is greater/less than V_{EN}.

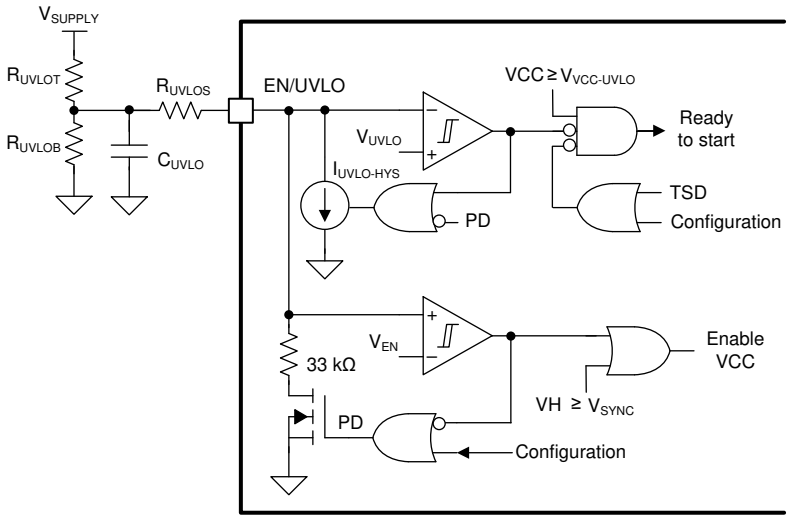


図 7-1. EN/UVLO Circuit

7.3.2 High Voltage VCC Regulator (BIAS, VCC Pin)

The device features a high voltage 5-V VCC regulator which is sourced from the BIAS pin. The internal VCC regulator turns on 50 µs after the device is enabled, and 120 µs device configuration starts when VCC is above VCC UVLO threshold ($V_{VCC-UVLO}$). The device configuration is reset when the device shuts down or VCC falls down below $V_{VCC-UVLO-FALLING}$. The preferred way to reconfigure the device is to shut down the device. During configuration time, the VOUT range is selected.

The high voltage VCC regulator allows the connection of the BIAS pin directly to supply voltages from 3.8 V to 42 V. When BIAS is less than the 5-V VCC regulation target ($V_{VCC-REG}$), the VCC output tracks the BIAS pin voltage with a small dropout voltage which is caused by 1.7-Ω resistance of the VCC regulator.

The recommended VCC capacitor value is 4.7 µF. The VCC capacitor should be populated between VCC and PGND as close to the device. The recommended BIAS capacitor value is 1.0 µF. The BIAS capacitor must be populated between BIAS and PGND close to the device.

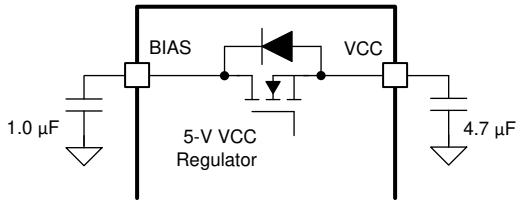


図 7-2. High Voltage VCC Regulator

The VCC regulator features a VCC current limit function that prevents device damage when the VCC pin is shorted to ground accidentally. The minimum sourcing capability of the VCC regulator is 100 mA (I_{VCC-CL}) during either the device configuration time or active mode operation. The minimum sourcing capability of the VCC regulator is reduced to 1 mA when EN/UVLO is less than V_{EN} and VH is greater than V_{SYNC}. The VCC regulator

supplies the internal drivers and other internal circuits. The external MOSFETs must be carefully selected to make the driver current consumption less than I_{VCC-CL}. The driver current consumption can be calculated in 式 1.

$$I_G = 2 \times Q_{G@5V} \times f_{SW} \quad (1)$$

where

- $Q_{G@5V}$ is the N-channel MOSFET gate charge at 5 V gate-source voltage

If VIN operation below 3.8 V is required, the BIAS pin can be connected to the output of the boost converter (V_{LOAD}). By connecting the BIAS pin to V_{LOAD}, the boost converter input voltage (V_{SUPPLY}) can drop down to 0.8 V if the BIAS pin is greater than 3.8 V. See *セクション 7.3.17* for more detailed information about the minimum V_{SUPPLY}.

7.3.3 Light Load Switching Mode Selection (MODE Pin)

The light load switching mode is selected based on the state of the MODE pin. If the MODE pin voltage is less than 0.4 V ($V_{MODE-FALLING}$) or floating, the device is configured to diode emulation (DE) mode. If the MODE pin voltage is greater than 2.0 V ($V_{MODE-RISING}$) or connected to VCC, the device is configured to forced PWM (FPWM) mode. The light load switching mode can be dynamically changed between DE and FPWM mode during operation. If the MODE pin is left floating the default light load switching mode is DE mode.

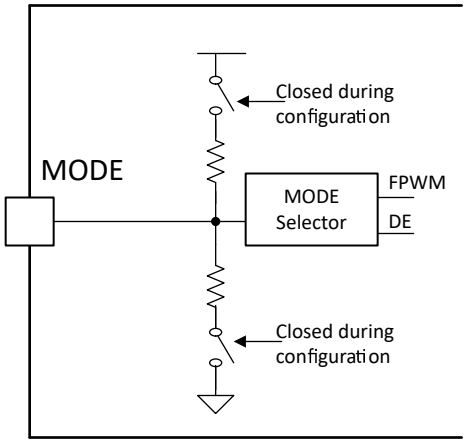


図 7-3. MODE Selection Circuit

7.3.4 VOUT Range Selection (RANGE Pin)

The programmable V_{OUT} range is selected during the device configuration and it cannot be changed until you reconfigure the device. Lower V_{OUT} range (5 V to 20 V) is selected if the resistance from VREF to AGND (R_{VREFT} + R_{VREFB}) is in the range of 75 kΩ to 100 kΩ during the device configuration. Upper V_{OUT} range (15 V to 57 V) is selected if the resistance from VREF to AGND is in the range of 20 kΩ to 35 kΩ during the device configuration. The accuracy of the V_{OUT} regulation is within the selected range.

7.3.5 Line Undervoltage Lockout (UVLO Pin)

When UVLO is greater than the UVLO threshold (V_{UVLO}), the device enters active mode if the device configuration is finished. UVLO hysteresis is accomplished with an internal 25-mV voltage hysteresis ($V_{UVLO-HYS}$) at the UVLO pin, and an additional 10-µA current sink ($I_{UVLO-HYS}$) that is switched on or off. When the UVLO pin voltage exceeds V_{UVLO}, the current sink is disabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below V_{UVLO} or during the device configuration time, the current sink is enabled, causing the voltage at the UVLO pin to fall quickly.

The external UVLO resistor voltage divider (R_{UVLOT}, R_{UVLOB}) must be designed so that the voltage at the UVLO pin is greater than V_{UVLO} when V_{SUPPLY} is in the desired operating range. The values of R_{UVLOT} and R_{UVLOB} can be calculated as follows.

$$R_{UVLOT} = \frac{\left(V_{SUPPLY\_ON} - \frac{V_{UVLO\_RISING}}{V_{UVLO\_FALLING}} \times V_{SUPPLY\_OFF}\right)}{I_{UVLO\_HYS}} \quad (2)$$

$$R_{UVLOB} = \frac{V_{UVLO\_FALLING} \times R_{UVLOT}}{V_{SUPPLY\_OFF} - V_{UVLO\_FALLING}} \quad (3)$$

A UVLO capacitor (C_{UVLO}) is required in case V_{SUPPLY} drops below $V_{SUPPLY-OFF}$ momentarily during the start-up or during a severe load transient at the low input voltage. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO pin when $I_{UVLO-HYS}$ is disabled.

The UVLO pin can be connected to the BIAS pin if not used. Drive the UVLO pin through a minimum of a 5-kΩ resistor if the BIAS pin voltage is less than the UVLO pin voltage in any conditions.

7.3.6 Fast Restart using VCC HOLD (VH Pin)

After the device configuration, a fast restart can be achieved without reconfiguration by toggling EN/UVLO when VH is greater than V_{SYNC}. The device stops switching, but keeps the VCC regulator active when EN is less than V_{EN} and VH is greater than V_{SYNC} (See 図 7-5).

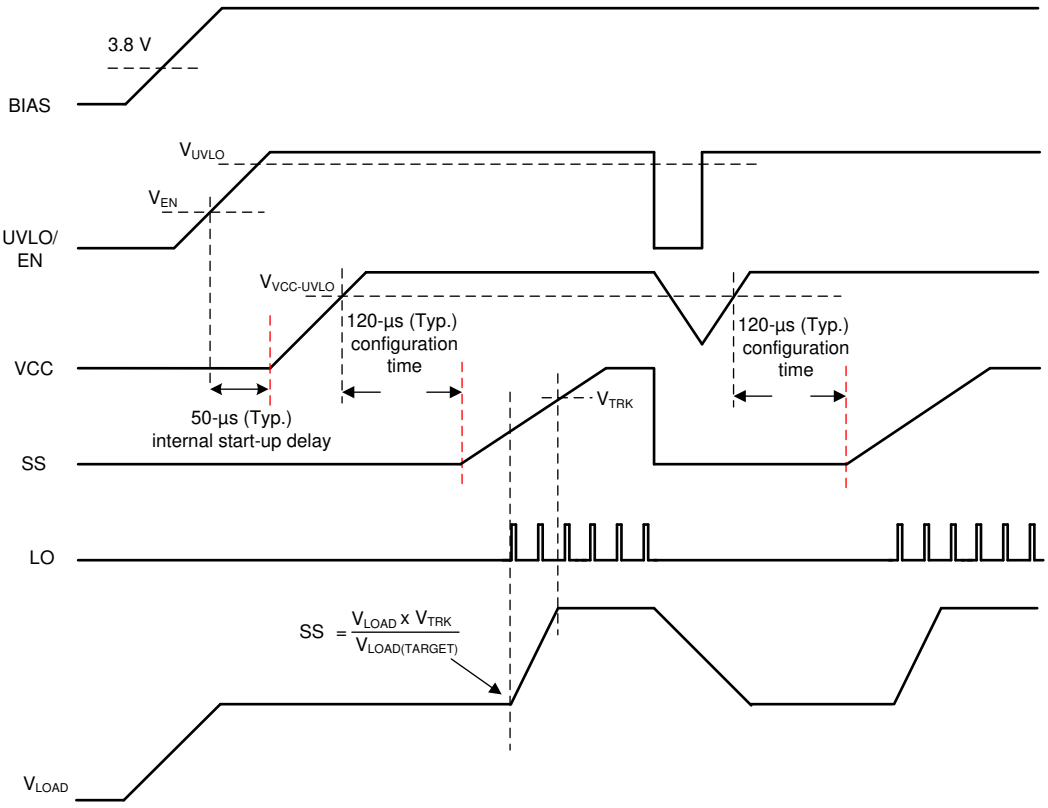


図 7-4. Boost Start-up Waveforms Case 1: Start-up by EN/UVLO, Restart when VH < V_{SYNC}

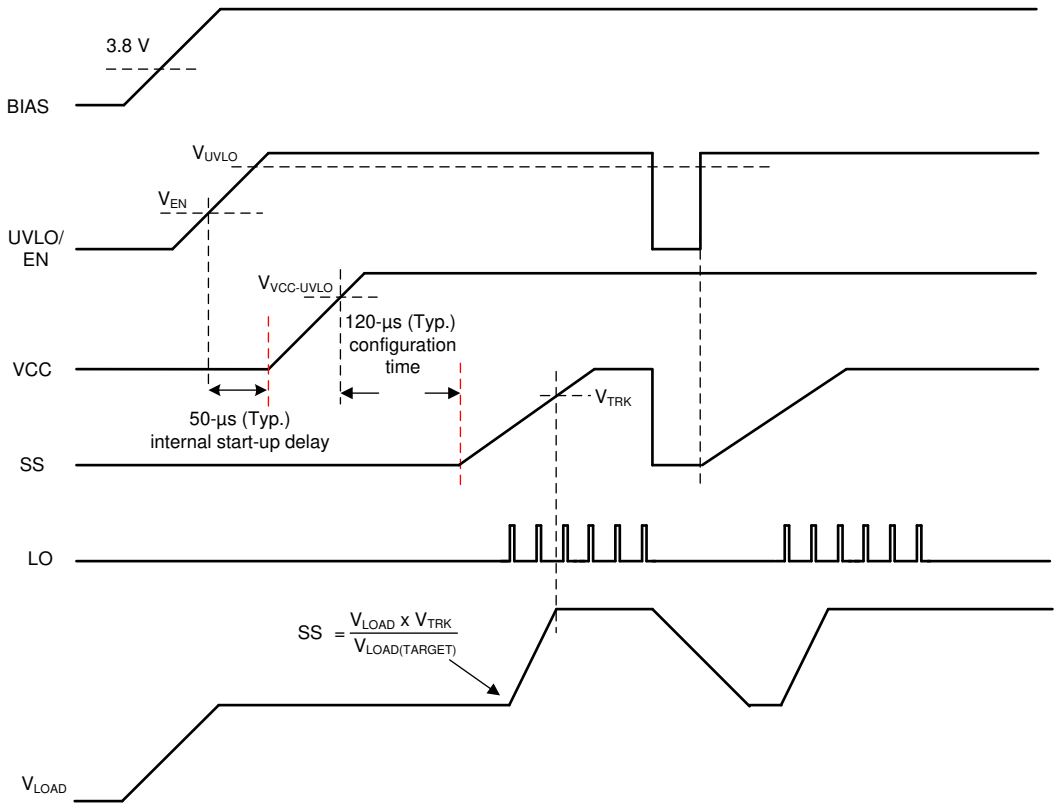


図 7-5. Boost Start-up Waveforms Case 2: Start-up by EN/UVLO, Restart when VH > V_{SYNC}

7.3.7 Adjustable Output Regulation Target (VOUT, TRK, VREF Pin)

The V_{OUT} regulation target ($V_{OUT-REG}$) is adjustable by programming the TRK pin voltage which is the reference of the internal error amplifier. The accuracy of $V_{OUT-REG}$ is ensured when the TRK voltage is between 0.25 V and 1.0 V. If the V_{OUT} regulation set point is set outside of the V_{OUT} range selection, V_{OUT} is still regulated. The high impedance TRK pin allows users to program the pin voltage directly by a D/A converter or by connecting to a resistor voltage divider (R_{VREFT}, R_{VREFB}) between VREF and AGND. See 図 7-6.

The device provides a 1-V voltage reference (V_{REF}) which can be used to program the TRK pin voltage through a resistor voltage divider. It is not recommended to use V_{REF} as a reference voltage of an external circuit. For stability reasons the VREF capacitor (C_{VREF}) should be between 330 pF and 1 nF, 470 pF are recommended.

When R_{VREFT} and R_{VREFB} are used to program the TRK pin voltage, $V_{OUT-REG}$ can be calculated as follows.

Lower VOUT Range

$$V_{OUT\_REG} = \frac{20 \times R_{VREFB}}{R_{VREFB} + R_{VREFT}} \quad (4)$$

Upper VOUT Range

$$V_{OUT\_REG} = \frac{60 \times R_{VREFB}}{R_{VREFB} + R_{VREFT}} \quad (5)$$

The TRK pin voltage can be dynamically programmed in active mode, which makes an envelope tracking power supply design easy. When designing a tracking power supply, it is required to adjust the TRK pin voltage slow enough so that the VOUT pin voltage can track the command and the internal overvoltage or undervoltage comparator is not triggered during the transient operation. It is recommended to use an RC filter at the TRK pin to slow down the slew rate of the command signal at the TRK pin, especially when a step input is applied. When a trapezoidal or sinusoidal input is applied, it is recommended to limit the slew rate or the frequency of the

command signal. Bypass mode, OVP and PGOOD functions are based on the TRK pin voltage, see セクション 7.4.1.4, セクション 7.3.8, セクション 7.3.9 respectively.

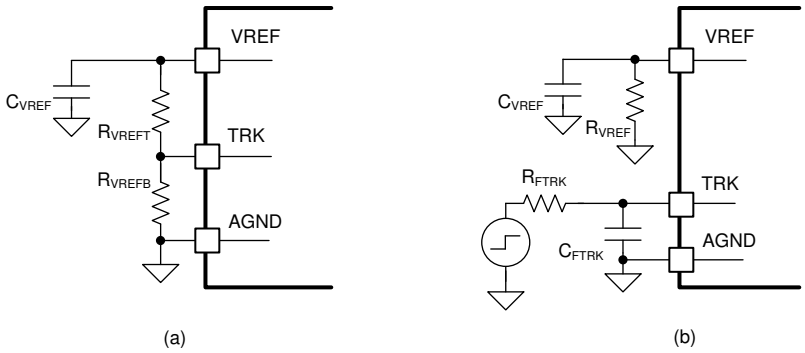


図 7-6. TRK Control (a) using VREF (b) by External Step Input

7.3.8 Overvoltage Protection (VOUT Pin)

The device provides an overvoltage protection (OVP) for boost converter output. The OVP comparator monitors the VOUT pin through an internal resistor voltage resistors. If the VOUT pin voltage rises above the overvoltage threshold (V_{OVTH}), OVP is activated. When OVP is triggered, the device turns off the low-side driver and turns on the high-side driver until zero current is detected in diode emulation. In FPWM mode, the low-side driver is not turned off when the OVP is triggered.

After at least 30 µs ($V_{OVTH-DLY}$) in OVP status, the device enters the OVP condition. The recommended capacitor from the VOUT pin to PGND (C_{VOUT}) is 0.1 µF.

7.3.9 Power Good Indicator (PGOOD Pin)

The device provides a power-good indicator (PGOOD) to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor between 5 kΩ and 100 kΩ can be externally connected. The PGOOD switch opens when the VOUT pin voltage is greater than the undervoltage threshold (V_{UVTH}). The PGOOD pin is pulled down to ground when the VOUT pin voltage is less than V_{UVTH}, UVLO is less than V_{UVLO}, VCC is less than $V_{VCC-UVLO}$, or during thermal shutdown. A 26-µs rising and 21-µs falling deglitch filter prevents any false pulldown of the PGOOD due to transients. The PGOOD pin voltage cannot be greater than V_{VOUT} + 0.3 V

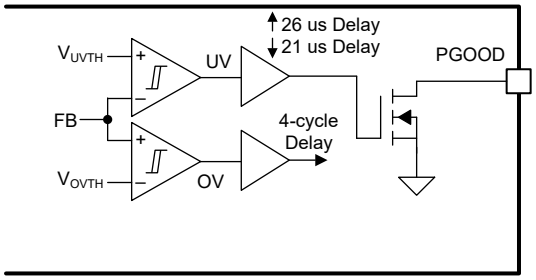


図 7-7. PGOOD Indicator

7.3.10 Dynamically Programmable Switching Frequency (RT)

The switching frequency of the device is set by a single RT resistor connected between RT and AGND if no external synchronization clock is applied to the SYNC pin. The resistor value to set the RT switching frequency (R_T) is calculated as follows.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(typical)}} - 955 \quad (6)$$

The RT pin is regulated to 0.5 V by an internal RT regulator when the device is in active mode or during the device configuration. The switching frequency can be dynamically programmed during operation as shown in 図 7-8.

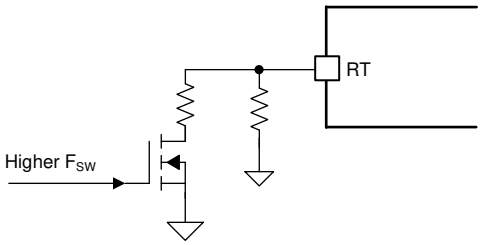


図 7-8. Frequency Hopping Example

7.3.11 External Clock Synchronization (SYNC Pin)

The switching frequency of the device can be synchronized to an external clock by directly applying an external pulse signal to the SYNC pin. The internal clock is synchronized at the rising edge of the external synchronization pulse using an internal PLL. Connect the SYNC pin to ground if not used.

The external synchronization pulse must be greater than V_{SYNC} in the high logic state and must be less than V_{SYNC} in the low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum on-pulse and the minimum off-pulse widths must be greater than 100 ns. The frequency of the external synchronization pulse must satisfy the following two inequalities.

$$200kHz \le f_{SYNC} \le 2.2MHz \quad (7)$$

$$0.75 \times f_{RT(typical)} \le f_{SYNC} \le 1.5 \times f_{RT(typical)} \quad (8)$$

For example, an RT resistor is required for typical 350-kHz switching to cover from 263-kHz to 525-kHz clock synchronization without changing the RT resistor.

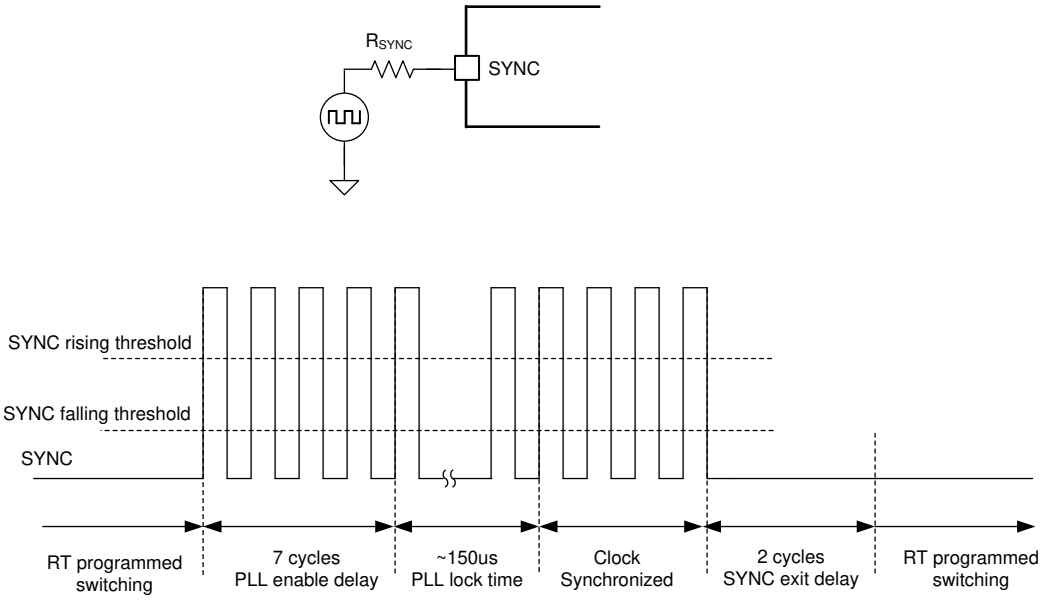


図 7-9. External Clock Synchronization

Drive the SYNC pin through a minimum 1-kΩ resistor if the BIAS pin voltage is less than the SYNC pin voltage in any conditions.

7.3.12 Programmable Spread Spectrum (DITHER Pin)

The device provides an optional programmable spread spectrum (clock dithering) function that is activated by connecting a capacitor between DITHER and AGND. A triangular waveform centered at 1.0 V is generated across the dither capacitor. This triangular waveform modulates the oscillator frequency by –6% to +5% of the frequency set by the RT resistor. The dither capacitance value sets the rate of the low frequency modulation.

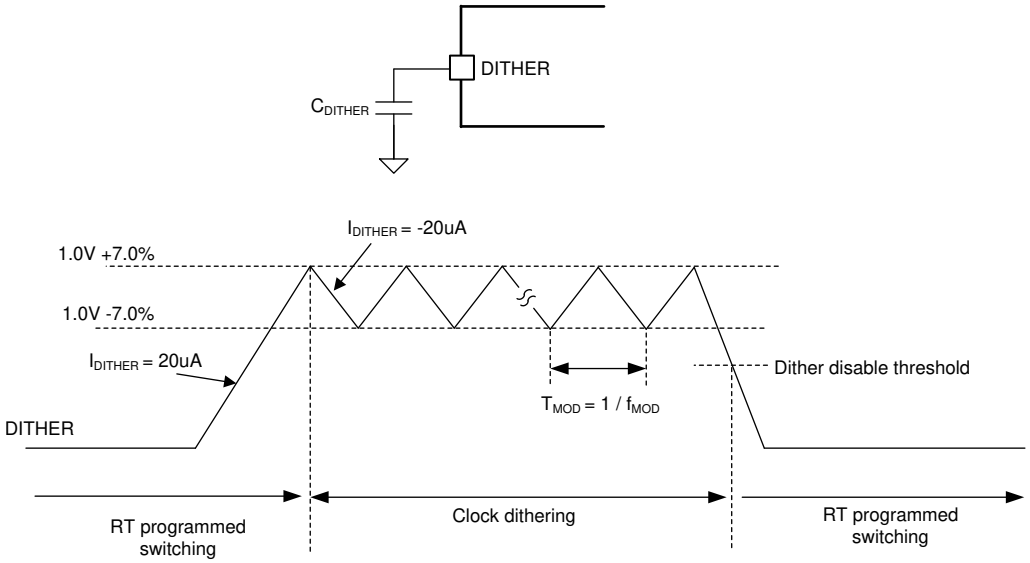


図 7-10. Switching Frequency Dithering

For the dithering circuit to effectively reduce peak EMI, the modulation frequency must be much less than the RT switching frequency. The dither capacitance which is required for a given modulation frequency (f_{MOD}), can be calculated from 式 9. Setting the f_{MOD} to 9 kHz or 10 kHz is a good starting point.

$$C_{DITHER} = \frac{20\mu A}{f_{MOD} \times 0.29} \quad (9)$$

Connecting DITHER to AGND deactivates clock dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Clock dithering is also disabled when an external synchronization pulse is applied.

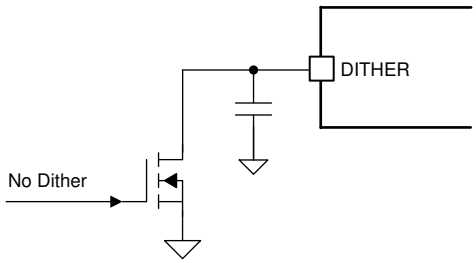


図 7-11. Dynamic Dither On/Off Example

7.3.13 Programmable Soft-start (SS Pin)

The soft-start feature helps the converter gradually reach the steady state operating point. To reduce start-up stresses and surges, the device regulates the error amplifier reference to the SS pin voltage or the TRK pin voltage (V_{TRK}), whichever is lower.

The internal 20-µA soft-start (I_{SS}) current turns on 120 µs after the VCC pin crosses $V_{VCC-UVLO}$. I_{SS} gradually increases the voltage on an external soft-start capacitor (C_{SS}). This results in a gradual rise of the output voltage.

In FPWM mode, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin voltage is greater than 1.5 V, the device changes the high-side negative current limit threshold from V_{ZCD-DE} to $V_{I-HS-NEG}$.

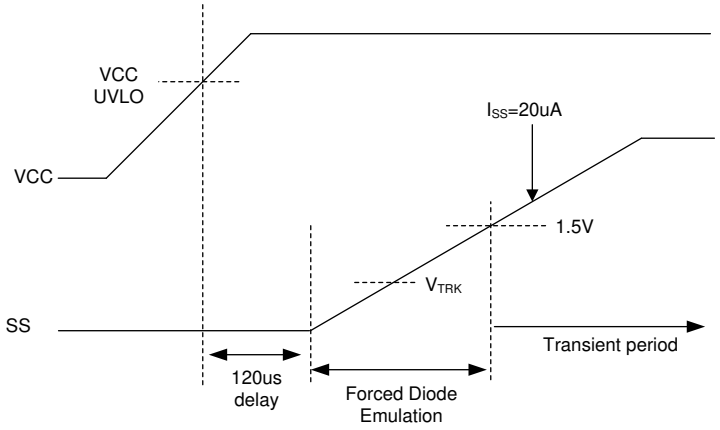


図 7-12. Soft Start and Smooth Transition to FPWM

In boost topology, the soft-start time (t_{SS}) varies with the input supply voltage because the boost output voltage is equal to the boost input voltage at the beginning of the soft-start switching. t_{SS} in boost topology is calculated in 式 10.

$$t_{SS} = V_{TRK} \times \frac{C_{SS}}{20\mu A} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \quad (10)$$

In general, it is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state. If the device is used for a pre-boost in automotive application, it is recommended to use 100-pF C_{SS} to reach steady state as soon as possible.

The device also features an internal SS-to-FB clamp (V_{SS-FB}), which clamps SS 55 mV above FB and is activated if 256 consecutive switching cycles occur with current limit. The SS-to-FB clamp is deactivated if 32 consecutive switching cycles occur without exceeding the current limit threshold. This clamp helps to minimize surges after output shorts or over load situations. The device can enter deep sleep mode when SS is greater than 1.5 V. It is not recommended to pulldown SS to stop switching.

7.3.14 Wide Bandwidth Transconductance Error Amplifier and PWM (TRK, COMP Pin)

The device includes an internal feedback resistor voltage divider. The internal feedback resistor voltage divider is connected to the negative input of the internal transconductance error amplifier, and the TRK pin voltage programs the positive input of the internal transconductance error amplifier after the soft start is finished. The internal transconductance error amplifier features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz) and sinks (or sources) current which is proportional to the difference between the negative and the positive inputs of the error amplifier.

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type-2 loop compensation network. R_{COMP}, C_{COMP}, and an optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency, a mid-band zero, and a high frequency pole.

The PWM comparator in 図 7-13 compares the sum of the amplified sensed inductor current and the slope compensation ramp with the sum of the COMP pin voltage and a –690 mV internal offset, and terminates the present cycle if the sum of the amplified sensed inductor current and the slope compensation ramp is greater than the sum of the COMP pin voltage and the –690 mV internal offset.

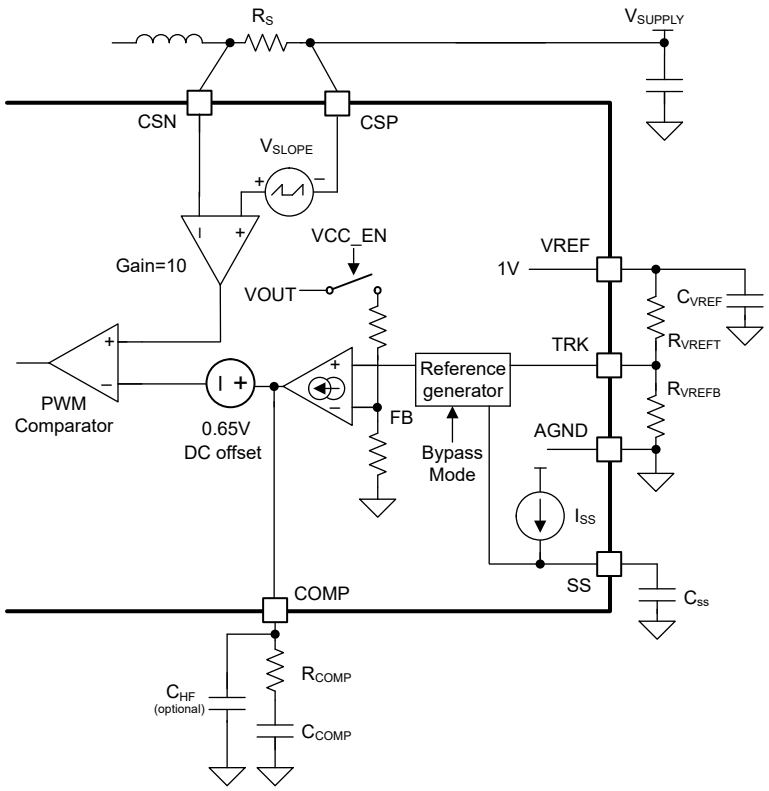


図 7-13. Error Amplifier, Current Sense Amplifier and PWM

7.3.15 Current Sensing and Slope Compensation (CSP, CSN Pin)

The device features a current sense amplifier with an effective gain of 10 (A_{CS}), and provides an internal slope compensation ramp to the PWM comparator to prevent a subharmonic oscillation at high duty cycle. The device generates the 45-mV peak slope compensation ramp (V_{SLOPE}) at the input of the current sense amplifier which is 0.45-V peak (at 100% duty cycle) slope compensation ramp at the PWM comparator input.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than at least half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of the slope compensation must satisfy 式 11.

$$0.5 \times (V_{LOAD} - V_{SUPPLY}) / L_M \times R_S \times \text{Margin} < V_{SLOPE} \times f_{SW} \text{ (in Boost)} \quad (11)$$

where

- 1.5-1.7 is recommended as the Margin to cover non-ideal factors.

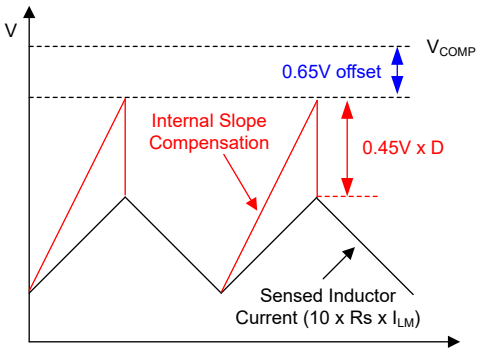


図 7-14. PWM Comparator Input

7.3.16 Constant Peak Current Limit (CSP, CSN Pin)

When the CSP-CSN voltage exceeds the 60-mV cycle-by-cycle current limit threshold (V_{CLTH}), the current limit comparator immediately terminates the LO output. The device provides an constant peak current limit whose peak inductor current limit is constant over the input and output voltage. For the case where the inductor current can overshoot, such as inductor saturation, the current limit comparator skips pulses until the current has decayed below the current limit threshold.

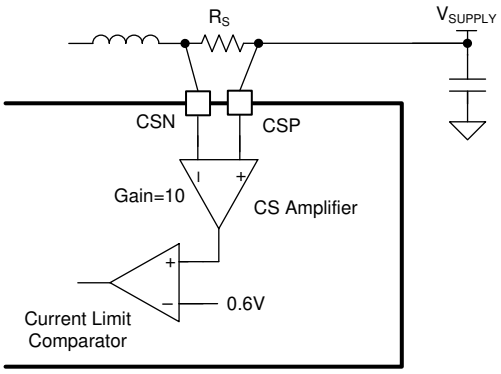


図 7-15. Current Limit Comparator

Cycle-by-cycle peak current limit is calculated as follows:

$$I_{PEAK-CL} = \frac{0.06}{R_S} \quad (12)$$

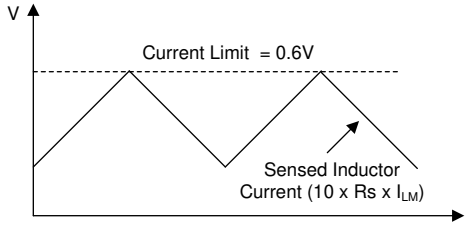


図 7-16. Current Limit Comparator Input

Boost converters have a natural pass-through path from the supply to the load through the high-side MOSFET body diode. Due to this path, boost converters cannot provide the peak current limit protection when the output voltage is close to or less than the input supply voltage, especially the peak current limit protection that does not work during the minimum on-time (t_{ON-MIN}).

7.3.17 Maximum Duty Cycle and Minimum Controllable On-time Limits

The device provides the maximum duty cycle limit (D_{MAX}) / minimum off-time to cover the non-ideal factors caused by resistive elements. D_{MAX} decides the minimum input supply voltage ($V_{SUPPLY(MIN)}$) which can achieve the target output voltage (V_{LOAD}) during CCM operation, but $V_{SUPPLY(MIN)}$ which can achieve the target output voltage during DCM operation is not limited by D_{MAX}. $V_{SUPPLY(MIN)}$, which can achieve the target output voltage during CCM operation, can be estimated as follows.

$$V_{SUPPLY(MIN)} \approx V_{LOAD} \times (1 - D_{MAX}) + I_{SUPPLY(MAX)} \times (R_{DCR} + R_S + R_{DS(ON)}) \quad (13)$$

where

- $I_{SUPPLY(MAX)}$ is the maximum input current at $V_{SUPPLY(MIN)}$
- R_{DCR} is the DC resistance of the inductor
- $R_{DS(ON)}$ is the on resistance of the MOSFET

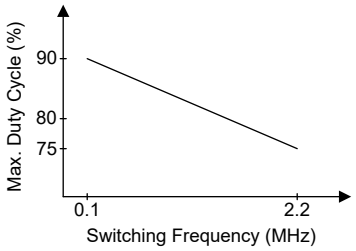


図 7-17. Switching Frequency vs max. Duty Cycle

At very light load condition or when V_{SUPPLY} is close to $V_{OUT-REG}$, the device skips the low-side driver pulses if the required on-time is less than t_{ON-MIN}. This pulse skipping appears as a random behavior. If V_{SUPPLY} is further increased to the voltage higher than $V_{OUT-REG}$, the required on-time becomes zero and eventually the device can start bypass operation which turns on the high-side driver 100% when the VOUT pin voltage is greater than V_{OVTH}.

7.3.18 MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LO, HO, HB Pin)

The device provides N-channel logic MOSFET drivers, which can source a peak current of 2.2 A and sink a peak current of 3.3 A. The LO driver is powered by VCC, and is enabled when EN is greater than V_{EN} and VCC is greater than $V_{VCC-UVLO}$. The HO driver is powered by HB, and is enabled when EN is greater than V_{EN} and HB-SW voltage is greater than HB UVLO threshold ($V_{HB-UVLO}$).

When the SW pin voltage is approximately 0 V by turning on the low-side MOSFET, the C_{HB} is charged from VCC through the internal boot diode. The recommended value of the C_{HB} is 0.1 µF.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs are not turned on at the same time. When the device commands LO to be turned on, the adaptive dead-time logic first turns off HO and waits for HO-SW voltage to drop. LO is then turned on after a small delay (t_{DHL}). Similarly, the HO driver turn-on is delayed until the LO-PGND voltage has discharged. HO is then turned on after a small delay (t_{DLH}).

If the BIAS pin voltage is below the 5-V VCC regulation target, take extra care when selecting the MOSFETs. The gate plateau voltage of the MOSFET switch must be less than the BIAS pin voltage to completely enhance the MOSFET, especially during start-up at low BIAS pin voltage. If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter may not start up properly and it can stick at the maximum duty cycle in a high-power dissipation state. This condition can be avoided by selecting a lower threshold MOSFET or by turning on the device when the BIAS pin voltage is sufficient. Care should be taken when the converter operates in bypass at any conditions. During the bypass operation, the minimum HO-SW voltage is 3.75 V.

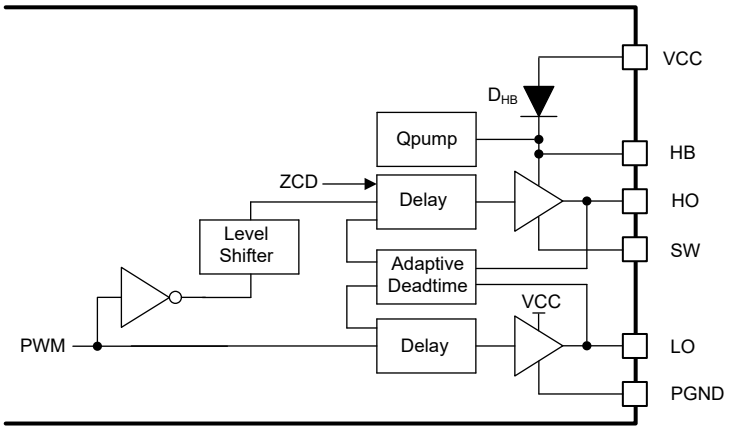


図 7-18. Driver Structure with Internal Boot Diode

The hiccup mode fault protection is triggered by the HB UVLO. If the HB-SW voltage is less than the HB UVLO threshold ($V_{HB-UVLO}$), the LO turns on by force for 75 ns to replenish the boost capacitor. The device allows up to four consecutive replenish switching. After the maximum four consecutive boot replenish switching, the device skips switching for 12 cycles. If the device fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching, the device stops switching and enters 512 cycles of hiccup mode off-time. During the hiccup mode off-time, PGOOD and SS are grounded.

If required, the slew rate of the switching node voltage can be adjusted by adding a gate resistor in parallel with pulldown PNP transistor. Extra care should be taken when adding the gate resistor since it can decrease the effective dead-time.

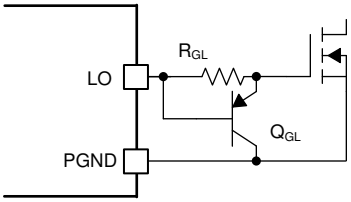


図 7-19. Slew Rate Control

7.3.19 Thermal Shutdown Protection

An internal thermal shutdown (TSD) is provided to protect the device if the junction temperature (T_J) exceeds 175°C. When TSD is activated, the device is forced into a low-power thermal shutdown state with the MOSFET drivers and the VCC regulator disabled. After the T_J is reduced (typical hysteresis is 15ºC), the device restarts.

7.4 Device Functional Modes

7.4.1 Device Status

7.4.1.1 Shutdown Mode

When EN is less than V_{EN} and VH is less than V_{SYNC}, the device shuts down, consuming 3 µA from BIAS. In shutdown mode, COMP, SS, and PGOOD are grounded. The device is enabled when EN is greater than V_{EN} or VH is greater than V_{SYNC}.

7.4.1.2 Configuration Mode

When the device is enabled initially, the 120-µs device configuration starts if VCC is greater than $V_{VCC-UVLO}$. During device configuration, the VOUT range is selected. The device configuration is reset when the device shuts down or VCC falls down below 2.2 V. The preferred way to reconfigure the device is to shut down the device. During the configuration time, a 33-kΩ internal EN pulldown resistor is connected, the minimum sourcing capability of the VCC regulator is 100 mA and the RT pin is regulated to 0.5 V by the internal RT regulator.

7.4.1.3 Active Mode

After the 120-µs initial device configuration is finished, the device enters active mode with all functions enabled if UVLO is greater than V_{UVLO}. In active mode, a soft-start sequence starts and the error amplifier is enabled.

7.4.1.4 Bypass Mode

Boost converters have a natural pass-through path from the supply to the load through the high-side MOSFET body diode when the supply voltage is greater than the target load voltage. During this operating condition, the high-side MOSFET dissipates power due to the forward voltage drop of the body diode. To reduce the power dissipation the high-side MOSFET (HO) is driven at 100% duty cycle and V_{LOAD} is approximately equal to V_{SUPPLY}. This mode of operation is called bypass mode.

The device behaves differently in bypass mode based on the selected light load switching mode operation, the sensed inductor current, and the input voltage. To enter bypass mode; the OVP status must be triggered for at least 30 µs ($V_{OVTH-DLY}$), see セクション 7.3.8 and the voltage between CSP and CSN must be greater than 6 mV (V_{CS-FWD}). To exit bypass mode either the OVP status is cleared, or $V_{SW-SENSE}$ is less than bypass mode zero

cross threshold. The bypass mode zero cross threshold is dependent on the selected light-load switching mode operation and detailed in セクション 7.4.1.4.1 and セクション 7.4.1.4.2, for DE mode and FPWM respectively.

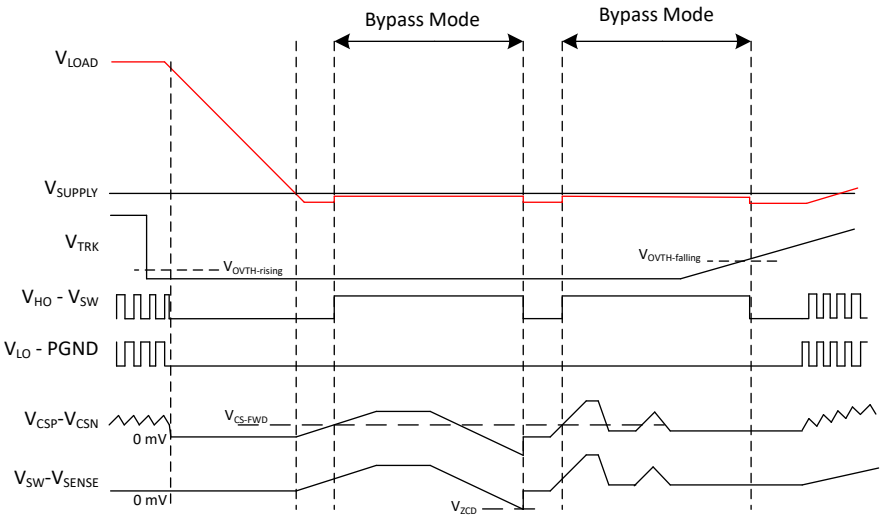


図 7-20. Bypass mode operation

7.4.1.4.1 Bypass DE mode

In DE mode switching operation, bypass mode is entered when the OVP status is triggered for at least 30 µs ($V_{OVTH-DLY}$), and $V_{CSP-CSN}$ is greater than 6 mV (V_{CS-FWD}), indicating positive inductor current. To exit bypass mode the either the OVP status is cleared or $V_{SW-SENSE}$ is less than -5 mV ($V_{ZCD-BYP}$). $V_{ZCD-BYP}$ indicates that current is flowing from V_{LOAD} to V_{SUPPLY} and the high-side FET is turned off to stop the negative current flow. Once the high-side FET is turned-off, the device enters active mode. The proper conditions must be achieved to enter bypass mode again. See 表 7-1 for details on how the device enters and exits bypass mode.

表 7-1. Bypass Mode: DE mode

	Conditions (1)
Enter bypass mode	$V_{VOUT} > V_{TRK} * K_{FB} * V_{OVTH\_RISING}$ AND $V_{CSP-CSN} > V_{CS-FWD}$
Exit bypass mode	$V_{VOUT} < V_{TRK} * K_{FB} * V_{OVTH\_FALLING}$ OR $V_{SW-SENSE} < V_{ZCD-BYP}$

(1) K_{FB} is either 20 or 60 depending on the selected output voltage range. See section セクション 7.3.7

7.4.1.4.2 Bypass FPWM

In FPWM switching operation, the device enters bypass mode when the OVP status is triggered for at least 30 µs ($V_{OVTH-DLY}$) and $V_{CSP-CSN}$ is greater than 6 mV (V_{CS-FWD}), indicating positive inductor current. To exit bypass mode the either the OVP status is cleared or $V_{SW-SENSE}$ is less than -150 mV ($V_{I-NEG-BYP}$). Current flow from V_{LOAD} to V_{SUPPLY} can occur in bypass mode while operating in FPWM. Once the high-side FET is disabled, the device enters active mode. The proper conditions must be achieved to enter bypass mode again. See 表 7-2 for details on how the device enters and exits bypass mode.

表 7-2. Bypass Mode: FPWM

	Conditions (1)
Enter bypass mode	$V_{VOUT} > V_{TRK} * K_{FB} * V_{OVTH\_RISING}$ AND $V_{CSP-CSN} > V_{CS-FWD}$

表 7-2. Bypass Mode: FPWM (continued)

	Conditions (1)
Exit bypass mode	$V_{VOUT} < V_{TRK} * K_{FB} * V_{OVTH\_FALLING}$ OR $V_{SW-SENSE} < V_{I-NEG-BYP}$

(1) K_{FB} is either 20 or 60 depending on the selected output voltage range. See section セクション 7.3.7

7.4.2 Light Load Switching Mode

The device provides two light load switching modes. Inductor current waveforms in each mode are different at the light/no load condition.

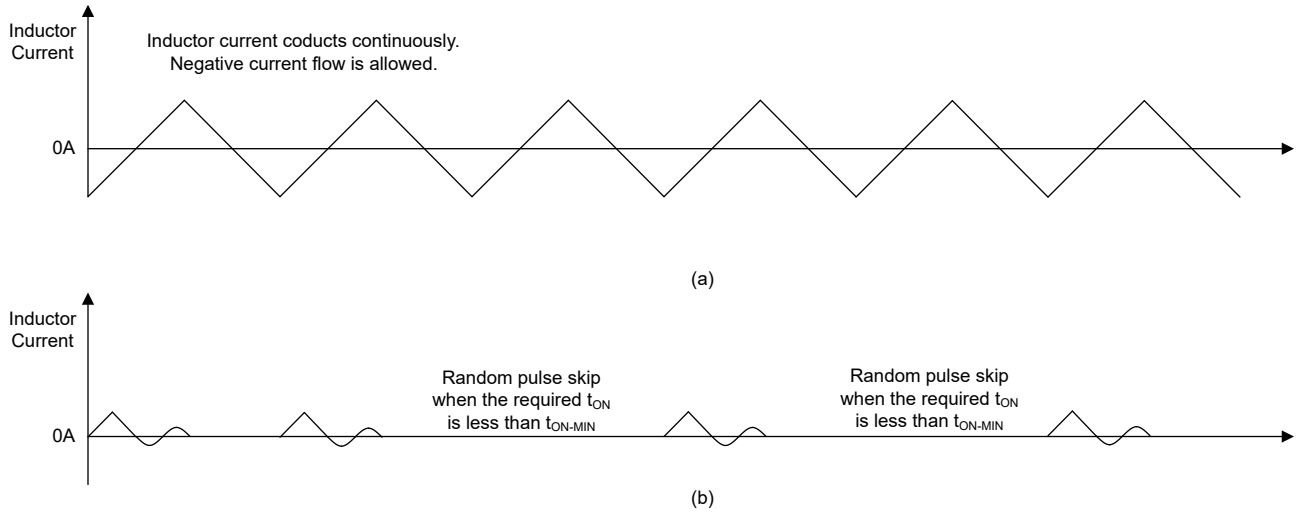


図 7-21. Inductor Current Waveform at Light Load (a) FPWM (b) Diode Emulation

7.4.2.1 Forced PWM (FPWM) Mode

In FPWM mode, the inductor current conducts continuously at light or no load conditions, allowing a continuous conduction mode (CCM) operation. The benefits of the FPWM mode are a fast light load to heavy load transient response, and constant switching frequency at light or no load conditions. The maximum reverse current is limited to 150 mV/$R_{DS(ON)}$ in FPWM mode.

7.4.2.2 Diode Emulation (DE) Mode

In diode emulation (DE) mode, inductor current flow is allowed only in one direction - from the input source to the output load. The device monitors the SW-SENSE voltage during the high-side switch on-time and turns off the high-side switch for the remainder of the PWM cycle when the SW-SENSE voltage falls down below the 5-mV zero current detection (ZCD) threshold (V_{ZCD}). The benefit of the diode emulation is a higher efficiency than FPWM mode efficiency at light load condition.

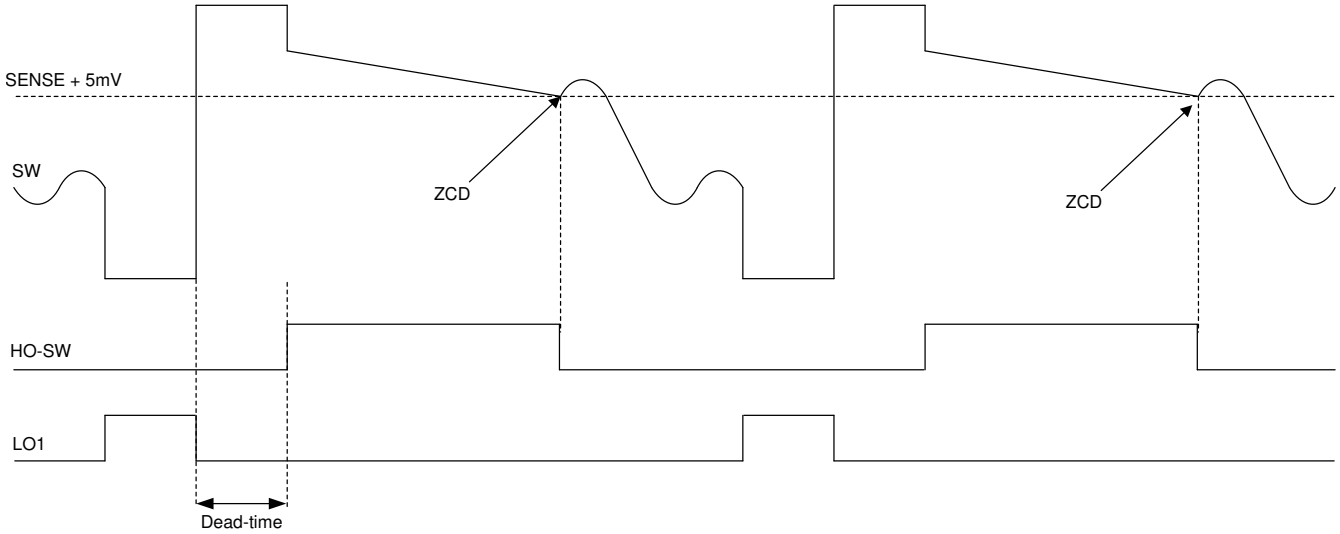


図 7-22. Zero Current Detection

7.4.2.3 Forced Diode Emulation Operation in FPWM Mode

During soft start, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin is greater than 1.5 V, the device shifts the zero current detection (ZCD) threshold down to -145 mV. The peak-to-peak inductor current must satisfy 式 14 for a proper FPWM operation at no load.

$$\frac{I_{PP} \times R_{DS(on)}}{2} < 145mV \tag{14}$$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device integrates several optional features to meet system design requirements, including input UVLO, programmable soft start, clock synchronization, spread spectrum, and selectable light load switching mode. Each application incorporates these features as needed for a more comprehensive design. Refer to the *LM5123EVM-BST* user's guide for more information.

8.2 Typical Application

図 8-1 shows the typical components to design a boost controller with a variable output voltage.

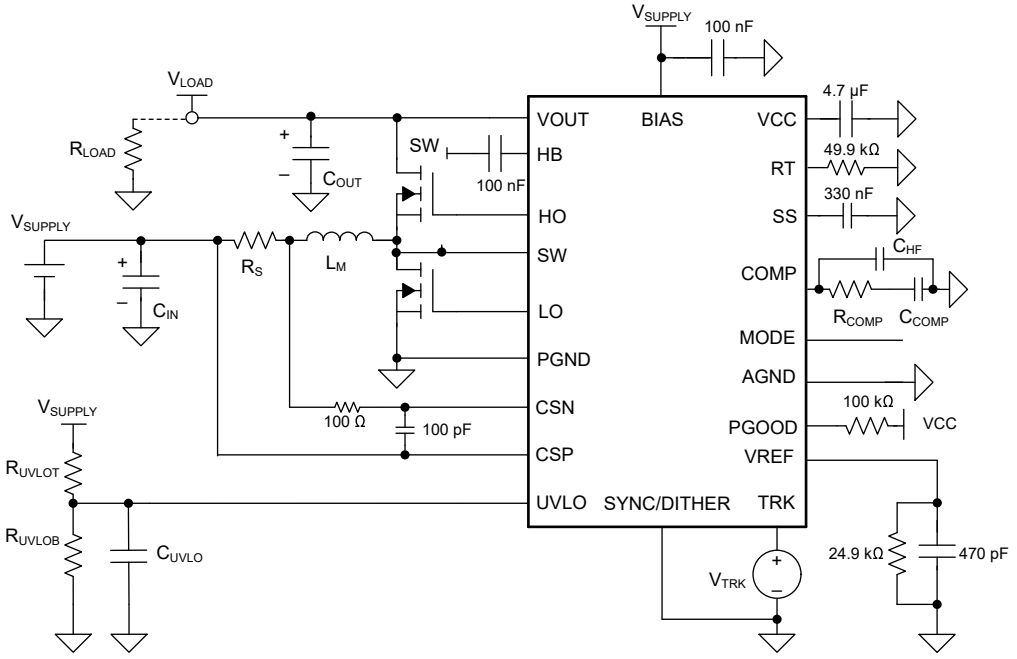


図 8-1. Typical Synchronous Boost Converter with Optional Components

'

表 8-1 provides the selected component values for the results found in セクション 8.2.4.

表 8-1. Component Selection

L_M	R_S	R_{COMP}	C_{COMP}	C_{HF}	C_{OUT}	C_{IN}
2.6 µH	1.5 mΩ	54.9 kΩ	6.8 nF	47 pF	450 µF	120 µF

8.2.1 Design Requirements

表 8-2 shows the intended input, output, and performance parameters for this application example. The design parameters reflect an application that requires a variable output voltage

表 8-2. Design Example Parameters

DESIGN PARAMETER	VALUE
Minimum input supply voltage ($V_{SUPPLY(MIN)}$)	9 V
Minimum output voltage (V_{LOAD_MAX})	24 V
Maximum output voltage (V_{LOAD_MAX})	45 V
Maximum output power (P_{OUT_MAX})	200 W
Typical switching frequency (f_{SW})	440 kHz

8.2.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application.

Refer to the *LM5123EVM-BST* EVM user guide for recommended components and typical application curves.

8.2.3 Application Ideas

For applications requiring the lowest cost with minimum conduction loss, inductor DC resistance (DCR) can be used to sense the inductor current rather than using a sense resistor. R_{DCRC} and C_{DCRC} must meet 式 15 to match a time constant.

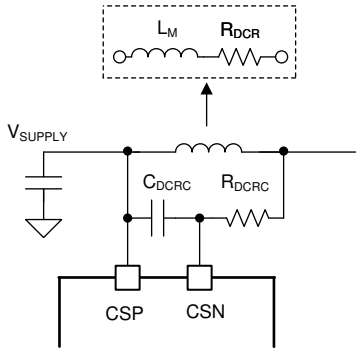


図 8-2. DCR Current Sensing

$$\frac{L_M}{R_{DCR}} = R_{DCRC} \times C_{DCRC} \tag{15}$$

If required, an additional PGOOD delay can be programmed using an external circuit.

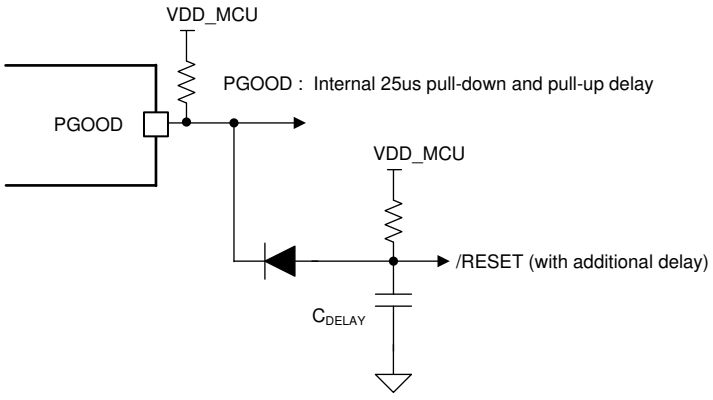


図 8-3. Additional PGOOD Delay

8.2.4 Application Curves

The data presented in this section were gathered using the*LM5123EVM-BST* evaluation module. The LM51231-Q1 replaced the LM5123-Q1 as the power supply controller.

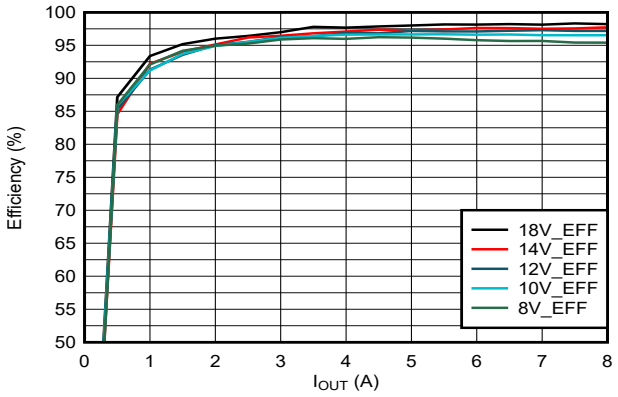


図 8-4. Efficiency vs. I_{OUT}, V_{OUT} = 24 V (FPWM)

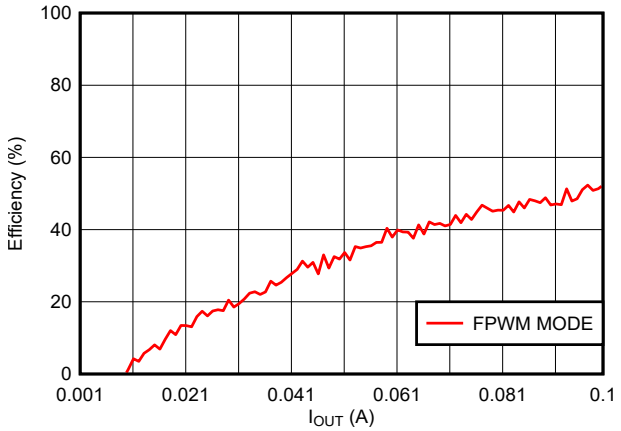


図 8-5. Efficiency vs. I_{OUT}, V_{OUT} = 24-V Light Load

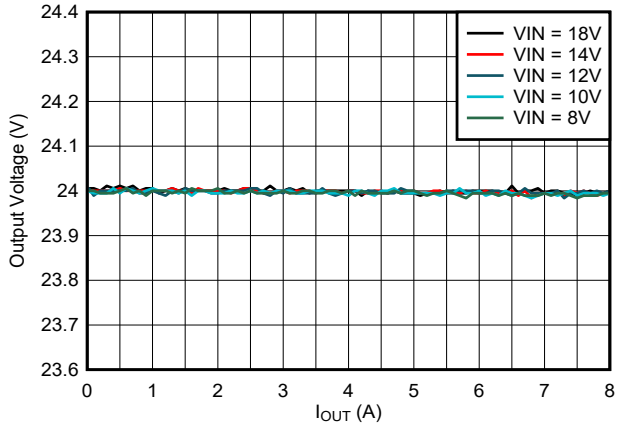


図 8-6. 24-V Load Regulation

8.3 System Example

Use the LM51231 in class-H audio applications. The TRK pin can be used to dynamically control the supply of the audio amplifier.

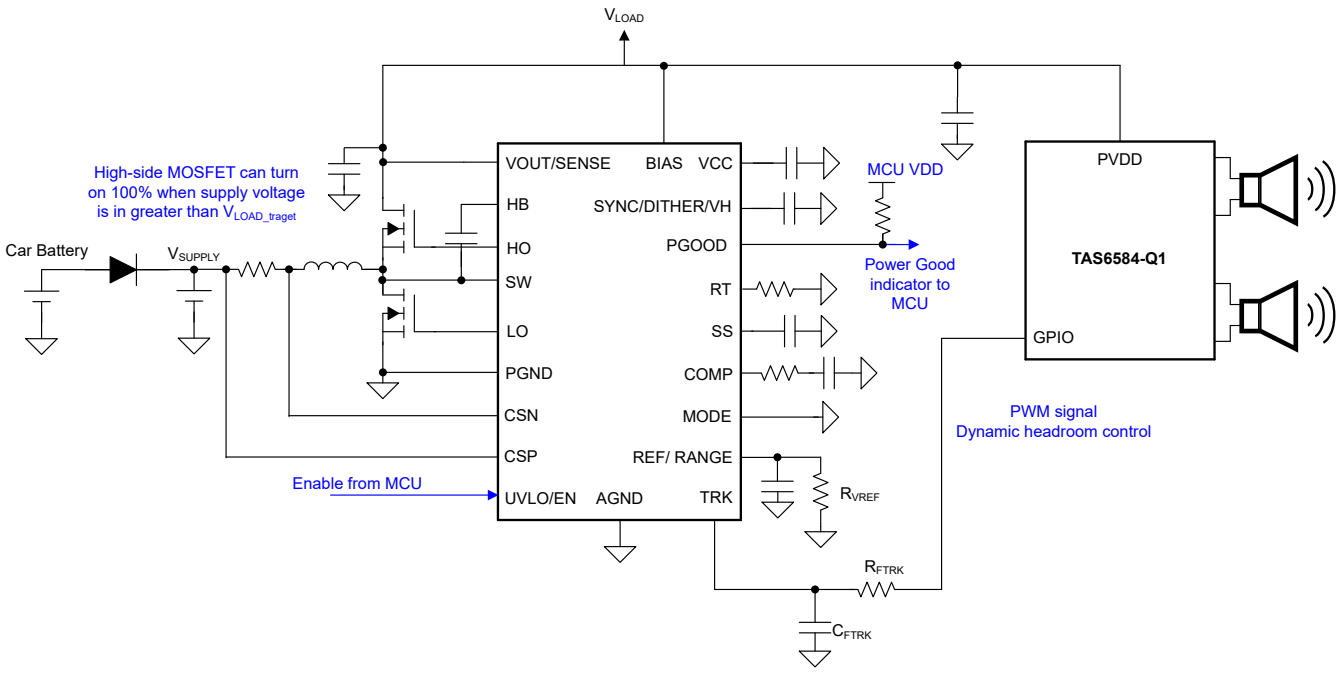


図 8-7. LM51231 in class-H audio application

Use LM51231 in LED application. The TRK pin can be used to control head-room.

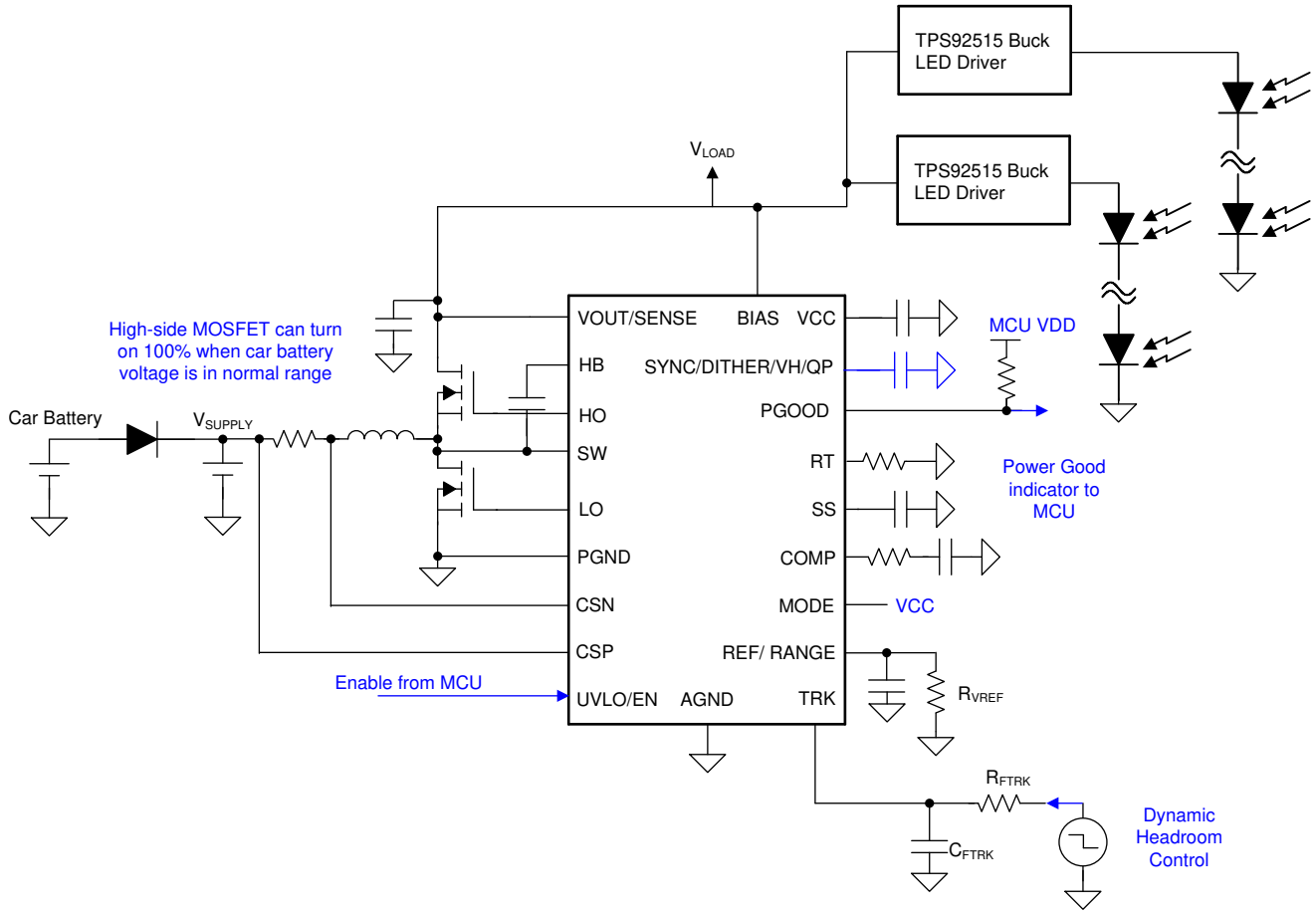


図 8-8. LM51231 in LED application

To configure non-synchronous boost controller, connect SW to PGND, and connect HB to VCC.

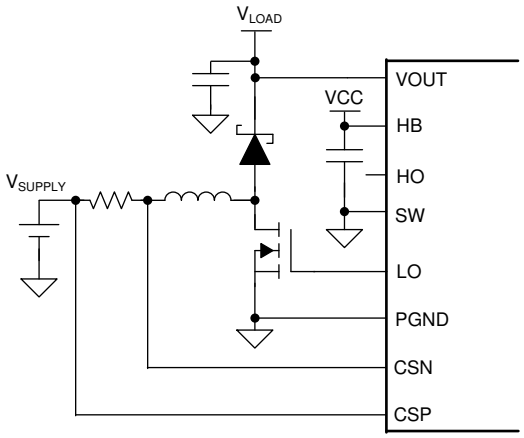


図 8-9. Non-synchronous boost configuration

8.4 Power Supply Recommendations

The device is designed to operate from a power supply or a battery whose voltage range is from 0.8 V to 42 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 0.8 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors can be required at the supply input of the converter.

8.5 Layout

8.5.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Place C_{VCC}, C_{BIAS}, C_{HB}, and C_{VOUT} as close to the device. Make direct connections to the pins.
- Place Q_H, Q_L, and C_{OUT}. Make the switching loop (C_{OUT} to Q_H to Q_L to C_{OUT}) as small as possible. A small size ceramic capacitor helps to minimize the loop length. Leave a copper area near the drain connection of Q_H for a thermal dissipation.
- Place L_M, R_S, and C_{IN}. Make the loop (C_{IN} to R_S to L_M to C_{IN}) as small as possible. A small size ceramic capacitor helps to minimize the loop length.
- Connect R_S to CSP-CSN. The CSP-CSN traces must be routed in parallel and surrounded by ground.
- Connect VOUT, HO, and SW. These traces must be routed in parallel using a short, low inductance path. VOUT must be directly connected the drain connection of Q_H. SW must be directly connected to the source connection of Q_H
- Connect LO and PGND. The LO-PGND traces must be routed in parallel using a short, low inductance path. PGND must be directly connected the source connection of Q_L
- Place R_{COMP}, C_{COMP}, C_{SS}, C_{VREF}, R_{VREFT}, R_{VREFB}, R_T, and R_{UVLOB} as close to the device, and connect to a common analog ground plane.
- Connect power ground plane (the source connection of the Q_L) to EP through PGND. Connect the common analog ground plane to EP through AGND. PGND and AGND must be connected underneath the device.
- Add several vias under EP to help conduct heat away from the device. Connect the vias to a large analog ground plane on the bottom layer.
- Do not connect C_{OUT} and C_{IN} grounds underneath the device and through the large analog ground plane which is connected to EP.

8.5.2 Layout Example

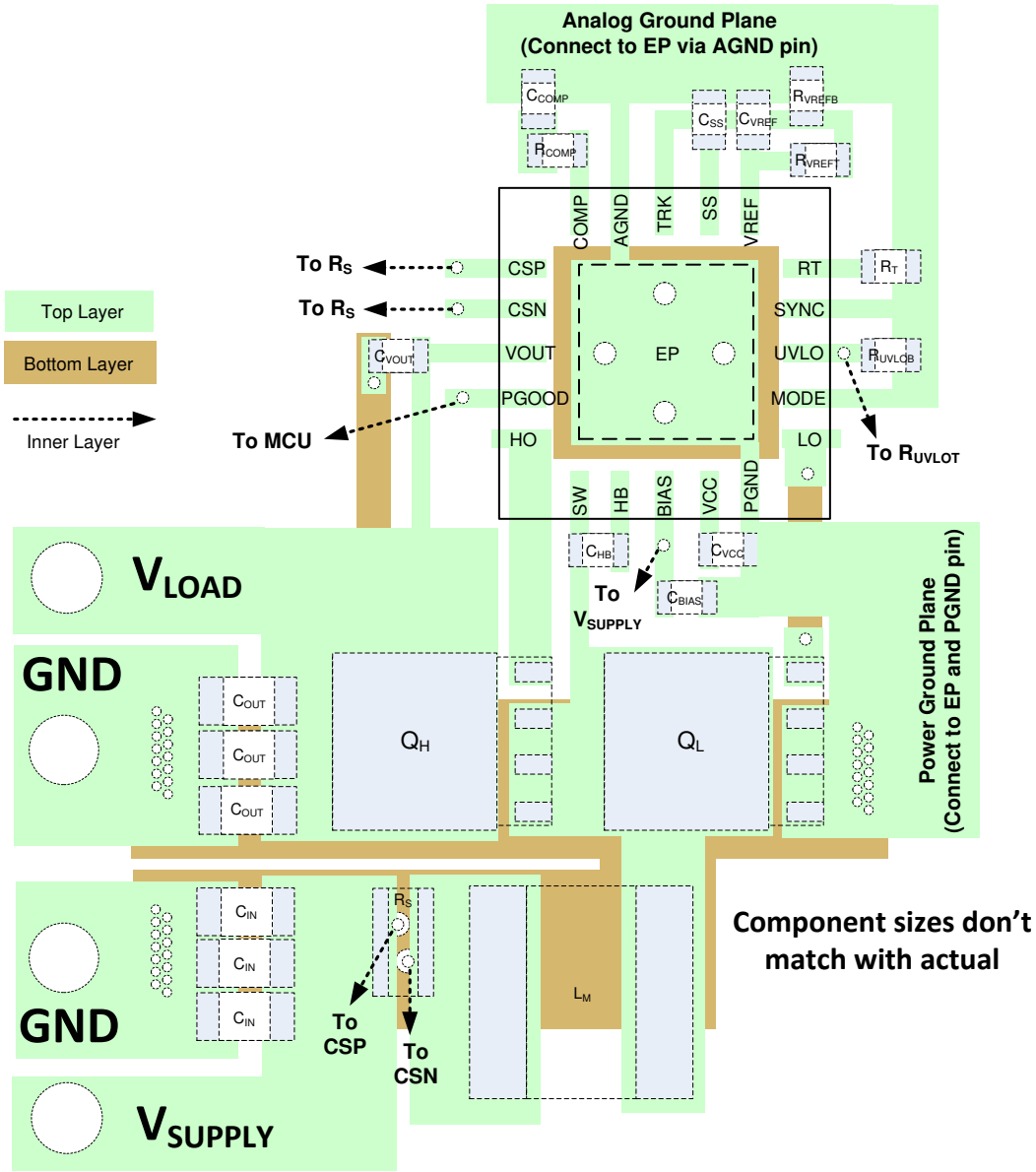


図 8-10. PCB Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM51231QRGRRQ1	ACTIVE	VQFN	RGR	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2W3L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

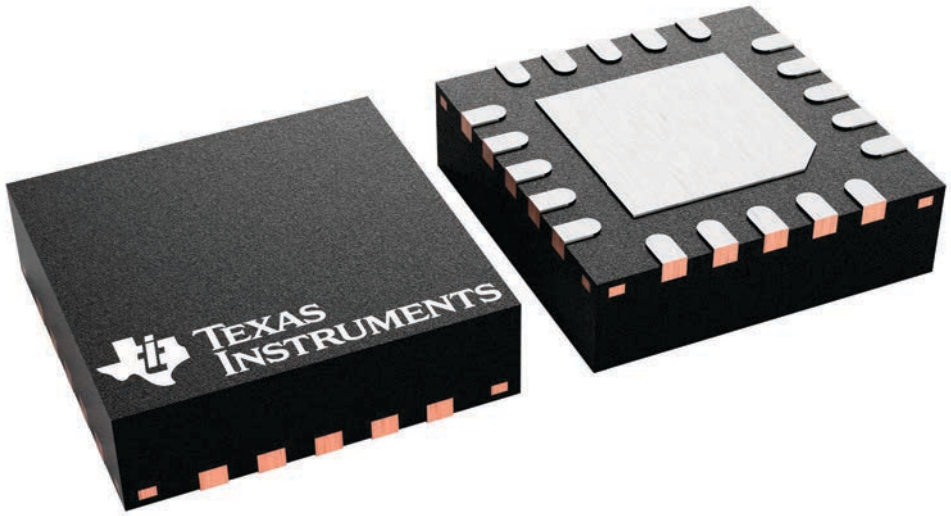
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



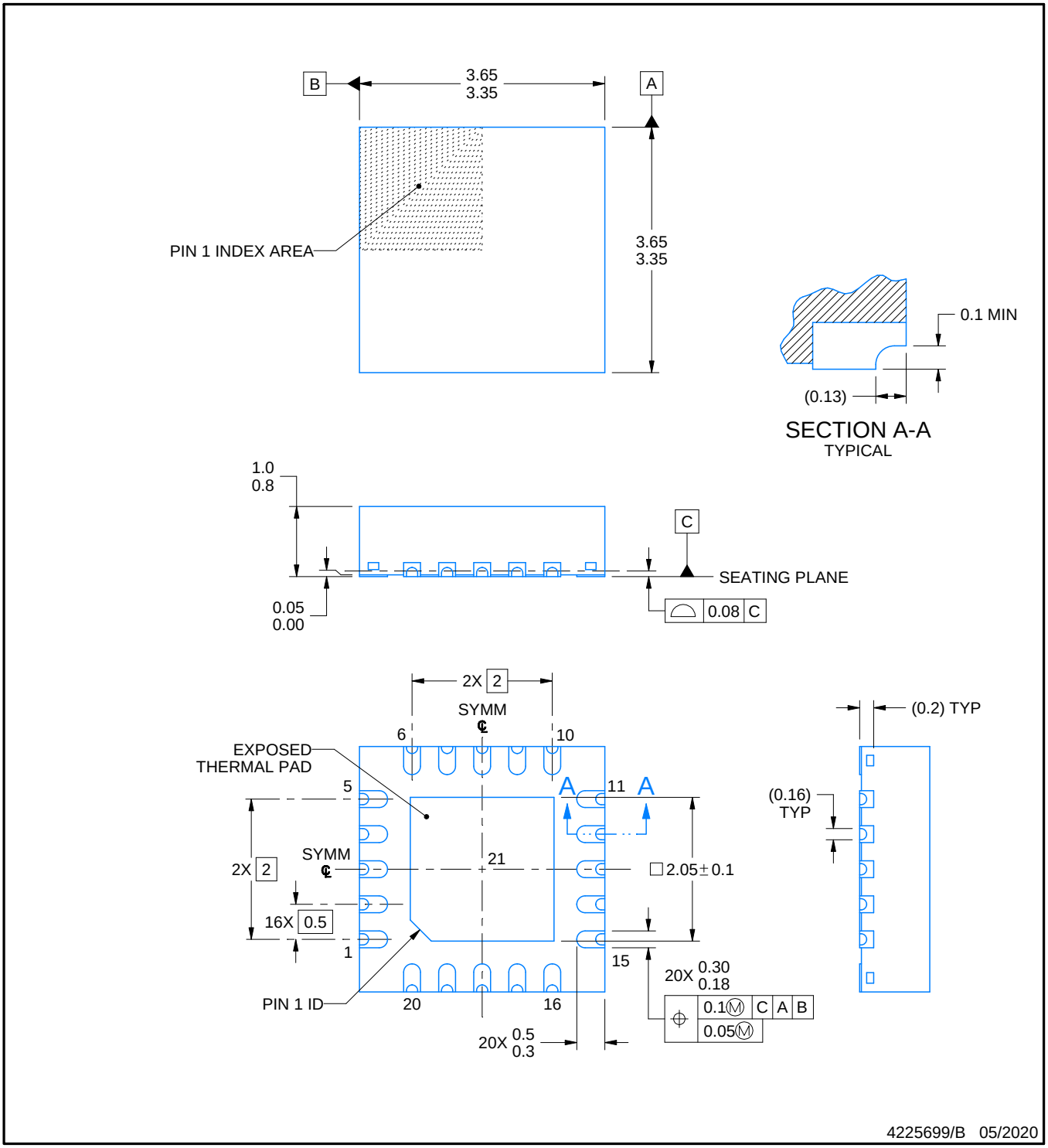
4228482/A

PACKAGE OUTLINE

RGR0020C

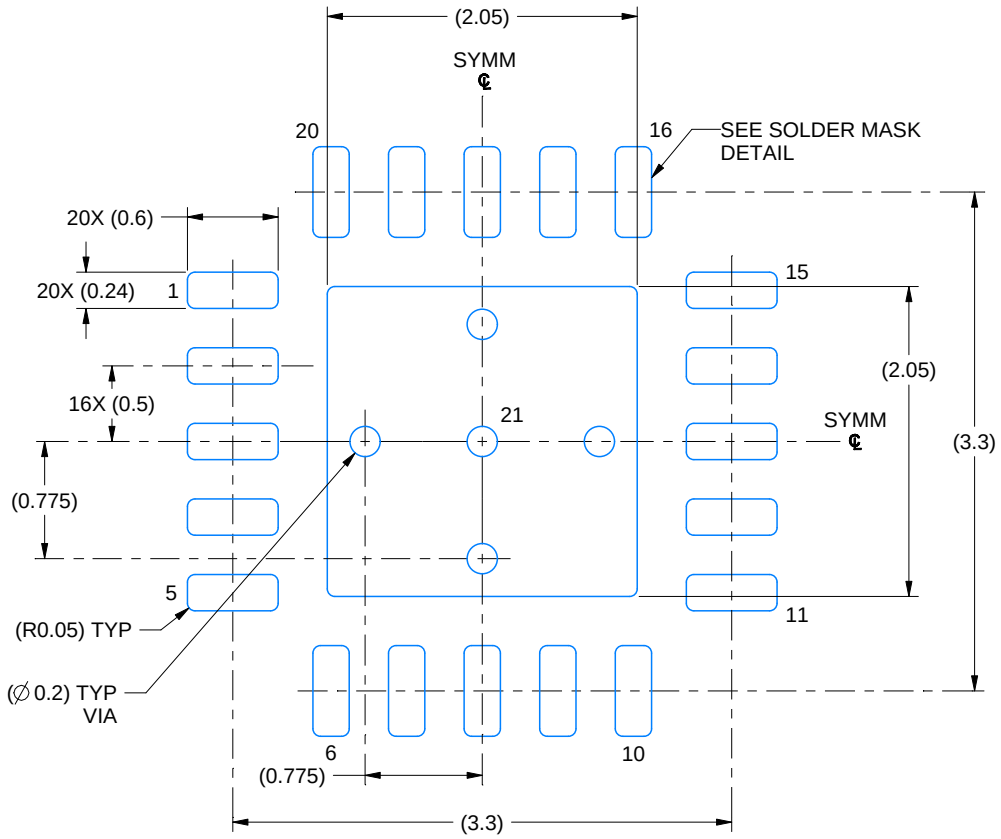
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

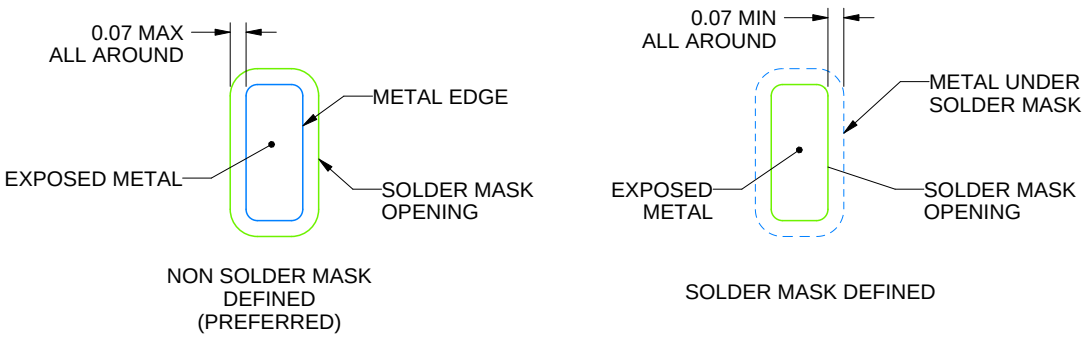


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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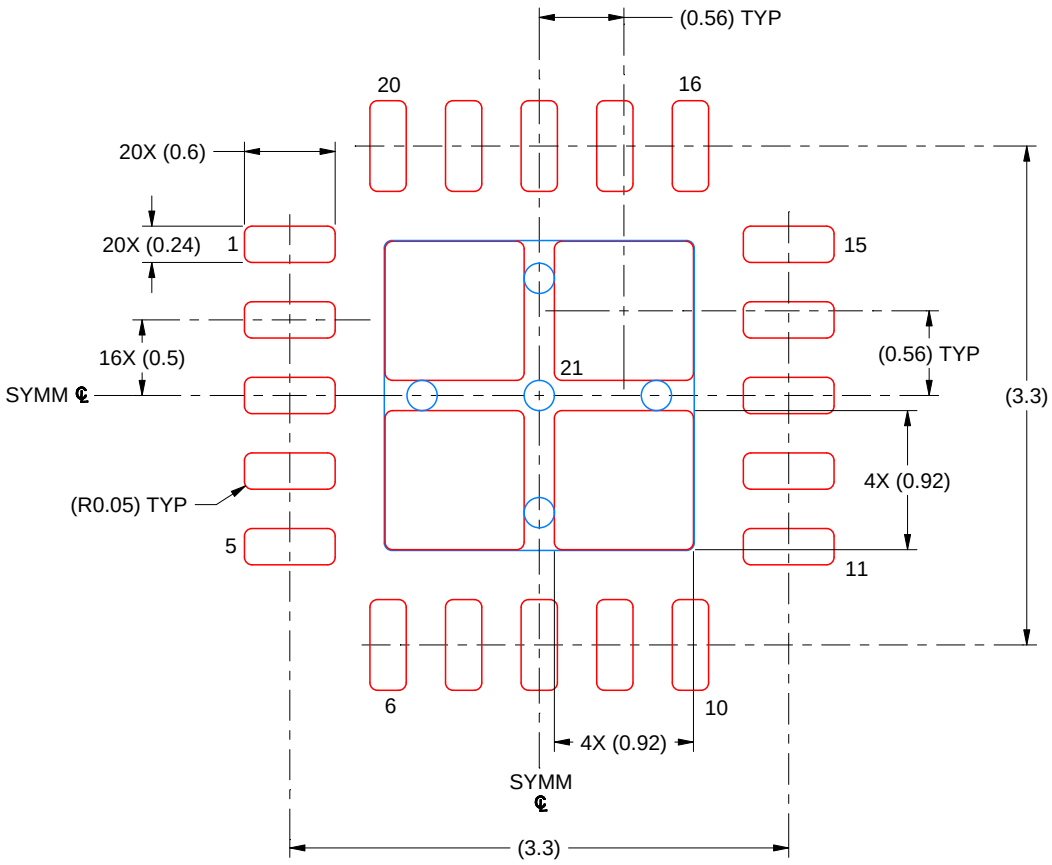
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225699/B 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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