TEXAS INSTRUMENTS
LM51772
JAJSRI9A – OCTOBER 2023 – REVISED MARCH 2024

LM51772 I²C インターフェイス搭載 55V 4 スイッチ昇降圧コントローラ

1 特長

- 入力範囲:3.5V～55V
- 出力電圧:3.3V～55V
- I²C を介した 3.3V からの動的 V_O プログラミング
  - 最大 48V (20mV 単調刻み)
  - 最大 24V (10mV 単調刻み)
- ピーク電流レギュレーション方式
- すべての動作モードで小さい電圧遷移リップル
- 動的な出力電圧トラッキング (デジタル PWM トラッキング入力、アナログ トラッキング入力)
  - I²C インターフェイスによるプログラミング経由
- シャットダウン時静止電流:3μA
- 動作時静止電流:60μA
- DRV ピンによる外部 FET 制御
- 軽負荷および高負荷条件で高効率を実現する動作モードの選択:
  - パワー セーブ モード (バースト / μSleep)
  - 自動 / プログラマブル導通モード
- 高電圧 LDO を内蔵
- 補助高電圧 LDO/リファレンス
- フルブリッジ ゲートドライブを内蔵
  - 2A ピーク電流能力
  - ブートストラップ過電圧および低電圧保護
  - ブートストラップ ダイオードを内蔵
- 動作モードから独立した固定周波数 (昇圧、昇降圧、降圧)
  - 強制 PWM モードを選択可能
  - スイッチング周波数:100kHz～2.2MHz
  - 外部クロック同期およびクロック出力
- スペクトラム拡散動作を選択可能
- ハイサイド出力電流センサ
  - 1A～7A の範囲で 50mA 刻みにプログラム可能
  - ISET ピンを選択可能
- I²C インターフェイスの読み出し値 (デバイス構成、強化された監視機能、プログラム可能な熱警告)
- WEBENCH® Power Designer により、LM51772 を使用するカスタム設計を作成

2 アプリケーション

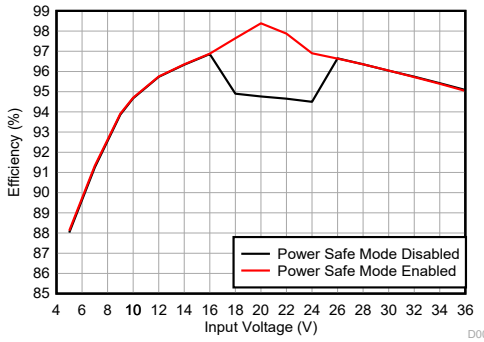
- USB Type-C パワー・デリバリ (ドッキング・ステーション、PC モニタ、デスクトップ PC)
- ワイヤレス充電
- 産業用 PC / 高耐久性 PC
- バッテリ・バックアップ・ユニット
- 商用 DC/DC
- 航空 / 海洋ソナー
- オフハイウェイ車両

3 概要

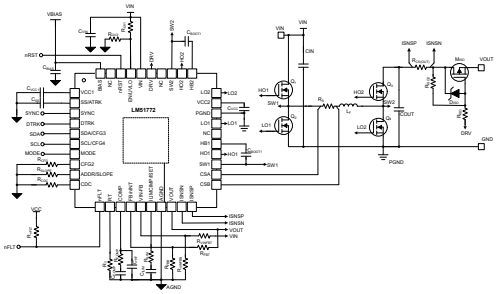
LM51772 は、4 スイッチ昇降圧コントローラです。入力電圧が、調整された出力電圧よりも高い、等しい、または低い場合に、レギュレートされた出力電圧を供給します。パワーセーブ モードでは、出力の動作範囲全体にわたって非常に高い効率をサポートします。LM51772 は固定スイッチング周波数で動作し、RT または SYNC ピンを経由して設定できます。強制 PWM で降圧、昇圧、昇降圧動作中、スイッチング周波数は一定に維持されます。外部補償ピンにより、さまざまなアプリケーションで非常に高速な過渡応答が可能です。(続き)

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LM51772RHAR	RHA040	6mm × 6mm



効率と入力電圧との関係、V_O = 20V、I_O = 5A



代表的なアプリケーション回路図

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4 概要 (続き)

このデバイスは、すべての動作モードにわたって小さなモード遷移リップルを維持します。出力電圧とデバイス構成は、内蔵の I^2C インターフェイスにより動的にプログラム可能です。内蔵およびオプションのハイサイド電流センサには、高精度の出力電流制限機能があります。LM51772 の定電流制限も、I2C インターフェイスにより構成可能です。

5 Pin Configuration and Functions

RHA Package
40-Pin QFN
Top View

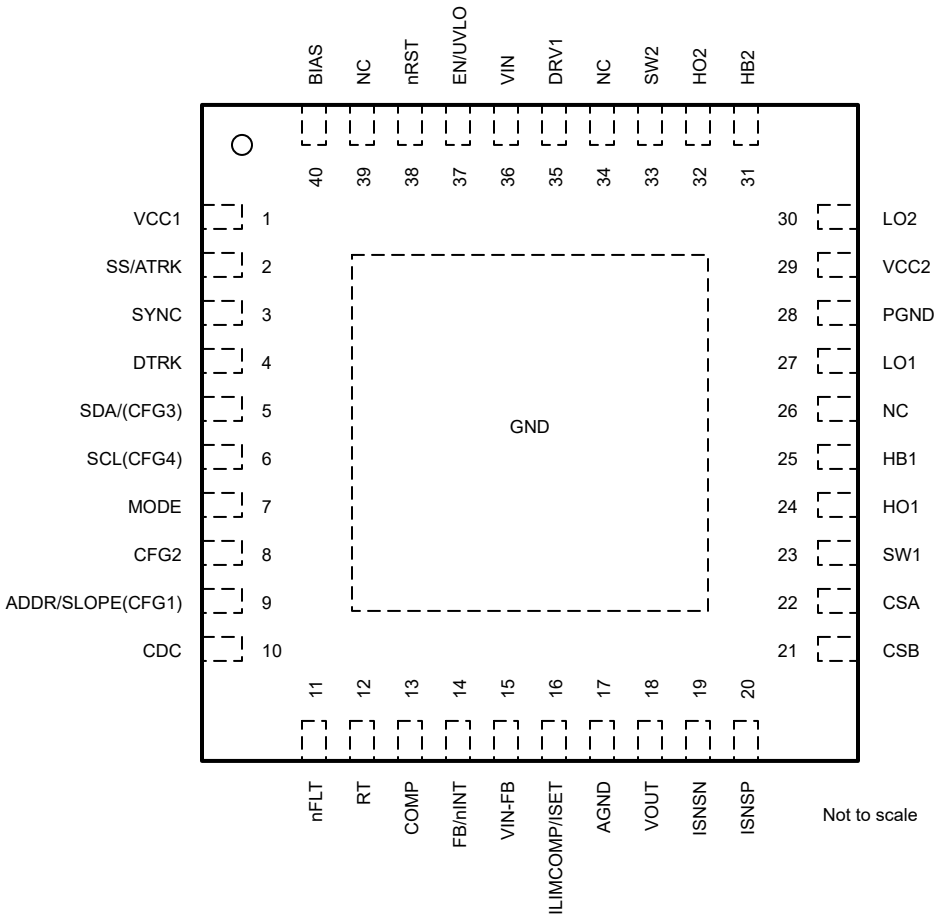

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表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VCC1	1	O	Auxiliary 5V regulator output. Place a capacitor close to the pin for good decoupling. If the output is disabled by the logic it can be tied to GND with a resistor or pulled to VCC2. Do not leave the pin floating.
SS/ATRK	2	I/O	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time. Analog output voltage tracking pin. The VOUT regulation target can be programmed by connecting the pin to variable voltage reference (for example, through a digital to analog converter). The internal circuit selects the lowest voltage applied to the pin.
SYNC	3	I	Synchronization clock input/output. The internal oscillator can be synchronized to an external clock during operation. If the output or input current sense amplifier is configured as a current limiter, pulling this pin is low during start-up, device switches the current limit direction to a negative polarity. *Do not leave this pin floating*. If this function is not used, connect the pin to VCC. The SYNC pin can be configured as internal clock synchronization output signal. The clock phase can be selected to 0° and 180° to directly operate two devices in a parallel (dual phase) operation.
DTRK	4	I	Digital PWM input pin for the dynamical output voltage tracking. *Do not leave this pin floating.* If this function is not used, connect the pin to VCC or GND.
SDA/CFG3	5	I/O	I^2C interface serial data line. Connect an external a pull-up resistor If I2C is disabled. this pin is a further configuration pin. Connect a resistor between the CFG3-pin and AGND to select the device operation according セクション 8.3.20
SCL/CFG4	6	I	I^2C interface serial clock line. Connect an external a pull-up resistor If I2C is disabled. this pin is a further configuration pin. Connect a resistor between the CFG4-pin and AGND to select the device operation according セクション 8.3.20
MODE	7	I	Digital input to select device operation mode. If the pin is pulled low, power save mode (PSM) is enabled. If the pin is pulled high, the forced PWM or CCM operation is enabled. The configuration can be changed dynamically during operation. *Do not leave this pin floating*.
CFG2	8	I/O	Device configuration pin. Connect a resistor between the CFG2 pin and GND to select the device operation according the セクション 8.3.20
ADDR/ SLOPE(CFG1)	9	I	Slope Compensation and Address selection. This pin also disables the I2C interface to use the SCL, SCA as additional slope configuration pins. Connect a resistor between the CFG1 pin and AGND to select the device operation according セクション 8.3.20
CDC	10		Cable drop compensation or current monitor output pin. Connect a resistor between the CFG pin and AGND to select the gain for the cable drop compensation. Per default this pin provides a current monitoring signal of the sensed voltage between the ISNSP and ISNSN pins In case the current monitor is disabled connect CDC to ground
nFLT/nINT	11	O	Open-drain output pin for fault indication or power good. This pin can be configured as interrupt pin. In case of a STATUS register change the pin toggles low for 256µs.
RT	12	I/O	Switching frequency programming pin. An external resistor is connected to the RT pin and AGND to set the switching frequency
COMP	13	O	Output of the error amplifier. An external RC network needs to beconnected between COMP and AGND to stabilize/compensate the regulator voltage loop.
FB/SEL_intFB	14	I	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin. Connect the FB pin to VCC2 to operate at a fixed output voltage default setting of the device. To select the internal feedback connect the pin to VCC2 before the device start-up

表 5-1. Pin Functions (続き)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VIN-FB	15		VIN sense pin. Connect to a VIN divider with the same gain as the VOUT divider for using PCM with external divider. If the internal Vout divider or if PCM is not used, connect to AGND. Do not leave floating.
ILIMCOMP/ISET	16		Compensation pin for average current limit loop. Connect an capacitor or a type 2 R-C network if the current limit is set by the internal DAC. If the internal DAC is disabled the pin sets the current limit threshold for the average current limit. Connect a resistor to AGND. A parallel filter of capacitor is recommended depending on the application requirements Connect a resistor to AGND if the current limit is set by ISET. Connect the ISET pin to VCC2 to disable the block and reduce the quiescent current
AGND	17	G	Analog Ground
VOUT	18	I	Output voltage sense input. Connect to the power stage output rail.
ISNSN	19	I	Negative sense input of the output or input average current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be located either on the input side or on the output side of the power stage. In case the optional current sensor is disabled connect ISNSN and ISNSP together to AGND
ISNSP	20	I	Positive sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be placed either on the input side or on the output side of the power stage. In case the optional current sensor is disabled connect ISNSP to ground
CSB	21	I	Inductor peak current sense negative input. Connect CSB to the negative side of the external current sense resistor using a Kelvin connection.
CSA	22	I	Inductor peak current sensor positive input. Connect CSA to the positive side of the external current sense resistor using a Kelvin connection.
SW1	23	P	Inductor switch node for the buck half-bridge
HO1	24	O	High-side gate driver output for the buck half-bridge
HB1	25	P	Bootstrap supply pin for buck half-bridge. An external capacitor is required between the HB1 pin and the SW1 pin, to provide bias to the high-side MOSFET gate driver. Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling
NC	26	O	Not Connected
LO1	27	O	Low-side gate driver output for the buck half-bridge
PGND	28	G	Power Ground
VCC2	29	O	Internal linear bias regulator output. Connect a ceramic decoupling capacitor from VCC to PGND. This rail supplies the internal logic and the gate driver. Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling.
LO2	30	O	Low-side gate driver output for the boost half-bridge
HB2	31	P	Bootstrap supply pin for boost half-bridge. An external capacitor is required between the HB2 pin and the SW2 pin, to provide bias to the high-side MOSFET gate driver Place the external capacitor close to the pin without any resistance between the pin and capacitor for good decoupling
HO2	32	O	High-side gate driver output for the boost half-bridge
SW2	33	P	Inductor switch node for the buck half-bridge
NC	34	O	Not Connected
DRV1	35		External FET drive pin. This pin features a high-voltage push pull stage, a open drain output or a charge pump driver stage according to the selected configuration.

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表 5-1. Pin Functions (続き)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
VIN	36	I	The input supply and sense input of the device. Connect VIN to the supply voltage of the power stage.
EN/UVLO	37	I	Enable pin. Digital input pin to enable the converter switching. The input features a precise analog comparator and a hysteresis to monitor the input voltage. Connect a resistor divider from the input voltage to maintain the under voltage lookout(UVLO) feature.
nRST	38	I	Digital input pin to enable the device internal logic, interface operation and the VCC1 regulator if selected.
NC	39	O	Not Connected
BIAS	40		Optional input to the VCC2 bias regulator. Powering VCC2 from an external supply instead of VIN can reduce power loss at high V_{IN}.
GND	PAD	G	Thermal pad

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

注

Commercial Product Preview Samples (see 図 6-1)

1. By operating the device with input voltages above 36V the current limit circuit can get shortly turned off during the SW1 node rising up. This results in a unregulated peak current and oscillations of the peak current loop.
2. By operating the device with output voltages above 36V the device can turn of the high side switch and restart
3. By connecting the ILIMCOMP/ISET pin to VVC2 to disable the function, the device operation gets unstable due to internal coupling. To disable the ILIM function the following cases are recommended:
   - disabled the current sensor fully. Pull ILIMCOMP to 4V by dividing VCC2 with 10kΩ and 40kΩ
   - IMON enabled (e.g. for CDC) but ILIM disabled. Pull ILIMCOMP/ISET to GND, do not leave the pin floating

The limitations above are removed for the prototype material. (see 図 6-2)

図 6-1. Top Marking Experimental Samples

図 6-2. Top Marking Prototype Samples

注

Please refer to the document revision for the summery of the changed to this document and device description

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6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise specified)(1)

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	59	V
	VIN, ISNSP, ISNSN to AGND	–0.3	59	
	EN/UVLO, nRST	–0.3	59 (4)	
			$V_{(VIN)}$ + 5 (4)	
	ATRK/SS, DTRK, RT, SYNC, MODE, SDA, SCL, ADDR/SLOPE, CFG2, to AGND	–0.3	5.8	
	FB, VIN-FB to AGND	–0.3	5.8	
	CSA, CSB to SW1	–0.3	0.3	
	SW1, SW2 to AGND(DC)	–0.5	59	
	SW1, SW2 to AGND (≤ 100ns duration)	–2	59	
	SW1, SW2 to AGND(≤ 10ns duration)	–3	59	
	SW1, SW2 to AGND(≤ 5ns duration)	–4	59	
	HB1 to SW1, CSA, CSB	–0.3	5.8	
	PGND to AGND	–0.3	0.3	
Output	VCC1, VCC2 to AGND	–0.3	5.5	V
	VOUT to AGND	–0.3	59	
	nFLT to AGND	–0.3	5.8	
	COMP, ILIMCOMP, CDC to AGND(2)	–0.3	5.8	
	LO1, LO2, to PGND	–0.3	$V_{(VCC2)}$+0.3	
	HB1 to SW1, HB2 to SW2	–0.3	5.5 (5)	
		–0.3	6	
	HO1 to SW1	–0.3	$V_{(HB1)}$+0.3	
	HO2 to SW2	–0.3	$V_{(HB2)}$+0.3	
	HO1, HO2, HB1, HB2 to AGND	–0.3	65	
Storage temperature, T_{STG}		–55	150	°C
Operating junction temperature, T_J (3)		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin has an internal max voltage clamp which can handle up to 1.6mA.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(4) Both of the stated conditios need to be observed
(5) Operating lifetime is de-rated for voltage bigger than the specified maximum

6.2 Handling Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input Voltage Sense	0	48	55	V
$V_{(BIAS)}$	Bias Input Voltage Supply	0		40	V
	Input/Bias start-up voltage	3.5			V
	Minumum voltage for PCM operatoin	6			V
$V_{(VOUT)}$	Output Voltage Sense	3.3		55	V
$V_{(ILIM)}$	ISNSP;ISNSN	2.8		55	V
$R_{(ISNS)}$	current limit sens resistor		10		mΩ
	current limit sens resistor tolerance	–1		1	%
$C_{(VCC2)}$	VCC regulator output capacitance	6			µF
$C_{(VCC1)}$	VCC regulator output capacitance	2			µF
V_{FB}	FB Input	0		$V_{(VCC)}$	V
V_{IL}	Logic pin low-level (MODE, DTRK, SYNC, SDA, SCL)			0.4	V
V_{IH}	Logic pin high-level (MODE, DTRK, SYNC, SDA, SCL)	1.3			V
F_{SW}	Typical Switching Frequency	100		2200	kHz
F_{SYNC}	Synchronization switching Frequency range	100		2200	kHz
T_J	Operating Junction Temperature(2)	–40		125	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see ElectricalCharacteristics.
(2) High junction temperatures degrade operating lifetimes.

6.4 Thermal Information

THERMAL METRIC(1)		LM51772 QFN 40 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	33.9	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	26.6	°C/W
R_{qJB}	Junction-to-board thermal resistance	15.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	15.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER				MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
	Shutdown current into VIN	$V_{(VIN)}$ = 48V, $V_{(BIAS)}$ = 0V $V_{(EN)}$ = 0V	T_J = 25°C		3.6		µA
	Shutdown current into BIAS	$V_{(VIN)}$ = 0V, $V_{(EN)}$ = 0V	T_J = 25°C		2.8		µA
	Quiescent current into BIAS	$V_{(EN)}$ = 3.3V, $V_{(FB)}$ > 1V, uSleep enabled, ILIMCOMP = $V_{(VCC2)}$, EN_VCC1 = 0b0	T_J = 25°C		25		µA
VCC1 REGULATOR							
	VCC1 regulation	V_I = 12.0V ,$I_{(VCC1)}$ = 1mA			5		V
	VCC1 drop-out voltage	$I_{(VCC1)}$ = 34mA;	V_I = 5V		0.6		V
			V_I = 4.5V		0.6		V
	VCC1 sourcing current limit	VCC1=GND	V_I = 12V		34		mA
VCC2 REGULATOR							
	VCC2 regulation	V_{BIAS} 12.0V ,$I_{(VCC2)}$ = 20mA			5		V
	VCC2 drop-out voltage	$I_{(VCC2)}$ = 45mA	V_I = 4V		130		mV
			V_I = 3.5V		190		mV
	VCC2 sourcing current limit	$V_{(VCC2)}$ ≥ 3V	V_I = 6V, V_{BIAS} = 12V		260		mA
$V_{T+(VCC2)}$	Positive going treshold	$V_{(VCC2)}$ rising			3.35		V
$V_{T-(VCC2)}$	Negative going treshold	$V_{(VCC2)}$ falling			3.05		V
$V_{T+(Force,BIAS)}$	Positive going treshold for Forced $V_{(BIAS)}$	FORCE_BIASPIN = 0b1			4.4		V
$V_{T+(VCC2,SUP)}$	Positive going treshold for LDO switch-over				6.5		V
	VCC2 UVLO rising detection delay time	$V_{(VCC2)}$ rising			100		µs
nRST							
$V_{T+(nRST)}$	Enable positive-going threshold	nRSTrising			1.4		V
$V_{T-(nRST)}$	Enable negative-going threshold	nRST falling			0.35		V
EN/UVLO							
$V_{T+(UVLO)}$	UVLO positive-going threshold	$V_{(EN/UVLO)}$ rising			1.25		V
$V_{T-(UVLO)}$	UVLO negative-going threshold	$V_{(EN/UVLO)}$ falling			1.2		V
$V_{hyst(UVLO)}$	UVLO threshold hysteresis	$V_{(EN/UVLO)}$ falling			50		mV
I_{UVLO}	UVLO hystereses sinking current	$V_{(EN/UVLO)}$ < 1.26V			5		µA
$t_{d(UVLO)}$	UVLO detection delay time	$V_{(EN/UVLO)}$ falling;			30		µs
SYNC							
$V_{T+(SYNC)}$	Sync input positive going threshold				1.19		V
$V_{T-(SYNC)}$	Sync input negative going threshold				0.41		V
	Sync activity detection frequency				99		kHz
$t_{d(Det,Sync)}$	Sync activity detection frequency threshold	refered to $f_{(SYNC)}$			3		cycles
	SYNC output drive streght	EN_SYNC_OUT = 0b1 $V_{(VCC2)}$ = 5V	sink		–38		mA
			source		52		mA
SOFT-START							
$I_{(SS)}$	Soft-start current				10		uA

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Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER					MIN	TYP	MAX	UNIT
	SS pull-down switch $R_{DS(on)}$		$V_{(SS)}$ = 1V			21		Ω
$t_{d(DISCH;SS)}$	SS Pin discharge time		Time from internal SS dischrage until the soft-start current can charge the pin again			500		µs
$t_{d(EN\_SS)}$	SS Pin charg delay time		Internal delay until soft-start current starts			4		µs
$V_{(SS,clamp)}$	Clamp Voltage for SS pin					4.1		V
VOUT TRACKING								
$V_{T+(DTRK)}$	DTRK positive-going threshold		$V_{(DTRK)}$ rising			1.19		V
$V_{T-(DTRK)}$	DTRK negative-going threshold		$V_{(DTRK)}$ falling			0.41		V
	DTRK activity dectection frequency	DTRK activity detection frequency				148		kHz
$t_{d(DTRK)}$	DTRK detection delay time					3		cycles
fc(LPF)	Corner freqeuncy of internal low pass					40		kHz
	$V_{(REF)}$voltage offset error	$V_{(REF)}$voltage offset error	$f_{(DTRK)}$ = 500kHz, duty = 50%				±10	mV
PULSE WIDTH MODULATION								
	Switching frequency		R_{RT} = 14kΩ, trimmed OSC			2200		kHz
	Switching frequency		R_{RT} = 15.4kΩ, trimmed OSC			2000		kHz
	Switching frequency		R_{RT} = 316kΩ, trimmed OSC			100		kHz
	Minimum controllable on-time		fPWM, R_{RT} = 14kΩ, positive inductor current	Boost Mode		59		ns
				Buck Mode		105		ns
	Minimum controllable off-time			Boost Mode		108		ns
				Buck Mode		108		ns
	RT regulation voltage					0.75		V
MODE SELECTION								
$V_{T+(MODE)}$	Mode input positive going threshold					1.19		V
$V_{T-(MODE)}$	Mode input negative going threshold					0.41		V
CURRENT SENSE								
	Positive peak current limit threshold					50		mV
	Negative peak current limit threshold					–50		mV
OUTPUT CURRENT LIMIT								
	Current sense amplifier transconductance		I2C interface disabled or DISABLE_ILIM_DAC = 0b1; $V_{(ISNSP)}$ > 3.3V; EN_NEG_CL_LIMIT = 0	25 mV ≤ $\Delta V_{(ISNS)}$ ≤ 50mV		1		mS
	Current sense amplifier output current		I2C interface disabled or DISABLE_ILIM_DAC = 0b1; $V_{(ISNSP)}$ > 3.V; EN_NEG_CL_LIMIT = 0	5 mV		5		µA
				25 mV		25		µA
				50 mV		50		µA

ADVANCE INFORMATION

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER					MIN	TYP	MAX	UNIT
	Offset voltage		V_{ISNS} > 4.8V	T_J= 25°C		0		mV
			V_{ISNS} > 4.8V	T_J=-40°C to 150°C		0		mV
	Current sense amplifier transconductance		I2C interface enabled and DISABLE_ILIM_DAC = 0b0 V_{ISNS} > 4.8V; N_NEG_CL_LIMIT = 0	$\Delta V_{(ISNS)}$ = 30mV and 50mV		500		µS
	Current limit		$R_{(ISNS)}$ = 10mΩ±1%; ILIM_THRESHOLD = 0x64			5		A
$\Delta V_{(ISNSx)}$	Current limit threshold voltage		ILIM_THRESHOLD = 0x14	EN_NEG_CL_LIMIT = 0, T_J=-40°C to 105°C; ISNSP/N ≥ 5V;		10		mV
	Current limit threshold voltage		ILIM_THRESHOLD = 0x3C			30		mV
	Current limit threshold voltage		ILIM_THRESHOLD = 0x64			50		mV
	Current limit threshold voltage step size		from 5mV to 68.5mV			0.5		mV
	Postive going threshold to disable ILIM		Referred to VCC2			64		%
	ISET regulation threshold voltage					1		V
ERROR AMPLIFIER								
V_{REF}	FB reference Voltage	FB reference				1		V
	FB pin leakage current		$V_{(FB)}$ = 1V			60		nA
	Transconductance					600		µS
	COMP sourcing current					150		uA
	COMP sinking current					150		uA
	COMP clamp voltage		$V_{(FB)}$ = 990mV			1.25		V
	COMP clamp voltage		$V_{(FB)}$ = 1.01V			0.240		V
$V_{T+(SEL,iFB)}$	postive going threshold to select internal FB operation		$V_{(FB)}$ rising			2.5		V
OVP								
VT+(OVP)	Over-voltage rising threshold		FB rising referece to V_{REF}			110		%
VT-(OVP)	Over-voltage falling threshold		FB falling referece to V_{REF}			105		%
VT+(OVP2)	Over-voltage rising threshold		$V_{(VOUT)}$ rising	V_OVP2 = 0b111111		55		V
	Over-voltage de-glitch time					10		µs
nFLT								
	nFLT pull-down switch R_{DSON}		1mA sinking			85		Ω
	Under-voltage positive going threshold		FB rising (referece to V_{REF})			95		%
	Under-voltage negative going threshold		FB falling (referece to V_{REF})			90		%
	nFLT off-state leakage		$V_{(nFLT)}$=12V			100		nA
	Deglitch filter					20		us
MOSFET DRIVER								
t_r	Rise time	HG1, HG2, LG1, LG2	C_G = 3.3nF			20		ns
t_f	Fall time	HG1, HG2, LG1, LG2	C_G = 3.3nF			15		ns

ADVANCE INFORMATION

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER					MIN	TYP	MAX	UNIT
	Gater driver high side on-resistance	LO1, LO2	$I_{(test)}$ = 500mA			1.12		Ω
	Gater driver high side on-resistance	HO1, HO2	$I_{(test)}$ = 500mA			1.16		Ω
	Gater driver low side on-resistance	LO1, LO2	$I_{(test)}$ = 500mA			0.5		Ω
	Gater driver low side on-resistance	HO1, HO2	$I_{(test)}$ = 500mA			0.51		Ω
THERMAL SHUTDOWN								
T_{T+J}	Thermal shutdown threshold	Thermal shutdown threshold	T_J rising			164		°C
	Thermal shutdown hysteresis	Thermal shutdown hysteresis				15		°C
THERMAL WARNING								
	Thermal warning threshold		T_J rising	THW_THRESHOLD=0b10		110		°C
	Thermal warning typ. programming range				95		140	°C
R2D INTERFACE								
	Internal reference resistor				31.77	33	34.23	kΩ

ADVANCE INFORMATION

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER					MIN	TYP	MAX	UNIT
R_{CFG}	External selection resistor resistance	R2D setting #0				0	0.1	kΩ
		R2D setting #1			0.49567	0.511	0.52633	kΩ
		R2D setting #2			1.1155	1.15	1.1845	kΩ
		R2D setting #3			1.8139	1.87	1.9261	kΩ
		R2D setting #4			2.6578	2.74	2.8222	kΩ
		R2D setting #5			3.7151	3.83	3.9449	kΩ
		R2D setting #6			4.9567	5.11	5.2633	kΩ
		R2D setting #7			6.2953	6.49	6.6847	kΩ
		R2D setting #8			8.0025	8.25	8.4975	kΩ
		R2D setting #9			10.185	10.5	10.815	kΩ
		R2D setting #10			12.901	13.3	13.699	kΩ
		R2D setting #11			15.714	16.2	16.686	kΩ
		R2D setting #12			19.885	20.5	21.115	kΩ
		R2D setting #13			24.153	24.9	25.647	kΩ
		R2D setting #14			29.197	30.1	31.003	kΩ
		R2D setting #15			35.405	36.5	37.595	kΩ
Protection/Monitoring								
	SCP Hiccup mode on time					1		ms
	SCP Hiccup mode off time					24		ms
CABLE DROP COMPENSATION								
	VOUT increase for cable droop compensation with external feedback	$R_{(FB,top)}$ = 100kΩ; CDC_GAIN=0b01		$V_{(CDC)}$ = 0.2V		0.1		V
				$V_{(CDC)}$ = 1V		0.5		V
	VOUT increase for cable droop compensation with internal feedback	CDC_GAIN=0b01		$V_{(CDC)}$ = 0.2V		0.1		V
				$V_{(CDC)}$ = 1V		0.5		V
$gm_{(CDC)}$	CDC current sense amplifier transconductance	$\Delta V_{(IMON)}$ = 50mV and 30mV		$V_{(ISNSP)}$ > 3.3V; EN_NEG_CL_LIMIT = 0		500		uS
	CDC current sense amplifier bandwith					1		MHz

ADVANCE INFORMATION

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12V

PARAMETER				MIN	TYP	MAX	UNIT
	Output current CDC	$\Delta V_{(IMON)}$ = 50mV; EN_NEG_CL_LIMIT = 0			25.0		µA
		$\Delta V_{(IMON)}$ = 25mV; EN_NEG_CL_LIMIT = 0			12.5		µA
		$\Delta V_{(IMON)}$ = 5mV; EN_NEG_CL_LIMIT = 0			2.5		µA
		$\Delta V_{(IMON)}$ = –5mV; EN_NEG_CL_LIMIT = 0			–2.5		µA
		$\Delta V_{(IMON)}$ = –25mV; EN_NEG_CL_LIMIT = 0			–12.5		µA
		$\Delta V_{(IMON)}$ = –50 mV; EN_NEG_CL_LIMIT = 0			–25.0		µA
DRIVE PIN							
	Pull down resistance	SEL_DRV_SUP = 0b00			1400		Ω
	Pull up resistance	SEL_DRV_SUP = 0b01 or SEL_DRV_SUP = 0b10,			1500		Ω
	Maximum output current	SEL_DRV_SUP = 0b00	sink		9		mA
	Maximum output current	SEL_DRV_SUP = 0b01 or SEL_DRV_SUP = 0b10,	source		9		mA
	Pull down resistance	SEL_DRV_SUP = 0b11			900		Ω
	Pull up resistance				1200		Ω
	Maximum output current		sink		9		mA
	Maximum output current		source		8		mA
	Charge pump switching frequency				100		kHz
OUTPUT DISCHARGE							
	Output discharge current	VO_DISCH = 0b00			25		mA
		VO_DISCH = 0b01			50		mA
		VO_DISCH = 0b10			75		mA
	Discharge done threshold				0.5		V
SPREAD SPECTRUM							
	Switching frequency modulation range upper limit				7.8		%
	Switching frequency modulation range lower limit				–7.8		%

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H	TBD			µs
I²C INTERFACE						
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus (1)	0		1000	

ADVANCE INFORMATION

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus (1)	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus (1)	0.5			
$t_{SU:STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{HD:DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus (1)	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus (1)			20	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20\times V_{DD}/5.5$		300	
		Fast mode plus (1)	$20\times V_{DD}/5.5$		120	
$t_{su:STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus (1)	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus (1)			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	pF
		Fast mode			400	

(1) Fast mode plus is supported but not fully compliant with I^2C standard

ADVANCE INFORMATION

6.7 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

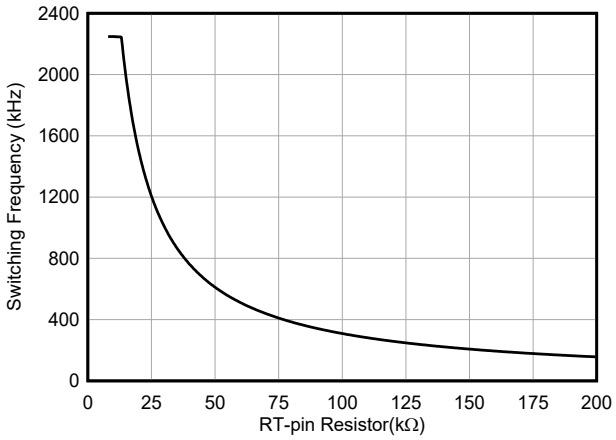

図 6-3. Switching Frequency Versus RT Resistance

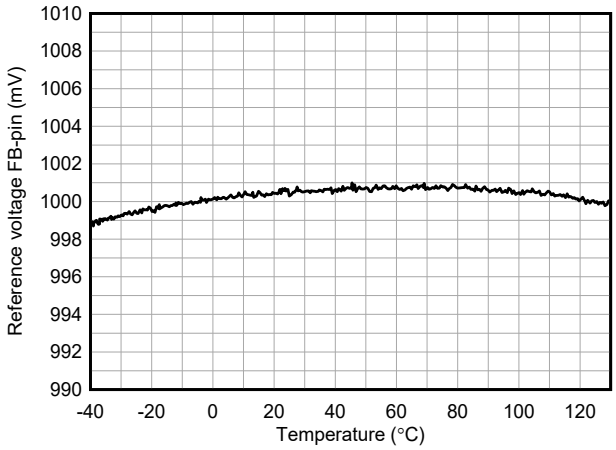

図 6-4. FB Pin Reference Voltage versus Temperature

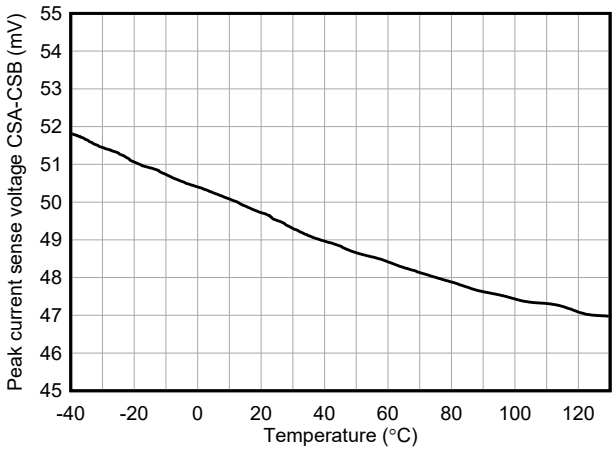

図 6-5. Current Limit Threshold Voltage Versus Temperature

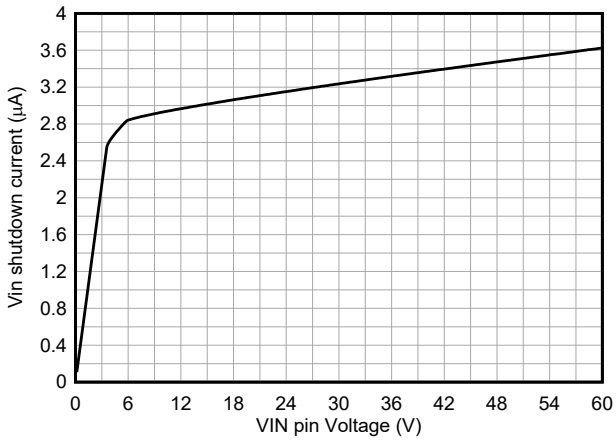

図 6-6. Shutdown Current into VIN versus Pin Voltage
$V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 12V, $V_{(BIAS)}$ = 0V

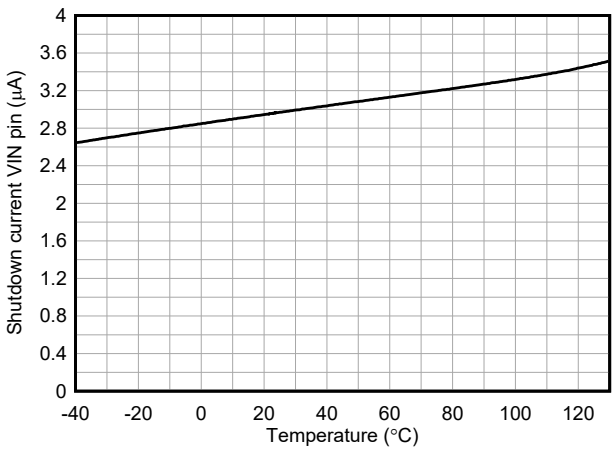

図 6-7. Shutdown Current into VIN versus Temperature
$V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 12V,$V_{(BIAS)}$ = 0V

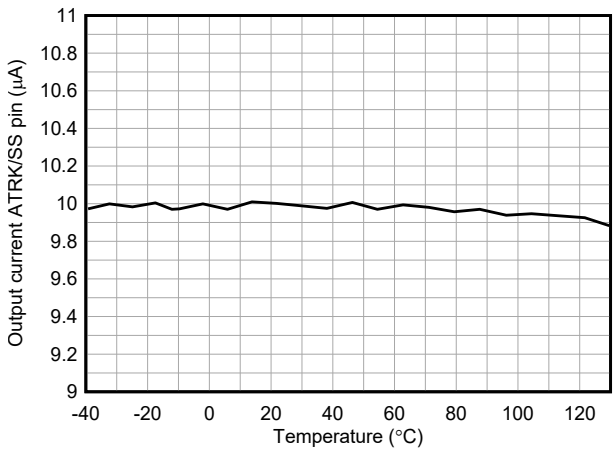

図 6-8. Soft-Start current versus Temperature

ADVANCE INFORMATION

6.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

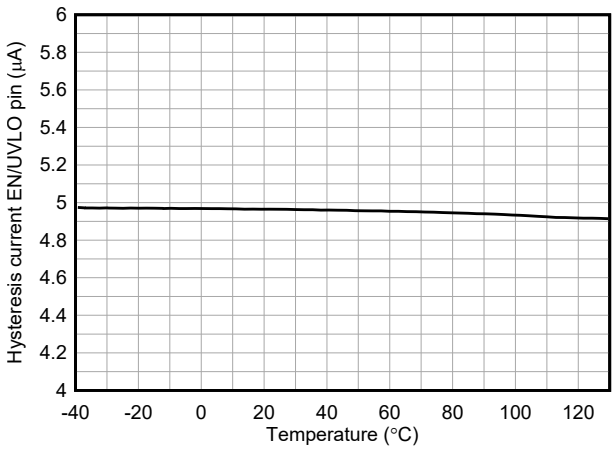

図 6-9. Hysteresis Current on EN/UVLO versus Temperature

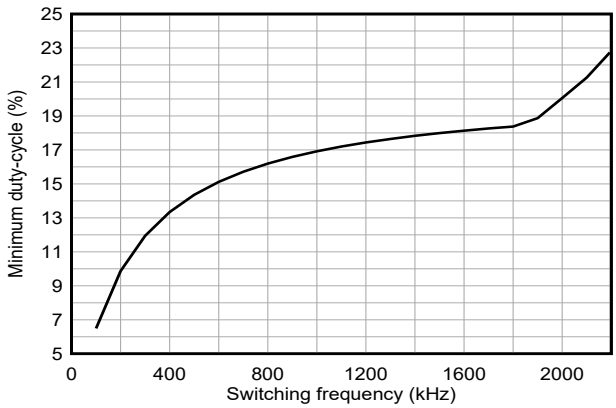

図 6-10. Buck Minimum Duty -cycle for PSM Operation versus Switching Frequency (SYNC_OUT = Enabled)

ADVANCE INFORMATION

7 Parameter Measurement Information

Gate Driver Rise Time and Fall Time

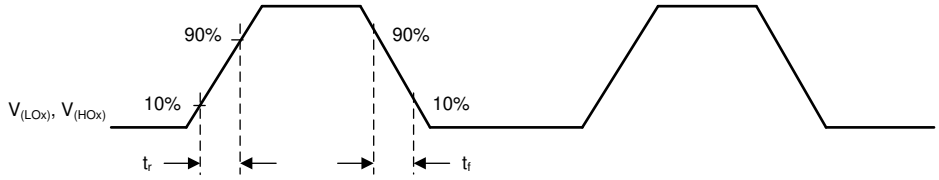

図 7-1. Timing Diagram Gate Driver t_r , t_f

Gate Driver Dead (Transition) - Time

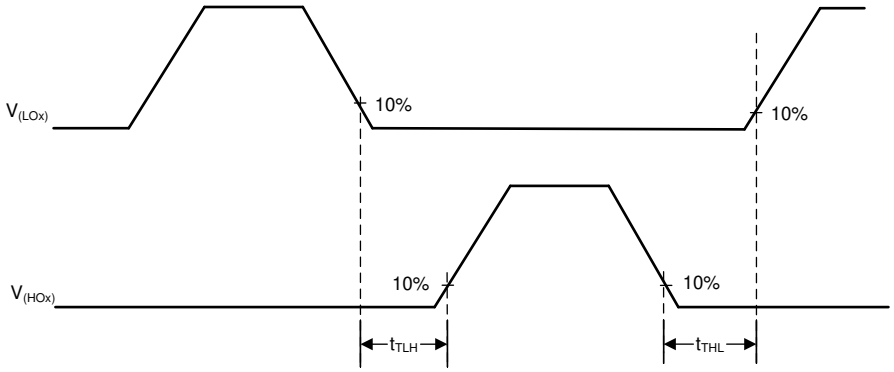

図 7-2. Timing Diagram Gate Driver t_t

8 Detailed Description

8.1 Overview

The LM51772 is a four switch Buck-Boost controller. It provides a regulated output voltage if the input voltage is higher, equal or lower as the adjusted output voltage. In power-save mode the device supports a high efficiency over the full range of the output load.

The LM51772 runs at a fixed switching frequency, which can be set via the RT and SYNC pin. The switching frequency remains constant during buck, boost and buck-boost operation. The device maintains small mode transition ripple over all operating modes.

The output voltage and device configurations can be dynamically programmed via the integrated I2C interface. The integrated and optional high side current sensor features an accurate and output current limitation. The average current limit of the LM51772 is also configurable through the I2C interface.

ADVANCE INFORMATION

ADVANCE INFORMATION

8.2 Functional Block Diagram

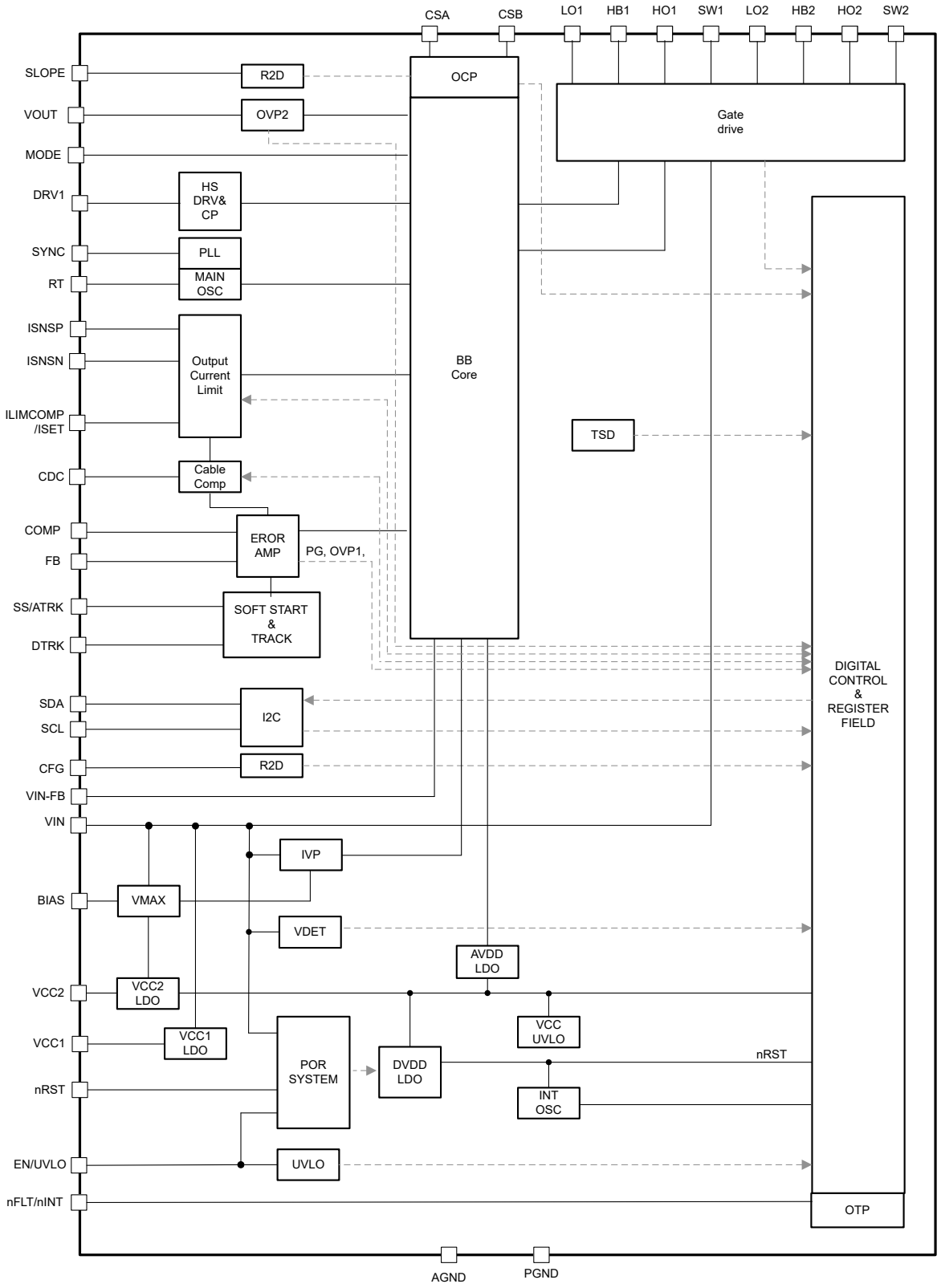

図 8-1. LM51772 Functional Block Diagram

8.3 Feature Description

8.3.1 Buck-Boost Control Scheme

The LM51772 buck-boost control algorithm ensure there is a seamless transition between the different operating modes, the fixed frequency operation, and the power stage protection features. The internal state machine controls the current flow using three active switching states:

State I: Transistors Q1 and Q3 are conducting. Q2 and Q4 are not conducting (boost mode magnetization state).

State II: Transistors Q1 and Q4 are conducting. Q2 and Q3 are not conducting (boost demagnetization or buck magnetization state).

State III: Transistors Q2 and Q4 are conducting. Q1 and Q3 are not conducting (buck demagnetization state).

Switch	State I	State II	State III
Q1	ON	ON	OFF
Q2	OFF	OFF	ON
Q3	ON	OFF	OFF
Q4	OFF	ON	ON

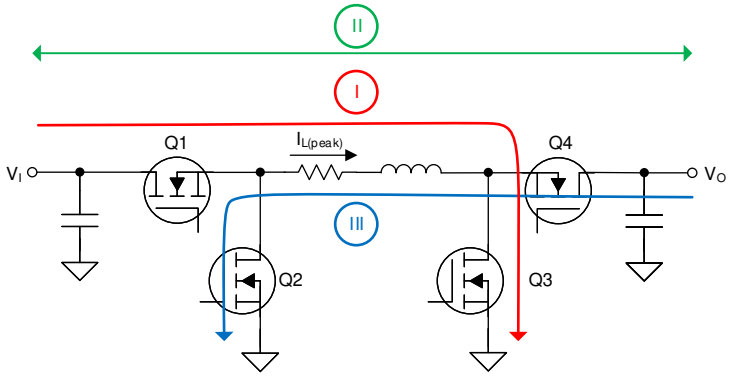

図 8-2. Buck-Boost Active Switching States

8.3.1.1 Buck Mode

In buck mode operation, the converter starts a buck magnetization cycle (state II) with the internal clock signal. When the inductor reaches its peak current, the converter proceeds to the buck demagnetization state III. With the next clock signal, the converter changes back to a buck magnetization cycle and starts a new switching cycle with sampling the peak current. As long as the duty cycle does not reach the minimum off-time, the current control remains in buck operating mode.

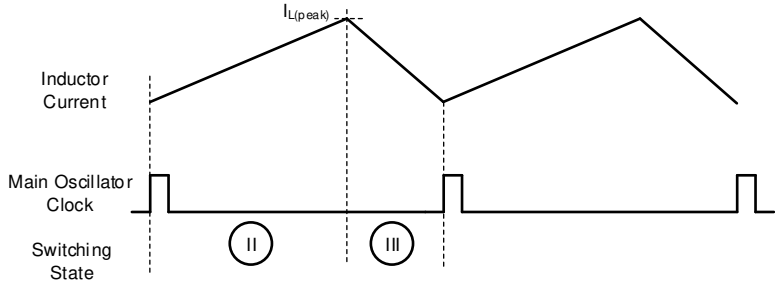

図 8-3. Inductor Current in Continuous Current Buck Operation

ADVANCE INFORMATION

8.3.1.2 Boost Mode

In boost mode operation, the converter starts a boost magnetization cycle (switching state I) with the internal clock signal. After it samples the inductor current, the device transitions to switching state II, which is the boost demagnetization state. The maximum duty cycle in boost mode is limited by the minimum boost on-time and the selected switching frequency.

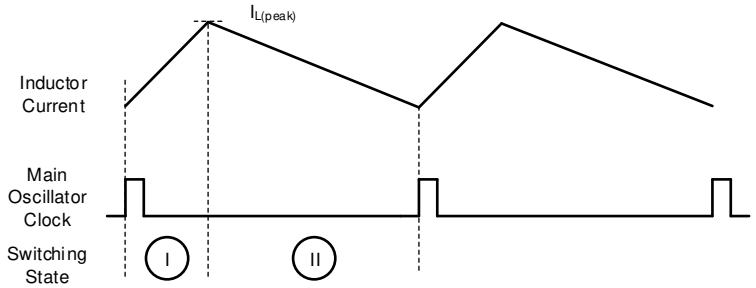

図 8-4. Inductor Current in Continuous Current Boost Operation

8.3.1.3 Buck-Boost Mode

As soon as the on time in boost mode operation is lower than the minimum on-time or the off-time in buck mode is lower than the minimum off-time, the control transits into the buck-boost operation. In the continuous current buck-boost mode, the control adds a boost magnetization (state I) switching cycle before the peak current is reached. Therefore, buck-boost operation mode always consists of all three switching cycles state I, state II, and state III. The peak current detection in this mode happens at the end of switching state I.

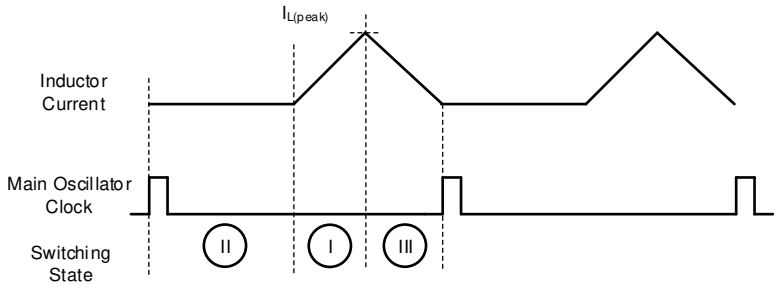

図 8-5. Inductor Current in Continuous Buck-Boost Operation

8.3.2 Power Save Mode

With the MODE pin low, power save mode is active. In this operating mode, the switching activity is reduced and efficiency is maximized. If the mode pin is high, power save mode is disabled. The converter operates in continuous conduction mode.

In boost or in buck mode, the converter is operating up to the duty cycles with the respective minimum off times or on times. If the timing limits are reached, the output voltage increases. As soon as this happens, the voltage regulation loop detects the increase and turns the device into a TI proprietary sleep mode as the energy consumed by the load is less than what the converter generates during switching. In this mode, both low sides are turned on to provide the high-side gate supply for HB1 and HB2 are charged. Other internal circuits are partially turned off to reduce the current consumption of the converter to a minimum possible. In case the output voltage reaches the nominal output voltage set point, the switching activity starts again.

In the buck-boost area where larger or smaller duty cycle is necessary, switching pulses are skipped. When necessary, the control initiates switching activities with a minimum time of state I or state III to maintain the inductor current as required by the voltage regulation loop.

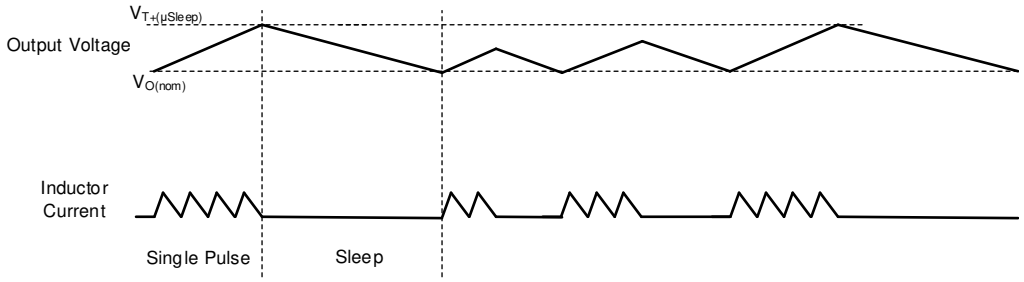

図 8-6. Timing Diagram for the Power Save Mode

If you intend operate in Buck operation with on-times smaller than ≈300ns and light load conditions, the recommendation is to turn-on the SYNC output instead of using the SYNC input function to provide low inductor current ripple.

ADVANCE INFORMATION

8.3.3 Programmable Conduction Mode PCM

The device also features a power save technique for high current applications. The main drawback of in most of the fixed frequency buck-boost operations are the power losses of the 4 active switches during the buck-boost mode. The Programmable Conduction Mode (PCM) is forcing the converter PWM logic to stop the switching operation in a programmable input voltage window. This function is available after the soft-start of the converter stage finishes. If the input voltage is inside the PCM window the output voltage approximately equals the input voltage as both high side FETs (Q1, Q4) are connecting the input to the output via the external power stage. Outside the programmed V_I window the selected thresholds are representing the nominal regulation targets of the converter.

The FETs supply are maintained by the integrated charge pump circuit of the device. During the PCM the current limit for the peak current protection is fully operational and the user benefits from a cycle-by-cycle current limit. The SCP hiccup protection can be used to overcome excessive thermal heating during a short like in the normal operation.

The integrated charge pump will operate down to the min. recommended PCM voltage. It is not recommended to program the PCM threshold below this value.

For low output currents and load profiles that have light load conditions the MODE pin can be used to further reduce the power consumption during the PCM is active. If the MODE pin is low the PCM deactivates the internal bias circuits to reduce the power consumption by monitoring the low inductor current.

The two voltage thresholds for this window are customer programmable via the I2C interface or selectable through the corresponding R2D pins.

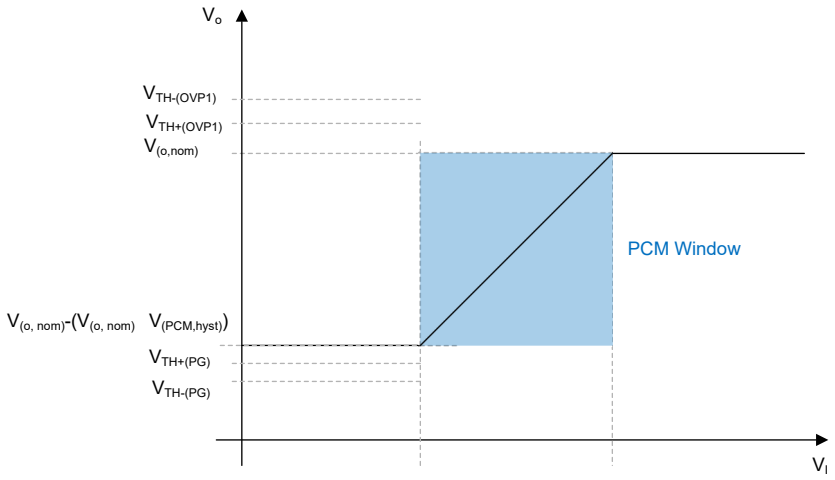

図 8-7. Output Voltage vs. Input Voltage

If you using the I2C interface of the device the upper threshold is set by the VOUT_TARGET1 logical register. The lower threshold is given by the hysteresis referenced to the Vo target and the selected hysteresis value set by the PCM_WINDOW_LOW register field.

If the thresholds are set by the external feedback divider the upper threshold of the PSM voltage window given by the FB-PIN and is equal to the nominal output voltage if the PCM is disabled. The lower threshold is programmed by default setting of the PCM_WINDOW_LOW register field and can be enabled/disabled via the CFG-PIN (PCM_EN). In case of using the ext. FB and R2D the VIN-FB-pin need to be connected to the input voltage using the same divider ration as the divider placed for Vo and connected to the FB-pin.

The OVP1 and power good thresholds of the protection features are fully functional if PCM is enabled and the input voltage outside the programmed window i.e. the convert regulates active to one of the two thresholds.

ADVANCE INFORMATION

8.3.4 Reference System

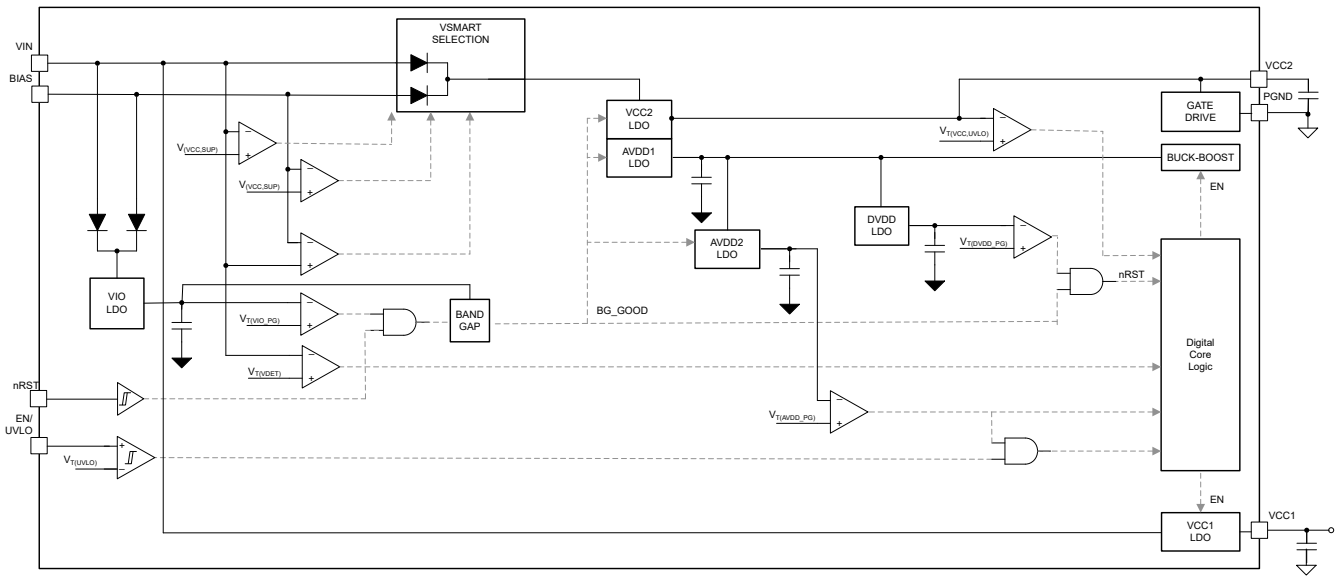

図 8-8. Functional Block Diagram Reference System

8.3.4.1 VIO LDO and nRST-PIN

The VIO LDO supplies the IO pin buffers and comparators. Once the voltage on the VIN-pin or BIAS-pin is above the positive going POR threshold VT+(POR) and the nRST-PIN is higher than VT+(nRST) the internal bias is active and the device is in standby mode.

When the nRST - pin is below the standby threshold $V_{T-(nRST)}$, the device is held in a low power shutdown mode to maintain a minimum input quiescent current of the device supply rails.

8.3.5 Supply Voltage Selection – VMAX Switch and Selection Logic

There are two pins to supply the LM51772 internal voltage regulators. Due to the internal supply voltage selection circuit, the device can reduce the power dissipation by ensuring a seamless operation at low input or output voltages as well as in transient operating conditions like an output short. The VMAX switch selects the pin with the lower voltage from the VIN or BIAS pin once the voltage on both is above the switch-over threshold ($V_{T(VCC, SUP)}$). If one pin voltage is lower than the threshold, the other supply pin is selected. And if both pins are lower than the switch-over threshold, the higher voltage of VIN or BIAS is selected as supply. The following are common configurations for the supply pins:

- The VIN pin is connected to the supply voltage. The BIAS pin is connected to VO. During start-up, that is as long as the output voltage is not higher than the supply switch-over threshold, the VIN supplies the internal regulators. Once V_O is high enough, the supply current comes from the BIAS pin.
- Both the VIN pin and the BIAS pin are connected together to the input supply voltage. This configuration is often used in applications where the input supply voltage is usually lower or equal than the output voltage. As the BIAS pin is connected to the input voltage, the device has the full current capability of the internal regulators at low input voltages for start-up.
- The VIN is connected to the input supply voltage and the BIAS pin is connected to an auxiliary supply (for example, an existing 12V DC/DC converter). This configuration is commonly used at high voltage applications on the input and output voltages where the power dissipation over the integrated linear regulators must be further minimized.

ADVANCE INFORMATION

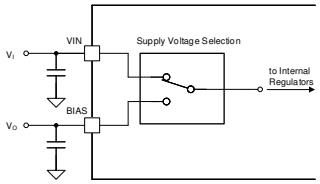

図 8-9. VMAX Supply Scenario 1

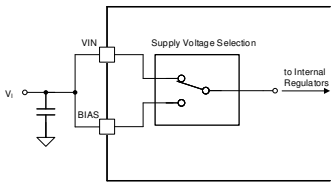

図 8-10. VMAX Supply Scenario 2

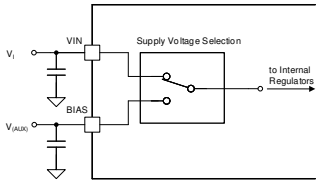

図 8-11. VMAX Supply Scenario 3

The VMAX does not directly select the highest voltage between the two supply pins BIAS and VIN. To achieve a minimum of power losses over the LDO the VMAX logic will decide what voltage is the closest one to the target supply $V_{T(VCC,SUP)}$. The 表 8-1 gives an overview for the selection conditions:

表 8-1. VMAX selection truth table

$V_{(BIAS)}$	$V_{(VIN)}$	VMAX supply
X	> $V_{T+(VCC,SUP)}$ && < $V_{(BIAS)}$	VIN-PIN
> $V_{T+(VCC,SUP)}$ && < $V_{(VIN)}$	X	BIAS-PIN
< $V_{T-(VCC,SUP)}$	X	VIN-PIN
X	< $V_{T-(VCC,SUP)}$	BIAS-PIN
> $V_{T+(VCC,SUP)}$ && > $V_{(VIN)}$	> $V_{T+(VCC,SUP)}$	VIN-PIN
> $V_{T+(VCC,SUP)}$	> $V_{T+(VCC,SUP)}$ && > $V_{(BIAS)}$	BIAS-PIN

There is a FORCE_BIAS bit if it is 0b1 it lowers and prioritizes the switchover threshold for the BIAS pin. Intention is to support an external supply of nominal 5V for the VCC2 but still be able to start-up with the VIN supply if the sequencing if the external supply does not meet the start-up timing. The selection of the VCC2 supply follows this behavior:

- If the BIAS voltages is below the $V_{T+(Force,BIAS)}$, then the VIN gets selected.
- If the BIAS voltage is above $V_{T+(Force,BIAS)}$, then the BIAS gets selected regardless of VIN being above the $V_{T+(VCC,SUP)}$

ADVANCE INFORMATION

8.3.6 Enable and Undervoltage Lockout

The LM51772 has a dual function enable and undervoltage lockout (UVLO) pin. Furthermore, the device features an internal UVLO function (VDET) which can be programmed through I2C interface. 図 8-12 shows the UVLO block diagram.

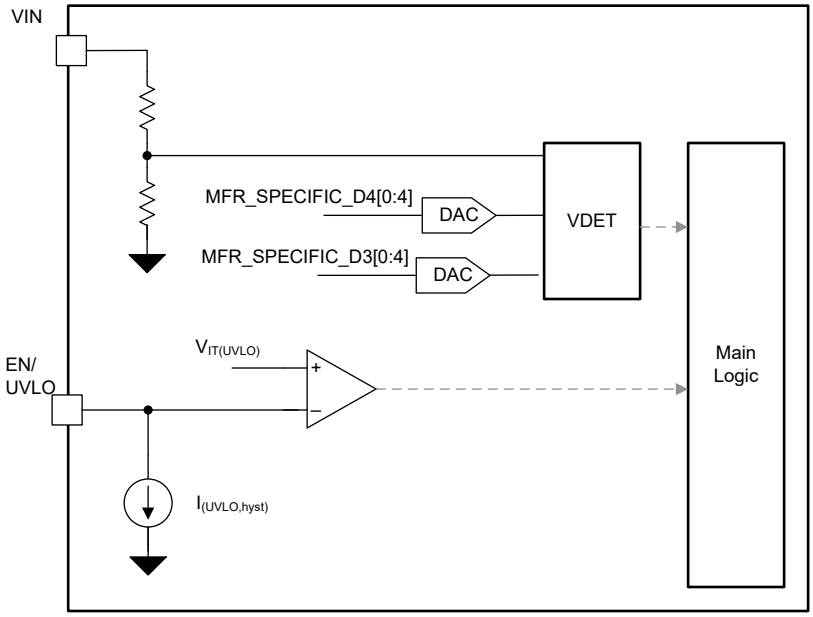

図 8-12. Functional Block Diagram UVLO and VDET

8.3.6.1 UVLO

With this function the device can detect an low input voltage condition for the power stage to avoid a brown out condition. The detection threshold as well as the required hysteresis is adjustable with the external voltage divider on the EN/UVLO - pin.

The UVLO features an internal delay time ($t_{d(UVLO)}$) for the shutdown to avoid any undesired converter shutdown due to input noise on the UVLO detection pin. The voltage on the EN/UVLO - pin must below the $V_{T-(UVLO)}$ threshold for the delay time $t_{d(UVLO)}$. Once these conditions are met the device logic will immediately stop the converter operation

If the EN/UVLO-pin voltage is above the $V_{T+(EN)}$ threshold the internal current source for the UVLO hysteresis is active. If the EN/UVLO-pin voltage is above the $V_{T+(UVLO)}$ threshold the internal current source for the UVLO hysteresis is off.

8.3.6.2 VDET Comparator

The VDET features an internal UVLO for the device. The comparator output goes directly to the digital main logic to enable disable the converter operation.

The rising and falling threshold can be programmed via the VDET_RISE, VDET_FALL register field. The VDET_EN register field enables or disables the function.

For seamless functionality is recommended to change the programmable VDET parameters in the CONV_OFF state.

If the programming for the VDET thresholds changes, make sure to disable the block via the EN_VDET register field first. Change the threshold register(s) and activated the VDET block again by setting EN_VDET to 0b1

ADVANCE INFORMATION

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8.3.7 Internal VCC Regulator

8.3.7.1 VCC1 Regulator

The LM51772 features a VCC1 regulator which provides an LDO output for auxiliary use in the system. VCC1 gets directly supplied by VIN pin. In most applications the output is used to supply the I2C controller device which sends data to the LM51772. You can find a drawing for this application below.

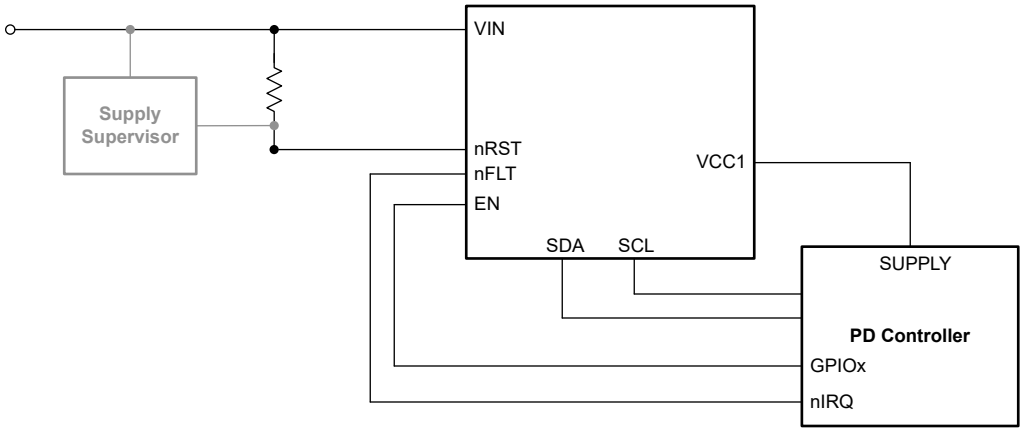

図 8-13. Simplified Schematic

To ensure the power sequence of such a system can be met the VCC1 starts-up when the device is entering the standby mode. See a typical power up sequence below.

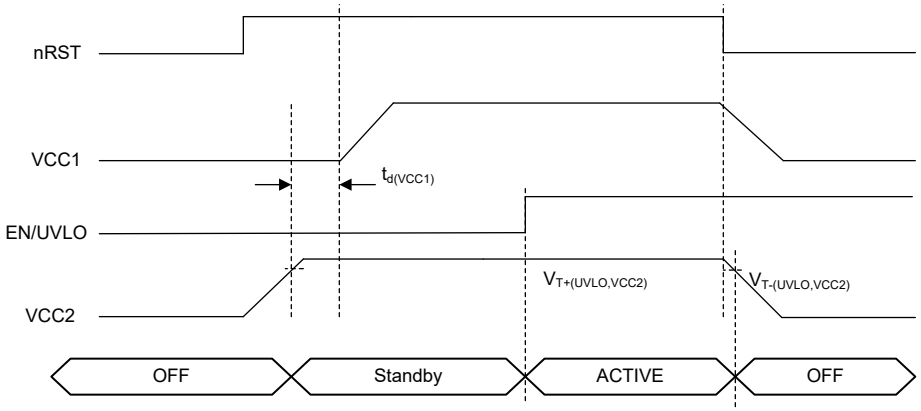

図 8-14. Timing Diagram VCC Regulator

The VCC1 regulator provides high DC accuracy at light load condition to support a use as a reference voltage for external circuits e.g. a comparator or operational amplifier.

The VCC1 is enabled/disabled via R2D interface. Therefore the start-up of VCC1 is gated by the R2D readout.

8.3.7.2 VCC2 Regulator

The VCC2 regulator is the supply for the integrated gate driver. The LDO starts to enable and pre-bias once the voltage on the nRST-Pin is higher that its rising threshold. If the EN/UVLO pin is higher that its rising threshold the VCC2 is fully active and provides the target performance specified by the electrical characteristics parameters.

It is not recommended to connect an external load to the VCC2-PIN

8.3.8 Error Amplifier and Control

8.3.8.1 Output Voltage Regulation

The device features an internal error amplifier (EA) to regulate the output voltage. The output voltage gets sensed on the FB-pin. The reference for the EA is supplied via the soft-start and V_O tracking pins. The COMP-pin is the output of the gm-stage and gets connected to the external compensation network.

The voltage over the compensation network is the target for the inner current control loop which sets the inductor peak current demand.

8.3.8.2 Internal Output Voltage Regulation

To maintain fixed voltage and interface programmable voltage the device contains an internal voltage divider. In this case the FB is not applicable for sensing the output voltage for the loop regulation. Instead the VOUT-pin is used to sense the output voltage on the power stage.

The device detects via the FB-pin if it shall operate with an external or internal voltage divider. If the voltage on the FB-pin is higher than $V_{T+(SEL,iFB)}$, before the soft-start is initiated, if the part should operate with a internal or external feedback. The selection of internal and external FB cannot be done dynamically and the pin information gets latched until the next EN or $V_{(POR)}$ power cycle.

The resolution of the programming can be changed with the SEL_DIV20 bit.

If the V_OUT register read back is used the low voltage clamping will be done with whatever SEL_DIV20 value is programmed at this time. If SEL_DIV20 is updated after VOUT_A, the clamping might not be correct anymore. To guarantee correct clamping its recommended to (re-)write VOUT_A after changing SEL_DIV20 bit.

Below an overview of the possible Vo setting according the VOUT_A and SEL_DIV20

表 8-2. SEL_DIV 20 = 0b0:

Parameter	Value
Output voltage min.	3.3V
Output voltage max.	24V
Output voltage programming step size typ.	10mV

ADVANCE INFORMATION

You can use the following equation to calculate the nominal output voltage:

$$V_{(O,NOM)} = [[VOUT\_TARGET1\_MSB[3:0]][VOUT\_TARGET1\_LSB[7:0]]] \cdot 10\ mV \quad (1)$$

表 8-3. SEL_DIV 20 = 0b1:

Parameter	Value
Output voltage min.	3.3V
Output voltage max	48V
Output voltage programming step size typ.	20mV

表 9-18

The read-out register value of the 'VOUT_A' control register is clamped for the lower and for the upper limit of the register range.

- The reg. readout value is clamped to the lowest clamp voltage (e.g. 3.3V if SEL_FB_DIV20 = 0b1) if a register value below the value of clamp voltage (e.g. 3.3V) has been written in before.
- The reg. readout value is clamped to the highest clamp voltage (e.g. 48V if SEL_FB_DIV20 = 0b1) if a register value above the highest value of clamp voltage (e.g. 48V) has been written in before.

You can use the following equation to calculate the nominal output voltage:

$$V_{(O,NOM)} = [[VOUT\_TARGET1\_MSB[3:0]][VOUT\_TARGET1\_LSB[7:0]]] \cdot 20\ mV \quad (2)$$

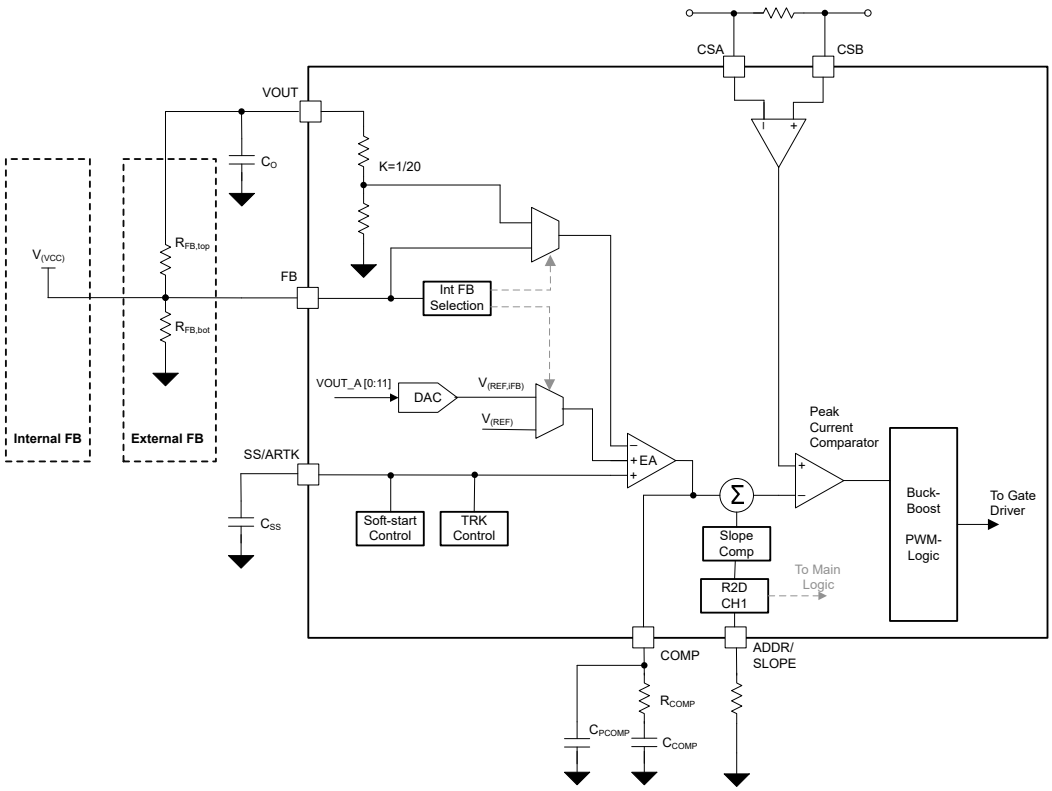

図 8-15. EA Functions Block Diagram

ADVANCE INFORMATION

8.3.8.3 Dynamic Voltage Scaling

The device features a dynamic voltage scaling. In case the output voltage register gets programmed during the converter is in operation. It shall avoid any excessive current and voltage spike as the control loop bandwidth is set by external components. If the output voltage target gets programmed in the converter off state the soft-start will ramp to newly programmed target voltage.

Once the VOUT_A field of the register is changed the reference voltage will slowly change-over to the new target value. The rising and falling slew rate shall not exceed the defined $\Delta V_{o(DVS)}$ within the time $t_{d(DVS)}$ the slope time is programmable via NVM setting.

If the converter operates in PSM i.e. the inductor current cannot go to negative values. The device features a passive and a active DVS configuration, selectable via NVM setting. If passive DVS is selected the Vo slope of the system will not follow the defined DVS slew rates as the output capacitor can only be discharged passively. If active DVS is selected the internal output discharge is active during the negative ramp of the DVS. The maximum discharge current is used for the active DVS setting not the register selection of the discharge strength. The output capacitor voltage can follow the reference as long as the capacitor is selected to match the maximum discharge current.

If you use the internal feedback or a fixed voltage version, It is not recommended to apply a DTRK signal or change ATRK during the o change by the DVS function.

8.3.9 Short Circuit - Hiccup Protection

The LM51772 features a short circuit protection or over current protection. This protection uses cycle-by-cycle peak current sensor connected to the CSA and CSB-pin. There are two modes for this protection. In hiccup mode, the controller stops the converter operation after detecting cycle-by-cycle peak current longer as the hiccup mode on-time. The converter logic initiates a discharge of the soft-start capacitor and the output stays off until the hiccup mode off-time elapses. Then the logic will exit the hiccup mode and re-start the output with a normal soft-start sequence were the soft-start capacitor is charged with the internal current source. If the short or overload persist the hiccup timer starts again after the soft-ramp finishes. If hiccup mode protection is not enabled, the device will operate in cycle-by-cycle current limiting as long as the overload condition persists. The peak inductor current limit in steady state is calculated as shown in 式 3

$$I_{L(PEAK,\ ILIMIT)} = \frac{50mV}{R_{CS}} \tag{3}$$

ADVANCE INFORMATION

8.3.10 Current Monitor/Limiter

8.3.10.1 Overview

The device features two high voltage current sensors. The first one maintains the peak current sensing between the CSA and CSB pins. The second current sensor inputs are connected to the ISNSP and ISNSN pins. This optional current sensing provides the capability to monitor (CDC-pin) and limit (ILIMCOMP-pin) either the input or the output current of the DC/DC converter.

If the optional current sense amplifier is not used, the customer can connect the ILIMCOMP pin to VCC2 to turn the bias current consumption of this block and all current limiting/monitoring functions off. It is not recommended to do this dynamical during the operation of the device because the configuration gets latched at start-up of the converter. In other words the current monitoring block cannot be disabled dynamically the pin information gets latched until the next EN, EN_CONV or $V_{(POR)}$ power cycle. It is recommended to directly connect the ILIMCOMP to VCC2 or with a pull-up resistor < 50kΩ.

Use the CFG pins or register table to select the following desired operation modes:

1. If the current sense amplifier operates in monitor configuration i.e. IMON_LIMITER_EN is set to 0b0 by I2C interface or R2D selection both pins, CDC and ILIMCOMP, provide a proportional current to the differential sense voltage.
2. The current monitor block limiter operation is activated via MON_LIMITER_EN bit or the corresponding R2D setting for this signal
3. The negative current limit direction is selected by the EN_NEG_CL_LIMIT or through the R2D selection for this signal
4. If ADDR/Slope (CFG1) selects a I2C address (pin to VCC or GND) the main logic activates the I2C interface and the internal DAC as default reference for the current limit threshold. The value for the DAC is set by the ILIM_THRESHOLD register. The internal DAC can be disabled via a register setting through the I2C interface to set the current limit again by a external resistor on ILIMCOMP

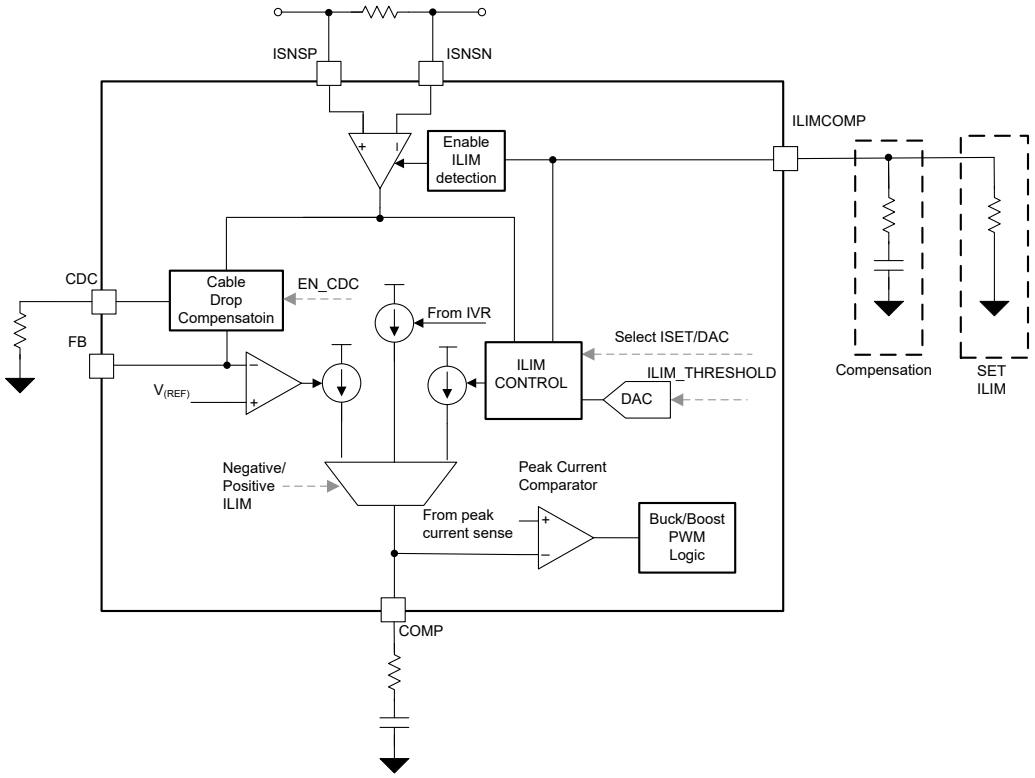

図 8-16. Current Monitor Functional Block Diagram

8.3.10.2 Output Current Limitation

In this configuration the current sense has an internal feedback to the peak current limit of the device. The ILIM circuit regulates the peak current limit down as long as the differential voltage between ISNSP and ISNSN exceeds the internal offset voltage of the ILIM circuit. The ILIM threshold can be set via the register programming or via the an ISET resistor in the ILIMCOMP pin.

If the threshold for the current limit is set by the internal DAC the bandwidth of the current limit can be optimized for different with a resistor and capacitor on the ILIMCOMP - pin. It is recommended to select the compensation bandwidth according the following equations

If the current limit threshold is selected by a resistor a internal comparator monitors the voltage on the ILIMCOMP pin. If the voltage exceeds the ISET threshold the current limit is reached. The threshold voltage for ISET can be calculated with:$V_{(\mathrm{ISET})} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(\mathrm{ILIMCOMP})} \times R_{(\mathrm{ILIMCOMP})}$

The current through the sense resistor can be monitored by the CDC pin simultaneously.

The read-out register value of the "ILIM_THRESHOLD" control register is clamped for the lower and for the upper limit of the register range.

- The reg. readout value is clamped to the lowest clamp current (e.g. 500mA) if a register value below the value of clamp current been written in before.
- The reg. readout value is clamped to the highest clamp current if a register value above the highest value of clamp current has been written in before.

8.3.10.3 Output Current Monitor

The current through the sense resistor can be monitored by the CDC pin simultaneously and has no impact to a configured current limit via the ILIMCOMP pin. If the limiter is disabled (IMON_LIMITER_EN = 0b0) both pins provide a proportional current to the differential voltage of ISNSP/N with. The Voltage can be calculated with

$$V_{(CDC)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(CDC)} \times R_{(CDC)} \quad (4)$$

$$V_{(\mathrm{ILIMCOMP})} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(\mathrm{ILIMCOMP})} \times R_{(\mathrm{ILIMCOMP})} \quad (5)$$

ADVANCE INFORMATION

8.3.11 Oscillator Frequency Selection

The LM51772 has a low tolerance internal trimmed oscillator. With the RT pin left open, the oscillator frequency is 75kHz. With the RT pin grounded, the switching frequency is at the maximum of 2.5MHz. The oscillator frequency can be programmed up or down by connecting a resistor from the RT pin to ground. To calculate the RT resistor for a specific oscillator frequency, use 式 6.

$$R_{(RT)} = \frac{1}{32 \cdot 10^{-12} \cdot f_{sw}} \quad (6)$$

The RT pin is regulated to 0.75V by an internal voltage source when the device is in active mode. Therefore, the switching frequency can be dynamically changed during operation by changing the current flowing through the resistor. 図 8-17 and 図 8-18 show two examples for changing the frequency by the switching the resistor value or applying a external voltage source through a resistor. Connecting any additional capacitance directly to the RT pin is not recommended.

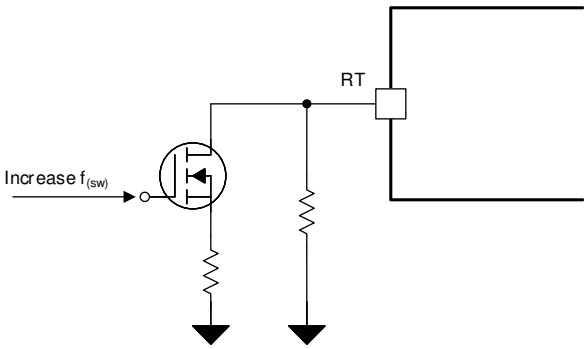

図 8-17. Frequency Hopping Example

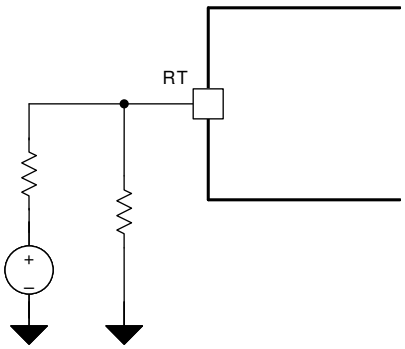

図 8-18. Dynamic Frequency Changing Example

ADVANCE INFORMATION

8.3.12 Frequency Synchronization

The device features an internal phase looked loop (PLL), which is designed to transition the switching frequency seamlessly between the frequency set by the RT pin and the external frequency synchronization signal. If no external frequency is provided, the RT pin sets the center frequency of the PLL. The external synchronization signal can change the switching frequency ±50%. To ensure low quiescence current, the input buffer of the SYNC pin is disabled if no valid sync frequency, that is a frequency signal outside the recommended synchronization range is applied.

The $f_{(SW)}$ synchronization stops if the device enters power save mode or µSleep operation, if enabled. Once the converter enters the PWM operation again, the device re-syncs to a pin signal. The synchronization timings are given in 図 8-20

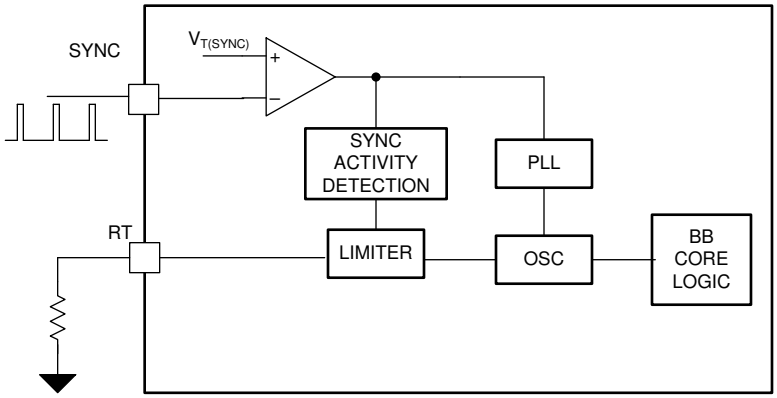

図 8-19. Main Oscillator Functional Block Diagram

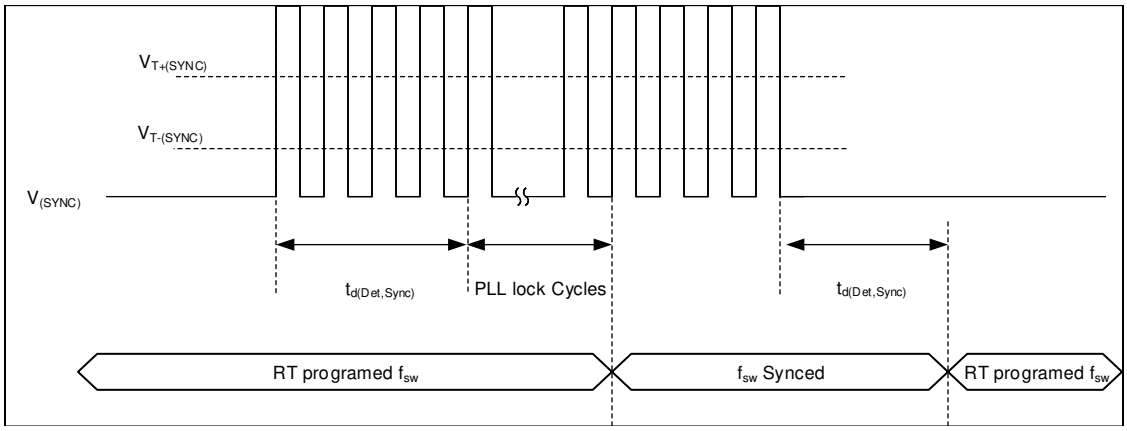

図 8-20. Timing Diagram SYNC Function

The sync pin can be programmed through I2C or config pin CFG2 as input or output.

ADVANCE INFORMATION

8.3.13 Output Voltage Tracking

There are two kinds of output voltage tracking features integrated in the device.

- Analog voltage tracking function through the SS/ATRK pin
- Digital voltage tracking function through the DTRK pin

8.3.13.1 Analog Voltage Tracking

For the analog output voltage tracking, an external applied voltage overwrites the reference voltage for the output regulation loop. Although it is possible, it is not recommended to apply this voltage before the soft start is finished because the soft-start ramp time and, therefore, the input current during the start-up is changed.

As the internal error amplifier is designed to use the lowest reference input voltage, the applied voltage on the SS/ATRK pin is only effective for voltages lower than the V_{ref} of the feedback pin. Hence, the maximum voltage for the output is determined by the resistor network on the FB pin.

If the analog voltage tracking is used to start-up the converter voltage a change at the mode pin from high to low or low to high will indicate the logic that the soft-start is completed.

8.3.13.2 Digital Voltage Tracking

The DTRK input of the LM51772 directly modulates the internal reference voltage. This function activates if the voltage on the DTRK pin is higher than the rising threshold of $V_{T(DTRK)}$ and a PWM signal in the recommended frequency is applied to the pin.

The maximum output voltage during digital tracking cannot exceed the nominal reference voltage for the FB resistor divider. The applied PWM signal reduces the internal reference voltage in relation with the duty cycle on the DTRK pin. A small duty cycle means less output voltage and a high duty cycle of the PWM input represents a high output voltage. For example, a duty cycle of 30% causes a output voltage of 30% of the selected voltage by the FB divider resistors.

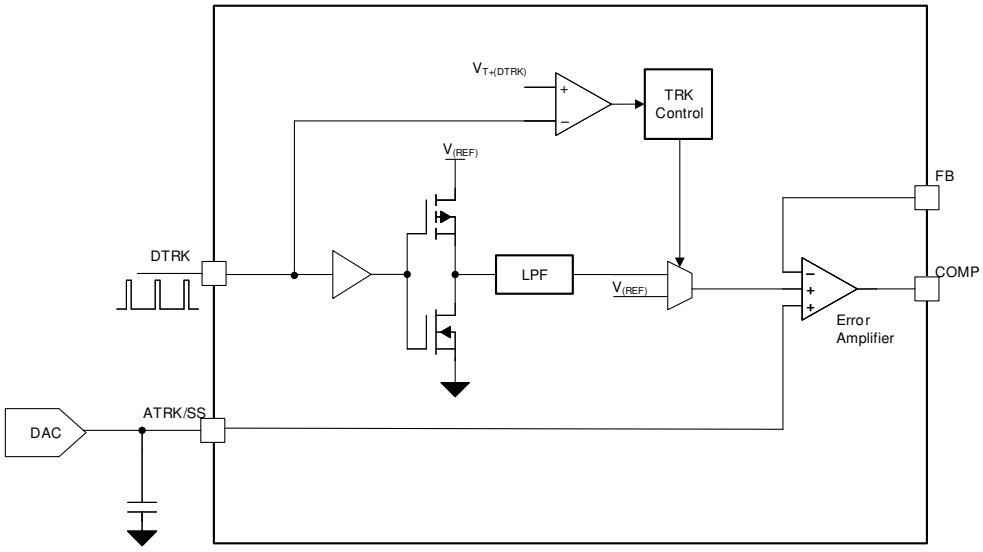

図 8-21. Output Voltage Tracking Functional Block Diagram

ADVANCE INFORMATION

8.3.14 Slope Compensation

The LM51772 provides slope compensation to ensure stable operation and the best transient performance over a wide operating range. According to peak current mode control theory, slope compensation is required at operation with duty cycle greater than 50%.

First a correction factor needs to be calculated from 式 7

$$m_{SC} = \frac{R_{CS}}{f_{SW} \times L} \times 625 \quad (7)$$

Based on the calculated correction factor the slope compensation can be programmed through I2C or by connecting a resistor to ADDR/Slope pin. See 表 8-4 for selecting the resistor value based on the slope compensation correction factor.

8.3.15 Configurable Soft Start

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM51772 features an adjustable soft start that determines the charging time of the output. The soft-start feature limits inrush current as a result of high output capacitance to avoid an over-current condition.

At the beginning of the soft-start sequence, the SS voltage is 0 V. If the SS pin voltage is below the feedback reference voltage, V_{REF}, the soft-start pin controls the regulated FB voltage and the internal soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the output voltage and FB pin. Once the voltage on the SS exceeds the internal reference voltage, the soft-start interval is complete and the error amplifier is referenced to $V_{(REF)}$.

The soft-start time ($t_{(ss)}$) is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} \quad (8)$$

The soft-start capacitor is internally discharged when the converter is disabled because of the following:

- EN/UVLO falling below the operating threshold
- VCC falling below the VCC UV threshold
- The device is in hiccup mode current limiting.
- The device is in thermal shutdown.

ADVANCE INFORMATION

8.3.16 Drive Pin

The device features a high voltage drive pin (DRV1) to support an input or output disconnect FET. This in can be also used as a driver for a charge pump output to do a reverse polarity protection using a external n-channel FET. The supply for this pin can be selected by R2D and I2C configurations.

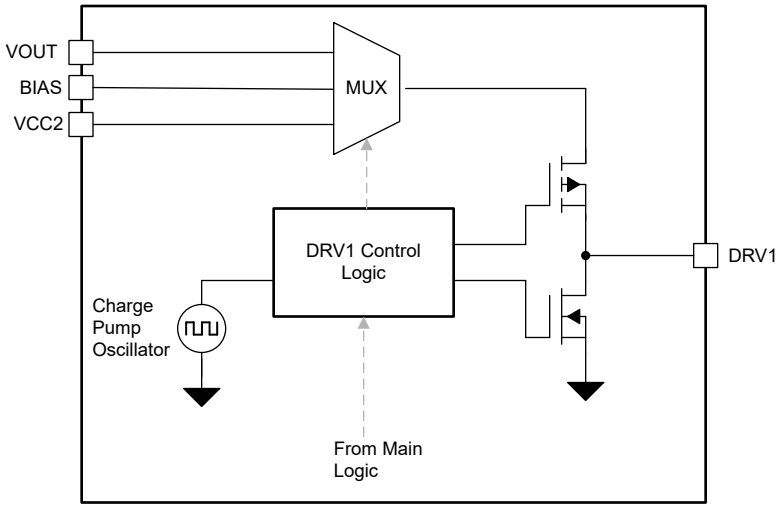

図 8-22. Functional Block Diagram - DRV pin

The following configurations are possible with to support with the DRV1 pin:

1. Open drain output.
2. High Voltage Push-pull supplied by VOUT
3. High Voltage Push-pull supplied by VBIAS
4. CP drive pin supplied by the VCC2

The sequencing of the DRV pin is depending on the R2D/I2C setting an given by the state diagram XREF

ADVANCE INFORMATION

8.3.17 Dual Random Spread Spectrum – DRSS

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function is enabled by the CFG pin. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the SYNC pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

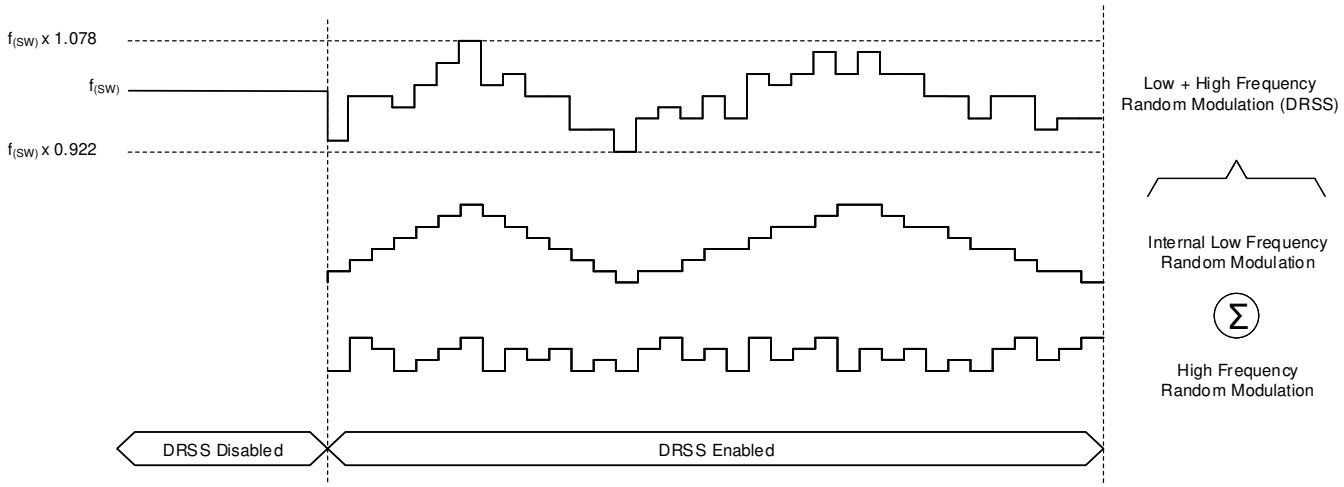

図 8-23. Dual Random Spread Spectrum

ADVANCE INFORMATION

8.3.18 Gate Driver

The LM51772 features four internal logic-level nMOS gate drivers. The drivers maintain the high frequency switching of both half bridges needed for a buck-boost operation. If the device is in boost or buck mode, the other half bridge high-side switch needs to be permanent on. The internal gate drivers support this by sharing the current from the other half bridge, which is switching. Therefore, a minimum of quiescent current can be provided as no additional char pump is needed. Due to the high drive current, the LM51772 can support a wide range of external power FETs as well as a parallel operation of them.

The LO and HO outputs are protected with a shoot-through protection, which allows both outputs are not turned on at the same time. If the PWM modulation logic of the buck-boost turns the LOx pin off, the HOx pin is not turned on until the following are true:

1. A minimum internal transition time ($t_{t(dead)}$) is reached.
2. The voltage on the LOx pin drops below the detection threshold $V_{TH(GATEOUT)}$.

This behavior is maintained and vice versa if the HOx pin turns off first.

The high-side supply voltage for the gate driver are monitored by an additional bootstrap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. If the voltage drops below the threshold the buck-boost converter operation turns off. The device restarts automatically once the positive going threshold is reached with the soft-start scheme.

Additionally, the LM51772 monitors the upper voltage between SWx and HBx. If this voltage exceeds the threshold voltage of the clamping circuit, the LM51772 activates a internal current source to pull the voltage down.

The minimum observed internal transition (dead) -time can be selected by the registers SEL_SCALE_DT, SEL_MIN_DEADTIME_GDR. The SEL_SCALE_DT can also be selected via the CFG-PIN in case the I^2C interface is not used in the application. Additionally there is a optional frequency dependency of the transition (dead) -time between high and low side. This addresses the usual differences of the silicon MOSFET Q_g in high power applications with low switching frequencies and lower power application with higher switching frequencies. The frequency dependency can be enabled/disable be the register EN_CONST_TDEAD

ADVANCE INFORMATION

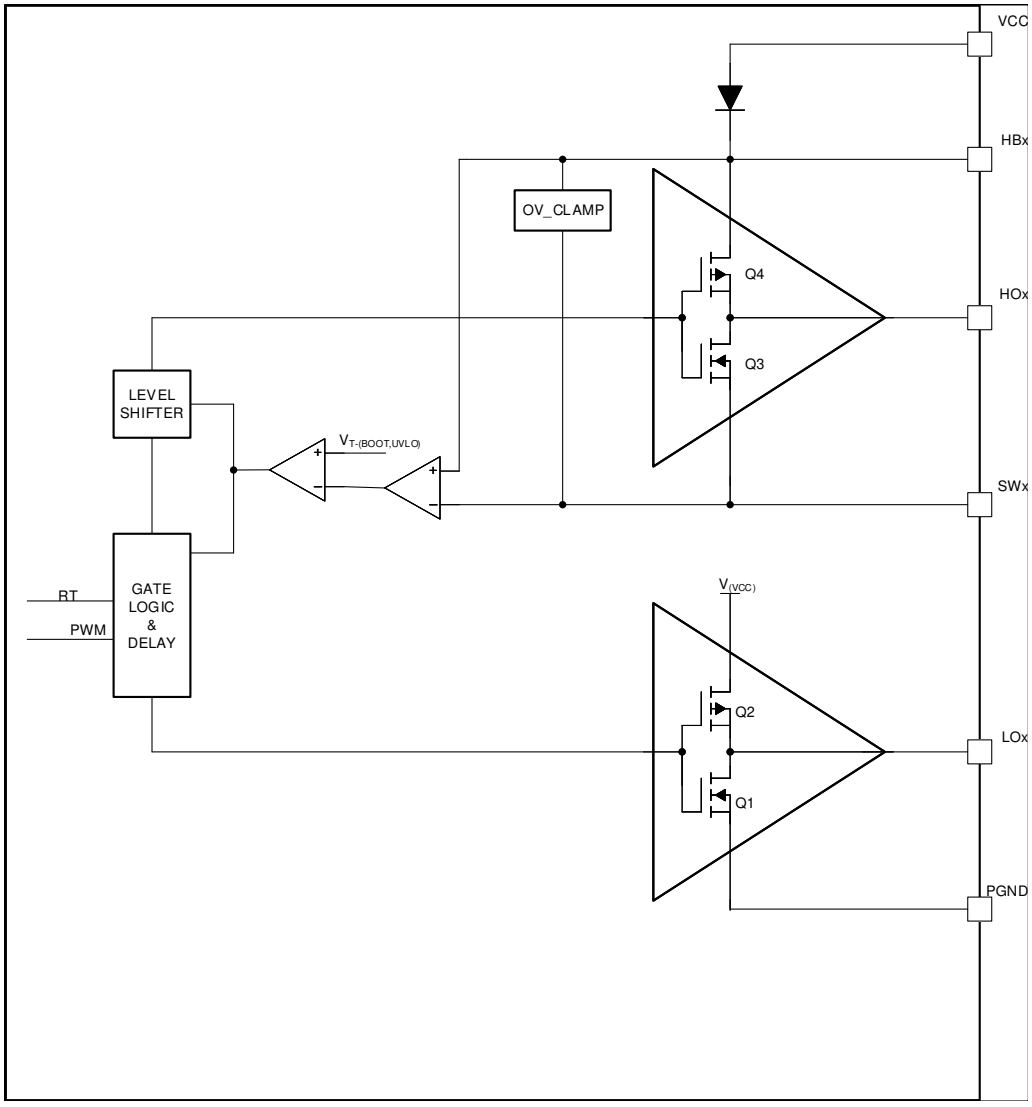

図 8-24. Functional Block Diagram Gate Driver

8.3.19 Cable Drop Compensation (CDC)

The cable drop compensation feature helps to keep the output voltage at the nominal value over a wide range of load current without the need for additional remote sensing. The voltage drop compensation measures the current and feeding back the current information to the internal voltage control loop of the converter

If enabled, the gm stage of the current monitor sensor (ISNSP/N) sends a proportional current to the CDC pin. The voltage across the CDC pin is applied as a offset to the nominal output voltage. It is recommended to select the resistor value on the CDC-pin not to exceed 1V. The Equation below:

$$V_{(CDC)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm_{(CDC)} \times R_{(CDC)} \quad (9)$$

The CDC function can operate for the internal or external feedback divider with the same behavior.

To achieve a accurate operation for the desired range cable drop compensation the gain of the CDC offset can be programmed by the CDC_GAIN register bits.

The CDC function operates equally with the external Feedback divider. It's recommended to use a 100kΩ feedback divider top resistance.

The figure below shows the control curve of the CDC feature.

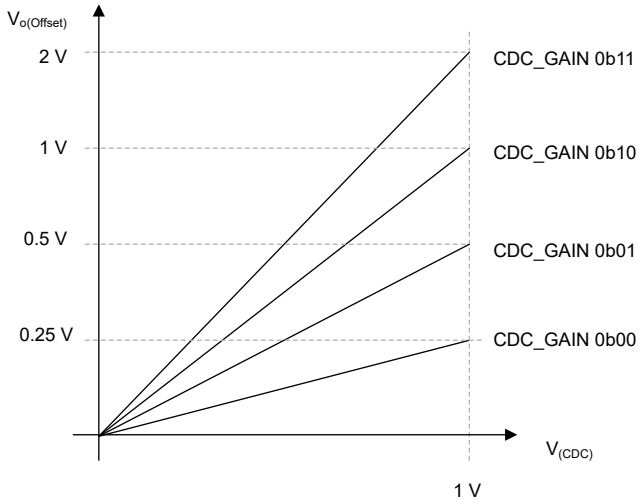

図 8-25. Vo Offset vs. CDC voltage

ADVANCE INFORMATION

8.3.20 CFG-pin and R2D Interface

The LM51772 has four register to digital channels, where the CFG1 is allocated to the ADDR/SLOPE -pin. The channels CFG3 and CFG4 are ultiplexed with the SDA/SCL pins.

The resistor selection on the CFG pins is read and latched during the power-up sequence of the device. The selection cannot be changed until the voltage on the EN or UVLO reaches the falling threshold or VCC voltage drops below the $V_{CCT-(UVLO)}$ threshold. The 表 8-4 shows the possible device configurations versus the different resistor values on the CFG pins.

表 8-4. ADDR/Slope Pin (R2D-CH1) Configuration Overview

#	$R_{(CFG)}$ / kΩ	I2C/ADDR	Slope Compensation
1	GND	I2C ENABLED Address 0x6A	Default NVM setting 0.875
2	0.511	I2C DISABLED	0.25
3	1.15		0.375
4	1.9		0.5
5	2.7		0.625
6	3.8		0.75
7	5.1		0.875
8	6.5		1
9	8.3		1.5
10	10.5		2
11	13.3		2.5
12	16.2		3
13	20.5		3.5
14	24.9		4
15	30.1		4.5
16	VCC2	I2C ENABLED Address 0x6B	Default NVM setting 0.875

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表 8-5. CFG2 Pin (R2D-CH2) Configuration Overview

#	$R_{(CFG)}$ / kΩ	EN_SYNC_OUT	SYNC_IN_FALLING	VDET_EN	PCM_EN
1	0	DISABLED	DISABLED	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED	DISABLED	ENABLED
10	10.5	ENABLED			
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED			

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表 8-6. CFG3 Pin (R2D-CH3) Configuration Overview

#	$R_{(CFG)}$ / kΩ	EN_VCC1	INC_INDUCT_De-Rate	µSLEEP	SCALE_DT
1	0	DISABLED	DISABLED	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED	DISABLED	ENABLED
10	10.5	ENABLED			
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED			

ADVANCE INFORMATION

表 8-7. CFG4 Pin (R2D-CH4) Configuration Overview

#	$R_{(CFG)}$ / kΩ	DRSS	SCP – Hiccup Mode	Negative Current Limit	Current Limit
1	0	DISABLED	DISABLED	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED	DISABLED	ENABLED
10	10.5	ENABLED			
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED			

ADVANCE INFORMATION

8.3.21 Advanced Monitoring Features

8.3.21.1 Overview

The device features a status register in which the current operation status can be pulled by the interface.

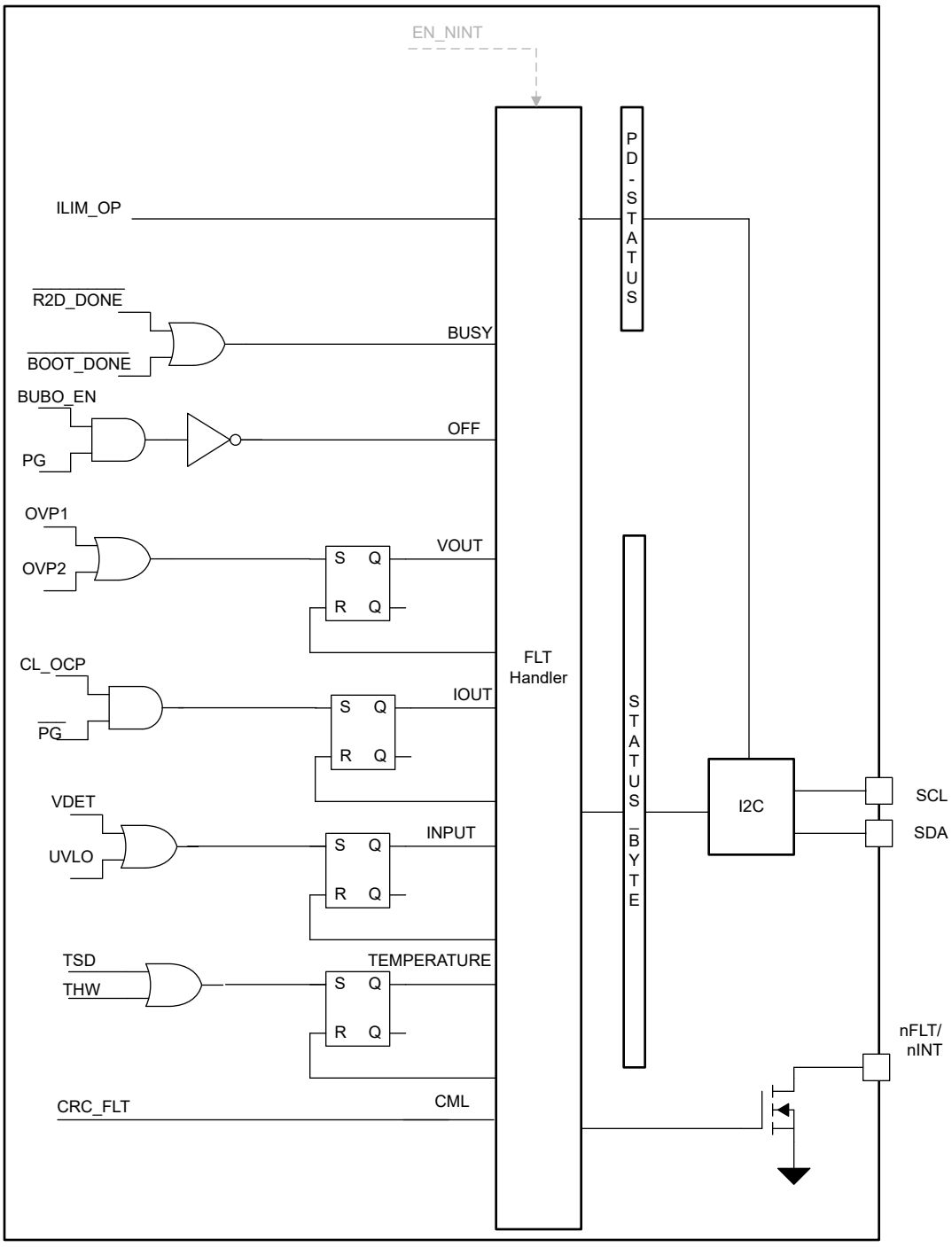

図 8-26. Functional Block Diagram Fault Handler

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8.3.21.2 BUSY

If the device register field is busy or in use by another instance this bit is high. Writing via the I^2C interface not recommended during busy flag high. This bit is only observed after the device start-up

8.3.21.3 OFF

Is high if the device is not providing a high enough output voltage ($V_{(VOUT)} < V_{T+(PG)}$). This bit is also high if the converter is turned off by system input. This bit is only observed after the device start-up

8.3.21.4 VOUT

Output voltage over voltage threshold (OVP1, OVP2) was exceeded. This error gets latched until the register is cleared or a power cycle happens

8.3.21.5 IOUT

Over current protection of peak current sensor is reached. This error gets latched until the register is cleared or a power cycle happens

8.3.21.6 INPUT

The input voltage detection (VDET) or the UVLO resistor senses voltage is blow the falling threshold. This error gets latched until the register is cleared or a power cycle happens

8.3.21.7 TEMPERATURE

The device has entered TSD state or the programmable thermal warning threshold is reached . This error gets latched until the register is cleared or a power cycle happens

8.3.21.8 CML

The device detects an internal logic fault i.e. the NVM memory check-sum has detected data retention event.

8.3.21.9 OTHER

unused

8.3.21.10 ILIM_OP

This signal is enabled together with the current limiter. If the current limiter is off the signal is low. If the programmed (via I^2C or ISET) current limit threshold is reached the signal goes high. The PD-STATUS byte is instantaneously changing with the ILIM_OP signal. The input signal gets de-glitch in the analog domain.

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8.3.21.11 nFLT/nINT Pin Output

If the bit EN_NINT is set to 0b0 the nFLT/nINT pin indicates all faults that is reported by the signal to the in the STATUS byte.

After a restart of the converter operation or in case the failure mode disappears the nFLT pin will go back to HighZ. The input signals to the STATUS-BYTE and therefore the nFLT/nINT pin are de-glitched. Because of this the maximum reaction time of the FLT pin is given by $t_{d(nFLT-PIN)}$

It is not recommended to change the EN_NINT dynamically during operation, but during the CONV_OFF state.

In case the EN_NINT = 0b1 the nFLT/nINT pin acts as interrupt pin. A change of the instantaneous signal to the STATUS_BYTE as well as the inputs to the USB_PD_STATUS_0 toggles the pin.

8.3.21.12 Status Byte

The following methods can be used to clear a fault

1. Perform an I^2C write to the CLEAR_FAULTS byte.
2. Perform an I^2C read to the CLEAR_FAULTS byte.
3. Perform an I^2C write to the STATUS_BYTE where a fault is indicated with a '1' and clear this bit by setting it to '1'. This allows to write an old STATUS_BYTE to clear the old faults for diagnosis.

8.3.22 Protection Features

8.3.22.1 Thermal Shutdown (TSD)

To avoid the case of a thermal damage of the device the temperature of the die is monitored. The device will stop operation once the sensed temperature rises over the thermal shutdown threshold. After the temperature drops below the thermal shutdown hysteresis the TSD signal goes back to normal and the converter will return to normal operation according to the main FSM definition.

8.3.22.2 Over Current Protection

The device features a hiccup mode short circuit protection to avoid excessive power dissipation in the die or at the fault of the application in the System. The CL_OCP triggers if the peak current sensing voltage between CSA-pin and CSB-pin is exceeded.

If enabled the protection will stop the converter operating and re-start the converter in case a short is event is detected.

The bit HICCUP_EN in the NVM register enables the OCP.

8.3.22.3 Output Over Voltage Protection 1 (OVP1)

This over voltage protection monitors the voltage of the FB-pin

As this threshold is referenced to the $V_{(REF)}$ the OVP1 is still working if one of the tracking features has changed the V_o target value. The OVP protection can be disabled during the $V_o$change of one of the V_o tracking features.

The converter maintains in regulation even the OVP1 threshold triggers.

The OVP1 is disabled during uSleep to avoid additional leakage current. The OVP signal gets masked that no fault is indicated from this signal during the uSleep operation.

This protection is disabled during the soft-start procedure and if the iFB is used instead of the ext. FB

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8.3.22.4 Output Over Voltage Protection 2 (OVP2)

This feature shall avoid any damage to the device in case the ext. feedback pin is not working properly i.e is shorted

The over voltage protection is realized by the converter core and reference system. The device main logic only monitors the OVP 2 function the converter logic will take an appropriate measure (e.g. emergency skip mode) to avoid a further increase of the output voltage.

If the output voltage threshold $V_{T+(OVP2)}$ is reach on the VOUT-pin the buck-boost core logic disables the converter power stage and enters a high impedance state at the switch nodes. If the output voltage falls back under this threshold the convert operation is resumed

Due to wide recommended operation range, the OVP2 protection of lower Vo application is limited. Therefore the OVP2 threshold is programmable by the V_OVP2 register field.

For power savings e.g. in burst mode or uSleep the OVP2 circuit can be turned off. In this case it need to be ensured that a fault on the feedback or any other mechanism enter- re-enter sleep will not impact the correct function of OVP

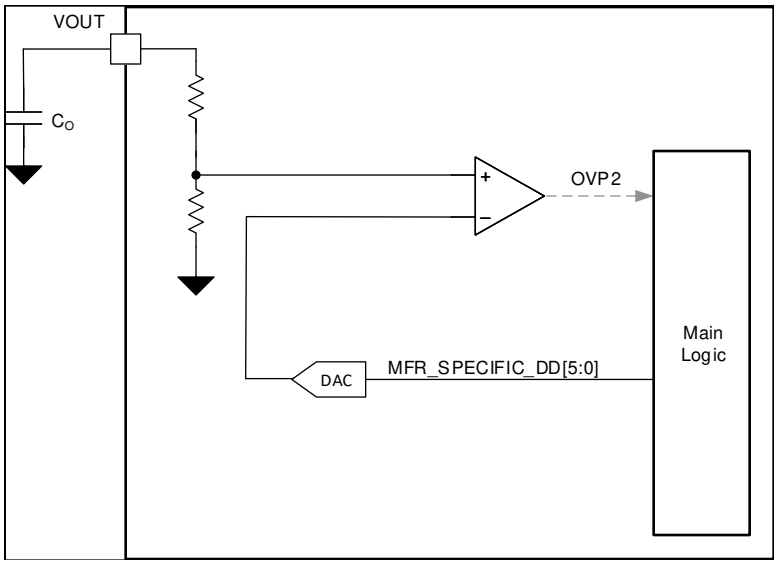

図 8-27. Functional Block Diagram OVP2

8.3.22.5 Input Voltage Protection (IVP)

The input over voltage protection is realized by the converter core modulation scheme. It shall avoid any damage to the device in case the current flows from the output to the input and the input source cannot sink current e.g. a diode in the supply path. If the converter forced PWM mode is active the current can go negative until to the sink current limit. Once the input voltage threshold $V_{T+(IVP)}$ is reach on the VIN-pin the protection disables the forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, the fPWM mode can be activated again.

The threshold for the $V_{T+(IVP)}$ is programmable via the V_IVP register field and can be disabled through the EN_IVP bit.

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8.3.22.6 Input Voltage Regulation (IVR)

The input over voltage protection the IVR regulates the input voltage using the current monitor block. The threshold for the target voltage is programmed by the V_IVP register. The IVR function is enabled once EN_IVP and EN_IVR set to 0b1. The fPWM need to be enabled the reverse current to charge the input. If Mode pin is pulled low the IVR operation is paused until the fPWM is enabled again.

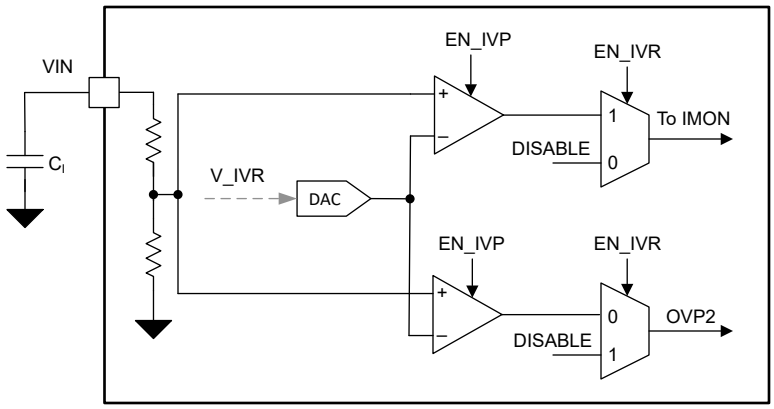

図 8-28. Functional Block Diagram IVP/IVR

8.3.22.7 Power Good

The device features a power good detection. The internal PG signal is used for the monitoring function.

As during soft-start the signal for the PG is not available the power good function is no available during this state.

8.3.22.8 Boot-Strap Under Voltage Protection

The high side supply voltage for the gate driver and as well for the are monitored by an additional boot strap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. This protection supports the two modes in the following manner.

1. If the measured voltage drops below $V_{TH-(BST\_UV)}$ in fPWM mode the converter stops operation after a trimmed amount of switching cycles.
2. In PSM i.e. 2 switching phase buck-boost operation, the BOOT_UV triggers switching of the converter to re-fresh the boot strap voltage. If the initiated switching does not bring up the BOOT_UV after the trimmed amount of re-fresh cycles the fPWM protection deactivates the converter operation.

8.3.22.9 Boot-strap Over Voltage Clamp

To protect the ext. FET gate and the internal gate drive circuit the charge sharing circuit of the gate driver features an over voltage clamp. If the voltage goes above $V_{TH(BST\_OV)}$ the linear regulator from the boot strap charge sharing sinks a current from HBx to SWx as long as the voltage is above the threshold.

8.3.22.10 CRC - CHECK

To ensure data integrity of the NVM the device features a CRC- algorithm to generate a check-sum for the data stored in the device NVM.

The check-sum gets generated and stored to the separate NVM register automatically with the OTP programming process.

After the NVM boot phase the CRC algorithm compares the check-sum of the loaded registers with the check-sum stored in the NVM register generated during the production tests. If the two values is not equal to device is not allowed to exit the CONV_OFF state.

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8.4 Device Functional Modes

8.4.1 Overview

The device contains a digital logic core that controls the functional behavior. The logic and internal oscillator are turned off to save current in case no interrupt of a converter internal signal occurs.

8.4.2 Logic State Description

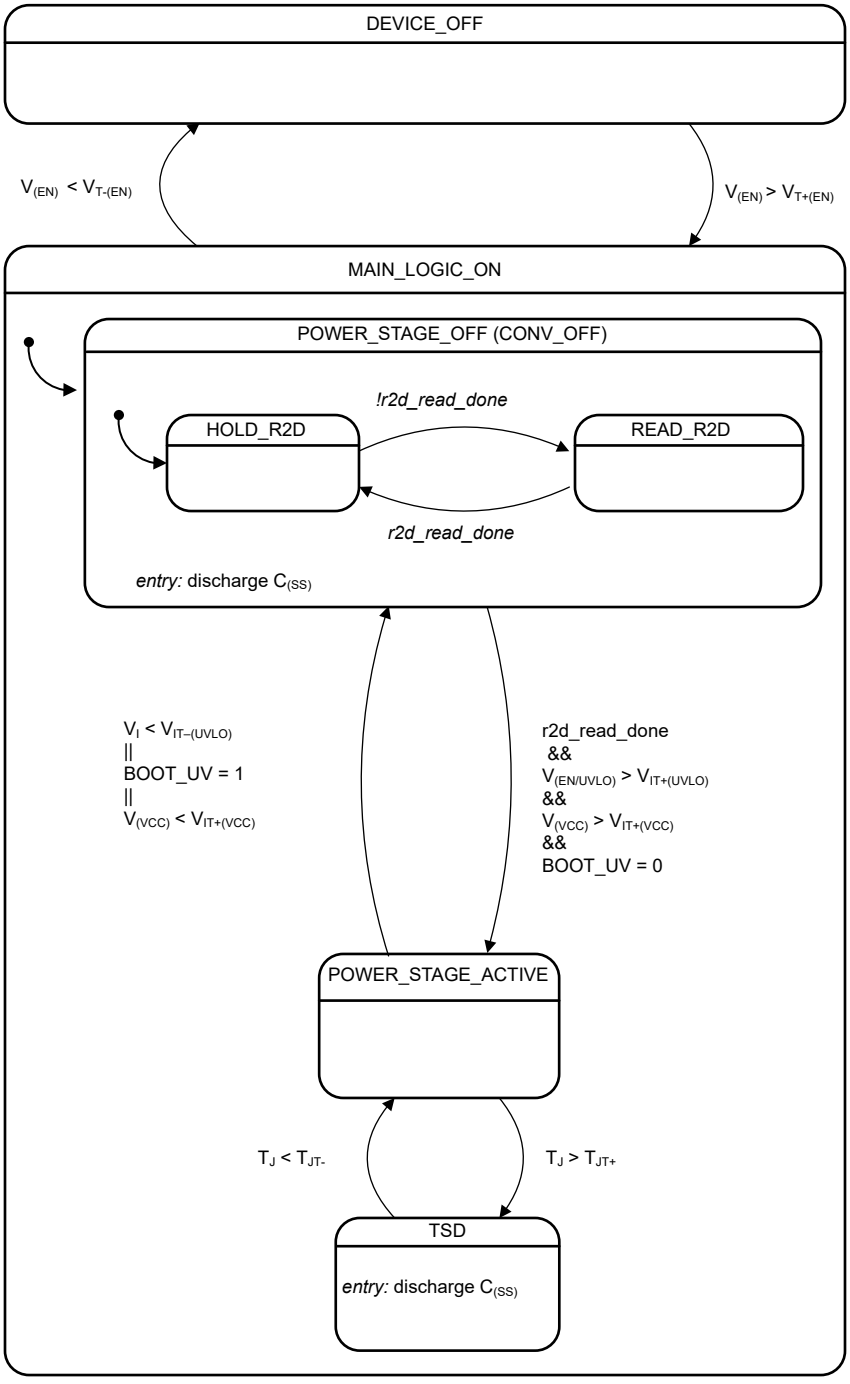

図 8-29. State Diagram

8.5 Programming

8.5.1 I²C Bus Operation

The I 2 C bus is a communications link between a controller and a series of target devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the target terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission. The device hosts a target I 2 C interface that supports standard-mode, fast-mode and fast-mode plus operation with data rates up to 100 kbit/s, 400 kbit/s and 1000 kbit/s respectively and auto-increment addressing compatible to I 2 C standard 3.0.

The 7 bit target address of this device is 0x6A if the ADDR/SLOPE pin I pulled to GND and 0x6B if the pin is connected to VCC2

Data transmission is initiated with a start bit from the controller as shown in the figure below . The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the target address bits are set for the device, then the device issues an acknowledge pulse and prepares the receive of register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I 2 C interfaces will auto-sequence through register addresses, so that multiple data words can be sent for a given I 2 C transmission.

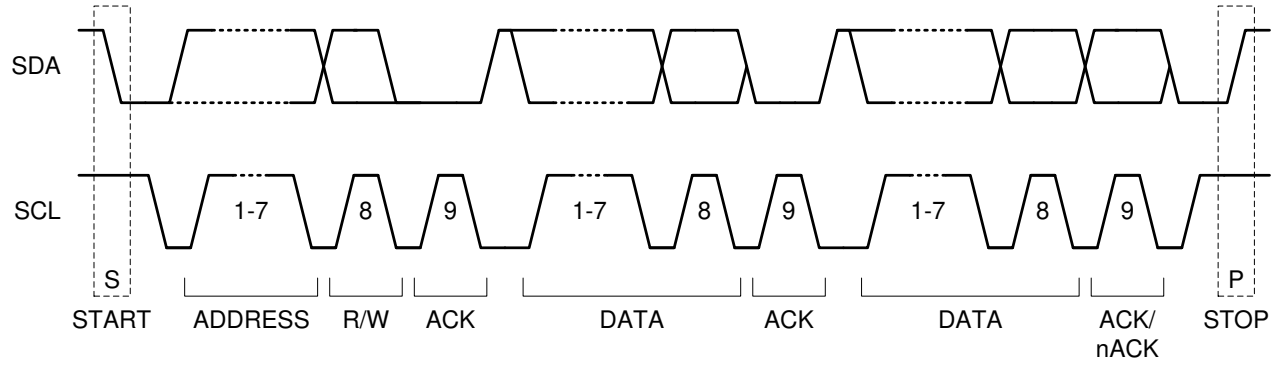

図 8-30. I 2 C START / STOP / ACKNOWLEDGE Protocol

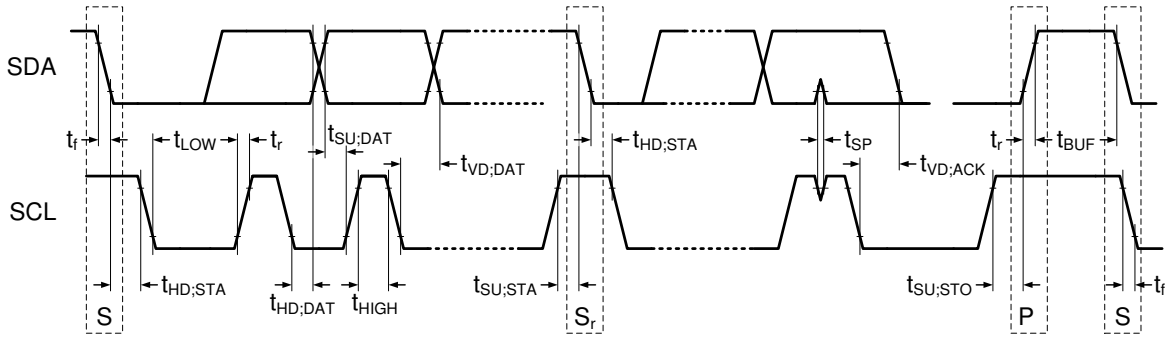

図 8-31. I 2 C Data Transmission Timing

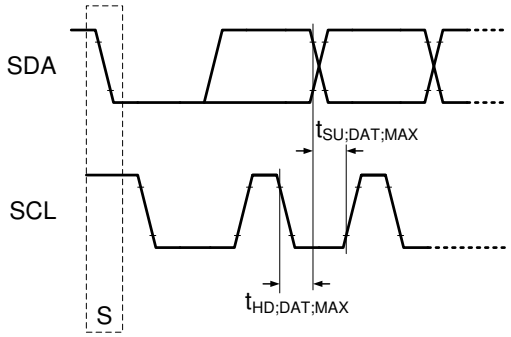

図 8-32. I 2 C Data Transmission Timing for maximum rise/fall times.

8.5.2 Clock Stretching

Clock stretching is not supported. If the device is addressed while busy and not able to process the received data, it does not acknowledge the transaction. This may happen if the controller initiates an I2C transaction while the device is in BOOT state.

8.5.3 Data Transfer Formats

The device supports four different read/write operations:

- Single read from a defined register address.
- Single write to a defined register address.
- Sequential read starting from a defined register address
- Sequential write starting from a defined register address

8.5.4 Single READ from a Defined Register Address

Single READ from a defined register address shows the format of a single read from a defined register address. First, the controller issues a start condition followed by a seven-bit I 2 C address. Next, the controller writes a zero to signify that it conducts a write operation. Upon receiving an acknowledge from the target the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the internal I 2 C register number to the defined value. Then the controller issues a repeat start condition and the seven-bit I 2 C address followed by a one to signify that it conducts a read operation. Upon receiving a third acknowledge, the controller releases the bus to the device. The device then returns the eight-bit data value from the register on the bus. The controller does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

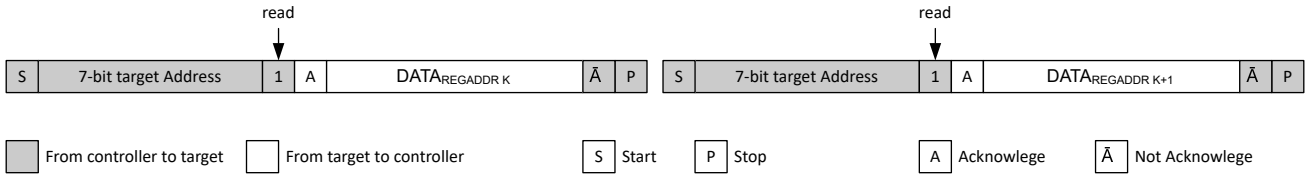

図 8-33. Single READ from a defined register address

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8.5.5 Sequential READ Starting from a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Sequential READ starting from a defined register address . The controller acknowledges the reception of a data byte, the device auto increments the register address and returns the data from the next register. The data transfer is stopped by the controller not acknowledging the last data byte and sending a stop condition.

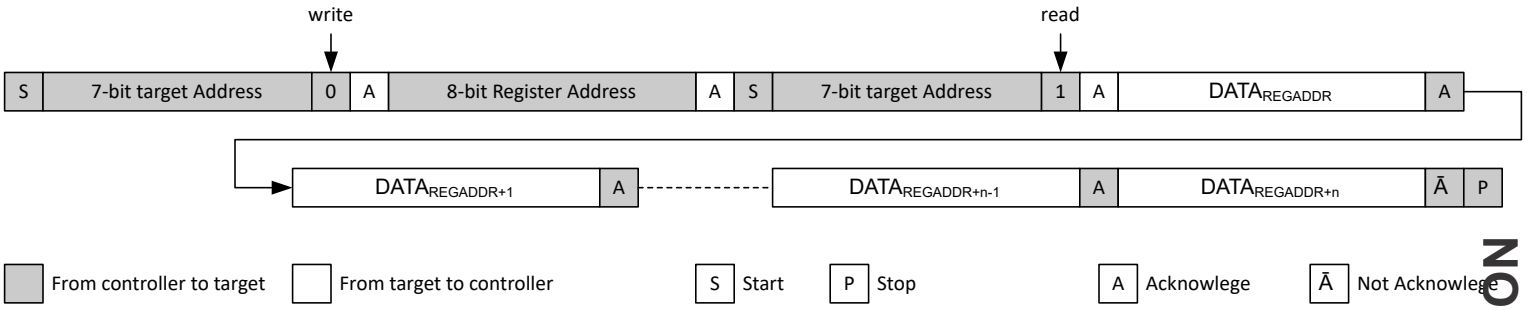

図 8-34. Sequential READ starting from a defined register address

8.5.6 Single WRITE to a Defined Register Address

Single WRITE to defined register address shows the format of a single write to a defined register address. First, the controller issues a start condition followed by a seven-bit I ^{2} C address. Next, the controller writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the target, the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the I ^{2} C register address to the defined value and the controller writes the eight-bit data value. Upon receiving a third acknowledge the device auto increments the I ^{2} C register address by one and the controller issues a stop condition. This action concludes the register write.

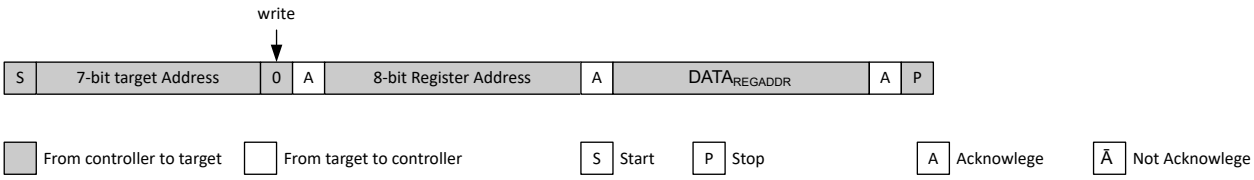

図 8-35. Single WRITE to defined register address

8.5.7 Sequential WRITE Starting at a Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Sequential WRITE starting at a defined register address . If the controller doesn't send a stop condition after the device has issued an ACK, the device auto increments the register address by one and the controller can write to the next register.

ADVANCE INFORMATION

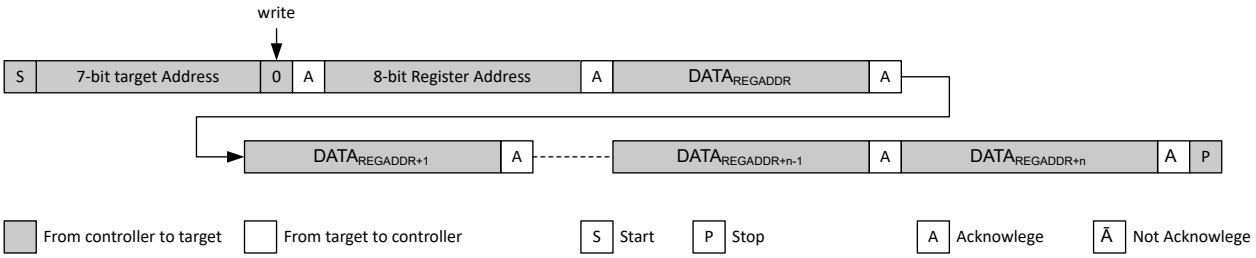

図 8-36. Sequential WRITE starting at a defined register address

ADVANCE INFORMATION

9 LM51772 Registers

表 9-1 lists the memory-mapped registers for the LM51772 registers. All register offset addresses not listed in 表 9-1 should be considered as reserved locations and the register contents should not be modified.

表 9-1. LM51772 Registers

Address	Acronym	Register Name	Section
0x3	CLEAR_FAULTS	CLEAR_FAULTS	Go
0xA	ILIM_THRESHOLD	ILIM_THRESHOLD	Go
0xC	VOUT_TARGET1_LSB	VOUT_TARGET1_LSB	Go
0xD	VOUT_TARGET1_MSB	VOUT_TARGET1_MSB	Go
0x21	USB_PD_STATUS_0	USB_PD_STATUS_0	Go
0x78	STATUS_BYTE	STATUS_BYTE	Go
0x81	USB_PD_CONTROL_0	USB_PD_CONTROL_0	Go
0xD0	MFR_SPECIFIC_D0	MFR_SPECIFIC_D0	Go
0xD1	MFR_SPECIFIC_D1	MFR_SPECIFIC_D1	Go
0xD2	MFR_SPECIFIC_D2	MFR_SPECIFIC_D2	Go
0xD3	MFR_SPECIFIC_D3	MFR_SPECIFIC_D3	Go
0xD4	MFR_SPECIFIC_D4	MFR_SPECIFIC_D4	Go
0xD5	MFR_SPECIFIC_D5	MFR_SPECIFIC_D5	Go
0xD6	MFR_SPECIFIC_D6	MFR_SPECIFIC_D6	Go
0xD7	MFR_SPECIFIC_D7	MFR_SPECIFIC_D7	Go
0xD8	MFR_SPECIFIC_D8	MFR_SPECIFIC_D8	Go
0xD9	MFR_SPECIFIC_D9	MFR_SPECIFIC_D9	Go
0xDA	IVP_VOLTAGE	IVP_VOLTAGE	Go

Complex bit access types are encoded to fit into small table cells. 表 9-2 shows the codes that are used for access types in this section.

表 9-2. LM51772 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

9.1 CLEAR_FAULTS Register (Address = 0x3) [Reset = 0x00]

CLEAR_FAULTS is shown in 表 9-3.

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clear all latched status flags

表 9-3. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLEAR_FAULTS	R	0x0	accessing the address is enough to clear fault

9.2 ILIM_THRESHOLD Register (Address = 0xA) [Reset = 0x64]

ILIM_THRESHOLD is shown in 表 9-4.

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表 9-4. ILIM_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ILIM_THRESHOLD	R/W	0x64	ISNS current limit threshold voltage. Value in bracket considers a 10mOhms sens resistor 0x0 = 5mV (0.5 A) 0x1 = 5mV (0.5 A) 0x2 = 5mV (0.5 A) 0x3 = 5mV (0.5 A) 0x4 = 5mV (0.5 A) 0x5 = 5mV (0.5 A) 0x6 = 5mV (0.5 A) 0x7 = 5mV (0.5 A) 0x8 = 5mV (0.5 A) 0x9 = 5mV (0.5 A) 0xA = 5mV (0.5 A) 0xB = 5.5mV (0.55 A) 0xC = 6mV (0.6 A) 0xD = 6.5mV (0.65 A) 0xE = 7mV (0.7 A) 0xF = 7.5mV (0.75 A) 0x10 = 8mV (0.8 A) 0x11 = 8.5mV (0.85 A) 0x12 = 9mV (0.9 A) 0x13 = 9.5mV (0.95 A) 0x14 = 10mV (1 A) 0x15 = 10.5mV (1.05 A) 0x16 = 11mV (1.1 A) 0x17 = 11.5mV (1.15 A) 0x18 = 12mV (1.2 A) 0x19 = 12.5mV (1.25 A) 0x1A = 13mV (1.3 A) 0x1B = 13.5mV (1.35 A) 0x1C = 14mV (1.4 A) 0x1D = 14.5mV (1.45 A) 0x1E = 15mV (1.5 A) 0x1F = 15.5mV (1.55 A) 0x20 = 16mV (1.6 A) 0x21 = 16.5mV (1.65 A) 0x22 = 17mV (1.7 A) 0x23 = 17.5mV (1.75 A) 0x24 = 18mV (1.8 A) 0x25 = 18.5mV (1.85 A) 0x26 = 19mV (1.9 A) 0x27 = 19.5mV (1.95 A) 0x28 = 20mV (2 A) 0x29 = 20.5mV (2.05 A) 0x2A = 21mV (2.1 A) 0x2B = 21.5mV (2.15 A) 0x2C = 22mV (2.2 A) 0x2D = 22.5mV (2.25 A) 0x2E = 23mV (2.3 A) 0x2F = 23.5mV (2.35 A) 0x30 = 24mV (2.4 A) 0x31 = 24.5mV (2.45 A) 0x32 = 25mV (2.5 A) 0x33 = 25.5mV (2.55 A) 0x34 = 26mV (2.6 A) 0x35 = 26.5mV (2.65 A) 0x36 = 27mV (2.7 A) 0x37 = 27.5mV (2.75 A) 0x38 = 28mV (2.8 A) 0x39 = 28.5mV (2.85 A) 0x3A = 29mV (2.9 A) 0x3B = 29.5mV (2.95 A) 0x3C = 30mV (3 A) 0x3D = 30.5mV (3.05 A) 0x3E = 31mV (3.1 A)

表 9-4. ILIM_THRESHOLD Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0x3F = 31.5mV (3.15 A) 0x40 = 32mV (3.2 A) 0x41 = 32.5mV (3.25 A) 0x42 = 33mV (3.3 A) 0x43 = 33.5mV (3.35 A) 0x44 = 34mV (3.4 A) 0x45 = 34.5mV (3.45 A) 0x46 = 35mV (3.5 A) 0x47 = 35.5mV (3.55 A) 0x48 = 36mV (3.6 A) 0x49 = 36.5mV (3.65 A) 0x4A = 37mV (3.7 A) 0x4B = 37.5mV (3.75 A) 0x4C = 38mV (3.8 A) 0x4D = 38.5mV (3.85 A) 0x4E = 39mV (3.9 A) 0x4F = 39.5mV (3.95 A) 0x50 = 40mV (4 A) 0x51 = 40.5mV (4.05 A) 0x52 = 41mV (4.1 A) 0x53 = 41.5mV (4.15 A) 0x54 = 42mV (4.2 A) 0x55 = 42.5mV (4.25 A) 0x56 = 43mV (4.3 A) 0x57 = 43.5mV (4.35 A) 0x58 = 44mV (4.4 A) 0x59 = 44.5mV (4.45 A) 0x5A = 45mV (4.5 A) 0x5B = 45.5mV (4.55 A) 0x5C = 46mV (4.6 A) 0x5D = 46.5mV (4.65 A) 0x5E = 47mV (4.7 A) 0x5F = 47.5mV (4.75 A) 0x60 = 48mV (4.8 A) 0x61 = 48.5mV (4.85 A) 0x62 = 49mV (4.9 A) 0x63 = 49.5mV (4.95 A) 0x64 = **50mV (5 A)** 0x65 = 50.5mV (5.05 A) 0x66 = 51mV (5.1 A) 0x67 = 51.5mV (5.15 A) 0x68 = 52mV (5.2 A) 0x69 = 52.5mV (5.25 A) 0x6A = 53mV (5.3 A) 0x6B = 53.5mV (5.35 A) 0x6C = 54mV (5.4 A) 0x6D = 54.5mV (5.45 A) 0x6E = 55mV (5.5 A) 0x6F = 55.5mV (5.55 A) 0x70 = 56mV (5.6 A) 0x71 = 56.5mV (5.65 A) 0x72 = 57mV (5.7 A) 0x73 = 57.5mV (5.75 A) 0x74 = 58mV (5.8 A) 0x75 = 58.5mV (5.85 A) 0x76 = 59mV (5.9 A) 0x77 = 59.5mV (5.95 A) 0x78 = 60mV (6 A) 0x79 = 60.5mV (6.05 A) 0x7A = 61mV (6.1 A) 0x7B = 61.5mV (6.15 A) 0x7C = 62mV (6.2 A) 0x7D = 62.5mV (6.25 A) 0x7E = 63mV (6.3 A) 0x7F = 63.5mV (6.35 A)

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表 9-4. ILIM_THRESHOLD Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0x80 = 64mV (6.4 A) 0x81 = 64.5mV (6.45 A) 0x82 = 65mV (6.5 A) 0x83 = 65.5mV (6.55 A) 0x84 = 66mV (6.6 A) 0x85 = 66.5mV (6.65 A) 0x86 = 67mV (6.7 A) 0x87 = 67.5mV (6.75 A) 0x88 = 68mV (6.8 A) 0x89 = 68.5mV (6.85 A) 0x8A = 69mV (6.9 A) 0x8B = 69.5mV (6.95 A) 0x8C = 70mV (7 A) 0x8D = 70mV (7 A) 0x8E = 70mV (7 A) 0x8F = 70mV (7 A) 0x90 = 70mV (7 A) 0x91 = 70mV (7 A) 0x92 = 70mV (7 A) 0x93 = 70mV (7 A) 0x94 = 70mV (7 A) 0x95 = 70mV (7 A) 0x96 = 70mV (7 A) 0x97 = 70mV (7 A) 0x98 = 70mV (7 A) 0x99 = 70mV (7 A) 0x9A = 70mV (7 A) 0x9B = 70mV (7 A) 0x9C = 70mV (7 A) 0x9D = 70mV (7 A) 0x9E = 70mV (7 A) 0x9F = 70mV (7 A) 0xA0 = 70mV (7 A) 0xA1 = 70mV (7 A) 0xA2 = 70mV (7 A) 0xA3 = 70mV (7 A) 0xA4 = 70mV (7 A) 0xA5 = 70mV (7 A) 0xA6 = 70mV (7 A) 0xA7 = 70mV (7 A) 0xA8 = 70mV (7 A) 0xA9 = 70mV (7 A) 0xAA = 70mV (7 A) 0xAB = 70mV (7 A) 0xAC = 70mV (7 A) 0xAD = 70mV (7 A) 0xAE = 70mV (7 A) 0xAF = 70mV (7 A) 0xB0 = 70mV (7 A) 0xB1 = 70mV (7 A) 0xB2 = 70mV (7 A) 0xB3 = 70mV (7 A) 0xB4 = 70mV (7 A) 0xB5 = 70mV (7 A) 0xB6 = 70mV (7 A) 0xB7 = 70mV (7 A) 0xB8 = 70mV (7 A) 0xB9 = 70mV (7 A) 0xBA = 70mV (7 A) 0xBB = 70mV (7 A) 0xBC = 70mV (7 A) 0xBD = 70mV (7 A) 0xBE = 70mV (7 A) 0xBF = 70mV (7 A) 0xC0 = 70mV (7 A)

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表 9-4. ILIM_THRESHOLD Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0xC1 = 70mV (7 A) 0xC2 = 70mV (7 A) 0xC3 = 70mV (7 A) 0xC4 = 70mV (7 A) 0xC5 = 70mV (7 A) 0xC6 = 70mV (7 A) 0xC7 = 70mV (7 A) 0xC8 = 70mV (7 A) 0xC9 = 70mV (7 A) 0xCA = 70mV (7 A) 0xCB = 70mV (7 A) 0xCC = 70mV (7 A) 0xCD = 70mV (7 A) 0xCE = 70mV (7 A) 0xCF = 70mV (7 A) 0xD0 = 70mV (7 A) 0xD1 = 70mV (7 A) 0xD2 = 70mV (7 A) 0xD3 = 70mV (7 A) 0xD4 = 70mV (7 A) 0xD5 = 70mV (7 A) 0xD6 = 70mV (7 A) 0xD7 = 70mV (7 A) 0xD8 = 70mV (7 A) 0xD9 = 70mV (7 A) 0xDA = 70mV (7 A) 0xDB = 70mV (7 A) 0xDC = 70mV (7 A) 0xDD = 70mV (7 A) 0xDE = 70mV (7 A) 0xDF = 70mV (7 A) 0xE0 = 70mV (7 A) 0xE1 = 70mV (7 A) 0xE2 = 70mV (7 A) 0xE3 = 70mV (7 A) 0xE4 = 70mV (7 A) 0xE5 = 70mV (7 A) 0xE6 = 70mV (7 A) 0xE7 = 70mV (7 A) 0xE8 = 70mV (7 A) 0xE9 = 70mV (7 A) 0xEA = 70mV (7 A) 0xEB = 70mV (7 A) 0xEC = 70mV (7 A) 0xED = 70mV (7 A) 0xEE = 70mV (7 A) 0xEF = 70mV (7 A) 0xF0 = 70mV (7 A) 0xF1 = 70mV (7 A) 0xF2 = 70mV (7 A) 0xF3 = 70mV (7 A) 0xF4 = 70mV (7 A) 0xF5 = 70mV (7 A) 0xF6 = 70mV (7 A) 0xF7 = 70mV (7 A) 0xF8 = 70mV (7 A) 0xF9 = 70mV (7 A) 0xFA = 70mV (7 A) 0xFB = 70mV (7 A) 0xFC = 70mV (7 A) 0xFD = 70mV (7 A) 0xFE = 70mV (7 A) 0xFF = 70mV (7 A)

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9.3 VOUT_TARGET1_LSB Register (Address = 0xC) [Reset = 0x58]

VOUT_TARGET1_LSB is shown in 表 9-5.

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表 9-5. VOUT_TARGET1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_A	R/W	0x58	Output target Voltage Logical Register Vout Setting Lower Limit: 3.3V Upper Limit: 48 V Step size: 20 mV or 10 mV depending on セクション 9.16 Value Calculation for 20mV 表 9-18 Value Calculation for 10mV 表 9-18

9.4 VOUT_TARGET1_MSB Register (Address = 0xD) [Reset = 0x02]

VOUT_TARGET1_MSB is shown in 表 9-6.

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表 9-6. VOUT_TARGET1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
3:0	VOUT_A	R/W	0x2	Output target Voltage Logical Register Vout Setting Lower Limit: 3.3V Upper Limit: 48 V Step size: 20 mV or 10 mV depending on MFR_SPECIFIC_D8 Register (Address = 0xD8) [Reset = 0x84] Value Calculation for 20mV 表 9-18 Value Calculation for 10mV 表 9-18

ADVANCE INFORMATION

9.5 USB_PD_STATUS_0 Register (Address = 0x21) [Reset = 0x00]

USB_PD_STATUS_0 is shown in 表 9-7.

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USB-PD STATUS REGISTER

表 9-7. USB_PD_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	CC_OPERATION	R	0x0	Instantanous status for constant current (CC) ILIM operation
5:0	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.

9.6 STATUS_BYTE Register (Address = 0x78) [Reset = 0x00]

STATUS_BYTE is shown in 表 9-8.

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FAULT STATUS LOW BYTE

表 9-8. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0x0	unit is busy 0x0 = **unit not busy** 0x1 = unit busy
6	OFF	R	0x0	device not providing VOUT and/or unit is off 0x0 = **unit on** 0x1 = unit off
5	VOUT	R	0x0	VOUT_OV fault 0x0 = **no fault** 0x1 = fault
4	IOUT	R	0x0	IOUT_OC fault 0x0 = **no fault** 0x1 = fault
3	INPUT	R	0x0	VIN_UV fault 0x0 = **no fault** 0x1 = fault
2	TEMPERATURE	R	0x0	Temperature fault or warning 0x0 = **no fault** 0x1 = fault
1	CML	R	0x0	Comm, Logic, Memory event 0x0 = **no fault** 0x1 = fault
0	OTHER	R	0x0	other fault or warning 0x0 = **no fault** 0x1 = fault

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9.7 USB_PD_CONTROL_0 Register (Address = 0x81) [Reset = 0x01]

USB_PD_CONTROL_0 is shown in 表 9-9.

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USB-PD CONTROL REGISTER

表 9-9. USB_PD_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
1	FORCE_DISCH	R/W	0x0	Activates Vo discharge 0x0 = **DISABLE** 0x1 = ENABLE
0	CONV_EN2	R/W	0x1	Enables the power stage 0x0 = DISABLE 0x1 = **ENABLE**

9.8 MFR_SPECIFIC_D0 Register (Address = 0xD0) [Reset = 0x32]

MFR_SPECIFIC_D0 is shown in 表 9-10.

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CONFIG_0 Device Configuration Register 0

表 9-10. MFR_SPECIFIC_D0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	EN_NEG_CL_LIMIT	R/W	0x0	Enables ILIM for negative current limit, If disabled ILIM clamps pos I_L 0x0 = **DISABLE** 0x1 = ENABLE
5	EN_VCC1	R/W	0x1	Enables the VCC1 auxiliary LDO 0x0 = DISABLE 0x1 = **ENABLE**
4	IMON_LIMITER_EN	R/W	0x1	Enables the Imon in limiter configuration 0x0 = DISABLE 0x1 = **ENABLE**
3	HICCUP_EN	R/W	0x0	Enables Hiccup short circuit 0x0 = **DISABLE** 0x1 = ENABLE
2	DRSS_EN	R/W	0x0	Enables Dual Spread Spectrum 0x0 = **DISABLE** 0x1 = ENABLE
1	USLEEP_EN	R/W	0x1	Enables micro sleep mode 0x0 = DISABLE 0x1 = **ENABLE**
0	CONV_EN	R/W	0x0	Enables the power stage 0x0 = **DISABLE** 0x1 = ENABLE

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9.9 MFR_SPECIFIC_D1 Register (Address = 0xD1) [Reset = 0x09]

MFR_SPECIFIC_D1 is shown in 表 9-11.

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CONFIG_1 Device Configuration Register 1

表 9-11. MFR_SPECIFIC_D1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_THER_WARN	R/W	0x0	Enables Thermal Warning 0x0 = **DISABLE** 0x1 = ENABLE
6:5	THW_THRESHOLD	R/W	0x0	Selects the Thermal Warning Threshold 0x0 = **140degC** 0x1 = 125degC 0x2 = 110degC 0x3 = 95degC
4	EN_NINT	R/W	0x0	Conigures the nFLT pin handler to act as interupt pin or nFLT pin 0x0 = **DISABLE** 0x1 = ENABLE
3	EN_DTRK_STARTOVER	R/W	0x1	Enables a direct start-up if DTRK is enabled without waiting for the DTRK PWM signal 0x0 = DISABLE 0x1 = **ENABLE**
2	FORCE_BIASPIN	R/W	0x0	Enables the priroty to supply VCC2 from BIAS by lowering the threshold. 0x0 = **DISABLE** 0x1 = ENABLE
1	EN_BB_2P_FPWM	R/W	0x0	Enables 2phase BB swiching in fPWM mode 0x0 = **DISABLE** 0x1 = ENABLE
0	EN_BB_2P_PSM	R/W	0x1	Enables 2phase BB swiching in PSM mode 0x0 = DISABLE 0x1 = **ENABLE**

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9.10 MFR_SPECIFIC_D2 Register (Address = 0xD2) [Reset = 0x40]

MFR_SPECIFIC_D2 is shown in 表 9-12.

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表 9-12. MFR_SPECIFIC_D2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
6	EN_ACTIVE_DVS	R/W	0x1	Enables the active down ramp for DVS using the discharge 0x0 = DISABLE 0x1 = **ENABLE**
5:4	DVS_SLEW_RAMP	R/W	0x0	Sets the positive and negative Vo slew rate for DVS 0x0 = **40mV/us** 0x1 = 20mV/us 0x2 = 1mV/us 0x3 = 0.5mV/us
3:2	DISCHARGE_STRENGTH	R/W	0x0	Sets the discharge current for the Vo discharge 0x0 = **SLOW (25mA)** 0x1 = MEDIUM (50mA) 0x2 = FAST (75mA) 0x3 = FAST (75mA)
1	DISCHARGE_CONFIG0	R/W	0x0	Selects the discharge together with CONV_EN 0x0 = **DISABLE** 0x1 = ENABLE
0	DISCHARGE_CONFIG1	R/W	0x0	Selects the discharge until the VTH DISCH 0x0 = **DISABLE** 0x1 = ENABLE

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9.11 MFR_SPECIFIC_D3 Register (Address = 0xD3) [Reset = 0x20]

MFR_SPECIFIC_D3 is shown in 表 9-13.

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表 9-13. MFR_SPECIFIC_D3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_IVP	R/W	0x0	Enabled input voltage protection. 0x0 = **DISABLE** 0x1 = ENABLE
6	SEL_IVR	R/W	0x0	Selected input voltage regulation instead of the input voltage protection. 0x0 = **DISABLE** 0x1 = ENABLE
5	VDET_EN	R/W	0x1	Enables internal VDET function 0x0 = DISABLE 0x1 = **ENABLE**
4:0	VDET_FALL	R/W	0x0	VDET falling threshold 0x0 = **2.7V** 0x1 = 2.9V 0x2 = 3.1V 0x3 = 3.3V 0x4 = 3.5V 0x5 = 3.7V 0x6 = 3.9V 0x7 = 4.1V 0x8 = 4.3V 0x9 = 4.5V 0xA = 4.7V 0xB = 4.9V 0xC = 5.1V 0xD = 5.3V 0xE = 5.5V 0xF = 5.7V 0x10 = 5.9V 0x11 = 6.1V 0x12 = 6.3V 0x13 = 6.5V 0x14 = 6.7V 0x15 = 6.9V 0x16 = 7.1V 0x17 = 7.3V 0x18 = 7.5V 0x19 = 7.7V 0x1A = 7.9V 0x1B = 8.1V 0x1C = 8.3V 0x1D = 8.5V 0x1E = 8.7V 0x1F = 8.9V

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9.12 MFR_SPECIFIC_D4 Register (Address = 0xD4) [Reset = 0x03]

MFR_SPECIFIC_D4 is shown in 表 9-14.

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表 9-14. MFR_SPECIFIC_D4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
4:0	VDET_RISE	R/W	0x3	VDET rising threshold 0x0 = 2.8V 0x1 = 3V 0x2 = 3.2V 0x3 = **3.4V** 0x4 = 3.6V 0x5 = 3.8V 0x6 = 4V 0x7 = 4.2V 0x8 = 4.4V 0x9 = 4.6V 0xA = 4.8V 0xB = 5V 0xC = 5.2V 0xD = 5.4V 0xE = 5.6V 0xF = 5.8V 0x10 = 6V 0x11 = 6.2V 0x12 = 6.4V 0x13 = 6.6V 0x14 = 6.8V 0x15 = 7V 0x16 = 7.2V 0x17 = 7.4V 0x18 = 7.6V 0x19 = 7.8V 0x1A = 8V 0x1B = 8.2V 0x1C = 8.4V 0x1D = 8.6V 0x1E = 8.8V 0x1F = 9V

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9.13 MFR_SPECIFIC_D5 Register (Address = 0xD5) [Reset = 0x3F]

MFR_SPECIFIC_D5 is shown in 表 9-15.

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表 9-15. MFR_SPECIFIC_D5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.

表 9-15. MFR_SPECIFIC_D5 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5:0	V_OVP2	R/W	0x3F	OVP2 threshold voltage 0x0 = 4.00V 0x1 = 4.500V 0x2 = 5.000V 0x3 = 5.500V 0x4 = 6.000V 0x5 = 6.500V 0x6 = 7.000V 0x7 = 7.500V 0x8 = 8.000V 0x9 = 8.500V 0xA = 9.000V 0xB = 9.500V 0xC = 10.000V 0xD = 10.500V 0xE = 11.000V 0xF = 11.500V 0x10 = 12.000V 0x11 = 12.500V 0x12 = 13.000V 0x13 = 13.500V 0x14 = 14.000V 0x15 = 14.500V 0x16 = 15.000V 0x17 = 15.500V 0x18 = 16.000V 0x19 = 17.000V 0x1A = 18.000V 0x1B = 19.000V 0x1C = 20.000V 0x1D = 21.000V 0x1E = 22.000V 0x1F = 23.000V 0x20 = 24.000V 0x21 = 25.000V 0x22 = 26.000V 0x23 = 27.000V 0x24 = 28.000V 0x25 = 29.000V 0x26 = 30.000V 0x27 = 31.000V 0x28 = 32.000V 0x29 = 33.000V 0x2A = 34.000V 0x2B = 35.000V 0x2C = 36.000V 0x2D = 37.000V 0x2E = 38.000V 0x2F = 39.000V 0x30 = 40.000V 0x31 = 41.000V 0x32 = 42.000V 0x33 = 43.000V 0x34 = 44.000V 0x35 = 45.000V 0x36 = 46.000V 0x37 = 47.000V 0x38 = 48.000V 0x39 = 49.000V 0x3A = 50.000V 0x3B = 51.000V 0x3C = 52.000V 0x3D = 53.000V 0x3E = 54.000V

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表 9-15. MFR_SPECIFIC_D5 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0x3F = **55.000V**

9.14 MFR_SPECIFIC_D6 Register (Address = 0xD6) [Reset = 0x15]

MFR_SPECIFIC_D6 is shown in 表 9-16.

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PS_Config0 Power stage Configuration

表 9-16. MFR_SPECIFIC_D6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CONFIG_SYNC_PIN	R/W	0x0	Selects the SYNC function to mainain paralell operation 0x0 = **Input sync on rising edge** 0x1 = Input sync on falling edge 0x2 = Sync output from internal rising edge 0x3 = Sync output from internal falling edge (180deg phase)
5	EN_CONST_TDEAD	R/W	0x0	Forces a constant deadtime for the setting of SEL_MIN_DEADTIME_GDRV. Disables frequnecy dependency of min Tdead 0x0 = **DISABLE** 0x1 = ENABLE
4	SEL_SCALE_DT	R/W	0x1	Scales the gate driver dead time freq dependence and 2 MHz setpoint 0x0 = DISABLE 0x1 = **ENABLE**
3:2	SEL_MIN_DEADTIME_GDRV	R/W	0x1	Defines the minimum dead time at fsw = 2Mhz for the gate driver 0x0 = 10 ns (No delay) 0x1 = **20 ns** 0x2 = 40 ns 0x3 = 60 ns
1:0	BB_MIN_TIME_OFFSET	R/W	0x1	Scales the BB min Ton or Toff time for the gate refresh 0x0 = 0.75 x 0x1 = **1 x** 0x2 = 1.25 x 0x3 = 1.5 x

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9.15 MFR_SPECIFIC_D7 Register (Address = 0xD7) [Reset = 0x36]

MFR_SPECIFIC_D7 is shown in 表 9-17.

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表 9-17. MFR_SPECIFIC_D7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
5:4	SEL_INDUC_DERATE	R/W	0x3	Select the inductor de-rating for PSM mode to slope 0x0 = DISABLE 0x1 = 10% 0x2 = 20% 0x3 = **30%**
3:0	SEL_SLOPE_COMP	R/W	0x6	Select slope comp current, as ratio of RT current 0x0 = 0.125 0x1 = 0.25 0x2 = 0.375 0x3 = 0.5 0x4 = 0.625 0x5 = 0.75 0x6 = **0.875** 0x7 = 1 0x8 = 1.5 0x9 = 2 0xA = 2.5 0xB = 3 0xC = 3.5 0xD = 4 0xE = 4.5 0xF = 5

9.16 MFR_SPECIFIC_D8 Register (Address = 0xD8) [Reset = 0x84]

MFR_SPECIFIC_D8 is shown in 表 9-18.

Return to the Summary Table.

表 9-18. MFR_SPECIFIC_D8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_FB_DIV20	R/W	0x1	Select internal FB divider ratio of 20 0x0 = DIV10 0x1 = **DIV20**
6	EN_CDC	R/W	0x0	Enables the cable drop compensation 0x0 = **DISABLE** 0x1 = ENABLE
5:4	CDC_GAIN	R/W	0x0	Selectes the Gain for the CDC voltage (1V) with respect to Vout 0x0 = **0.250V** 0x1 = 0.500V 0x2 = 1.000V 0x3 = 2.000V
3:2	SEL_DRV1_SEQ	R/W	0x1	Select the sequencing for the DRV 1 operation 0x0 = Pull-Low/ CP running if converter operation is off 0x1 = **Pull-Low/ CP running if converter operation is on** 0x2 = FORCE ACTIVE 0x3 = FORCE OFF
1:0	SEL_DRV1_SUP	R/W	0x0	Select the driver configuration for DRV1 pin 0x0 = **Open Drain (active = pull low)** 0x1 = Vout 0x2 = VBIAS 0x3 = VCC2 (Charge Pump driver)

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9.17 MFR_SPECIFIC_D9 Register (Address = 0xD9) [Reset = 0x2C]

MFR_SPECIFIC_D9 is shown in 表 9-19.

Return to the Summary Table.

表 9-19. MFR_SPECIFIC_D9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NIL	R	0x0	This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations 0 is returned.
5	SEL_ISET_PIN	R/W	0x1	Forces the ISET pin in I2C active config and disables the ILIM DAC. 0x0 = DISABLE 0x1 = **ENABLE**
4:0	PCM_WINDOW_LOW	R/W	0xC	Select the lower voltage window threshold refered to VOUT for the PCM 0x0 = 0 (Disable)% 0x1 = 2.50% 0x2 = 5% 0x3 = 7.5% 0x4 = 10% 0x5 = 12.5% 0x6 = 15% 0x7 = 17.5% 0x8 = 20% 0x9 = 22.5% 0xA = 25% 0xB = 27.5% 0xC = **30%** 0xD = 32.5% 0xE = 35% 0xF = 37.5% 0x10 = 40% 0x11 = 42.5% 0x12 = 45% 0x13 = 47.5% 0x14 = 50% 0x15 = 52.5% 0x16 = 55% 0x17 = 57.5% 0x18 = 60% 0x19 = 62.5% 0x1A = 65% 0x1B = 67.5% 0x1C = 70% 0x1D = 72.5% 0x1E = 75% 0x1F = 77.5%

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9.18 IVP_VOLTAGE Register (Address = 0xDA) [Reset = 0xFF]

IVP_VOLTAGE is shown in 表 9-20.

Return to the Summary Table.

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表 9-20. IVP_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	V_IVP	R/W	0xFF	Input Overvoltage Protection and Regulatoin Threshold 0x0 = 4.75V 0x1 = 4.875V 0x2 = 5.000V 0x3 = 5.125V 0x4 = 5.250V 0x5 = 5.375V 0x6 = 5.500V 0x7 = 5.625V 0x8 = 5.750V 0x9 = 5.875V 0xA = 6.000V 0xB = 6.125V 0xC = 6.250V 0xD = 6.375V 0xE = 6.500V 0xF = 6.625V 0x10 = 6.750V 0x11 = 6.875V 0x12 = 7.000V 0x13 = 7.125V 0x14 = 7.250V 0x15 = 7.375V 0x16 = 7.500V 0x17 = 7.625V 0x18 = 7.750V 0x19 = 7.875V 0x1A = 8.000V 0x1B = 8.125V 0x1C = 8.250V 0x1D = 8.375V 0x1E = 8.500V 0x1F = 8.625V 0x20 = 8.750V 0x21 = 8.875V 0x22 = 9.000V 0x23 = 9.125V 0x24 = 9.250V 0x25 = 9.375V 0x26 = 9.500V 0x27 = 9.625V 0x28 = 9.750V 0x29 = 9.875V 0x2A = 10.000V 0x2B = 10.125V 0x2C = 10.250V 0x2D = 10.375V 0x2E = 10.500V 0x2F = 10.625V 0x30 = 10.750V 0x31 = 10.875V 0x32 = 11.000V 0x33 = 11.125V 0x34 = 11.250V 0x35 = 11.375V 0x36 = 11.500V 0x37 = 11.625V 0x38 = 11.750V 0x39 = 11.875V 0x3A = 12.000V 0x3B = 12.125V 0x3C = 12.250V 0x3D = 12.375V 0x3E = 12.500V 0x3F = 12.625V

表 9-20. IVP_VOLTAGE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0x40 = 12.750V 0x41 = 12.875V 0x42 = 13.000V 0x43 = 13.125V 0x44 = 13.250V 0x45 = 13.375V 0x46 = 13.500V 0x47 = 13.625V 0x48 = 13.750V 0x49 = 13.875V 0x4A = 14.000V 0x4B = 14.125V 0x4C = 14.250V 0x4D = 14.375V 0x4E = 14.500V 0x4F = 14.625V 0x50 = 14.750V 0x51 = 14.875V 0x52 = 15.000V 0x53 = 15.125V 0x54 = 15.250V 0x55 = 15.375V 0x56 = 15.500V 0x57 = 15.625V 0x58 = 15.750V 0x59 = 15.875V 0x5A = 16.000V 0x5B = 16.125V 0x5C = 16.250V 0x5D = 16.375V 0x5E = 16.500V 0x5F = 16.625V 0x60 = 16.750V 0x61 = 16.875V 0x62 = 17.000V 0x63 = 17.125V 0x64 = 17.250V 0x65 = 17.375V 0x66 = 17.500V 0x67 = 17.625V 0x68 = 17.750V 0x69 = 17.875V 0x6A = 18.000V 0x6B = 18.125V 0x6C = 18.250V 0x6D = 18.375V 0x6E = 18.500V 0x6F = 18.625V 0x70 = 18.750V 0x71 = 18.875V 0x72 = 19.000V 0x73 = 19.125V 0x74 = 19.250V 0x75 = 19.375V 0x76 = 19.500V 0x77 = 19.625V 0x78 = 19.750V 0x79 = 19.875V 0x7A = 20.000V 0x7B = 20.125V 0x7C = 20.250V 0x7D = 20.375V 0x7E = 20.500V 0x7F = 20.625V 0x80 = 20.750V

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表 9-20. IVP_VOLTAGE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0x81 = 20.875V 0x82 = 21.000V 0x83 = 21.125V 0x84 = 21.250V 0x85 = 21.375V 0x86 = 21.500V 0x87 = 21.625V 0x88 = 21.750V 0x89 = 21.875V 0x8A = 22.000V 0x8B = 22.125V 0x8C = 22.250V 0x8D = 22.375V 0x8E = 22.500V 0x8F = 22.625V 0x90 = 22.750V 0x91 = 22.875V 0x92 = 23.000V 0x93 = 23.125V 0x94 = 23.250V 0x95 = 23.500V 0x96 = 23.750V 0x97 = 24.000V 0x98 = 24.250V 0x99 = 24.500V 0x9A = 24.750V 0x9B = 25.000V 0x9C = 25.250V 0x9D = 25.500V 0x9E = 25.750V 0x9F = 26.000V 0xA0 = 26.250V 0xA1 = 26.500V 0xA2 = 26.750V 0xA3 = 27.000V 0xA4 = 27.250V 0xA5 = 27.500V 0xA6 = 27.750V 0xA7 = 28.000V 0xA8 = 28.250V 0xA9 = 28.500V 0xAA = 28.750V 0xAB = 29.000V 0xAC = 29.250V 0xAD = 29.500V 0xAE = 29.750V 0xAF = 30.000V 0xB0 = 30.250V 0xB1 = 30.500V 0xB2 = 30.750V 0xB3 = 31.000V 0xB4 = 31.250V 0xB5 = 31.500V 0xB6 = 31.750V 0xB7 = 32.000V 0xB8 = 32.250V 0xB9 = 32.500V 0xBA = 32.750V 0xBB = 33.000V 0xBC = 33.250V 0xBD = 33.500V 0xBE = 33.750V 0xBF = 34.000V 0xC0 = 34.250V 0xC1 = 34.500V

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表 9-20. IVP_VOLTAGE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
				0xC2 = 34.750V 0xC3 = 35.000V 0xC4 = 35.250V 0xC5 = 35.500V 0xC6 = 35.750V 0xC7 = 36.000V 0xC8 = 36.250V 0xC9 = 36.500V 0xCA = 36.750V 0xCB = 37.000V 0xCC = 37.250V 0xCD = 37.500V 0xCE = 37.750V 0xCF = 38.000V 0xD0 = 38.250V 0xD1 = 38.500V 0xD2 = 38.750V 0xD3 = 39.000V 0xD4 = 39.250V 0xD5 = 39.500V 0xD6 = 39.750V 0xD7 = 40.000V 0xD8 = 40.250V 0xD9 = 40.500V 0xDA = 40.750V 0xDB = 41.000V 0xDC = 41.250V 0xDD = 41.500V 0xDE = 41.750V 0xDF = 42.000V 0xE0 = 42.250V 0xE1 = 42.500V 0xE2 = 42.750V 0xE3 = 43.000V 0xE4 = 43.250V 0xE5 = 43.500V 0xE6 = 43.750V 0xE7 = 44.000V 0xE8 = 44.250V 0xE9 = 44.500V 0xEA = 44.750V 0xEB = 45.000V 0xEC = 45.250V 0xED = 45.500V 0xEE = 45.750V 0xEF = 46.000V 0xF0 = 46.250V 0xF1 = 46.500V 0xF2 = 46.750V 0xF3 = 47.000V 0xF4 = 47.250V 0xF5 = 47.500V 0xF6 = 47.750V 0xF7 = 48.000V 0xF8 = 48.250V 0xF9 = 48.500V 0xFA = 48.750V 0xFB = 49.000V 0xFC = 49.250V 0xFD = 49.500V 0xFE = 49.750V 0xFF = **50.000V**

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10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The LM51772 is a wide input voltage, synchronous, non-inverting buck-boost controller, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. To expedite and streamline the process of designing the external circuits and select the components, a comprehensive quickstart calculator is available for download to assist the designer with component selection for a given application.

10.2 Typical Application

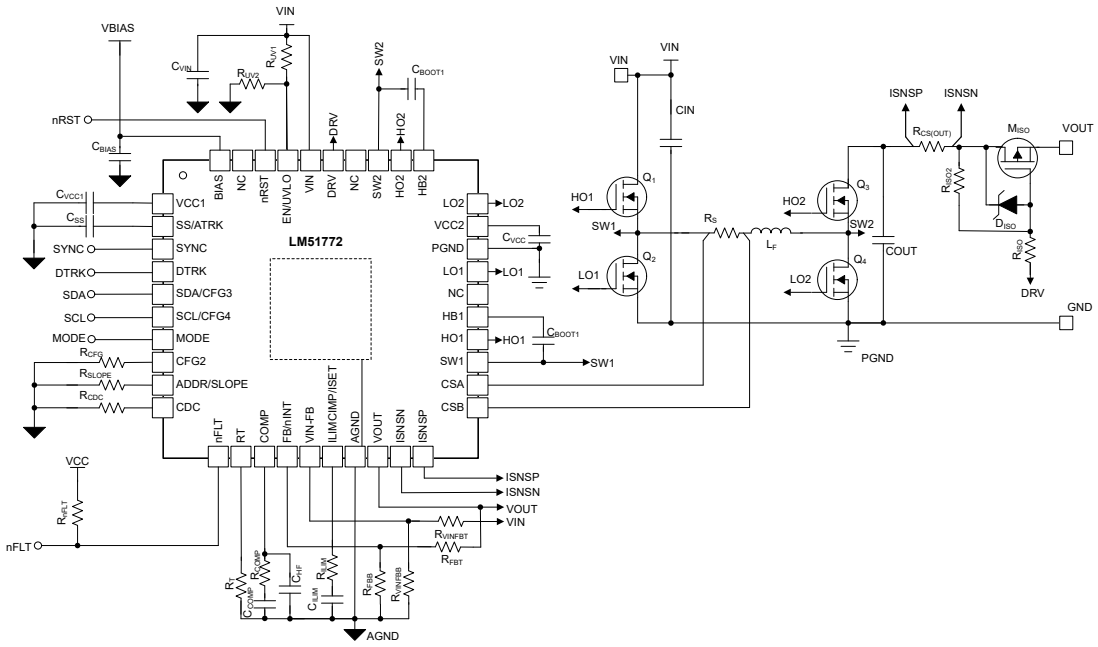

図 10-1. Simplified Schematic of a Typical Application

10.2.1 Design Requirements

表 10-1 shows the intended input, output, and performance parameters for a typical design example.

表 10-1. Design Parameters

Parameter	Value
V_I minimum	9V
V_I typical = V_I start-up	19.5V
V_I maximum	48V
V_O nominal	20V
P_O maximum	100W

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10.2.2 Detailed Design Procedure

10.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM51772 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

10.2.2.2 Frequency

The switching frequency of LM51772 is set by an R_T resistor connected from the RT/SYNC pin to AGND. The R_T resistor required to set the desired frequency is calculated using 式 10. A 1% standard resistor of 51.0kΩ is selected for f_{SW} = 600kHz.

$$R_{(RT)} = \left(\frac{1}{f_{SW}} - 18ns\right) \times 31.5 \frac{G\Omega}{s} \quad (10)$$

10.2.2.3 Feedback Divider

The feedback voltage divider is found with 式 11:

$$R_{FB,top} = \left(V_{(VOUT)} - V_{(REF)}\right) \times R_{FB,bot} \quad (11)$$

For the 20V output, an upper resistor of 82.0kΩ and a lower resistor of 4.3kΩ have been selected.

FB Pin Resistor Divider Examples with $R_{FB,top}$ = 71.5kΩ shows an overview of a possible selection for the feedback divider resistors over common output voltages.

表 10-2. FB Pin Resistor Divider Examples with $R_{FB,top}$ = 71.5kΩ

V_O – Target	$R_{FB,bot}$ – Calculation	$R_{FB,bot}$ – E48 Series	V_O Nominal	Error from FB Resistor
5V	17.9kΩ	17.8kΩ	5.02V	0.3%
9V	8.94kΩ	9.09kΩ	8.87V	-1.5%
12V	6.50kΩ	6.59kΩ	12.02V	0.1%
16V	4.77kΩ	4.87kΩ	15.68V	-2.0%
24V	3.11kΩ	3.16kΩ	23.63V	–1.6%
28V	2.65kΩ	2.61kΩ	28.39V	1.4%
36V	2.04kΩ	2.05kΩ	35.88V	–0.3%
42V	1.74kΩ	1.78kΩ	41.17V	-2.0%
48V	1.50kΩ	1.54kΩ	47.43V	–1.2%

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10.2.2.4 Inductor and Current Sense Resistor Selection

The inductor selection is based on consideration of both buck and boost modes of operation and the range of the supported slope compensation. As inductor and current sense resistor influencing each other both needs to be selected depending on each other. A good starting point is to set the current sense resistor to have an aveage current level of 60% of the overcurrent detection level. This considers an inductor ripple ΔI_L of 20% and a margin of 20% to the overcurrent detection level. The highest inductor current appears at the lowest input voltage.

$$I_{L\,Peak,\ \max,\mathrm{est.}} = \frac{V_{OUT}}{V_{IN,min}} \times I_{OUT} \times 1.4 = 15.6\ A \tag{12}$$

The sense resistor can be calculated with:

$$R_{CS} = \frac{50\ mV}{I_{L\,Peak,\ \max,\mathrm{est.}}} = 3.2\ m\Omega \tag{13}$$

The inductor can be selected with have a mid level slope compensation. This can be calculated with:

$$L = \frac{R_{CS} \times 625}{f_{SW}} = 3.35\ \mu H \tag{14}$$

Additionally, the inductor selection can be based on the peak-to-peak current ripple ΔI_L for buck and boost mode, depending if better efficiency for buck or boost operartion is important. The target inductance for buck mode with approximately 60% of the maximum inductor current at the maximum input voltage is:

$$\mathrm{L_{BUCK}} = \frac{\left(\mathrm{V_{IN(MAX)}} - \mathrm{V_{OUT}}\right) \times \mathrm{V_{OUT}}}{0.6 \times \mathrm{I_{OUT(MAX)}} \times \mathrm{F_{SW}} \times \mathrm{V_{IN(MAX)}}} = 6.48\ \mu\mathrm{H} \tag{15}$$

The target inductance for boost mode with approximately 30% of the maximum inductor current at the maximum input voltage is:

$$\mathrm{L_{BOOST}} = \frac{\mathrm{V_{IN(MIN)}^2} \times \left(\mathrm{V_{OUT}} - \mathrm{V_{IN(MIN)}}\right)}{0.3 \times \mathrm{I_{OUT(MAX)}} \times \mathrm{F_{SW}} \times \mathrm{V_{OUT}^2}} = 2.48\ \mu\mathrm{H} \tag{16}$$

For this application, an inductor with 3.3µH was selected.

The peak inductor current occurs at in this configuration occurs at minimum input voltage and with an efficiency of 95% is given by:

$$I_{L\,Peak\,Boost} = \frac{V_{OUT}{}^{*}\,I_{OUT}}{\eta^{*}V_{IN,min}} + \frac{V_{IN,min}{}^{*}\left(V_{OUT} - V_{IN,min}\right)}{2^{*}L^{*}f_{SW}{}^{*}V_{OUT}} = 12.9A \tag{17}$$

For the current sense resistor a margin of 20% is considered to have enough headroom for the dymamic responses, e.g. load step regulation. To ensure the maximum output current can be delivered the mimimum level of the peak current limit threshold is used:

$$R_{CS} = \frac{39\ mV}{I_{L\,Peak\,Boost}} = 3.0\ m\Omega \tag{18}$$

The standard value of RCS = 2.5mΩ with 2 times 5mΩ is selected. With the two resistors in parallel it also reduces the parasitic inductance. The maximum power dissipation in RCS happens at VIN(MAX):

$$\mathrm{P_{R_{CS(Max)}}} = \left(\frac{59\ mV}{R_{CS}}\right)^2 \times R_{CS} \times \left(1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN(Max)}}}\right) = 0.81\ \mathrm{W} \tag{19}$$

10.2.2.5 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by:

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (20)$$

where the minimum V_{IN} corresponds to the maximum capacitor current.

In this example, the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 5.5A. A 3mΩ output capacitor ESR causes an output ripple voltage of 33.3mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (21)$$

A 80µF output capacitor causes a capacitive ripple voltage of 151mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (22)$$

Typically, a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. セクション 10.2 shows a good starting point for C_{OUT} for typical applications.

10.2.2.6 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (23)$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)} = I_{OUT} / 2$ = 2.5A. A combination of ceramic and bulk capacitors must be used to provide a short path for high di/dt current and to reduce the output voltage ripple. 図 10-1 is a good starting point for C_{IN} for typical applications.

10.2.2.7 Slope Compensation

For stable current loop operation and to avoid subharmonic oscillations, the slope resistor must be selected based on 式 24:

$$SlopeComp = \frac{R_{CS}}{L \times f_{sw}} \times 625 = 0.79 \quad (24)$$

The next higher value has to be selected which is 0.825 and then be set via R_{CFG1} or the I2C interface. This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically, a current mode loop is stable with half the “dead-beat” slope (considered already in the calculated slope resistor value in 式 24). A smaller slope capacitor results in larger slope signal, which is better for noise immunity in the transition region (V_{IN} is approximately equal to V_{OUT}). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design, a slope compensation factor of 0.875 (see Configuration Pin CFG2) is selected for better transition region behavior while still providing the required V_{IN} range. This selection of slope capacitor, inductor, switching frequency, and inductor satisfies the COMP range limitation.

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10.2.2.8 UVLO Divider

The UVLO resistor divider must be designed for turn-on below 8. 7V. Selecting $R_{UVLO,top}$ = 75kΩ gives a UVLO hysteresis of 0.375V based on 式 25. The lower UVLO resistor is selected using:

$$V_{(VIN,\,IT+,\,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \quad (25)$$

A standard value of 12.4kΩ is selected for $R_{UVLO,bot}$.

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN}.

10.2.2.9 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} = 18\ nF \quad (26)$$

C_{SS} = 18nF gives a soft-start time of 1.8ms.

10.2.2.10 MOSFETs QH1 and QL1

The input side MOSFETs QH1 (Q1) and QL1 (Q2) need to withstand the maximum input voltage of 48V. In addition, they must withstand the transient spikes at SW1 during switching. Therefore, QH1 and QL1 must be rated for 58V or higher. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH1 in boost mode is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QH1)} \quad (27)$$

The power loss in QH1 in buck mode consists of both conduction and switching loss components given by 式 28 and 式 29, respectively:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QH1)} \quad (28)$$

$$P_{SW(QH1)} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \quad (29)$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (smaller conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is shown in 式 30:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times {I_{OUT}}^2 \times R_{DS,\,On(QL1)} \quad (30)$$

10.2.2.11 MOSFETs QH2 and QL2

The output side MOSFETs QH2 (Q4) and QL2 (Q3) see the output voltage of 48V and additional transient spikes at SW2 during switching. Therefore, QH2 and QL2 must be rated for 58V or more. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH2 in buck mode of operation is approximated by:

$$P_{COND(QH2)} = I_{OUT}^2 \times R_{DS,On(QH2)} \quad (31)$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QL2)} \quad (32)$$

and, respectively:

$$P_{SW(QL2)} = \frac{1}{2} \times V_{OUT} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right) \times (t_r + t_f) \times f_{SW} \quad (33)$$

The rise (t_r) and the fall (t_f) times can be based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is shown below:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,On(QH2)} \quad (34)$$

10.2.2.12 Loop Compensation

This section presents the control loop compensation design procedure for the LM51772 buck-boost controller. The LM51772 operates mainly in buck or boost modes, separated by a transition region, and therefore, the control loop design is done for both buck and boost operating modes. Then, a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically, for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in boost mode.

The boost power stage output pole location is given by:

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 995\ \text{Hz} \quad (35)$$

where

- R_{OUT} = 5.0Ω corresponds to the maximum load of 5.0A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 73.7\ \text{kHz} \quad (36)$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L_1}\right) = 39.1\ \text{kHz} \quad (37)$$

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where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN}.

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 497 \text{ Hz} \quad (38)$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from 式 39 that RHP zero is the main factor limiting the achievable bandwidth. For a robust design, the crossover frequency must be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 8kHz:

$$f_{bw} = 8 \text{ kHz} \quad (39)$$

For some power stages, the boost RHP zero may not be as restrictive, which happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero (f_{RHP} / 3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at three times the buck output pole frequency, which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{ZC} = 1.5 \text{ kHz} \quad (40)$$

The compensation gain resistor, R_{c1}, is calculated with:

$$R_{C1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \frac{A_{CS} \times R_{CS} \times C_{OUT}}{1 - D_{MAX}} \times \frac{1}{\sqrt{1 + \left(\frac{f_{bw}}{f_{RHP}}\right)^2}} = 7.4 \text{ k}\Omega \quad (41)$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode.
- A_{CS} is the current sense amplifier gain.

The compensation capacitor, C_{c1}, is then calculated from:

$$C_{C1} = \frac{1}{2\pi \times f_{ZC} \times R_{c1}} = 14.5\text{nF} \quad (42)$$

The standard values of compensation components are selected to be R_{c1} = 7.32kΩ and C_{c1} = 15nF.

A high frequency pole (f_{pc2}) is placed using a capacitor (C_{c2}) in parallel with R_{c1} and C_{c1}. Set the frequency of this pole at seven to ten times of f_{bw} to provide attenuation of switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target f_{pc2} = 98kHz, C_{c2} is calculated using 式 43:

$$C_{C2} = \frac{1}{2\pi \times f_{pc2} \times R_{c1}} = 263 \text{ pF} \quad (43)$$

Select a standard value of 270pF for C_{c2}. These values provide a good starting point for the compensation design. Each design must be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

ADVANCE INFORMATION

10.2.2.13 External Component Selection

表 10-3. Components Example for Typical Application

Reference	Description	Part Number	Comment
R_{COMP}	7.32kΩ		
C_{COMP1}	15nF, 50V Ceramic Capacitor		
C_{COMP2}	270pF, 50V Ceramic Capacitor		
C_{SS}	18nF, 50V Ceramic Capacitor or 20nF, 80V Ceramic Capacitor	GCM21B5C1H183JA16 or GCM21B5C1K203JA16	
$R_{FB,top}$	71. 5kΩ		
$R_{FB,bot}$	4.7kΩ		
$C_{FB,ff}$	N/A		
R_{nFLT}	10kΩ		
$R_{IMONOUT}$	82kΩ		
C_{IN1}	2 × 10µF, 50V Ceramic Capacitor	GCM32EC71H106KA03	
C_{IN2}	1× 100µF, 63V Aluminum Capacitor	PCR1J101MCL1GS	
M_1	N-Channel 40-V MOSFET, $R_{DS(on)}$ = 4.3 mΩ	SQJ422EP	
M_2	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP	
M_3	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP	
M_4	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP	
R_{CS}	1.33mΩ	3xKRL2012E-C-R004-F	
L_1	1.8µH, DCR = 3.2mΩ	IHLP-5050FD-A1	
C_{OUT1}	5 × 10µF, 50V Ceramic Capacitor	GCM32EC71H106KA03	
C_{OUT2}	1 × 100µF, 63V Aluminum Capacitor	PCR1J101MCL1GS	
R_{ISNS}	4mΩ	KRL2012E-C-R004-F	
C_{BST1}	0.1µF, 35V Ceramic Capacitor	GRT033R6YA104KE01	
C_{BST2}	0.1µF, 35V Ceramic Capacitor	GRT033R6YA104KE01	
C_{VCC}	22µF, 6.3V Ceramic Capacitor	GRT188R61A226ME13	
$R_{UVLO,top}$	75kΩ		
$R_{UVLO,bot}$	12.4kΩ		
R_{SLOPE}	5.1kΩ		
R_{CFG2}	8.3kΩ		
R_{RT}	39kΩ		

ADVANCE INFORMATION

ADVANCE INFORMATION

10.2.3 Application Curves

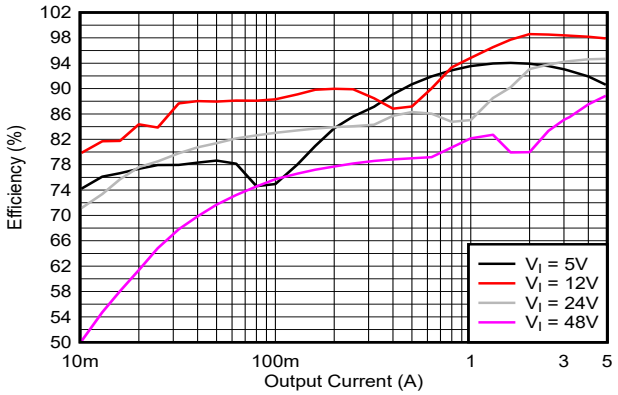

図 10-2. Efficiency Versus I_O(MODE = 0V V_o = 12V)

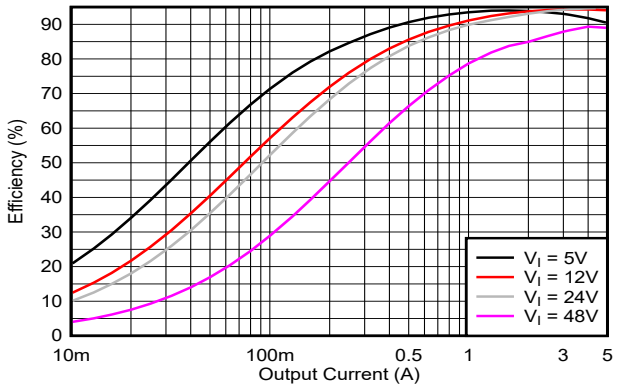

図 10-3. Efficiency Versus I_O(MODE = VCC2 V_o = 12V)

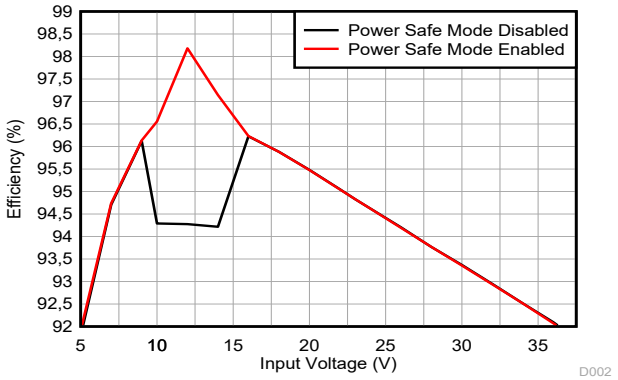

図 10-4. Efficiency Versus V_I (V_o = 12V, I_O = 5A)

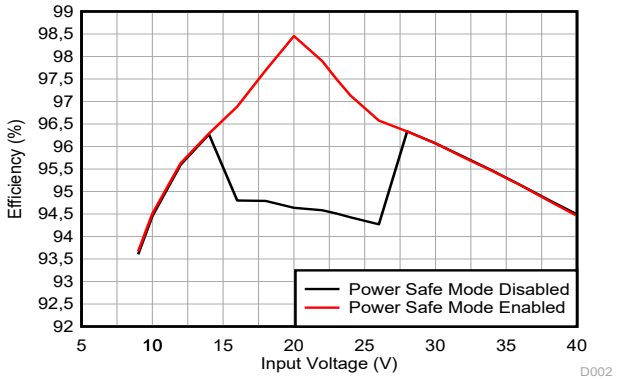

図 10-5. Efficiency Versus V_I (V_o = 20V, I_O = 5A)

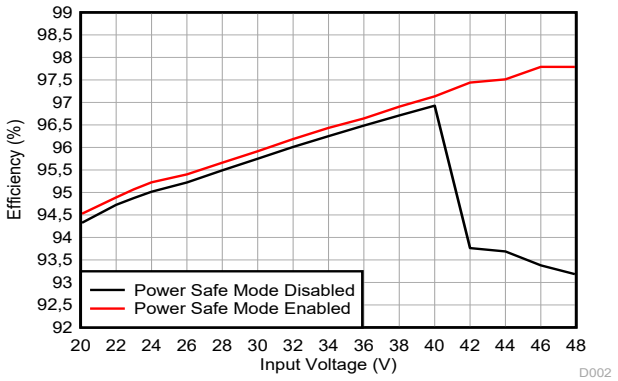

図 10-6. Efficiency Versus V_I(V_o = 48V, I_O = 5A)

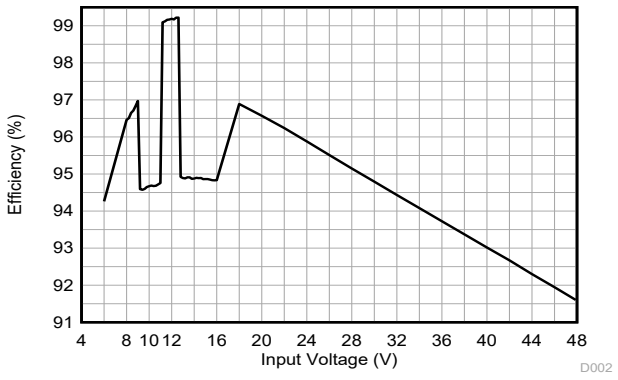

図 10-7. Efficiency Versus V_I ($V_{(PCM,low)}$ = 11V, $V_{(PCM,high)}$ = 13V, I_O = 5A,MODE = VCC2)

10.3 Power Supply Recommendations

The LM51772 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use 式 44 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{44}$$

where

- η the efficiency.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Unless carefully designed, it can lead to instability as well as some of the previously mentioned affects.

10.4 Layout

10.4.1 Layout Guidelines

10.4.1.1 Power Stage Layout

Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of the buck-boost regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized when leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield, and isolate the small-signal traces from noisy power traces.

The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.

- The most important loop areas to minimize are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops.
- In addition to these recommendation, follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

10.4.1.2 Gate Driver Layout

The LM51772 high-side and low-side gate drivers incorporate short propagation delays, frequency depended dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the external power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths are not well controlled. Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, and thereby increasing MOSFET switching times.

Connections from the gate driver outputs, HO1 and HO2, to the respective gates of the high-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route HO1 and HO2 and SW1 and SW2 gate traces as a differential pair from the device pin to the high-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Connections from gate driver outputs, LO1 and LO2, to the respective gates of the low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route LO1 and LO2, and PGND traces as a differential pair from the device pin to the low-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Minimize the current loop path from the VCC, HB1, and HB2 pins through their respective capacitors as these provide the high instantaneous current.

10.4.1.3 Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, SLOPE, SS/ATRK, and RT away from high-voltage switching nodes such as the following to avoid mutual coupling:
  - SW1
  - SW2
  - HO1
  - HO2
  - LO1
  - LO2
  - HB1
  - HB2
- Use an internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Route the CSA and CSB and ISNSP and ISNSN traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.
- Locate the upper and lower feedback resistors close to the FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the output voltage sense point.
- Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
- The HTSSOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate (ground) of the device. This connection allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem.

10.4.2 Layout Example

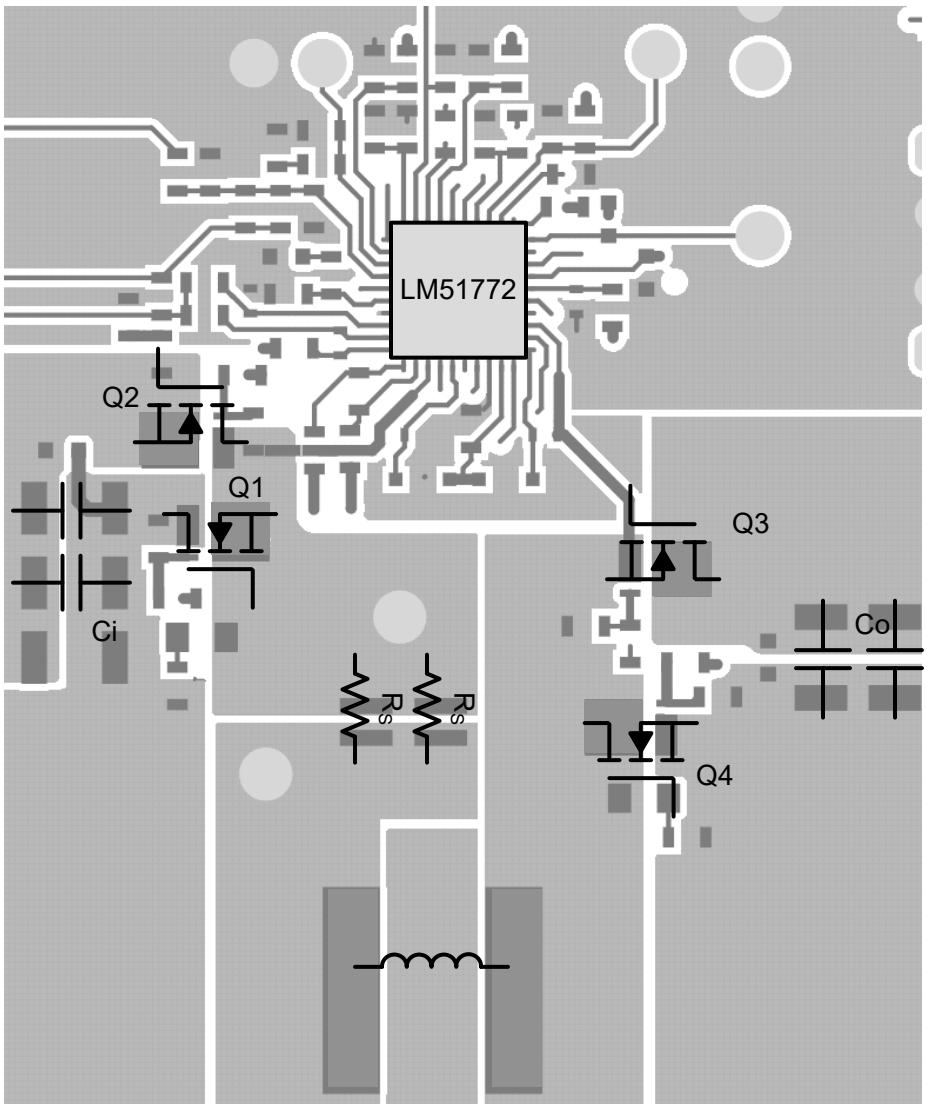

図 10-8. LM51772 Simplified Top Layer Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

ADVANCE INFORMATION

ADVANCE INFORMATION

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2023) to Revision A (March 2024)	Page
• Changed pin functions table descriptions	3
• Added topside marking for experimental and prototype samples	7
• Changed preview samples limitation description	7
• Changed absolute maximum rating for SWx	8
• Changed absolute maximum rating for LOx	8
• Added absolute maximum rating for HBx,HOx	8
• Changed BIAS recommended operation voltage	9
• Added buck minimum duty -cycle for PSM operation versus switching frequency	17
• Added recommendation for PSM buck mode on times.	23
• Change equation for RT resistor calculation	34
• Added description for gate drive dead time configuration	40
• Changed default output voltage from 5V to 12V (0xD from 0x0 to 0x02 and 0xC from 0xFA to 0x58)	57
• Changed current limit setting to ISET pin configuration option. (0xD9 SEL_ISET_PIN form 0x0 0x1)	57
• Changed IVP to disable per default (0xD3 EN_IVP from 0x0 to 0x1)	57
• Changed output discharge to disabled per default (0xD2 DISCHARGE_CONFIG0 form 0x1 to 0x0)	57
• Changed drive Pin sequence to pull low during converter operation. (0xD8 SEL_DRV1_SEQ from 0x0 to 0x1)	57
• Changed PCM_HYST name to PCM_WINDOW_LOW. (0xD9)	57
• Added application curves for efficiency measurements	94

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

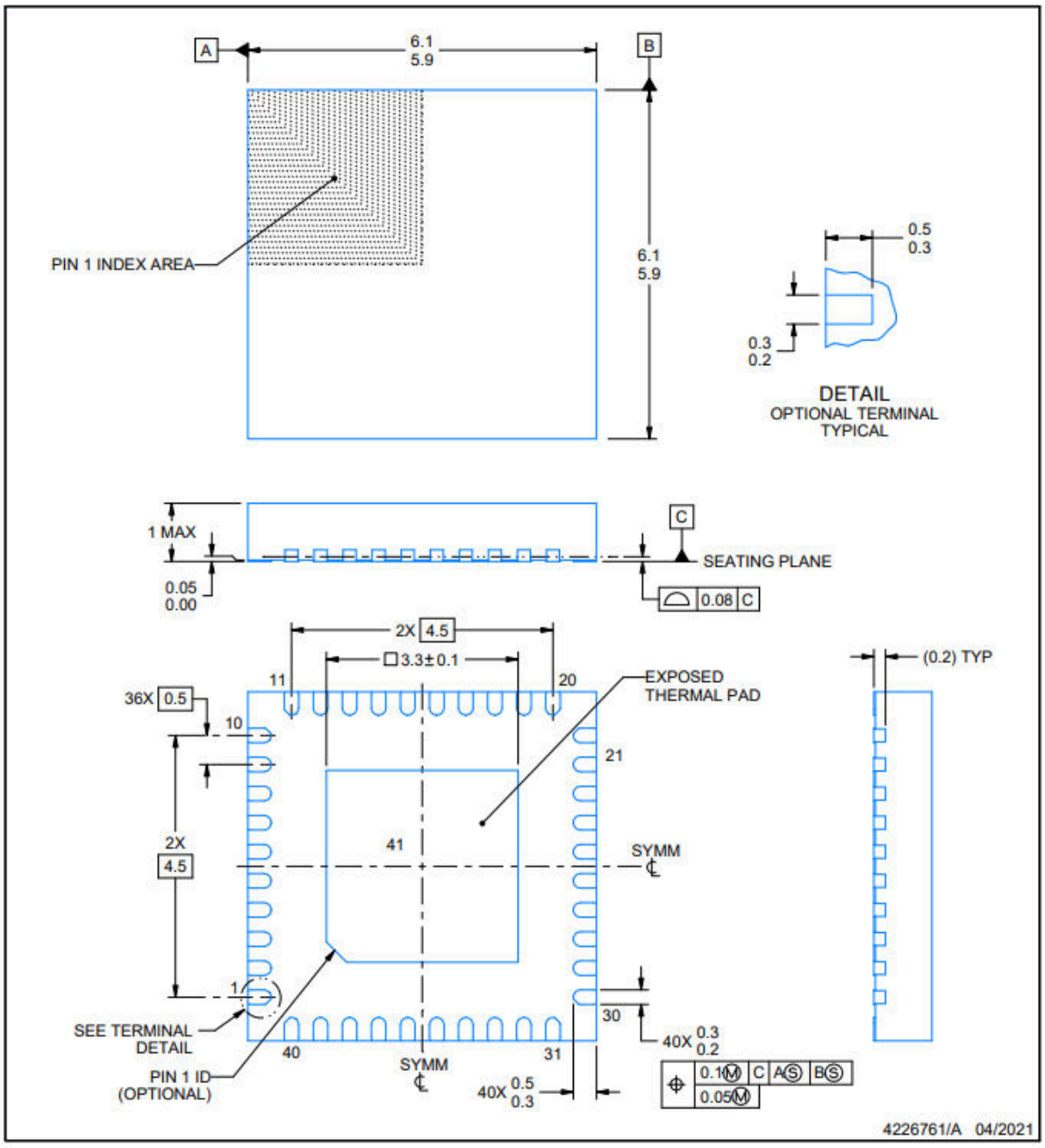
ADVANCE INFORMATION

PACKAGE OUTLINE

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM51772RHAR	ACTIVE	VQFN	RHA	40	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM51772	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

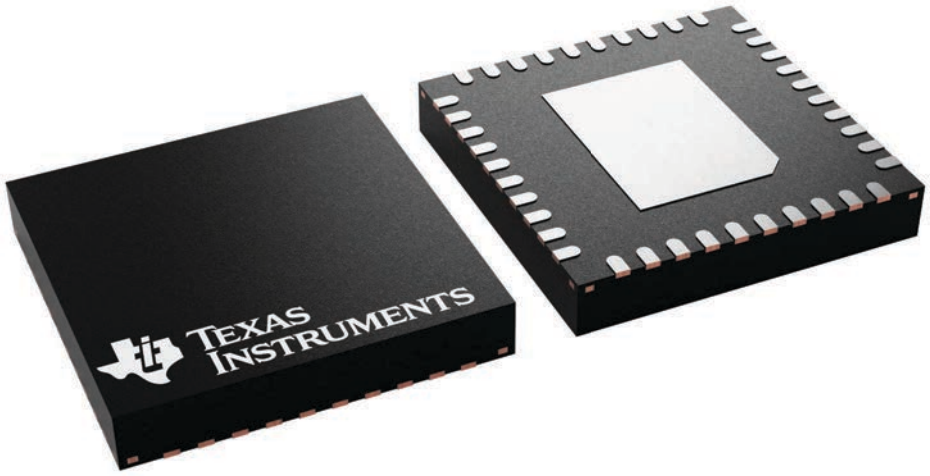
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



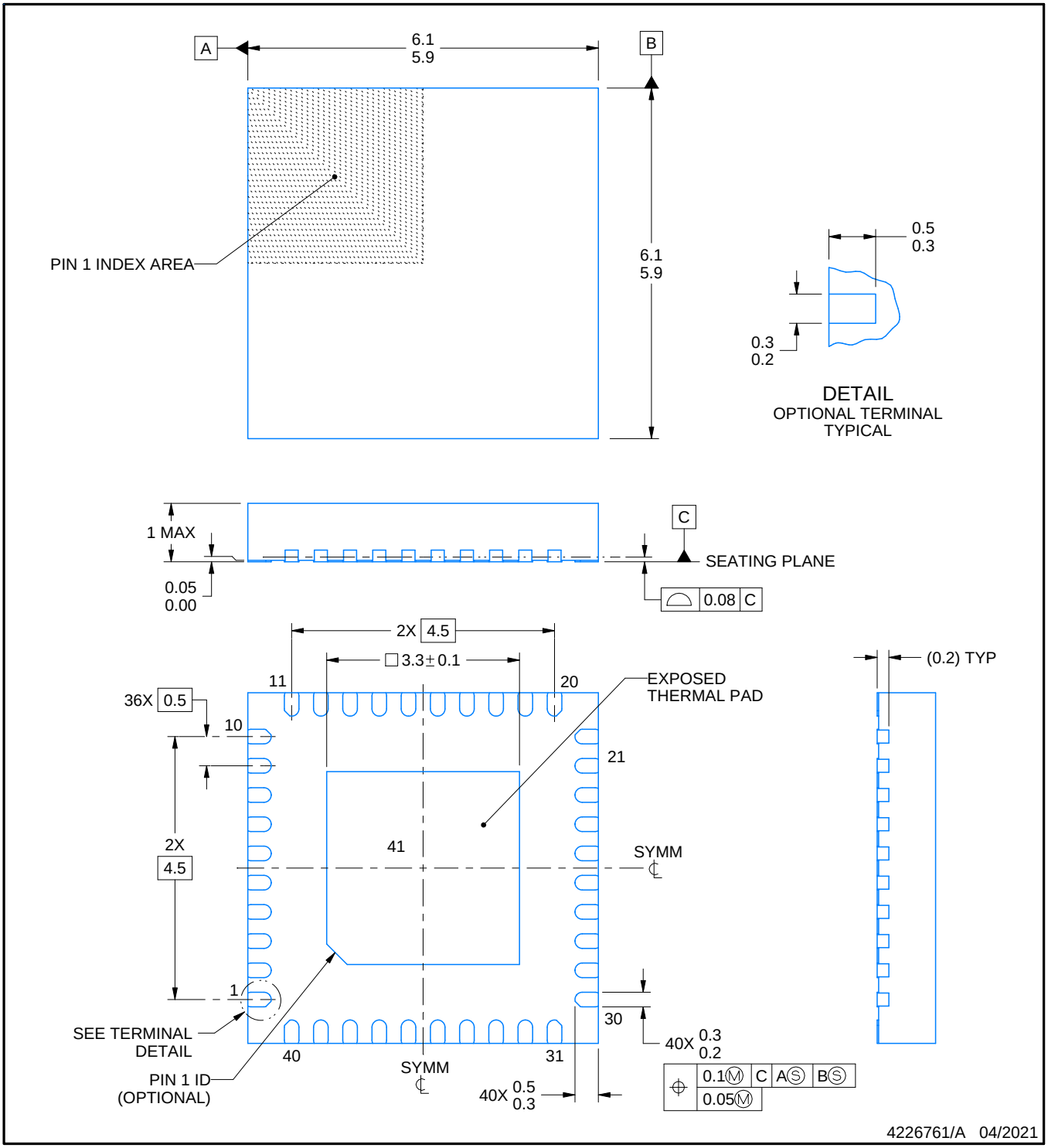
4225870/A

PACKAGE OUTLINE

RHA0040P

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

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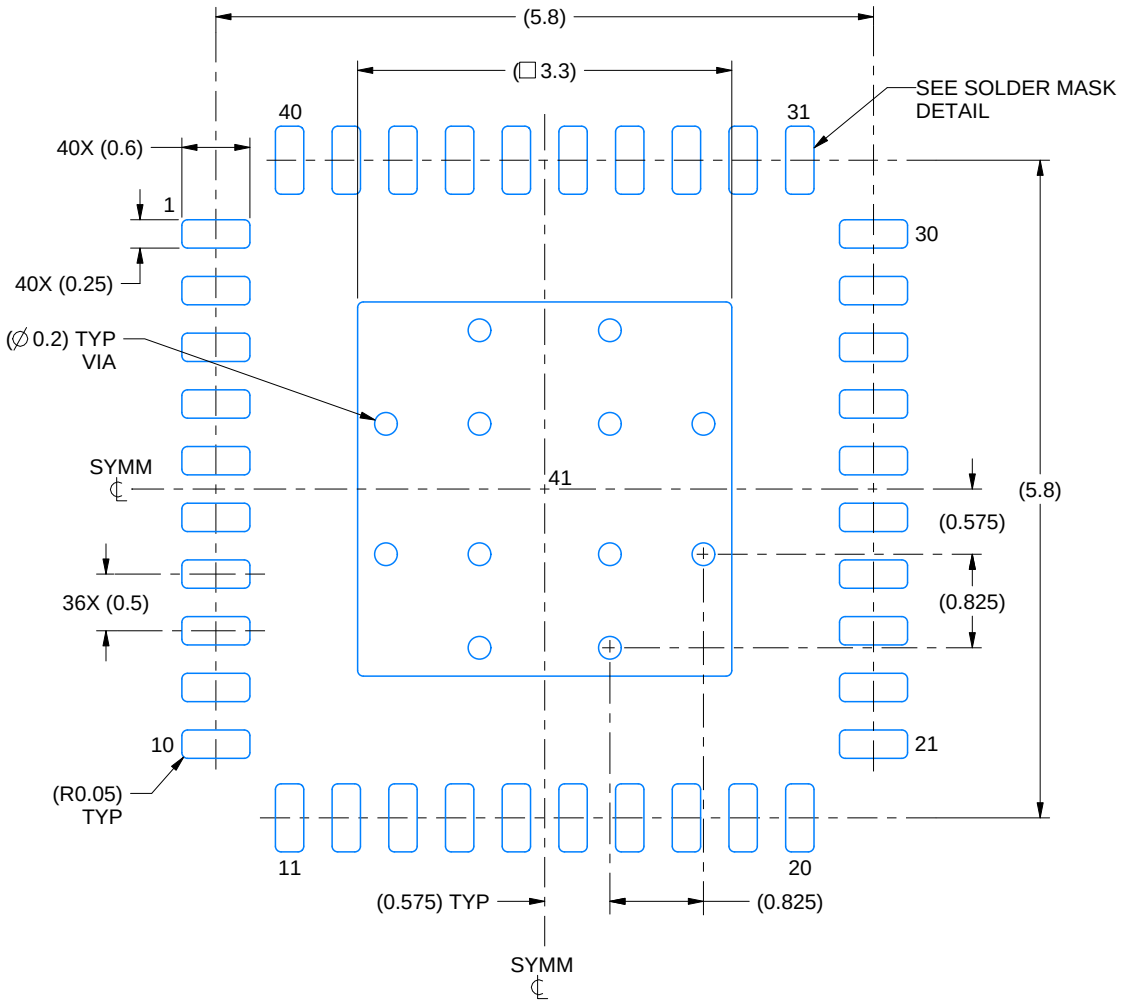
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHA0040P

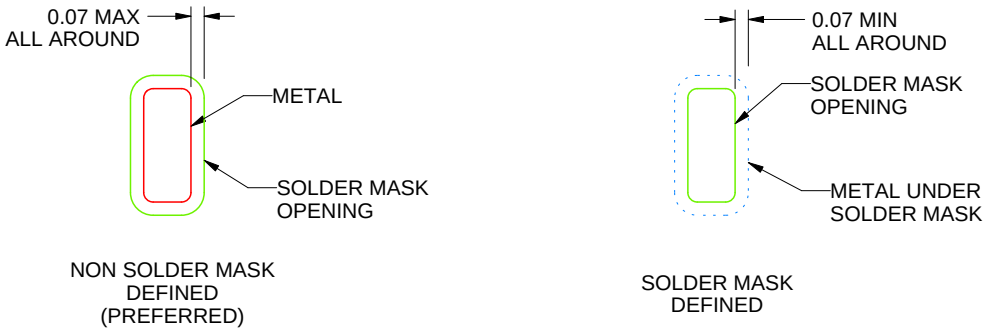
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

SCALE:15X



SOLDER MASK DETAILS

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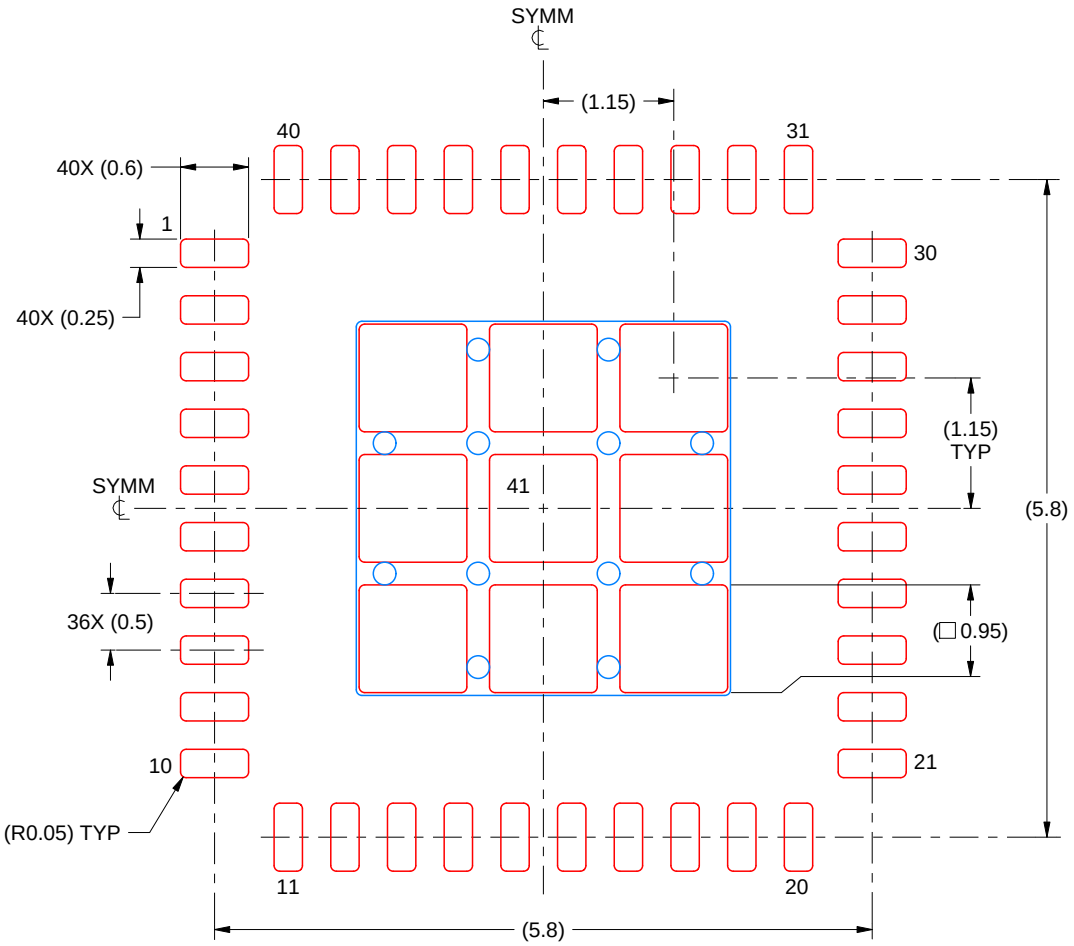
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
78.25% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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