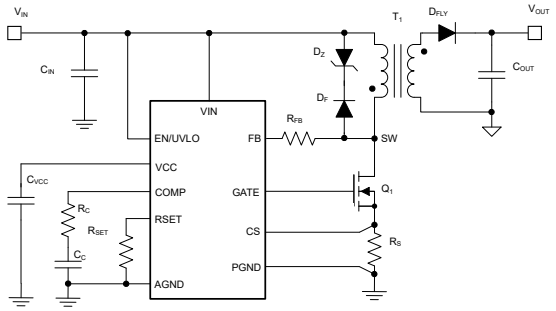
TEXAS INSTRUMENTS
LM5185
JAJSRX5 – NOVEMBER 2023

LM5185 低 I_Q および低 EMI を備えた、100V_{IN}、PSR フライバック方式、DC/DC コントローラ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 4.5V ~ 100V の広い入力電圧範囲
- 1W 未満から 50W 超までの広い電力範囲
- 信頼性が高く堅牢なアプリケーション向けの堅牢な PSR フライバック設計
  - 1 台の変圧器のみが絶縁バリアと交差する堅牢な設計
  - 総出力レギュレーション精度：±1.5%
  - オプションの VOUT 温度補償
  - 入力 UVLO およびサーマル・シャットダウン保護
  - ヒカップ・モード過電流フォルト保護
  - 14 ピン HTSSOP パッケージで 0.9mm の HV-LV ピン間隔
  - -40℃ ~ +150℃の接合部温度範囲
- 統合により設計のサイズとコストを低減
  - V_{OUT} のレギュレーションにフォトカプラも変圧器の補助巻線も不要
  - 2A ピーク・シンクと 1A ピーク・ソース、大電流パワー MOSFET ゲート・ドライバ
- クラス最高のアクティブ I_Q による高効率
  - 重負荷時の境界導通モード (BCM) での擬似共振スイッチング
  - 外部 VCC オプションによる効率向上
  - 軽負荷時の高効率と最小の I_Q (代表値 25µA、外部 VCC 使用時)
  - シングルおよびマルチ出力の実装
- 非常に小さい伝導および放射 EMI シグネチャ
  - ソフト・スイッチングによりダイオードの逆回復を回避
  - CISPR 32 EMI 要件に合わせて設計



概略回路図

- WEBENCH® Power Designer により、LM5185 を使用したカスタム設計を作成

2 アプリケーション

- ファクトリ・オートメーション / 制御：絶縁型フィールド トランスミッタ、フィールド アクチュエータ、およびアナログ入力モジュール向けの複数の出力レール
- モータ駆動：IGBT および SiC ゲート・ドライバの電源
- 太陽エネルギー システム マイクロ インバータおよび太陽光発電オプティマイザ
- PoE PD DC/DC コンバータ
- ビル・オートメーション用 HVAC システム
- 産業用およびテレコム システム用の汎用絶縁型バイアス電源レール
- 汎用 IGBT、MOSFET、GaN、SiC ゲート ドライバ

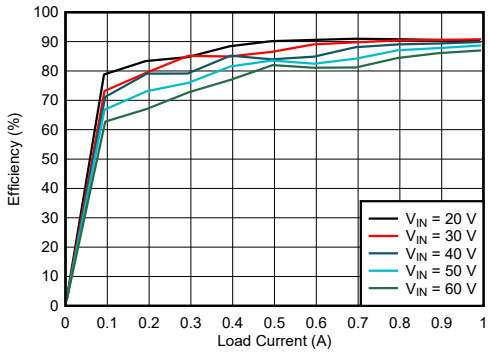
3 概要

LM5185 は、1 次側レギュレーション (PSR) のフライバック コントローラで、4.5V ~ 100V の広い入力電圧範囲にわたって高効率を実現します。絶縁出力電圧は 1 次側フライバック電圧からサンプリングされるため、出力電圧のレギュレーションを行うためにフォトカプラ、基準電圧、変圧器からの 3 次巻線を必要としません。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)	本体サイズ (公称)
LM5185	PWP (HTSSOP、14)	5.00mm × 6.40mm	5.00mm × 4.40mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的な事例の効率、V_{OUT} = 16.4V

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4 概要 (続き)

高レベルの集積化により、シンプルで信頼性が高く、絶縁バリアと交差する変圧器が 1 台のみの高密度な設計を実現しています。境界導通モード (BCM) スイッチングにより、小型の磁気的設計と、±1.5% 以内の負荷およびライン・レギュレーション性能を実現できます。入力過渡応答に対するヘッドルームが強化されており、最大 100V の入力電圧までのアプリケーションに対応しています。

LM5185 フライバック・コントローラを使用すると、対象の最終機器に合わせて性能を最適化するためのオプション機能を備えた絶縁型 DC/DC 電源を簡単に実装できます。出力電圧を 1 つの抵抗で設定でき、オプションの抵抗を使用するとフライバック・ダイオードの電圧降下の温度係数を打ち消して出力電圧精度を向上させることもできます。LM5185 コントローラは、大電流 MOSFET ゲート ドライバを内蔵し、電力範囲が 1W 未満から 50W 以上に拡張されているため、広い電力範囲にわたってスケーラブルで移行しやすい設計になっています。COMP ピンを使用した調整可能な補償と、電流検出抵抗による調整可能なピーク電流制限により、設計の柔軟性が高まり、さまざまなアプリケーション要件に対する優れた選択肢となります。

追加機能としては、内部固定または外部プログラム可能なソフトスタート、オプションの高効率のための外部 VCC、可変ライン UVLO 用のヒステリシス付き高精度イネーブル入力、シャント電流検出によるピーク電流モード制御、ヒカップ・モード過負荷保護、大電流 MOSFET ゲート・ドライバ、自動回復機能付きサーマル・シャットダウン保護があります。高電圧 MOSFET のドレインへの接続が不要なため、安全性が向上し、PCB のクリアランス距離要件が簡素化されます。

LM5185 フライバック・コントローラは、14 ピン、5mm × 4.4mm、0.65mm ピン・ピッチ、熱特性強化型 HTSSOP パッケージで供給されます。

5 Pin Configuration and Functions

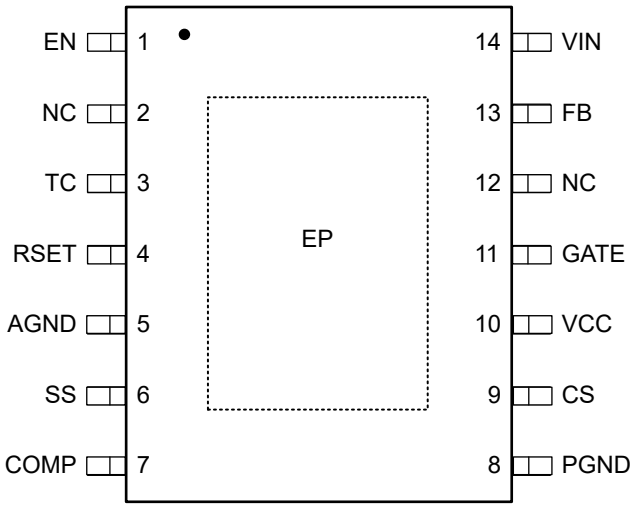


図 5-1. PWP Package 14-Pin HTSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable input and undervoltage lockout (UVLO) programming pin. If the EN voltage is below 1.1 V, the converter is in shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 1.1 V and below 1.5 V, the converter is in standby mode with the internal regulator operational and no switching. If the EN/UVLO voltage is above 1.5 V, the start-up sequence begins.
3	TC	I	Temperature compensation pin. Tie a resistor from TC to RSET to compensate for the temperature coefficient of the forward voltage drop of the secondary diode, thus improving regulation at the secondary-side output.
4	RSET	I	Reference resistor tied to GND to set the reference current for FB. Connect a 10-kΩ resistor from RSET to GND.
5	AGND	G	Analog ground. Ground connection of internal control circuits.
6	SS	I	Soft start input. Connect a capacitor from SS to AGND to adjust the output start-up time and input inrush current. If SS is left open, the internal 6-ms soft-start timer is activated.
7	COMP	O	Transconductance error amplifier output. Connect the compensation network from COMP to AGND
8	PGND	G	Power Ground. Ground connection of the gate driver.
9	CS	I	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
10	VCC	P	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
11	GATE	O	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
13	FB	I	Primary-side feedback pin. Connect a resistor from FB to SW. The ratio of the FB resistor to the resistor at the RSET pin sets the output voltage.
14	VIN	P/I	Input supply connection. Source for internal bias regulators and input voltage sensing pin. Connect directly to the input supply of the converter with short, low impedance paths.
2, 12	NC	—	No electrical connection.
—	EP	—	Exposed Pad. Connect to AGND and the printed-circuit board ground plane to improve power dissipation.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND	–0.3	105	V
	EN/UVLO to AGND	–0.3	105	V
	TC to AGND	–0.3	5.5	V
	SS to AGND	–0.3	5.5	V
	FB to AGND	–0.3	105	V
	FB to VIN	–0.3	0.3	V
	RSET to AGND	–0.3	3	V
	CS to AGND	-0.3	0.3	V
	VCC to AGND	-0.3	15	V
	PGND to AGND	-0.3	0.3	V
Output voltage	GATE to AGND	–0.3	V_{VCC} + 0.3	V
	GATE to AGND (20-ns transient)	–1.5		
	COMP to AGND	-0.3	5.5	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VIN}	Input voltage after turn on	4.5		100	V
$V_{EN/UVLO}$	EN/UVLO voltage			100	V
V_{FB}	FB voltage			100	V
V_{VCC}	VCC voltage	4.5		14	V
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM5185 PWP (HTSSOP) 14 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	52.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	28.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.1	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the full –40°C to 150°C junction temperature range unless otherwise indicated. V_{IN} = 24 V and $V_{EN/UVLO}$ = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$ = 0 V		1.7		µA
I_{ACTIVE}	VIN active current	$V_{EN/UVLO}$ = 2.5 V, V_{RSET} = 1.8 V		425	575	µA
$I_{ACTIVE-VCC}$	VIN current with external VCC supply	V_{VCC} = 8 V		25	40	µA
BIAS REGULATOR						
$V_{VCC-REG}$	VCC regulation voltage			7		V
$V_{VCC-UVLO}$	VCC UVLO rising threshold			4.25		V
$V_{VCC-HYST}$	VCC UVLO hysteresis			0.35		V
$I_{VCC-LIM}$	VCC sourcing current limit			30		mA
ENABLE AND INPUT UVLO						
$V_{SD-RISING}$	Standby threshold	$V_{EN/UVLO}$ rising		0.8	1.1	V
$V_{SD-FALLING}$	Shutdown threshold	$V_{EN/UVLO}$ falling	0.3			V
$V_{UV-RISING}$	Enable threshold	$V_{EN/UVLO}$ rising	1.45	1.5	1.53	V
$V_{UV-HYST}$	Enable voltage hysteresis	$V_{EN/UVLO}$ falling	0.04	0.05		V
$I_{UV-HYST}$	Enable current hysteresis	$V_{EN/UVLO}$ = 1.6 V	4.75	5	5.25	µA
FEEDBACK						
I_{RSET}	RSET current	R_{RSET} = 10 kΩ		100		µA
V_{RSET}	RSET regulation voltage	R_{RSET} = 10 kΩ	0.99	1	1.01	V
$V_{FB-VIN1}$	FB to VIN voltage	I_{FB} = 80 µA	–40			mV
$V_{FB-VIN2}$	FB to VIN voltage	I_{FB} = 120 µA			40	mV
ERROR AMPLIFIER						
g_m	EA transconductance			600		uS
$I_{COMP-SRC}$	V_{COMP} source current			100		µA
$I_{COMP-SNK}$	V_{COMP} sink current			-100		µA
SWITCHING FREQUENCY						
F_{SW-MIN}	Minimum switching frequency			11		kHz
F_{SW-MAX}	Maximum switching frequency			350		kHz
t_{ON-MIN}	Minimum switch on-time			125		ns
DRIVER						

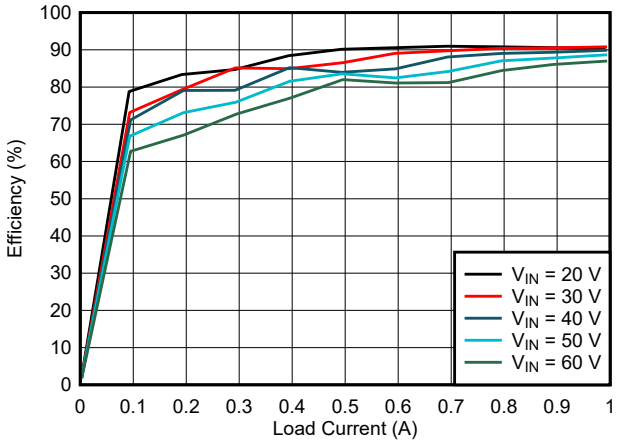
6.5 Electrical Characteristics (続き)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the full –40°C to 150°C junction temperature range unless otherwise indicated. V_{IN} = 24 V and $V_{EN/UVLO}$ = 2 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{GATE-LOW}$	GATE output low voltage			0.02		V
$V_{GATE-HIGH}$	GATE output high voltage			0.07		V
$t_{GATE-RISE}$	GATE output rise time			30		ns
$t_{GATE-FALL}$	GATE output fall time			15		ns
DIODE THERMAL COMPENSATION						
V_{TC}	TC voltage	I_{TC} = ±10 µA, T_J = 25°C		1	1.05	V
SOFT-START AND BIAS						
I_{SS}	SS ext capacitor charging current			5		µA
t_{SS}	Internal SS time			6		ms
CURRENT LIMIT						
V_{CS-MAX}	Peak current limit threshold max		95	100	105	mV
V_{CS-MIN}	Peak current limit threshold min		18	20	22	mV
$t_{CS-DELAY}$	Peak current limit response time			35		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			10		°C

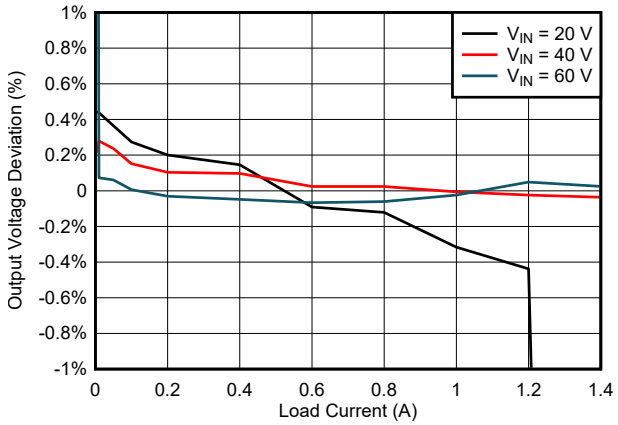
6.6 Typical Characteristics

V_{IN} = 24 V (unless otherwise stated).



See セクション 8.2.1

図 6-1. Efficiency versus Load



See セクション 8.2.1

図 6-2. Output Voltage versus Load

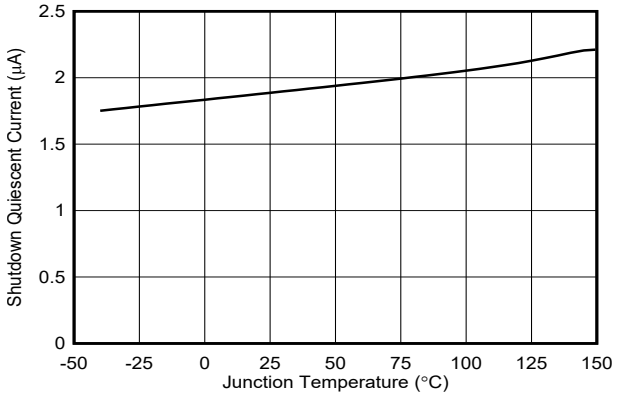


図 6-3. Shutdown Quiescent Current vs. Temperature

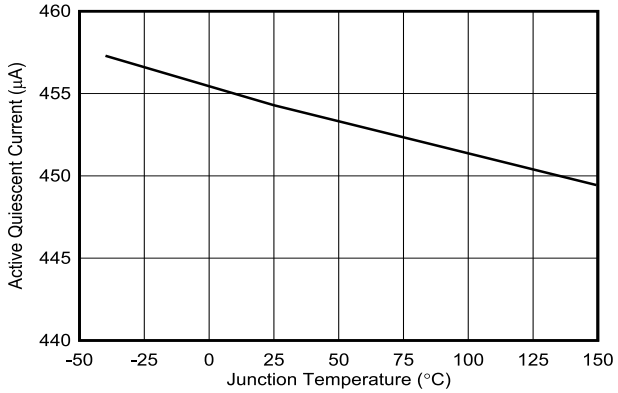


図 6-4. Active Quiescent Current vs. Temperature

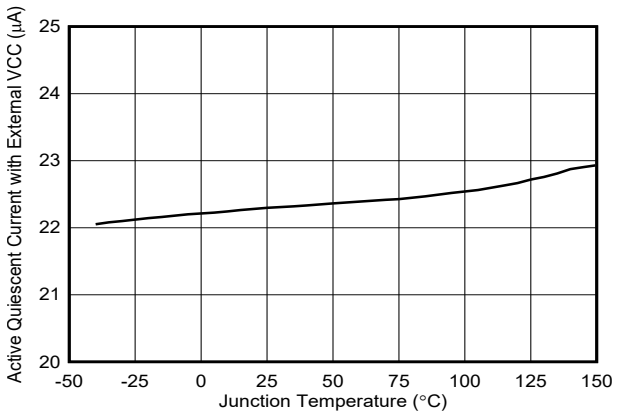


図 6-5. Active Quiescent Current with External VCC vs. Temperature

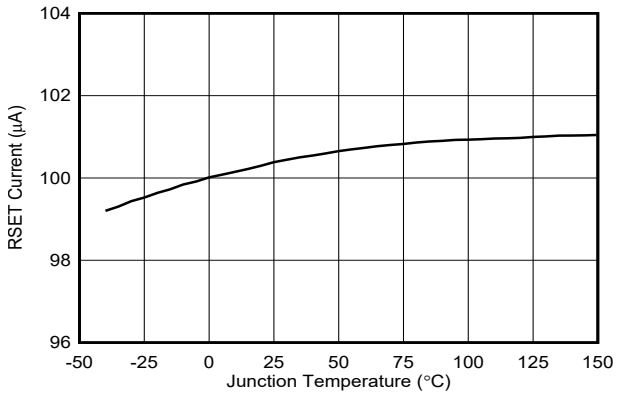


図 6-6. RSET Current versus Temperature

6.6 Typical Characteristics (continued)

V_{IN} = 24 V (unless otherwise stated).

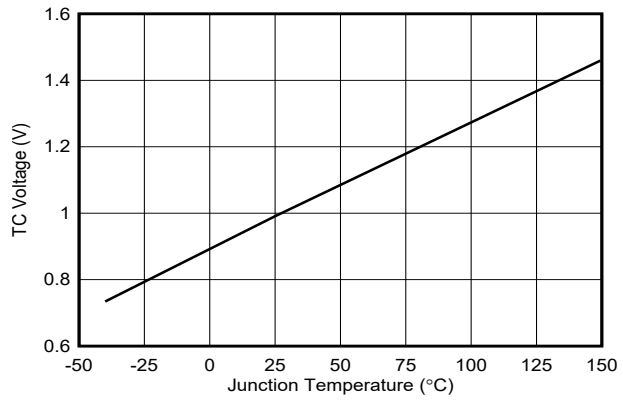


図 6-7. TC Voltage versus Temperature

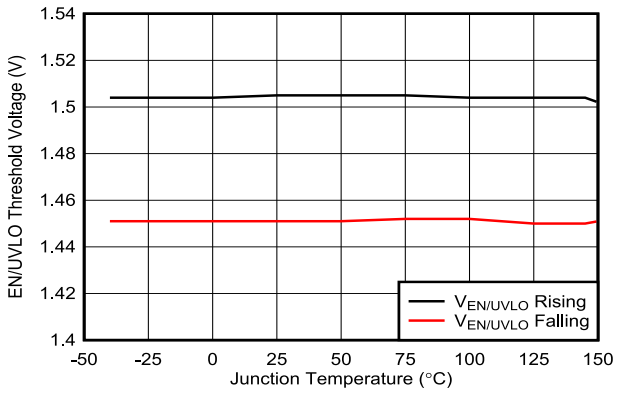


図 6-8. EN/UVLO Threshold Voltages versus Temperature

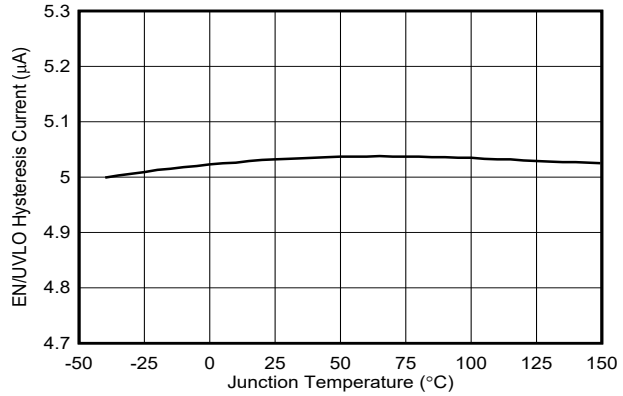


図 6-9. EN/UVLO Hysteresis Current versus Temperature

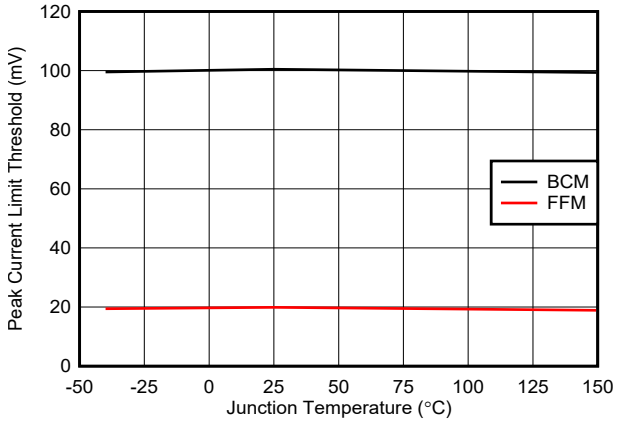


図 6-10. Peak Current Limit Thresholds vs. Temperature

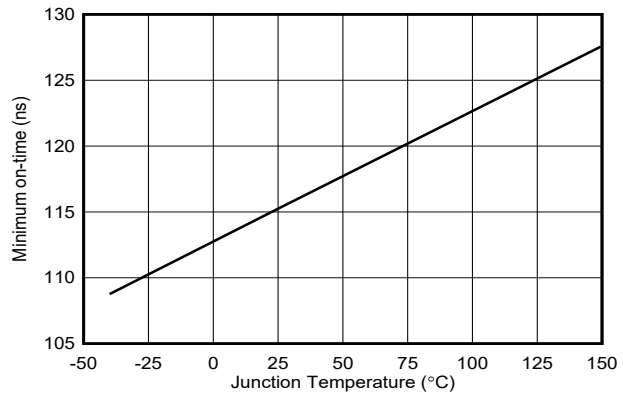


図 6-11. Minimum Switch On-Time versus Temperature

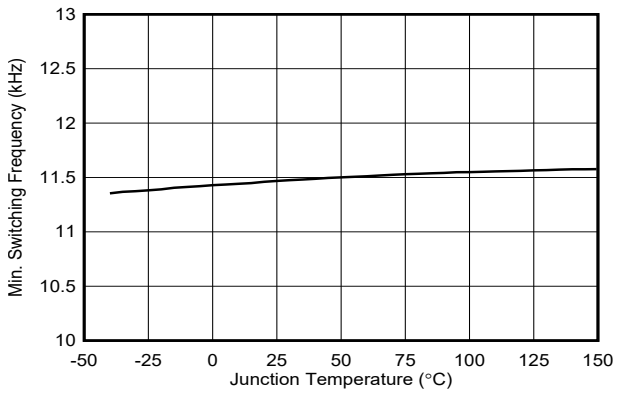


図 6-12. Minimum Switching Frequency versus Temperature

6.6 Typical Characteristics (continued)

V_{IN} = 24 V (unless otherwise stated).

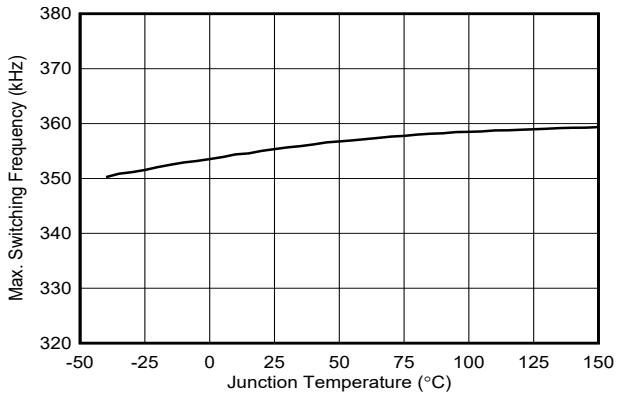


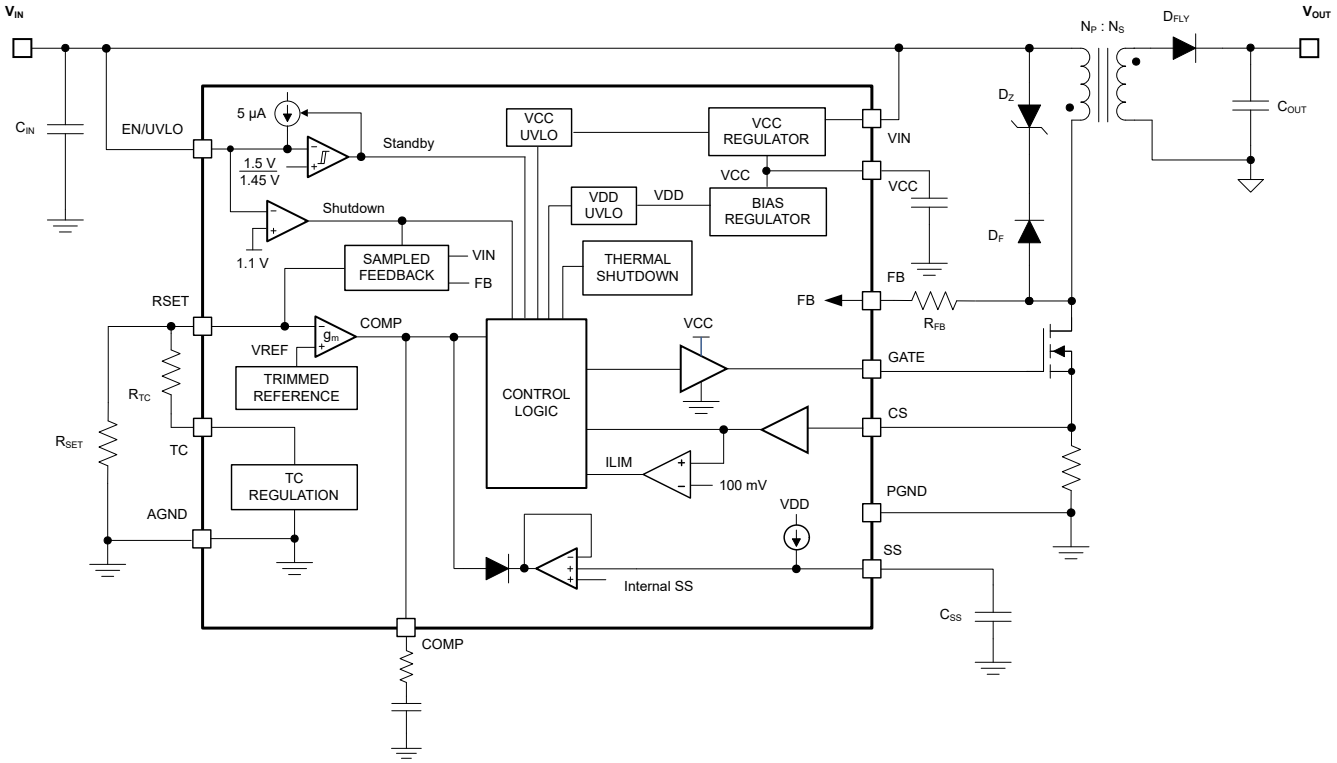
図 6-13. Maximum Switching Frequency versus Temperature

7 Detailed Description

7.1 Overview

The LM5185 primary-side regulated (PSR) flyback controller is a high-density, cost-effective design for industrial systems requiring isolated DC/DC power from less than 1 W to more than 50 W. This compact, easy-to-use flyback controller with low I_Q can be applied over a wide input voltage range from 4.5 V to 100 V. Innovative frequency and current amplitude modulation enables high conversion efficiency across the entire load and line range. Primary-side regulation of the isolated output voltage using sampled values of the primary winding voltage eliminates the need for an optocoupler or an auxiliary transformer winding for feedback. Regulation performance that rivals that of traditional optocoupler designs is achieved without the associated cost, design size, and reliability concerns. The LM5185 controller services a wide range of applications, including IGBT and SiC-based motor drives, factory automation, and medical equipment.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power MOSFET Gate Driver

The LM5185 is a flyback DC/DC controller with integrated N-channel power MOSFET gate driver that can sink a peak current of 2 A and source a peak current of 1 A. During the MOSFET on-time, the transformer primary current increases from zero with a slope of V_{IN} / L_{MAG} (where L_{MAG} is the transformer primary-referred magnetizing inductance) while the output capacitor supplies the load current. When the MOSFET is turned off by the gate driver, the switch voltage V_{SW} swings up to approximately V_{IN} + (N_{PS} × V_{OUT}), where N_{PS} = N_P/N_S is the primary-to-secondary turns ratio of the transformer. The magnetizing current flows in the secondary side through the flyback diode, charging the output capacitor and supplying current to the load. Duty cycle D is defined as t_{ON} / t_{SW}, where t_{ON} is the MOSFET conduction time and t_{SW} is the switching period.

図 7-1 shows a typical schematic of the LM5185 PSR flyback circuit. Components denoted in red are optional depending on the application requirements.

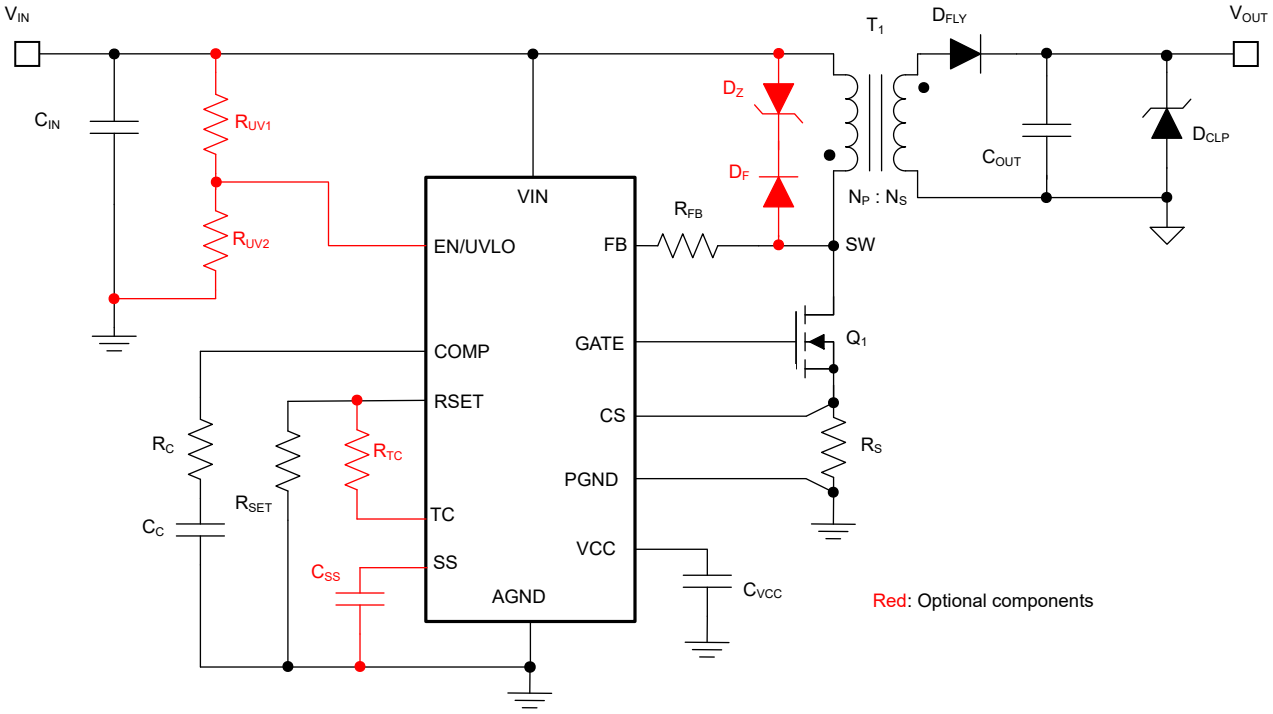


図 7-1. LM5185 Flyback Converter Schematic (Optional Components in Red)

7.3.2 PSR Flyback Modes of Operation

The LM5185 uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as illustrated in 図 7-2.

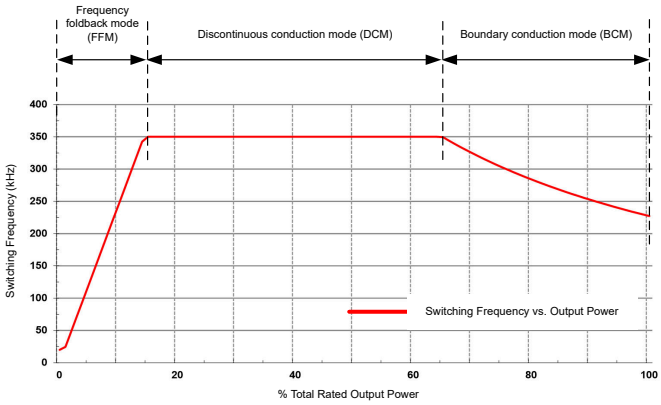


図 7-2. Three Modes of Operation Illustrated by Variation of Switching Frequency With Load

The LM5185 operates in boundary conduction mode (BCM) at heavy loads. The power MOSFET turns on when the current in the secondary winding reaches zero, and the MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the frequency increases to maintain BCM operation. 式 1 gives the duty cycle of the flyback converter in BCM.

$$D = \frac{(V_{OUT} + V_D) \times N_{PS}}{V_{IN} + (V_{OUT} + V_D) \times N_{PS}} \quad (1)$$

where

- V_D is the forward voltage drop of the flyback diode as the current approaches zero

式 2 gives the output power in BCM, where the applicable switching frequency and peak primary current are specified by 式 3 and 式 4, respectively.

$$P_{OUT(BCM)} = \frac{L_{MAG} \times I_{PRI-PK(BCM)}^2}{2} \times F_{SW(BCM)} \quad (2)$$

$$F_{SW(BCM)} = \frac{1}{I_{PRI-PK(BCM)} \times \left(\frac{L_{MAG}}{V_{IN}} + \frac{L_{MAG}}{N_{PS} \times (V_{OUT} + V_D)} \right)} \quad (3)$$

$$I_{PRI-PK(BCM)} = \frac{2 \times (V_{OUT} + V_D) \times I_{OUT}}{V_{IN} \times D} \quad (4)$$

As the load decreases, the LM5185 clamps the maximum switching frequency to 350 kHz, and the converter enters discontinuous conduction mode (DCM). The power delivered to the output in DCM is proportional to the peak primary current squared as given by 式 5 and 式 6. Thus, as the load decreases, the peak current reduces to maintain regulation at 350-kHz switching frequency.

$$P_{OUT(DCM)} = \frac{L_{MAG} \times I_{PRI-PK(DCM)}^2}{2} \times F_{SW(DCM)} \quad (5)$$

$$I_{PRI-PK(DCM)} = \sqrt{\frac{2 \times I_{OUT} \times (V_{OUT} + V_D)}{L_{MAG} \times F_{SW(DCM)}}} \quad (6)$$

$$D_{DCM} = \frac{L_{MAG} \times I_{PRI-PK(DCM)} \times F_{SW(DCM)}}{V_{IN}} \quad (7)$$

At even lighter loads, the primary-side peak current set by the internal error amplifier decreases to a minimum level of 20 mV on V_{CS}, or 20% of the 100-mV peak value, and the MOSFET gate off-time extends to maintain the output load requirement. The system operates in frequency foldback mode (FFM), and the switching frequency decreases as the load current is reduced. Other than a fault condition, the lowest frequency of operation of the LM5185 is 11 kHz, which sets a minimum load requirement of approximately 0.5% full load.

7.3.3 High Voltage VCC Regulator

The LM5185 has an internal wide input VCC regulator that provides the bias supply for the PWM controller and the gate driver for the external power MOSFET. The VCC regulator is sourced from VIN pin and allows a wide input range from 4.5 V to 100 V. When the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

At power up, the VCC regulator sources current into the capacitor connected at the VCC pin. When the VCC voltage exceeds 4.25 V (typical) and the EN/UVLO pin voltage is greater than 1.5 V (typical), the soft-start sequence begins. The output remains active unless the VCC voltage falls below the VCC UVLO falling threshold of 3.9 V (typical) or EN/UVLO is switched to a low state. Connect a ceramic capacitor from VCC to PGND. The recommended range of VCC capcitor is from 1 µF to 4.7 µF.

The LM5185 has an external VCC supply feature that reduces input quiescent current and increases efficiency. When the external VCC supply voltage is greater than the VCC regulation target, the external VCC supply powers the VCC. This external supply can be an external voltage source or from a transformer auxiliary winding as shown in 図 7-3.The VIN pin voltage must be greater than the VCC voltage when external VCC is used.

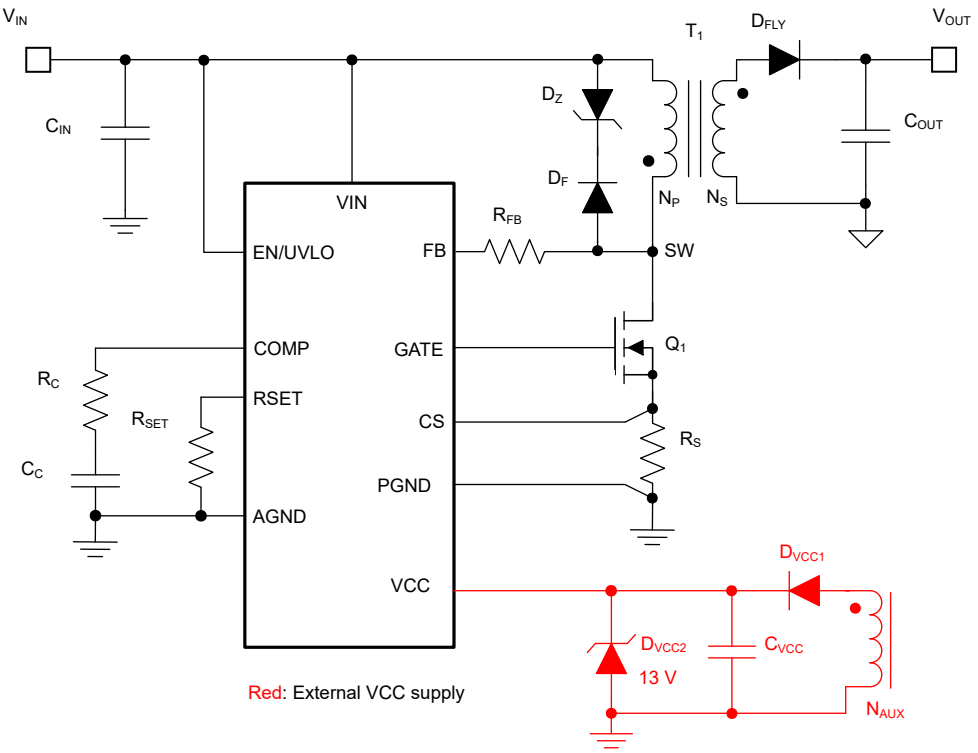


図 7-3. External VCC Supply Using Transformer Auxiliary Winding

7.3.4 Setting the Output Voltage

To minimize output voltage regulation error, the LM5185 senses the reflected secondary voltage when the secondary current reaches zero. The feedback (FB) resistor, which is connected between SW and FB, is determined using 式 8, where R_{SET} is nominally 10 kΩ.

$$R_{FB} = \left(V_{OUT} + V_D\right) \times N_{PS} \times \frac{R_{SET}}{V_{REF}} \tag{8}$$

7.3.4.1 Diode Thermal Compensation

The LM5185 employs a unique thermal compensation circuit that adjusts the feedback setpoint based on the thermal coefficient of the forward voltage drop of the flyback diode. Even though the output voltage is measured when the secondary current is effectively zero, there is still a non-zero forward voltage drop associated with the flyback diode. Select the thermal compensation resistor using 式 9.

$$R_{TC}[\text{k}\Omega] = \frac{R_{FB}[\text{k}\Omega]}{N_{PS}} \times \frac{3.8}{TC_{Diode}[\text{mV/°C}]} \tag{9}$$

The temperature coefficient of the diode voltage drop can not be explicitly provided in the diode data sheet, so the effective value can be estimated based on the measured output voltage shift over temperature when the TC resistor is not installed.

7.3.5 Control Loop Error Amplifier

The inputs of the error amplifier include a level-shifted version of the FB voltage and an internal 1-V reference set by the resistor at RSET. The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network to stabilize the converter. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. In BCM operation when the output voltage is in regulation, an on-time interval is initiated when the

secondary current reaches zero. The power MOSFET is subsequently turned off when an amplified version of the peak primary current exceeds the error amplifier output.

7.3.6 Precision Enable

The precision EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis for application specific power-up and power-down requirements. EN/UVLO connects to a comparator with a 1.5-V reference voltage and 50-mV hysteresis. An external logic signal can be used to drive the EN/UVLO input to toggle the output on and off for system sequencing or protection. The simplest way to enable the LM5185 is to connect EN/UVLO directly to V_{IN}. This connection allows the LM5185 to start up when V_{IN} is within the valid operating range. However, many applications benefit from using resistor divider R_{UV1} and R_{UV2} as shown in 図 7-4 to establish a precision UVLO level.

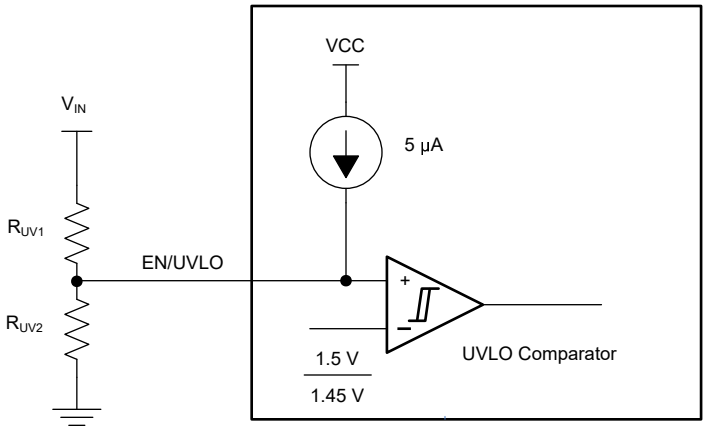


図 7-4. Programmable Input Voltage UVLO With Hysteresis

Use 式 10 and 式 11 to calculate the input UVLO voltages turn-on and turn-off voltages, respectively.

$$V_{IN(ON)} = V_{UV-RISING} \times \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (10)$$

where

- $V_{UV-RISING}$ and $V_{UV-FALLING}$ are the UVLO comparator thresholds
- $I_{UV-HYST}$ is the hysteresis current

$$V_{IN(OFF)} = V_{UV-FALLING} \times \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) - I_{UV-HYST} \times R_{UV1} \quad (11)$$

The LM5185 also provides a low-I_Q shutdown mode when the EN/UVLO voltage is pulled below a base-emitter voltage drop (approximately 0.6 V at room temperature). If the EN/UVLO voltage is below this hard shutdown threshold, the internal LDO regulator powers off, and the internal bias-supply rail collapses, shutting down the bias currents of the LM5185. The LM5185 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision-enable thresholds.

7.3.7 Configurable Soft Start

The LM5185 has a flexible and easy-to-use soft-start control pin, SS. The soft-start feature prevents inrush current impacting the LM5185 and the input supply when power is first applied. This is achieved by controlling the voltage at the output of the internal error amplifier. Soft start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. Selectable and adjustable start-up timing options include a 6-ms internally-fixed soft start and an externally-programmable soft start.

The simplest way to use the LM5185 is to leave SS open. The LM5185 employs an internal soft-start control ramp and starts up to the regulated output voltage in 6 ms.

However, in applications with a large amount of output capacitance, higher V_{OUT}, or other special requirements, the soft-start time can be extended by connecting an external capacitor C_{SS} from SS to AGND. A longer soft-start time further reduces the supply current needed to charge the output capacitors while sourcing the required load current. When the EN/UVLO voltage exceeds the UVLO rising threshold and a delay of 20 µs expires, an internal current source I_{SS} of 5 µA charges C_{SS} and generates a ramp to control the primary current amplitude. Calculate the soft-start capacitance for a desired soft-start time, t_{SS}, using 式 12.

$$C_{SS}[\text{nF}] = 5 \times t_{SS}[\text{ms}] \tag{12}$$

C_{SS} is discharged by an internal FET when switching is disabled by EN/UVLO or thermal shutdown.

7.3.8 Minimum On-Time and Off-Time

When the power MOSFET is turned off, the leakage inductance of the transformer resonates with the SW node parasitic capacitance. The resultant ringing behavior can be excessive with large transformer leakage inductance and can corrupt the secondary zero-current detection. To prevent such a situation, a minimum switch off-time, designated as $t_{OFF\text{-}MIN}$, of 400 ns, is set internally to make sure of proper functionality.

Furthermore, noise effects as a result of power MOSFET turn-on can impact the internal current sense circuit measurement. To mitigate this effect, the LM5185 provides a blanking time after the MOSFET turns on. This blanking time forces a minimum on-time, $t_{ON\text{-}MIN}$, of 125 ns.

7.3.9 Current Sensing and Overcurrent Protection

The device has a low-side current sense through the CS pin. The PWM controller and the cycle-by-cycle peak current limit protection circuit use the low-side current sense. If required, a small external RC filter at the CS pin can be added to overcome the leading edge noise of the current sense signal.

In case of an overcurrent condition on the isolated output or outputs, the output voltage drops lower than the regulation level because the maximum power delivered is limited by the peak current capability on the primary side. The peak primary current is maintained at 100 mV on V_{CS} (plus an amount related to the 100-ns propagation delay of the current limit comparator) until the output decreases to the secondary diode voltage drop to impact the reflected signal on the primary side. At this point, the LM5185 assumes the output cannot be recovered and re-calibrates the switching frequency to 9 kHz until the overload condition is removed. The LM5185 responds with similar behavior to an output short circuit condition.

For a given input voltage, 式 13 gives the maximum output current prior to the engagement of overcurrent protection. The typical threshold value for $I_{SW\text{-}PEAK}$ from the *Electrical Characteristics* is 100 mV / R_{CS}.

$$I_{OUT}(\text{max}) = \frac{\eta}{2} \times \frac{I_{SW-PEAK}}{\left(\frac{V_{OUT}}{V_{IN}} + \frac{1}{N_{PS}}\right)} \tag{13}$$

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 175°C to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the LM5185 restarts when the junction temperature falls to 165°C.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO facilitates ON and OFF control for the LM5185. When $V_{EN/UVLO}$ is below approximately 0.6 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 1.7 µA at V_{IN} = 24 V. The LM5185 also employs internal bias rail undervoltage protection. If the internal bias supply voltage is below the UV threshold, the converter remains off.

7.4.2 Standby Mode

The internal bias rail LDO regulator has a lower enable threshold than the converter itself. When $V_{EN/UVLO}$ is above 0.6 V and below the precision-enable threshold (1.5 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on after the VCC is above the UV threshold. The switching action and voltage regulation are not enabled until $V_{EN/UVLO}$ rises above the precision enable threshold.

7.4.3 Active Mode

The LM5185 is in active mode when $V_{EN/UVLO}$ is above the precision-enable threshold and the internal bias rail is above the UV threshold. The LM5185 operates in one of three modes depending on the load current requirement:

1. Boundary conduction mode (BCM) at heavy loads
2. Discontinuous conduction mode (DCM) at medium loads
3. Frequency foldback mode (FFM) at light loads

Refer to the *PSR Flyback Modes of Operation* section for more detail.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM5185 requires only a few external components to convert from a wide range of supply voltages to one or more isolated output rails. To expedite and streamline the process of designing of a LM5185-based converter, a comprehensive quick-start calculator is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for a single-output implementations using a specific circuit design example.

As mentioned previously, the LM5185 also integrates several optional features to meet system design requirements, including precision enable, input UVLO, programmable soft start, output voltage thermal compensation, adjustable peak current limit, compensation network, and external VCC supply connection. Each application incorporates these features as needed for a more comprehensive design.

The application circuits detailed in the *Typical Applications* show LM5185 configuration options designed for several application use cases. Refer to the *LM5185EVM-SIO* user's guide for more detail.

8.2 Typical Applications

For step-by-step design procedures, circuit schematics, bill of materials, PCB files, simulation and test results of LM5185-powered implementations, refer to the *TI Reference Design* library.

8.2.1 Design 1: Wide V_{IN}, Low I_Q PSR Flyback Converter Rated at 16.4 V, 1 A

図 8-1 shows the schematic diagram of a 16.4-V, 1-A PSR flyback converter.

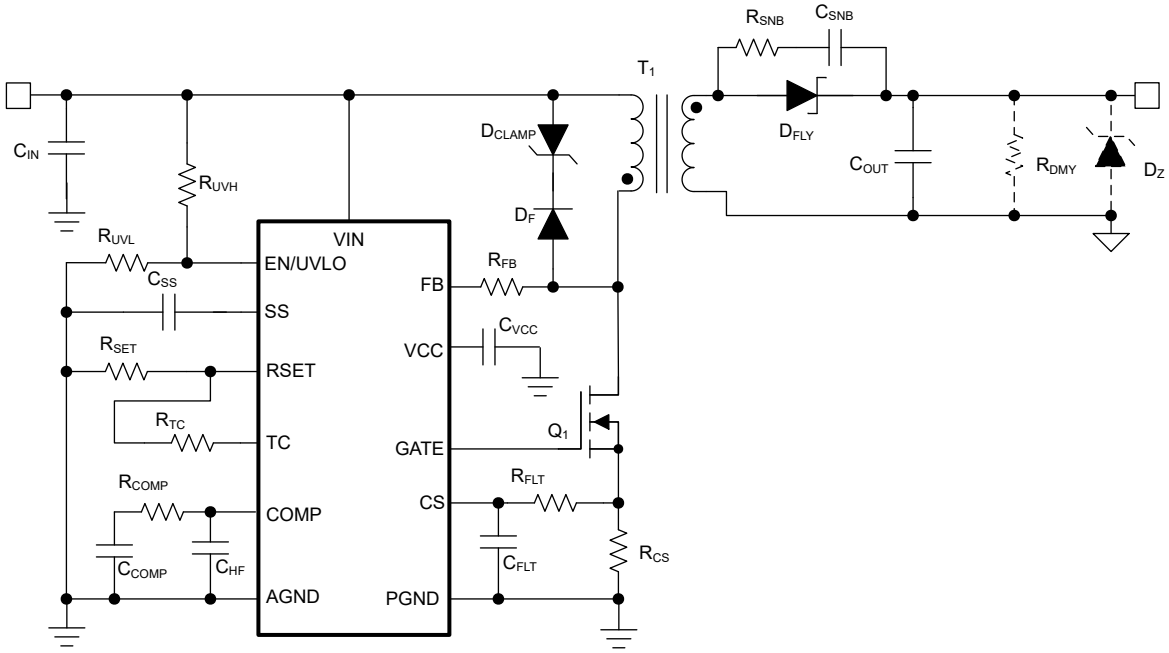


図 8-1. Schematic for Design 1 With V_{IN} = 20 V to 60 V, V_{OUT} = 16.4 V, I_{OUT} = 1 A

8.2.1.1 Design Requirements

表 8-1 shows the required input, output, and performance parameters for this application example.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range	20 V to 60 V
Input UVLO thresholds	19 V on, 18 V off
Output voltage	16.4 V
Rated load current	1 A
Output voltage regulation	±1.5%

The target full-load efficiency is 89% based on a nominal input voltage of 24 V and an isolated output voltage of 16.4 V. The LM5185 is chosen to deliver a fixed 16.4-V output voltage set by resistor R_{FB} connected between the SW and FB pins. The input voltage turn-on and turn-off thresholds are established by R_{UV1} and R_{UV2}. Refer to the *LM5185-Q1 Single-Isolated-Output Evaluation Module* user's guide for the detailed component list.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5185 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Custom Design With Excel Quickstart Tool

Select components based on the converter specifications using the LM5185 quick-start calculator.

8.2.1.2.3 Flyback Transformer T_1 and Current-Sense Resistor (R_{CS})

The turns ratio of the transformer is selected such that the maximum duty cycle is smaller than 70%. While the maximum duty cycle can approach 80% if needing a particularly wide input voltage application, the maximum duty cycle increases the peak current stress of the secondary-side components. The turns ratio for this design is 1:1.

$$N_{PS} < \frac{D_{MAX}}{1 - D_{MAX}} \times \frac{V_{IN(min)}}{V_{OUT} + V_D} = \frac{0.7}{1 - 0.7} \times \frac{20\ \text{V}}{16.4\ \text{V} + 0.3\ \text{V}} = 2.8 \quad (14)$$

The magnetizing inductance is selected based on the switching frequency being 250 kHz for the nominal V_{IN} at 24 V at full load 1 A. The 250 kHz is usually a good tradeoff for flyback design in terms of transformer size and overall efficiency, and so forth. Use 式 1, 式 4, and 式 3 to calculate the required inductance. A value of 12 µH is chosen for this design. Use 式 4 to calculate the primary peak current and the peak current with the selected 12-µH 1:1 transformer is 3.7 A. By giving a 15% margin, the peak current limit is around 4.3 A. Use 式 15 to calculate the R_{CS}. In this design, R_{CS} is set to 20 mΩ. A small RC filter (100 Ω, 100 pF) is added to overcome the leading edge noise of the current sense signal.

$$R_{CS} \leq \frac{V_{CS-MAX}}{I_{pk}} = \frac{100\text{mV}}{4.3\text{A}} = 23.3m\Omega \quad (15)$$

Note that a higher magnetizing inductance provides a larger operating range for BCM and FFM, but the leakage inductance can increase based on a higher number of primary turns, N_P. 式 16 and 式 17 give the primary and secondary winding RMS currents, respectively.

$$I_{PRI-RMS} = \sqrt{\frac{D}{3}} \times I_{PRI-PK} \quad (16)$$

$$I_{SEC-RMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRI-PK} \times N_{PS}}{3}} \quad (17)$$

8.2.1.2.4 Flyback Diode – D_{FLY}

The flyback diode reverse voltage is given by 式 18.

$$V_{D-REV} \geq \frac{V_{IN(MAX)}}{N_{PS}} + V_{OUT} = \frac{60\text{ V}}{1} + 16.4\text{ V} = 76.4\text{ V} \quad (18)$$

Select a 100-V, 5-A Schottky diode for this application to account for inevitable diode voltage overshoot and ringing related to the resonance of transformer leakage inductance and diode parasitic capacitance. Connect an appropriate RC snubber circuit (for example, 100 Ω and 150 pF) across the flyback diode if needed, particularly if the transformer leakage inductance is high. Also, choose a flyback diode with current rating that aligns with the maximum peak secondary winding current of $N_{PS} \times I_{SW-PEAK}$.

8.2.1.2.5 Leakage Inductance Clamp Circuit – D_F, D_{CLAMP}

Connect a diode-Zener clamp circuit across the primary winding to limit the peak switch voltage after MOSFET turnoff below the maximum level of the external MOSFET rating.

Choose a 28-V Zener diode for D_{CLAMP} to give a clamp voltage of approximately 1.5 times the reflected output voltage, as specified by 式 19. This action provides a balance between the maximum switch voltage excursion and the leakage inductance demagnetization time. Select a Zener diode with low package parasitic inductance to manage the high slew-rate current during the switch turn-off transition.

$$V_{DZ(clamp)} = 1.5 \times N_{PS} \times (V_{OUT} + V_D) = 1.5 \times 1 \times (16.4\text{ V} + 0.4\text{ V}) = 25.2\text{ V} \quad (19)$$

Choose an ultra-fast switching diode or Schottky diode for D_F with reverse voltage rating greater than the maximum input voltage.

8.2.1.2.6 Feedback Resistor – R_{FB}

Select a feedback resistor, designated R_{FB}, of 166 kΩ based on the secondary winding voltage at the end of the flyback conduction interval (the sum of the 16.4-V output voltage and the Schottky diode forward voltage drop as the current approaches zero) reflected by the transformer turns ratio of 1:1.

$$R_{FB} = \frac{(V_{OUT} + V_D) \times N_{PS}}{0.1\text{ mA}} = \frac{(16.4\text{ V} + 0.2\text{ V}) \times 1}{0.1\text{ mA}} = 166\text{ k}\Omega \quad (20)$$

8.2.1.2.7 Thermal Compensation Resistor – R_{TC}

Select a resistor for output voltage thermal compensation, designated R_{TC}, based on 式 21. The 294-kΩ resistor is selected for this design.

$$R_{TC}[\text{k}\Omega] = \frac{R_{FB}[\text{k}\Omega]}{N_{PS}} \times \frac{3.8}{TC_{Diode}[\text{mV/°C}]} = \frac{166 \times 3.8}{1 \times 2.1} = 300\text{k}\Omega \quad (21)$$

8.2.1.2.8 UVLO Resistors – R_{UV1}, R_{UV2}

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turn-on and turn-off thresholds of 19.3 V and 17.6 V, respectively, select the upper and lower UVLO resistors using the following expressions:

$$R_{UV1} = \frac{V_{IN(on)} \times \frac{V_{UV-FALLING}}{V_{UV-RISING}} - V_{IN(off)}}{I_{UV-HYST}} = \frac{19.3\ \text{V} \times \frac{1.45\ \text{V}}{1.5\ \text{V}} - 17.6\ \text{V}}{5\ \mu\text{A}} = 212\ \text{k}\Omega \quad (22)$$

$$R_{UV2} = R_{UV1} \times \frac{V_{UV-RISING}}{V_{IN(on)} - V_{UV-RISING}} = 212\ \text{k}\Omega \times \frac{1.5\ \text{V}}{19.3\ V - 1.5\ V} = 17.9\ \text{k}\Omega \quad (23)$$

The nearest standard E96 resistor values for R_{UV1} and R_{UV2} are 200 kΩ and 16.9 kΩ, respectively. Calculate the actual input voltage turn-on and turn-off thresholds as follows:

$$V_{IN(on)} = V_{UV-RISING} \times \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) = 1.5\ \text{V} \times \left(1 + \frac{200\ \text{k}\Omega}{16.9\ \text{k}\Omega}\right) = 19.25\ \text{V} \quad (24)$$

$$V_{IN(off)} = V_{UV-FALLING} \times \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) - I_{UV-HYST} \times R_{UV1} = 1.45\ \text{V} \times \left(1 + \frac{200\ \text{k}\Omega}{16.9\ \text{k}\Omega}\right) - 5\ \mu\text{A} \times 200\ \text{k}\Omega = 17.61\ \text{V} \quad (25)$$

8.2.1.2.9 Soft-Start Capacitor – C_{SS}

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 100 nF based on 式 12 to achieve a soft-start time of 20 ms.

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power Management* technical articles.

8.2.1.2.10 Compensation Components

Choose compensation components for a stable control loop using the procedure outlined as follows.

First, calculate the power stage transfer function with 式 26. L_{mag} is the magnetizing inductance of the transformer. C_{out} is the output capacitance. R_{load} is the load resistance.

$$G_{pw}(s) = A_M \times A_{CS} \times \frac{\left(1 - \frac{s}{\omega_{zRHP}}\right)\left(1 + \frac{s}{\omega_{zESR}}\right)}{1 + \frac{s}{\omega_p}} \quad (26)$$

where

$$A_M = \frac{R_{load} \times N_{ps} \times (1 - D)}{2 \times (1 + D)} \quad (27)$$

$$A_{CS} = \frac{1}{10 \times R_{CS}} \quad (28)$$

$$\omega_{zRHP} = \frac{(1 - D)^2}{D} \frac{R_{load} \times N_{ps}^2}{L_{mag}} \quad (29)$$

$$\omega_{zESR} = \frac{1}{C_{out} \times R_{ESR}} \quad (30)$$

$$\omega_p = \frac{1 + D}{C_{out} \times R_{load}} \quad (31)$$

Next, use 式 32 to calculate the power stage gain at the cross-over frequency F_{co} which is selected to be 1 kHz for this design.

$$Gain(F_{co}) = 20 \times \log\left(\left|G_{pw}\left(2j \times \pi \times F_{co}\right)\right|\right) \quad (32)$$

Select R_{COMP} to satisfy the desired cross-over frequency.

$$R_{COMP} = \frac{10^{-\frac{Gain(F_{co})}{20}}}{g_m} R_{FB} \frac{100\ \mu A}{V_{ref}} \quad (33)$$

Select C_{COMP} to set the compensator zero at 2 times of the load pole.

$$C_{COMP} = \frac{1}{2 \times \omega_p \times R_{COMP}} \quad (34)$$

Select C_{HF} to set the compensator pole at 50 to 200 times the compensator zero.

$$C_{HF} = \frac{C_{COMP}}{150} \quad (35)$$

8.2.1.3 Application Curves

Unless otherwise stated, application performance curves were taken at T_A = 25°C.

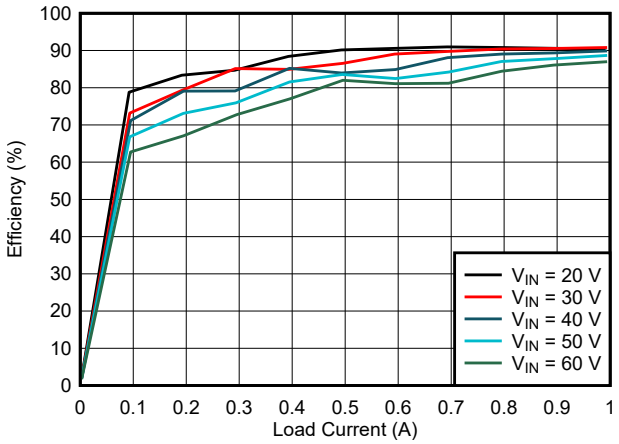


図 8-2. Efficiency

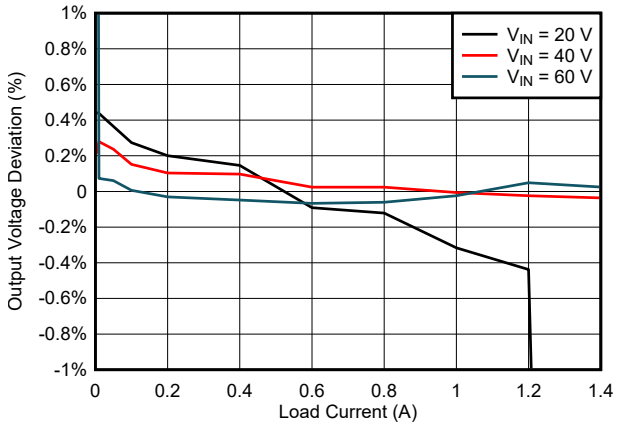
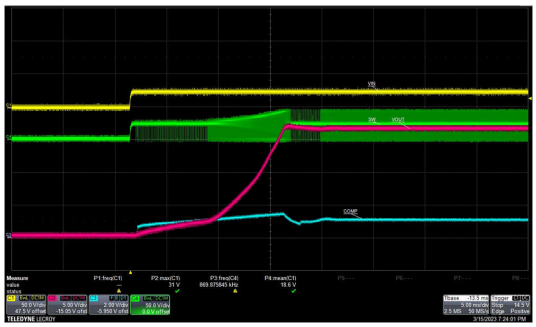
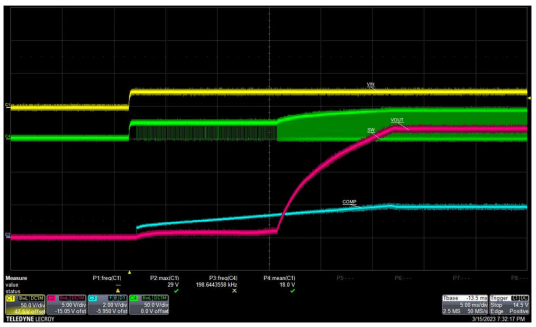


図 8-3. Load Regulation



VIN stepped to 24 V　　0-A Load

図 8-4. Start-Up Characteristic at No Load



VIN stepped to 24 V　　1-A Load

図 8-5. Start-Up Characteristic at Full Load

8.3 Power Supply Recommendations

The LM5185 flyback controller operates over a wide input voltage range from 4.5 V to 100 V. The characteristics of the input supply must be compatible with the design specification ranges. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with 式 36.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{36}$$

where

- η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum electrolytic input capacitor in parallel with the ceramics.

The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 22 µF to 100 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients. A typical ESR of 200 mΩ provides enough damping for most input circuit configurations.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

8.4 Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

8.4.1 Layout Guidelines

PCB layout is critical for good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with transformer leakage inductance or parasitic capacitance to generate noise and EMI or degrade the performance of the power supply.

1. Bypass VIN to GND with a low-ESR ceramic capacitor, preferably of X7R or X7S dielectric. Place C_{IN} as close as possible to the LM5185 VIN and GND pins. Ground return paths for the input capacitor or capacitors must consist of localized top-side planes that connect to the GND pin and exposed PAD.
2. Minimize the loop area formed by the input capacitor connections and the VIN and GND pins.
3. Locate the transformer close to the switch node. Minimize the area of the switch trace or plane to prevent excessive e-field or capacitive coupling.
4. Minimize the loop area formed by the diode-Zener clamp circuit connections and the primary winding terminals of the transformer.
5. Minimize the loop area formed by the flyback rectifying diode, output capacitor, and the secondary winding terminals of the transformer.
6. Tie the GND pin directly to the DAP under the device and to a heat-sinking PCB ground plane.
7. Use a ground plane in one of the middle layers as a noise shielding and heat dissipation path.
8. Have a single-point ground connection to the plane. Route the return connections for the reference resistor, soft start, and enable components directly to the GND pin. This guidelines prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
9. Make V_{IN+}, V_{OUT+}, and ground bus connections short and wide. This guidelines reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
10. Minimize trace length to the FB pin. Locate the feedback resistor close to the FB pin.
11. Locate components R_{SET}, R_{TC}, and C_{SS} as close as possible to their respective pins. Route with minimal trace lengths.
12. Place a capacitor between input and output return connections to route common-mode noise currents directly back to their source.
13. Provide adequate heatsinking for the LM5185 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the DAP to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. The connection to V_{OUT+} provides heatsinking for the flyback diode.

8.4.2 Layout Examples

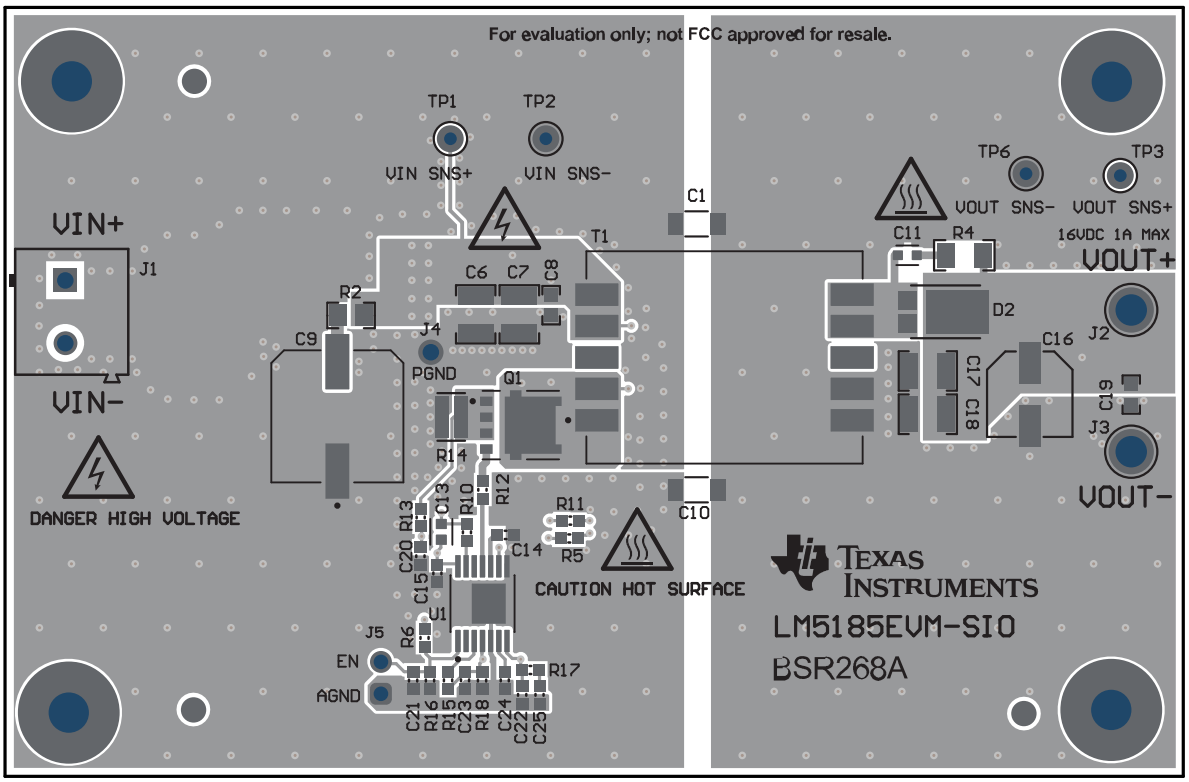


図 8-6. Single-Output PCB Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

Besides the PSR flyback controller family, TI also provides the PSR flyback converter family which have integrated MOSFET. With input voltage range and current capability as specified in 表 9-1, the PSR flyback DC/DC converter family of parts from TI provides flexibility, scalability and optimized design size for a range of applications. Note that the converter devices are not pin-to-pin compatible with the controller devices.

Using an 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch, these converters enable isolated DC/DC designs with high density and low component count.

表 9-1. PSR Flyback DC/DC Converter Family

PSR FLYBACK DC/DC CONVERTER	INPUT VOLTAGE RANGE	PEAK SWITCH CURRENT	MAXIMUM LOAD CURRENT, V_{OUT} = 12 V, N_{PS} = 1	
			V_{IN} = 4.5 V	V_{IN} = 13.5 V
LM5181	4.5 V to 65 V	0.75 A	90 mA	180 mA
LM5180	4.5 V to 65 V	1.5 A	180 mA	360 mA
LM25180	4.5 V to 42 V	1.5 A	180 mA	360 mA
LM25183	4.5 V to 42 V	2.5 A	300 mA	600 mA
LM25184	4.5 V to 42 V	4.1 A	500 mA	1 A

For development support, see the following:

- LM5185*Quick-start Calculator*.
- LM5185 *Simulation Models*.
- For TI's reference design library, visit TI Designs.
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center.
- To view a related device of this product, see the LM25185 product page.
- TI Designs:
  - *Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller*
  - *Compact, Efficient, 24-V Input Auxiliary Power Supply Reference Design for Servo Drives*
  - *Reference Design for Power-Isolated Ultra-Compact Analog Output Module*
  - *HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design*
  - *4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers*
  - *Channel-to-Channel Isolated Analog Input Module Reference Design*
  - *SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET*
  - *>95% Efficiency, 1-kW Analog Control AC/DC Reference Design for 5G Telecom Rectifier*
  - *3.5-W Automotive Dual-output PSR Flyback Regulator Reference Design*
- TI Technical Articles:
  - *Flyback Converters: Two Outputs are Better Than One*
  - *Common Challenges When Choosing the Auxiliary Power Supply for Your Server PSU*
  - *Maximizing PoE PD Efficiency on a Budget*

9.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5185 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LM25184 Single-Output EVM User's Guide*
- Texas Instruments, *LM5180 Single-Output EVM User's Guide*
- Texas Instruments, *LM5180 Dual-Output EVM User's Guide*
- Texas Instruments, *How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density analog design journal*
- Texas Instruments, *Why Use PSR-Flyback Isolated Converters in Dual-Battery mHEV Systems analog design journal*
- Texas Instruments, *IC Package Features Lead to Higher Reliability in Demanding Automotive and Communications Equipment Systems application brief*
- Texas Instruments, *PSR Flyback DC/DC Converter Transformer Design for mHEV Applications application brief*
- Texas Instruments, *Flyback Transformer Design Considerations for Efficiency and EMI*
- Texas Instruments, *Under the Hood of Flyback SMPS Designs*
- White Papers:
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
- Texas Instruments, *Using New Thermal Metrics application report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics application report*
- Texas Instruments, *AN-2162: Simple Success with Conducted EMI from DC-DC Converters application report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントを工キスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages have mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5185PWPR	ACTIVE	HTSSOP	PWP	14	3000	RoHS & Green	NIPDAU	Level-3-260C-168HRS	-40 to 125	LM5185	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

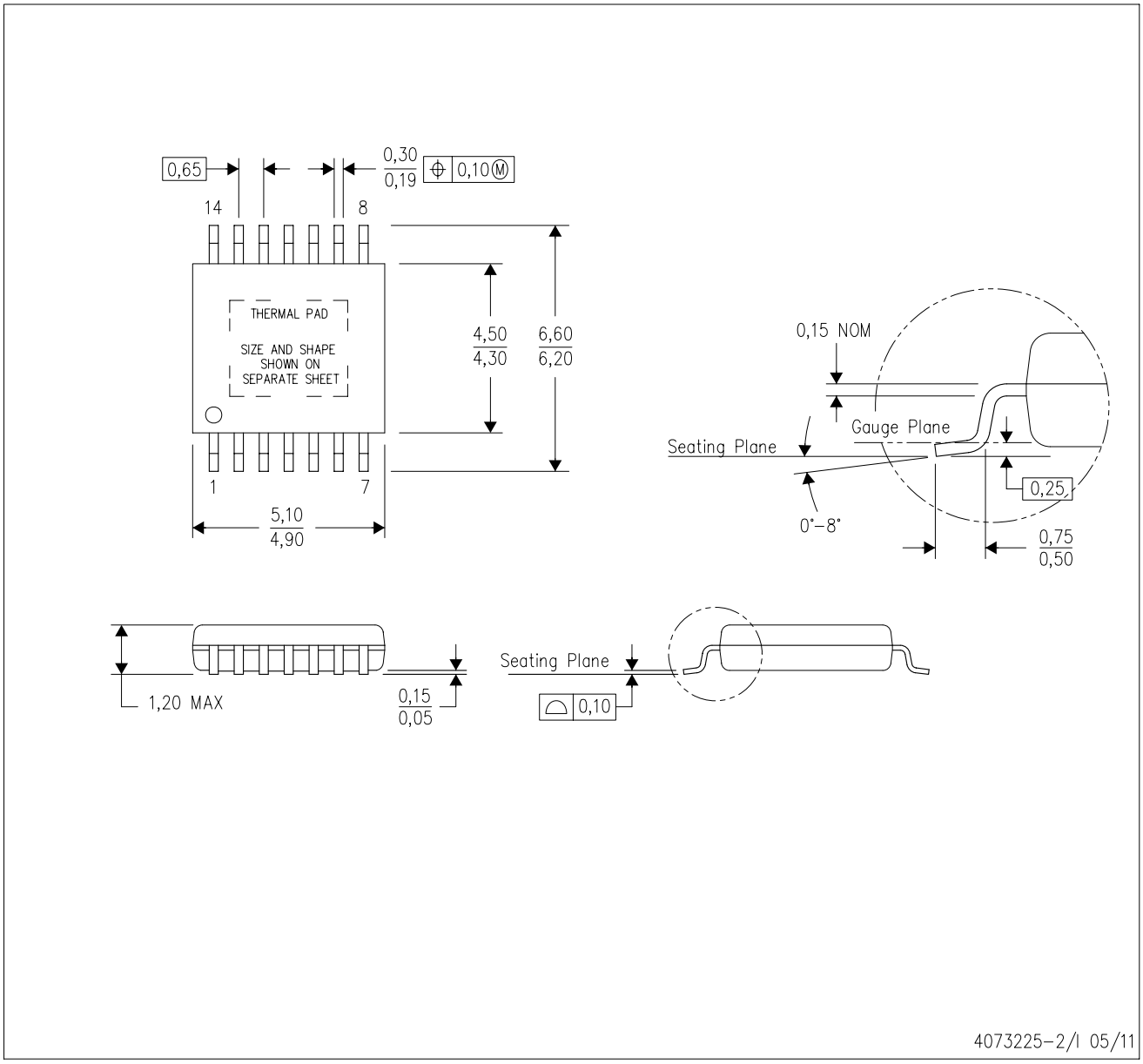
OTHER QUALIFIED VERSIONS OF LM5185 :

- Automotive : LM5185-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

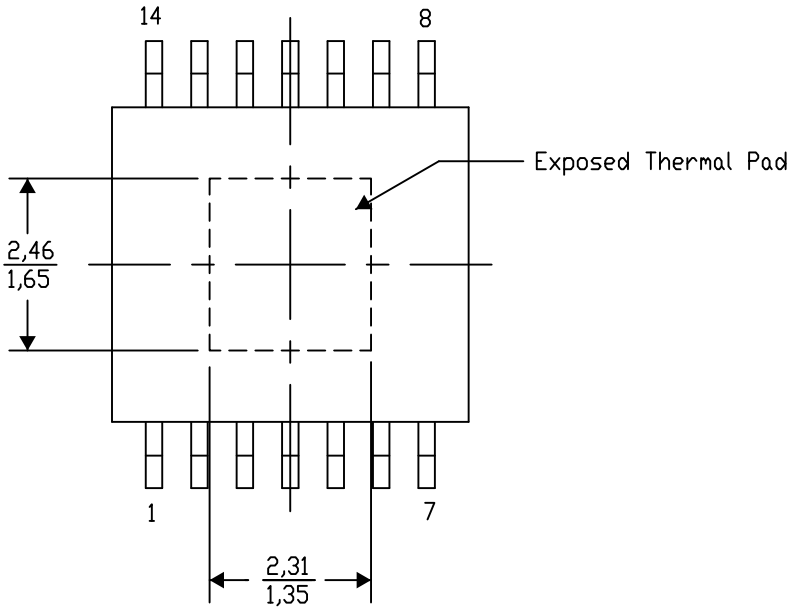
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

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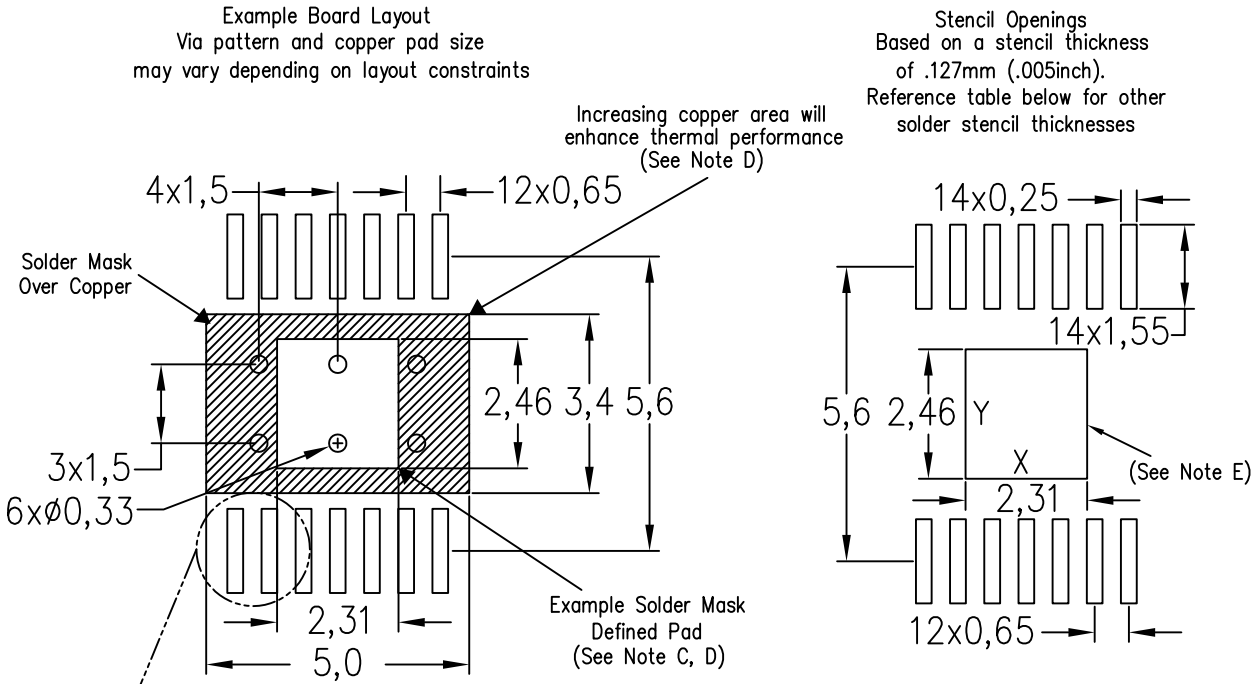
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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