LM567x トーン・デコーダ

1 特長

- 1 つの外付け抵抗による 20:1 の周波数範囲
- 100mA の電流シンク能力を備えたロジック互換出力
- 0～14% に調整可能な帯域幅
- 大きい帯域外信号およびノイズ除去比
- 誤信号に対する耐性
- 非常に安定した中心周波数
- 0.01Hz～500kHz に調整可能な中心周波数

2 アプリケーション

- タッチ・トーンのデコード処理
- 高精度の発振器
- 周波数の監視と制御
- 広帯域 FSK 復調
- 超音波の制御
- 搬送電流の遠隔制御
- 通信のページング・デコーダ

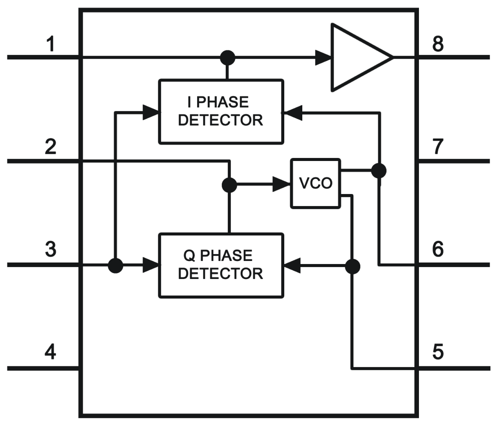
3 概要

LM567 と LM567C は、通過帯域内に入力信号が存在する場合、グランドに接続された飽和トランジスタ・スイッチがオンするように設計された汎用トーン・デコーダです。この回路は、デコーダの中心周波数を決定する電圧制御発振器によって駆動される I および Q 検出器で構成されます。外付け部品を使って中心周波数、帯域幅、出力遅延を独立して設定できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LM567C	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略ブロック図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Device Comparison ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 Recommended Operating Conditions ... 4
7.3 Thermal Information ... 4
7.4 Electrical Characteristics ... 5
7.5 Typical Characteristics ... 6
8 Parameter Measurement Information ... 8
9 Detailed Description ... 8
9.1 Overview ... 8
9.2 Functional Block Diagram ... 8
9.3 Feature Description ... 9
9.4 Device Functional Modes ... 10
10 Application and Implementation ... 12
10.1 Application Information ... 12
10.2 Typical Applications ... 12
11 Power Supply Recommendations ... 18
12 Layout ... 18
12.1 Layout Guidelines ... 18
12.2 Layout Example ... 18
13 Device and Documentation Support ... 19
13.1 Receiving Notification of Documentation Updates ... 19
13.2 サポート・リソース ... 19
13.3 Trademarks ... 19
13.4 Electrostatic Discharge Caution ... 19
13.5 Glossary ... 19
14 Mechanical, Packaging, and Orderable Information ... 19

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2014) to Revision F (January 2022) — **Page**

- Changed the pin number of 5 and 6 in the Pin Functions table ... 3
- Changed 式 1 ... 9
- Changed 式 2 ... 13

Changes from Revision D (March 2013) to Revision E (October 2014) — **Page**

- 「ピン構成および機能」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

Changes from Revision C (March 2013) to Revision D (March 2013) — **Page**

- Changed layout of National Data Sheet to TI format ... 9

5 Device Comparison

表 5-1. Device Comparison

DEVICE NAME	DESCRIPTION
LM567, LM567C	General Purpose Tone Decoder
LMC567	Same as LM567C, but lower power supply current consumption and double oscillator frequency

6 Pin Configuration and Functions

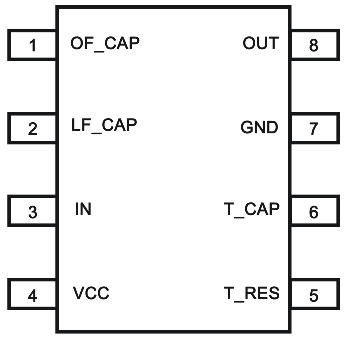


図 6-1. 8-Pin PDIP (P) and SOIC (D) Package Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	7	P	Circuit ground.
IN	3	I	Device input.
LF_CAP	2	I	Loop filter capacitor pin (LPF of the PLL).
OUT	8	O	Device output.
OF_CAP	1	I	Output filter capacitor pin.
T_CAP	6	I	Timing capacitor connection pin.
T_RES	5	I	Timing resistor connection pin.
VCC	4	P	Voltage supply pin.

7 Specifications

7.1 Absolute Maximum Ratings

See [(1)] [(2)]

			MIN	MAX	UNIT
Supply Voltage Pin				9	V
Power Dissipation[(1)]				1100	mW
V_8				15	V
V_3				−10	V
V_3				V_4 + 0.5	V
Operating Temperature Range	LM567CM, LM567CN		0	70	°C
	PDIP Package	Soldering (10 s)		260	°C
	SOIC Package	Vapor Phase (60 s)		215	°C
		Infrared (15 s)		220	°C
Storage temperature range, T_{stg}			−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Recommended Operating Conditions. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) See http://www.ti.com for other methods of soldering surface mount devices.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	3.5	8.5	V
V_{IN}	Input Voltage Level	–8.5	8.5	V
T_A	Operating Temperature Range	–20	120	°C

7.3 Thermal Information

THERMAL METRIC[(1)]		LM567C D (SOIC) 8 PINS	LM567C P (PDIP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	53.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.6	42.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	30.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.0	19.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.0	30.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, (SPRA953).

7.4 Electrical Characteristics

AC Test Circuit, T_A = 25°C, V^+ = 5 V

PARAMETER	TEST CONDITIONS	LM567			LM567C/LM567CM			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 – 6.75 V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75 – 5.75 V)	0 < T_A < 70 −55 < T_A < +125		35 ± 60 35 ± 140			35 ± 60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75 V – 6.75 V 4.75 V – 9 V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15 V		0.01	25		0.01	25	µA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

(1) The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the DIP package must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the SOIC package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

7.5 Typical Characteristics

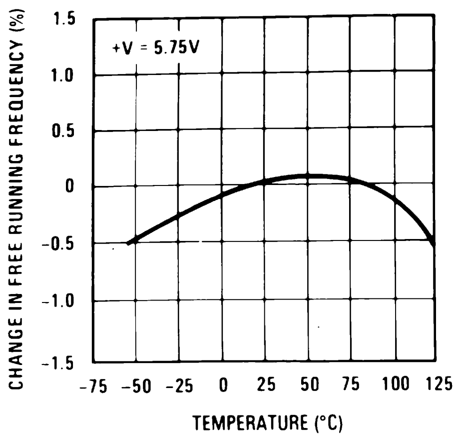


図 7-1. Typical Frequency Drift

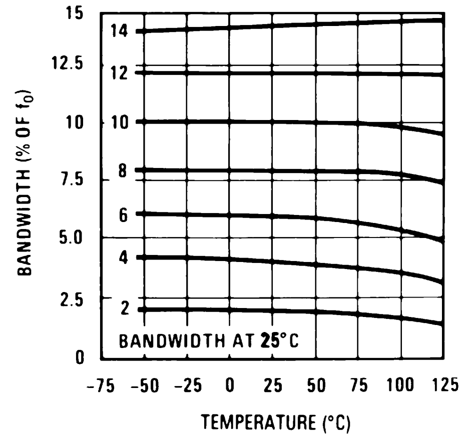


図 7-2. Typical Bandwidth Variation

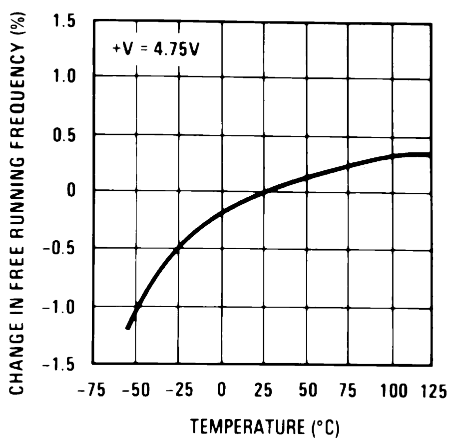


図 7-3. Typical Frequency Drift

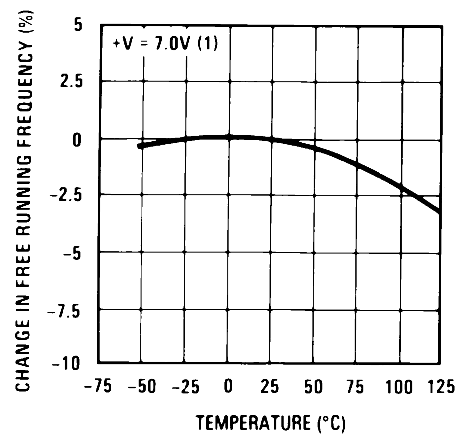


図 7-4. Typical Frequency Drift

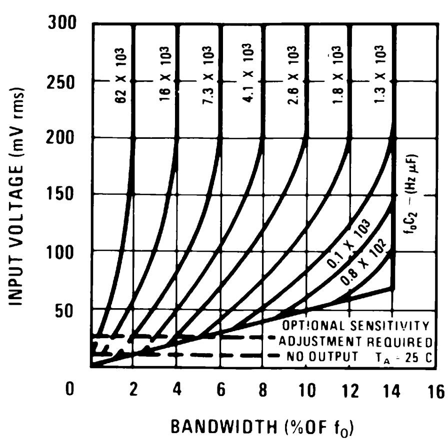


図 7-5. Bandwidth vs Input Signal Amplitude

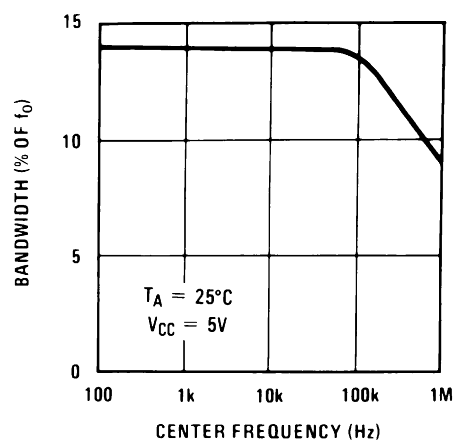


図 7-6. Largest Detection Bandwidth

7.5 Typical Characteristics (continued)

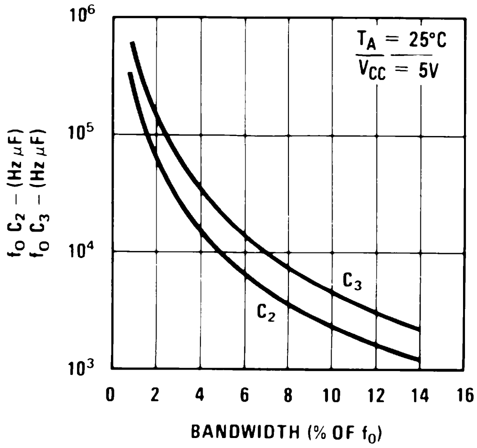


図 7-7. Detection Bandwidth as a Function of C_2 and C_3

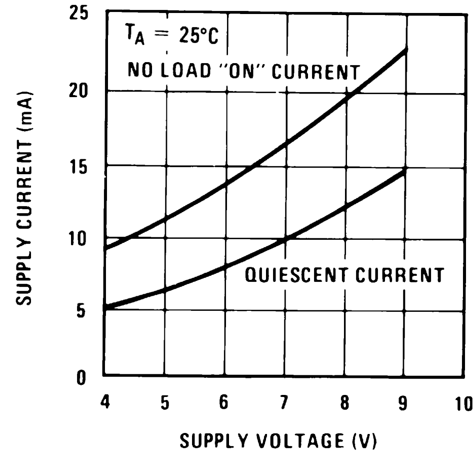


図 7-8. Typical Supply Current vs Supply Voltage

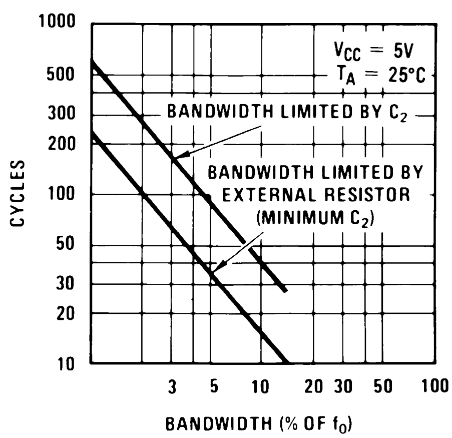


図 7-9. Greatest Number of Cycles Before Output

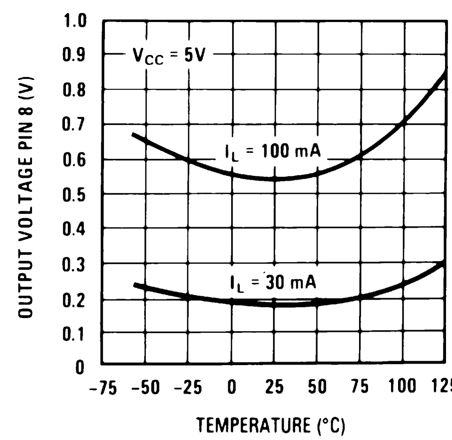


図 7-10. Typical Output Voltage vs Temperature

8 Parameter Measurement Information

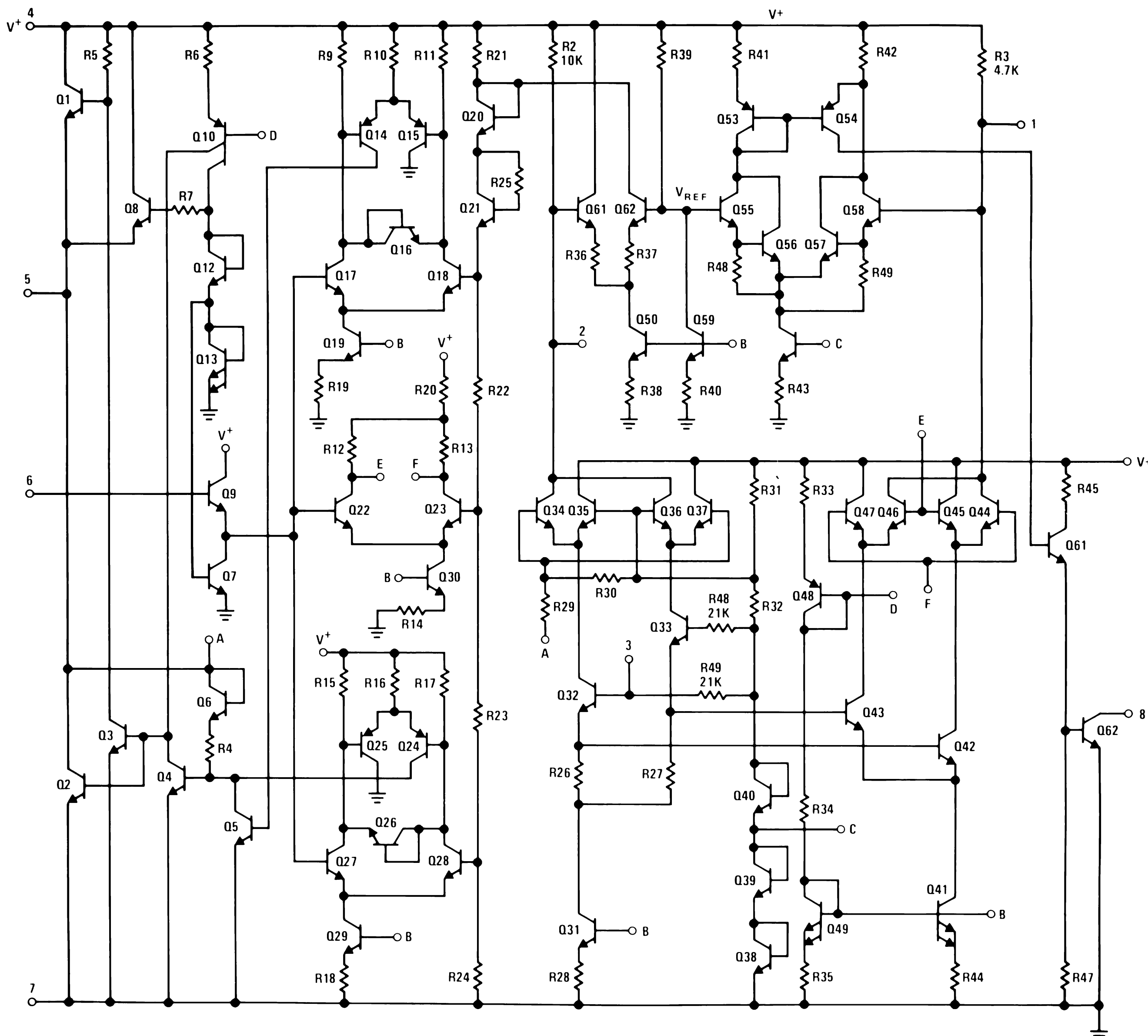
All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The LM567C is a general purpose tone decoder. The circuit consists of I and Q detectors driven by a voltage controlled oscillator which determines the center frequency of the decoder. This device is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. Center frequency is set by an external timing circuit composed by a capacitor and a resistor. Bandwidth and output delay are set by external capacitors.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Center Frequency

The center frequency of the LM567 tone decoder is equal to the free running frequency of the voltage controlled oscillator. In order to set this frequency, external components should be placed externally. The component values are given by:

$$f_o \simeq 1 / (1.1 \times R_1 \times C_1) \quad (1)$$

where

- R_1 = Timing Resistor
- C_1 = Timing Capacitor

9.3.2 Output Filter

To eliminate undesired signals that could trigger the output stage, a post detection filter is featured in the LM567C. This filter consists of an internal resistor (4.7K-Ω) and an external capacitor. Although typically external capacitor value is not critical, it is recommended to be at least twice the value of the loop filter capacitor. If the output filter capacitor value is too large, the turn-on and turn off-time of the output will present a delay until the voltage across this capacitor reaches the threshold level.

9.3.3 Loop Filter

The phase locked loop (PLL) included in the LM567 has a pin for connecting the low pass loop filter capacitor. The selection of the capacitor for the filter depends on the desired bandwidth. The device bandwidth selection is different according to the input voltage level. Refer to the *Operation With V_i < 200m – V_{RMS}* section and the *Operation With V_i > 200m – V_{RMS}* section for more information about the loop filter capacitor selection.

9.3.4 Logic Output

The LM567 is designed to provide a transistor switch to ground output when the input signal frequency matches the center frequency pass band. The logic output is an open collector power transistor that requires an external load resistor that is used to regulate the output current level.

9.3.5 Die Characteristics

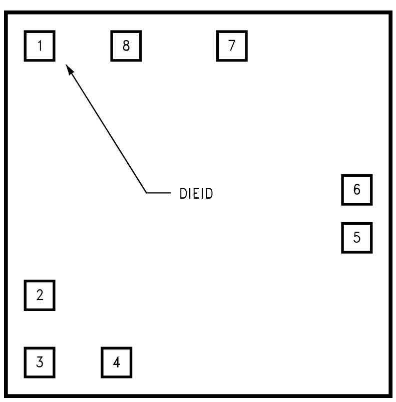


図 9-1. Die Layout (C - Step)

表 9-1. Die and Wafer Characteristics

Fabrication Attributes		General Die Information	
Physical Die Identification	LM567C	Bond Pad Opening Size (min)	91µm x 91µm
Die Step	C	Bond Pad Metalization	0.5% COPPER_BAL. ALUMINUM
Physical Attributes		Passivation	VOM NITRIDE
Wafer Diameter	150mm	Back Side Metal	BARE BACK
Dise Size (Drawn)	1600µm x 1626µm 63.0mils x 64.0mils	Back Side Connection	Floating
Thickness	406µm Nominal		
Min Pitch	198µm Nominal		
Special Assembly Requirements:			
Note: Actual die size is rounded to the nearest micron.			

Die Bond Pad Coordinate Locations (C - Step)						
(Referenced to die center, coordinates in µm) NC = No Connection, N.U. = Not Used						
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
OUTPUT FILTER	1	-673	686	91	x	91
LOOP FILTER	2	-673	-419	91	x	91
INPUT	3	-673	-686	91	x	91
V+	4	-356	-686	91	x	91
TIMING RES	5	673	-122	91	x	91
TIMING CAP	6	673	76	91	x	91
GND	7	178	686	117	x	91
OUTPUT	8	-318	679	117	x	104

9.4 Device Functional Modes

9.4.1 Operation With V_i < 200m – V_{RMS}

When the input signal is below a threshold voltage, typically 200m-VRMS, the bandwidth of the detection band should be calculated 式 2.

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

where

- V_i = Input voltage (volts rms), $V_i \le 200mV$
- C_2 = Capacitance at Pin 2(µF)

9.4.2 Operation With V_i > 200m – V_{RMS}

For input voltages greater than 200m-VRMS, the bandwidth depends directly from the loop filter capacitance and free running frequency product. Bandwidth is represented as a percentage of the free running frequency, and according to the product of f0·C2, it can have a variation from 2 to 14%. 表 9-2 shows the approximate values for bandwidth in function of the product result.

表 9-2. Detection Bandwidth in Function of $f_o \times C_2$

$f_o \times C_2$ (kHzµF)	Bandwidth (% of f_o)
62	2
16	4
7.3	6
4.1	8
2.6	10
1.8	12
1.3	14
< 1.3	14

10 Application and Implementation

Note

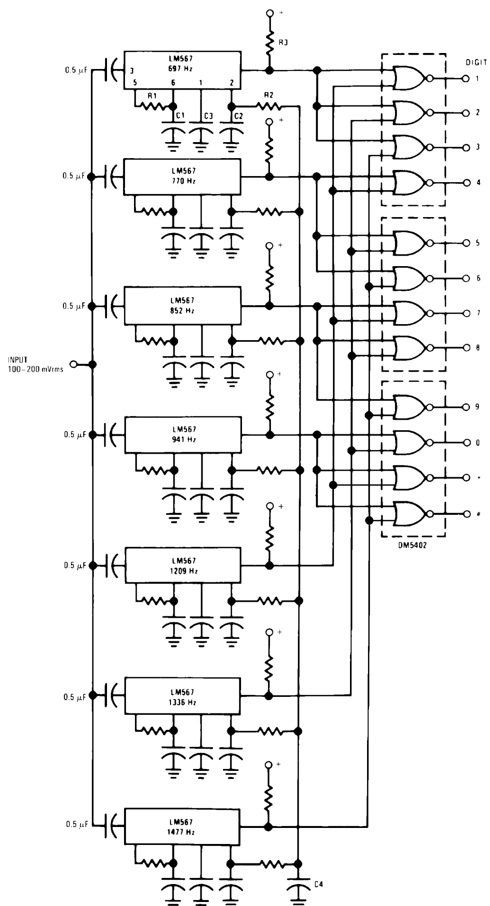
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The LM567 tone decoder is a device capable of detecting if an input signal is inside a selectable range of detection. The device has an open collector transistor output, so an external resistor is required to achieve proper logic levels. When the input signal is inside the detection band, the device output will go to a LOW state. The internal VCO free running frequency establishes the detection band central frequency. An external RC filter is required to set this frequency. The bandwidth in which the device will detect the desired frequency depends on the capacitance of loop filter terminal. Typically a 1µF capacitor is connected to this pin. The device detection band has a different behavior for low and high input voltage levels. Refer to the *Operation With V_i < 200m – V_{RMS}* section and the *Operation With V_i > 200m – V_{RMS}* section for more information.

10.2 Typical Applications

10.2.1 Touch-Tone Decoder



Component values (typ) R1 6.8 to 15k R2 4.7k R3 20k C1 0.10 mfd C2 1.0 mfd 6V C3 2.2 mfd 6V C4 250 mfd 6V

図 10-1. Touch-Tone Decoder

10.2.1.1 Design Requirements

PARAMETERS	VALUES
Supply Voltage Range	3.5 V to 8.5 V
Input Voltage Range	20 mV_{RMS} to VCC + 0.5
Input Frequency	1 Hz to 500 kHz
Output Current	Max. 15 mA

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Timing Components

To calculate the timing components for an approximated desired central detection frequency (f_0), the timing capacitor value (C_1) should be stated in order to calculate the timing resistor value (R_1). Typically for most applications, a 0.1-µF capacitor is used.

$$f_o = 1 / (1.1 \times R_1 \times C_1) \tag{2}$$

10.2.1.2.2 Bandwidth

Detection bandwidth is represented as a percentage of f0. It can be selected based on the input voltage levels (Vi). For Vi < 200 mV_{RMS},

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o \tag{3}$$

For Vi > 200 mV_{RMS}, refer to 表 9-2 or 図 7-5.

10.2.1.2.3 Output Filter

The output filter selection is made considering the capacitor value to be at least twice the Loop filter capacitor.

$$C_3 \geq 2C_2 \tag{4}$$

10.2.1.3 Application Curve

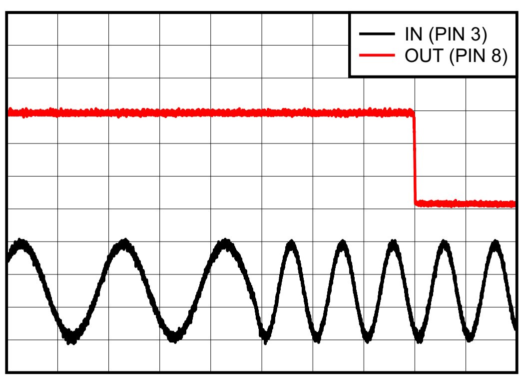
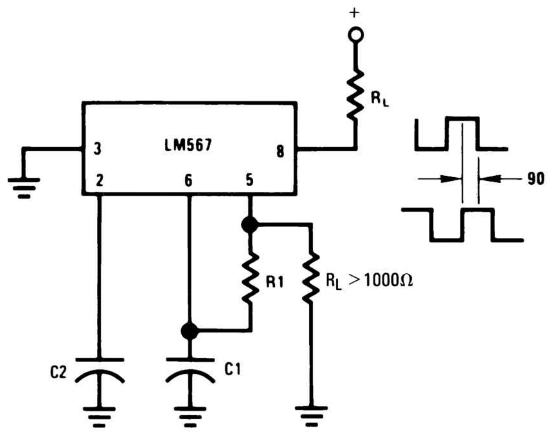


図 10-2. Frequency Detection

10.2.2 Oscillator with Quadrature Output



Connect Pin 3 to 2.8V to Invert Output

図 10-3. Oscillator with Quadrature Output

10.2.2.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.2.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.2.3 Application Curve

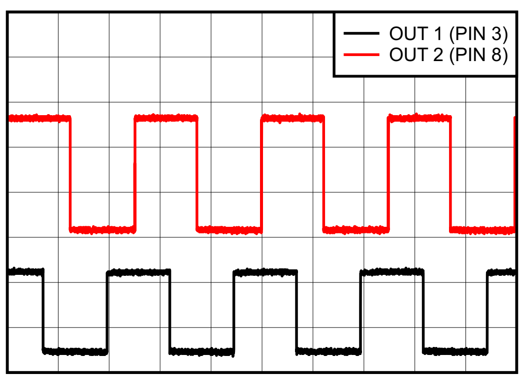


図 10-4. Quadrature Output

10.2.3 Oscillator with Double Frequency Output

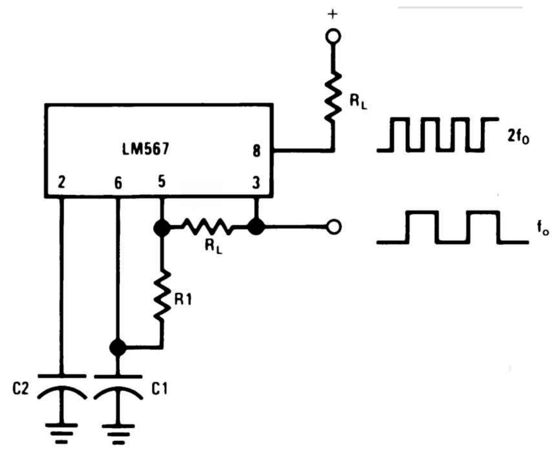


図 10-5. Oscillator with Double Frequency Output

10.2.3.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.3.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.3.3 Application Curve

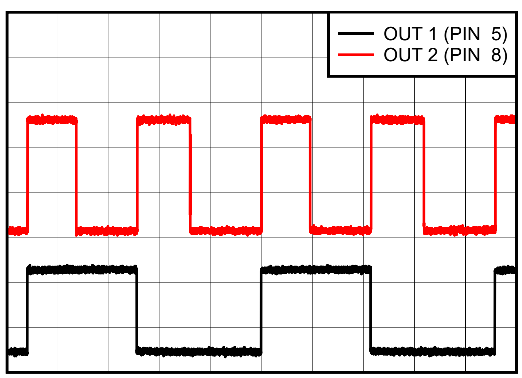


図 10-6. Double Frequency Output

10.2.4 Precision Oscillator Drive 100-mA Loads

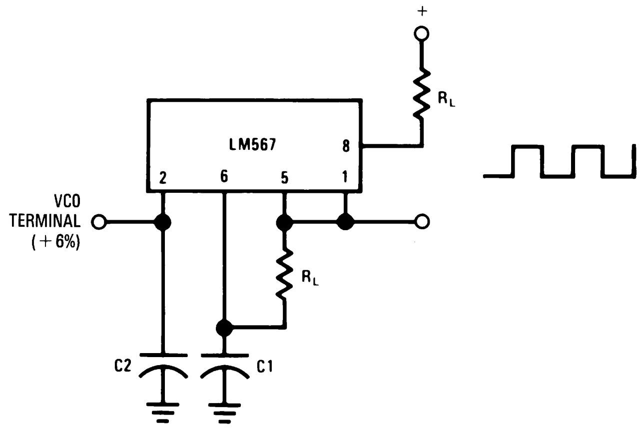


図 10-7. Precision Oscillator Drive 100-mA Loads

10.2.4.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.4.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.4.3 Application Curve

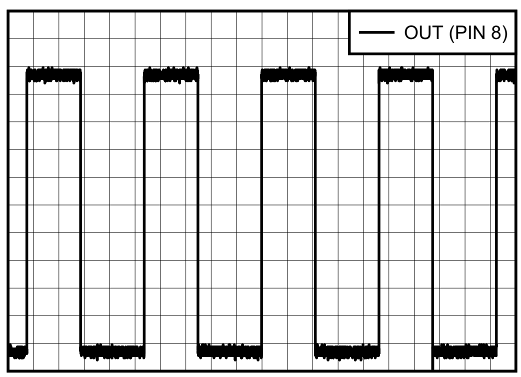
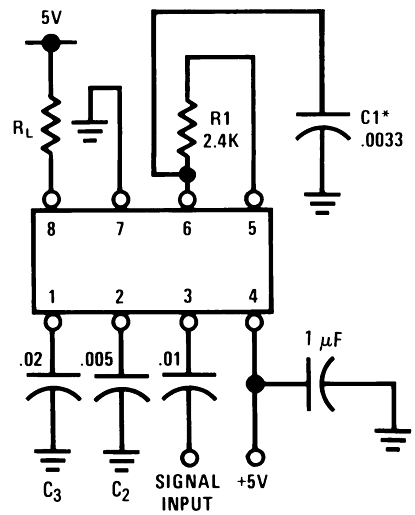


図 10-8. Output for 100-mA Load

10.2.5 AC Test Circuit



f_i = 100 kHz + 5 V

***Note:** Adjust for f_o = 100 kHz.

10.2.5.1 Design Requirements

Refer to the previous *Design Requirements* section.

10.2.5.2 Detailed Design Procedure

Refer to the previous *Detailed Design Procedure* section.

10.2.5.3 Application Curve

Refer to the previous *Application Curve* section.

11 Power Supply Recommendations

The LM567C is designed to operate with a power supply up to 9 V. It is recommended to have a well regulated power supply. As the operating frequency of the device could be very high for some applications, the decoupling of power supply becomes critical, so is required to place a proper decoupling capacitor as close as possible to VCC pin.

12 Layout

12.1 Layout Guidelines

The VCC pin of the LM567 should be decoupled to ground plane as the device can work with high switching speeds. The decoupling capacitor should be placed as close as possible to the device. Traces length for the timing and external filter components should be kept at minimum in order to avoid any possible interference from other close traces.

12.2 Layout Example

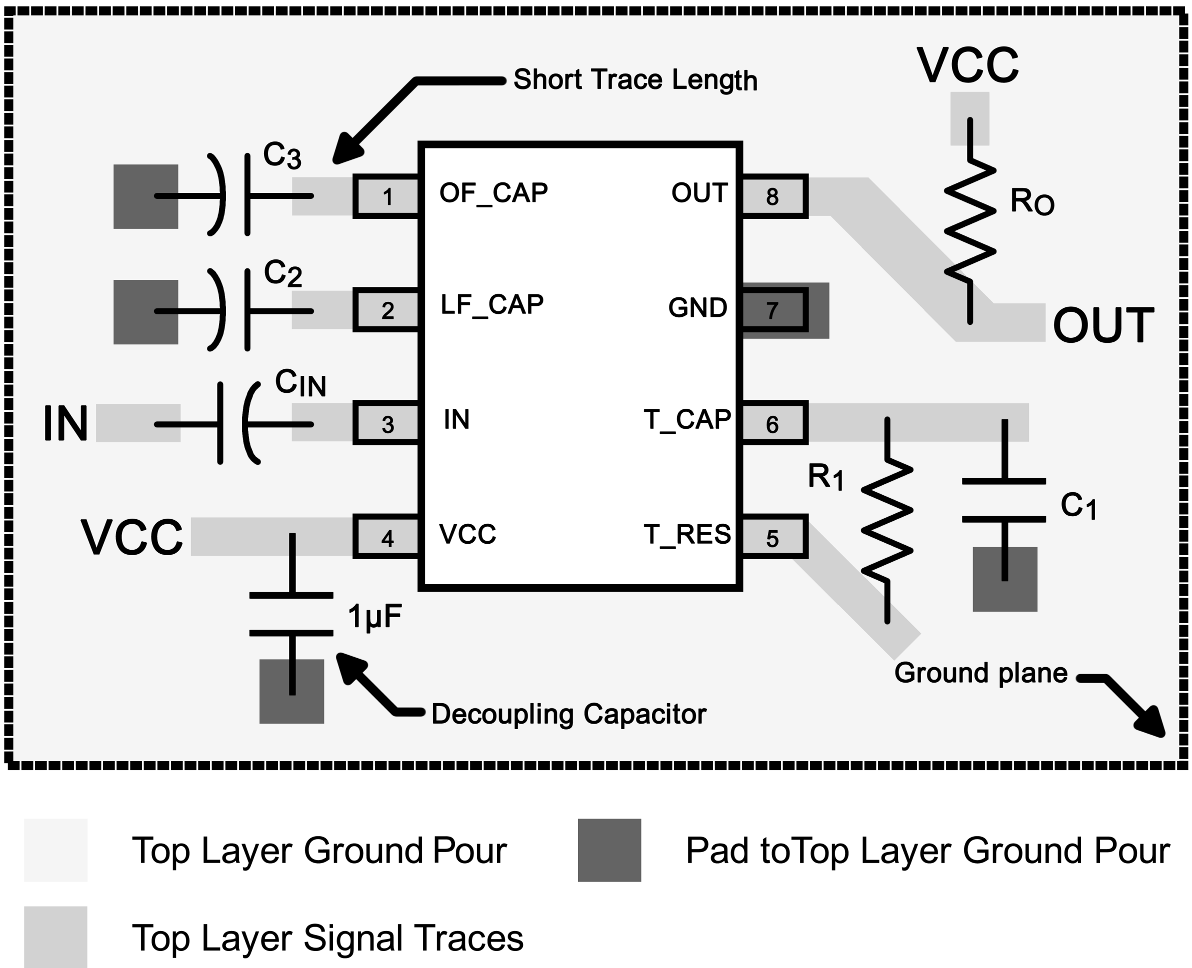


図 12-1. LM567 Layout Example

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 サポート・リソース

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13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM567CM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM 567CM	Samples
LM567CMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM 567CM	Samples
LM567CN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LM 567CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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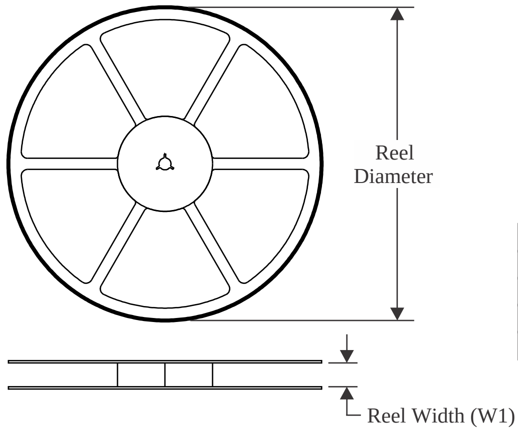
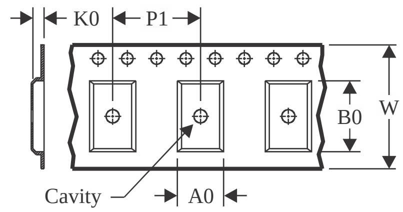
TAPE AND REEL INFORMATION

REEL DIMENSIONS

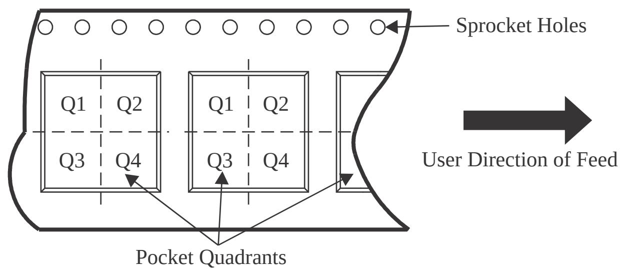


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

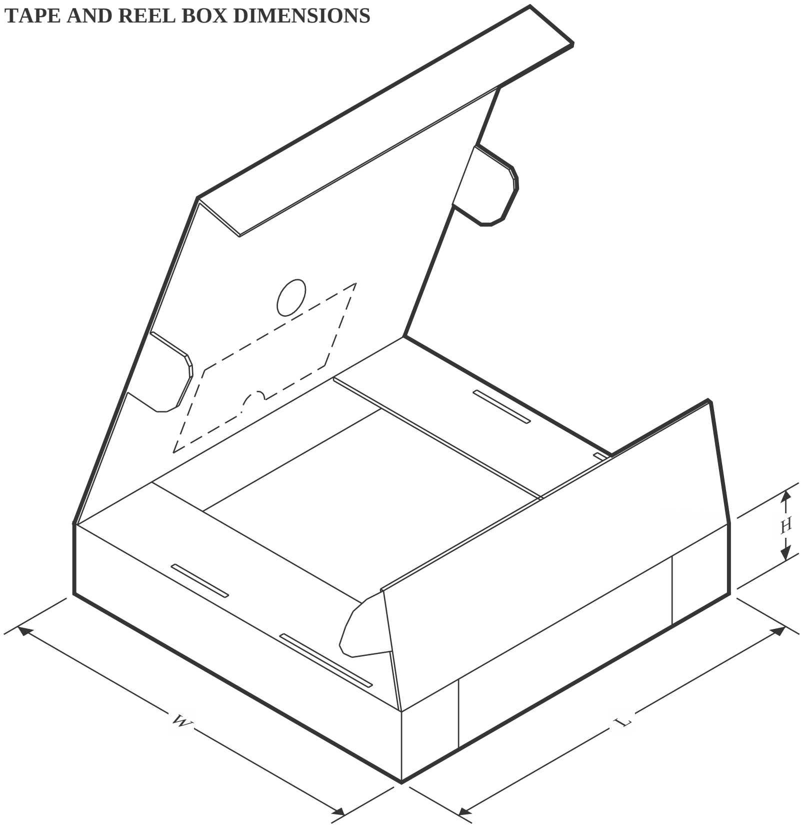
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM567CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

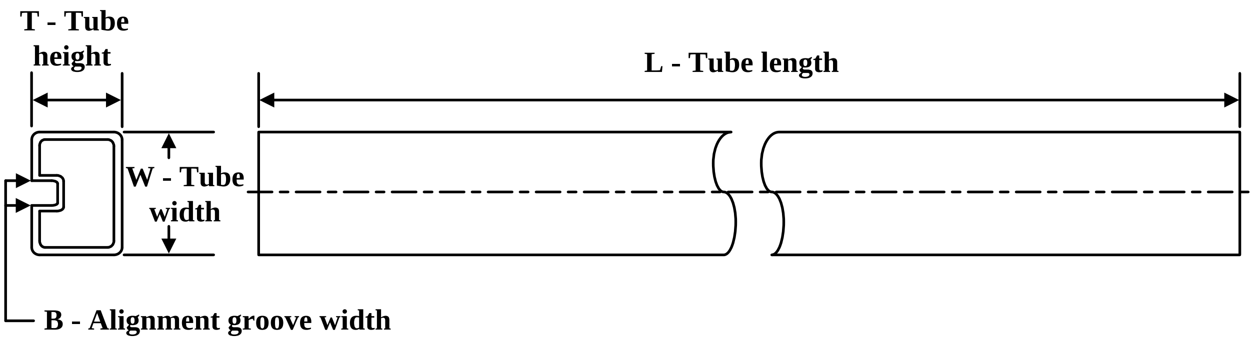
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

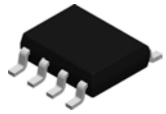
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM567CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

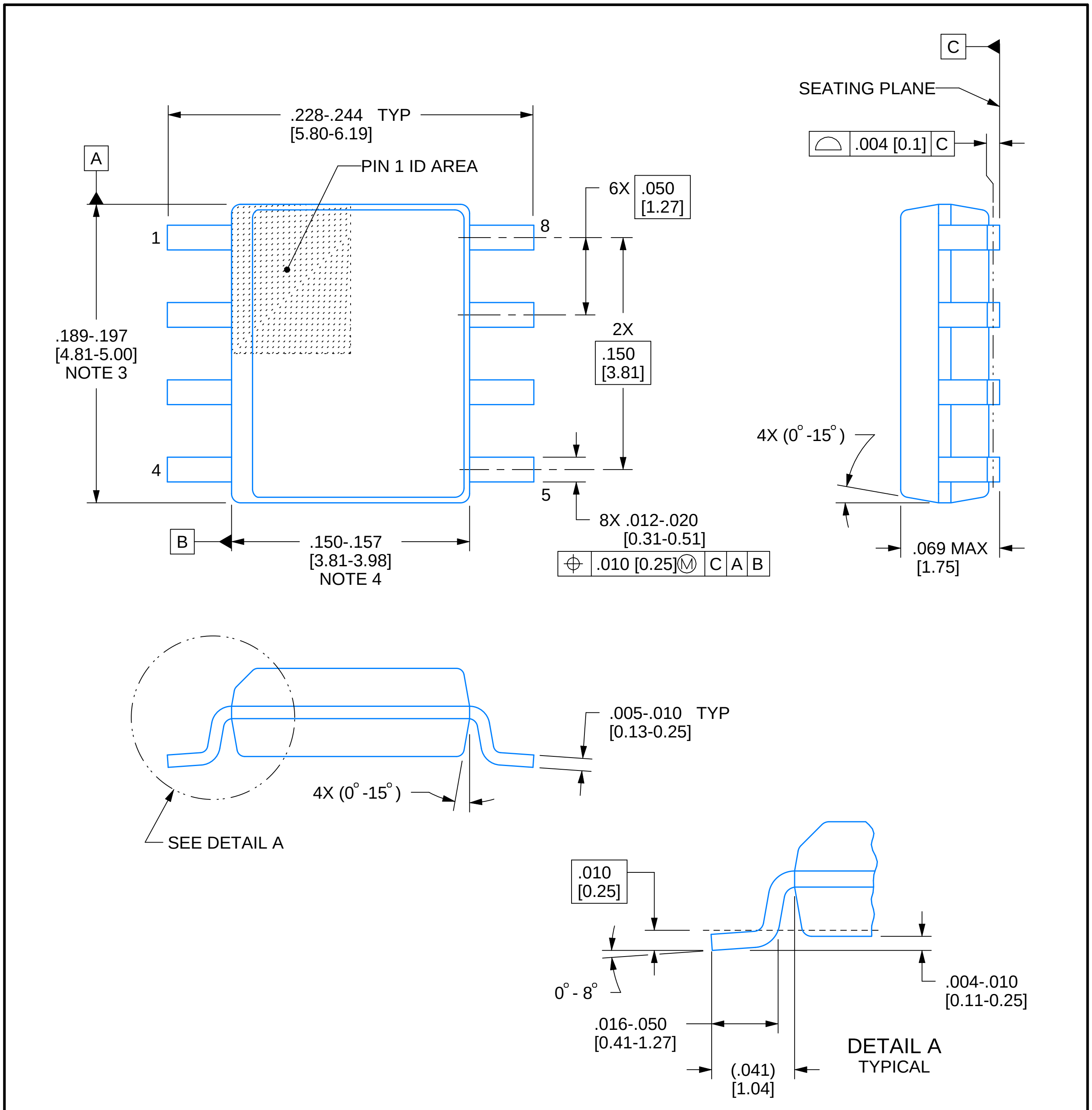
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM567CM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM567CN/NOPB	P	PDIP	8	40	502	14	11938	4.32



D0008A

SOIC - 1.75 mm max height

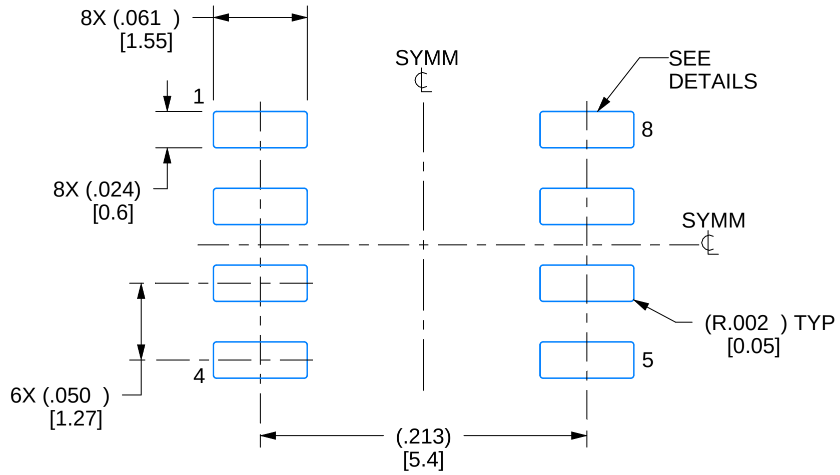
SMALL OUTLINE INTEGRATED CIRCUIT



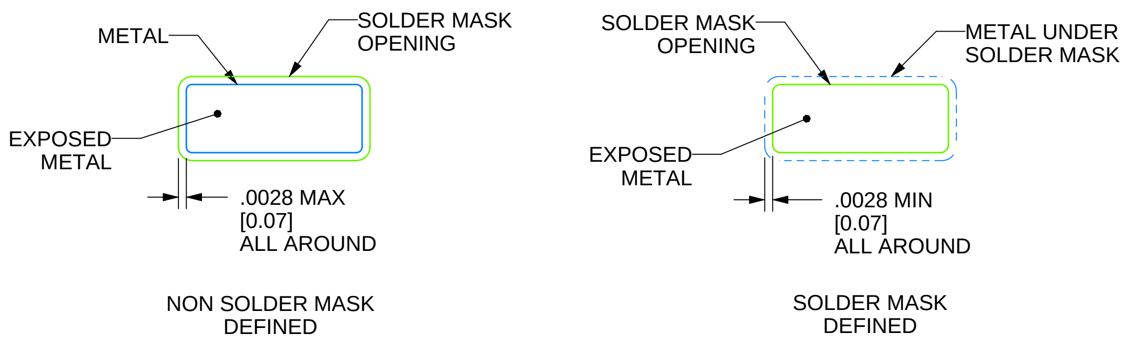
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

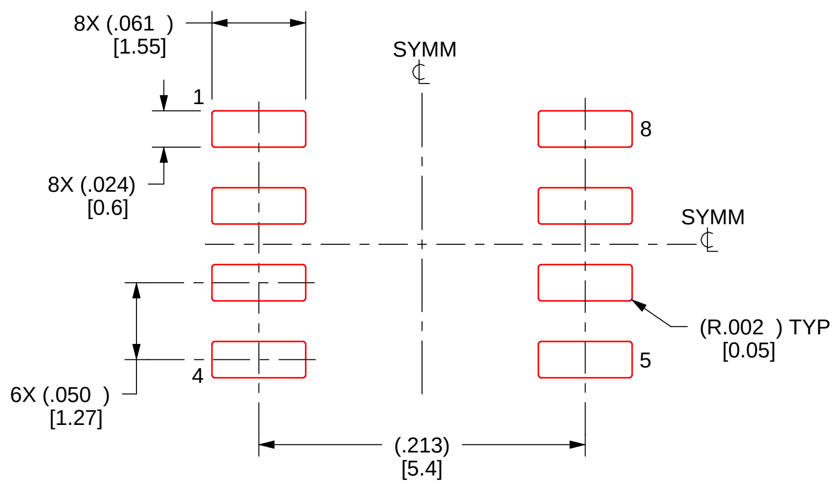


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



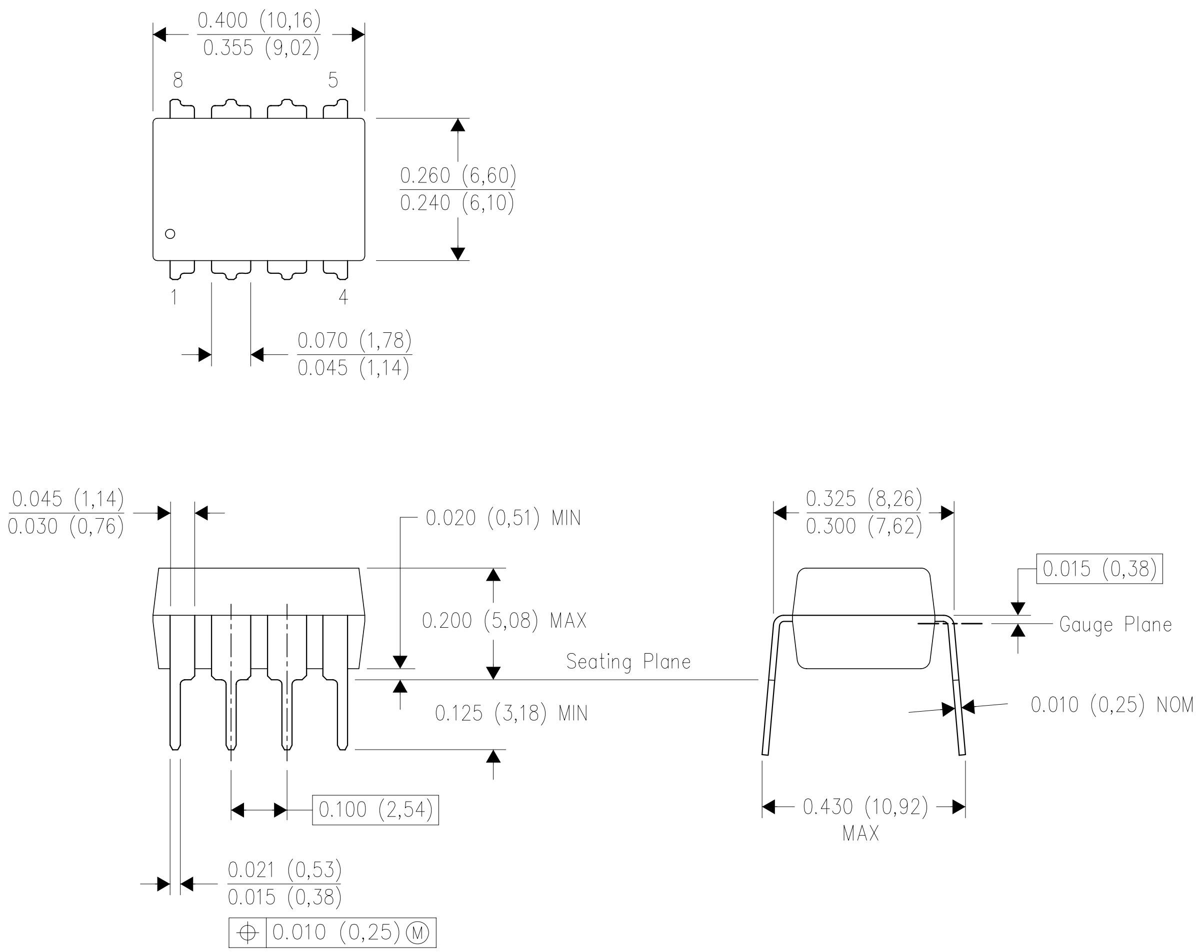
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

重要なお知らせと免責事項

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