TEXAS INSTRUMENTS
LM65645-Q1
JAJSVB4 – SEPTEMBER 2024

LM656x5-Q1 高性能パワー コンバータ、3V～65V、ピン互換、2.5A/3.5A/4.5A、車載用、低 EMI 同期整流降圧コンバータ

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1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- 幅広い入力電圧範囲:3V～65V
- 低 EMI 要件向けの設計
  - CISPR 25 Class 5 準拠
  - モードピンで構成可能な ±5% または ±10% のデュアル ランダム スペクトラム拡散により、ピーク放射を低減
  - 対称型ピン配置付き拡張 HotRod™ QFN パッケージ
  - スイッチング周波数:300kHz～2.2MHz
  - ピンで構成可能な 400kHz および 2.2MHz
  - ピンで構成可能な自動または FPWM 動作
- 短い最小オン時間:40ns (最大値)
  - 2.2MHz で 36V から 3.3V への変換を実現
- あらゆる負荷で高効率の電力変換
  - 94% 超のピーク効率 ($24V_{IN}$、$5V_{OUT}$、400kHz)
  - 2.5µA PFM 無負荷時入力電流
- 高い電力密度
  - 補償、電流制限、TSD を内蔵
  - 3.6mm × 2.6mm、ウェッタブル フランク、20 ピン パッケージ
  - Θ_{JA} = 25.5℃/W (LM65645-Q1EVM)
- WEBENCH® Power Designer により、LM656x5-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 先進運転支援システム (ADAS)
- 車載用インフォテインメントおよびクラスタ
- ハイブリッド、電動、パワートレイン システム

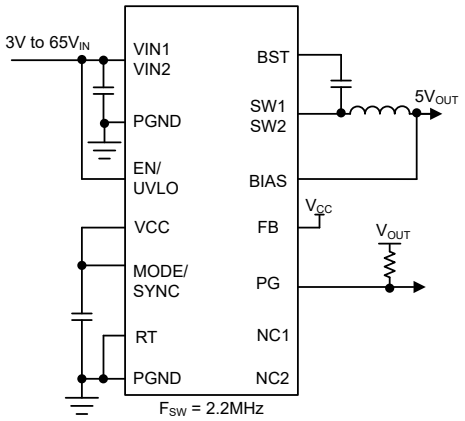
3 概要

LM656x5-Q1 は、高効率、高い電力密度、超低電磁干渉 (EMI) を実現するように設計された車載用降圧コンバータ ファミリです。これらのコンバータは、3V～65V (70V 許容) (外部入力サージ保護の必要性が低下) の広い入力電圧範囲で動作します。LM656x5-Q1 は、3.3V および 5V または可変構成でのピン選択可能な固定出力電圧を備えています。ループ インダクタンスを最小化し、スイッチ ノードのスルーレートを最適化することで、低 EMI での動作がイネーブルになります。ピン選択可能な ±5% または ±10% のデュアル ランダム スペクトラム拡散 (DRSS) により、三角波変調と疑似ランダム変調の組み合わせによりピーク放射が大幅に低減されると同時に、出力電圧リップルが非常に低く維持されます。電流モード制御アーキテクチャの標準最小オン時間は 30ns で、高周波数での高い変換比、高速過渡応答、優れた負荷およびライン レギュレーションを実現します。

製品情報

部品番号 (3)	パッケージ (1)	パッケージ サイズ (2)
LM65625-Q1 (4)、LM65635-Q1 (4)、LM65645-Q1	RZT (WQFN-FCRLF、20)	2.60mm × 3.60 mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) デバイス比較表を参照してください。
(4) プレビュー情報 (事前情報ではありません)。



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

ORDERABLE PART NUMBER	CURRENT	SAMPLING
LM65645SRZTRQ1	4.5A	Yes
LM65635SRZTRQ1(2)	3.5A(1)	No
LM65625SRZTRQ1(2)	2.5A	No

(1) For more information about sampling requests, please contact Texas Instruments.
(2) Preview information (not Advance Information).

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5 Pin Configuration and Functions

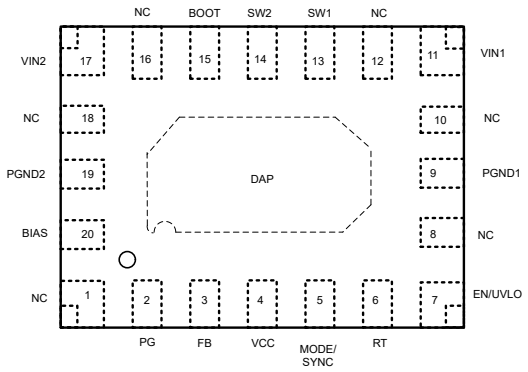

図 5-1. 20 Pin RZT, WQFN-FCRLF Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
NC	1	—	No connect pin. Leave floating.
PG	2	O	Power Good flag output. Open drain output that goes low if VOUT is outside of the specified regulation window.
FB	3	A	Feedback configuration pin. Connect to GND to configure 3.3V fixed output voltage. Connect to VCC to configure 5V fixed output voltage. Connect this pin to a feedback divider for adjustable output options. The regulation threshold is 0.8V.
VCC	4	P	Internal LDO output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Can be used for logic pull-up to control or flag pins. Connect a high quality 1µF capacitor from this pin to GND.
MODE / SYNC	5	I/O	Mode and synchronization input pin. Connect to GND, or drive the pin low to operate in AUTO mode. Connect to VCC, or drive the pin high, or send a synchronization clock signal to operate in FPWM mode. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency.
RT	6	I/O	Switching frequency programming pin. Connect this pin to VCC for 400kHz operation, or to GND for 2.2MHz operation. Connect this pin to ground through a resistor to set the switching frequency between 300kHz and 2200kHz. Do not float.
EN / UVLO	7	P	Precision enable pin. High = ON, Low = OFF. This pin can be directly connected to VIN. The precision threshold on this input enables use as an adjustable UVLO. Do not float.
NC	8	—	No connect pin. Leave floating.
PGND1	9	G	Power ground to low-side MOSFET. Connect to system ground. Connect a high-quality bypass capacitor or capacitors between this pin and VIN1.
NC	10	—	No connect pin. Leave floating.
VIN1	11	P	Input supply to the regulator. Connect high-quality bypass capacitors from this pin to PGND1. Provide a low-impedance connection to VIN2.
NC	12	—	No connect pin. Leave floating.
SW1, SW2	13, 14	P	Device switch pins. Connect to the output inductor.
BOOT	15	P	High-side driver upper supply rail. Connect a high quality 100nF capacitor between the SW node and BOOT. An internal diode charges the capacitor while SW node is low.
NC	16	—	No connect pin. Leave floating.
VIN2	17	P	Input supply to the regulator. Connect high-quality bypass capacitors from this pin to PGND2. Provide a low-impedance connection to VIN1.
NC	18	—	No connect pin. Leave floating.
PGND2	19	G	Power ground to internal low-side MOSFET. Connect to system ground. Connect high-quality bypass capacitors between this pin and VIN2.

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表 5-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BIAS	20	P	Input to internal voltage regulator. If configured for fixed VOUT, connect this pin to the VOUT node to close the control loop. If configured for an adjustable VOUT, connect this pin to the VOUT node or an external bias supply from 3.3V to 30V. If output voltage is above 30V and no external supply is used, tie the pin to GND.
DAP	—	G	Exposed ground pad. Connect to system GND on the PCB. This pin is a major heat dissipation path for the die. The pad must be used for heat sinking by soldering to the GND copper on a PCB. Implementing as many thermal vias as suggested in the example board layout makes sure of the lowest package thermal resistance and best possible thermal performance.

(1) I = input, O = output, A = Analog, P = Power, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	70	V
Input voltage	EN/UVLO to PGND	–0.3	70	V
Input voltage	RT to PGND	–0.3	70	V
Input voltage	BIAS to PGND	–0.3	40	V
Input voltage	MODE/CLKIN to PGND	–0.3	5.5	V
Input voltage	FB to PGND	–0.3	5.5	V
Output voltage	SW to PGND	–0.6	V_{IN} + 0.3	V
Output voltage	PGOOD to PGND	–0.3	40	V
Output voltage	BST to SW	–0.3	5.5	V
Output voltage	VCC to PGND	–0.3	5.5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	3	65	V
Input voltage	EN	0	65	V
Input voltage	BIAS, PGOOD	0	30	V
Input voltage	FB	0	5.5	V
Input voltage	MODE/SYNC, RT	0	5.5	V
Pullup resistance	$R_{PU(PGOOD)}$	4		kΩ
Pullup reference voltage	$V_{PU(PGOOD)}$	0.8	30	V
Output voltage	VOUT	0.8		V
Output current	LM65645/LM65645-Q1	0	4.5	A
Output current	LM65635/LM65635-Q1	0	3.5	A
Output current	LM65625/LM65645-Q1	0	2.5	A
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE RZT (WQFN-FCRLF) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3)	25.5	°C/W

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6.4 Thermal Information (続き)

THERMAL METRIC(1)		DEVICE RZT (WQFN-FCRLF) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)(2)	43.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. The thermal parameters do not represent the performance obtained in an actual application. For example, the EVM $R_{\Theta JA}$ = 25.5 °C/W. For design information please see the Maximum Ambient Temperature section.
(3) Refer to the LM65645EVM user guide for board layout and additional information. For thermal design information please see the Maximum Ambient Temperature section.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, f_{SW} = 2.2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN PIN)						
VIN_{UVLO_R}	VIN UVLO rising threshold	V_{IN} rising (needed to start up), I_{VCC} = 0A	3.25	3.5	3.65	V
VIN_{UVLO_F}	VIN UVLO falling threshold	V_{IN} falling (once operating), I_{VCC} = 0A		2.5	2.57	V
VIN_{UVLO_H}	VIN UVLO hysteresis			0.9		V
I_{Q-SD}	V_{IN} Shutdown supply current	V_{EN} = 0V, T_J = 25°C			0.81	µA
I_{VIN}	VIN pin input current, no switching	V_{BIAS} = 3.3V + 2%		0.45		µA
$I_{BIAS(FIX-3.3V)}$	BIAS pin input current, fixed 3.3V output, no switching	V_{BIAS} = 3.3V + 2%, Auto Mode enabled		8.0		µA
$I_{Q(FIX-3.3V)}$	Total V_{IN} quiescent current, fixed 3.3V output, no switching	V_{IN} = 24V, V_{BIAS} = 3.3V + 2%, T_J = 25°C, Auto Mode enabled		1.5	2	µA
		T_J = 125°C			3.4	µA
$I_{BIAS(ADJ-3.3V)}$	BIAS pin input current, adjustable 3.3V output, no switching	V_{FB} = 0.8V+2%, Auto Mode		6.5		µA
$I_{Q(ADJ-3.3V)}$	Total V_{IN} quiescent current, adjustable 3.3V output, no switching	V_{IN} = 24.0V, V_{FB} = 0.8V + 2%, Auto Mode		1.35		µA
ENABLE (EN PIN)						
$V_{EN\_TH\_R}$	Enable voltage rising threshold	V_{EN} rising	1.15	1.25	1.35	V
$V_{EN\_TH\_F}$	Enable input low threshold	V_{EN} falling	0.9	1	1.1	V
V_{EN_HYS}	Enable voltage hysteresis			250		mV
I_{EN_LKG}	Enable input leakage current	V_{EN} = V_{IN}		0.2	3.6	µA
INTERNAL LDO (VCC PIN)						
V_{VCC}	Internal LDO output voltage	3.4V ≤ V_{IN} ≤ , $V_{BIA\ S}$ = 0V		3.35		V
		3.4V ≤ V_{BIAS} ≤ 30V		3.35		V
$V_{VCC-UVLO\_R}$	VCC UVLO rising threshold	VCC rising under voltage threshold, I_{VCC} = 0A	3.23	3.5	3.65	V
$V_{VCC-UVLO\_H}$	VCC UVLO hysteresis	Hysteresis below $V_{VCC-UVLO\_R}$		0.9		V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Internal feedback reference voltage	FPWM Mode	0.792	0.8	0.808	V
I_{FB-LKG}	Feedback pin input leakage current	V_{FB} = 0.8V, Adjustable Version		0.025		nA

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6.5 Electrical Characteristics (続き)

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{FB-SEL-5V}$	Resistance for fixed 5.0V setting from FB pin to VCC				200	Ω
$R_{FB-SEL-3V}$	Resistance for fixed 3.3V setting from FB pin to GND				200	Ω
$R_{FB-SEL-ADJ}$	Thevenin Equivalent resistance of external FB divider on FB pin to select adjustable output voltage setting		4		100	kΩ
FIXED OUTPUT VOLTAGE (BIAS PIN)						
$V_{OUT(3.3V)}$	3.3V fixed output voltage	FB shorted to GND	3.267	3.3	3.333	V
$V_{OUT(5V)}$	5.0V fixed output voltage	FB shorted to VCC	4.95	5	5.05	V
STARTUP (SS PIN)						
t_{EN_HIGH}	Enable high to start of switching delay	V_{FB} = V_{RT} = V_{MODE} = GND, V_{BIAS} = V_{OUT}		2		ms
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{REF} at 90% of set point	2.9	4.8	8.1	ms
CURRENT LIMITS AND HICCUP						
I_{HS-LIM}	High side peak current limit, 4.5A Trim Option	Duty-cycle approaches 0%.	5.7	6.6	7.25	A
I_{LS-LIM}	Low side valley current limit, 4.5A Trim Option	Valley current limit on LS FET	4.4	5.2	5.65	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty cycle, 4.5A Trim Option	V_{VCC} = 3.3V, tpulse ≤ 100ns, Auto Mode	1.21	1.57	1.92	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty cycle, 4.5A Trim Option	V_{VCC} = 3.3V, tpulse ≥1µs, Auto Mode		0.66		A
I_{HS-LIM}	High side peak Current limit, 3.5A Trim Option	Duty-cycle approaches 0%.	4.8	5.45	5.9	A
I_{LS-LIM}	Low side valley current limit, 3.5A Trim Option	Valley current limit on LS FET	3.8	4.4	4.8	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty cycle, 3.5A Trim Option	V_{CC} = 3.3V, tpulse ≤ 100ns, Auto Mode	0.99	1.29	1.58	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty cycle, 3.5A Trim Option	V_{CC} = 3.3V, tpulse ≥ 1µs, Auto Mode		0.52		A
I_{HS-LIM}	High side peak current limit, 2.5A Trim Option	Duty-cycle approaches 0%.	3.6	4.1	4.5	A
I_{LS-LIM}	Low side valley current limit, 2.5A Trim Option	Valley current limit on LS FET	2.9	3.3	3.6	A
$I_{L-PEAK-MIN}$	Minimum peak inductor current at minimum duty cycle, 2.5A Trim Option	V_{CC} = 3.3V, tpulse ≤ 100ns, Auto Mode	0.8	1.1	1.2	A
$I_{L-PEAK-MAX}$	Minimum peak inductor current at maximum duty cycle, 2.5A Trim Option	V_{CC} = 3.3V, tpulse ≥ 1µs, Auto Mode		0.43		A
$I_{LS-NEG-LIM}$	Low side negative current limit	Sinking current limit on LS FET, FPWM Mode	-6	-4.3	-2.8	A
$I_{L-ZC-LIM}$	Zerocross current limit	V_{CC} = 3.3V, Auto Mode		45		mA
V_{HIC}	Overcurrent hiccup threshold on FB Pin	LS FET on-time > 165ns, Not during Soft-start		0.32		V
t_{HIC_DLY}	Hiccup mode activation delay		128		256	cycles
t_{HIC}	Hiccup mode duration time			40		ms
POWER GOOD (PG PIN)						
$V_{PG-OVP-R}$	PG overvoltage rising threshold	% of FB voltage (Adj) or Bias Voltage (Fixed)	103	105	107	%
$V_{PG-OVP-F}$	PG overvoltage falling threshold	% of FB voltage (Adj) or Bias Voltage (Fixed)	102	104	106	%
$V_{PG-UVP-R}$	PG undervoltage rising threshold	% of FB voltage (Adj) or Bias Voltage (Fixed)	94	96	98	%

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6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, f_{SW} = 2.2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PG-UVP-F}$	PG undervoltage falling threshold	% of FB voltage (Adj) or Bias Voltage (Fixed)	93	95	97	%
$t_{PG-DEGLITCH-F}$	Deglitch filter delay on PG falling edge		55	114	175	µs
$t_{PG-DEGLITCH-R}$	Deglitch filter delay on PG rising edge		1.4	2	4.5	ms
$V_{IN-PG-VALID}$	Minimum VIN for valid PG output	$V_{OL(PG)}$ < 0.4V, R_{PU} = 50kΩ, V_{PU} = 5V			1.25	V
V_{OL-PG}	Output low voltage	I_{OL} = 1mA, V_{IN} = 1.2V			0.4	V
R_{ON-PG}	PGOOD on-resistance	I_{PG} = 1mA		40	125	Ω
SWITCHING FREQUENCY (RT PIN)						
$f_{SW1(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = GND	1.98	2.2	2.42	MHz
$f_{SW2(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = 15.8kΩ, 1%	900	1000	1100	kHz
$f_{SW3(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = VCC	360	400	440	kHz
SYNCHRONIZATION (MODE/SYNC PIN)						
$V_{IH(MODE/CLKIN)}$	MODE/CLKIN input high level threshold				1.3	V
$V_{IL(MODE/CLKIN)}$	MODE/CLKIN input low level threshold		0.45			V
$f_{CLKIN-RANGE(FPWM)}$	Synchronization frequency range for set 2.2MHz f_{SW}	R_{RT} = 6.81kΩ, 1%	1.76		2.64	MHz
$t_{CLKIN(TON)}$	Minimum positive pulse width of external sync signal				80	ns
$t_{CLKIN(TOFF)}$	Minimum negative pulse width of external sync signal				80	ns
$t_{CLKIN-SW-DLY}$	CLKIN to SW delay time		-15		15	ns
DUAL RANDOM SPREAD SPECTRUM						
Δf_{SS1-LF}	Low-frequency triangular spread spectrum modulation range - standard	Mode pin short to ground		8.5		%
Δf_{SS2-LF}	Low-frequency triangular spread spectrum modulation range - extended	R_{MODE} = 149.9kΩ, 1%		17		%
f_{m1-LF}	Triangular modulation frequency - standard	Mode pin short to ground	7.2	12	16.8	kHz
f_{m2-LF}	Triangular modulation frequency - extended	R_{MODE} = 149.9kΩ, 1%	3.6	6	8.4	kHz
Δf_{SS-HF}	High-frequency pseudo-random spread spectrum modulation range	RMODE = 149.9kΩ, 1%		2.0		%
POWER STAGE						
$R_{DS-ON-HS}$	High-side fet on-resistance	I_{SW} = 500mA, $V_{BOOT-SW}$ = 3.3V		99		mΩ
$R_{DS-ON-LS}$	Low-side fet on-resistance			50		mΩ
$t_{ON-MIN(FPWM)}$	Minimum on-time	FPWM: I_{OUT} = 0A, V_{IN} = 36V, RT = GND		30	40	ns
$t_{ON-MIN(AUTO)}$	Minimum on-time	AUTO: I_{OUT} = 2A, V_{IN} = 36V, RT = GND		28	40	ns
$t_{OFF-MIN}$	Minimum off-time	V_{IN} = 4V		80	110	ns
t_{ON-MAX}	Maximum on-time	f_{SW} = 400kHz, R_{RT} = 40.2kΩ		13.3		µs
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown(1)	Shutdown threshold	155	165	177	ºC
		Recovery threshold		156		ºC

(1) Specified by design.

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6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not specified by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN_MIN1}	V_{IN} for full functionality, after start-up	V_{VOUT} set to 3.3V			3	V
I_{Q_VIN}	Operating input quiescent current at V_{IN} PIN for fixed V_{OUT} option	V_{IN} = 24.0V, I_{OUT} = 0A, V_{OUT} = 3.3V (fixed), V_{FB} = 0V, V_{BIAS} = V_{VOUT}, PFM mode		1.8		µA
	Operating input quiescent current at V_{IN} PIN for fixed V_{OUT} option	V_{IN} = 24.0V, I_{OUT} = 0A, V_{OUT} = 5.0V (fixed), V_{FB} = V_{VCC}, V_{BIAS} = V_{VOUT}, PFM mode		1.8		µA
I_{Q_VIN}	Operating input quiescent current at V_{IN} PIN for fixed V_{OUT} option	V_{IN} = 13.5V, I_{OUT} = 0A, V_{OUT} = 3.3V (fixed), V_{FB} = 0V, V_{BIAS} = V_{OUT}, PFM mode		3.0		µA
	Operating input quiescent current at V_{IN} PIN for fixed V_{OUT} option	V_{IN} = 13.5V, I_{OUT} = 0A, V_{OUT} = 5.0V (fixed), V_{FB} = V_{VCC}, V_{BIAS} = V_{VOUT}, PFM mode		3.0		µA
OUTPUT VOLTAGE						
$V_{VOUT\_5V\_ACC}$	Load and Line regulation for 5V VOUT (fixed and adjustable)	VIN = 4V to 42V, IOUT = 0A to full load, FPWM Mode	–1.5		1.5	%
		VIN = 4V to 42, IOUT = 0A to full load, PFMMode	–1.5		2.5	%
$V_{VOUT\_3P3V\_ACC}$	Load and Line regulation for 3.3V VOUT (fixed and adjustable)	VIN = 4V to 42V, IOUT = 0A to full load, FPWM Mode	–1.5		1.5	%
		VIN = 4V to 42, IOUT = 0A to full load, PFM Mode	–1.5		2.5	%
D_{MAX}	Maximum switch duty cycle	F_{SW} = 400kHz, while in frequency foldback		99		%
EFFICIENCY						
MISCELLEANEOUS						
V_{DROP}	Input to output voltage differential to maintain fSW ≥ 1.85MHz, without inductor DCR drop		TBD			

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7 Detailed Description

7.1 Overview

The LM656x5-Q1 is a family of high-efficiency, high-power density, ultra low-EMI buck converters. These converters operate over a wide input voltage range of 3V to 65V (70V tolerant) with pin selectable fixed output voltages of 3.3V, 5V, or as in adjustable output configuration.

The current-mode control architecture, with 30ns minimum on-time, allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the switching frequency is automatically reduced. This feature allows regulation to be maintained during load dump events and cold cranking situations.

This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The LM656x5-Q1 can be set to operate at fixed 400kHz, fixed 2.2MHz, or in adjustable mode from 300kHz to 2.2MHz by using the RT pin. An integrated compensation network combined with an accurate current limit scheme minimizes bill of material cost and component count.

The LM656x5-Q1 has been designed for low EMI. The device includes the following:

- Mode pin-configurable ±5% or ±10% dual random spread spectrum (DRSS) frequency hopping
- Symmetrical pin out minimizing parasitic package inductance
- Operation over a frequency range above and below AM radio band
- Pin-configurable for AUTO or FPWM mode along with external clock synchronization capabilities

These features can eliminate shielding and other expensive EMI mitigation measures.

To use the device in reliability-conscious environments, the LM656x5-Q1 has a package with enlarged corner terminals for improved board level reliability and wettable flanks, allowing optical inspection.

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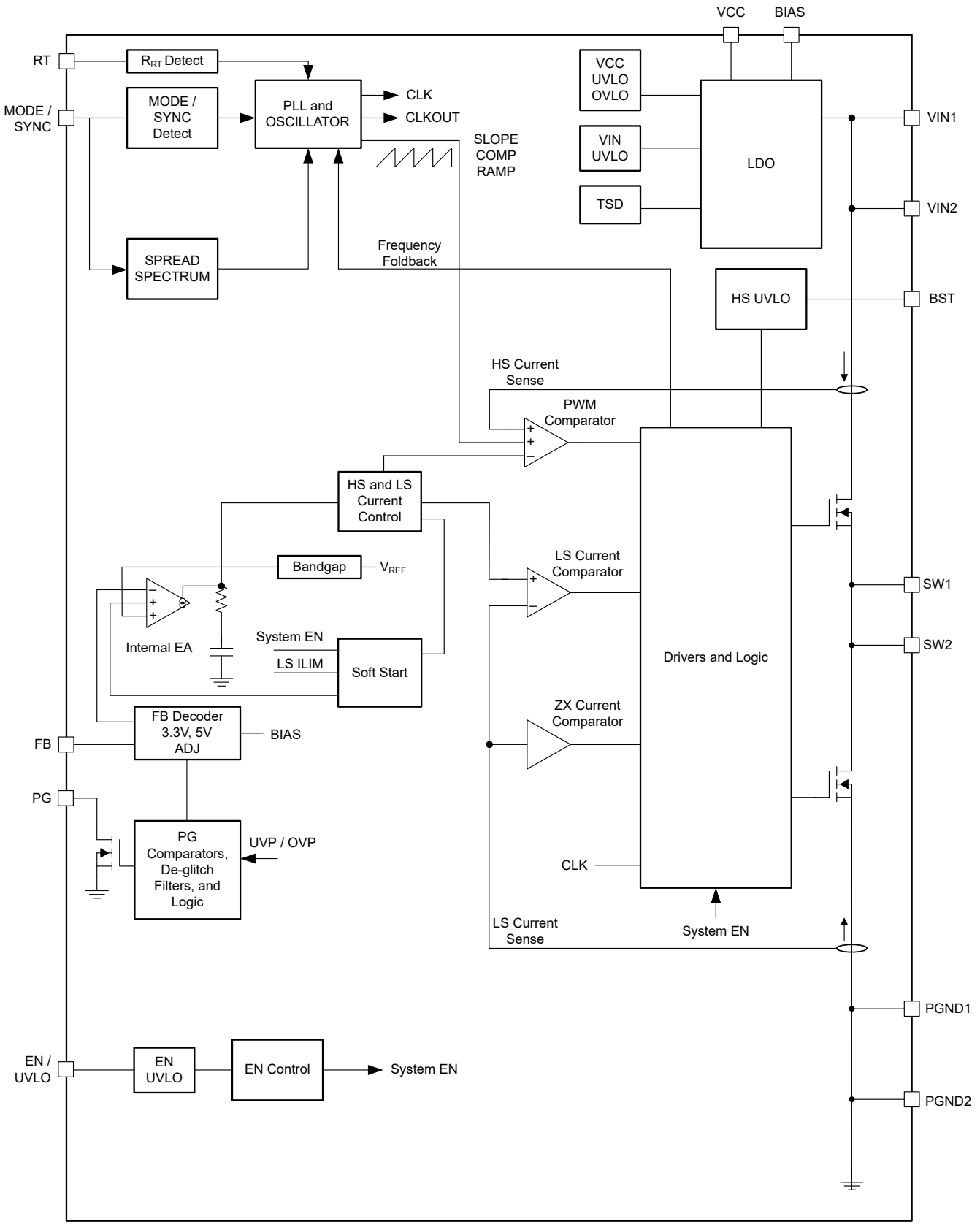
7.2 Functional Block Diagram



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7.3 Feature Descriptions

7.3.1 Output Voltage Selection

The LM656x5-Q1 features pin-selectable fixed output voltage or adjustable output voltage mode. In fixed output voltage mode, the output voltage is selected by the FB pin. Connect the FB pin to GND to select the fixed 3.3V output, or connect to VCC for a fixed 5V output. When the fixed output voltage mode is selected, the BIAS pin is connected directly to the output of the regulator. In this mode, the BIAS pin closes the feedback loop of the regulator and provides input power to the internal bias regulator. Because of the internal LDO is supplied through this pin, a reliable bode plot cannot be taken in fixed output voltage mode however this measurement can be take in adjustable mode. Connect BIAS to VOUT as shown in 図 8-1.

表 7-1. Output Voltage Selection

FB	VOUT
Short to GND	3.3V
Short to VCC	5V
Connect to a feedback resistor divider (図 7-1)	ADJ

In the adjustable output voltage mode, a voltage divider is connected between the regulator output voltage and the FB pin. The resistor values are calculated based on the desired output voltage and the 0.8V reference of the regulator. See 図 7-1 for detailed connections.

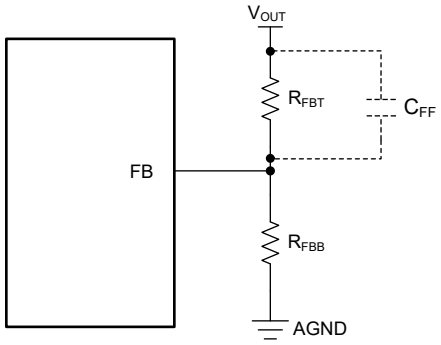

図 7-1. Setting Output Voltage of Adjustable Versions

Use 式 1 to select a value for R_{FBB}, based on a desired value of R_{FBT}. Limiting the value of R_{FBT} to 100kΩ or less is best practice. Larger values of resistance are susceptible to leakage currents on the PCB, caused by environmental contamination, that can shift the desired output voltage. Values up to about 1MΩ can be used to reduce the no-load supply current, in those cases where excessive PCB leakage currents are not present.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 0.8} \quad (1)$$

In some cases, when using the adjustable mode, a feed forward capacitor can be used to improve the loop phase margin or load transient response. The exact value of C_{FF} is best selected empirically during the initial bench evaluation of the design. Leave a placeholder for this capacitor in the PCB layout if needed at some stage during development.

7.3.2 EN Pin and Use as V_{IN} UVLO

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input Undervoltage Lockout (UVLO), if desired. Applying a voltage greater than $V_{EN\_TH\_R}$ fully enables the device, allowing the device to enter start-up mode and begin the soft-start period. When the EN input is brought below $V_{EN\_TH\_F}$, the regulator stops switching and enters shutdown mode, with a VIN input current of less than 0.81µA (Max). Note that the EN input draws a current of

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about 0.2µA (typical). The EN input can be connected directly to VIN if this feature is not needed. The enable must not float, as floating the enable pin turns the device off. The values for the various EN thresholds can be found in the *Electrical Characteristics* table.

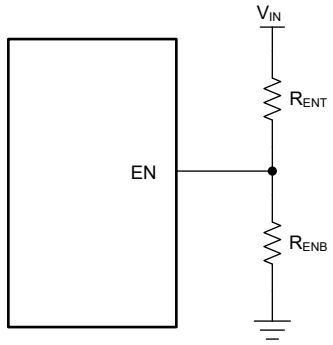

図 7-2. VIN UVLO Using the EN Pin

In some cases, an input UVLO level different than that provided internal to the device is needed. This feature can be used for special sequencing or to prevent input voltage oscillations caused by excessively long power cables. External UVLO can be accomplished by using the circuit shown in 図 7-2. The input voltage at which the device turns on is designated as V_{ON} while the turnoff voltage is V_{OFF}. The current in the divider must be greater than the current into the EN input (I_{EN_LKG}), to preserve accuracy. Values for R_{ENB} between 10kΩ and 50kΩ are reasonable. Then, 式 2 is used to calculate R_{ENT} and 式 3 is used to calculate V_{OFF}.

$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN\_TH\_R}} - 1 \right) \quad (2)$$

$$V_{OFF} = V_{ON} \times \left(\frac{V_{EN\_TH\_F}}{V_{EN\_TH\_R}} \right) \quad (3)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

7.3.3 Mode Selection

The MODE / SYNC pin is a multifunction pin that configures the mode of operation, and serves as an input for an external synchronization signal. If the pin is grounded or driven to logic low, the converter operates in AUTO mode. If the pin is tied to VCC or driven to logic high, or synchronized to an external clock source, the converter operates in FPWM mode.

表 7-2. Mode Selection

MODE/SYNC	Mode	Dynamic Mode Change	Spread Spectrum
Short to GND or driven low	AUTO	Enabled	Standard ±5% DRSS
49.9kΩ to GND	FPWM	Disabled	Wide ±10% DRSS
149.9kΩ to GND	AUTO	Disabled	Wide ±10% DRSS
Short to VCC or driven high	FPWM	Enabled	Standard ±5% DRSS
Synchronizing Signal	FPWM	Enabled	Disabled

Transitioning the device from AUTO to FPWM mode requires driving the pin from low to high or sending a synchronization signal. Transitioning the device from FPWM to AUTO mode requires driving the pin from high to low or stop sending the synchronization signal. Note that a short to ground or a pullup to VCC requires < 200Ω resistor.

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7.3.3.1 MODE/SYNC Pin Uses for Synchronization

The LM656x5-Q1 MODE/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by coupling a positive edge into the pin. The coupled edge voltage at the pin must exceed the SYNC amplitude threshold of $V_{IH(SYNC)}$ to trip the internal synchronization pulse detector. The minimum SYNC ON pulse and OFF pulse durations must be longer than $t_{SYNC(TON-MIN)}$ and $t_{SYNC(TOFF-MIN)}$ respectively. The LM656x5-Q1 switching action can be synchronized to an external clock from 300kHz to 2.2MHz.

Note, an external SYNC signal can only be applied before or after pin detection. If applied during the pin detection, the SYNC signal can not be detected.

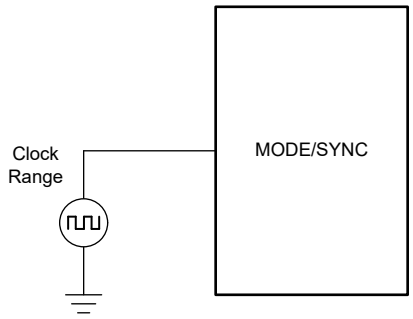
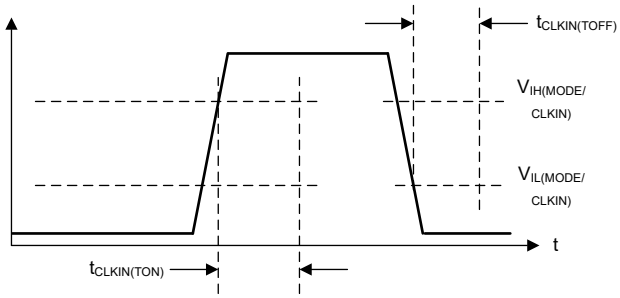


図 7-3. Typical Implementation Allowing Synchronization Using the MODE/SYNC Pin



This figure shows the conditions needed for detection of a synchronization signal.

図 7-4. Typical SYNC Waveform

7.3.3.2 Clock Locking

After a valid synchronization signal is detected, a clock locking procedure is initiated. After approximately 2048 pulses, the clock frequency locks to the frequency of the synchronization signal. While the switching frequency adjusts, phase is maintained so that the clock cycle lying between the operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. After frequency is adjusted, phase is adjusted over a few tens of cycles so that the rising synchronization edges correspond with the rising SW node pulses. See 図 7-5.

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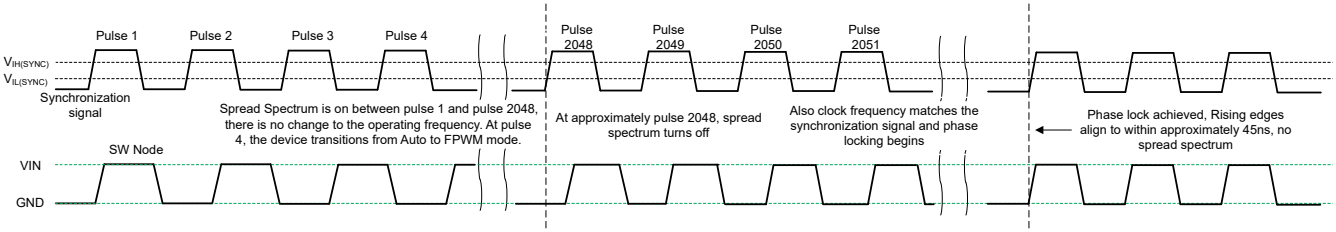

On the fourth pulse, the synchronization signal is detected. After approximately 2048 pulses, the synchronization signal is ready to synchronize, and the frequency is adjusted using a glitch-free technique, then the phase is locked.

図 7-5. Synchronization Process

7.3.4 Adjustable Switching Frequency

The RT pin is configurable. This pin can be tied to VCC for 400kHz operation, grounded for 2.2MHz operation, or a resistor to GND can be used to set an adjustable operating frequency; see 表 7-3. Note that if a resistor value falls outside of the recommended range the LM656x5-Q1 reverts to 400kHz or 2.2MHz. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC/MODE pin in セクション 7.3.3.1. The switching frequency can be programmed in the range of 300kHz to 2200kHz by placing a resistor from the RT pin to GND. See 式 4 and 図 7-6.

$$R_T(k\Omega) = \frac{16.4}{F_{SW}(MHz)} - 0.633 \quad (4)$$

For example, for f_{SW} = 400kHz, R_T = 40.37kΩ so a 40.2kΩ resistor can be selected as the closest value.

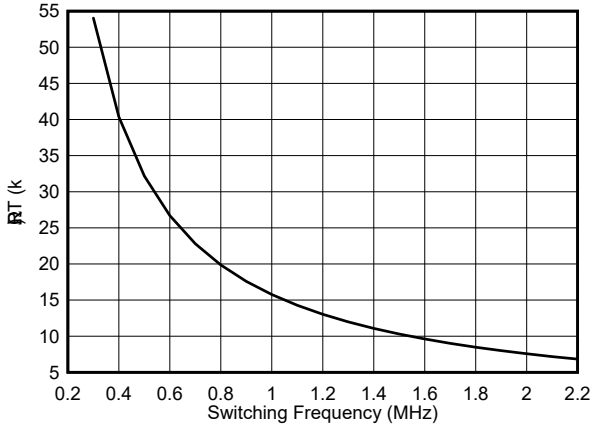

図 7-6. Switching Frequency vs RT

表 7-3. Switching Frequency Settings

RT	Switching Frequency
VCC	400kHz
GND	2200kHz
RT Resistor to GND	300kHz to 2200kHz
Float	Do not float

Note that a short to ground or a pullup to VCC requires < 200Ω resistor.

7.3.5 Dual Random Spread Spectrum (DRSS)

The LM656x5-Q1 provides a Dual Random Spread Spectrum (DRSS) function, which reduces the EMI of the power supply over a wide-frequency range. The DRSS function combines a low-frequency triangular modulation profile (standard or wide) with a high-frequency cycle-by-cycle pseudo-random modulation profile. The low

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frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

The low frequency triangular modulation profiles are pin-selectable. The standard low-frequency modulation profile spreads the switching frequency by ±5% with a 12kHz modulation frequency while the wide low frequency modulation profile spreads the switching frequency by ±10% with a 6kHz modulation frequency.

Spread spectrum works by converting a narrowband signal into a wideband signal which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, the CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance in the high and low RBWs with the low frequency triangular modulation and high-frequency cycle-by-cycle pseudo-random modulation. In the low-frequency band (150kHz – 30MHz), the DRSS function can reduce the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz – 108MHz) by as much as 5dBµV. The DRSS function is disabled when an external clock is applied to the MODE / SYNC pin.

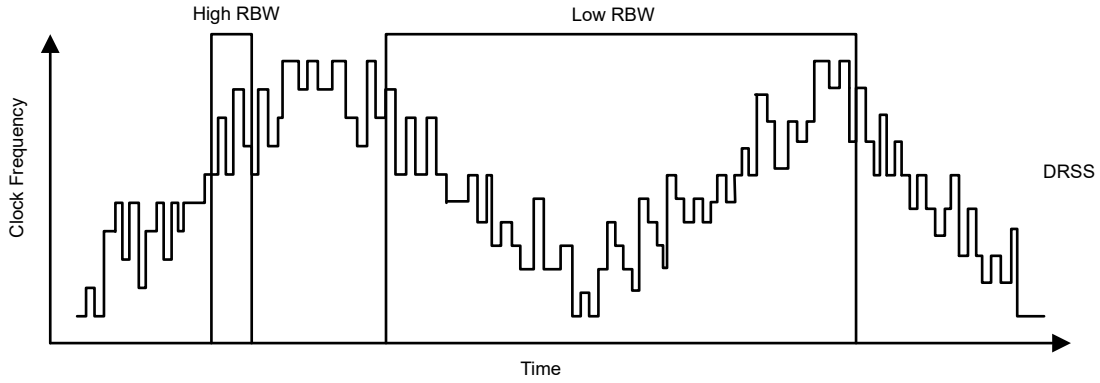

図 7-7. Dual Random Spread Spectrum Implementation

7.3.6 Internal LDO, VCC UVLO, and BIAS Input

The LM656x5-Q1 has a dual input for the VCC regulator that is supplied from either VIN or BIAS. After the LM656x5-Q1 is active, power comes from VIN if BIAS is less than approximately 3.1V. However power comes from BIAS if BIAS is more than 3.2V (maximum). VCC is typically 3.3V under most conditions, but can be lower if VIN is very low. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See $V_{CC\text{-}UVLO\_R}$ and $V_{CC\text{-}UVLO\_HYST}$ in *Electrical Characteristics*. TI recommends a 1µF capacitor rated for 10V with X7R or better dielectric for the VCC capacitor.

7.3.7 Bootstrap Voltage (BST Pin)

The driver of the power switch (HS switch) requires bias higher than VIN when the HS switch is ON. The capacitor connected between BST and SW works as a charge pump to boost voltage on the BST terminal to (SW + VCC). The boot diode is integrated on the LM656x5-Q1 die to minimize the physical design size. TI recommends a 100nF capacitor rated for 10V with X7R or better dielectric for the BST capacitor.

7.3.8 Soft Start and Recovery From Dropout

When designing with the LM656x5-Q1, slower rise in output voltage due to recovery from dropout and soft start must be considered separate phenomena. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see セクション 7.3.9.3.
- Recovery from shutdown due to overtemperature protection.
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is initiated, the IC takes the following actions:

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- The reference used by the IC to regulate output voltage is slowly ramping up from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of regulation value.
- Operating mode is set to auto, activating diode emulation. This allows start-up without pulling the output voltage low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see セクション 7.3.9.3.

All of these actions together provide a controlled start-up with limited inrush current. These actions also allow the use of output capacitors and loading conditions that can cause current limit during start-up without triggering hiccup. In addition, if the output voltage is already present the output voltage does not discharge.

Any time the output voltage is more than a few percent low for any reason, the output voltage ramps back up slowly. This is the recovery from dropout condition which differs from soft start in three important ways:

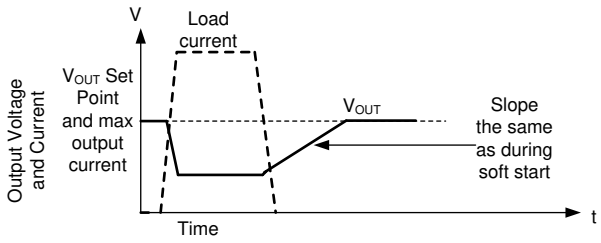
- Hiccup is allowed only if output voltage is less than 40 percent the set point. Note that during dropout regulation, hiccup is inhibited. See セクション 7.3.9.3.
- FPWM mode is allowed during recovery from dropout. If the output voltage were to suddenly be pulled up by an external supply, the LM656x5-Q1can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.
- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. The reference voltage is not started from zero.

Despite the name, recovery from dropout is active whenever output voltage is more than a few percent lower than the setpoint for long enough that:

- Duty factor is controlled by minimum on-time or
- When the part is operating in current limit.

This primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage for the desired output voltage to be generated.
- Overcurrent that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See セクション 7.3.9.3.



Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the setpoint is removed, output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, hiccup can, in principal, be triggered during recovery if output voltage is below 0.4 times output the setpoint for more than 128 clock cycles during recovery.

図 7-8. Recovery From Dropout

7.3.9 Safety Features

The LM656x5-Q1 includes a set of safety features:

- Power-Good monitor with output undervoltage (UV) and overvoltage (OV) protection
- Overcurrent and short-circuit protection with HICCUP mode
- Thermal shutdown (TSD)

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7.3.9.1 Power-Good Monitor

The LM656x5-Q1 includes a power-good function to simplify supply sequencing and supervision in a system. The power good function can be used to enable downstream circuits that are supplied by the LM656x5-Q1, control downstream protection circuits such as load switches, or to turn on sequenced supplies. The function monitors the output voltage with a window comparator through the FB pin for adjustable V_{OUT} configurations and the BIAS pin for fixed V_{OUT} configurations. The power-good output (PG) switches to a high impedance open-drain state when the output voltage is in regulation. When the output voltage is outside of the ±5% range from the set voltage, the PG pin is driven low (< $V_{OL(PG)}$) warning the system of an output over-voltage or under-voltage condition. A 114µs deglitch filter on the PG falling edge prevents false tripping of the power good signals during transients. When the output voltage returns within the regulation window, a 2ms filter on the PG rising edge allows extra processing time for the downstream components.

TI recommends a100kΩ pullup resistor from the PG pin to the relevant logic rail not greater than 30V. PG is asserted low during soft start and when the LM656x5-Q1 is disabled.

7.3.9.2 Overcurrent and Short-Circuit Protection

The LM656x5-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the minimum of a fixed current setpoint, or the output of the voltage regulation loop minus slope compensation, every switching cycle. Because the voltage loop has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle if duty cycle is above 35%.

When the LS switch is turned on, the current going through is also sensed and monitored. Like the high-side MOSFET, the low-side MOSFET turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if the current limit is exceeded, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit; see the *Electrical Characteristics* for values. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not turned on. The LS switch is turned off after the LS current falls below the limit. The HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

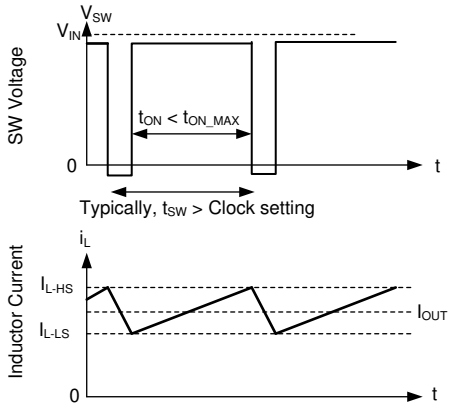

図 7-9. Current Limit Waveforms

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Because the current waveform assumes values between I_{L-HS} and I_{L-LS}, output current is close to the average of these two values unless duty cycle is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

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If the duty cycle is very high, current ripple must be very low to prevent instability; refer to セクション 8.2.2.4. Since the current ripple is low, the device is able to deliver the full load current. The current delivered is close to I_{L-LS}.

After the overload condition is removed, the device recovers as though in soft start; see セクション 7.3.8. Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.9.3 Hiccup

The LM656x5-Q1 employs hiccup overcurrent protection when all of the following conditions are met for 128 consecutive switching cycles:

- A time greater than t_{SS} has passed since soft start has started; see セクション 7.3.8.
- Output voltage is below approximately 0.4 times output setpoint.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts down and attempts to soft start after t_{HIC}. Hiccup mode helps reduce the device power dissipation under severe overcurrent and short circuit conditions.

7.3.9.4 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 165°C (typical) and power-good (PG) asserts. Thermal shutdown does not trigger below 155°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 156°C. When the junction temperature falls below 156°C (typical), the LM656x5-Q1 attempts to soft start.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.9V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops below 0.81µA.

7.4.2 Active Mode

The LM656x5-Q1 is in active mode when the following occurs:

- The EN pin is above $V_{EN\_TH\_R}$.
- V_{IN} is above $V_{IN\_UVLO\_R}$.
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See セクション 7.3 for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN\_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM656x5-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN}
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load
- A current limiting condition where the output voltage remains above 0.4 times the output setpoint
- Dropout mode when switching frequency is reduced to minimize dropout

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- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

7.4.2.1 Peak Current Mode Operation

The following operating description of the LM656x5-Q1 refers to セクション 7.2 and the waveforms in 図 7-10. Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

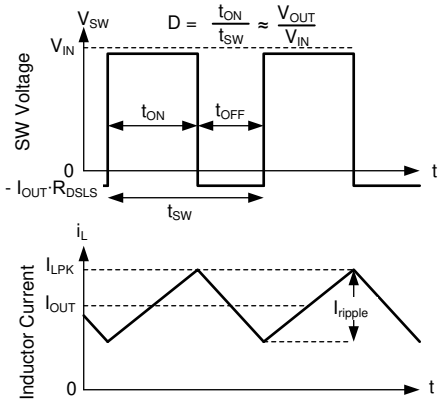

図 7-10. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.2.2 Auto Mode Operation

The LM656x5-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior known as FPWM mode, maintains full frequency even when unloaded. Which mode the LM656x5-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the part is in FPWM. When SYNC/MODE is low, the part is in PFM.

In auto mode, light-load operation is employed in the LM656x5-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency foldback

Note that while these two features operate together to create excellent light load behavior, these features operate independently of each other.

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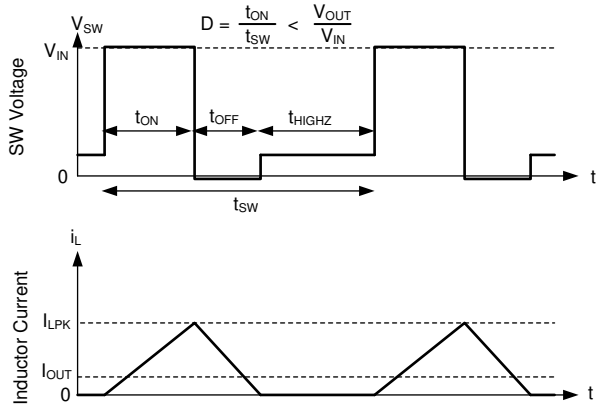
7.4.2.2.1 Diode Emulation

Diode emulation prevents reverse current though the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency is reduced when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off after inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the part operates in DCM. This is equivalent to saying that diode emulation is active.

図 7-11. PFM Operation

The LM656x5-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.2.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the *Electrical Characteristics* for reverse current limit values.

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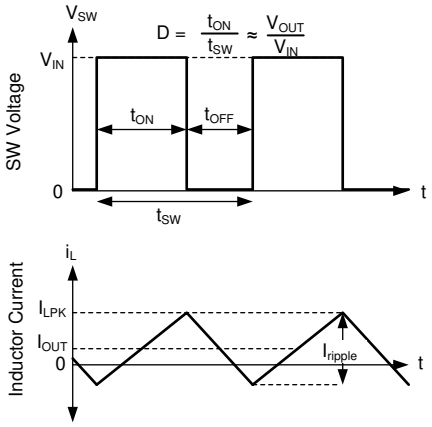

FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of Iripple.

図 7-12. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This allows good behavior during faults which involves the output being pulled up.

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8 Application and Implementation

注

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8.1 Application Information

The LM656x5-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5A, 3.5A, or 4.5A. The following design procedure can be used to select components for the LM656x5-Q1. Alternately, use the WEBENCH design tool to generate a complete design (WEBENCH). This tool uses an iterative design procedure and has access to a comprehensive database of components. This feature allows the tool to create an optimized design and allows the user to experiment with various options.

注

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias, the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This action can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

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8.2 Typical Application

図 8-1 and 図 8-2 show typical application circuits for the LM656x5-Q1, when using the adjustable output mode or the fixed output mode, respectively. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is designed for a certain range of external inductance and output capacitance. As a quick-start guide, 表 8-1 through 表 8-5 provide typical component values for a range of application parameters. The component values in these table represent stable designs and are not necessarily optimized. Note that the designs in these tables are based on a typical input voltage of 12V; or 36V for the 24V outputs.

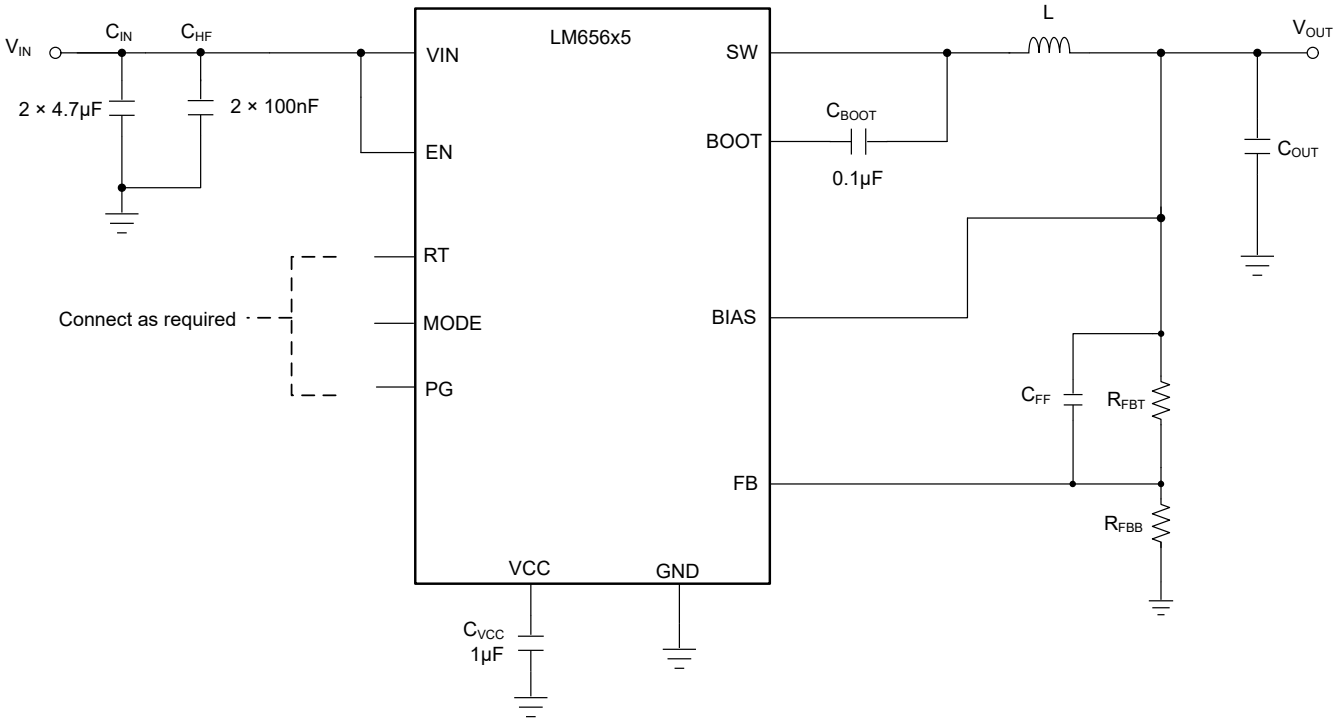

図 8-1. Example Application Circuit for Adjustable Output Voltage Mode With LM656x5

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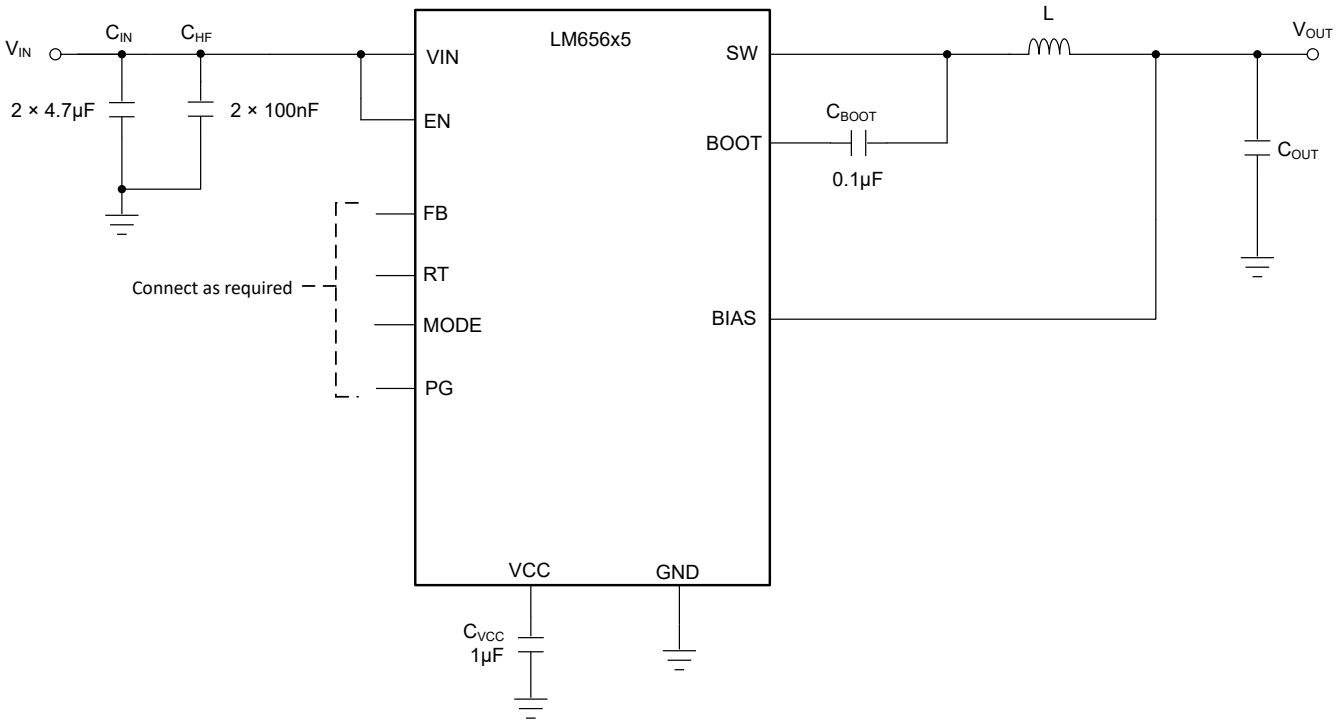

図 8-2. Example Application Circuit for Fixed Output Voltage Mode With LM656x5

表 8-1. Typical External Components for Fixed Output Voltage Mode

Output Voltage	Frequency	FB	LM6x625		LM6x635		LM6x645	
			L	COUT	L	COUT	L	COUT (1)
3.3V	400kHz	GND	8.2µH	75µF	6.8µH	94µF	5.6µH	110µF
3.3V	2200kHz	GND	1.5µH	20µF	1.5µH	25µF	1.0µH	30µF
5V	400kHz	VCC	10µH	50µF	8.2µH	55µF	8.2µH	70µF
5V	2200kHz	VCC	2.2µH	15µF	1.5µH	20µF	1.5µH	25µF

(1) Please note all COUT values are the de-rated output capacitor values in the tables.

表 8-2. Typical External Components for LM6x625 in Adjustable Output Voltage Mode

Output Voltage	Frequency	L	COUT(1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	8.2µH	75µF	100kΩ	31.6kΩ	20pF
5V	400kHz	10µH	50µF	100kΩ	19.1kΩ	20pF
24V	400kHz	47µH	15µF	205kΩ	7.15kΩ	
3.3V	2200kHz	1.5µH	25µF	100kΩ	31.6kΩ	5pF
5V	2200kHz	1.5µH	15µF	100kΩ	19.1kΩ	5pF
24V	2200kHz	8.2µH	10µF	205kΩ	7.15kΩ	

表 8-3. Typical External Components for LM6x635 in Adjustable Output Voltage Mode

Output Voltage	Frequency	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	6.8µH	70µF	100kΩ	31.6kΩ	10pF
5V	400kHz	10µH	60µF	100kΩ	19.1kΩ	15pF
24V	400kHz	47µH	25µF	205kΩ	7.15kΩ	10pF
3.3V	2200kHz	1.2µH	30µF	100kΩ	31.6kΩ	5pF
5V	2200kHz	1.5µH	20µF	100kΩ	19.1kΩ	5pF

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表 8-3. Typical External Components for LM6x635 in Adjustable Output Voltage Mode (続き)

Output Voltage	Frequency	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
24V	2200kHz	5.6µH	10µF	205kΩ	7.15kΩ	5pF

表 8-4. Typical External Components for LM6x645 in Adjustable Output Voltage Mode

Output Voltage	Frequency	L	COUT(1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	400kHz	5.6µH	80µF	100kΩ	31.6kΩ	15pF
5V	400kHz	8.2µH	70µF	100kΩ	19.1kΩ	15pF
24V	400kHz	22µH	30µF	205kΩ	7.15kΩ	10pF
3.3V	2200kHz	1.2µH	40µF	100kΩ	31.6kΩ	5pF
5V	2200kHz	1.2µH	30µF	100kΩ	19.1kΩ	5pF
24V	2200kHz	5.6µH	10µF	205kΩ	7.15kΩ	5pF

表 8-5. Typical External Components for Various Adjustable Output Voltage Applications

Output Voltage	Output Current	Frequency	L	COUT (1)	R_{FBT}	R_{FBB}	C_{FF}
3.3V	3.5A	1100kHz	3.3µH	45µF	N/A	N/A	N/A
1V	4.5A	500kHz	2.2µH	550µF	100kΩ	402kΩ	25pF
12V	3.5A	1100kHz	6.8µH	15µF	100kΩ	7.15kΩ	10pF
16V	3.5A	1600kHz	5.6µH	10µF	100kΩ	5.23kΩ	5pF

8.2.1 Design Requirements

The following example provides a detailed design procedure based on the specifications found in 表 8-6.

表 8-6. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	24V (typical)
Output voltage	5V
Maximum output current	0A to 3.5A
Switching frequency	2200kHz

8.2.2 Detailed Design Procedure

The following design procedure applies to 図 8-2 and 表 8-6.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM656x5-Q1device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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8.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this application example, we select a frequency of 2200kHz. In this case, the RT pin is connected to the GND. See セクション 7.3.4 for more details.

8.2.2.3 FB for Adjustable or Fixed Output Voltage Mode

this example uses the fixed output voltage mode to set the output voltage to 5V, by connecting the FB pin to the VCC pin.

If an output voltage different from either 3.3V or 5V is required, then the adjustable output voltage mode must be used. In that case, an external voltage divider must be connected between the output node and the FB pin, while 式 5 and 式 6 are used to determine the divider values.

$$R_{FBB} = R_{FBT} \times \frac{0.8}{V_{OUT} - 0.8} \tag{5}$$

$$100k\Omega \geq R_{FBB} \| R_{FBT} \geq 4k\Omega \tag{6}$$

Note that 式 6 states that the parallel combination of R_{FBB} and R_{FBT} must be greater than 4kΩ and less than 100kΩ. This limit is required because the regulator must reliably detect the sate of the FB pin during the start-up sequence to set the output voltage mode correctly.

If the adjustable output voltage mode was chosen for this example, then values of R_{FBT} = 100kΩ and R_{FBB} = 19.1kΩ satisfy both 式 5 and 式 6.

For more details, see セクション 7.3.1.

8.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current *rating* of the device. Experience shows that the best value for inductor ripple current is 30% of the maximum output current rating. Larger values of ripple current can restrict the maximum output current, before current limit is reached. Smaller values of ripple current reduce the SNR of the current mode controller and can lead to increased jitter in the duty cycle. Both the inductor and switching frequency tolerance have an impact on the selection of ripple current, and, therefore, inductor value. Use the maximum device current rating when calculating the ripple current for applications with much smaller maximum load than the maximum available from the device. The ratio of inductor ripple current over maximum output current is designated as K. 式 7 is used to determine the value of inductance

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times K \times I_{OUT-rated} \times F_{SW}} \tag{7}$$

The typical input voltage for the application is usually used in 式 7. However, if the application requires and very wide range of input voltages, then some voltage near the upper end of the range can be used. In any case, after the inductor has been selected, the ripple current must be checked at the maximum input voltage. Too large a ripple current can limit the maximum output current, as mentioned above. Use 式 8 to check for these concerns.

$$I_{OUT-max} \cong I_{HS-LIM} - \frac{1}{2} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times F_{SW}} \tag{8}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{HS-LIM}. This size makes sure that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise

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very rapidly. Although the valley current limit is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This rise can lead to component damage. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1MHz In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, the inductance value must not be less than that given in 式 9. This limit applies to applications where the switch duty cycle becomes greater than or equal to 50%, under any operating condition.

$$L_{min} \geq M \times \frac{V_{OUT}}{F_{SW}} \tag{9}$$

where

- M = 0.47 for the 2.5A device
- M = 0.35 for the 3.5A device
- M = 0.29 for the 4.5A device

The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

For this example, assuming a 24V input, 式 7 gives a value of 1.7µH. Use the next standard value of 2.2uH. Alternatively,表 8-1 can be used to select the inductor value for a typical input voltage of 12V.

8.2.2.5 Output Capacitor Selection

The current mode control scheme of the LM656x5-Q1 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. The best starting point for estimating the required output capacitance is to use the values in 表 8-1 through 表 8-5. The values found in those tables can be interpolated for other output voltages or switching frequencies. In general, higher output voltages and higher switching frequencies require less output capacitance. In addition, when using the adjustable output voltage mode, the C_{FF} capacitor can be used to optimize the loop performance.

After the output capacitance is selected, and assuming a low ESR ceramic is used, the approximate peak-to-peak output voltage ripple can be estimated using 式 10 and 式 11.

$$V_r \cong \frac{\Delta I}{8 \times F_{SW} \times C_{OUT}} \tag{10}$$

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times L} \tag{11}$$

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and Bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1nF to 100nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

The maximum output capacitance must be limited to approximately 10 times the design value, or 1000µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

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This example uses an output capacitance of 15µF, based on 表 8-1. Keep in mind that this represents the value after applying D.C. bias derating and any other applicable tolerance in the capacitance. This is true for all the values shown in the tables. Any ceramic capacitor, or combination of capacitors, with an X7R or better dielectric, that provides 15µF at 5V bias, can be used. The values shown in the table must be considered as typical to provide a stable design. Maximum and minimum limits on the output capacitance can be found by testing the application, as mentioned above.

8.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 2 × 4.7µF is required on the input of the regulator. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. This capacitance must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. The value can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a high frequency bypass capacitance of 2 × 100nF ceramic capacitor must be used at the input, as close a possible to the regulator. Place one capacitor on each side of the package and connected directly to the VIN and GND pins of the device. This requirement provides a high frequency bypass for the control circuits internal to the device.

For this example, 2 × 4.7µF, 100V, X7R (or better) ceramic capacitors are chosen. The 100nF capacitors must also be rated at 100V with an X7R dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is often desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator, or an input EMI filter is used. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by any inductance on the input. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from 式 12 and must be checked against the manufacturers maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \tag{12}$$

8.2.2.7 C_{BOOT}

The LM656x5-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the high-side gate driver for the power MOSFET, along with other critical control circuits. A high-quality ceramic capacitor of 100nF and at least 16V is required.

8.2.2.8 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This need can be accomplished by using the circuit shown in 図 8-3. The turn-on voltage is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then use 式 13 and 式 14 to calculate R_{ENT} and V_{OFF}.

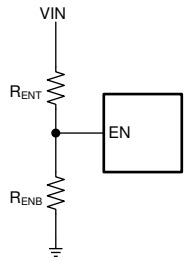

図 8-3. Setup for External UVLO Application

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$$R_{ENT} = R_{ENB} \times \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \quad (13)$$

$$V_{OFF} = V_{EN-L} \times \left(\frac{V_{ON}}{V_{EN-H}} \right) \quad (14)$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage

8.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the regulator dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LM656x5-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 15 shows the relationships between the important parameters. Higher ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note, the values given in the *Thermal Information* table are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. See the *Semiconductor and IC Package Thermal Metrics* application note for more information and the resources given at the end of this section.

$$I_{OUT_{MAX}} = \left(\frac{T_J - T_A}{R_{\theta JA}} \right) \times \left(\frac{\eta}{1-\eta} \right) \times \left(\frac{1}{V_{OUT}} \right) \quad (15)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature, flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The advanced package used for this regulator features a die attach paddle, or "thermal pad" (DAP), to provide a place to solder down to the PCB heat-sinking copper. This feature provides a good heat conduction path from the regulator junction to the heat sink and must be properly soldered to the PCB heat sink copper. A typical curve of $R_{\theta JA}$ versus copper board area can be found in 図 8-4. The copper area given in the graph is for each layer. The top and bottom layers are 2-oz. copper each, while the inner layers are 1 oz. Remember that the data given in this graph is for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors. As one data point, the LM65645EVM exhibits an approximate $R_{\theta JA}$ of about 25ºC/W for a copper area of about 58cm^2.

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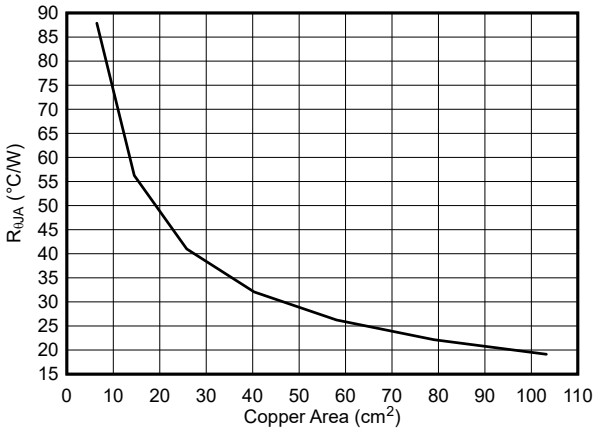

図 8-4. Thermal Resistance vs. Copper Area

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application report
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- *How to Properly Evaluate Junction Temperature with Thermal Metrics* application report

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8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings.*
- Do not exceed the *Recommended Operating Conditions.*
- Do not exceed the *ESD Ratings.*
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make the project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 16.

$$I_{IN} = \frac{V_{IN}}{V_{OUT}} \times \frac{I_{OUT}}{\eta} \tag{16}$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This action can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the regulator is dependent on the PCB layout, to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or input capacitors, and power ground, as shown in 図 8-5. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce

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the parasitic inductance. セクション 8.5.2 shows a recommended layout for the critical components of the LM656x5-Q1 .

- *Place the input capacitors as close as possible to the VIN pins and connect to ground through a short wide trace.*
- *Apply the symmetrical input capacitors technique* as shown in the LM65645EVM
- *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. The BOOT and SW pins are adjacent which simplifies the C_{BOOT} capacitor placement.
- *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise sources (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and also act as a heat dissipation path.
- *Connect the thermal pad to the ground plane.* The WQFN package has a thermal pad (PAD) connection that can be soldered down to the PCB ground plane. This pad acts as a heat-sink connection. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
- *Provide wide planes for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat sinking.* Enough copper area must be used to keep a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. With the WQFN package, use at least six heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies* application report
- *Simple Switcher PCB Layout Guidelines* application report
- *Construction Your Power Supply- Layout Considerations* seminar
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

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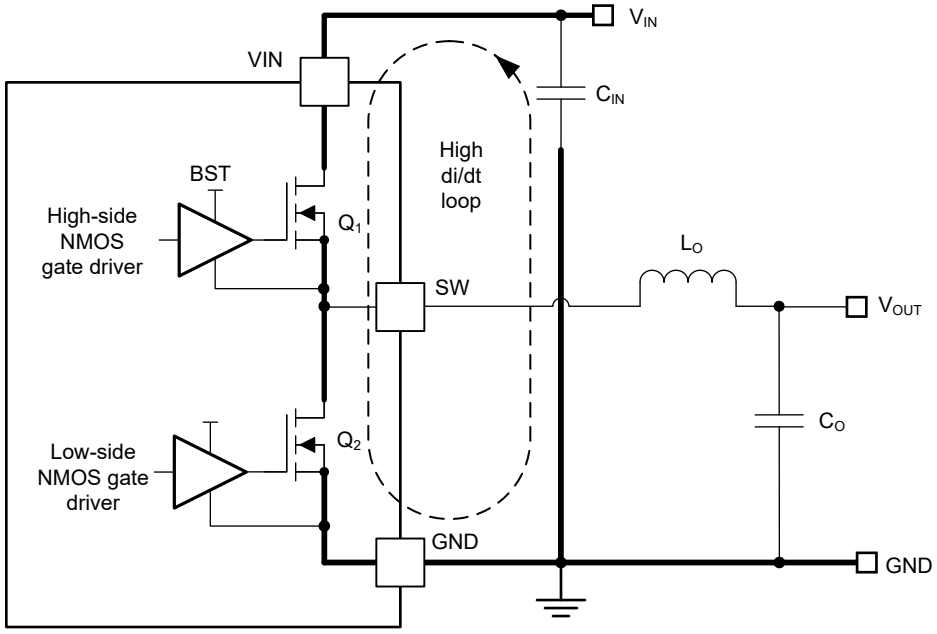

図 8-5. Current Loops With Fast Edges

8.5.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. PGND pins are connected directly to the source of the low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends providing adequate device heat sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum of six 10mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2oz / 1oz / 1oz / 2oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

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8.5.2 Layout Example

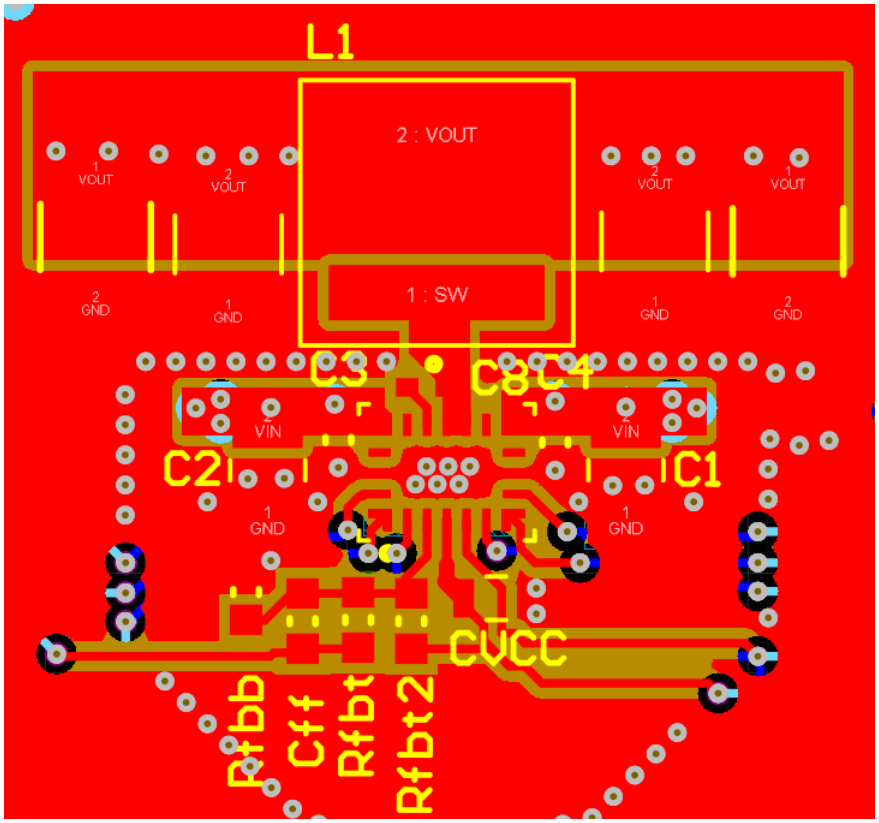

図 8-6. Layout Example

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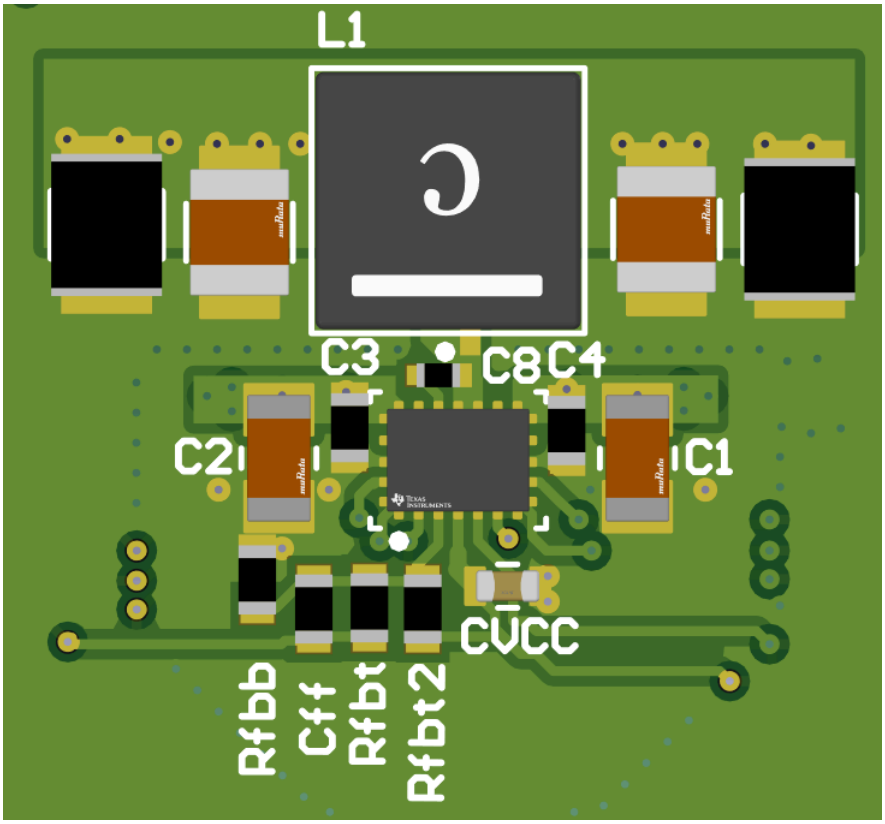

図 8-7. PCB Image

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9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM656x5-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight* application report
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- Texas Instruments, *How to Properly Evaluate Junction Temperature with Thermal Metrics* application report
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Simple Switcher PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations* seminar
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2024	*	Initial Release

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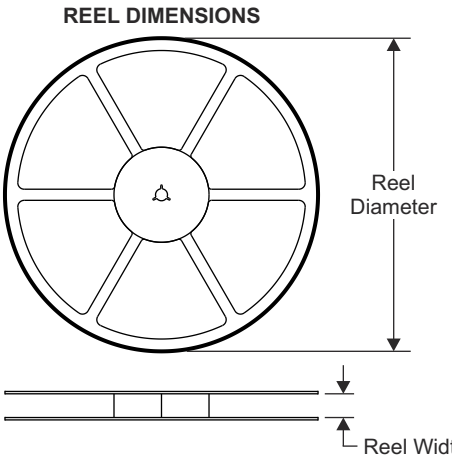
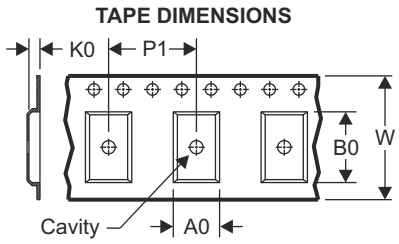
ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

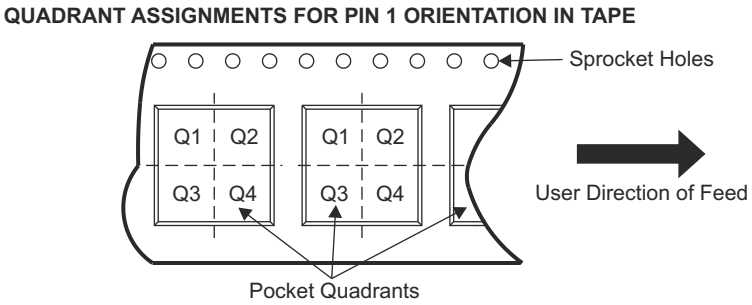
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM65645SRZTRQ1	QFN	RZT	20	3000	330	12.4	3.79	3.79	0.71	8.0	12.0	Q1

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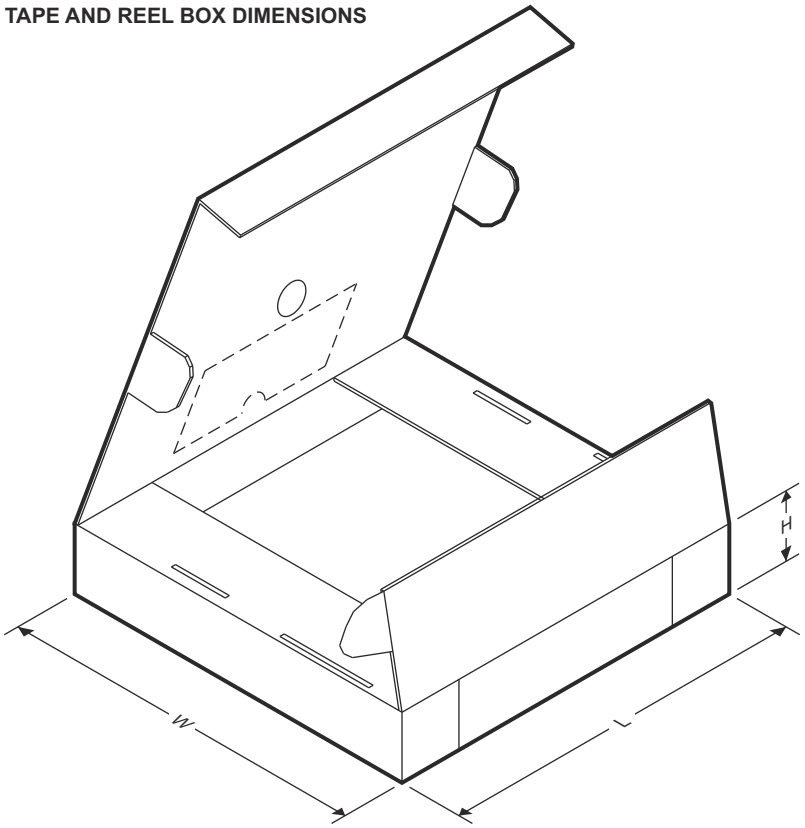
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM65645SRZTRQ1	QFN	RZT	20	3000	367	367	35

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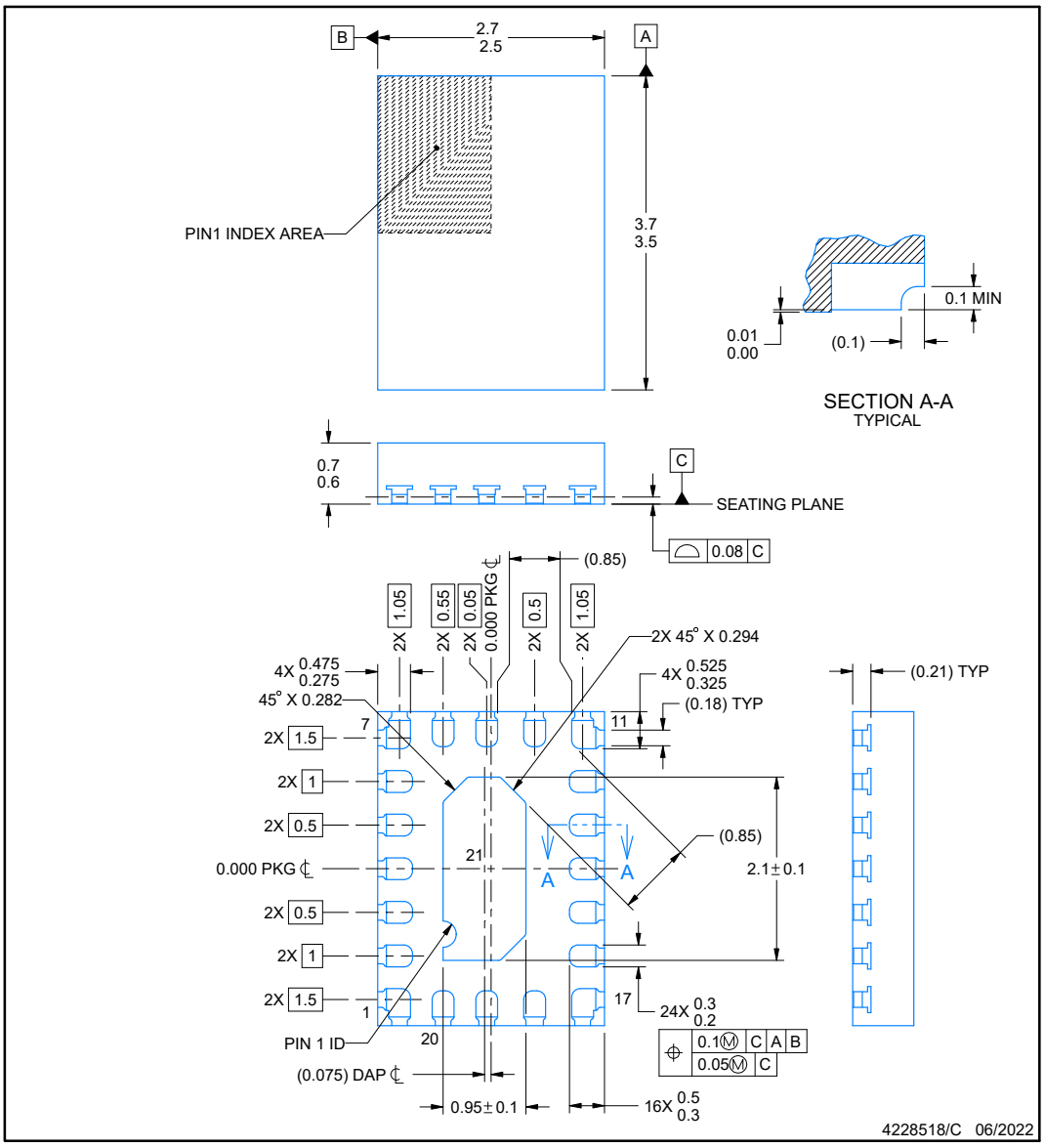
PACKAGE OUTLINE

RZT0020A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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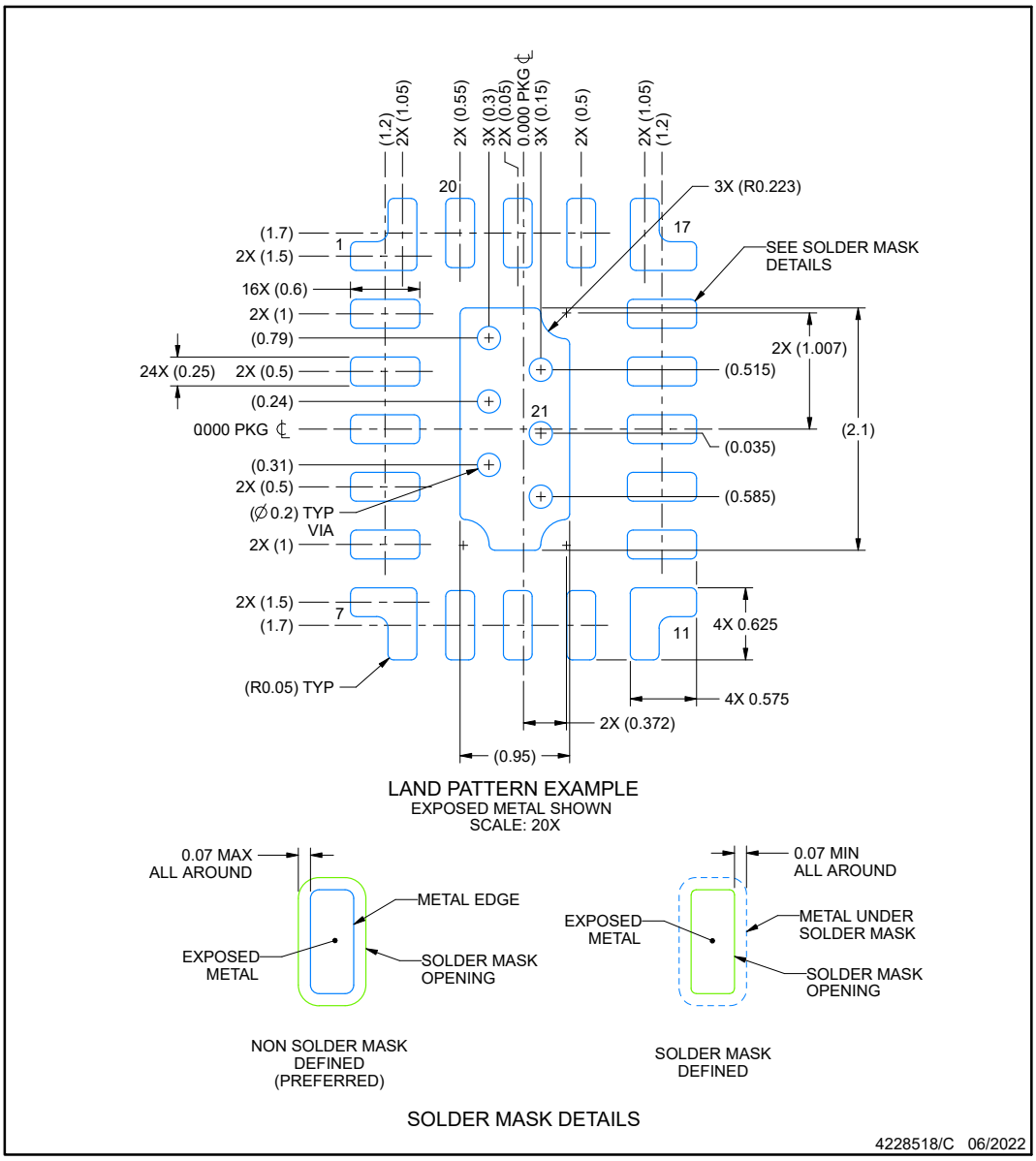
EXAMPLE BOARD LAYOUT

RZT0020A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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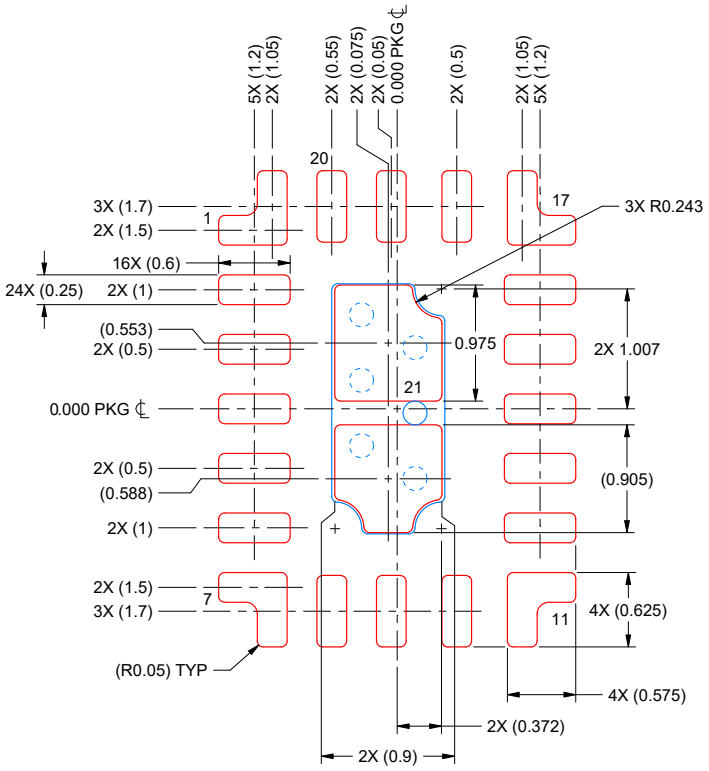
EXAMPLE STENCIL DESIGN

RZT0020A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

EXPOSED PAD 21:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4228518/C 06/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM65645SRZTRQ1	ACTIVE	WQFN-FCRLF	RZT	20	2500	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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