TEXAS INSTRUMENTS
LM74703-Q1, LM74704-Q1
JAJSOY6A – MAY 2023 – REVISED DECEMBER 2023

LM74703-Q1、LM74704-Q1 外部 FET の健全性表示機能搭載、車載用理想ダイオード コントローラ

1 特長

- 下記結果で AEC-Q100 認定済み
  - デバイス温度グレード 1:
    動作時周囲温度範囲:-40℃～125℃
- 3.2V～65V の入力範囲 (スタートアップ時 3.9V)
- 逆電圧定格:-65V
- 外部の N チャネル MOSFET 用のチャージ・ポンプ
- アノードからカソード ピンへの順方向電圧降下レギュレーション:20mV
- イネーブル・ピン機能
- シャットダウン時電流 (EN=LOW):1µA
- 動作時静止電流 (EN = HIGH):80µA
- ピーク・ゲート・ターンオフ電流:2.3A
- 外部 MOSFET の健全性状態を示す FETGOOD 出力
- 逆電流阻止に対する高速応答:
  < 0.75µs
- 拡張周波数範囲 (150kHz～1GHz) における EMI 性能
- 外部 TVS ダイオードにより車載用 ISO7637 過渡要件に適合
- 8 ピンの SOT-23 パッケージ (2.90mm × 1.60mm)

2 アプリケーション

- 車載用 ADAS システム - カメラ
- 車載用インフォテインメント・システム - デジタル計器クラスタ、ヘッド・ユニット
- 車体エレクトロニクスおよび照明
- 冗長化電源用のアクティブ OR

3 概要

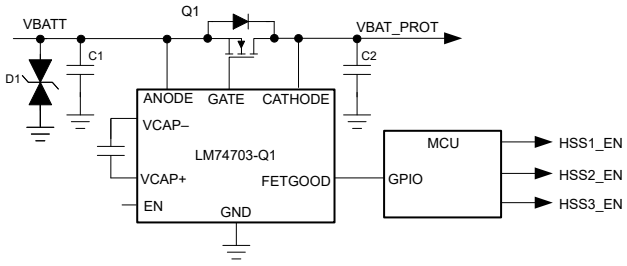
LM74703-Q1、LM74704-Q1 は、外部の N チャネル MOSFET と組み合わせることで理想ダイオード整流器として動作し、20mV の順方向電圧降下で低損失逆極性保護を実現する車載用 AEC Q100 認定済み理想的ダイオード コントローラです。入力電源電圧範囲が 3.2V～65V と広いため、12V、24V、48V の車載用バッテリ システムなどの一般的な DC バス電圧を制御できます。3.2V の入力電圧をサポートしているため、特に車載用システムの厳しいコールド クランク要件に向けた設計になっています。このデバイスは、最低 -65V の負の電源電圧に耐えられ、負荷を保護できます。

このデバイスは、MOSFET のゲートを制御し、順方向電圧降下を 20mV にレギュレートします。このレギュレーション方式により、逆電流発生時に MOSFET を穏やかにオフにでき、DC 逆電流をゼロにします。このデバイスは、逆電流阻止への応答が高速 (0.75µs 未満) なため、ISO7637 のパルス テスト時や電源障害および入力マイクロ短絡状況で出力電圧のホールドアップ要件を持つシステムに適用できます。LM74703-Q1、LM74704-Q1 には、外部 MOSFET ドレインからソースへの短絡またはオープン状態を示す FETGOOD 出力があります。このデバイスはイネーブル・ピン (EN) を備えています。イネーブル ピンが Low のとき、コントローラはオフで、消費電流は約 1µA です。

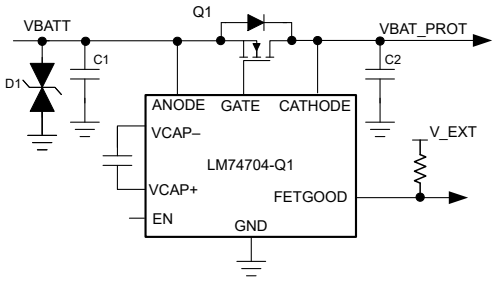
製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM74703-Q1	DDF (SOT-23、8)	2.90mm × 1.60mm
LM74704-Q1		

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



LM74703-Q1 の代表的なアプリケーション回路



LM74704-Q1 の代表的なアプリケーション回路

Table of Contents

4 Device Comparison Table

	LM74703-Q1	LM74704-Q1
FETGOOD Output Type	Push-Pull Output	Open-Drain Output

5 Pin Configuration and Functions

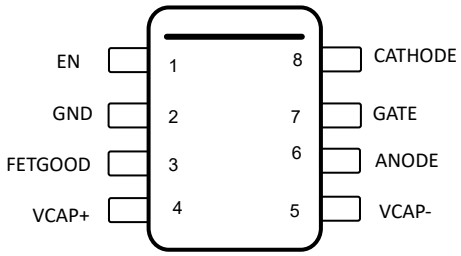


図 5-1. DDF Package, 8-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
2	GND	G	Ground pin.
3	FETGOOD	O	External MOSFET status indicator. LM74703-Q1 has push-pull while LM74704-Q1 has open drain FETGOOD output. When not used, FETGOOD pin can be left floating.
4	VCAP+	O	Charge pump output. Connect to external charge pump capacitor between VCAP+ and VCAP-.
5	VCAP-	I	Charge pump capacitor reference input.
6	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
7	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	ANODE, VCAP– to GND	–65	65	V
	EN to GND, $V_{(ANODE)}$ > 0 V	–0.3	65	V
	EN to GND, $V_{(ANODE)}$ ≤ 0 V	$V_{(ANODE)}$	(65 + $V_{(ANODE)}$)	V
Output pins	FETGOOD to GND	–0.3	80	V
	$I_{FETGOOD}$		1	mA
	GATE to ANODE	–0.3	15	V
	VCAP+ to VCAP–, ANODE	–0.3	15	V
Output to input pins	CATHODE to ANODE	–5	75	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011, CDM ESD classification level C4B	Corner pins (EN, VCAP+, VCAP– CATHODE)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	ANODE, VCAP– to GND	–60		60	V
	CATHODE to GND			60	
	EN to GND	–60		60	
Input to output pins	ANODE to CATHODE	–70			V
External capacitance	ANODE	22			nF
	CATHODE to GND, VCAP+ to VCAP–	0.1			µF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *セクション 6.5*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM74703-Q1, LM74704-Q1 DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to 125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4		60	V
$V_{(ANODE\ POR)}$	VANODE POR rising threshold				3.9	V
	VANODE POR falling threshold		2.2	2.8	3.1	V
$I_{(SHDN)}$	Shutdown supply current	$V_{(EN)}$ = 0 V		1	1.5	µA
$I_{(Q)}$	Operating quiescent current			80	130	µA
ENABLE INPUT						
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN\_IH)}$	Enable input high threshold		1.06	2	2.6	
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3	5	µA
FETGOOD						
FETGOOD High	FETGOOD voltage for logic high	VCAP > VCAP_UVLO, V_{ANODE} – $V_{CATHODE}$ < 200 mV, LM74703-Q1	4.45	5.2	6	V
$R_{FETGOOD(pullup)}$	FETGOOD pullup resistor	VCAP > VCAP_UVLO, V_{ANODE} – $V_{CATHODE}$ < 200 mV, LM74703-Q1		50		kΩ
$R_{FETGOOD(pulldown)}$	FETGOOD pulldown resistor	VCAP < VCAP_UVLO or V_{ANODE} – $V_{CATHODE}$ > 200 mV, LM74703-Q1		50		kΩ
$R_{FETGOOD(pulldown)}$	FETGOOD pulldown resistor	VCAP < VCAP_UVLO or V_{ANODE} – $V_{CATHODE}$ > 200 mV, LM74704-Q1		1	1.3	kΩ
FETGOOD Comparator	V_{AC} comparator rising threshold for FETGOOD going low		180	200	230	mV
FETGOOD Comparator	V_{AC} comparator falling threshold for FETGOOD going high		160	185	215	mV
FETGOOD Comparator hysteresis				15		mV
V_{ANODE} to $V_{CATHODE}$						
$V_{(AC\_REG)}$	Regulated forward $V_{(AC)}$ threshold		13	20	29	mV
$V_{(AC\_FC)}$	$V_{(AC)}$ threshold for full conduction mode		34	50	57	mV
$V_{(AC\_REV)}$	$V_{(AC)}$ threshold for reverse current blocking		–17	–11	–2	mV
GATE DRIVE						

T_J = –40°C to 125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV, $V_{(GATE)} – V_{(ANODE)}$ = 200 mV	3	11		mA
	Peak sink current	$V_{(ANODE)} – V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} – V_{(ANODE)}$ = 5 V		2370		mA
	Regulation max sink current	$V_{(ANODE)} – V_{(CATHODE)}$ = 0 V, $V_{(GATE)} – V_{(ANODE)}$ = 200 mV	6	26		µA
RDS_{ON}	Discharge switch RDS_{ON}	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV, $V_{(GATE)} – V_{(ANODE)}$ = 100 mV	0.4	1	2	Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge pump source current (charge pump on)	$V_{(VCAP+)} – V_{(VCAP–)}$ = 7 V	162	300	600	µA
	Charge pump sink current (charge pump off)	$V_{(VCAP+)} – V_{(VCAP–)}$ = 14 V		5	10	µA
$V_{(VCAP+)} – V_{(VCAP–)}$	Charge pump voltage at $V_{(ANODE)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA	8			V
	Charge pump turn on voltage		10.8	12.1	12.9	V
	Charge pump turn off voltage		11.6	13	13.9	V
	Charge pump enable comparator hysteresis		0.54	0.9	1.36	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(ANODE)}$ UV release at rising edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.8	6.6	7.7	V
	$V_{(VCAP)} – V_{(ANODE)}$ UV threshold at falling edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.11	5.68	6	V
CATHODE						
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = 12 V, $V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV		1.7	2	µA
		$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV		1.2	2.2	µA
		$V_{(ANODE)}$ = –12 V, $V_{(CATHODE)}$ = 12 V		1.25	2.06	µA

6.6 Switching Characteristics

T_J = –40°C to 125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to gate turn on delay	$V_{(VCAP)} > V_{(VCAP\ UVLOR)}$		75	115	µs
$t_{Reverse\ delay}$	Reverse voltage detection to gate turn off delay	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV to –100 mV		0.5	0.75	µs
$t_{Forward\ recovery}$	Forward voltage detection to gate turn on delay	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV to 700 mV		1.4	2.6	µs
$t_{FETGOOD\_ASSERT(DLY)}$	FETGOOD assert delay	$V_{ANODE} – V_{CATHODE}$ > 200 mV or VCAP < VCAP_UVLO to FETGOOD ↓		40	60	us
$t_{FETGOOD\_DEASSERT(DLY)}$	FETGOOD de-assert delay	$V_{ANODE} – V_{CATHODE}$ < 200 mV and VCAP > VCAP_UVLO to FETGOOD ↑		5		us

6.7 Typical Characteristics

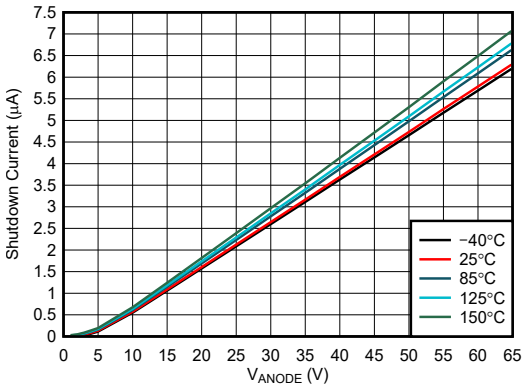


図 6-1. Shutdown Supply Current vs Supply Voltage

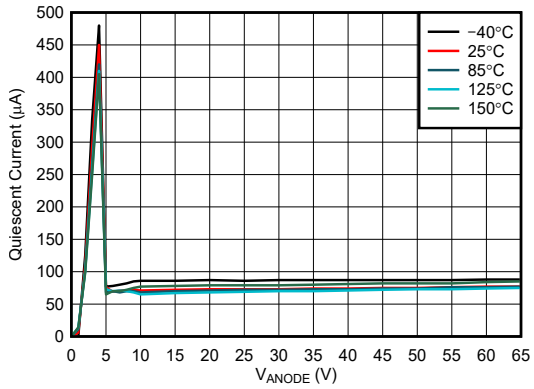


図 6-2. Operating Quiescent Current vs Supply Voltage

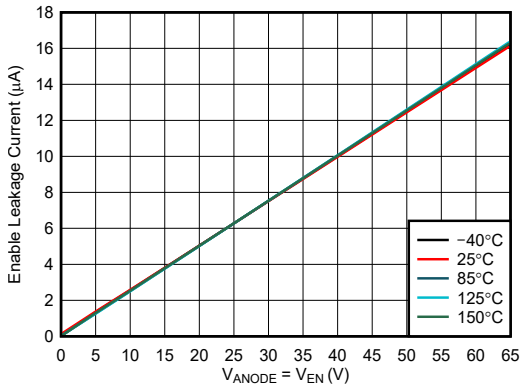


図 6-3. Enable Sink Current vs Supply Voltage

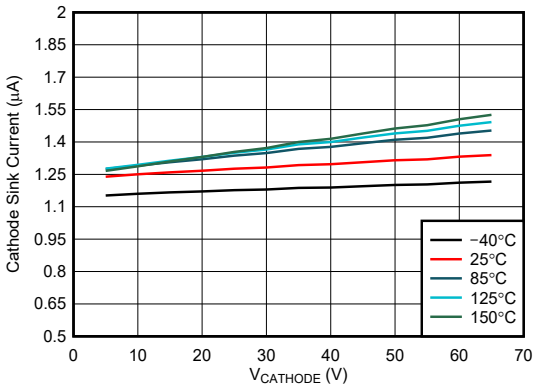


図 6-4. CATHODE Sink Current vs Supply Voltage

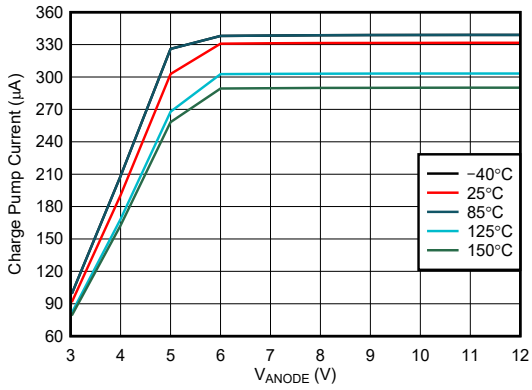


図 6-5. Charge Pump Current vs Supply Voltage at VCAP = 6 V

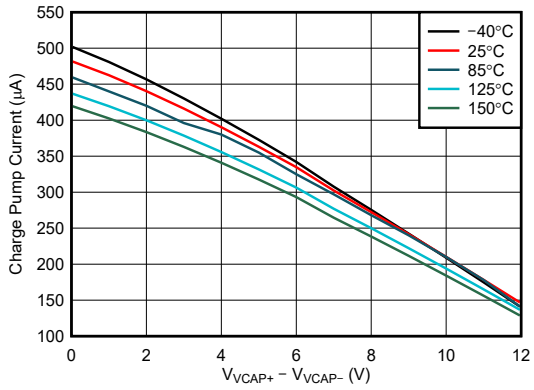


図 6-6. Charge Pump V-I Characteristics at ANODE >= 12 V

6.7 Typical Characteristics (continued)

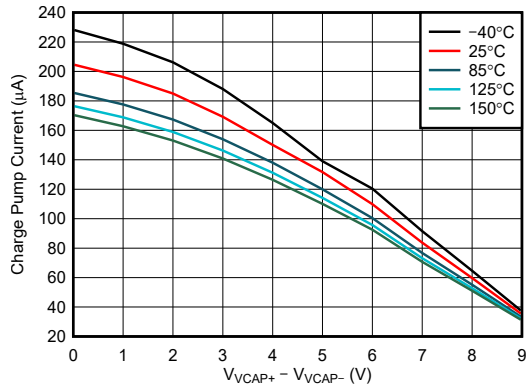


図 6-7. Charge Pump V-I Characteristics at ANODE = 3.2 V

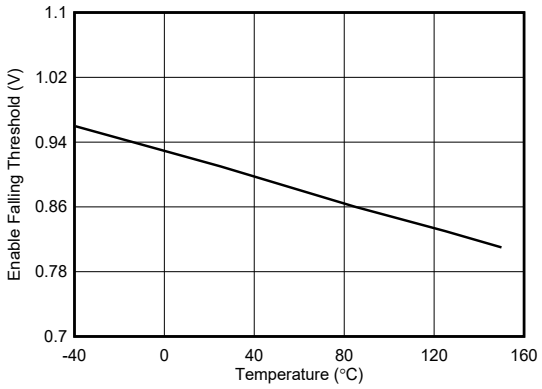


図 6-8. Enable Falling Threshold vs Temperature

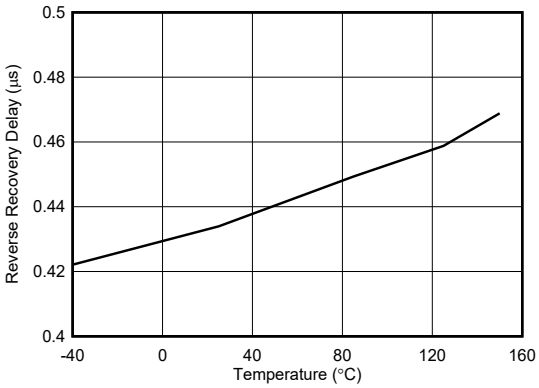


図 6-9. Reverse Current Blocking Delay vs Temperature

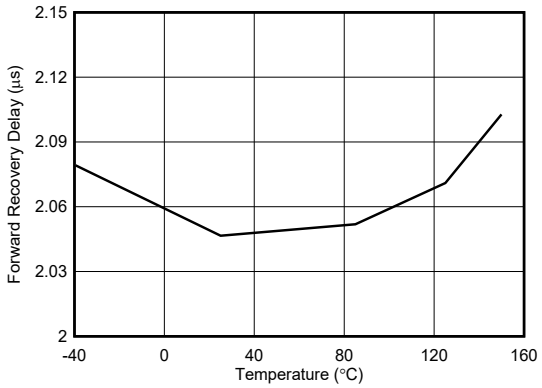


図 6-10. Forward Recovery Delay vs Temperature

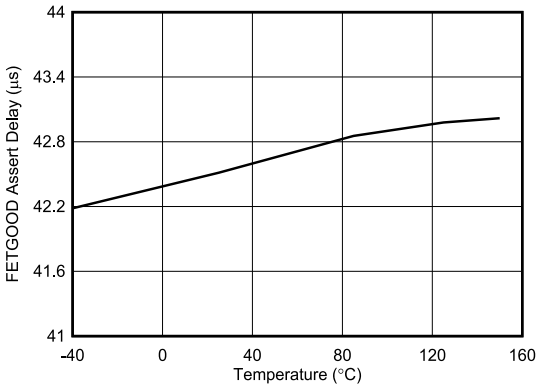


図 6-11. FETGOOD Assert Delay

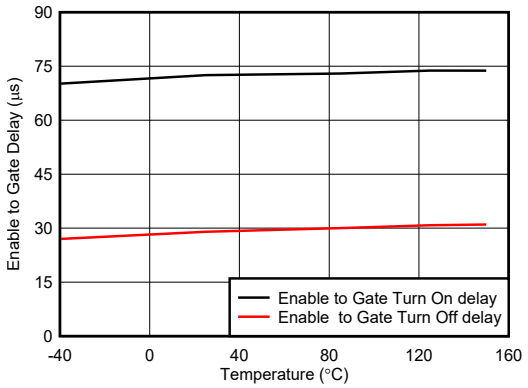


図 6-12. Enable to Gate Delay vs Temperature

6.7 Typical Characteristics (continued)

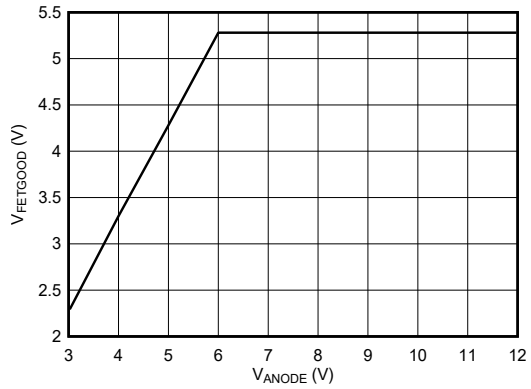


図 6-13. LM74703-Q1 FETGOOD Output Level (Push-Pull Variant)

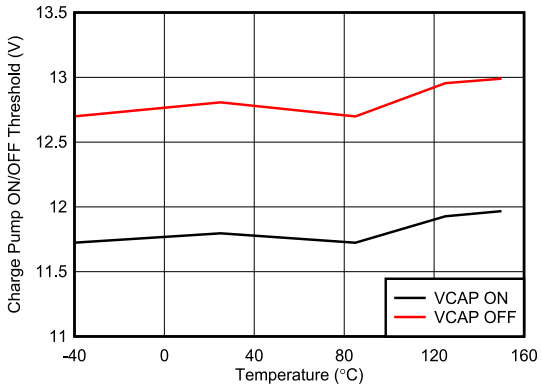


図 6-14. Charge Pump ON/OFF Threshold vs Temperature

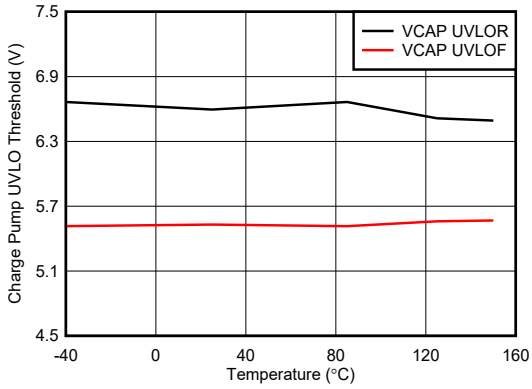


図 6-15. Charge Pump UVLO Threshold vs Temperature

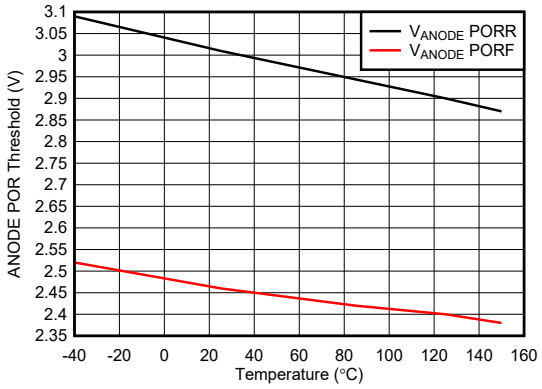


図 6-16. ANODE POR Threshold vs Temperature

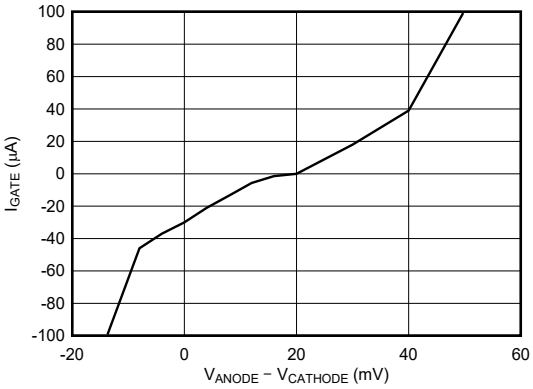


図 6-17. Gate Current vs Forward Voltage Drop

7 Parameter Measurement Information

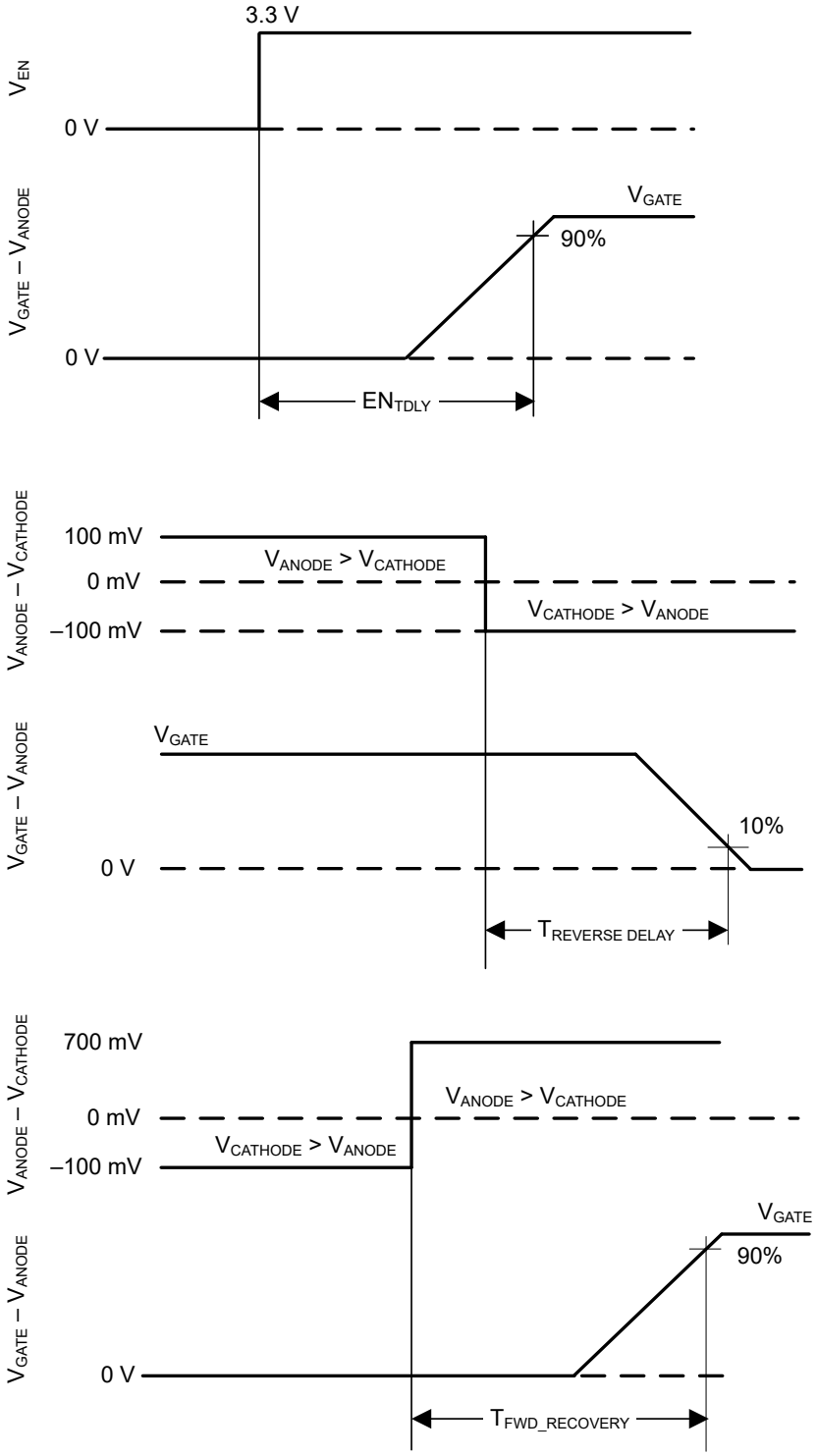


図 7-1. Timing Waveforms

8 Detailed Description

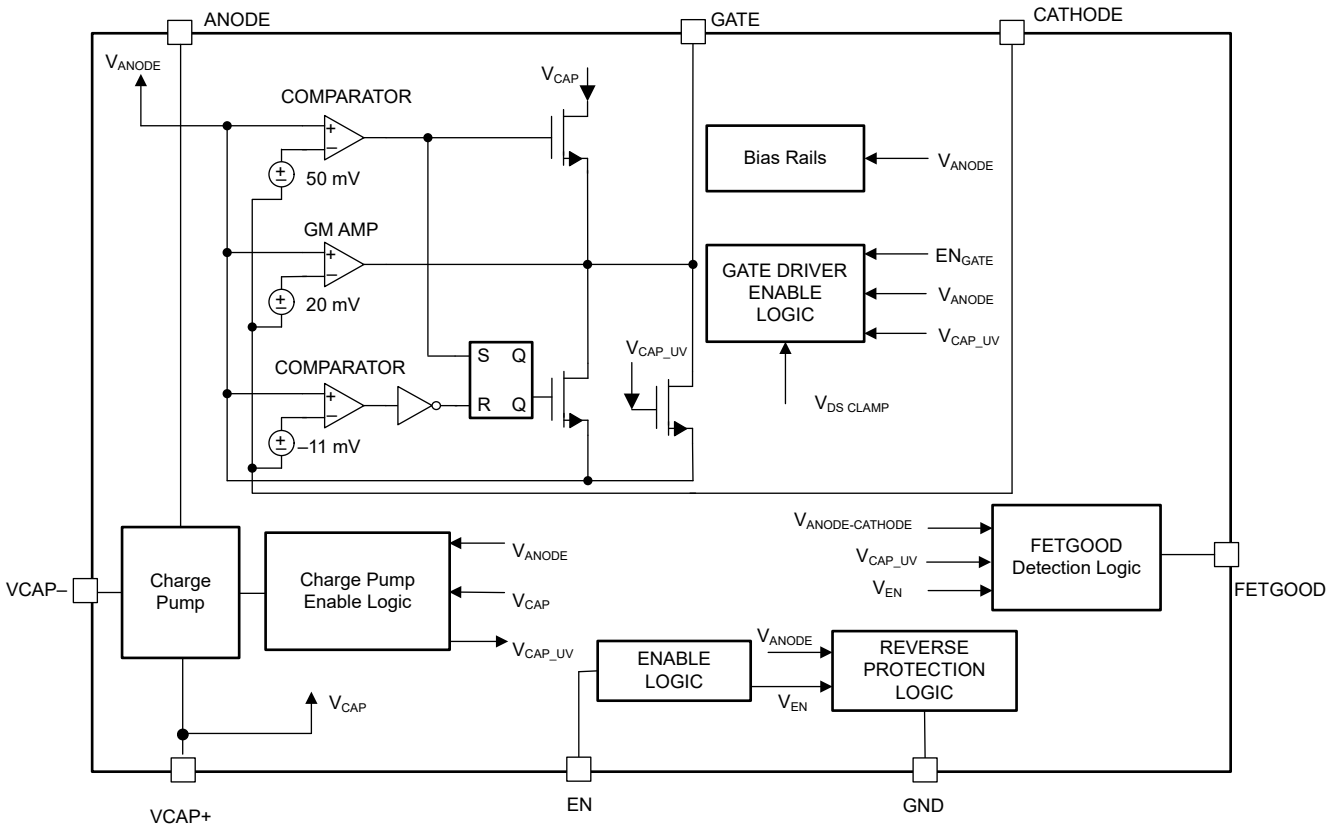
8.1 Overview

The LM74703-Q1 and LM74704-Q1 ideal diode controllers have all the features necessary to implement an efficient and fast reverse polarity protection circuit. The devices can be used in an ORing configuration while minimizing the number of external components. This easy-to-use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes like a P-channel MOSFET or a Schottky diode. An internal charge pump drives the external N-Channel MOSFET to a maximum gate-to-source drive voltage of approximately 12 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE pin voltages are adjusted as needed to regulate the forward voltage drop at 20 mV. This closed-loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and provides zero DC reverse current flow. A fast reverse current condition is detected when the voltage across the ANODE and CATHODE pins reduces below –11 mV. This behavior connects the GATE pin internally to the ANODE pin, turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the LM74703-Q1 in shutdown mode, disabling the N-Channel MOSFET and minimizing the quiescent current.

LM74703-Q1 and LM74704-Q1 offer an external FET health monitoring feature with the FETGOOD pin. The device monitors for external FET drain-to-source short or open condition during power-up and pulls the FETGOOD pin low in case the external FET fault condition is diagnosed.

For automotive applications like automotive lighting, camera modules that are typically exterior facing require low conducted and radiated emissions in the frequency band ranging up to few Gigahertz (GHz). LM74703-Q1 and LM74704-Q1 offer low emissions in high-frequency band, making these devices a good candidate for applications where emissions in high-frequency band are a key consideration.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The ANODE pin is used to power the internal circuitry of the LM74703-Q1, LM74704-Q1 typically drawing 80 µA when enabled and 1 µA when disabled. If the ANODE pin voltage is greater than the POR rising threshold, then LM74703-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from –65 V to 65 V, allowing the device to withstand negative voltage transients.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP+ and VCAP– pins to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor, the EN pin voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled, the charge pump sources a charging current of 300-µA typical. If EN pins is pulled low, then the charge pump remains disabled. To make sure that the external MOSFET can be driven above the specified threshold voltage of the MOSFET, the VCAP+ to VCAP–voltage must be above the undervoltage lockout threshold, which is typically 6.6 V, before the internal gate driver is enabled. Use 式 1 to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = 75\ \mu s + C_{VCAP} \times \frac{V_{VCAP\_UVLOR}}{300\ \mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP\_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive, approximately 900 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP+ to VCAP–voltage reaches the typical 13 V, typically, at which point the charge pump is disabled, decreasing the current drawn on the ANODE pin. The charge pump remains disabled until the VCAP+ to VCAP– voltage is below the typical 12.1 V, enabling the charge pump. The voltage between VCAP+ to VCAP– continue to charge and discharge between 12.1 V and 13 V as shown in 図 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74703-Q1 is reduced. When the charge pump is disabled, the charge pump typically sinks 5 µA.

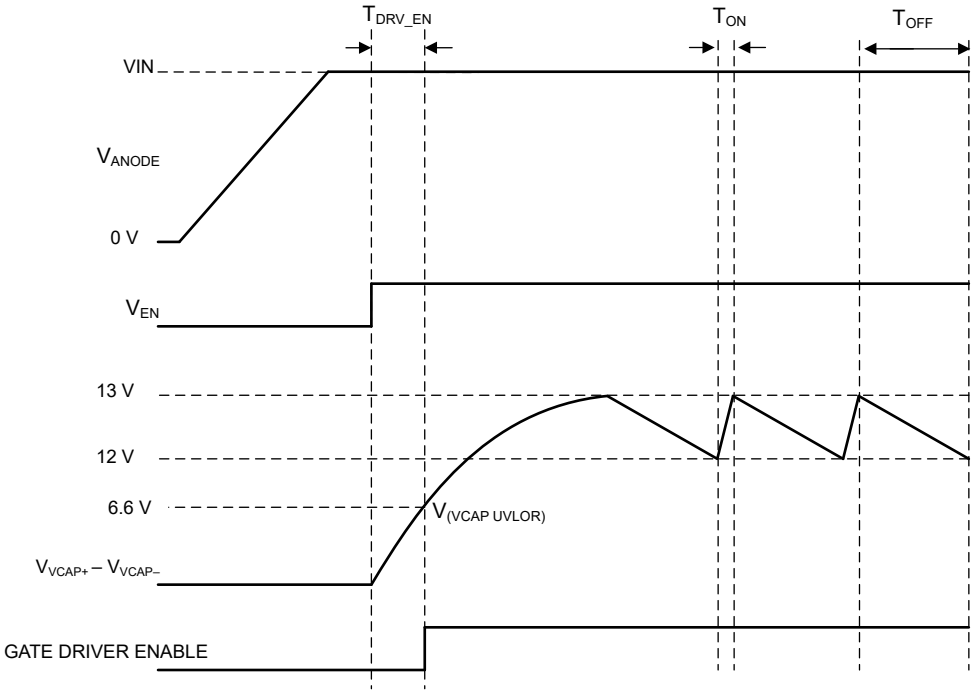


図 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. According to the ANODE to CATHODE voltage, there are three defined modes of operation that the gate driver operates under: forward regulation, full conduction mode, and reverse current protection. Forward regulation mode, full conduction mode, and reverse current protection mode are described in more detail in the *Regulated conduction Mode*, *Full Conduction Mode*, and *Reverse Current Production Mode* sections. 図 8-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74703-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE pin voltages are –11 mV.

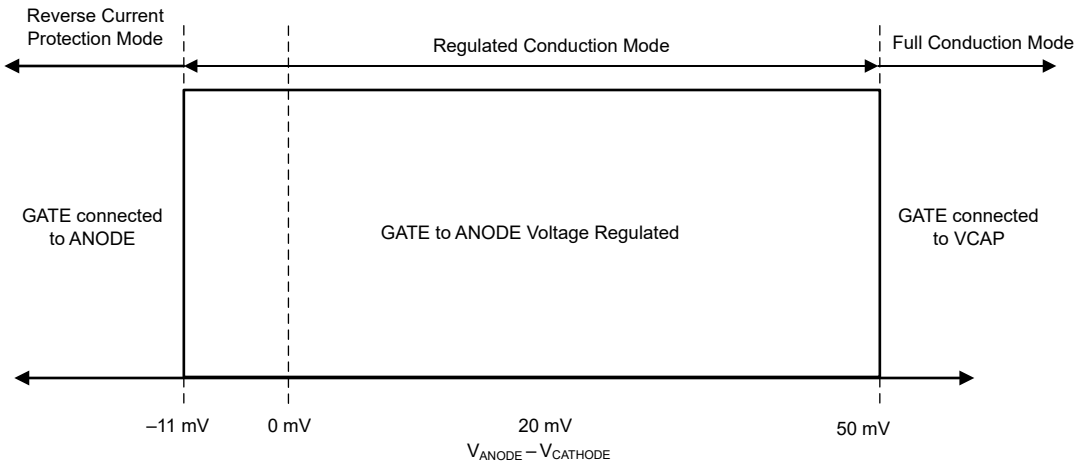


図 8-2. Gate Driver Mode Transitions

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP+ to VCAP– voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than V_{ANODE} POR rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE pin voltage.

8.3.4 Enable

The LM74703-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74703-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –65 V. This range allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 uA pulls the EN pin low and disables the device.

8.3.5 FET Status Indication (FETGOOD)

LM74703-Q1 and LM74704-Q1 have FETGOOD pin, which can be used to detect external MOSFET health, such as in cases where a MOSFET is short or open. The device monitors the external MOSFET source to drain voltage drop to decide MOSFET status as either MOSFET open or MOSFET short condition. The FETGOOD pin is pulled low whenever a MOSFET fault condition is detected.

MOSFET source to drain short detection is performed and status is indicated at each start-up event (ANODE ramp-up or EN pin going from low to high). For MOSFET source to drain short detection to work correctly, the device ANODE pin voltage must be 200 mV higher than the CATHODE pin voltage before performing external MOSFET short diagnosis.

For ideal diode configuration when the controller is off, output loads are always powered through the body diode of the external MOSFET. Detecting if the external MOSFET is completely turned-on or not before turning on downstream loads is important for avoiding large currents flowing through the body diode of MOSFET, which can potentially damage the MOSFET. This condition can arise due to gate voltage not getting applied to the MOSFET gate pin under specific fault condition, such as a MOSFET gate pin open due to a PCB manufacturing defect. LM74703-Q1 and LM74704-Q1 monitor external MOSFET source-to-drain drops and pulls the FETGOOD pin low if this drop is higher than 200 mV, even when the gate voltage is applied to the MOSFET. This behavior helps the system to monitor the MOSFET off condition during start-up (even when ideal diode controller is enabled) and indicate the MOSFET open fault using FETGOOD pin so that a decision on system level can be taken to turn off downstream loads to avoid large load current flowing through the body diode of the MOSFET. MOSFET open detection is available during device start-up as well as during normal operation.

The FETGOOD pin is also pulled low if the charge pump voltage is lower than the charge pump UVLO threshold of 6.6 V indicating gate drive voltage is not enough to fully enhance the MOSFET.

LM74703-Q1 has a push-pull FETGOOD output to support systems where there are not external pullups or bias voltages available when the system starts-up.

LM74704-Q1 has an open-drain FETGOOD output. The FETGOOD pin must be pulled to an external bias voltage through a pullup resistor. The external pullup resistor must be selected such that current through the FETGOOD pulldown switch is less than 1-mA to stay within the recommended operating conditions.

When not used, the FETGOOD pin must be left floating.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74703-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN\_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74703-Q1 enters low I_Q operation with the ANODE pin only sinking 1 µA. When the LM74703-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the body diode of the MOSFET.

8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE pin voltage of the LM74703-Q1. Each of the three modes is described in the *Regulated Condution Mode*, *Full Conduction Mode* and *Reverse Current Protection Mode* sections.

8.4.2.1 Regulated Conduction Mode

For the LM74703-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be within range to result in an ANODE to CATHODE pin voltage drop of –11 mV to 50 mV. During forward regulation mode, the ANODE to CATHODE pin voltages are regulated to 20 mV by adjusting the GATE to ANODE pin voltage. This closed loop regulation scheme provides graceful turn off of the MOSFET at very light loads and provides zero DC reverse current flow.

8.4.2.2 Full Conduction Mode

For the LM74703-Q1 to operate in full conduction mode the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE pin voltage drop of greater than 50-mV typical. If these conditions are achieved, the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE pin voltages being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE pin the $R_{DS(ON)}$ of the external MOSFET is minimized reducing the power loss of the external MOSFET when forward currents are large.

8.4.2.3 Reverse Current Protection Mode

For the LM74703-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the *Gate Driver* section and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE pin voltage is typically less than –11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM74703-Q1, LM74704-Q1 is used with an N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in 図 9-1 where the LM74703-Q1, LM74704-Q1 is used in series with a battery to drive the MOSFET Q1. The external TVS diode is not required for the LM74703-Q1 and LM74704-Q1 to operate, but the TVS diode is used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

9.2 Typical Application

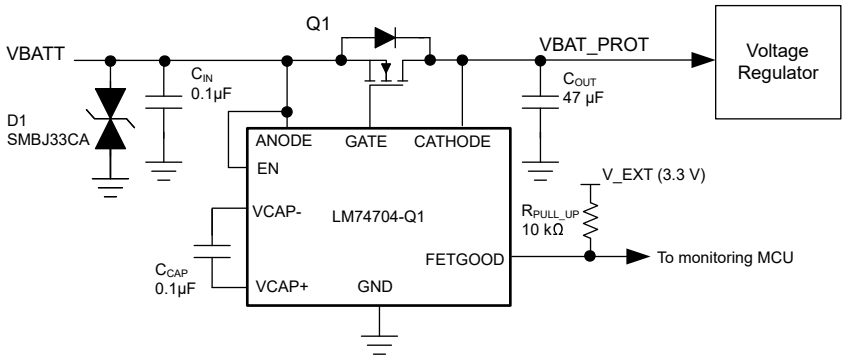


図 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters listed in 表 9-1 is presented.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 12-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A Nominal, 6-A Maximum
Output capacitance	1-µF Minimum, optional 47-µF Hold Up Capacitance
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

9.2.2.2 MOSFET Selection

Important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum source current through body diode, and the drain-to-source On resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application, including any anticipated fault conditions. Using MOSFETs with voltage rating up to 60-V maximum with the LM74704-Q1 is recommended because the ANODE and CATHODE pin maximum voltage rating is 65 V. The maximum V_{GS} that the LM74704-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} must be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level. During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ is not always beneficial. Higher $R_{DS(ON)}$ provides increased voltage information to the reverse comparator of the LM74704-Q1 at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Operating the MOSFET in regulated conduction mode during nominal load conditions is recommended as well as selecting $R_{DS(ON)}$ such that at nominal operating current the forward voltage drop V_{DS} is close to 20-mV regulation point and not more than 50 mV.

As a guideline, choose $(20\ mV / I_{Load(Nominal)}) \leq R_{DS(ON)} \leq (50\ mV / I_{Load(Nominal)})$.

MOSFET manufacturers typically specify $R_{DS(ON)}$ at 4.5-V V_{GS} and 10-V V_{GS}. $R_{DS(ON)}$ increases drastically below 4.5-V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th}. For stable regulation at light load conditions, operating the MOSFET close to 4.5-V V_{GS} is recommended, which is much higher than the MOSFET gate threshold voltage. Choosing a MOSFET with a typical gate threshold voltage V_{th} of 2 V to 2.5 V is recommended. Choosing a lower V_{th} MOSFET also reduces the turn ON time.

Based on the design requirements, the preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 3-A nominal current: $(20\ mV / 3\ A) \leq R_{DS(ON)} \leq (50\ mV / 3\ A) = 6.67\ m\Omega \leq R_{DS(ON)} \leq 16.67\ m\Omega$
- MOSFET gate threshold voltage V_{th}: 2 V typical

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to make sure that the junction temperature (T_J) is well controlled.

9.2.2.3 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP, input and output capacitance are:

- VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x $C_{ISS(MOSFET)}$(µF)
- C_{IN}: minimum 22 nF of input capacitance
- C_{OUT}: minimum 100 nF of output capacitance

9.2.2.4 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in 図 9-2, a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car. These transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

Two important specifications are breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche, similar to a Zener diode, and is specified at a low current value (typical 1 mA). The breakdown voltage must be higher than worst-case steady state voltages seen in the system. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74703-Q1 and LM74704-Q1 (65 V). The breakdown

voltage of TVS- must be beyond the maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high-current pulse situations. This voltage is much higher than the breakdown voltage. TVS diodes are designed to clamp transient pulses and must not interfere with steady-state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This behavior translates to 15 A flowing through the TVS- and the voltage across the TVS is close to the clamping voltage.

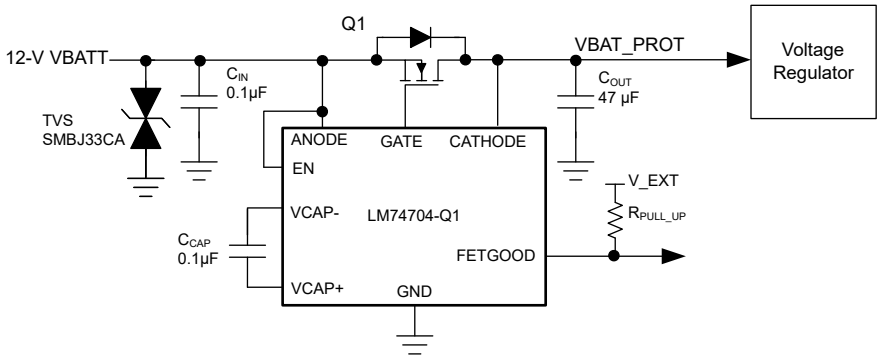


図 9-2. Typical 12-V Battery Protection With Single Bidirectional TVS

The next criterion is that the absolute maximum rating of anode-to-cathode reverse voltage of the LM74703-Q1 and LM74704-Q1 (–75 V) and the maximum V_{DS} rating MOSFET must not be exceeded. In the design example, 60-V rated MOSFET is selected and the maximum limit on the cathode to anode voltage is 60 V.

In case of an ISO 7637-2 pulse 1, the anode of LM74703-Q1, LM74704-Q1 is pulled down by the ISO pulse and clamped by TVS-. The MOSFET is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- must not exceed (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection applications. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During an ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –42 V with 15 A of peak surge current as shown in 図 9-5 and meets the clamping voltage ≤ 44 V.

The SMBJ series of TVS diodes are rated up to 600-W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

9.2.2.5 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

A typical 24-V battery protection application circuit shown in 図 9-3. This circuit uses two unidirectional TVS diodes to protect from positive and negative transient voltages.

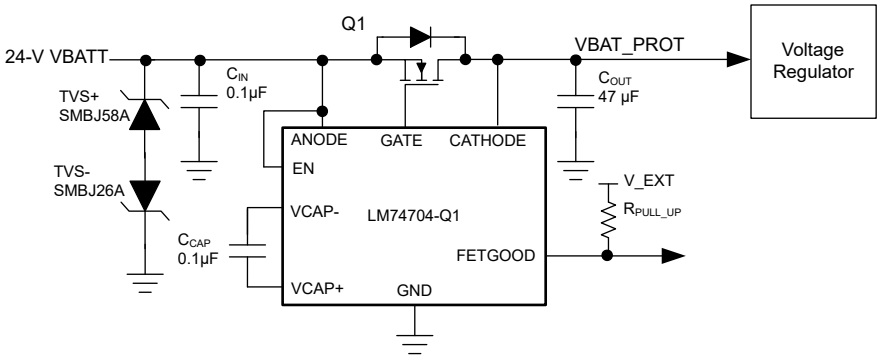


図 9-3. Typical 24-V Battery Protection With Two Unidirectional TVS

The breakdown voltage of the TVS+ must be higher than the 48-V jump start voltage, less than the absolute maximum ratings of the anode and enable pin of the LM74703-Q1 and LM74704-Q1 (65 V) and must withstand 65-V suppressed load dump. The breakdown voltage of TVS- must be lower than the maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This behavior translates to 12 A flowing through the TVS-. The clamping voltage of the TVS- can not be the same as that of the 12-V battery protection circuit because during the ISO 7637-2 pulse, the ANODE to CATHODE pin voltage seen is equal to (-TVS Clamping voltage + Output capacitor voltage). For a 24-V battery application, the maximum battery voltage is 32 V, which indicates that the clamping voltage of the TVS- must not exceed, 75 V – 32 V = 43 V.

Single bidirectional TVS can not be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65 V, maximum clamping voltage is ≤ 43 V and the clamping voltage can not be less than the breakdown voltage. Two unidirectional TVS that are connected back-to-back need to be used at the input. For the positive side TVS+, the SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, the SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage of –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with the SMBJ26A and SMBJ58A connected back-to-back at the input.

9.2.3 Application Curves

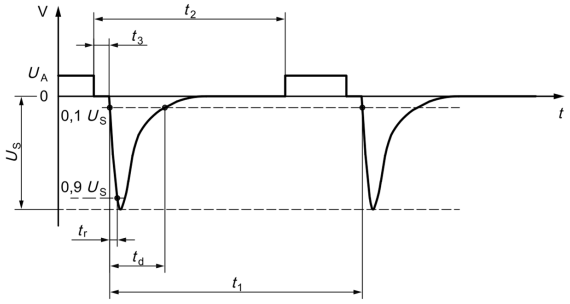
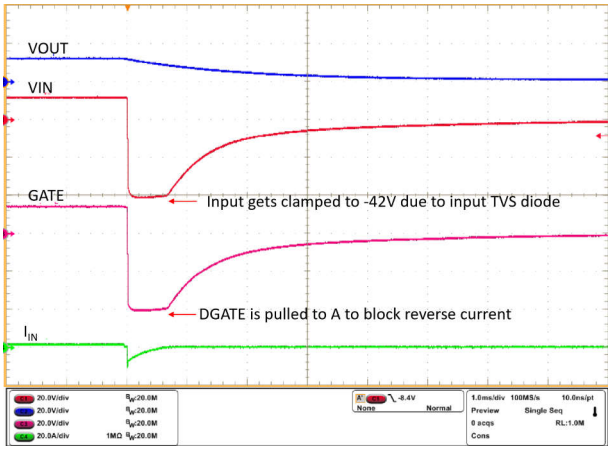
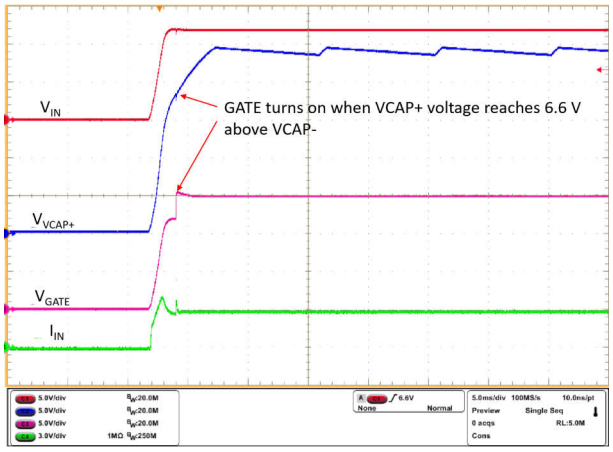


図 9-4. ISO 7637-2 Pulse 1



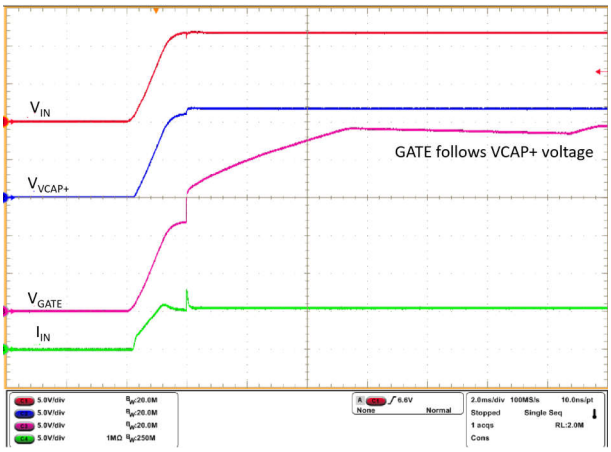
Time (1 ms/DIV)

図 9-5. Response to ISO 7637-2 Pulse 1



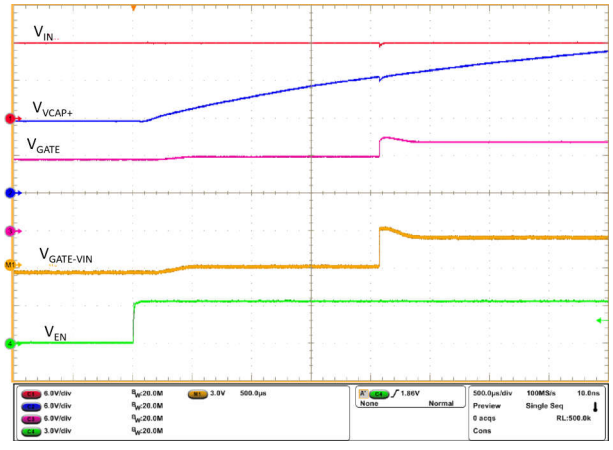
Time (5 ms/DIV)

図 9-6. Start-up With 3-A Load



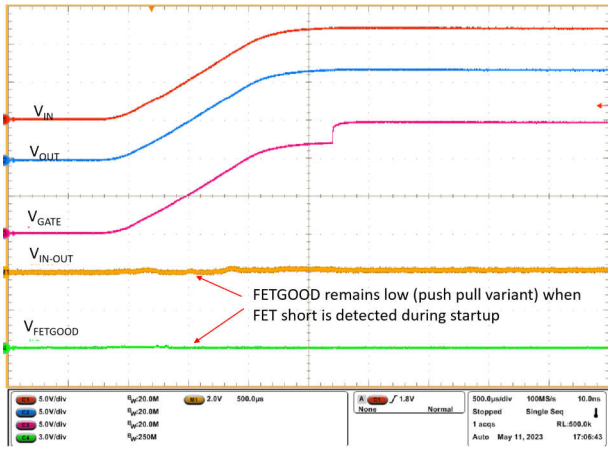
Time (2 ms/DIV)

図 9-7. Start-up With 5.8-A Load



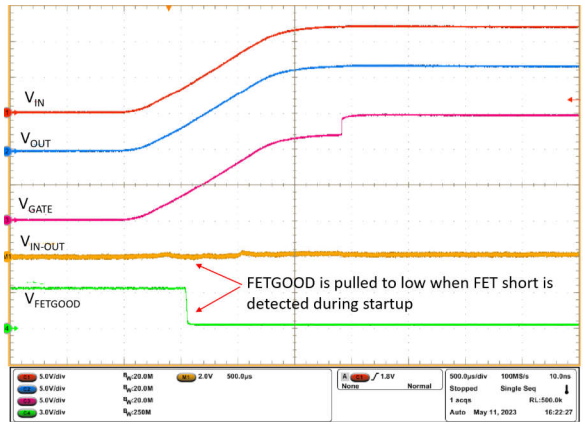
Time (0.5 ms/DIV)

図 9-8. Device Start-up With EN Toggle



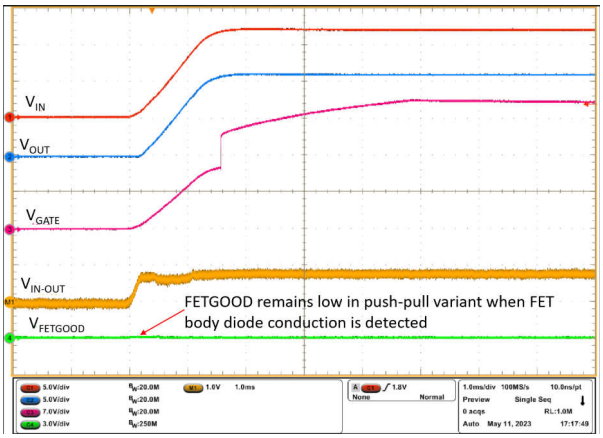
Time (0.5 ms/DIV)

図 9-9. FETGOOD During Start-up With FET Short (LM74703-Q1)



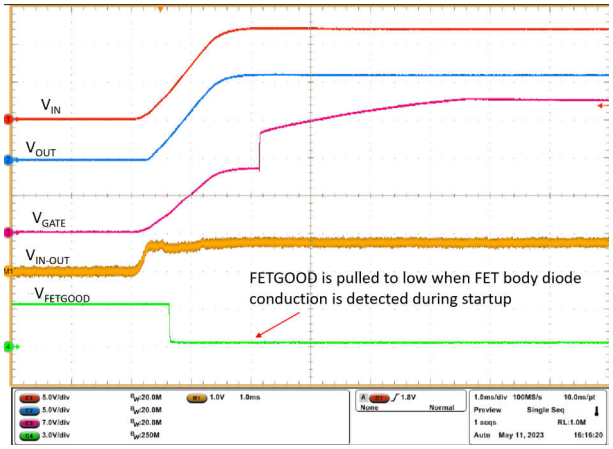
Time (0.5 ms/DIV)

図 9-10. FETGOOD During Start-up With FET Short (LM74704-Q1)



Time (1 ms/DIV)

図 9-11. FETGOOD During Start-up With FET Off or GATE Pin Open (LM74703-Q1)



Time (1 ms/DIV)

図 9-12. FETGOOD During Start-up With FET Off or GATE Pin Open (LM74704-Q1)

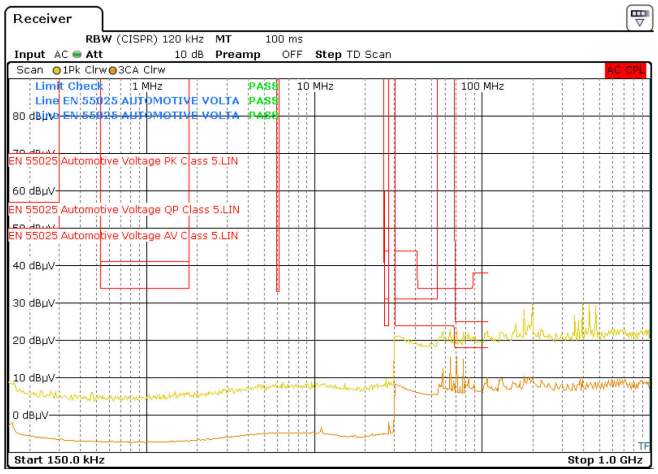


図 9-13. LM74703-Q1, LM74704-Q1 Conducted EMI Performance (150 kHz to 1 GHz)

9.3 Power Supply Recommendations

The LM74703-Q1, LM74704-Q1 Ideal Diode Controller is designed for the supply voltage range of 3.2 V ≤ V_{ANODE} ≤ 65 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 100 nF is recommended. To prevent LM74703-Q1 and surrounding components from damage under the conditions of a direct output short circuit, using a power supply with overload and short circuit protection is necessary.

9.4 Layout

9.4.1 Layout Guidelines

- Connect ANODE, GATE, and CATHODE pins of LM74703-Q1, LM74704-Q1 close to the SOURCE, GATE, and DRAIN pins of the MOSFET.
- The high current path of this design is through the MOSFET, using thick traces for source and drain of the MOSFET to minimize resistive losses is important.
- The charge pump capacitor across VCAP+ and VCAP– pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The GATE pin of the LM74703-Q1, LM74704-Q1 must be connected to the MOSFET gate with a short trace. Avoid excessively thin and long traces to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increases in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and produces good results.

9.4.2 Layout Example

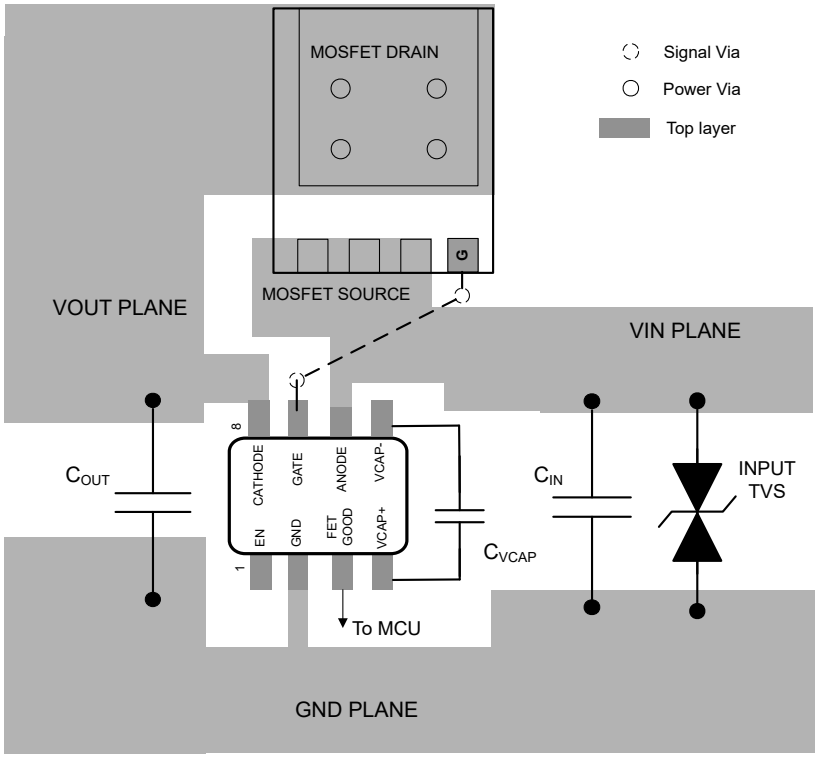


図 9-14. LM74703-Q1 DDF Package Example Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Texas Instruments, *LM74704Q1EVM: LM74704-Q1 and LM74703-Q1 evaluation module for ideal diode controllers*, product page

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (December 2023)	Page
• ドキュメントのステータスを「*事前情報*」から「*量産データ*」に変更	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74703QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L703Q	Samples
LM74704QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	L704Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

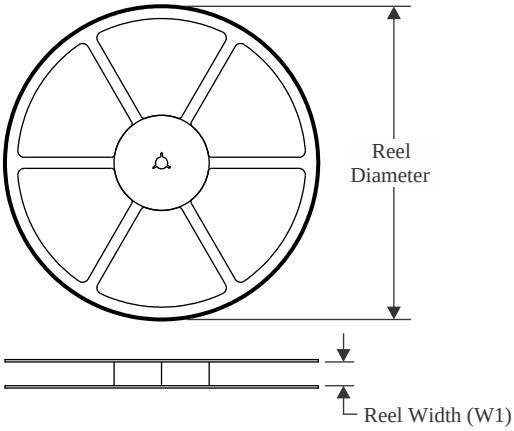
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

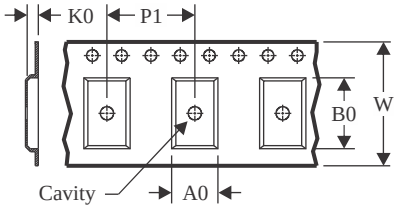
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

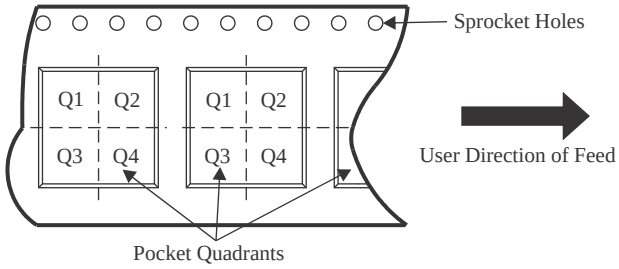


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

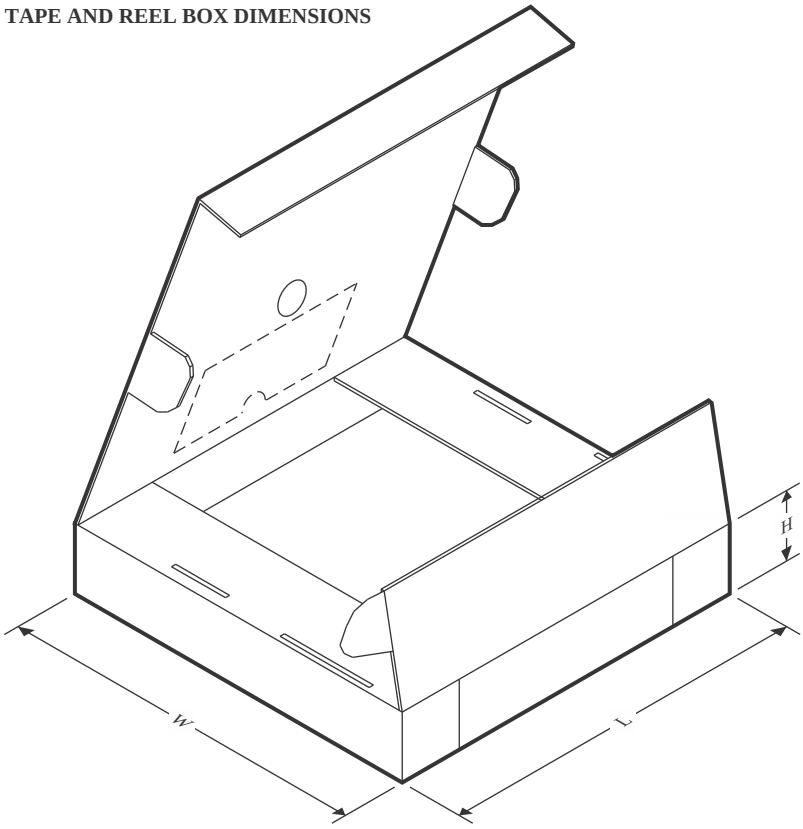
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74703QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3
LM74704QDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

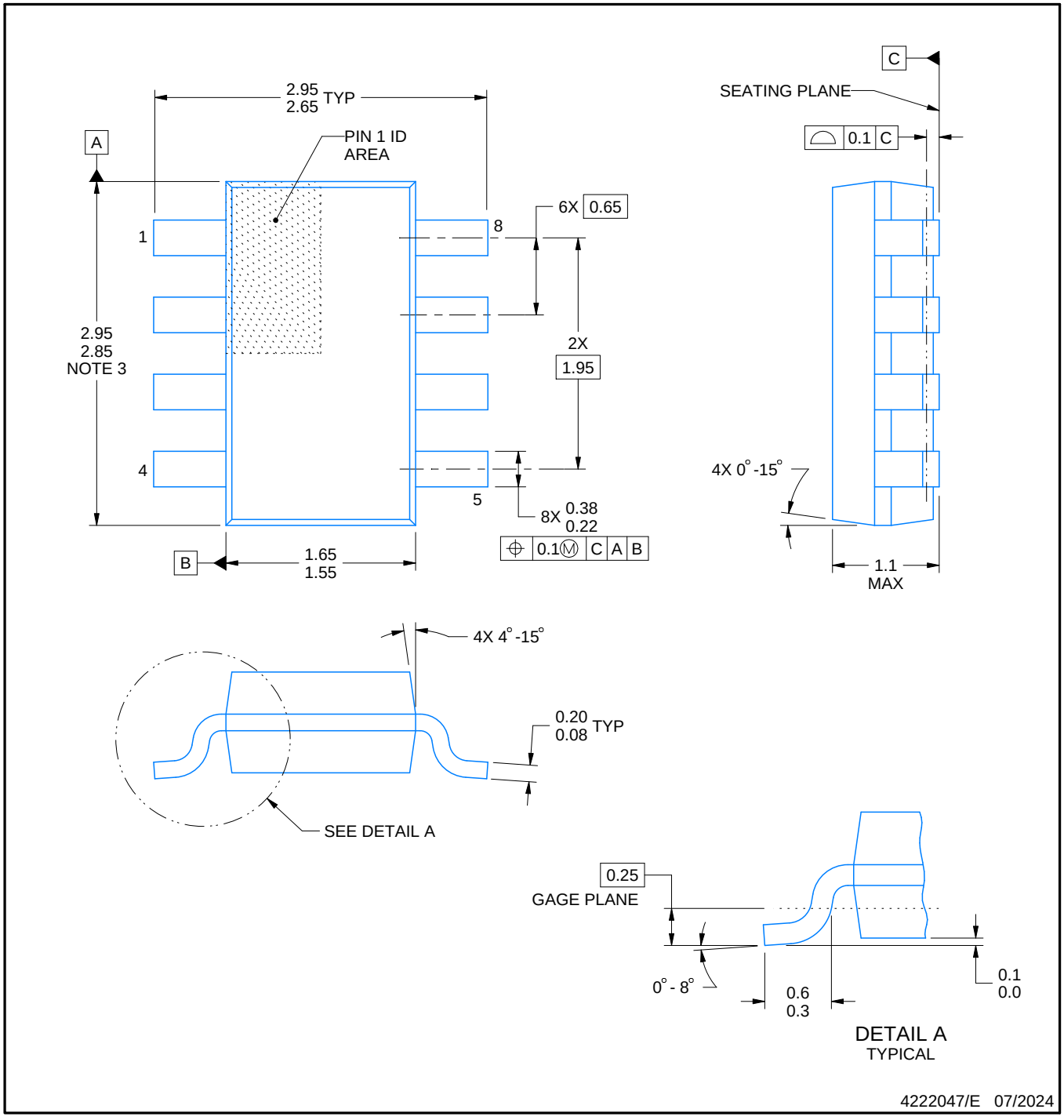
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74703QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM74704QDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

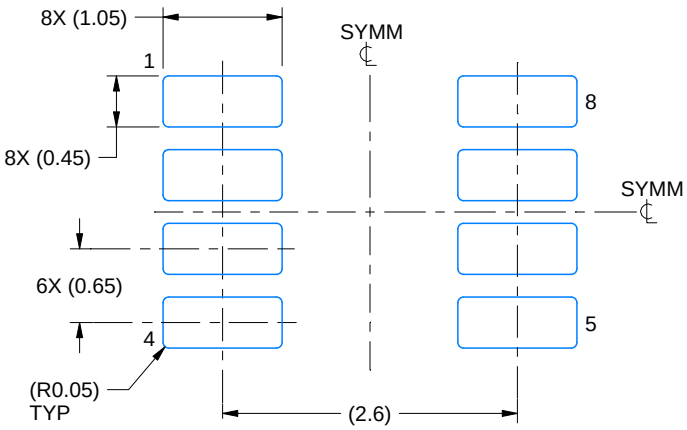
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

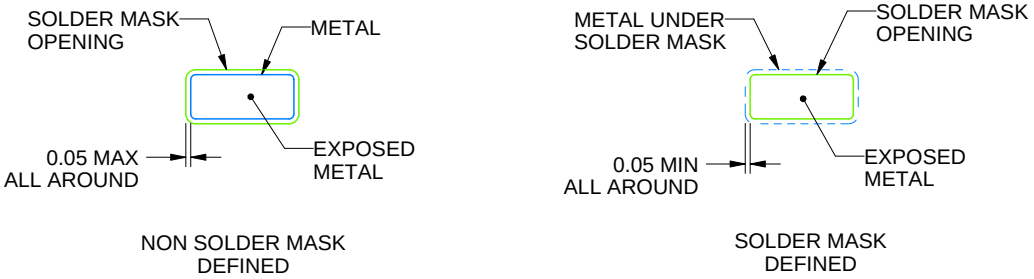


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

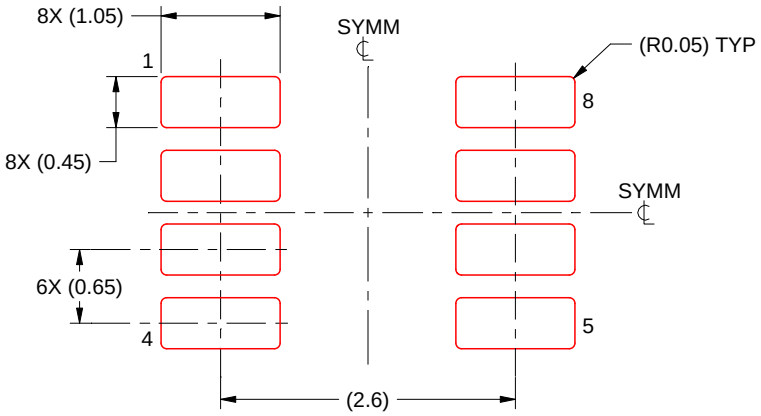
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265