LMG3100R017 100V、 126A、 ドライバ内蔵 GaN FET

1 特長

- 1.7mΩ の GaN FET とドライバを内蔵
- 電圧定格:連続 100V、パルス 120V
- ハイサイドのレベル シフトとブートストラップを内蔵
- 2 つの LMG3100 でハーフ ブリッジを形成
  - 外付けのレベル シフタが不要
- 5V の外部バイアス電源
- 3.3V および 5V の入力ロジック レベルをサポート
- 低リンギングで、高スルーレートのスイッチング
- ゲートドライバは最高 10MHz のスイッチングが可能
- 内部的なブートストラップ電源電圧クランピングにより、GaN FET オーバードライブを防止
- 電源レールの低電圧誤動作防止保護
- 低消費電力
- 簡単に PCB をレイアウトするよう最適化されたパッケージ
- 上面冷却用の露出上面 QFN パッケージ
- 底面に底面冷却用の大型露出パッド

2 アプリケーション

- 降圧、昇圧、昇降圧コンバータ
- LLC コンバータ
- 太陽光インバータ
- テレコムとサーバー電源
- モータ駆動
- 電動工具
- Class-D オーディオ アンプ

3 概要

LMG3100 デバイスは、100V 連続、120V パルス、126A、ドライバを内蔵した、窒化ガリウム (GaN) FET です。このデバイスは、高周波 GaN FET ドライバによって駆動される 100V の GaN FET で構成されています。LMG3100 には、ハイサイドのレベル シフタとブートストラップ回路が組み込まれているので、追加のレベル シフタなしで、2 つの LMG3100 デバイスを使用してハーフ ブリッジを形成できます。

GaN FET は逆方向回復時間がゼロで、入力容量 C_{ISS} および出力容量 C_{OSS} が非常に小さいため、電力変換において大きな利点があります。ドライバおよび GaN FET は、ボンド ワイヤを一切使用しないパッケージ プラットフォームに取り付けられ、パッケージの寄生要素は最小限に抑えられます。LMG3100 デバイスは、6.5mm × 4mm × 0.89mm の鉛フリー パッケージで供給され、簡単に PCB へ取り付けできます。

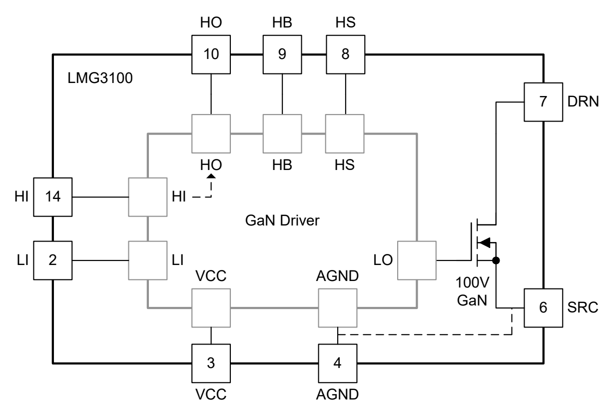
TTL ロジック互換の入力は、VCC 電圧にかかわらず 3.3V および 5V のロジック レベルをサポートできます。独自のブートストラップ電圧クランピング技法により、エンハンスメント モード GaN FET のゲート電圧が安全な動作範囲内であることが保証されます。

このデバイスは、ディスクリート GaN FET に対してより使いやすいインターフェイスを提供し、その利点を拡大します。小さなフォーム ファクタで高周波数、高効率の動作が必要なアプリケーションに理想的なソリューションです。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
LMG3100R017	VBE (VQFN、15)	6.50mm × 4.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図

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4 Pin Configuration and Functions

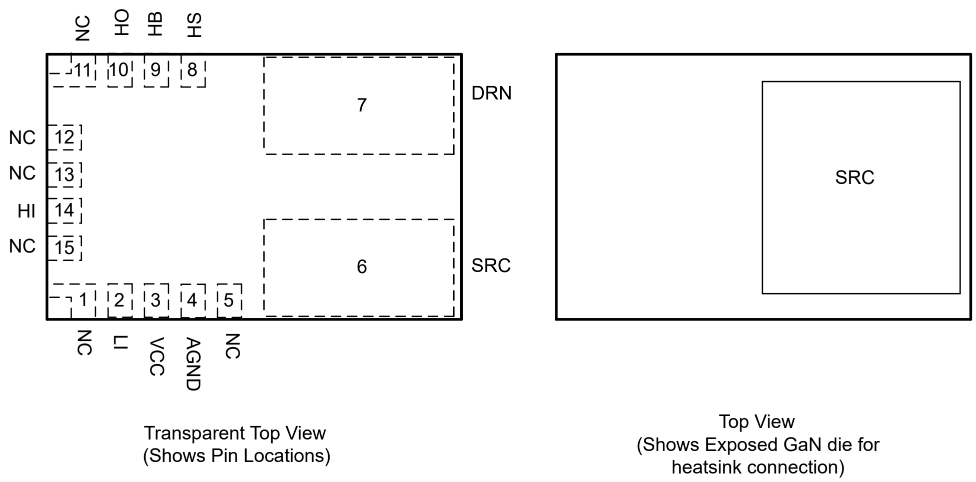


図 4-1. VBE Package, 15-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
NC	1, 5, 11–13, 15	—	Not connected internally. Leave floating.
LI	2	I	Low-side gate driver control input.
VCC	3	P	5V device power supply.
AGND	4	G	Analog ground.
SRC	6	P	Source of GaN FET. Internally connected to AGND.
DRN	7	P	Drain of GaN FET.
HS	8	P	Bootstrap voltage ground reference.
HB	9	P	High-side gate driver bootstrap rail with HS as the ground reference.
HO	10	O	Level shifted high-side gate driver control output.
HI	14	I	High-side gate driver control input.

(1) I = Input, O = Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

See(1)

	MIN	MAX	UNIT
DRN to SRC		100	V
DRN to SRC (up to 10,000 5ms pulses at 150°C)		120	V
HB to AGND	-0.3	100	V
HS to AGND		93	V
HI to AGND	-0.3	6	V
LI to AGND	-0.3	6	V
VCC to AGND	-0.3	6	V
HB to HS	-0.3	6	V
HB to VCC	0	93	V
IOUT from DRN pin (Continuous), T_J = 125℃, LMG3100R017		126	A
IOUT from DRN pin (Pulsed, 300 µs), T_J = 25℃, LMG3100R017		350	A
Junction Temperature, T_J	-40	150	°C
Storage Temperature, T_{stg}	-40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted, voltages are with respect to AGND

	MIN	NOM	MAX	UNIT
VCC	4.75	5	5.25	V
LI or HI Input	0		5.5	V
HB	V_{HS}+ 4		V_{HS}+ 5.25	V
HS, SW Slew rate(1)			50	V/ns

(1) Determined through design and characterization. Not tested in production.

5.4 Thermal Information

THERMAL METRIC [(1)]		LMG3100R017	UNIT
		QFN	
		15 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.39	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953 .

5.5 Electrical Characteristics

Unless otherwise noted, voltages are with respect to AGND; -40℃ ≤ T_J ≤125℃[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE R017						
$R_{DS(ON)}$	GaN FET on-resistance	LI=VCC=5V, HI=0V, I(DRN-SRC)=45A, T_J = 25℃		1.7	2.2	mΩ
V_{SD}	GaN 3rd quadrant conduction drop	I_{SD} = 500 mA, V_{VCC} = 5 V, HI = LI = 0V		1.5		V
$I_{L\text{-}DRN\text{-}SRC}$	Leakage from DRN to SRC when the GaN FET is off	DRN = 80V, HI = LI = 0V, V_{VCC} = 5V, T_J=25℃		12	200	µA
C_{OSS}	Output Capacitance of GaN FET	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V)		1035	1423	pF
$C_{OSS(ER)}$	Output Capacitance of GaN FET - Energy Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V)		1223		pF
$C_{OSS(TR)}$	Output Capacitance of GaN FET - Time Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V)		1547		pF
Q_G	Total Gate Charge of GaN FET	V_{DS}=50V, I_D= 45A, V_{GS}= 5V		20	29	nC
Q_{GD}	Gate to Drain Charge of GaN FET	V_{DS}=50V, I_D= 45A		2		nC
Q_{GS}	Gate to Source Charge of GaN FET	V_{DS}=50V, I_D= 45A		6.7		nC
Q_{OSS}	Output Charge	V_{DS}=50V, VGS = 0 V		77	104	nC
Q_{RR}	Source to Drain Reverse Recovery Charge	Not including internal driver bootstrap diode		0		nC
t_{HIPLH}	Propagation delay: HI Rising[(2)]	LI=0V, VCC=5V, HB-HS=5V, VIN=48V	38	70	120	ns
t_{HIPHL}	Propagation delay: HI Falling[(2)]	LI=0V, VCC=5V, HB-HS=5V, VIN=48V	38	70	120	ns
t_{LIPLH}	Propagation delay: LI Rising[(2)]	HI=0V, VCC=5V, HB-HS=5V, VIN=48V	19	40	65	ns
t_{LIPHL}	Propagation delay: LI Falling[(2)]	HI=0V, VCC=5V, HB-HS=5V, VIN=48V	19	40	65	ns
t_{MON}	Delay Matching: LI high & HI low[(2)]		4	30	55	ns
t_{MOFF}	Delay Matching: LI low & HI high[(2)]		4	30	55	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			10		ns
INPUT PINS HI, LI						
V_{IH}	High-Level Input Voltage Threshold	Rising Edge	1.87	2.06	2.22	V
V_{IL}	Low-Level Input Voltage Threshold	Falling Edge	1.48	1.66	1.76	V
V_{HYS}	Hysteresis between rising and falling threshold			350		mV
R_I	Input pull down resistance		100	200	300	kΩ
OUTPUT PIN HO						
V_{OL}	Low level output voltage	I_{OL} = 10 mA			0.03	V
V_{OH}	High level output voltage	I_{OL} = -10 mA	V_{HB}-0.06			V
UNDER VOLTAGE PROTECTION						
V_{CCR}	V_{CC} Rising edge threshold	Rising	3.2	3.8	4.5	V
V_{CCF}	V_{CC} Falling edge threshold		3.0	3.6	4.3	V

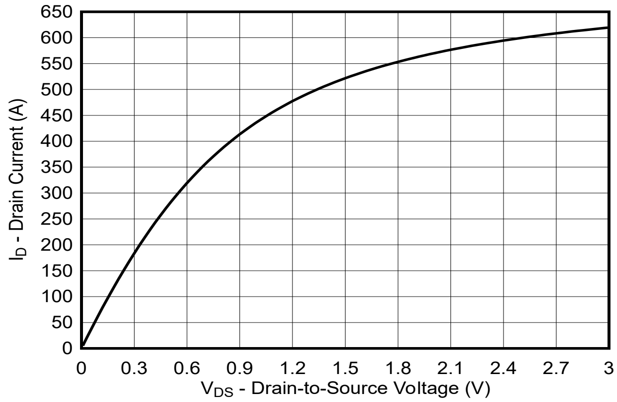
5.5 Electrical Characteristics (続き)

Unless otherwise noted, voltages are with respect to AGND; -40℃ ≤ T_J ≤125℃[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(hyst)}$	V_{CC} UVLO threshold hysteresis			210		mV
V_{HBR}	HB Rising edge threshold	Rising	2.5	3.2	3.9	V
V_{HBF}	HB Falling edge threshold		2.3	3.0	3.7	V
$V_{HB(hyst)}$	HB UVLO threshold hysteresis			220		mV
BOOTSTRAP DIODE						
V_{DL}	Low-Current forward voltage	I_{VDD-HB} = 100µA		0.45	0.65	V
V_{DH}	High current forward voltage	I_{VDD-HB} = 100mA		0.9	1.2	V
R_D	Dynamic Resistance	I_{VDD-HB} = 100mA		1.85		Ω
	HB-HS Clamp	Regulation Voltage	4.65	5	5.2	V
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, IR = 100 mA		40		ns
Q_{RR}	Bootstrap diode reverse recovery charge	V_{VIN} = 50 V		2		nC
SUPPLY CURRENTS						
I_{CC}	VCC Quiescent Current	LI = HI = 0V, VCC = 5V		0.08	0.125	mA
I_{CC}	VCC Quiescent Current	LI=VCC=5V, HI=0V, LMG3100R017		0.17	5	mA
I_{CCO}	Total VCC Operating Current	f = 500 kHz, 50% Duty cycle, V_{IN} = 48V, LMG3100R017		10	20	mA
I_{HB}	HB Quiescent Current	LI = HI = 0V, VCC = 5V, HB-HS = 4.6V		0.1	0.150	mA
I_{HB}	HB Quiescent Current	LI=0V, HI=VCC=5V, HB-HS=4.6V, VIN=48V, LMG3100R017		0.16	0.25	mA
I_{HBO}	HB Operating Current	f = 500 kHz, 50% Duty cycle, V_{DD} = 5V, V_{IN} = 48V, for low side device in half-bridge configuration, LMG3100R017, HB-HS = 4.6V (supplied externally)		1.5	2.5	mA

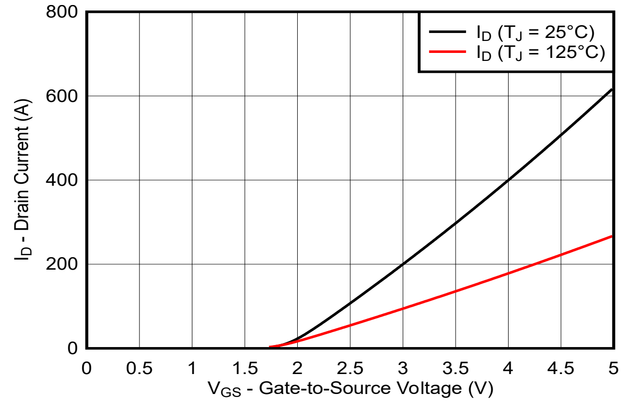
(1) Parameters that show only a typical value are determined by design and may not be tested in production
(2) See *Propagation Delay and Mismatch Measurement* section

5.6 Typical Characteristics



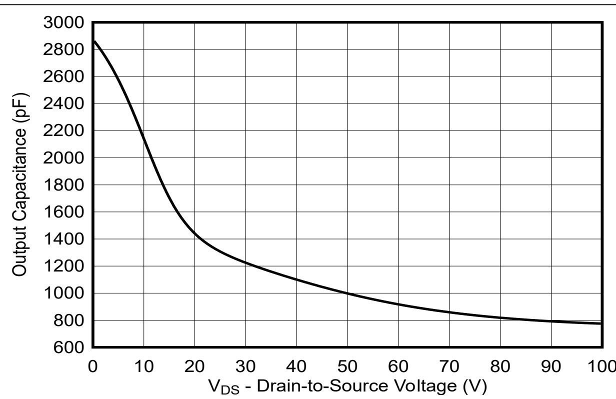
V_{GS} = 5V

図 5-1. Typical Output Characteristics



V_{DS} = 3V

図 5-2. Typical Transfer Characteristics



$C_{OSS} = C_{GS} + C_{GD}$

図 5-3. Typical Capacitance (Linear Scale)

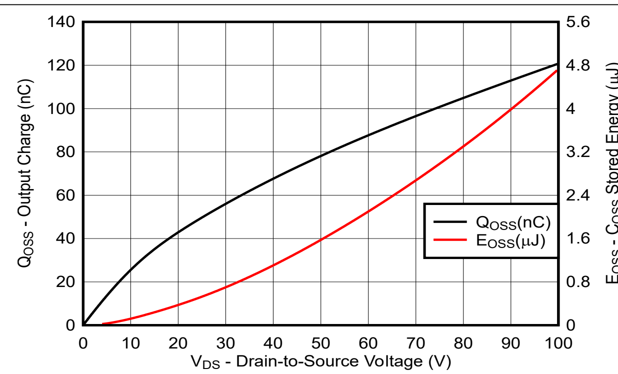
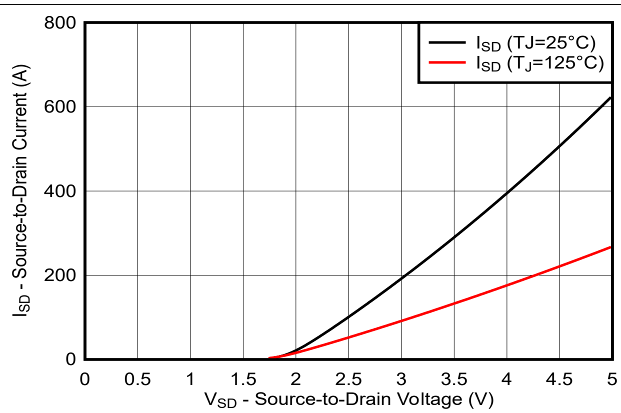
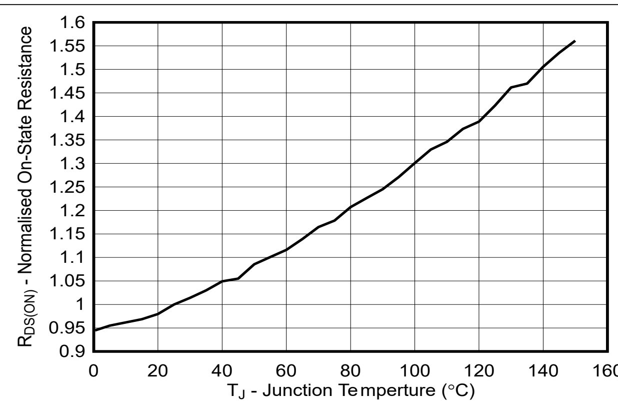


図 5-4. Typical Output Charge and C_{OSS} Stored Energy



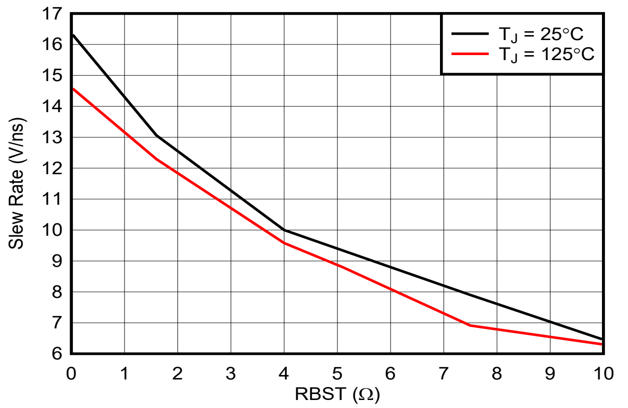
V_{GS} = 0V

図 5-5. Reverse Drain-Source Characteristics



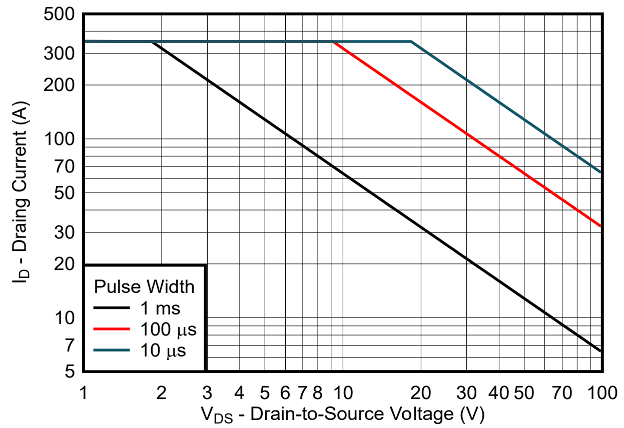
I_D = 10A V_{GS} = 5V

図 5-6. Normalized On-State Resistance vs Junction Temperature



V_{IN} = 48V V_{OUT} = 24V I_{OUT} = 20A

図 5-7. Slew Rate Control for a Buck Converter Using R_{BST}



T_J = Max rated T_C = 25°C Single pulse

図 5-8. Safe Operating Area

6 Parameter Measurement Information

6.1 Propagation Delay and Mismatch Measurement

図 6-1 shows the typical test setup used to measure the propagation mismatch. As the gate drives are not accessible, pullup and pulldown resistors in this test circuit are used to indicate when the low-side GaN FET turns ON and the high-side GaN FET turns OFF and vice versa to measure the t_{MON} and t_{MOFF} parameters. Resistance values used in this circuit for the pullup and pulldown resistors are in the order of 1kΩ; the current sources used are 2A.

図 6-2 through 図 6-5 show propagation delay measurement waveforms. For turnon propagation delay measurements, the current sources are not used. For turnoff time measurements, the current sources are set to 2A, and a voltage clamp limit is also set, referred to as $VIN_{(CLAMP)}$. When measuring the high-side component turnoff delay, the current source across the high-side FET is turned on, the current source across the low-side FET is off, HI transitions from high-to-low, and output voltage transitions from V_{IN} to $V_{IN(CLAMP)}$. Similarly, for low-side component turnoff propagation delay measurements, the high-side component current source is turned off, and the low-side component current source is turned on, LI transitions from high to low and the output transitions from GND potential to $V_{IN(CLAMP)}$. The time between the transition of LI and the output change is the propagation delay time.

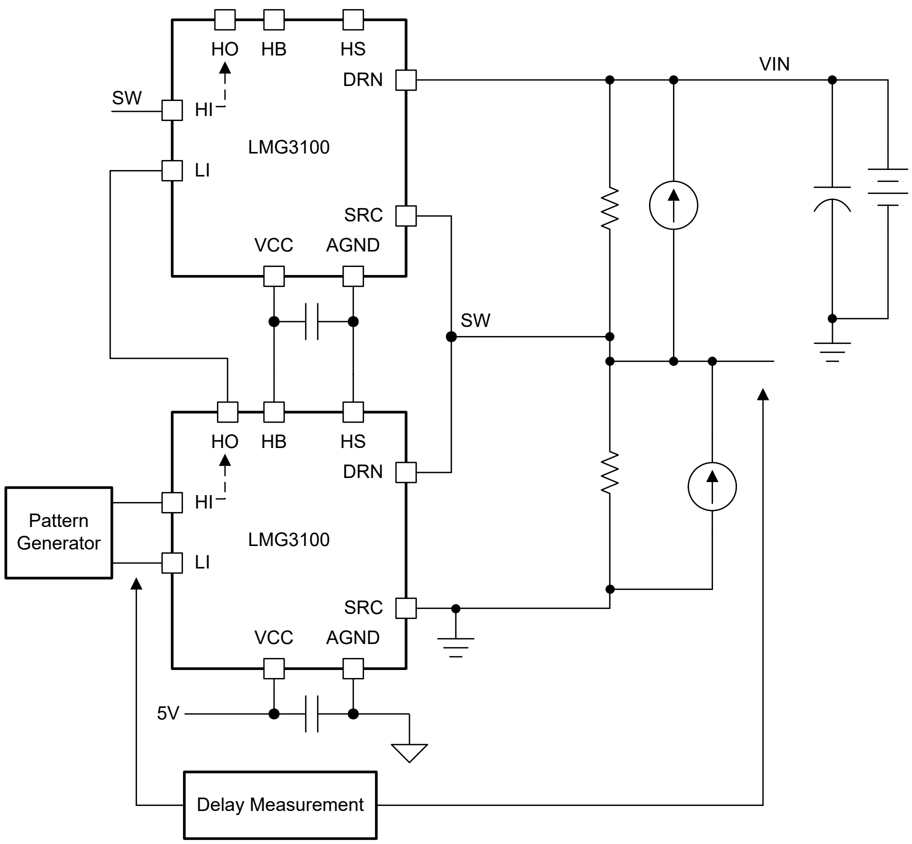


図 6-1. Propagation Delay and Propagation Mismatch Measurement

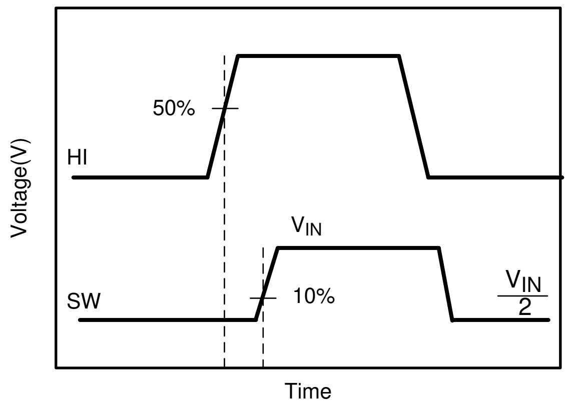


図 6-2. High-Side Gate Driver Turnon

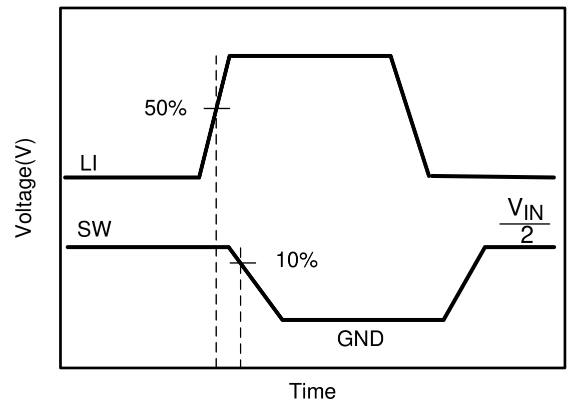


図 6-3. Low-Side Gate Driver Turnon

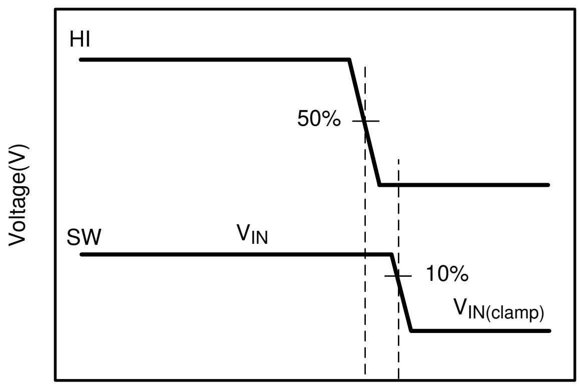


図 6-4. High-Side Gate Driver Turnoff

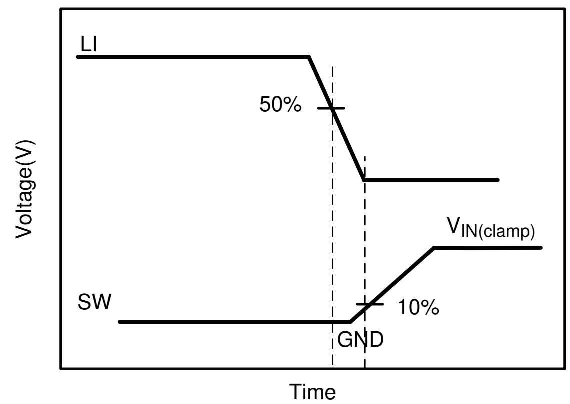


図 6-5. Low-Side Gate Driver Turnoff

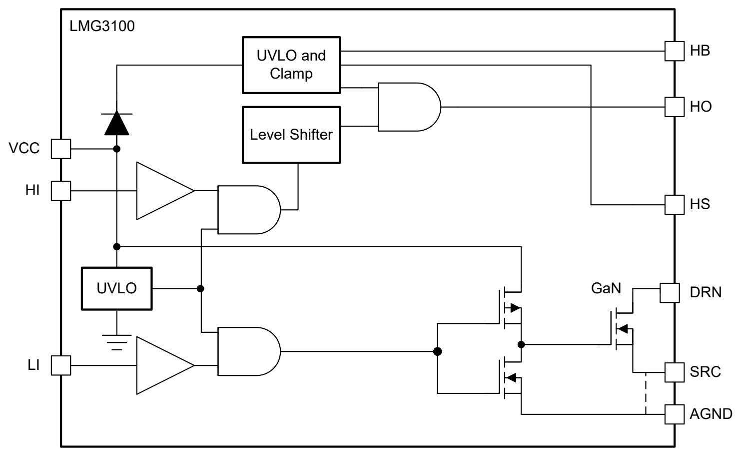
7 Detailed Description

7.1 Overview

セクション 7.2 shows the LMG3100 GaN FET with gate driver, high-side level shift and bootstrap circuit, which includes built-in UVLO protection circuitry and an overvoltage clamp circuitry. The clamp circuitry limits the bootstrap refresh operation to ensure that the high-side gate driver overdrive does not exceed 5.4V. The device integrates a 1.7mΩ GaN FET, with the possibility of using two LMG3100 to form a half-bridge without external level shifter. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The drive strengths for turnon and turnoff are optimized to ensure high voltage slew rates without causing any excessive ringing on the gate or power loop.

7.2 Functional Block Diagram

The functional block diagram of the LMG3100 device with integrated GaN FET and driver, high-side level shift, and bootstrap circuit.



7.3 Feature Description

The LMG3100 device brings ease of designing high power density boards without the need for underfill while maintaining creepage and clearance requirements. The propagation delays between the high-side gate driver and low-side gate driver are matched to allow very tight control of dead time. Controlling the dead time is critical in GaN-based applications to maintain high efficiency. HI and LI can be independently controlled to minimize the third quadrant conduction of the low-side FET for hard switched buck converters. A very small propagation mismatch between the HI and LI to the drivers for both the falling and rising thresholds ensures dead times of < 20 ns. Co-packaging the GaN FET half-bridge with the driver ensures minimized common source inductance. This minimized inductance has a significant performance impact on hard-switched topologies.

The built-in bootstrap circuit with clamp prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage (Vgs) without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the VDD and bootstrap (HB-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on. Below UVLO, if there is sufficient voltage (V_{VCC} > 2.5 V), the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis of 200 mV prevents chattering and unwanted turnon due to voltage spikes. Use an external VCC bypass capacitor with a value of 1 µF or higher. TI recommends a size of 0402 to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close as possible to the device to minimize parasitic inductance.

7.3.1 Control Inputs

The LMG3100's inputs pins are independently controlled with TTL input thresholds and can can support 3.3-V and 5-V logic levels regardless of the VCC voltage.

In order to allow flexibility to optimize deadtime according to design needs, the LMG3100 does not implement an overlap protection functionality. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned on. Careful consideration must be applied to the control inputs in order to avoid a shoot-through condition.

7.3.2 Start-up and UVLO

The LMG3100 has an UVLO on both the V_{CC} and HB (bootstrap) supplies. When the V_{CC} voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient V_{CC} voltage, the UVLO actively pulls the high- and low-side GaN FET gates low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only the high-side GaN FET gate is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

表 7-1. V_{CC} UVLO Feature Logic Operation

CONDITION (V_{HB-HS} > V_{HBR} for all cases below)	HI	LI	SW
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} during device start-up	L	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	L	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	H	H	Hi-Z
V_{CC} - V_{SS} < V_{CCR} - $V_{CC(hyst)}$ after device start-up	L	L	Hi-Z

表 7-2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION (V_{CC} > V_{CCR} for all cases below)	HI	LI	SW
V_{HB-HS} < V_{HBR} during device start-up	H	L	Hi-Z
V_{HB-HS} < V_{HBR} during device start-up	L	H	PGND
V_{HB-HS} < V_{HBR} during device start-up	H	H	PGND
V_{HB-HS} < V_{HBR} during device start-up	L	L	Hi-Z

表 7-2. V_{HB-HS} UVLO Feature Logic Operation (続き)

CONDITION ($V_{CC} > V_{CCR}$ for all cases below)	HI	LI	SW
$V_{HB-HS} < V_{HBR} - V_{HB(hyst)}$ after device start-up	H	L	Hi-Z
$V_{HB-HS} < V_{HBR} - V_{HB(hyst)}$ after device start-up	L	H	PGND
$V_{HB-HS} < V_{HBR} - V_{HB(hyst)}$ after device start-up	H	H	PGND
$V_{HB-HS} < V_{HBR} - V_{HB(hyst)}$ after device start-up	L	L	Hi-Z

7.3.3 Bootstrap Supply Voltage Clamping

The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5 V (typical). This clamp prevents the gate voltage from exceeding the maximum gate-source voltage rating of the enhancement-mode GaN FETs.

7.3.4 Level Shift

The level-shift circuit is the interface from the high-side input HI to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the high-side GaN FET gate driver output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.4 Device Functional Modes

The LMG3100 operates in normal mode and UVLO mode. See セクション 7.3.2 for information on UVLO operation mode. In the normal mode, the output state is dependent on the states of the HI and LI pins. 表 7-3 lists the output states for different input pin combinations. Note that when both HI and LI are asserted, both GaN FETs in the power stage are turned on. Careful consideration must be applied to the control inputs in order to avoid this state, as it will result in a shoot-through condition, which can permanently damage the device.

表 7-3. Truth Table

HI	LI	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	SW
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	PGND
H	L	ON	OFF	VIN
H	H	ON	ON	- - -

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMG3100 GaN power stage is a versatile building block for various types of high-frequency, switch-mode power applications. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the GaN FETs. The device design is highly optimized for synchronous buck converters and other half-bridge configurations.

8.2 Typical Application

図 8-1 shows a synchronous buck converter application using a digital PWM controller. The control signal for the high-side LMG3100 provided by the digital controller is level shifted through the low-side LMG3100, to complete the half-bridge without using an additional level shifter. It is critical to optimize the power loop (loop impedance from VIN capacitor to PGND). Having a high power loop inductance causes significant ringing in the SW node and also causes the associated power loss.

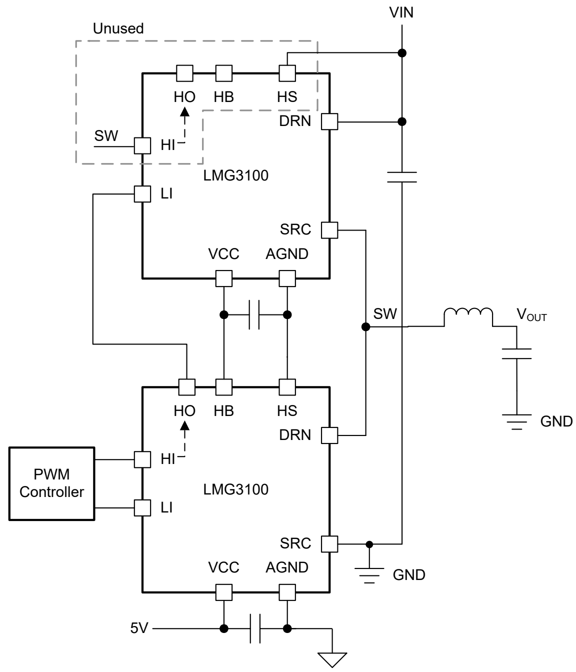


図 8-1. Typical Connection Diagram For a Synchronous Buck Converter

8.2.1 Design Requirements

When designing a synchronous buck converter application that incorporates the LMG3100 power stage, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are the input voltages, passive components, operating frequency, and controller selection. *表 8-1* shows some sample values for a typical application. See *セクション 8.3*, *セクション 8.4*, and *セクション 8.2.2.5* for other key design considerations for the LMG3100.

表 8-1. Design Parameters

PARAMETER	SAMPLE VALUE
Half-bridge input supply voltage, V_{IN}	48 V
Output voltage, V_{OUT}	12 V
Output current	8 A
V_{HB-HS} bootstrap capacitor	0.3 uF, X7R
Switching frequency	1 MHz
Dead time	8 ns
Inductor	4.7 µH
Controller	LM5148

8.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LMG3100 in a synchronous buck converter. For additional design help, see *セクション 9.1.1*.

8.2.2.1 V_{CC} Bypass Capacitor

The V_{CC} bypass capacitor provides the gate charge for the low-side and high-side transistors and absorbs the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with 式 1.

$$C_{VCC} = (2 \times Q_G + Q_{RR}) / \Delta V \quad (1)$$

Q_G is the individual and equal gate charge of the high-side and low-side GaN FETs. Q_{RR} is the reverse recovery charge of the bootstrap diode. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 1-µF or larger value, good-quality, ceramic capacitor is recommended. Place the bypass capacitor as close as possible to the V_{CC} and AGND pins of the device to minimize the parasitic inductance.

8.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side gate drive, dc bias power for HB UVLO circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated using 式 2.

$$C_{BST} = (Q_G + Q_{RR} + I_{CC} * t_{ON(max)}) / \Delta V \quad (2)$$

where

- I_{CC} is the quiescent current of the high side device
- t_{ON}(maximum) is the maximum on-time period of the high-side gate driver
- Q_{RR} is the reverse recovery charge of the bootstrap diode
- Q_G is the gate charge of the high-side GaN FET
- ΔV is the permissible ripple in the bootstrap capacitor (< 100 mV, typical)

A 0.3-µF, 16-V, 0402 ceramic capacitor is suitable for most applications. Place the bootstrap capacitor as close as possible to the HB and HS pins.

8.2.2.3 Slew Rate Control

図 8-2 shows a switching application where the slew rate on the switch node may be controlled by using resistors R_{VCCL} and R_{VCCH}. R_{VCCL} may be used to slow down the turn-on of the Low Side GaN FET, and R_{VCCH} may be used to slow down the turn-on of the High Side GaN FET. Using these resistors allows the system engineer to optimize the tradeoff between higher efficiency (faster slew rates) and lower ringing (slower slew rates).

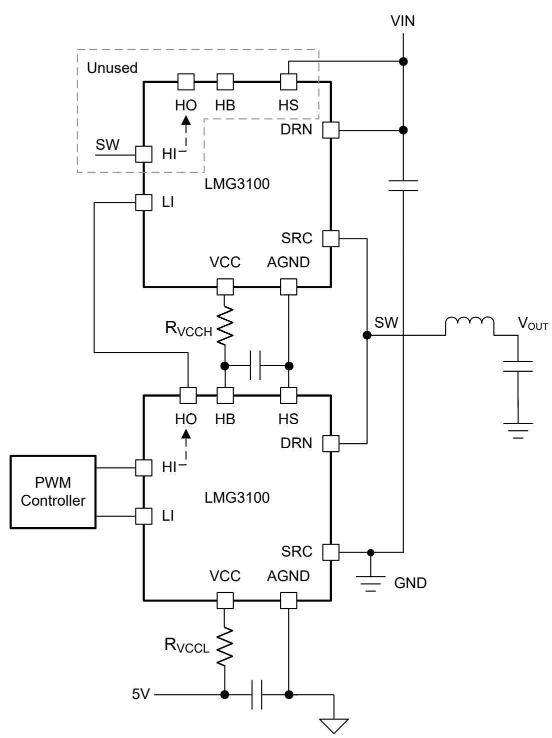


図 8-2. Slew Rate Control with R_{VCCL} and R_{VCCH} Resistors

8.2.2.4 Use With Analog Controllers

図 8-3 shows a synchronous buck converter application using an analog controller that provides level-shifted high-side control with the switch node as reference. The analog controller also generates the bootstrap voltage. In this use case, the level-shifted high-side control output, HO, from the controller may be directly connected to the input pin, LI, of the high-side LMG3100. The in-built level shifter and boot-strap circuits of the low-side LMG3100 are left unused.

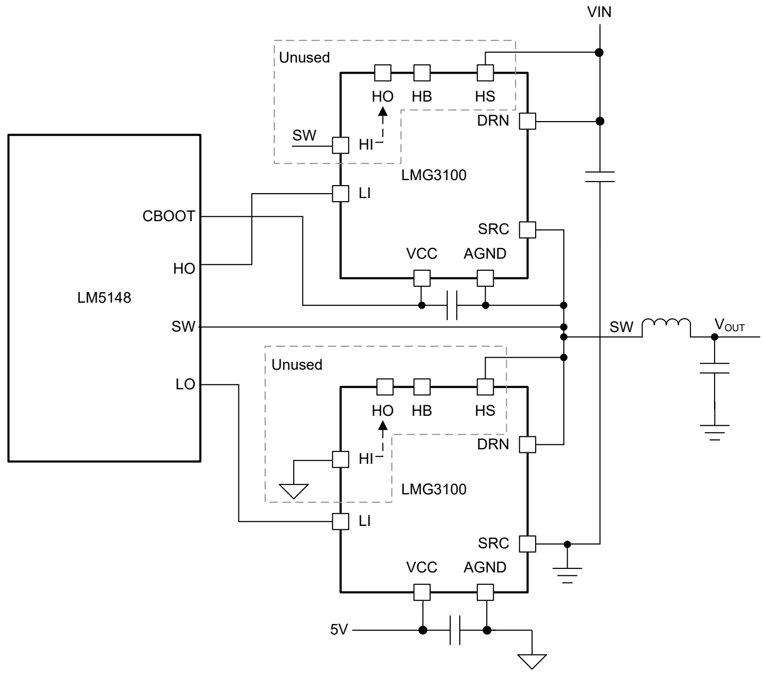


図 8-3. Use With Analog Controllers That Have In-built Level-shifting

8.2.2.5 Power Dissipation

Ensure that the power loss in the driver and the GaN FETs is maintained below the maximum power dissipation limit of the package at the operating temperature. The smaller the power loss in the driver and the GaN FETs, the higher the maximum operating frequency that can be achieved in the application. The total power dissipation of the LMG3100 device is the sum of the gate driver losses, the bootstrap diode power loss and the switching and conduction losses in the FETs.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated using 式 3.

$$P = 2 \times Q_G \times VCC \times f_{SW} \tag{3}$$

where

- Q_G is the gate charge
- VCC is the bias supply
- f_{SW} is the switching frequency

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the outputs.

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

The power losses due to the GaN FETs can be divided into conduction losses and switching losses. Conduction losses are resistive losses and can be calculated using 式 4.

$$P_{COND} = \left[(I_{RMS(HS)})^2 \times RDS_{(on)HS} \right] + \left[(I_{RMS(LS)})^2 \times RDS_{(on)LS} \right] \tag{4}$$

where

- $R_{DS(on)HS}$ is the high-side GaN FET on-resistance
- $R_{DS(on)LS}$ is the low-side GaN FET on-resistance
- $I_{RMS(HS)}$ is the high-side GaN FET RMS current
- $I_{RMS(LS)}$ and low-side GaN FET RMS current

The switching losses can be computed to a first order using , t_{TR} can be approximated by dividing V_{IN} by 25V/ns, which is a conservative estimate of the switched node slew rate. 式 5.

$$P_{SW} = V_{IN} \times I_{OUT} \times t_{TR} \times f_{SW} + V_{IN} \times V_{IN} \times C_{OSS(ER)} \times f_{SW} \tag{5}$$

where

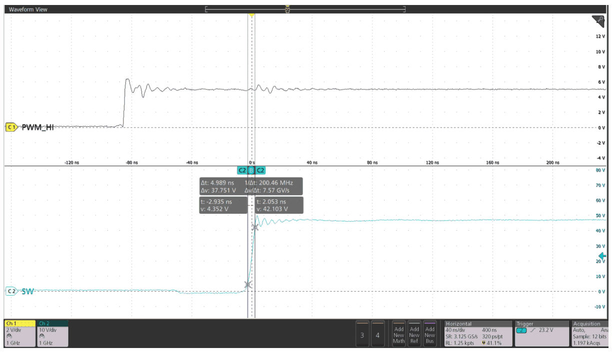
- t_{TR} is sum of the switch node transition times from ON to OFF and from OFF to ON
- $C_{OSS(ER)}$ is the output capacitance of each GaN FET

Note that the low-side FET does not suffer from this loss. The third quadrant loss in the low-side device is ignored in this first order loss calculation.

As described previously, switching frequency has a direct effect on device power dissipation. Although the gate driver of the LMG3100 device is capable of driving the GaN FETs at frequencies up to 10MHz, careful consideration must be applied to ensure that the running conditions for the device meet the recommended operating temperature specification. Specifically, hard-switched topologies tend to generate more losses and self-heating than soft-switched applications.

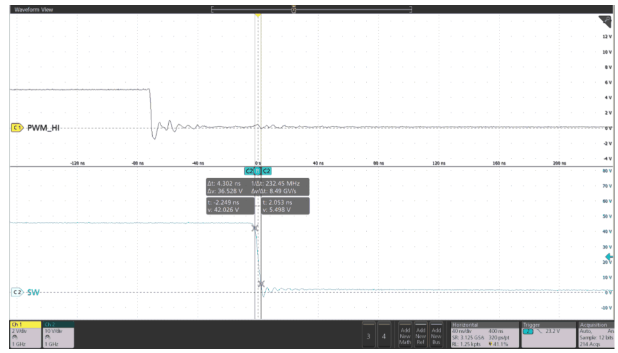
The sum of the driver loss, the bootstrap diode loss, and the switching and conduction losses in the GaN FETs is the total power loss of the device. Careful board layout with an adequate amount of thermal vias close to the power pads (VIN and PGND) allows optimum power dissipation from the package. A top-side mounted heat sink with airflow can also improve the package power dissipation.

8.2.3 Application Curves



I_{OUT} = 20 A V_{IN} = 48 V V_{OUT} = 24 V

図 8-4. SW Node Behavior Showing the Dead Time and Rise Time for R_{BST} = 3 Ω in a buck configuration



I_{OUT} = 20 A V_{IN} = 48 V V_{OUT} = 24 V

図 8-5. SW node Falling Behavior in a buck configuration

8.3 Power Supply Recommendations

The recommended bias supply voltage range for LMG3100 is from 4.75 V to 5.25 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the V_{CC} supply circuit. The upper end of this range is driven by the 6 V absolute maximum voltage rating of V_{CC}. Note that the gate voltage of the low-side GaN FET is not clamped internally. Hence, it is important to keep the V_{CC} bias supply within the recommended operating range to prevent exceeding the low-side GaN transistor gate breakdown voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{CC} voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, $V_{CC(hyst)}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LMG3100 to avoid triggering device-shutdown.

Place a local bypass capacitor between the VDD and VSS pins. This capacitor must be located as close as possible to the device. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

8.4 Layout

8.4.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, it is extremely important to optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VIN and PGND), small and directly underneath the first layer as shown in 図 8-6 and 図 8-7. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction.

Insufficient attention to the above power loop layout guidelines can result in excessive overshoot and undershoot on the switch node.

It is also critical that the VCC capacitors and the bootstrap capacitors are as close as possible to the device and in the first layer. Carefully consider the AGND connection of LMG3100 device. It must NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals.

8.4.2 Layout Examples

Placements shown in 図 8-6 and in the cross section of 図 8-7 show the suggested placement of the device with respect to sensitive passive components, such as VIN, bootstrap capacitors (HS and HB) and VSS capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

The layout must be designed to minimize the capacitance at the SW node. Use as small an area of copper as possible to connect the device SW pin to the inductor, or transformer, or other output load. Furthermore, ensure that the ground plane or any other copper plane has a cutout so that there is no overlap with the SW node, as this would effectively form a capacitor on the printed circuit board. Additional capacitance on this node reduces the advantages of the advanced packaging approach of the LMG3100 and may result in reduced performance.

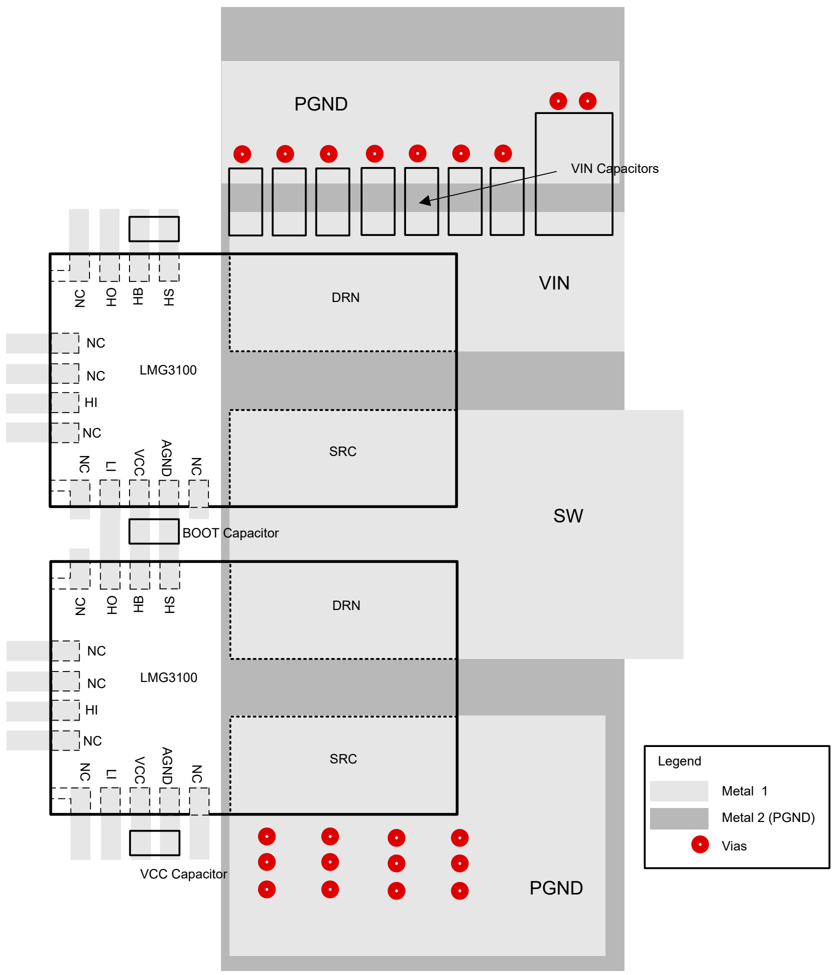


図 8-6. External Component Placement (Multi Layer Board)

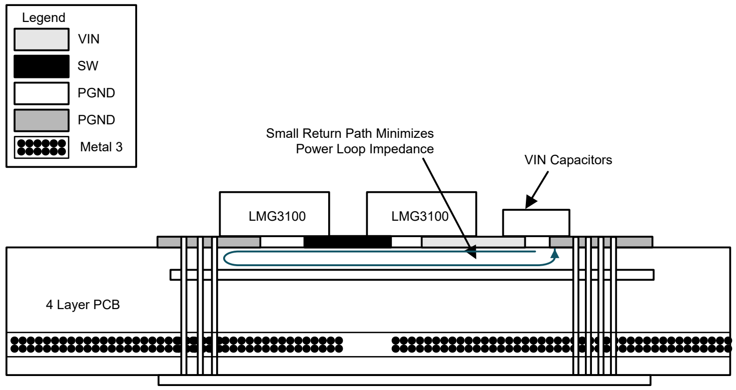


図 8-7. Four-Layer Board Cross Section With Return Path Directly Underneath for Power Loop

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Layout Guidelines for LMG3100 GaN Power Stage Module

Using the LMG3100: GaN Half-Bridge Power Module Evaluation Module

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2024) to Revision A (July 2024)	Page
• ドキュメントのステータスを「事前情報」から*「量産データ」に変更*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Information

The LMG3100 device package is rated as an MSL3 package (Moisture Sensitivity Level 3). Refer to application report *AN-2029 Handling and Process Recommendations* for specific handling and process recommendations of an MSL3 package.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XLMG3100R017VBER	ACTIVE	VQFN-FCRLF	VBE	15	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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