LMH12x9 リクロッカ内蔵 12G UHD 長距離ケーブル イコライザ

1 特長

- リクロッカ内蔵の適応型ケーブル イコライザ
- ST-2082-1 (12G)、ST-2081-1 (6G)、ST-424 (3G)、ST-292 (HD)、ST-259 (SD) をサポート
- DVB-ASI および AES10 (MADI) と互換
- リファレンスレス リクロッカを内蔵し、以下の SMPTE レートをロック可能:11.88Gbps、5.94Gbps、2.97Gbps、1.485Gbps、divide-by-1.001 サブレート、270Mbps
- 代表的なケーブルの到達範囲 (Belden 1694A)、PRBS-9 パターン:
  - 11.88Gbps (4Kp60 UHD) で 100m
  - 5.94Gbps (UHD) で 150m
  - 2.97Gbps (FHD) で 220m
  - 1.485Gbps (HD) で 300m
  - 270Mbps (SD) で 600m
- 代表的なケーブルの到達範囲 (Belden 1694A)、病理的パターン [1]
  - 11.88Gbps (4Kp60 UHD) で 90m
  - 5.94Gbps (UHD) で 140m
  - 2.97Gbps (FHD) で 220m
  - 1.485Gbps (HD) で 300m
  - 270Mbps (SD) で 600m
- オンチップの 75Ω 終端およびリターン損失補償ネットワーク
- 入力ケーブル イコライザおよびリクロッカの特長:
  - ストレス パターンによるケーブル到達距離の延長
  - プログラム可能な CDR ループ帯域幅設定
  - 2:1 75Ω 入力マルチプレクサ (LMH1239 のみ)
- 出力ドライバの特長:
  - ディエンファシス付き 1:2 100Ω ファンアウト出力
  - ケーブル障害検出を備えた、リクロック付き 75Ω ループスルー出力 (最大 600m)
- PRBS ジェネレータ、チェッカを内蔵
- アイ開口モニタを内蔵
- 2.5V 単一電源
- 低消費電力:350 mW (標準値)
- パワー セーブ モード:70 mW
- 制御ピン、SPI、SMBus インターフェイスにより構成可能
- 5mm × 5mm、32 ピン WQFN パッケージ
- 動作温度範囲:-40℃～+85℃

2 アプリケーション

- SMPTE 互換のシリアル デジタル インターフェイス
- UHDTV/4K/8K/HDTV/SDTV ビデオ
- 放送用ビデオ ルーター、スイッチャ、分配アンプ、モニタ
- デジタル ビデオ処理および編集

3 概要

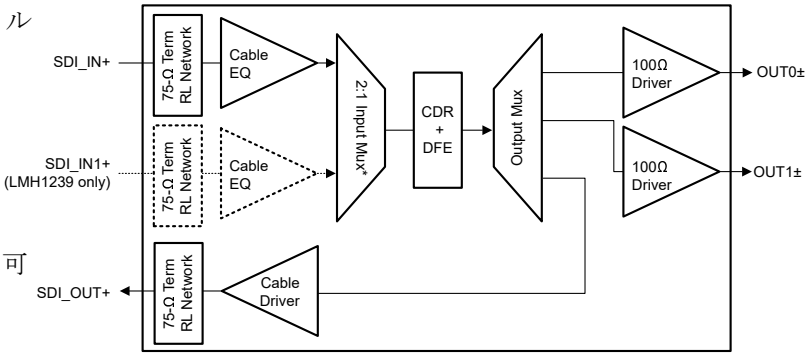
LMH12x9 (LMH1229、LMH1239) は、長距離対応の適応型ケーブル イコライザであり、リクロッカ、デュアル出力、75Ω ループ スルー出力を内蔵しています。このデバイスは、75Ω の同軸ケーブル経由で伝送するデータをイコライジング (平衡化) する設計を採用しており、125Mbps～11.88Gbps の SMPTE データ レートで動作します。

4K/8K ビデオ アプリケーションで 12G-SDI (11.88Gbps) を使用する場合、SDI 入力に実装した適応型イコライザは、最大 100m の Belden1694A のケーブル到達距離にわたって自動損失補償を行うことができます。オンチップのリクロッカは高周波ジッタを減衰させ、クリーンで低ジッタのクロックを使用して、データを全面的に再生成します。CDR ループ帯域幅を削減するため、オプションの外付けコンデンサを使用してリクロッカのループ フィルタを調整できます。

製品情報

部品番号	2:1、75Ω 入力マルチプレクサ内蔵の有無	パッケージ (1)	パッケージ サイズ (2)
LMH1229	なし	RTV (QFN、32)	5 mm × 5mm
LMH1239	あり		

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



*2:1 Input mux is only applicable with the LMH1239 variant. For LMH1229, SDI_IN+ data path is routed directly to the CDR.

概略ブロック図

[1] SDI 病理的実装の詳細については、『SDI 病理的データ パターンの研究』アプリケーション ノートを参照してください。

配線の簡素化とデバッグのため、VOD およびディエンファシス制御付きの 2 つの 100Ω ファンアウトと、1 つの 75Ω ループスルー SDI 出力で構成された 1:3 出力マルチプレクサを LMH12x9 は備えています。75Ω ループスルー出力は、信号の到達範囲を拡大し、またはシステム レベルの診断を可能にするために備わっています。

LMH12x9 は、すべてのデータ速度にわたる厳格な SMPTE 仕様を満たすリターン ロス ネットワークを内蔵しています。また、LMH12x9 は、システムの診断とボードの立ち上げをサポートするため、内部アイ開口モニタと、CDR ロック表示、入力搬送波検出、ケーブル障害検出、ハードウェア割り込み用のプログラム可能ピンも備えています。

ケーブル イコライザ アプリケーションで使用する場合、LMH1229 は LMH1297 (リクロッカ内蔵 12G UHD-SDI 双方向 I/O) とピン互換です。システム レベルの冗長性のため、LMH1239 は追加の SDI 入力マルチプレクサを 1 つ内蔵しています。

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4 Pin Configuration and Functions

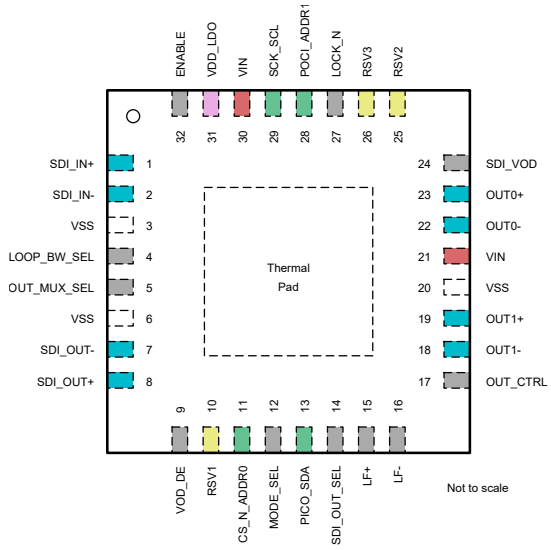


図 4-1. LMH1229 RTV Package, 32-Pin QFN (Top View)

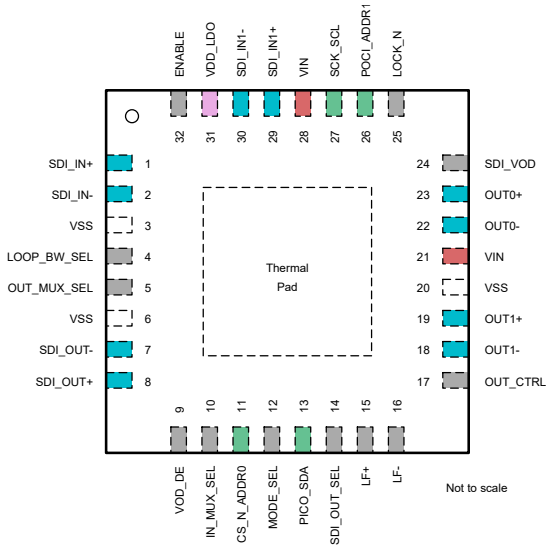


図 4-2. LMH1239 RTV Package, 32-Pin QFN (Top View)

Legend			
High Speed Signals	Serial Control Interface (SPI or SMBus) Pins		Reserved Pins
Control Pins	Power (2.5V)	LDO Output (1.8V)	GND

表 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	LMH1229 NO.	LMH1239 NO.		
HIGH SPEED DIFFERENTIAL I/Os				
SDI_IN+	1	1	I, Analog	Single-ended complementary inputs with on-chip 75Ω termination at SDI_IN+ and SDI_IN-. Either SDI_IN+ or SDI_IN- can be used as the 75Ω input port of the adaptive cable equalizer for SMPTE video applications. SDI_IN± include integrated return loss networks designed to meet the SMPTE input and output return loss requirements. Connect either SDI_IN+ or SDI_IN- to a BNC through a 4.7µF AC coupling capacitor. AC terminate the unused polarity (SDI_IN- or SDI_IN+, respectively) with external 4.7µF and 75Ω to GND.
SDI_IN-	2	2	I, Analog	
SDI_IN1+	N/A	29	I, Analog	Redundant single-ended complementary inputs with on-chip 75Ω termination at SDI_IN1+ and SDI_IN1-. Either SDI_IN1+ or SDI_IN1- can be used as a secondary 75Ω input port of the adaptive cable equalizer for SMPTE video applications. SDI_IN1± include integrated return loss networks designed to meet the SMPTE input and output return loss requirements. Connect either SDI_IN1+ or SDI_IN1- to a BNC through a 4.7µF AC coupling capacitor. AC terminate the unused polarity (SDI_IN- or SDI_IN+, respectively) with external 4.7µF and 75Ω to GND.
SDI_IN1-	N/A	30	I, Analog	
SDI_OUT+	8	8	O, Analog	Single-ended complementary loop-through cable driver outputs with on-chip 75Ω termination at SDI_OUT+ and SDI_OUT-. SDI_OUT± include integrated return loss networks designed to meet the SMPTE output return loss requirements. Connect either SDI_OUT+ or SDI_OUT- to a BNC through a 4.7µF AC coupling capacitor. AC terminate the unused polarity (SDI_IN- or SDI_IN+, respectively) with external 4.7µF and 75Ω to GND. Note that Cable Fault Detection is only available when using the SDI_OUT+ polarity.
SDI_OUT-	7	7	O, Analog	

表 4-1. Pin Functions (続き)

PIN			TYPE[1]	DESCRIPTION
NAME	LMH1229 NO.	LMH1239 NO.		
OUT0+	23	23	O, Analog	Differential complementary outputs with 100Ω internal termination. Requires external 4.7µF AC coupling capacitors. Output driver OUT0± can be disabled under user control.
OUT0-	22	22	O, Analog	
OUT1+	19	19	O, Analog	Differential complementary outputs with 100Ω internal termination. Requires external 4.7µF AC coupling capacitors. Output driver OUT1± can be disabled under user control.
OUT1-	18	18	O, Analog	
CONTROL PINS				
LOOP_BW_SEL	4	4	I, 4-Level	LOOP_BW_SEL enables 4-level CDR loop bandwidth control. Additional CDR loop bandwidth settings are available by register override.
IN_MUX_SEL	N/A	10	I, 4-Level	LMH1239 Only: IN_MUX_SEL selects between SDI_IN or SDI_IN1. This pin setting can be overridden by register control. See 表 6-2 for details.
OUT_MUX_SEL	5	5	I, 4-Level	OUT_MUX_SEL controls OUT0± and OUT1± enable behavior. This pin setting can be overridden using register control. See 表 6-3 for details.
VOD_DE	9	9	I, 4-Level	VOD_DE selects the driver output amplitude and de-emphasis level for both OUT0± and OUT1±. This pin setting can be overridden by register control. See 表 6-8 for details.
MODE_SEL	12	12	I, 4-Level	MODE_SEL enables SPI or SMBus serial control interface. See 表 6-9 for details.
SDI_OUT_SEL	14	14	I, LVCMOS	SDI_OUT_SEL enables the use of the 75Ω output driver at SDI_OUT±. SDI_OUT_SEL is internally pulled high. The SDI_OUT± is turned off by default. See 表 6-4 for details.
LF+	15	15	I, Analog	Optional 470nF external loop filter capacitor connected between LF+ and LF- for reduced CDR loop bandwidth settings. If reduced CDR loop bandwidth is not required, these pins can either be left floating (no connect) or, if connected, programmed with the desired CDR loop bandwidth settings by register control.
LF-	16	16	I, Analog	
OUT_CTRL	17	17	I, 4-Level	OUT_CTRL selects the signal flow from the SDI input (either SDI_IN± or SDI_IN1±) to OUT0± and OUT1±. The pin selects reclocked data, reclocked data and clock, or bypassed reclocker data (equalized data to output driver). Register control can override the pin settings. See 表 6-6 for details.
SDI_VOD	24	24	I, 4-Level	SDI_VOD selects one of four output amplitudes for the cable drivers at SDI_IO± and SDI_OUT±. See 表 6-7 for details.
LOCK_N	27	25	O, LVCMOS, OD	LOCK_N is the reclocker lock indicator for the selected input. LOCK_N is pulled LOW when the reclocker has acquired locking condition. LOCK_N is an open drain output, 3.3V tolerant, and requires an external 2kΩ to 5kΩ pullup resistor to logic supply. LOCK_N pin can be re-configured to indicate CD_N (Carrier Detect), Cable Fault Detect (CFD_N), or INT_N (Interrupt) for the selected SDI input through register programming.
ENABLE	32	32	I, LVCMOS	ENABLE controls device operation. A logic-low on ENABLE configures device in power down state. A logic-high on ENABLE configures the device in normal operation. ENABLE has an internal weak pull up.
SERIAL CONTROL INTERFACE				
CS_N_ADDR0	11	11	SPI Mode: I, LVCMOS SMBus Mode: Strap, 4-Level	**SPI Mode (MODE_SEL = F): CS_N** CS_N is the Chip Select. When CS_N is at logic Low, the pin enables SPI access to the LMH12x9 peripheral device. CS_N is a LVCMOS input pulled high by default. **SMBus Mode (MODE_SEL = L): ADDR0** ADDR[1:0] are SMBus address straps to select one of the 16 supported SMBus addresses. ADDR[1:0] are 4-level straps and are read into the device at power up. See 表 6-10 for details.

表 4-1. Pin Functions (続き)

PIN			TYPE(1)	DESCRIPTION
NAME	LMH1229 NO.	LMH1239 NO.		
POCI_ADDR1	28	26	SPI Mode: O, LVCMOS SMBus Mode: Strap, 4-Level	**SPI Mode (MODE_SEL = F): POCI** POCI "Peripheral Output Controller Input" is the SPI control serial data output from the LMH12x9 peripheral device. POCI is a LVCMOS output referenced to VIN. **SMBus Mode (MODE_SEL = L): ADDR1** ADDR[1:0] are SMBus address straps to select one of the 16 supported SMBus addresses. ADDR[1:0] are 4-level straps and are read into the device at power up. See 表 6-10 for details.
PICO_SDA	13	13	SPI Mode: I, LVCMOS SMBus Mode: IO, LVCMOS, OD	**SPI Mode (MODE_SEL = F): PICO** PICO "Peripheral Input Controller Output" is used as the SPI control serial data input to the LMH12x9 peripheral device. PICO is LVCMOS input referenced to VIN **SMBus Mode (MODE_SEL = L): SDA** SDA is the SMBus bi-directional open drain SDA data line to or from the LMH12x9 target device. SDA is an open drain IO and 3.3V tolerant. SDA requires an external 2kΩ to 5kΩ pullup resistor to the SMBus termination voltage.
SCK_SCL	29	27	SPI Mode: I, LVCMOS SMBus Mode: I, LVCMOS, OD	**SPI Mode (MODE_SEL = F): SCK** SCK is the SPI serial input clock to the LMH12x9 peripheral device. SCK is LVCMOS referenced to VIN. **SMBus Mode (MODE_SEL = L): SCL** SCL is the SMBus input clock to the LMH12x9 target device when SMBus is enabled. The pin is driven by a LVCMOS open drain driver from the SMBus controller and is 3.3V tolerant. SCL requires an external 2kΩ to 5kΩ pullup resistor to the SMBus termination voltage.
RESERVED				
RSV1	10	N/A	N/A	Reserved pins. Do not connect.
RSV2	25	N/A		
RSV3	26	N/A		
POWER				
VSS	3, 6, 20	3, 6, 20	I, Ground	Ground reference.
VIN	30, 21	28, 21	I, Power	Connect the VIN to the same external 2.5V ± 5% power supply. TI recommends to place decoupling capacitors as close as possible to both VIN pins.
VDD_LDO	31	31	O, Power	VDD_LDO is the output of the internal 1.8V LDO regulator. VDD_LDO output requires an external 1µF and 0.1µF bypass capacitor to VSS. The internal LDO is designed to power internal circuitry only.
EP			I, Ground	EP is the exposed pad at the bottom of the QFN package. The exposed pad must be connected to the ground plane through a 3x3 via array.

(1) I = Input, O = Output, IO = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
2.5V supply voltage (VIN)		–0.5	2.75	V
4-level input		–0.5	2.75	V
2-level LVCMOS input		–0.5	2.75	V
SMBus input/output	SDA, SCL	–0.5	4	V
High-speed inputs/output voltage	SDI_IN±, SDI_IN1±, SDI_OUT±, OUT0±, OUT1±	–0.5	2.75	V
High-speed input current	SDI_IN±, SDI_IN1±	–30	30	mA
Junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	All pins including high-speed pins(2)	±6000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(3)		±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) High speed I/O pins include: SDI_IN±, SDI_OUT±, OUT0±, and OUT1±.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	VIN		2.375	2.5	2.625	V
VDD_{SMBUS}	SDA, SCL		2.375		3.6	V
$V_{SDI\_INx\_LAUNCH}$	SDI_IN±, SDI_IN1±		720	800	880	mVpp
T_J	Operating junction temperature				110	°C
$T_{RampVCC}$	VCC supply ramp time	From 0V to 2.5V	0.150		100	ms
T_A	Ambient temperature		–40	25	85	°C
NT_{psmax}	Maximum supply noise tolerance(1)	50Hz to 1MHz, sinusoidal		<20		mVpp
		1.1MHz to 6GHz, sinusoidal		<10		mVpp

(1) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

5.4 Thermal Information

THERMAL METRIC(1)		RTV (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W

THERMAL METRIC(1)		RTV (QFN) 32 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD_{ACTIVE}	Power dissipation, measured with PRBS10, CDR locked to 11.88Gbps, VOD = default	SDI_OUT± disabled OUT0± enabled OUT1± disabled		350	466	mW
		SDI_OUT± disabled OUT0± enabled OUT1± enabled		380	517	mW
		SDI_OUT± enabled OUT0± enabled OUT1± disabled		480	640	mW
		SDI_OUT± enabled OUT0± enabled OUT1± enabled		520	688	mW
PD_Z	Power dissipation, power save mode	MODE_SEL = High		70	110	mW
PD_Z	Power dissipation, power save mode with no signal	No signal applied at SDI_IN+, MODE_SEL = F or MODE_SEL = Low		75	115	mW
IDD_{ACTIVE}	Current consumption, measured with PRBS10, CDR locked to 11.88Gbps, VOD = default	SDI_OUT± disabled OUT0± enabled OUT1± disabled		140	177	mA
		SDI_OUT± disabled OUT0± enabled OUT1± enabled		152	197	mA
		SDI_OUT± enabled OUT0± enabled OUT1± disabled		192	244	mA
		SDI_OUT± enabled OUT0± enabled OUT1± enabled		208	262	mA
IDD_Z	Current consumption, power save mode	No signal applied at SDI_IN+		28	42	mA
IDD_{TRANS}	Current consumption, CDR acquiring lock	SDI_OUT± disabled OUT0± enabled OUT1± disabled		210	268	mA
		SDI_OUT± disabled OUT0± enabled OUT1± enabled		230	287	mA
		SDI_OUT± enabled OUT0± enabled OUT1± disabled		270	333	mA
		SDI_OUT± enabled OUT0± enabled OUT1± enabled		280	353	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Logic high input voltage	2-Level input (CS_N, SCK, PICO, SDI_OUT_SEL, ENABLE)	0.72 × VIN		VIN + 0.3	V
		2-Level input (SCL, SDA)	0.7 × VIN		3.6	V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Logic Low input voltage	2-Level input (CS_N, SCK, PICO, SDI_OUT_SEL, ENABLE, SCL, SDA)	0		0.3 × VIN	V
V_{OH}	Logic high output voltage	I_{OH} = –2mA, (POCI)	0.8 × VIN		VIN	V
V_{OL}	Logic low output voltage	I_{OL} = 2mA, (POCI)	0		0.2 × VIN	V
		I_{OL} = 3mA, (LOCK_N, SDA)			0.4	V
I_{IH}	Input high leakage current (Vinput = VIN)	LVCMOS (SDI_OUT_SEL, ENABLE)			15	µA
		SPI mode: LVCMOS (CS_N, SCK, PICO)			15	µA
		SMBus mode: LVCMOS (SCL, SDA)			15	µA
I_{IL}	Input low leakage current (Vinput = GND)	LVCMOS (SDI_OUT_SEL, ENABLE)	–50			µA
		SPI mode: LVCMOS (SCK, PICO)	–15			µA
		SPI mode: LVCMOS (CS_N)	–50			µA
		SMBus mode: LVCMOS (SCL, SDA)	–10			µA
4-LEVEL LOGIC DC SPECIFICATIONS (APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
V_{LVL_H}	LEVEL-H input voltage	Measured voltage at 4-level pin with external 1kΩ to VIN		VIN		V
V_{LVL_F}	LEVEL-F default voltage	Measured voltage 4-level pin at default		2/3 × VIN		V
V_{LVL_R}	LEVEL-R input voltage	Measured voltage at 4-level pin with external 20kΩ to VSS		1/3 × VIN		V
V_{LVL_L}	LEVEL-L input voltage	Measured voltage at 4-level pin with external 1kΩ to VSS		0		V
I_{IH}	Input high leakage current (Vinput = VIN)	4-Levels (LOOP_BW_SEL, IN_MUX_SEL, OUT_MUX_SEL, VOD_DE, MODE_SEL, OUT_CTRL, SDI_VOD)	20	45	80	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	20	45	80	µA
I_{IL}	Input low leakage current (Vinput = GND)	4-Levels (LOOP_BW_SEL, IN_MUX_SEL, OUT_MUX_SEL, VOD_DE, MODE_SEL, OUT_CTRL, SDI_VOD)	–160	–90	–40	µA
		SMBus mode: 4-Levels (ADDR0, ADDR1)	–160	–90	–40	µA
SDI RECEIVER SPECIFICATIONS (SDI_IN+[4])						
$R_{SDI\_IN\_TERM}$	DC input single-ended termination	SDI_IN+ and SDI_IN– to internal common-mode bias	63	75	87	Ω
$RL_{SDI\_IN\_S11}$	Input Return Loss at SDI_IN+ reference to 75Ω[1]	S11, 5MHz to 1.485GHz		–30		dB
		S11, 1.485GHz to 3GHz		–25		dB
		S11, 3GHz to 6GHz		–16		dB
		S11, 6GHz to 12GHz		–13		dB
$V_{SDI\_IN\_CM}$	SDI_IN+ DC common-mode voltage	Input DC common-mode voltage at SDI_IN+ or SDI_IN– to GND		1.4		V
$V_{SDI\_IN\_WANDER}$	Input DC wander tolerance	SD, input signal at SDI_IN+, input launch amplitude = 800mVpp		150		mVpp
		HD, 3G, 6G, 12G, input signal at SDI_IN+, input launch amplitude = 800mVpp		50		mVpp

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Reach_{PRBS9}$	Input cable reach with B1694A, measured with LMH1239EVM, OUT1± and SDI_OUT+ disabled	Measured at OUT0±, PRBS9 (BER ≤ 1E-12), TX launch amplitude = 800mVpp before cable 11.88Gbps ± 1000ppm (12G-SDI)		100		m
		5.94Gbps ± 1000ppm (6G-SDI)		150		m
		2.97Gbps ± 1000ppm (3G)		220		m
		1.485Gbps ± 1000ppm (HD)		300		m
		270Mbps ± 1000ppm (SD)		600		m
	Input cable reach with B1694A, measured with LMH1239EVM, OUT1± and SDI_OUT+ enabled	Measured at OUT0±, PRBS9 (BER ≤ 1E-12), TX launch amplitude = 800mVpp before cable 11.88Gbps ± 1000ppm (12G-SDI)		90		m
		5.94Gbps ± 1000ppm (6G-SDI)		140		m
		2.97Gbps ± 1000ppm (3G)		220		m
		1.485Gbps ± 1000ppm (HD)		300		m
		270Mbps ± 1000ppm (SD)		600		m
$Reach_{PATH}$	Input cable reach with B1694A, measured with LMH1239EVM, OUT1± and SDI_OUT+ disabled	Measured at OUT0±, Pathological Pattern (BER ≤ 1E-12), TX launch amplitude = 800mVpp before cable 11.88Gbps (12G-SDI) Test with SDI_IN1+		90		m
		5.94Gbps (6G-SDI)		140		m
		2.97Gbps (3G)		220		m
		1.485Gbps (HD)		300		m
		270Mbps (SD)		600		m
	Input cable reach with B1694A, measured with LMH1239EVM, OUT1± and SDI_OUT+ enabled	Measured at OUT0±, Pathological Pattern (BER ≤ 1E-12), TX launch amplitude = 800mVpp before cable 11.88Gbps (12G-SDI) Test with SDI_IN+		80		m
		5.94Gbps (6G-SDI)		140		m
		2.97Gbps (3G)		220		m
		1.485Gbps (HD)		300		m
		270Mbps (SD)		600		m
RECLOCKER CLOCK AND DATA RECOVERY SPECIFICATIONS						
$LOCK_{RATE}$	Reclocker lock data rates	SMPTE 12G, /1		11.88		Gbps
		SMPTE 12G, /1.001		11.868		Gbps
		SMPTE 6G, /1		5.94		Gbps
		SMPTE 6G, /1.001		5.934		Gbps
		SMPTE 3G, /1		2.97		Gbps
		SMPTE 3G, /1.001		2.967		Gbps
		SMPTE HD, /1		1.485		Gbps
		SMPTE HD, /1.001		1.4835		Gbps
		SMPTE SD, /1		270		Mbps
$BYPASS_{RATE}$	Reclocker automatically goes to bypass(6)	MADI		125		Mbps

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW_{PLL}	PLL bandwidth, LOOP_BW_SEL=F (default)	Applied 0.2UI input sinusoidal jitter, measure –3dB bandwidth on input-to-output jitter transfer 11.88Gbps		7		MHz
		5.94Gbps		7		MHz
		2.97Gbps		5		MHz
		1.485Gbps		3		MHz
		270Mbps		0.8		MHz
	PLL bandwidth, LOOP_BW_SEL=H(5)	Applied 0.2UI input sinusoidal jitter, measure –3dB bandwidth on input-to-output jitter transfer 11.88Gbps		7		MHz
		5.94Gbps		7		MHz
		2.97Gbps		5		MHz
		1.485Gbps		3		MHz
		270Mbps		0.8		MHz
	PLL bandwidth, LOOP_BW_SEL=R(5)	Applied 0.2UI input sinusoidal jitter, measure –3dB bandwidth on input-to-output jitter transfer 11.88Gbps		0.70		MHz
		5.94Gbps		0.60		MHz
		2.97Gbps		0.46		MHz
		1.485Gbps		0.24		MHz
		270Mbps		0.05		MHz
	PLL bandwidth, LOOP_BW_SEL=L(5)	Applied 0.2UI input sinusoidal jitter, measure –3dB bandwidth on input-to-output jitter transfer 11.88Gbps		0.35		MHz
		5.94Gbps		0.30		MHz
		2.97Gbps		0.23		MHz
		1.485Gbps		0.12		MHz
		270Mbps		0.03		MHz
J_{PEAK}	PLL jitter peaking	12G/6G/3G/HD/SD		<0.3		dB
J_{TOL_SDI}	SDI_IN+ input jitter tolerance	Sinusoidal jitter, tested at 12G/6G/3G SJ amplitude swept from 1MHz to 80MHz, tested at BER ≤ 1E-12, cable equalizer at SDI_IN+ bypassed		0.55		UI
T_{LOCK}	CDR Lock Time	SMPTE supported data rates, includes EQ coarse adaptation. Does not include SSLMS adaptation. No external LF capacitor applied.		1.2	4.5	ms
T_{ADAPT}	EQ adapt time	SMPTE supported data rates, includes CDR lock time. No external LF capacitor applied.		1.6		ms
$TEMP_{LOCK}$	VCO temperature lock range	Measured with temperature ramp of 5°C per min, ramp up and down, –40°C to 85°C operating range at 11.88Gbps		125		°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{LATENCY}$	Input-to-output latency (propagation delay)	Measured from SDI_IN+ to OUT0, all supported data rates, CDR enabled and locked		2.1 UI + 270		ps
		Measured from SDI_IN+ to SDI_OUT+, all supported data rates, CDR enabled and locked		2.1 UI + 255		ps
		Measured from SDI_IN+ to OUT0, all supported data rates, raw mode (CDR bypassed)		270		ps
		Measured from SDI_IN+ to SDI_OUT+, 12G/6G/3G/HD, raw mode (CDR bypassed), OUT_CTRL = L		255		ps
		Measured from SDI_IN+ to SDI_OUT+, SD, raw mode (CDR bypassed), OUT_CTRL = L		900		ps
RECLOCKER DIFFERENTIAL OUTPUT JITTER (OUT0±, OUT1±)						
TJ_{DIFF_OUT}	Total jitter (BER ≤ 1E-12), reclocked output with SDI_OUT disabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable 11.88Gbps: 100m Belden 1694A		0.12	0.20	UI
		5.94Gbps: 150m Belden 1694A		0.08		
		2.97Gbps: 220m Belden 1694A		0.07		
		1.485Gbps: 300m Belden 1694A		0.05		
		270Mbps: 600m Belden 1694A		0.11		
	Total jitter (BER ≤ 1E-12), reclocked output with SDI_OUT enabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable 11.88Gbps: 90m Belden 1694A		0.12	0.20	UI
		5.94Gbps: 140m Belden 1694A		0.08		
		2.97Gbps: 220m Belden 1694A		0.07		
		1.485Gbps: 300m Belden 1694A		0.05		
		270Mbps: 600m Belden 1694A		0.11		
DJ_{DIFF_OUT}	Deterministic jitter (BER ≤ 1E-12), reclocked output with SDI_OUT disabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable to SDI_IN+ 11.88Gbps: 100m Belden 1694A		35	80	mUI
		5.94Gbps: 150m Belden 1694A		26		
		2.97Gbps: 220m Belden 1694A		16		
		1.485Gbps: 300m Belden 1694A		20		
		270Mbps: 600m Belden 1694A		23		
	Deterministic jitter (BER ≤ 1E-12), reclocked output with SDI_OUT enabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable to SDI_IN+ 11.88Gbps: 90m Belden 1694A		35	80	mUI
		5.94Gbps: 140m Belden 1694A		26		
		2.97Gbps: 220m Belden 1694A		16		
		1.485Gbps: 300m Belden 1694A		20		
		270Mbps: 600m Belden 1694A		23		

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ_{DIFF_OUT}	Random jitter (BER ≤ 1E-12), reclocked output with SDI_OUT disabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable to SDI_IN+ 11.88Gbps: 100m Belden 1694A		6.2	11	mUIrms
		5.94Gbps: 150m Belden 1694A		5.3		
		2.97Gbps: 220m Belden 1694A		5.3		
		1.485Gbps: 300m Belden 1694A		4.5		
		270Mbps: 600m Belden 1694		7.8		
	Random jitter (BER ≤ 1E-12), reclocked output with SDI_OUT enabled(1) (3)	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable to SDI_IN+ 11.88Gbps: 90m Belden 1694A		6.2	11	mUIrms
		5.94Gbps: 1540m Belden 1694A		5.3		
		2.97Gbps: 220m Belden 1694A		5.3		
		1.485Gbps: 300m Belden 1694A		4.5		
		270Mbps: 600m Belden 1694A		7.8		
TJ_{RAW}	Total jitter (BER ≤1E-12) with CDR bypassed	Measured at OUT0±, PRBS9, TX launch amplitude = 800mVpp before cable to SDI_IN+ 125Mbps: 600m Belden 1694A		0.2		UI
RECLOCKER SDI OUTPUT JITTER (SDI_OUT+)						
AJ_{SDI_OUT}	Alignment jitter(1)	Measured with 12G-SDI at SDI_OUT+ OUT0± and OUT1± disabled		0.14		UI
TMJ_{SDI_OUT}	Timing jitter(1)	Measured with 12G-SDI at SDI_OUT+ OUT0± and OUT1± disabled		0.45		UI
DIFFERENTIAL DRIVER OUTPUT (OUT0±, OUT1±)						
$R_{DIFF\_OUT\_TERM}$	DC output differential termination	Measured across OUT0+ and OUT0-	80	100	120	Ω
VOD_{DIFF_OUT}	Output differential voltage	Measured with 8T pattern at 11.88Gbps VOD_DE = H		410		mVpp
		VOD_DE = F	485	560	635	mVpp
		VOD_DE = R		635		mVpp
		VOD_DE = L		810		mVpp
$VOD_{DIFF\_OUT\_DE}$	Output de-emphasis level	Measured with 8T pattern at 11.88Gbps VOD_DE = H		410		mVpp
		VOD_DE = F		500		mVpp
		VOD_DE = R		480		mVpp
		VOD_DE = L		400		mVpp
t_R/t_F	Output rise/fall time	Measured with 8T Pattern at 11.88Gbps, 20%-80% amplitude		45		ps
$RL_{DIFF\_OUT-SDD22}$	Output differential return loss(1)	Measured with the device powered up and outputs a 10MHz clock signal SDD22, 10MHz to 2.8GHz		–26		dB
		SDD22, 2.8GHz to 6GHz		–18		dB
		SDD22, 6GHz to 11.1GHz		–13		dB
$RL_{DIFF\_OUT-SCC22}$	Output common-mode return loss(1)	Measured with the device powered up and outputs a 10MHz clock signal. SCC22, 10MHz to 4.75GHz		–14		dB
		SCC22, 4.75GHz to 11.1GHz		–16		dB
$V_{DIFF\_OUT\_CM}$	AC common-mode voltage on OUT0±(1)	Default setting, PRBS9, 11.88Gbps		7		mVrms

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDI DRIVER OUTPUT (SDI_OUT+)						
R_{OUT_TERM}	DC output single-ended termination	SDI_OUT+ and SDI_OUT– to VIN	63	75	87	Ω
VOD_{CD_OUTP}	Output single-ended output voltage	Measure AC signal at SDI_OUT+, with SDI_OUT- AC terminated with 75Ω. Measured with color bar on Phabrix Qx with 1m B1694A at 11.88Gbps SDI_VOD=H		840		mVpp
		SDI_VOD=F(3)	720	800	880	mVpp
		SDI_VOD=R		880		mVpp
		SDI_VOD=L		760		mVpp
VOD_{CD_OUTN}	Output single-ended output voltage	Measure AC signal at SDI_OUT-, with SDI_OUT+ AC terminated with 75Ω. Measured with color bar on Phabrix Qx with 1m B1694A at 11.88Gbps SDI_VOD=H		840		mVpp
		SDI_VOD=F(3)	720	800	880	mVpp
		SDI_VOD=R		880		mVpp
		SDI_VOD=L		760		mVpp
PRE_{CD_OUTP}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT+, programmed to maximum setting through register, measured at SDI_VOD=F with 8T pattern at 11.88Gbps		2.5		dB
$PRE_{CD\_OUTP\_T}$	Output pre-emphasis duration	Output pre-emphasis time duration, measured after 0.5" trace, BNC connector, and 1m B1694A cable with 8T pattern at 11.88Gbps		83		ps
PRE_{CD_OUTN}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT–, programmed to maximum setting through register, measured at SDI_VOD=F with 8T pattern at 11.88Gbps		2.5		dB
$PRE_{CD\_OUTN\_T}$	Output pre-emphasis duration	Output pre-emphasis time duration, measured after 0.5" trace, BNC connector, and 1m B1694A cable with 8T pattern at 11.88Gbps		83		ps
$t_{R\_F\_SDI}$	Output rise and fall time(1)	Measured with color bar on Phabrix Qx, default VOD, default pre-emphasis 11.88Gbps		36		ps
		5.94Gbps		36		ps
		2.97Gbps		60		ps
		1.485Gbps		60		ps
		270Mbps		520		ps
$t_{R\_F\_DELTA}$	Output rise/fall time mismatch(1)	Measured with color bar on Phabrix Qx, default VOD, default pre-emphasis 11.88Gbps		5		ps
		5.94Gbps		8		ps
		2.97Gbps		13		ps
		1.485Gbps		53		ps
		270Mbps		75		ps
$V_{OVERSHOOT}$	Output overshoot or undershoot(2)	Measured with color bar on Phabrix Qx with 1m B1694A at SDI_OUT+, default VOD, default pre-emphasis, 12G		8		%

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DC_OFFSET}	DC offset	Measured with Phabrix Qx with 1m B1694A at SDI_OUT+, 12G/6G/3G/HD/SD		±0.2		V
V_{DC_WANDER}	DC wander	Measured with real-time scope with 1m B1694A at SDI_OUT+, 12G/6G/3G/HD with pathological pattern		13		mV
RL_{CD_S22}	Output return loss at SDI_OUT+ reference to 75Ω(1)	S22, 5MHz to 1.485GHz		–23		dB
		S22, 1.485GHz to 3GHz		–16		dB
		S22, 3GHz to 6GHz		–16		dB
		S22, 6GHz to 12GHz		–15		dB

(1) This parameter is measured with the LMH1239EVM (Evaluation board for LMH12x9).
(2) $V_{OVERSHOOT}$ overshoot/undershoot maximum measurements are largely affected by the PCB layout and input test pattern. The maximum value specified in Electrical Characteristics for $V_{OVERSHOOT}$ is based on bench evaluation across temperature and supply voltages with the LMH1239EVM.
(3) This limit is ensured by bench characterization and is not production tested.
(4) All specifications characterized with SDI_IN± on LMH1229 are applicable to both SDI_IN± and SDI_IN1± on LMH1239.
(5) External loop filter capacitor required between LF+ and LF- to implement reduced PLL bandwidth.
(6) Reclocker automatically goes into bypass when the LMH12x9 does not lock to a valid $LOCK_{RATE}$ data rate. When bypassed, LMH12x9 EQ adaptation is disabled and EQ index must be programmed manually (for more information, refer to the LMH12x9 Programming Guide).

5.6 Timing Requirements for Serial Management (SM) Bus Interface

over recommended operating supply and temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
F_{SCL}	SMBus SCL frequency			400	kHz
T_{BUF}	Bus free time between stop and start condition	1.3			µs
$T_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$T_{SU:STA}$	Repeated start condition setup time	0.6			µs
$T_{SU:STO}$	Stop condition setup time	0.6			µs
$T_{HD:DAT}$	Data hold time	0			ns
$T_{SU:DAT}$	Data setup time	100			ns
T_{LOW}	Clock low period	1.3			µs
T_{HIGH}	Clock high period	0.6			µs
T_R	Clock/data rise time			300	ns
T_F	Clock/data fall time			300	ns
T_{POR}	SMBus ready time after POR. Time from minimum VIN to SMBus valid write/read access.			50	ms

(1) These parameters support SMBus 2.0 specifications.
(2) For explanation of parameters, refer to SMBus timing parameter figures.

5.7 Timing Requirements for Serial Parallel Interface (SPI) Interface

over recommended operating supply and temperature range (unless otherwise noted)(1) (2)

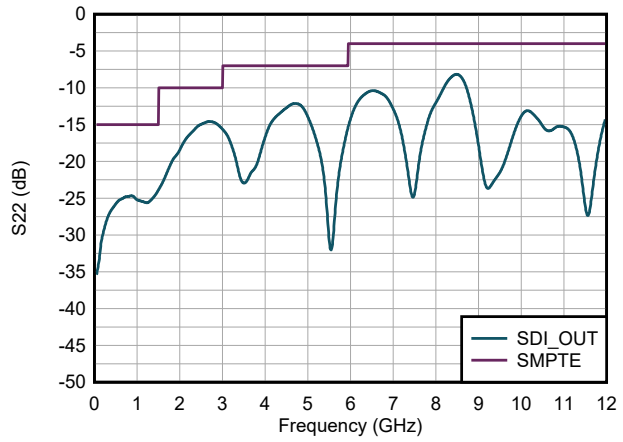
		MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK frequency			10	MHz
T_{PH}	SCK pulse width high	40			% SCK period
T_{PL}	SCK pulse width low	40			% SCK period
T_{SU}	PICO setup time	4			ns
T_{H}	PICO hold time	4			ns
T_{SSSU}	SS setup time	14			ns
T_{SSH}	SS hold time	4			ns
T_{SSOF}	SS off time	1			µs
T_{ODZ}	POCI driven-to-tristate time		20		ns
T_{OZD}	POCI tristate-to-driven time		10		ns
T_{OD}	POCI output delay time		15		ns

(1) Typical SPI load capacitance is 2 pF.
(2) For explanation of parameters, refer to SPI timing parameter figures.

5.8 Typical Characteristics

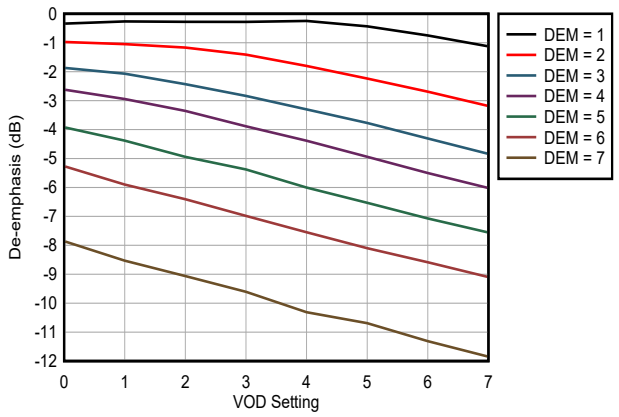
5.8.1 TX Characteristics

The following conditions apply (unless otherwise noted): T_A = 25°C; VDD = 2.5V, All measurements performed with LMH1239EVM.



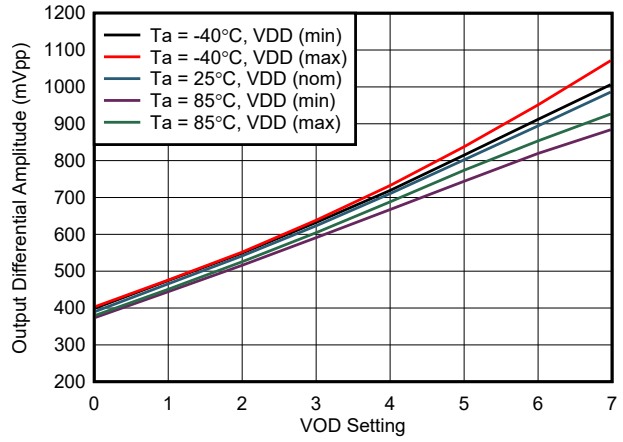
Measured with LMH1239EVM.

図 5-1. Output Return Loss (RL) vs Frequency



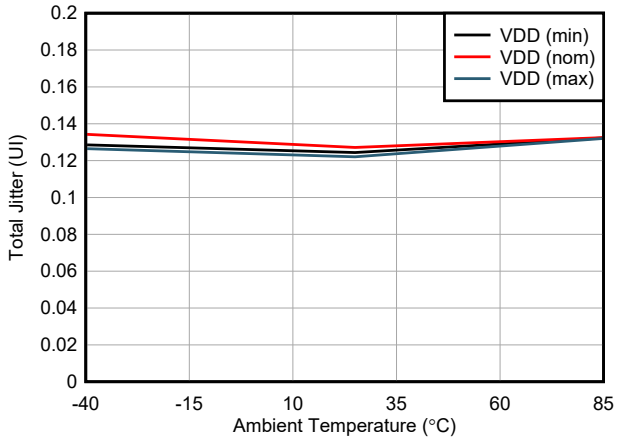
Measured with 8T pattern at 11.88Gbps.

図 5-2. OUT0 De-Emphasis vs. Register Settings



Measured with 8T pattern at 11.88Gbps.

図 5-3. OUT0 VOD vs. Register Settings

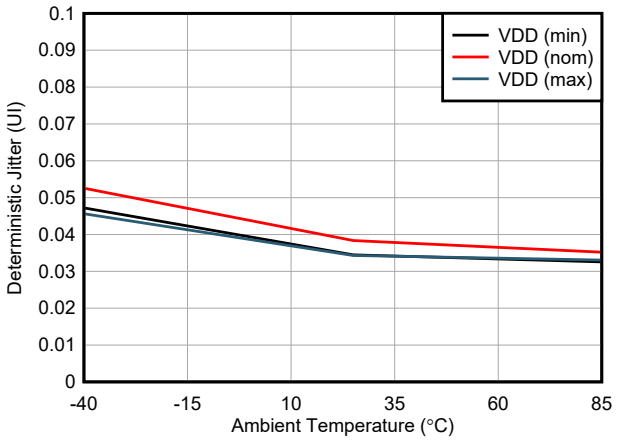


Measured with PRBS9 pattern.

図 5-4. OUT0 Total Jitter (TJ) at 11.88Gbps

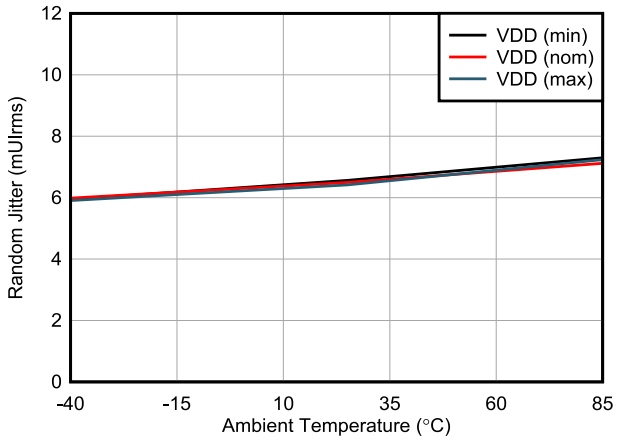
5.8.1 TX Characteristics (continued)

The following conditions apply (unless otherwise noted): T_A = 25°C; VDD = 2.5V, All measurements performed with LMH1239EVM.



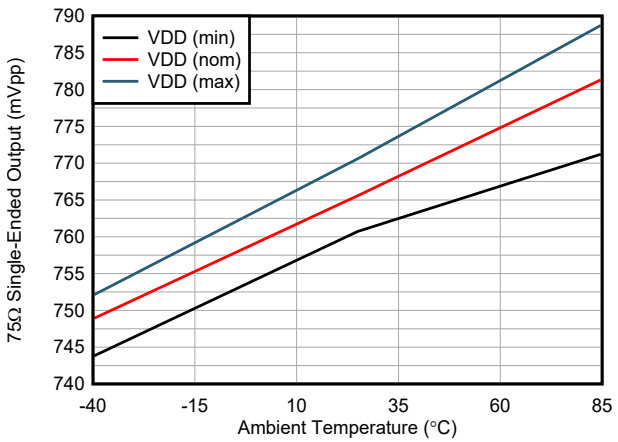
Measured with PRBS9 pattern.

図 5-5. OUT0 Deterministic Jitter (DJ) at 11.88Gbps



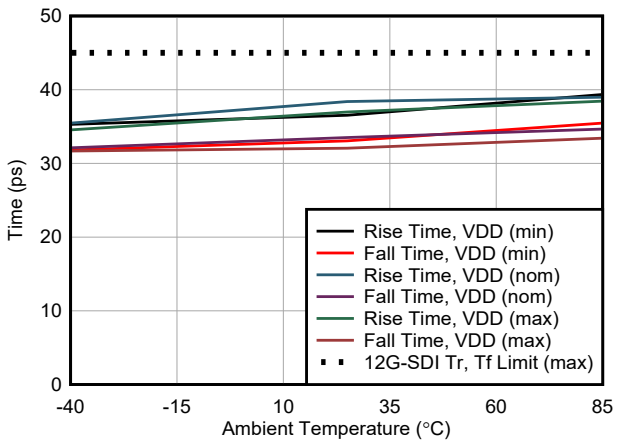
Measured with PRBS9 pattern.

図 5-6. OUT0 Random Jitter (RJ) at 11.88Gbps



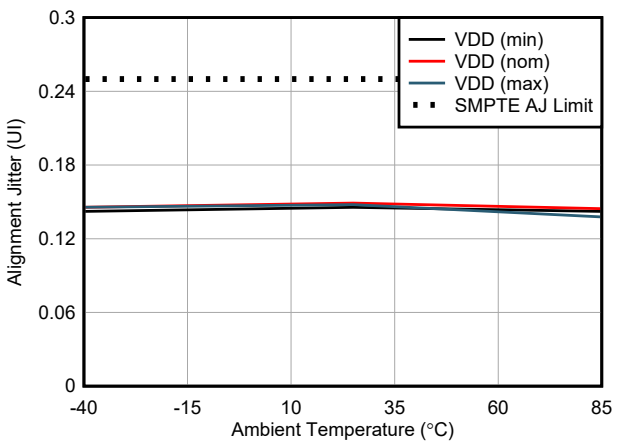
Measured with Phabrix Qx color bar pattern.

図 5-7. SDI_OUT VOD at 11.88Gbps



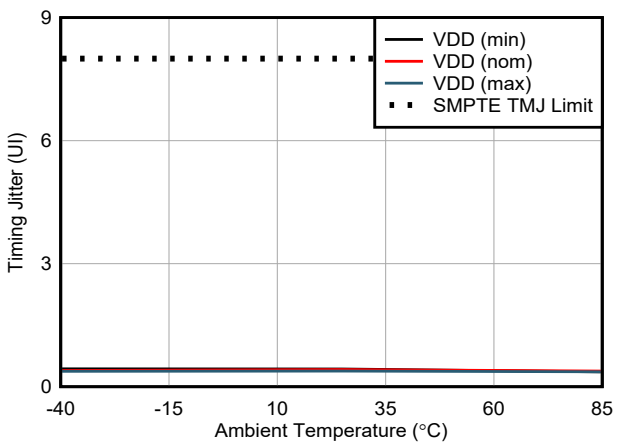
Measured with Phabrix Qx color bar pattern.

図 5-8. SDI_OUT Rise and Fall Time at 11.88Gbps



Measured with Phabrix Qx color bar pattern.

図 5-9. SDI_OUT Alignment Jitter (AJ) at 11.88Gbps

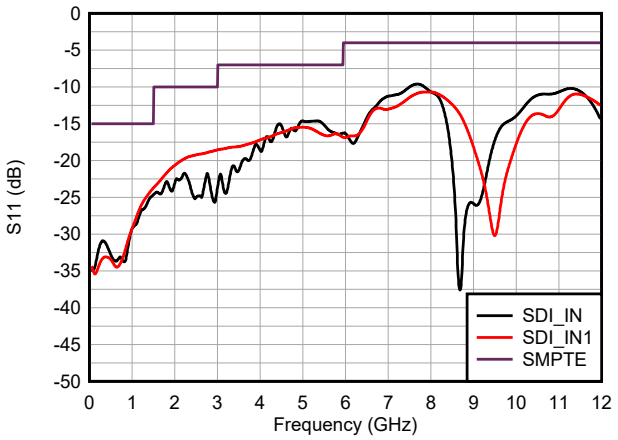


Measured with Phabrix Qx color bar pattern.

図 5-10. SDI_OUT Timing Jitter (TMJ) at 11.88Gbps

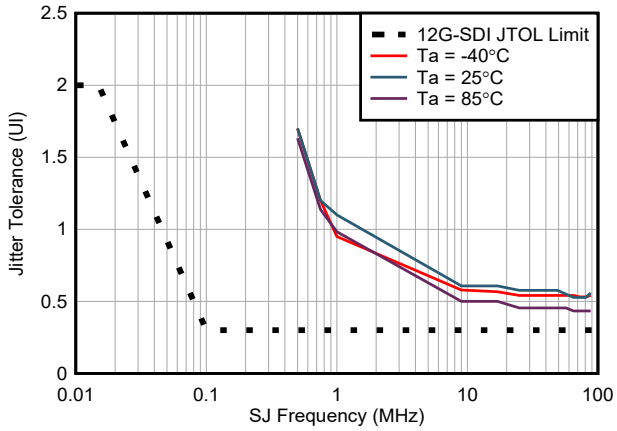
5.8.2 RX Characteristics

The following conditions apply (unless otherwise noted): T_A = 25°C; VDD = 2.5V, All measurements performed with LMH1239EVM.



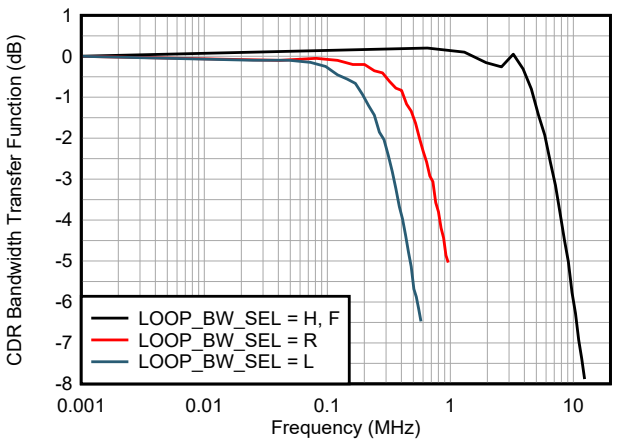
Measured with LMH1239EVM.

図 5-11. Input Return Loss (RL) vs Frequency



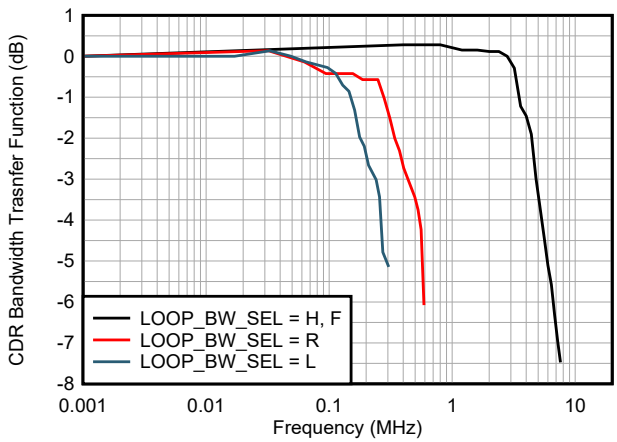
Measured with 1m B1694A cable input.

図 5-12. Typical Jitter Tolerance vs Frequency



Measured with 1m B1694A cable input.

図 5-13. Typical PLL Bandwidth at 11.88Gbps vs Frequency



Measured with 1m B1694A cable input.

図 5-14. Typical PLL Bandwidth at 2.97Gbps vs Frequency

6 Detailed Description

6.1 Overview

The LMH12x9 is TI's second generation long-reach 12G UHD-SDI adaptive cable equalizer with integrated reclocker, supporting all SMPTE video rates up to 11.88Gbps. The LMH12x9 has a 75Ω cable equalizer input capable of equalizing up to 100m Belden 1694A cable.

The 75Ω cable equalizer input features an internal 75Ω termination and compensation network to meet stringent SMPTE return loss requirements. The 75Ω cable equalizer input passes through a multi-rate reclocker with a programmable loop filter.

The on-chip reclocker attenuates high-frequency jitter and fully regenerates the data using a clean, low-jitter clock. The reclocker has a built-in loop filter and does not require any input reference clock. The LMH12x9 also has an internal eye opening monitor and a programmable pin for CDR lock indication, input carrier detect, or hardware interrupts to support system diagnostics and board bring-up.

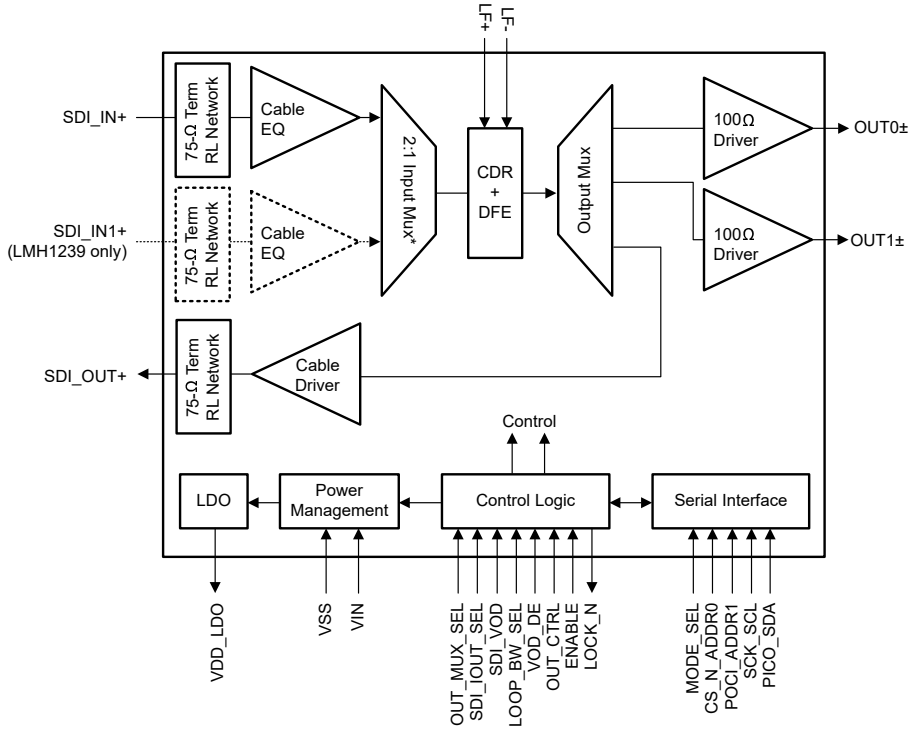
After the reclocker is a 1:3 fan-out mux. Two of the outputs are 100Ω drivers with de-emphasis for PCB routing of data or clock signals, while the third output is a 75Ω driver with pre-emphasis for reclocked SDI loop-through data in cascaded applications.

The LMH12x9 is offered in a 5mm × 5mm 32-pin WQFN package with two pinout variants:

- **LMH1229:** Pin-to-pin drop-in replacement for LMH1297 12G-SDI Bidirectional I/O (Equalizer mode)
- **LMH1239:** Unique pinout with additional 2:1 75Ω input mux included for system redundancy

The LMH12x9 is powered from a single 2.5V supply with an on-chip 1.8V LDO regulator. The operating state of the LMH12x9 can be configured through control pins, SPI, or SMBus serial control interface. In the absence of an input signal, the LMH12x9 automatically goes into Power Save mode. Users can also manually force the LMH12x9 into Power Save mode through the ENABLE control pin. The LMH1297 is offered in a small 5mm × 5mm, 32-pin QFN package.

6.2 Functional Block Diagram



*2:1 Input mux is only applicable with the LMH1239 variant. For LMH1229, SDI_IN+ data path is routed directly to the CDR.

6.3 Feature Description

The LMH12x9 consists of several key blocks, which are as follows:

- 4-Level Input Configuration Pins
- Input and Output Signal Flow Control
- Input Carrier Detect
- Adaptive Cable Equalizer (SDI_IN±, SDI_IN1±)
- Clock and Data (CDR) Recovery
- CDR Loop Bandwidth Control
- Output Function Control
- Output Driver Control
- Debug and Diagnostic Features

6.3.1 4-Level Input Pins and Thresholds

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30kΩ pullup and a 60kΩ pulldown connected to the control pin that sets the default voltage at 2/3 x VIN. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1kΩ pulldown, 20kΩ pulldown, no connect, and 1kΩ pullup, the optimal voltage levels for each of the four input states are achieved as provided in 表 6-1.

表 6-1. 4-Level Control Pin Settings

LEVEL	SETTING	RESULTING PIN VOLTAGE
H	Tie 1 kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20 kΩ to VSS	1/3 × VIN
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VIN
- Internal Threshold between R and F = 0.5 × VIN
- Internal Threshold between F and H = 0.8 × VIN

6.3.2 Input and Output Signal Flow Control

The input and output signal flow of the LMH12x9 is determined by the IN_MUX_SEL (LMH1239 only), OUT_MUX_SEL, and SDI_OUT_SEL pins.

6.3.2.1 Input Mux Selection (LMH1239 Only)

The LMH12x9 receives a 75Ω SDI input signal. For the LMH1229, the input is provided on SDI_IN+. For the LMH1239, the input setting can be between SDI_IN± and SDI_IN1± based on the IN_MUX_SEL pin logic settings provided in 表 6-2. These settings can be overridden through register control by applying the appropriate override bit values. For more information, refer to the LMH12x9 Programming Guide.

表 6-2. IN_MUX_SEL Pin Settings

LEVEL(1)	DEFINITION
H	Select SDI_IN±
F	
R	Select SDI_IN1±
L	

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.

注

Either positive (+) or negative (-) polarity can be used for SDI_IN± and SDI_IN1± for the 75Ω SDI input signal. The unused polarity should be AC terminated with external 4.7µF and 75Ω to GND.

6.3.2.2 Output Mux and SDI_OUT Selection

The OUT_MUX_SEL and SDI_OUT_SEL pins select the LMH12x9 output data-path routes. 表 6-3 and 表 6-4 show how to configure the output signal path for various configurations.

表 6-3. OUT_MUX_SEL Pin Settings

LEVEL(1)	DEFINITION
H	Disable OUT0± Disable OUT1±
F	Enable OUT0± Disable OUT1±
R	Enable OUT0± Enable OUT1±
L	Enable OUT0± Disable OUT1±

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.

表 6-4. SDI_OUT_SEL Pin Settings

LEVEL(1)	DEFINITION
H	Disable SDI_OUT±
L	Enable SDI_OUT±

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.

6.3.3 Input Carrier Detect

The LMH12x9 has a carrier detect circuit to monitor the presence or absence of an input signal. When the input signal amplitude for the selected input exceeds the carrier detect assert threshold, the LMH12x9 operates in normal operation mode.

In the absence of an input signal, the LMH12x9 automatically goes into Power Save mode to conserve power dissipation. When a valid signal is detected, the LMH12x9 automatically exits Power Save mode and returns to the normal operation mode. If the ENABLE pin is pulled low, the LMH12x9 is forced into Power-Down mode. In Power Save mode, both the carrier detect circuit and the serial interface remain active. In Power-Down mode, only the serial interface (SMBus or SPI based on MODE_SEL pin) remains active.

Users can monitor the status of the carrier detect through register programming. This can be done either by configuring the LOCK_N pin to output the CD_N status or by monitoring the carrier detect status register.

6.3.4 Adaptive Cable Equalizer (SDI_IN±, SDI_IN1±)

The LMH12x9 receiver features an adaptive continuous-time linear equalizer (CTLE) and a continuously adaptive three-tap decision feedback equalizer (DFE).

- **CTLE:** Compensates for frequency-dependent loss due to the transmission media prior to the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies. The CTLE block extends the signal bandwidth, restores the signal amplitude, and reduces ISI caused by the transmission medium. The CTLE adapts once following each signal detection event.
- **Three-tap DFE:** Works in tandem with the CTLE to provide additional insertion loss compensation alongside crosstalk and reflection tolerance. The DFE is continuously-adaptive to compensate for temperature-related variations in the channel.

注

The CTLE can be manually overridden through register control. Manual override is not recommended for data rates where reclocker is enabled (see 表 6-5).

Adaptive cable equalization is enabled by default. The LMH12x9 SDI_input (SDI_IN, SDI_IN1) has an on-chip 75-Ω termination to the input common-mode voltage and includes a series return loss compensation network for meeting stringent SMPTE return loss requirements. The cable equalizer is designed with high gain and low noise circuitry to compensate for the insertion loss of a coaxial cable (such as Belden 1694A), which is widely used in broadcast video infrastructures.

注

Adaptation is not applied for data rate inputs where the relocker is bypassed (including MADI). When operating with the reclocker bypassed, the appropriate EQ index must be programmed manually.

6.3.5 Clock and Data (CDR) Recovery

After the input signal passes through the adaptive cable equalizer, the equalized data is fed into the clock and data recovery (CDR) block. Using an internal PLL, the CDR locks to the incoming equalized data and recovers a clean internal clock to re-sample the equalized data. The LMH12x9 CDR is able to tolerate high input jitter, tracking low-frequency input jitter below the PLL bandwidth while reducing high-frequency input jitter above the PLL bandwidth. The supported data rates are listed in 表 6-5.

表 6-5. Supported Data Rates

INPUT	DATA RATE	RECLOCKER
SDI_IN+ or SDI_IN1+	11.88Gbps, 5.94Gbps, 2.97Gbps, 1.485Gbps, 270Mbps(1)	Enable
	All other data rates (including 125Mbps)	Bypass

(1) The LMH12x9 supports divide-by-1.001 lock rates for 11.88Gbps, 5.94Gbps, 2.97Gbps, and 1.485Gbps.

6.3.6 CDR Loop Bandwidth Control

A key characteristic of CDR operation is the loop bandwidth. Input jitter at frequencies above the -3dB CDR loop bandwidth are attenuated by the CDR, while input jitter at frequencies below the -3dB CDR loop bandwidth are tracked but not attenuated at the CDR output. Depending on the input jitter present at the LMH12x9 input and application needs for the LMH12x9 output jitter, the CDR loop bandwidth can be adjusted.

The LMH12x9 features a highly configurable CDR loop bandwidth that can be controlled by either pin or register settings.

注

The default LMH12x9 CDR loop bandwidth (no external capacitor on LF+ and LF- pins) are comparable to previous generation LMH1219 and LMH1297 (EQ Mode) devices. To enable a lower CDR loop bandwidth, an external 470nF capacitor on LF+ and LF- is required.

6.3.7 Output Function Control

The LMH12x9 output function control for data routed to outputs SDI_OUT, OUT0, and OUT1 is configured by the OUT_CTRL pin. The OUT_CTRL pin determines whether to bypass the input cable equalizer, reclocker, or both. In normal operation (OUT_CTRL = F), both input equalizer and reclocker are enabled.

表 6-6 lists the OUT_CTRL pin logic settings. These settings can be overridden through register control by applying the appropriate override bit values. For more information, refer to the LMH12x9 Programming Guide.

表 6-6. OUT_CTRL Settings for Bypass Modes

OUT_CTRL(1)	SDI INPUT CABLE EQUALIZER	RECLOCKER	DEFINITION
H, F	Enable	Enable	Normal operation OUT0, SDI_OUT, and OUT1: Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled
R	Enable	Enable	OUT0 and SDI_OUT: Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled OUT1: Full-Rate Recovered Clock if Data Rate ≤ 2.97Gbps. 297MHz Recovered Clock if Data Rate > 2.97Gbps
L	Enable	Bypass	Debug Only OUT0, SDI_OUT, and OUT1: Equalized Data, Cable EQ (CTLE, DFE) enabled and reclocker bypassed(2)

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.
(2) When OUT_CTRL = L, the reclocker is bypassed but not powered down (that is, still locked), as the reclocker is needed for the DFE to function properly.

6.3.8 Output Driver Control

6.3.8.1 Line-Side 75Ω Output Cable Driver (SDI_OUT±)

The LMH12x9 has one output cable driver (CD) block for SDI_OUT. The SDI output is designed to drive 75Ω single-ended coaxial cables at data rates up to 11.88Gbps. SDI_OUT features an integrated 75Ω termination and return loss compensation network for meeting stringent SMPTE return loss requirements.

6.3.8.1.1 Output Amplitude (VOD)

SDI_OUT serves as a loop-through output and is designed for transmission across 75Ω single-ended impedance. The nominal SDI cable driver output amplitude (VOD) is 800mVpp single-ended. In the presence of long output cable lengths or crosstalk, the SDI_VOD pin can be used to optimize the cable driver output with respect to the nominal amplitude. 表 6-7 details VOD settings that can be applied to SDI_OUT. The SDI_VOD pin can be overridden through register control. In addition, the nominal VOD amplitude can be changed by register control. For more information, refer to the LMH12x9 Programming Guide.

表 6-7. SDI_VOD Settings for Line-Side Output Amplitude

SDI_VOD(1)	DESCRIPTION
H	about +5% of nominal
F	800mVpp (nominal)
R	about +10% of nominal
L	about –5% of nominal

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.

6.3.8.1.2 Output Pre-Emphasis

In addition to SDI cable driver VOD control, the LMH12x9 can add pre-emphasis on the cable driver output to improve output signal integrity when the reclocker recovers a UHD (12G, 6G) or HD (3G, 1.5G) input data rate. By default, pre-emphasis is enabled for 12G and 6G data rates, and is disabled for all other data rates. When pre-emphasis is disabled, the effects of crosstalk on SDI_IN are minimized at SDI_OUT. When enabled, the amount of pre-emphasis applied to the cable driver output is determined by register control. If the reclocker is bypassed or if the user desires to disable automatic pre-emphasis, pre-emphasis can be enabled manually through register control. For more information, refer to the LMH12x9 Programming Guide.

6.3.8.1.3 Output Slew Rate

SMPTE specifications require different output driver rise and fall times depending on the operating data rate. To meet these requirements, the output edge rate of SDI_OUT is automatically programmed according to the signal recovered by the reclocker. Typical edge rates at the cable driver output are shown in the *Electrical Characteristics* table.

If the reclocker is bypassed, users must program the desired edge rate manually through register control. For more information, refer to the LMH12x9 Programming Guide.

6.3.8.1.4 Output Polarity Inversion

Polarity inversion is supported on the SDI_OUT output through register control.

6.3.8.2 Host-Side 100Ω Output Driver (OUT0±, OUT1±)

OUT0 and OUT1 are host-side 100Ω driver outputs from the SDI input cable equalizer. Both OUT0 and OUT1 also support polarity inversion.

The driver offers the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

The VOD_DE pin determines the output amplitude (VOD) and de-emphasis levels applied to the OUT0 and OUT1 PCB driver. These settings can be changed through register control if finer resolution in settings is desired.

表 6-8 details the OUT0 and OUT1 VOD and de-emphasis settings that can be applied. The VOD_DE pin settings can be overridden by register control. When these parameters are controlled by registers, the VOD and de-emphasis levels can be programmed independently. For more information, refer to the LMH12x9 Programming Guide.

表 6-8. VOD_DE Pin Settings

VOD_DE(1)	OUT0± and OUT1± VOD (mVpp)	OUT0± and OUT1± DEM (dB)	RECOMMENDED BOARD TRACE AT OUT0± and OUT1±(2)
H	410	0	< 1 inch
F	560	–1.0	1-2 inches
R	635	–2.4	4-5 inches
L	810	–6.1	8-10 inches

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.
(2) Recommended board trace at 11.88Gbps.

6.3.9 Debug and Diagnostic Features

6.3.9.1 Internal Eye Opening Monitor (EOM)

The LMH12x9 has an on-chip eye opening monitor (EOM) that can be used to analyze, monitor, and diagnose the post-equalized waveform, just prior to the CDR reclocker.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400mV. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of hits, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of hits registered at each point needs to be taken in context with the total number of bits observed at that voltage and phase offset to determine the corresponding probability for that point.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. 図 6-1 and 図 6-2 show two common ways to visualize this data. These diagrams depict examples of eye monitor plots implemented by software. The first plot is an example using the EOM data to plot a basic eye using ASCII characters, which can be useful for diagnostic software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossings that comprise the eye.

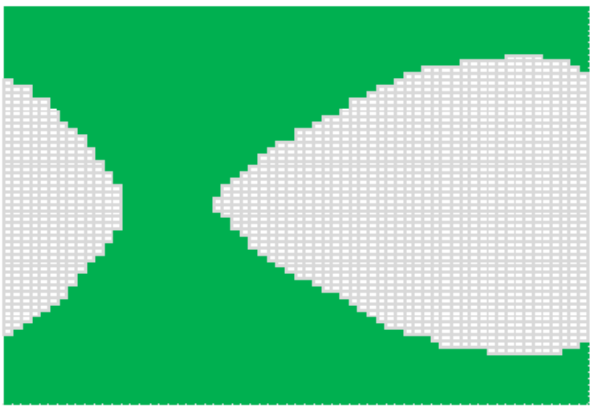


図 6-1. Internal Input Eye Monitor Plot

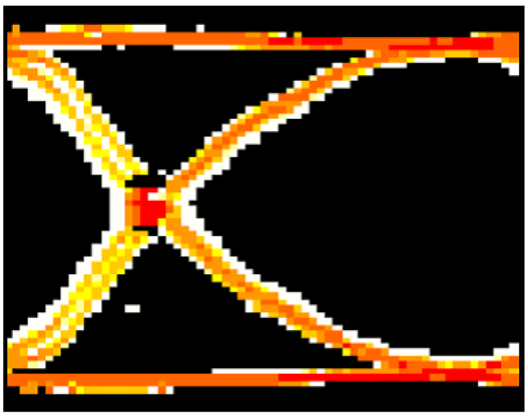


図 6-2. Internal Eye Monitor Hit Density Plot

A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0V differential amplitude, measured in unit intervals or picoseconds (ps). The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase. HEO and VEO measurements can be read back through register control.

6.3.9.2 PRBS Generator, Error Checker, and Error Injector

Each LMH12x9 transmitter output can be configured independently to output a PRBS-7, PRBS-9, PRBS-23, or PRBS-31 for debug purposes. To output a PRBS signal, the LMH12x9 input must be CDR locked to a valid incoming signal at the same rate as the desired PRBS output generated rate.

The LMH12x9 SDI receiver input (SDI_IN or SDI_IN1) can be configured as a PRBS error checker, capable of identifying and tracking PRBS-7, PRBS-9, PRBS-23, or PRBS-31 signals for errors for debug purposes. To enable PRBS error checker functionality, the LMH12x9 must be locked to a valid SDI data rate.

To check the accuracy of the PRBS error checker, each transmitter, when configured as a PRBS generator, can be programmed to inject a single bit error through register control. This error injection ability allows users to verify that the PRBS generator is outputting correctly and that PRBS error checker is functioning as expected.

6.3.9.3 Status Indicators and Interrupts

The LOCK_N pin is a 3.3V tolerant, active-low, open-drain output. An external resistor to the logic supply is required. The LOCK_N pin can be configured to indicate reclocker lock, input carrier detect, cable fault detection, or an interrupt event.

6.3.9.3.1 LOCK_N (Lock Indicator)

By default, LOCK_N is the reclocker lock indicator, and this pin asserts low when the LMH12x9 achieves lock to a valid SMPTE data rate. The LOCK_N pin functionality can also be configured through register control to indicate CD_N (carrier detect) or INT_N (interrupt) events. For more information about how to reconfigure the LOCK_N pin functionality, refer to the LMH12x9 Programming Guide.

6.3.9.3.2 CD_N (Carrier Detect)

The LOCK_N pin can be reconfigured through register control to indicate a CD_N (carrier detect) event. When configured as a CD_N output, the pin asserts low at the end of adaptation after a valid signal is detected by the carrier detect circuit of the selected input. For more information about how to configure the LOCK_N pin for CD_N functionality, refer to the LMH12x9 Programming Guide.

6.3.9.3.3 Cable Fault Detection (SDI_OUT+ Only)

The LMH12x9 features cable fault detection to indicate when no cable is connected to the SDI_OUT+ output. Cable fault detection can determine a fault for up to 600m of Belden 1694A cable at SDI_OUT+. This feature allows a method for users to react to cable attachment and removal.

When SDI_OUT_SEL is enabled, the LMH12x9 senses the SDI_OUT+ amplitude. If the output is not properly terminated (through a terminated cable or local termination), the cable fault detection signal asserts. The cable fault detection signal deasserts when a proper 75Ω termination is applied.

If cable fault detection is used to power down the LMH12x9 through the ENABLE pin, periodic polling with the LMH12x9 momentarily powered up is recommended to monitor the SDI_OUT+ termination.

注

Cable Fault Detection is only available when using the SDI_OUT+ polarity.

6.3.9.3.4 INT_N (Interrupt)

The LOCK_N pin can be configured to indicate an INT_N (interrupt) event. When configured as an INT_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Four separate masks can be programmed through register control as interrupt sources:

- If there is a loss of signal (LOS) event on the SDI input, irrespective of the input channel (SDI_IN± or SDI_IN1±) selected (two separate masks).
- If a CDR Lock event has occurred (two separate masks).

INT_N is a sticky bit, meaning that the bit flags after an interrupt occurs and will not clear until read-back. After the Interrupt Status Register is read, the INT_N pin asserts high again. For more information about how to configure the LOCK_N pin for INT_N functionality, refer to the LMH12x9 Programming Guide.

6.3.9.4 Additional Programmability

The LMH12x9 supports extended programmability through SPI or SMBus serial control interface. Such added

programmability includes:

- Cable EQ Index (CEI)
- Digital $MUTE_{REF}$

6.3.9.4.1 Cable EQ Index (CEI)

The Cable EQ Index (CEI) indicates the cable EQ boost index used at SDI_IN+. CEI is accessible through register control. The 6-bit setting ranges in decimal value from 0 to 55 (000000'b to 110111'b in binary), with higher values corresponding to larger gain applied at the SDI input.

6.3.9.4.2 Digital $MUTE_{REF}$

Digital $MUTE_{REF}$ sets the threshold for the maximum cable length at the SDI input to be equalized before muting the outputs. The $MUTE_{REF}$ register value is directly proportional to the cable length being equalized. $MUTE_{REF}$ is data rate dependent. Refer to the LMH12x9 Programming Guide to set the $MUTE_{REF}$ threshold for any desired SDI rate.

6.4 Device Functional Modes

The LMH12x9 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. To determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power-up, as detailed in 表 6-9.

表 6-9. MODE_SEL Pin Settings

LEVEL(1)	DEFINITION
H(2)	Forced Power Save Mode, only SPI is enabled (all other circuitry powered down)
F	Select SPI for register access
R	Reserved for factory testing – do not use
L	Select SMBus Interface for register access

(1) See Pin Configurations and Functions for LMH12x9 pin mapping details.
(2) For pin compatibility, note that the LMH1297 pin configuration defines Level H as “Reserved for factory testing – do not use.”

6.4.1 System Management Bus (SMBus) Mode

The SMBus interface can also be used to control the device. If MODE_SEL = Low (1 kΩ to VSS), PICO_SDA and SCK_SCL pins are configured as SDA and SCL. CS_N_ADDR0 and POCI_ADDR1 pins are address straps ADDR0 and ADDR1 during power up. The maximum operating speed supported on the SMBus pins is 400kHz.

表 6-10. SMBus Device Target Addresses (1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT TARGET ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	3D	7A
L	R	3E	7C
L	F	3F	7E
L	H	40	80
R	L	41	82
R	R	42	84
R	F	43	86
R	H	44	88
F	L	45	8A
F	R	46	8C
F	F	47	8E
F	H	48	90
H	L	49	92
H	R	4A	94
H	F	4B	96
H	H	4C	98

(1) The 8-bit write command consists of the 7-bit target address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit target address is 0x3D (011 1101'b), the 8-bit write command is 0x7A (0111 1010'b).

6.4.1.1 SMBus Read and Write Transaction

SMBus is a two-wire serial interface through which various system component chips can communicate with the controller. Target devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the controller to all of the target devices on the bus. SDA is a bidirectional data signal between the controller and target devices. The LMH12x9 SMBus SCL and SDA signals are open-drain and require external pullup resistors.

Start and Stop:

The controller generates Start and Stop patterns at the beginning and end of each transaction.

- Start: High to low transition (falling edge) of SDA while SCL is high.
- Stop: Low to high transition (rising edge) of SDA while SCL is high.

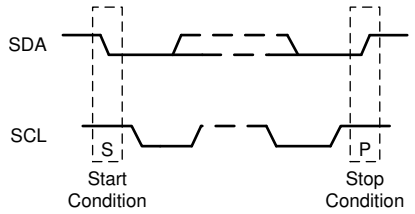


図 6-3. Start and Stop Conditions

The controller generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

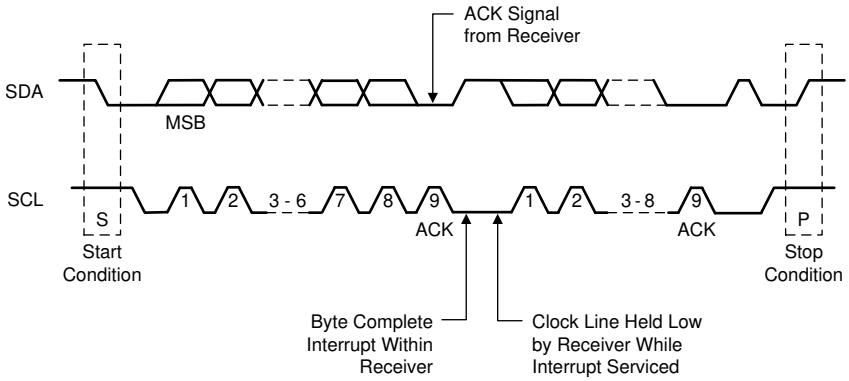


図 6-4. Acknowledge (ACK)

6.4.1.1.1 SMBus Write Operation Format

Writing data to a target device consists of three parts, as illustrated in 図 6-5:

1. The controller begins with a start condition followed by the target device address with the R/ $\overline{W}$ bit set to 0'b.
2. After an ACK from the target device, the 8-bit register word address is written.
3. After an ACK from the target device, the 8-bit data is written, followed by a stop condition.

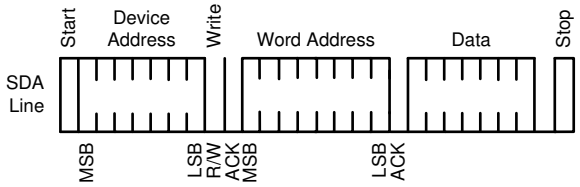


図 6-5. SMBus Write Operation

6.4.1.1.2 SMBus Read Operation Format

SMBus read operation consists of four parts, as illustrated in 図 6-6:

1. The controller begins with a start condition, followed by the target device address with the R/ $\overline{W}$ bit set to 0'b.
2. After an ACK from the target device, the 8-bit register word address is written.
3. After an ACK from the target device, the controller initiates a restart condition, followed by the Target address with the R/ $\overline{W}$ bit set to 1'b.
4. After an ACK from the target device, the 8-bit data is read-back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

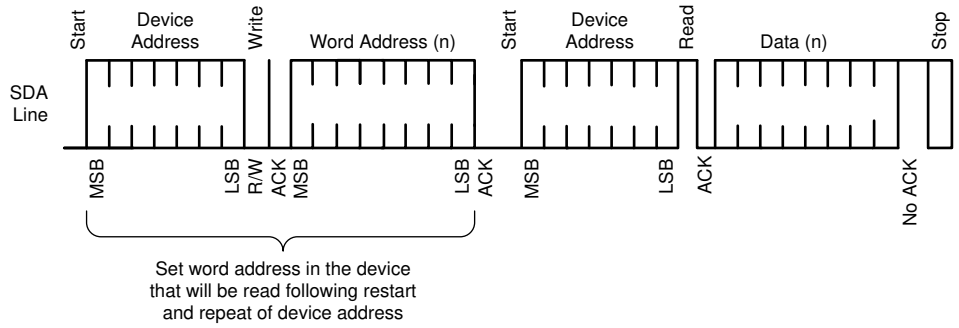


図 6-6. SMBus Read Operation

6.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH12x9 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- PICO_SDA: Peripheral Input Controller Output
- POCI_ADDR1: Peripheral Output Controller Input
- CS_N_ADDR0: Chip Select (Active Low)
- SCK_SCL: Serial Clock (Input to the LMH12x9 peripheral device)

6.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by CS_N when asserted low. The PICO input is ignored, and the POCI output is floated whenever CS_N is deasserted (high).

The bits are shifted in left-to-right. The first bit is R/ $\overline{W}$, which is 1'b for *read* and 0'b for *write*. Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on POCI as the current command, address, and data are shifted in on PICO. In all SPI transactions, the POCI output signal is enabled asynchronously when CS_N asserts low. The contents of a single PICO or POCI transaction frame are shown in 表 6-11.

表 6-11. 17-Bit Single SPI Transaction Frame

R/ $\overline{W}$	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

6.4.2.1.1 SPI Write Transaction Format

For SPI writes, the R/W bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of CS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in 図 6-7. The *prime* values on POCI (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are do not care for the current transaction.

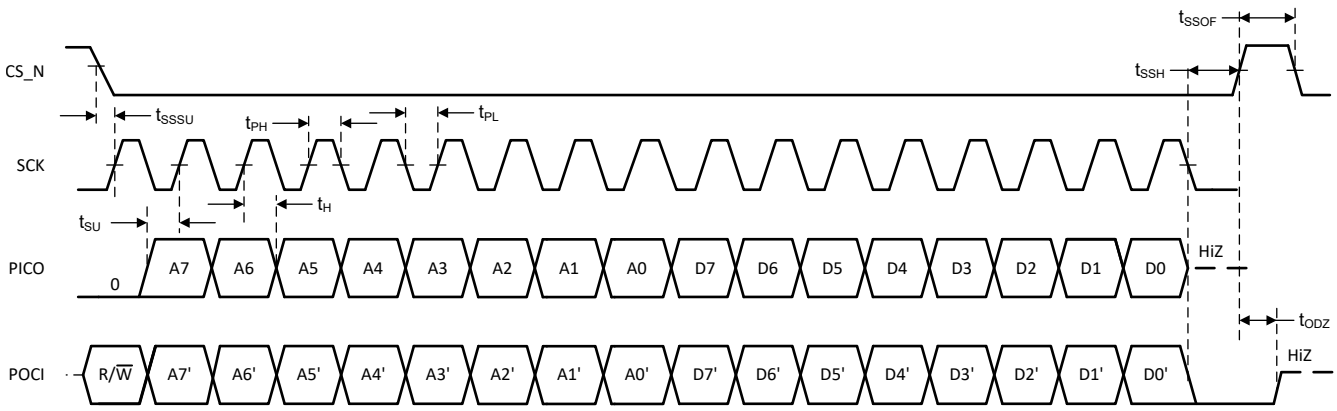


図 6-7. Signal Timing for a SPI Write Transaction

6.4.2.1.2 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/W bit is 1'b for the read transaction, as shown in 図 6-8.

The first 17 bits from the read transaction specifies 1-bit of R/W and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary to shift out the read data D7-D0 in the last 8 bits of the POCI output. As with the SPI Write, the *prime* values on POCI during the first 16 clocks are listed as do not care for this portion of the transaction. The values shifted out on POCI during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

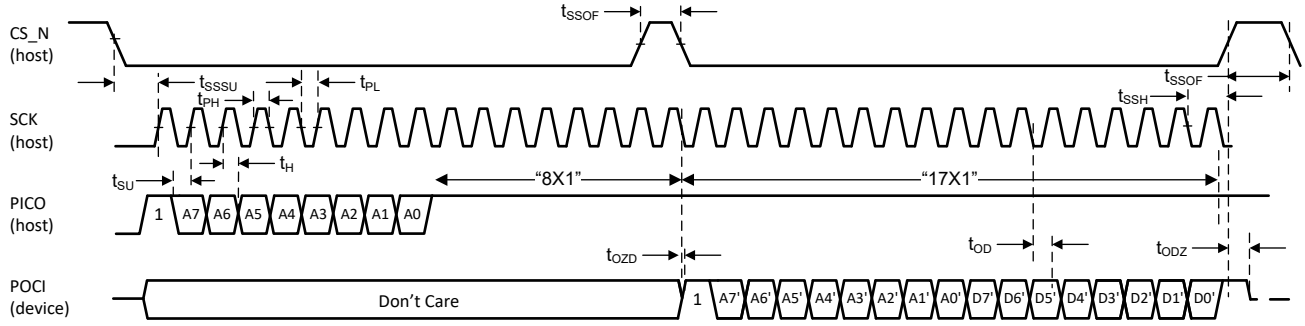


図 6-8. Signal Timing for a SPI Read Transaction

6.4.2.2 SPI Daisy Chain

The LMH12x9 supports SPI daisy-chaining among multiple devices, as shown in 図 6-9.

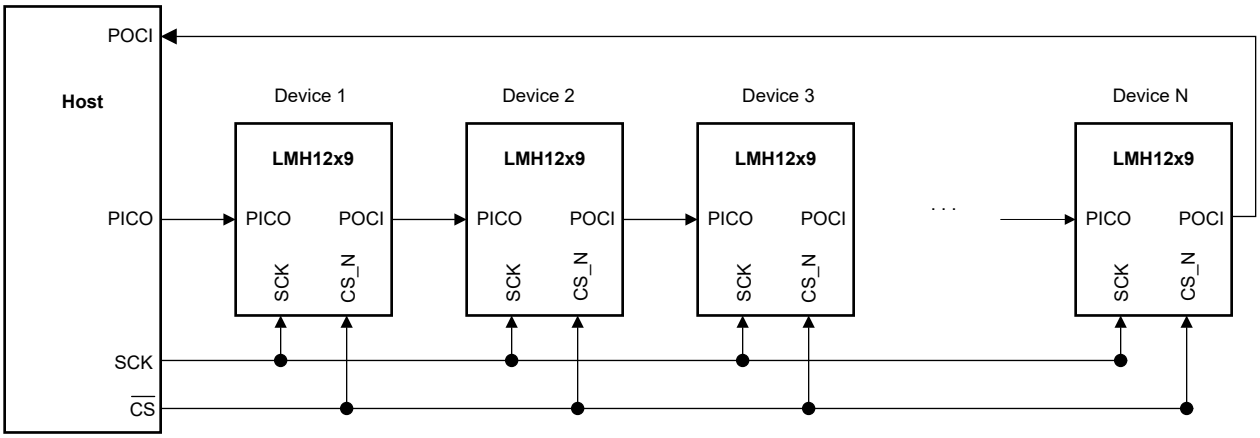


図 6-9. Daisy-Chain Configuration

Each LMH12x9 device is directly connected to the SCK and CS_N pins of the host. The first LMH12x9 device in the chain is connected to the host's PICO pin, and the last device in the chain is connected to the host's POCI pin. The PICO pin of each intermediate LMH12x9 device in the chain is connected to the POCI pin of the previous LMH12x9 device, thereby creating a serial shift register. In a daisy-chain configuration of N × LMH12x9 devices, the host conceptually sees a shift register of length 17 × N for a basic SPI transaction, during which CS_N is asserted low for 17 × N clock cycles.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 SMPTE Requirements and Specifications

SMPTE specifies several key requirements for the Serial Digital Interface to transport digital video over coaxial cables. Such requirements include return loss, AC coupling, and data rate dependency with rise and fall times.

1. **Return Loss:** This specification details how closely the port resembles 75Ω impedance across a specified frequency band. The LMH12x9 features a built-in 75Ω return-loss network on SDI_IN, SDI_IN1, and SDI_OUT to minimize parasitics and improve overall signal integrity.
2. **AC Coupling:** AC-coupling capacitors are required for transporting uncompressed serial data streams with heavy low-frequency content. The use of 4.7µF, AC-coupling capacitors is recommended to avoid low-frequency DC wander.
3. **Rise/Fall Time:** Output 75Ω signals are required to meet data dependent rise and fall timing. This improves the eye opening observed for the receiving device. The LMH12x9 SDI_OUT cable driver features automatic edge rate adjustment to meet SMPTE rise and fall time requirements.

TI recommends placing the LMH12x9 as close as possible (approximately 1 inch) to the 75Ω BNC ports to meet SMPTE specifications.

7.1.2 Optimizing the Time to Adapt and Lock

When carrier detect is asserted, the LMH12x9 adapts the cable equalizer to the optimal CTLE and DFE settings and locks to the determined SDI data rate. In applications where not all SDI rates are used, the time required to adapt the equalizer and achieve CDR lock to the incoming signal can be optimized by manually programming the LMH12x9 to lock only to the expected data rates. Refer to the LMH12x9 Programming Guide for more details.

7.1.3 Optimized Loop Bandwidth Settings for Diagnostic or Cascade Applications

The LMH12x9 default loop bandwidth setting is optimized for a wide variety of applications. For diagnostic or cascade applications, the SDI_OUT cable driver output can be used for monitoring, fanout, or cable extender purposes. To minimize the impact of jitter peaking caused by multiple cascaded devices having the same CDR loop bandwidth setting, the LMH12x9 CDR loop bandwidth can be increased or decreased from the default setting by pin strap (LOOP_BW_SEL) or by register control. Refer to *CDR Loop Bandwidth Control* for information regarding CDR loop bandwidth control. For more granular loop bandwidth control than the LOOP_BW_SEL pin strap options, refer to the LMH12x9 Programming Guide.

7.1.4 LMH1229 and LMH1297 (EQ Mode) Pin-to-Pin Compatibility

The LMH1229 pinout and footprint is compatible with the LMH1297 (12G-SDI Bidirectional I/O with Integrated Reclocker) when the LMH1297 is used in EQ mode. This pin compatibility enables an easy upgrade path for improved SDI cable reach performance. A summary of pinout differences is shown in 図 7-1.

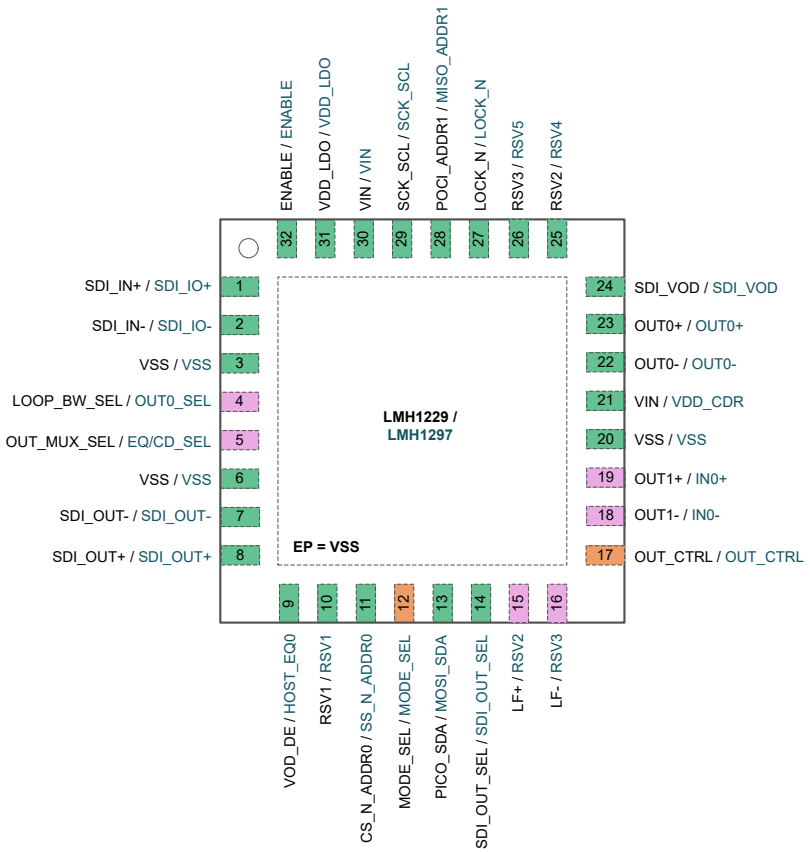


図 7-1. LMH1219 vs. LMH1297 Pinout Differences

Legend
No special provisions needed
Minor pin setting differences
Major pin setting and definition differences

For a detailed comparison of device pin functionality, refer to 表 7-1.

表 7-1. LMH1229 vs. LMH1297 (EQ Mode) Pin-to-Pin Comparison

PIN NO.	LMH1229	LMH1297	DIFFERENCE SUMMARY(1)
1	SDI_IN+	SDI_IO+	None
2	SDI_IN-	SDI_IO-	
8	SDI_OUT+	SDI_OUT+	None
7	SDI_OUT-	SDI_OUT-	
23	OUT0+	OUT0+	None
22	OUT0-	OUT0-	
19	OUT1+	IN0+	LMH1229: Secondary 100Ω PCB output. LMH1297: Don't care. Pins are unused in EQ mode. For pin compatible functionality: Leave floating.
18	OUT1-	IN0-	
4	LOOP_BW_SEL	OUT0_SEL	LMH1229: 4-level CDR loop bandwidth control. LMH1297: Don't care. OUT0 always enabled in EQ mode. For pin compatible functionality: Leave floating (Level F).

表 7-1. LMH1229 vs. LMH1297 (EQ Mode) Pin-to-Pin Comparison (続き)

PIN NO.	LMH1229	LMH1297	DIFFERENCE SUMMARY(1)
5	OUT_MUX_SEL	EQ/CD_SEL	LMH1229: 4-level output mux select control. LMH1297: Tie low for EQ mode For pin compatible functionality: Tie low for 100Ω OUT0 PCB output only.
9	VOD_DE	HOST_EQ0	None
12	MODE_SEL	MODE_SEL	LMH1229: Level H forces Power save mode (SPI enabled). LMH1297: Level H reserved. For pin compatible functionality: Use Levels F, R, or L only.
14	SDI_OUT_SEL	SDI_OUT_SEL	None
15	LF+	RSV2	LMH1229: Optional external loop filter cap (do not connect for default operation). LMH1297: Reserved (do not connect). For pin compatible functionality: Leave floating.
16	LF-	RSV3	
17	OUT_CTRL	OUT_CTRL	LMH1229: Selects bypass mode operation for OUT0, OUT1, and SDI_OUT. LMH1297: Selects bypass mode operation for OUT0 only For pin compatible functionality: Leave floating (Level F).
24	SDI_VOD	SDI_VOD	None
27	LOCK_N	LOCK_N	None
32	ENABLE	ENABLE	None
11	CS_N_ADDR0	SS_N_ADDR0	None Note: There are differences in LMH1229 vs. LMH1297 SMBus mode device addresses.
28	POCI_ADDR1	MISO_ADDR1	None Note: There are differences in LMH1229 vs. LMH1297 SMBus mode device addresses.
13	PICO_SDA	MOSI_SDA	None
29	SCK_SCL	SCK_SCL	None
10	RSV1	RSV1	None
25	RSV2	RSV4	None
26	RSV3	RSV5	None
3, 6, 20	VSS	VSS	None
30	VIN	VIN	None
21	VIN	VDD_CDR	None. Connect to same supply as Pin 30 (VIN) externally.

(1) In the difference summary, LMH1297 is assumed to be operating in EQ mode.

7.2 Typical Application

The LMH12x9 is a long-reach cable equalizer with integrated reclocker that supports SDI data rates up to 11.88Gbps.

This device supports multiple configurations and can be used either as a pin-compatible upgrade to the previous generation LMH1297 in EQ mode (LMH1229) or a robust cable equalizer with redundant SDI inputs (LMH1239). 図 7-2 shows a typical application circuit for the LMH1229.

Specific examples of typical applications for the LMH12x9 are detailed in the following subsections.

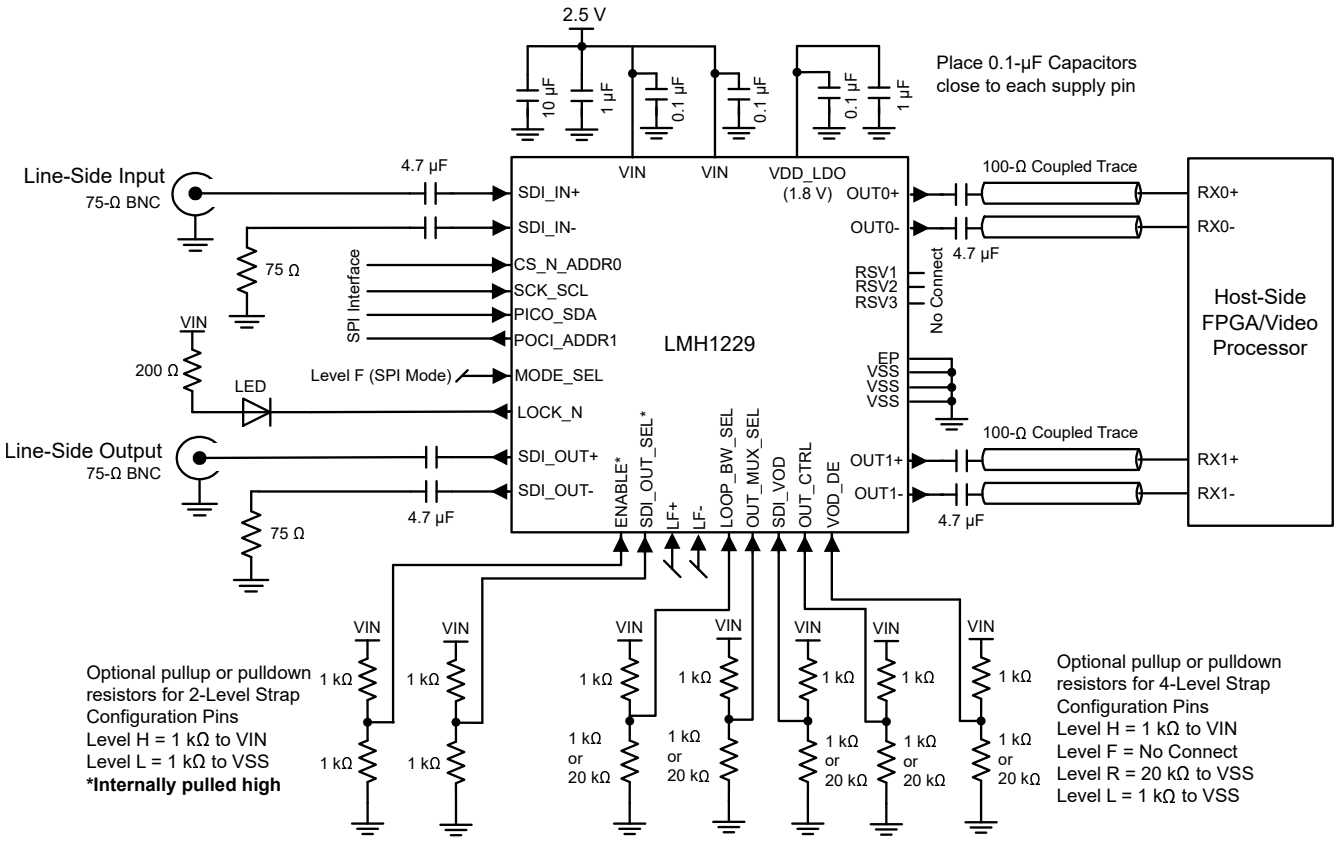


図 7-2. LMH12x9 SPI mode Connection Diagram

7.2.1 Cable Equalizer With Loop-Through

The LMH12x9 can be configured as a cable equalizer with loop-through output. The LMH12x9 takes in SDI data at the SDI_IN adaptive cable equalizer input and outputs the reclocked SDI signal at OUT0 (primary output) and OUT1 (optional secondary output). Meanwhile, a redundant reclocked loop-through SDI signal is output on SDI_OUT for system monitoring or cascade purposes.

図 7-3 shows a typical application of an LMH12x9 as a cable loop-through device. In this example, the LMH12x9 provides an SDI signal to the SDI FPGA on both OUT0 and OUT1. Concurrently, the equalized and reclocked SDI_IN signal is sent to the loop-through SDI_OUT cable driver output. Meanwhile, the FPGA sends post-processed SDI data out on an LMH1228 dual cable driver with integrated reclocker.

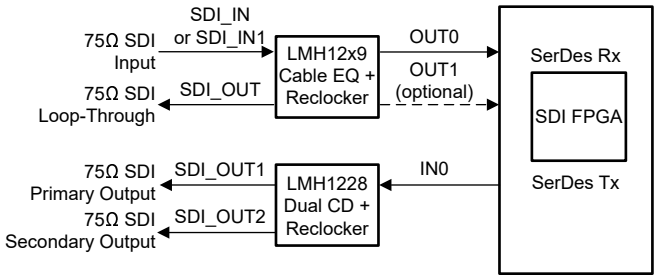


図 7-3. LMH12x9 Cable Loop-Through Application

7.2.1.1 Design Requirements

For general LMH12x9 design requirements, reference the guidelines in 表 7-2.

For cable equalizer with loop-through application-specific requirements, reference the guidelines in 表 7-3.

表 7-2. General Design Requirements

DESIGN PARAMETER	REQUIREMENTS
SDI_IN+, SDI_IN1+ (LMH1239 only), SDI_OUT+ AC-coupling capacitors	4.7µF 0402 surface mount ceramic capacitors recommended.
SDI_IO–, SDI_IN1– (LMH1239 only), SDI_OUT– AC-coupling capacitors	4.7µF 0402 surface mount ceramic capacitors recommended, AC terminated with 75Ω to VSS. Negative polarity can be used if positive polarity is AC terminated with 75Ω to VSS.
OUT0± and OUT1± AC-coupling capacitors	4.7µF 0402 surface mount ceramic capacitors recommended.
Input and output terminations	Input and output terminations provided internally. Do **not** add external terminations.
High-speed OUT0± and OUT1± trace impedance	Route the OUT0± and OUT1± with coupled board traces and100Ω differential impedance.
SMPTE return loss	Place BNC within 1 inch of the LMH12x9 and consult BNC vendor for recommended BNC landing pattern to meet SMPTE requirements.
SDI_IN+ and SDI_OUT+ crosstalk	When a long length coax cable is connected to SDI_IN+, the signal amplitude at SDI_IN+ can be just a few mVpp. Layout precautions must be taken to minimize crosstalk from adjacent devices or from adjacent output port SDI_OUT+. To reduce cross coupling effects, keep SDI_OUT+ traces as far from SDI_IN+ as possible. When SDI_OUT+ is not used, TI recommends to turn off the output (SDI_OUT_SEL = H) for best results. Note: When using the LMH1239, the same design requirements are applicable for SDI_IN1+ and SDI_OUT+ too.
DC power supply decoupling capacitors	10µF and 1µF bulk capacitors: place close to each device. 0.1µF capacitor: place close to each supply pin.
VDD_LDO decoupling capacitors	1µF and 0.1µF capacitors: place as close as possible to the device VDD_LDO pin. Do **not** use VDD_LDO as a 1.8V power supply source to external components.
MODE_SEL Pin	SPI: Leave MODE_SEL unconnected (Level F) SMBus: Connect 1kΩ to VSS (Level L)

表 7-2. General Design Requirements (続き)

DESIGN PARAMETER	REQUIREMENTS
Input SDI Reclocked Data Rate	11.88Gbps, 5.94Gbps, 2.97Gbps, 1.485Gbps, or Divide-by-1.001 sub-rates and 270Mbps. For all other input data rates, the reclocker is automatically bypassed.

表 7-3. Cable Equalizer with Loop-Through Requirements

DESIGN PARAMETER	REQUIREMENTS
OUT_MUX_SEL Pin	1kΩ to VSS (Level L) or float (Level F) to enable OUT0± only. 20kΩ to VSS (Level R) to enable both OUT0± and OUT1±.
LOOP_BW_SEL Pin	1kΩ to VIN (Level H) or float (Level F) for default CDR loop bandwidth operation (no external capacitor on LF±). 20kΩ to VSS (Level R) or 1kΩ to VSS (Level L) for decreased loop bandwidth (external capacitor required on LF±).
SDI_OUT_SEL Pin	1 kΩ to VSS (Level L) to enable cable loop-through SDI_OUT. 1 kΩ to VIN (Level H) to disable cable loop-through SDI_OUT.

7.2.1.2 Detailed Design Procedure

The design procedure for cable equalizer with loop-through applications is as follows:

1. Select a power supply that meets the DC and AC requirements in *Recommended Operating Conditions*.
2. Choose small 0402 surface mount ceramic capacitors for AC-coupling capacitors to maintain characteristic impedance.
3. Choose a high-quality, 75Ω BNC connector that is capable of supporting 11.88Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended footprint for meeting SMPTE return loss.
4. Follow detailed high-speed layout recommendations provided in *Layout Guidelines* to ensure optimal signal quality when interconnecting 75Ω and 100Ω signals to the LMH12x9.
5. Determine whether SPI or SMBus communication is necessary. If the LMH12x9 must be programmed with settings other than what is offered by pin control, users must use SPI or SMBus mode for additional programming.
6. Configure all two-level and four-level pins according to the desired use case. Note that pin settings can be overridden by register control.
7. Tune the VOD_DE 100Ω driver control pin to equalize the PCB output trace following OUT0± and OUT1± (if used). Use register control for more tuning options if necessary.
8. If SDI_OUT is used for diagnostic or cascade applications, tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_OUT+. Use register control for more tuning options if necessary.

7.2.1.3 Application Curves

The LMH12x9 output eye performance was measured with the test setups shown in 図 7-4 and 図 7-5.

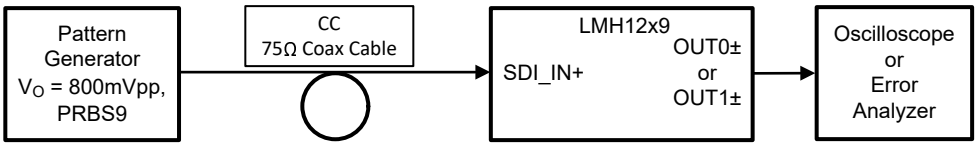


図 7-4. Test Setup for LMH12x9 PCB Output (OUT0±, OUT1±)

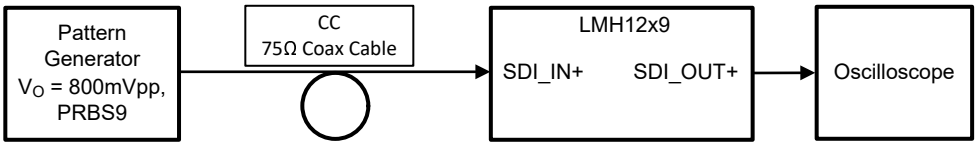


図 7-5. Test Setup for LMH12x9 Loop-Through (SDI_OUT+)

The eye diagrams measured on the LMH1239EVM in this subsection show the LMH12x9 100Ω differential PCB output at OUT0± and OUT1± (図 7-7 - 図 7-8) and LMH12x9 75Ω loop-through cable output at SDI_OUT+ (図 7-9).

Additionally, LMH12x9 BER (bit error rate) performance was measured with the test setup shown in 図 7-6. Phabrix Qx BER results on the LMH1239EVM are shown in 図 7-10.

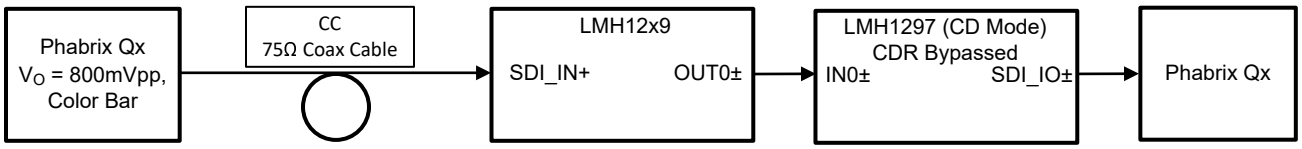
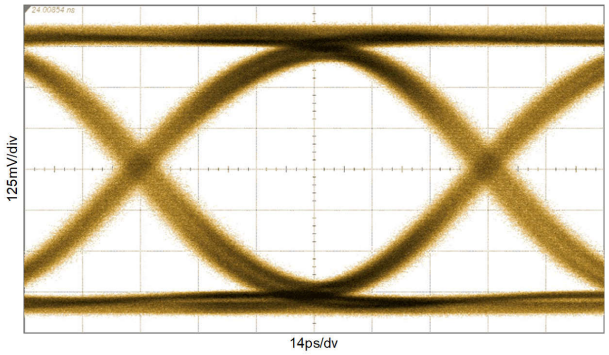
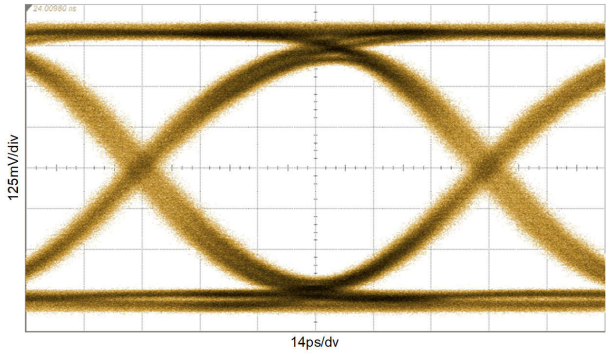


図 7-6. Test Setup for LMH12x9 BER Performance (OUT0±)



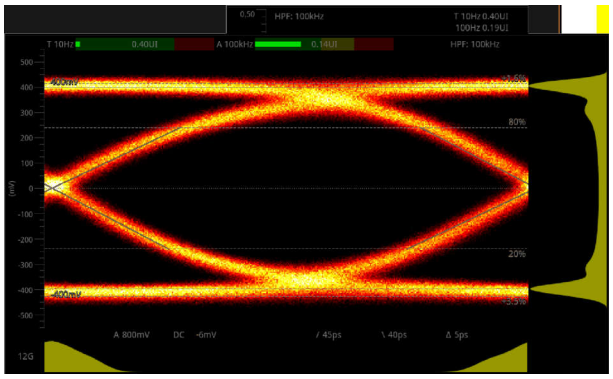
VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-7. OUT0± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A, Reclocked



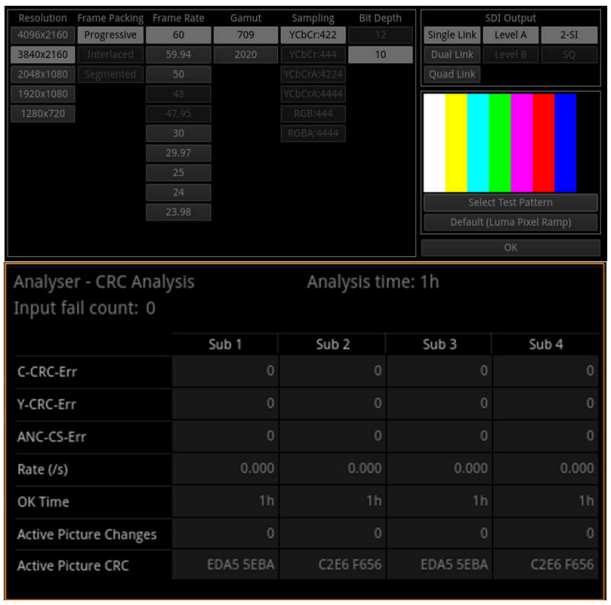
VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-8. OUT1± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A, Reclocked



VOD_DE = F, SDI_OUT_SEL = L, OUT_CTRL = F

図 7-9. SDI_OUT+ at 11.88Gbps (12G-SDI), CC = 90m Belden 1694A, Reclocked



VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-10. OUT0± BER at 11.88Gbps (12G-SDI), CC = 100m Belden 1694A, Reclocked

7.2.2 Cable Equalizer With Redundant SDI Input (LMH1239 only)

The LMH1239 can be configured as a cable equalizer with redundant SDI input for applications requiring system robustness and routing flexibility. The SDI input data is selected from either SDI_IN or SDI_IN1 by the 2:1 input mux. The chosen SDI input is then fed through the adaptive cable equalizer, and the reclocked SDI signal is output on OUT0 (primary output) and OUT1 (optional secondary output). Meanwhile, a redundant reclocked loop-through SDI signal is output on SDI_OUT for system monitoring or cascade purposes.

図 7-11 shows a typical application of a LMH1239 with redundant SDI input. In this example, the LMH1239 selects between a primary BNC input (SDI_IN) and a back-up BNC input (SDI_IN1). In this use case, SDI_IN1 is only used if issues are found at SDI_IN. The LMH1239 provides an SDI signal to the SDI FPGA on both OUT0 and OUT1.

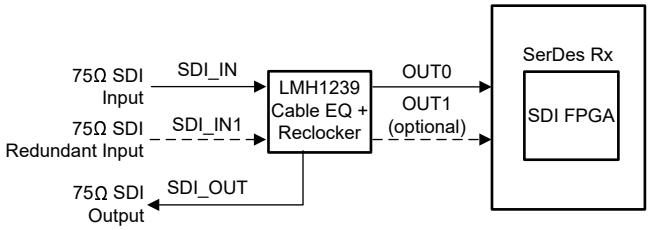


図 7-11. LMH1239 Cable Equalizer with Redundant SDI Input Application

7.2.2.1 Design Requirements

See *Design Requirements* for general LMH12x9 design requirements.

For LMH1239 cable equalizer with redundant SDI input application-specific requirements, reference the guidelines in 表 7-4.

表 7-4. LMH1239 Cable Equalizer with Redundant SDI Input Requirements

DESIGN PARAMETER	REQUIREMENTS
IN_MUX_SEL Pin	1kΩ to VIN (Level H) or leave floating (Level F) to select SDI_IN 20kΩ or 1kΩ to VSS (Level R, L) to select SDI_IN1

7.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure* and follow all steps. Refer to additional steps below for redundant SDI input applications.

1. Determine the desired primary and secondary SDI input. For additional immunity in cable loop-through applications (SDI_OUT_SEL = L), SDI_IN1 is recommended as the primary to maximize physical isolation (and minimize degradation from crosstalk) between SDI input and SDI output (SDI_OUT).
2. Configure IN_MUX_SEL 4-level input according to the desired SDI input.

7.2.2.3 Application Curves

The LMH1239 output eye performance was measured with the test setup shown in 図 7-12.

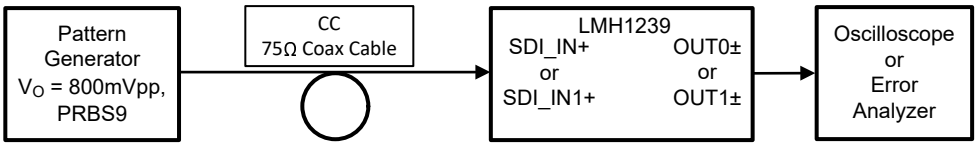


図 7-12. Test Setup for LMH1239 PCB Output with Redundant SDI Input

The eye diagrams measured on the LMH1239EVM in this subsection show the LMH1239 100Ω differential PCB output at OUT0± and OUT1± (図 7-14 - 図 7-17).

Additionally, LMH1239 BER (bit error rate) performance was measured with the test setup shown in 図 7-13. Phabrix Qx BER results on the LMH1239EVM are shown in 図 7-18 and 図 7-19.

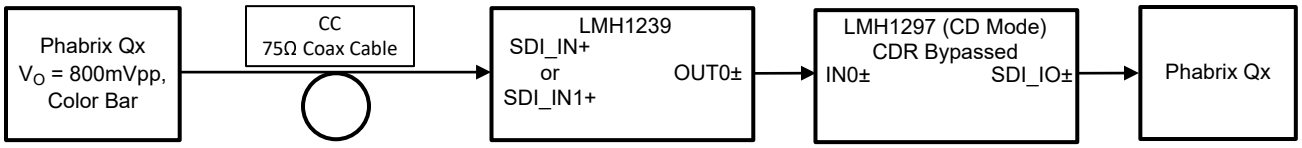
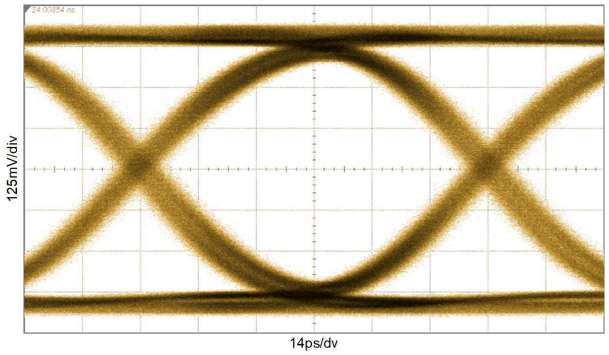
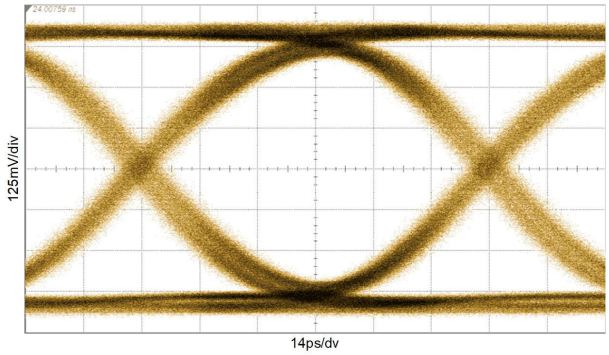


図 7-13. Test Setup for LMH1239 BER Performance (OUT0±) with Redundant SDI Input



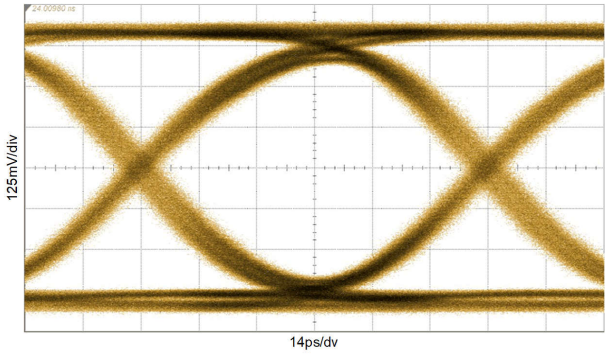
IN_MUX_SEL = F, VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-14. OUT0± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A at SDI_IN+, Reclocked



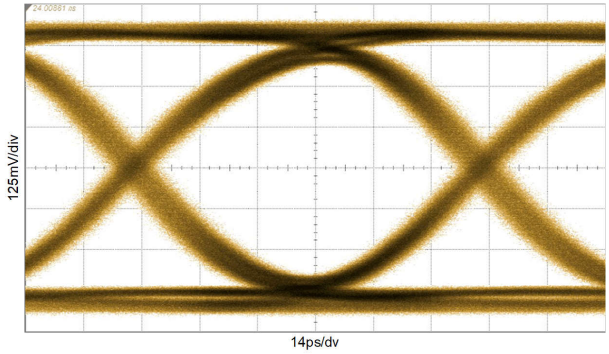
IN_MUX_SEL = L, VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-15. OUT0± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A at SDI_IN1+, Reclocked



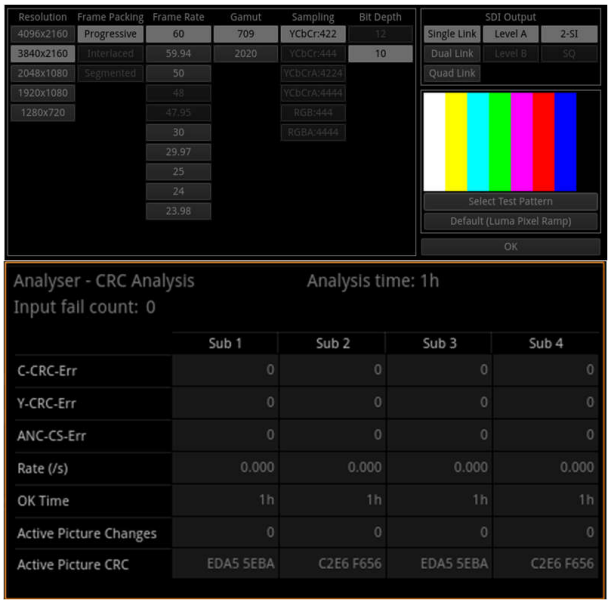
IN_MUX_SEL = F, VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-16. OUT1± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A at SDI_IN+, Reclocked



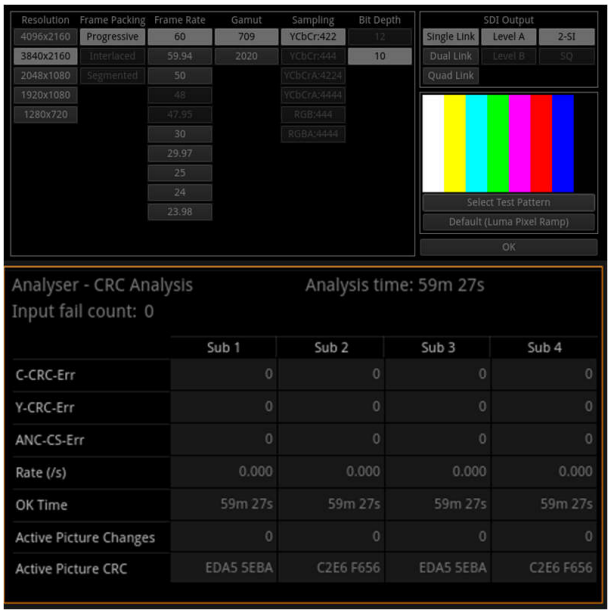
IN_MUX_SEL = L, VOD_DE = F, SDI_OUT_SEL = H, OUT_CTRL = F

図 7-17. OUT1± at 11.88 Gbps (12G-SDI), CC = 100m Belden 1694A at SDI_IN1+, Reclocked



IN_MUX_SEL = F (SDI_IN selected), VOD_DE = F,
SDI_OUT_SEL = H, OUT_CTRL = F

図 7-18. OUT0± BER at 11.88Gbps (12G-SDI), CC = 100m Belden 1694A, Reclocked



IN_MUX_SEL = L (SDI_IN1 selected), VOD_DE = F,
SDI_OUT_SEL = H, OUT_CTRL = F

図 7-19. OUT0± BER at 11.88Gbps (12G-SDI), CC = 100m Belden 1694A, Reclocked

7.3 Power Supply Recommendations

The LMH12x9 requires decoupling capacitors to ensure a stable power supply. For power supply decoupling, 0.1µF surface-mount ceramic capacitors must be placed close to each VDD_LDO and VIN supply pin to VSS. Larger bulk capacitors (for example, 10µF and 1µF) are recommended for VIN.

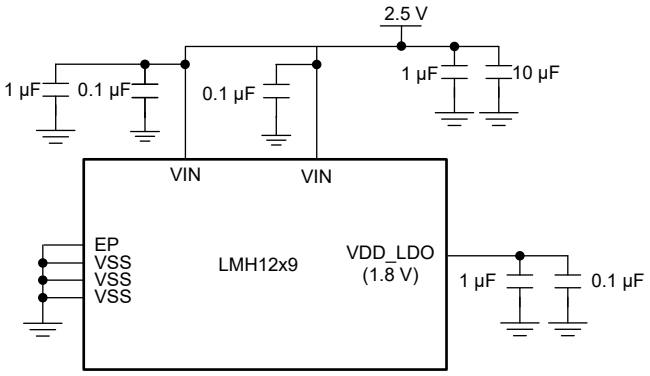


図 7-20. Recommended Power Supply Decoupling

Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2mil to 4mil dielectric in a printed circuit board.

7.4 Layout

7.4.1 Layout Guidelines

The following guidelines are recommended to optimize the board layout for the LMH12x9.

7.4.1.1 Board Stack-Up and Ground References

- Choose a suitable board stack-up that supports 75Ω single-ended trace and 100Ω differential trace routing on the top layer of the board. This is typically done with a Layer 2 ground plane reference for the 100Ω differential traces and a Layer 3 ground plane reference for the 75Ω single-end traces.
- Maintain a distance of at least 5 times the trace width between signal trace and ground reference if the signal trace and ground are on the same layer. This prevents unwanted changes in the characteristic impedance.
- Maintain a consistent ground plane reference for each high-speed trace from source to endpoint. Ground reference discontinuities lead to characteristic impedance mismatch.

7.4.1.2 High-Speed PCB Trace Routing and Coupling

Observe the following general high-speed recommendations for high-speed trace routing:

- For differential pairs, maintain a uniform width and gap for each differential pair where possible. When traces must diverge (for example, due to AC-coupling capacitors), ensure that the traces branch out or merge uniformly.
- To prevent reflections due to trace routing, ensure that trace bends are at most 45°. Implement right angle bends with at least two 45° corners. Radial bends are ideal.
- Avoid using signal vias. If signal vias must be used, a return path (GND) via must be placed near the signal via to provide a consistent ground reference and minimize impedance discontinuities.
- Avoid via stubs by back-drilling as necessary.

7.4.1.2.1 SDI_IN± and SDI_OUT±:

- Use an uncoupled trace with 75Ω single-ended impedance for signal routing to SDI_IN± and SDI_OUT±.
- The trace width is typically 8-10 mils with reference to a Layer-3 ground plane.
- The same layout guidelines are relevant to SDI_IN1± when using the LMH1239.

7.4.1.2.2 OUT0± and OUT1±:

- Use coupled traces with 100Ω differential impedance for signal routing to OUT0± and OUT1±.
- The trace width is typically 5-8 mils with reference to a Layer-2 ground plane.

7.4.1.3 Anti-Pads

- Place anti-pads (ground relief) on the power and ground planes directly under the 4.7µF, AC-coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad and the number of layers to use the anti-pad depend on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.

7.4.1.4 BNC Connector Layout and Routing

- Use a well-designed BNC footprint to ensure the signal landing pad of the BNC achieves 75Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
- Keep trace length short between the BNC and SDI_IN±. Keep the trace routing for SDI_IN+ and SDI_IN– as symmetrical as possible, with approximately equal lengths and equal loading. The same is true for SDI_OUT+ and SDI_OUT–.
- The same layout guidelines are relevant to SDI_IN1± when using the LMH1239.

7.4.1.5 Power Supply and Ground Connections

- Connect each supply pin (VIN, VDD_LDO) directly to the power or ground planes with a short via. The via is usually placed tangent to the landing pads of the supply pins with the shortest trace possible.
- Make sure the power supply decoupling capacitors are a small physical size (0402 or smaller) and placed close to the supply pins to minimize inductance. The capacitors are commonly placed on the bottom layer and share the ground of the EP (Exposed Pad).

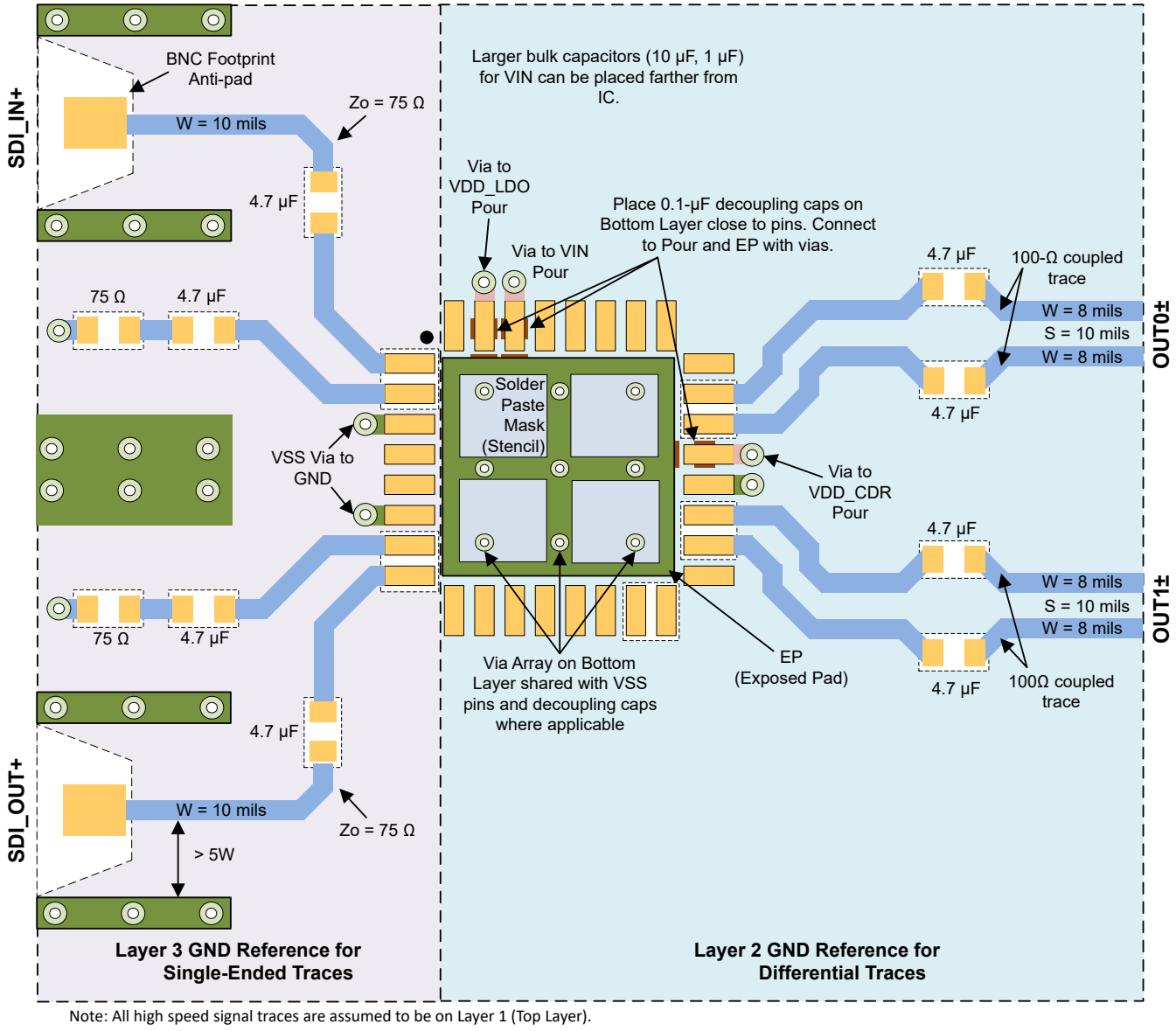
7.4.1.6 Footprint Recommendations

- Stencil parameters for the EP (Exposed Pad) such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the QFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder can flow unevenly through the EP. Stencil parameters for aperture opening and via locations are shown in the RTV package drawing in the *Mechanical, Packaging, and Orderable Information*.
- The EP of the package must be connected to the ground plane through a 3 × 3 via array. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process. Details about via dimensions are also shown in the RTV package drawing in *Mechanical, Packaging, and Orderable Information*.

More information on the QFN style package is provided in *QFN/SON PCB Attachment* application note.

7.4.2 Layout Example

The example shown in 図 7-21 demonstrates the layout guidelines highlighted in *Layout Guidelines* for the LMH1229. For layouts with the LMH1239, the same layout guidelines that apply to SDI_IN+ are applicable to SDI_IN1+. Refer to the LMH1239EVM User's Guide for more details.



Note: All high speed signal traces are assumed to be on Layer 1 (Top Layer).

図 7-21. LMH12x9 High-Speed Trace Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *A Study of the SDI Pathological Data Pattern* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision * (June 2024) to Revision A (October 2024)	Page
• データシートのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1229RTVR	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1229	Samples
LMH1229RTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1229	Samples
LMH1239RTVR	ACTIVE	WQFN	RTV	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1239	Samples
LMH1239RTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1239	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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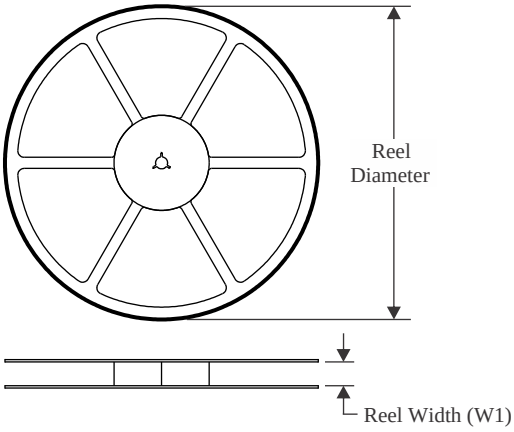
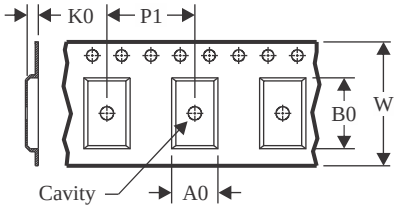
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

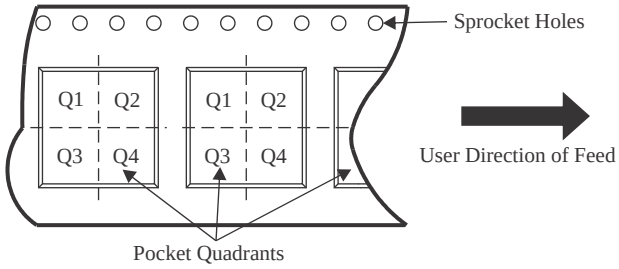


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

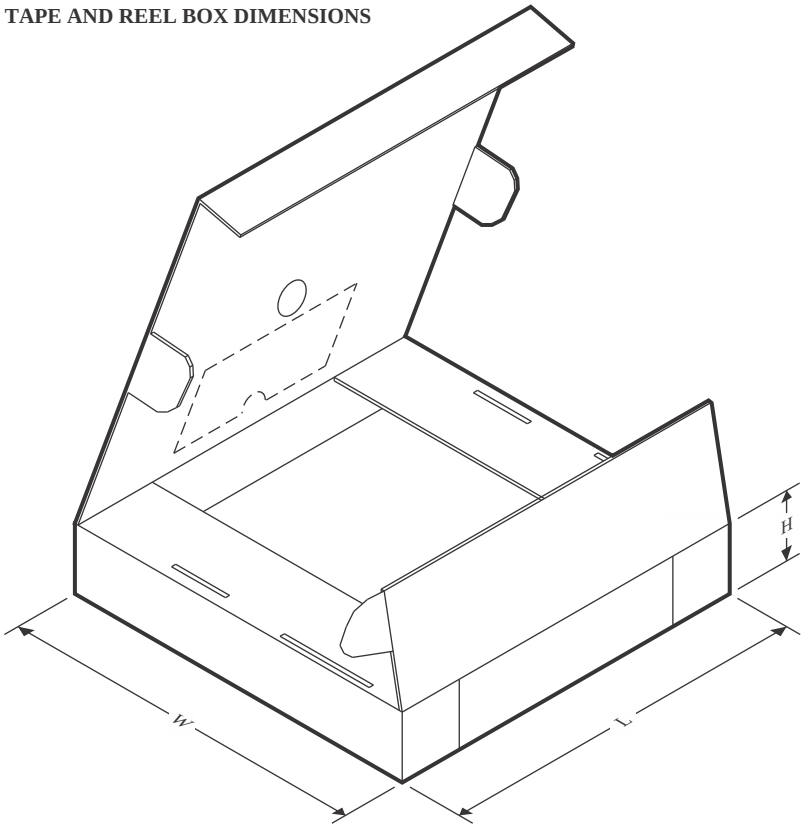
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1229RTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1229RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1239RTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1239RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

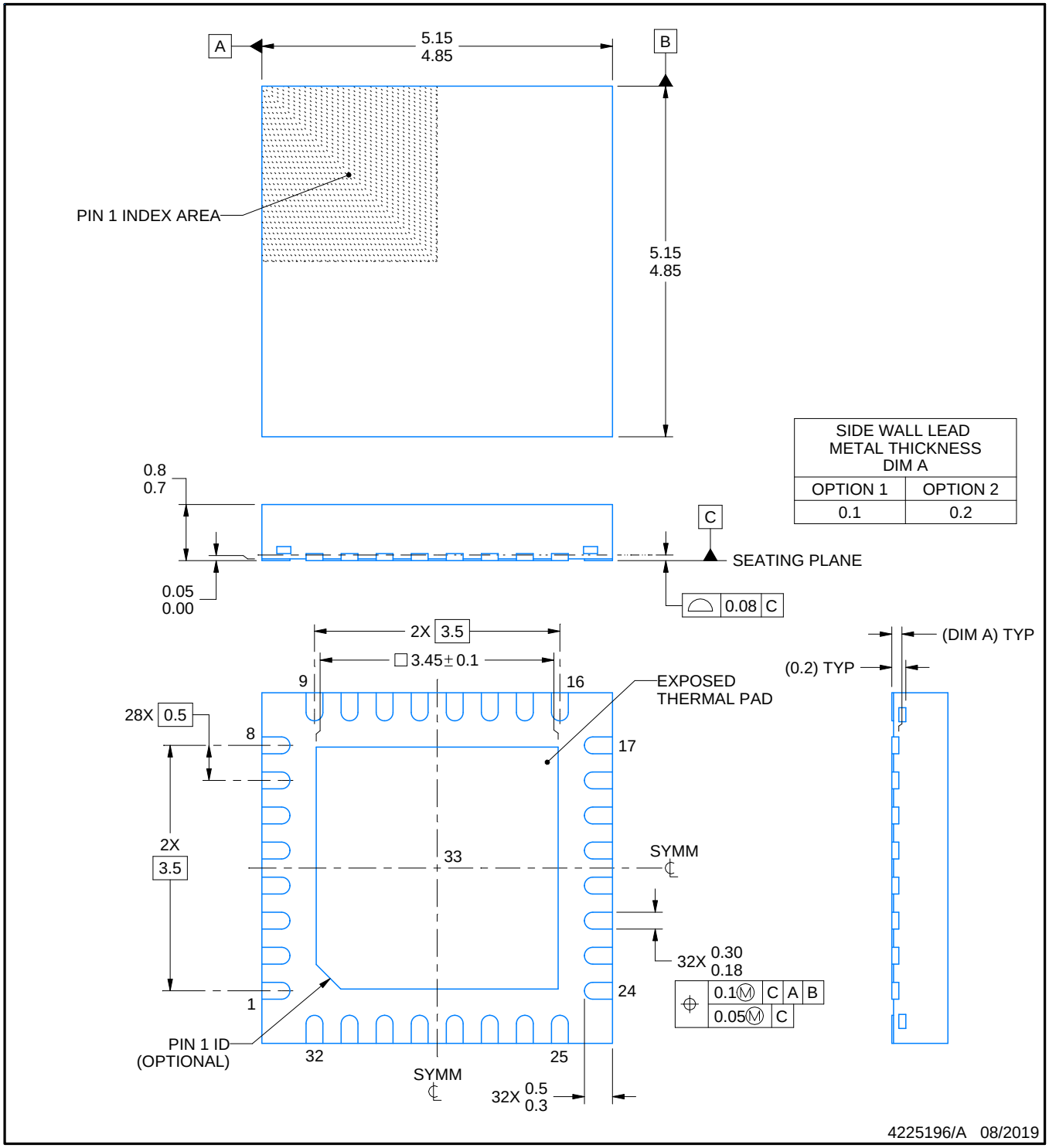
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1229RTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
LMH1229RTVT	WQFN	RTV	32	250	210.0	185.0	35.0
LMH1239RTVR	WQFN	RTV	32	3000	367.0	367.0	35.0
LMH1239RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

RTV0032E

PACKAGE OUTLINE

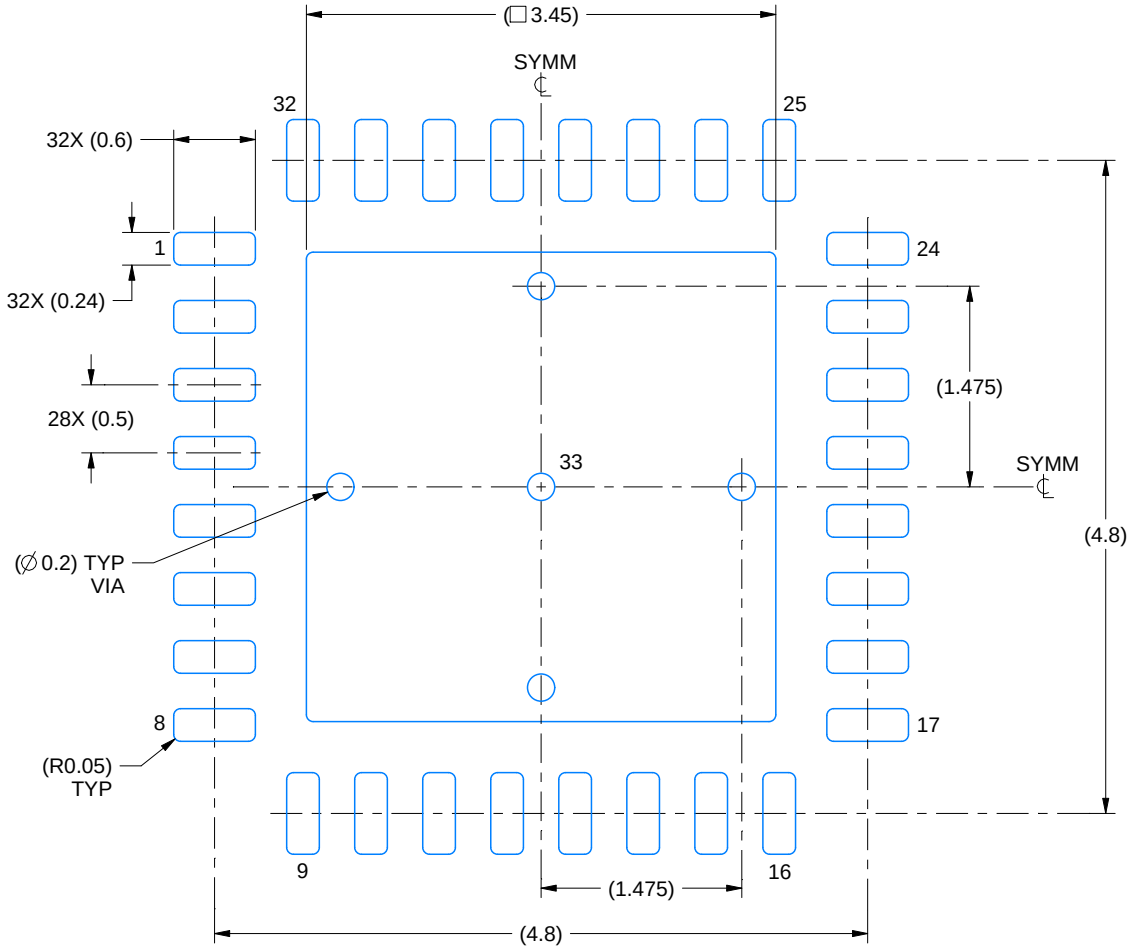
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

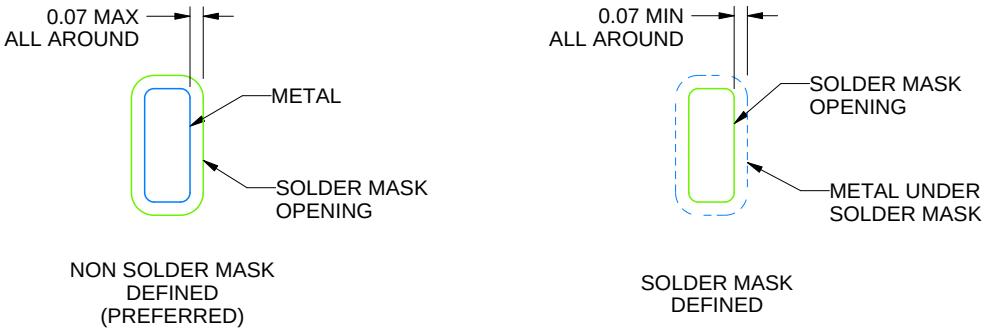


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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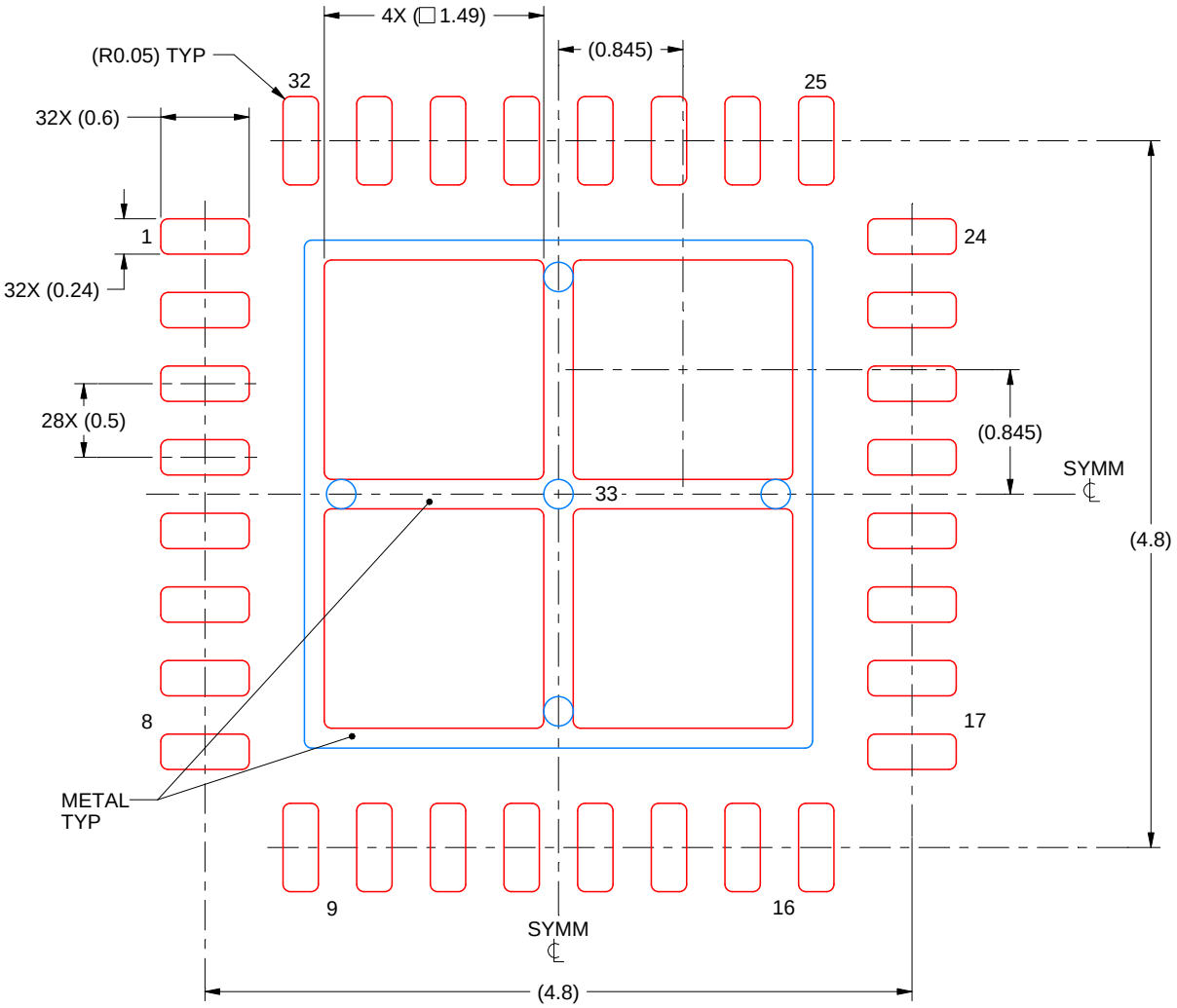
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225196/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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