

LMK62XX 高性能低ジッタ発振器

1 特長

- 低ノイズ、高性能
 - ジッタ: 150fs RMS (標準値)、 $F_{out} > 100\text{MHz}$
 - PSRR: -60dBc、堅牢な電源ノイズ耐性
- 対応出力フォーマット:
 - LVPECL、LVDS、HCSL (最大 400MHz)
- 合計周波数許容値: $\pm 50\text{ppm}$ (LMK62X2) および $\pm 25\text{ppm}$ (LMK62X0)
- 動作電圧: 3.3V
- 産業用温度範囲: $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$
- 5mm × 3.2mm の 6 ピンパッケージ、業界標準の 5032 XO パッケージとピン互換

2 アプリケーション

- 水晶振動子、SAW、またはシリコン ベースの発振器に代わる高性能の代替品
- スイッチ、ルータ、ネットワークライン カード、ベースバンド ユニット (BBU)、サーバ、ストレージ / SAN
- テストおよび測定
- 医療用画像処理
- FPGA、プロセッサ接続

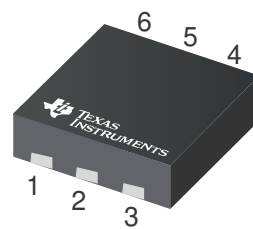
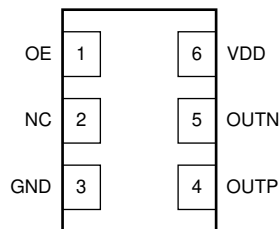
3 概要

LMK62XX デバイスは低ジッタの発振器で、一般的に使用されるリファレンス・クロックを生成します。このデバイスは、任意のリファレンス・クロック周波数をサポートするよう工場であらかじめプログラムされ、出力フォーマットとして LVPECL、LVDS、HCSL で最大 400MHz をサポートします。内部的な電力コンディショニングにより、電源リップル除去 (PSRR) が非常に優れているため、電力供給ネットワークのコストと複雑性を減らすことができます。単一の $3.3\text{V} \pm 5\%$ 電源で動作します。

製品情報

| 部品番号 | 出力周波数 (MHz) とフォーマット | 総合周波数安定性 (ppm) | パッケージ サイズ (1) (2) |
|--------------|---------------------|----------------|---------------------------------|
| LMK62E2-100M | 100 LVPECL | ± 50 | SIA (QFM, 6) 5.00mm × 3.20mm |
| LMK62E2-156M | 156.25 LVPECL | ± 50 | |
| LMK62E0-156M | 156.25 LVPECL | ± 25 | |
| LMK62A2-100M | 100 LVDS | ± 50 | |
| LMK62A2-150M | 150 LVDS | ± 50 | |
| LMK62A2-156M | 156.25 LVDS | ± 50 | |
| LMK62A2-200M | 200 LVDS | ± 50 | |
| LMK62A2-266M | 266.66 LVDS | ± 50 | |
| LMK62I0-100M | 100 HCSL | ± 25 | |
| LMK62I0-156M | 156.25 HCSL | ± 25 | |

- 供給されているすべてのパッケージについては、[セクション 10](#) を参照してください。
- パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



ピン配置



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4 Pin Configuration and Functions

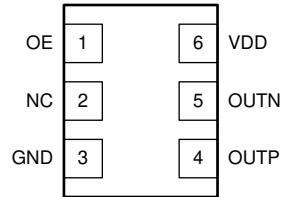


図 4-1. SIA Package 6-pin QFM Top View

表 4-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------------------------------|-----|-----------|--|
| NAME | NO. | | |
| POWER | | | |
| GND | 3 | Ground | Device ground |
| VDD | 6 | Analog | 3.3-V power supply |
| OUTPUT BLOCK | | | |
| OUTP | 4 | Universal | Differential output pair (LVPECL, LVDS or HCSL). |
| OUTN | 5 | | |
| DIGITAL CONTROL / INTERFACES | | | |
| NC | 2 | N/A | No connect |
| OE | 1 | LVC MOS | Output enable (internal pulldown). When set to low, output pair is disabled and set at high impedance. The recommended external pullup resistor value is 10 kΩ. |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|----------------------------------|------|-----------|------|
| VDD | Device supply voltage | -0.3 | 3.6 | V |
| V _{IN} | Output voltage for logic inputs | -0.3 | VDD + 0.3 | V |
| V _{OUT} | Output voltage for clock outputs | -0.3 | VDD + 0.3 | V |
| T _J | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature | -40 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|------------------------|-------|-----|-------|------|
| VDD | Device supply voltage | 3.135 | 3.3 | 3.465 | V |
| T _A | Ambient temperature | -40 | 25 | 85 | °C |
| T _J | Junction temperature | | | 105 | °C |
| t _{RAMP} | VDD power-up ramp time | 0.1 | | 100 | ms |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LMK62XX ⁽²⁾ ⁽³⁾ ⁽⁴⁾ | | UNIT |
|-------------------------------|--|--|--|------|
| | | SIA (QFM) | | |
| | | 6 PINS | | |
| | | Airflow (LFM) 0 | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 94.5 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 65.1 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 59 | | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 23.3 | | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 64.1 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal resistance is calculated on a 4-layer JEDEC board.
- (3) Connected to GND with 2 thermal vias (0.3-mm diameter).
- (4) ψ_{JB} (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

5.5 Electrical Characteristics - Power Supply

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-----------|--|-----------------------|-----|-----|------|----|
| IDD | Device current consumption | LVPECL ⁽²⁾ | | 95 | 110 | mA |
| | | LVDS | | 85 | 100 | |
| | | HCSL ⁽³⁾ | | 90 | 105 | |
| IDD-PD | Device current consumption when output is disabled | OE = GND | | 70 | mA | |

- (1) See [Parameter Measurement Information](#) for relevant test conditions.
- (2) On-chip power dissipation should exclude 40 mW, dissipated in the 150-Ω termination resistors, from total power dissipation.
- (3) Excludes load current.

5.6 LVPECL Output Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|----------------------|-----|------|------|
| f _{OUT} | Output frequency ⁽²⁾ | | | 400 | MHz |
| V _{OD} | Output voltage swing (V _{OH} - V _{OL}) ⁽²⁾ | 700 | 950 | 1200 | mV |
| V _{OUT, DIFF, PP} | Differential output peak-to-peak swing | 2 × V _{OD} | | | V |
| V _{OS} | Output common-mode voltage | VDD - 1.45 | | | V |
| t _R / t _F | Output rise/fall time (20% to 80%) ⁽³⁾ | | 260 | 350 | ps |
| ODC | Output duty cycle ⁽³⁾ | 45% | | 55% | |

- (1) See [Parameter Measurement Information](#) for relevant test conditions.
- (2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.

(3) Ensured by characterization.

5.7 LVDS Output Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|-----------------|----------------------|-----|-------|------|
| f _{OUT} | Output frequency ⁽¹⁾ | | | | 400 | MHz |
| V _{OD} | Output voltage swing (V _{OH} - V _{OL}) ⁽¹⁾ | | 300 | 390 | 480 | mV |
| V _{OUT, DIFF, PP} | Differential output peak-to-peak swing | | 2 x V _{OD} | | | V |
| V _{OS} | Output common-mode voltage | | 1.125 | 1.2 | 1.375 | V |
| t _R / t _F | Output rise/fall time (20% to 80%) ⁽²⁾ | | | 260 | 350 | ps |
| ODC | Output duty cycle ⁽²⁾ | | 45% | | 55% | |
| R _{OUT} | Differential output impedance | | | 107 | | Ω |

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.

(2) Ensured by characterization.

5.8 HCSL Output Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--|-----------------|------|-----|-----|------|
| f _{OUT} | Output frequency | | | | 400 | MHz |
| V _{OH} | Output high voltage | | 660 | | 900 | mV |
| V _{OL} | Output low voltage | | -100 | | 100 | mV |
| V _{CROSS} | Absolute crossing voltage ^{(2) (3)} | | 250 | | 475 | mV |
| V _{CROSS-DELTA} | Variation of V _{CROSS} ^{(2) (3)} | | 0 | | 140 | mV |
| dV/dt | Slew rate ⁽⁴⁾ | | 1 | | 3 | V/ns |
| ODC | Output duty cycle ⁽⁴⁾ | | 45% | | 55% | |

(1) See [Parameter Measurement Information](#) for relevant test conditions.

(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.

(3) Ensured by design.

(4) Ensured by characterization.

5.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------|-----------------------|-----|-----|-----|------|
| V _{IH} | Input high voltage | | 1.4 | | | V |
| V _{IL} | Input low voltage | | | | 0.6 | V |
| I _{IH} | Input high current | V _{IH} = VDD | -40 | | 40 | μA |
| I _{IL} | Input low current | V _{IL} = GND | -40 | | 40 | μA |
| C _{IN} | Input capacitance | | | 2 | | pF |

5.10 Frequency Tolerance Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| f _T Total frequency tolerance | LMK62X2: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C | -50 | | 50 | ppm |
| | LMK62X0: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C | -25 | | 25 | ppm |

(1) Ensured by characterization.

5.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-----|-----|------|
| V _{THRESH} Threshold voltage ⁽¹⁾ | | 2.85 | | 3 | V |
| V _{DROOP} Allowable voltage droop ⁽²⁾ | | | | 0.1 | V |
| t _{STARTUP} Start-up time ⁽¹⁾ | Time elapsed from VDD at 3.135 V to output enabled | | | 10 | ms |
| t _{OE-EN} Output enable time ⁽²⁾ | Time elapsed from OE at V _{IH} to output enabled | | | 50 | µs |
| t _{OE-DIS} Output disable time ⁽²⁾ | Time elapsed from OE at V _{IL} to output disabled | | | 50 | µs |

(1) Ensured by characterization.

(2) Ensured by design.

5.12 PSRR Characteristics

VDD = 3.3 V, T_A = 25°C⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------------------|-----|-----|-----|------|
| PSRR Spurs induced by 50-mV power supply ripple ⁽²⁾ at 156.25-MHz output, all output types | Sine wave at 50 kHz | | -60 | | dBc |
| | Sine wave at 100 kHz | | -60 | | |
| | Sine wave at 500 kHz | | -60 | | |
| | Sine wave at 1 MHz | | -60 | | |

(1) See [Parameter Measurement Information](#) for relevant test conditions.

(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin

(3) DJ_{SPUR} (ps, pk-pk) = $[2 \cdot 10 \cdot (SPUR/20) / (\pi \cdot f_{OUT})] \cdot 1e6$, where PSRR or SPUR in dBc and f_{OUT} in MHz.

5.13 PLL Clock Output Jitter Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C⁽¹⁾ (3)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|--------|
| RJ RMS phase jitter ⁽²⁾ (12 kHz – 20 MHz) | f _{OUT} ≥ 100 MHz, all output types | | 150 | 250 | fs RMS |

(1) See [Parameter Measurement Information](#) for relevant test conditions.

(2) Ensured by characterization.

(3) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

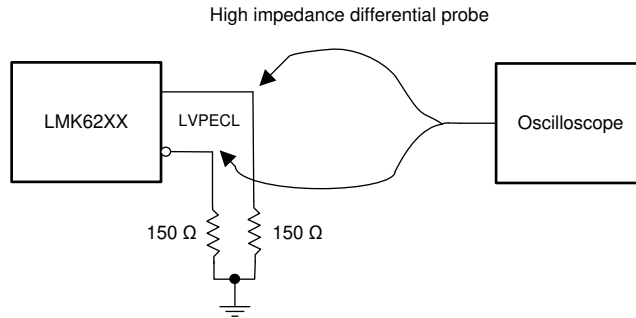


5.14 Additional Reliability and Qualification

| PARAMETER | CONDITION / TEST METHOD |
|----------------------------|-------------------------|
| Mechanical Shock | MIL-STD-202, Method 213 |
| Mechanical Vibration | MIL-STD-202, Method 204 |
| Moisture Sensitivity Level | J-STD-020, MSL3 |

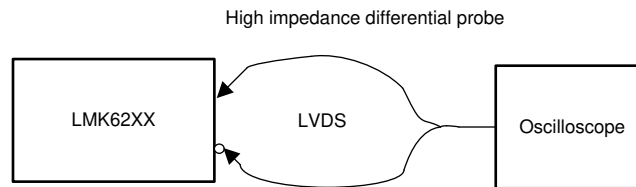
6 Parameter Measurement Information

6.1 Device Output Configurations



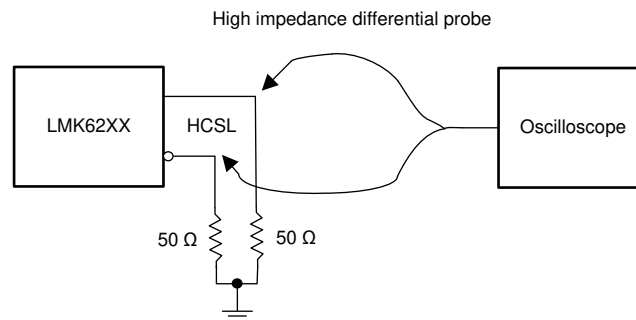
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图 6-1. LVPECL Output DC Configuration During Device Test



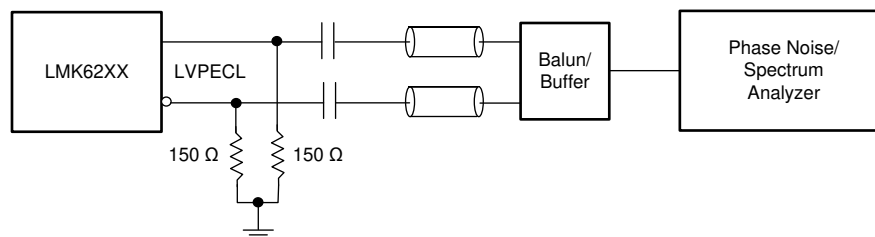
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图 6-2. LVDS Output DC Configuration During Device Test



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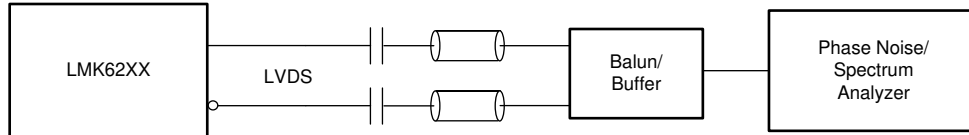
图 6-3. HCSL Output DC Configuration During Device Test ¹



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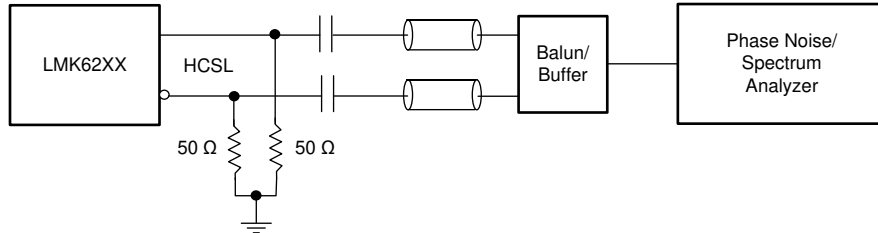
图 6-4. LVPECL Output AC Configuration During Device Test

¹ Also compatible with 85 Ω termination



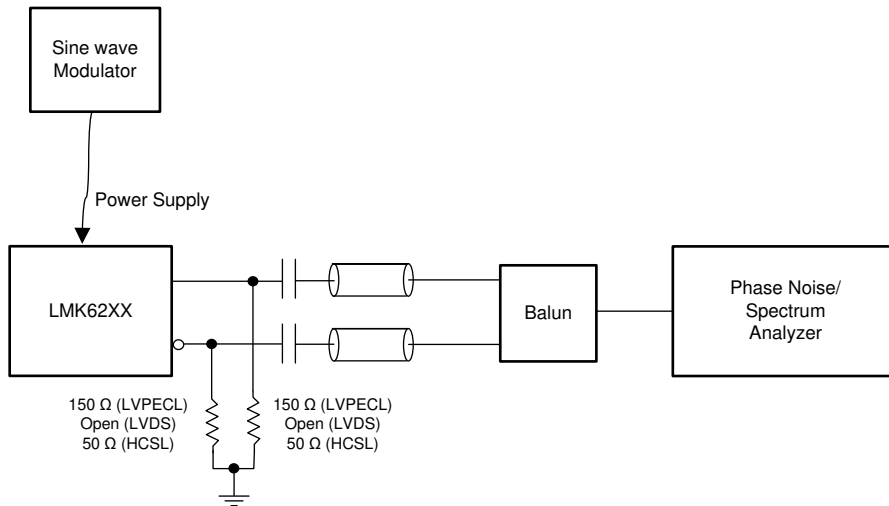
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6-5. LVDS Output AC Configuration During Device Test



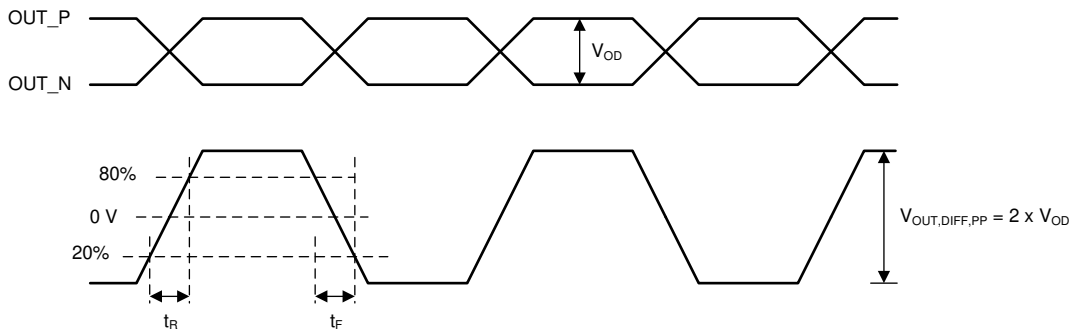
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6-6. HCSSL Output AC Configuration During Device Test



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6-7. PSRR Test Setup



6-8. Differential Output Voltage and Rise/Fall Time

7 Application and Implementation

注

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7.1 Power Supply Recommendations

For best electrical performance of LMK62XX, TI recommends using a combination of 10 μ F, 1 μ F, and 0.1 μ F on the power-supply bypass network of the device. TI also recommends using component side mounting of the power-supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. [図 7-1](#) shows the layout recommendation for power supply decoupling of LMK62XX.

7.2 Layout

7.2.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK62XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

7.2.1.1 Ensuring Thermal Reliability

The LMK62XX is a high-performance device. Therefore, pay careful attention to the device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in [図 7-1](#), to maximize thermal dissipation out of the package.

[式 1](#) shows the relationship between the PCB temperature around the LMK62XX and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

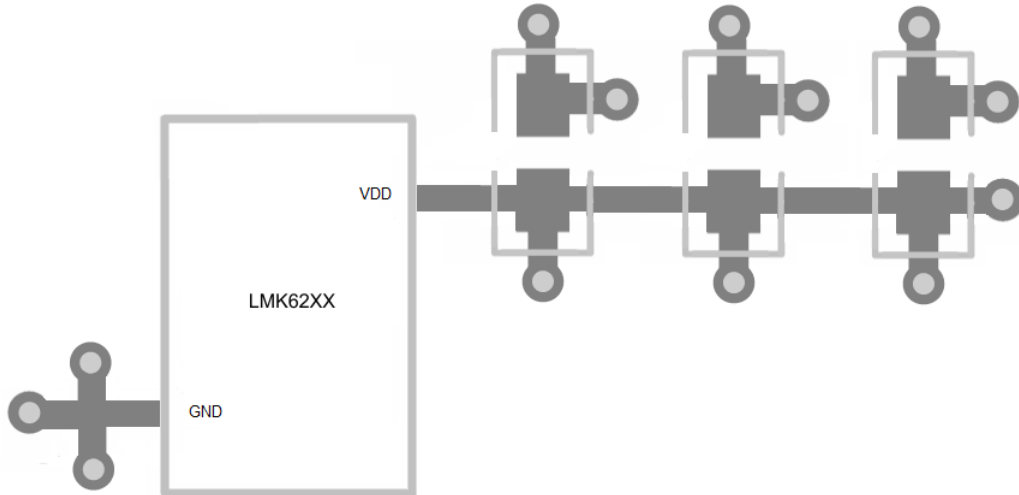
where

- T_B : PCB temperature around the LMK62XX
- T_J : Junction temperature of LMK62XX
- Ψ_{JB} : Junction-to-board thermal resistance parameter of LMK62XX (64.1°C/W without airflow)
- P: On-chip power dissipation of LMK62XX

To ensure that the maximum junction temperature of LMK62XX is below 105°C, it can be calculated that the maximum PCB temperature without airflow should be at 81°C or below when the device is optimized for best performance, resulting in maximum on-chip power dissipation of 0.36 W.

7.2.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK62XX, TI recommends routing vias into decoupling capacitors and then into the LMK62XX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. [図 7-1](#) shows the layout recommendation for LMK62XX.



7-1. LMK62XX Layout Recommendation for Power Supply and Ground

7.2.1.3 Recommended Solder Reflow Profile

TI recommends following the recommendations set by the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing LMK62XX with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferred. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well as the recommended soldering profile from the manufacturer, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

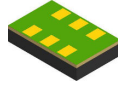
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision D (July 2018) to Revision E (December 2023) | Page |
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| 「製品情報」表を変更..... | 1 |
| Changed the OE pin description in the <i>Pin Functions</i> table..... | 3 |
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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

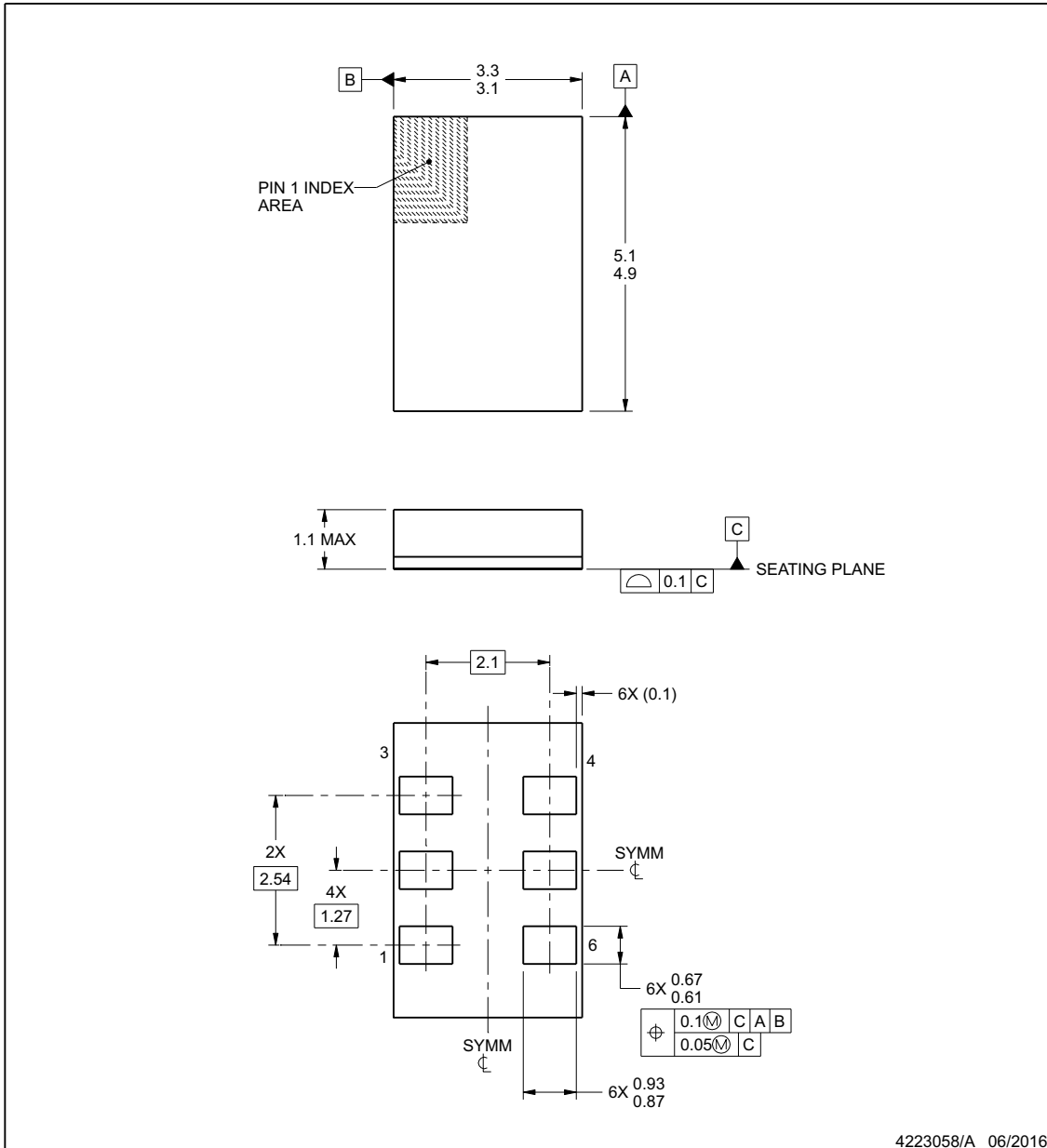


SIA0006B

PACKAGE OUTLINE

QFM - 1.1 mm max height

QUAD FLAT MODULE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

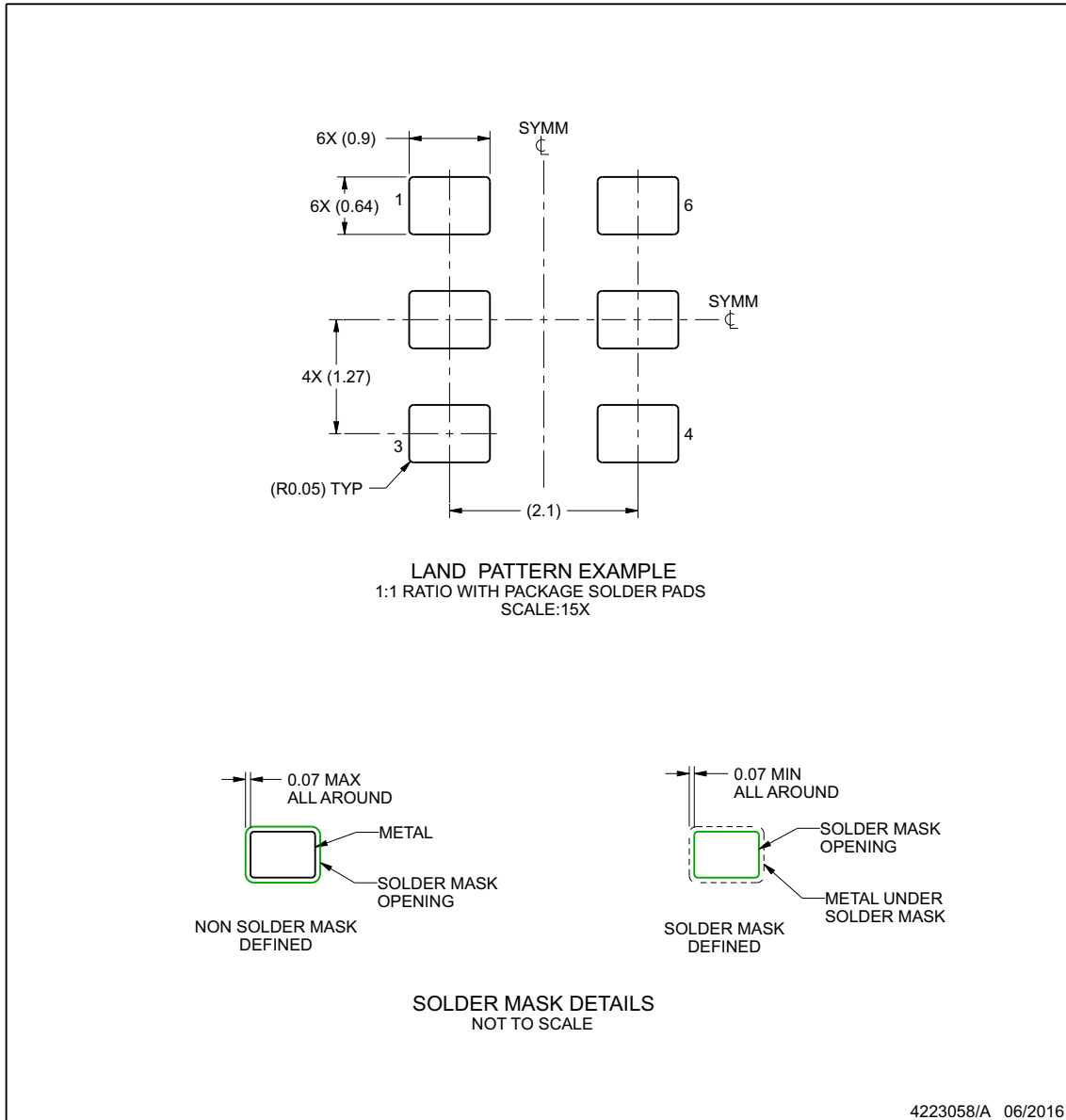
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EXAMPLE BOARD LAYOUT

SIA0006B

QFM - 1.1 mm max height

QUAD FLAT MODULE



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

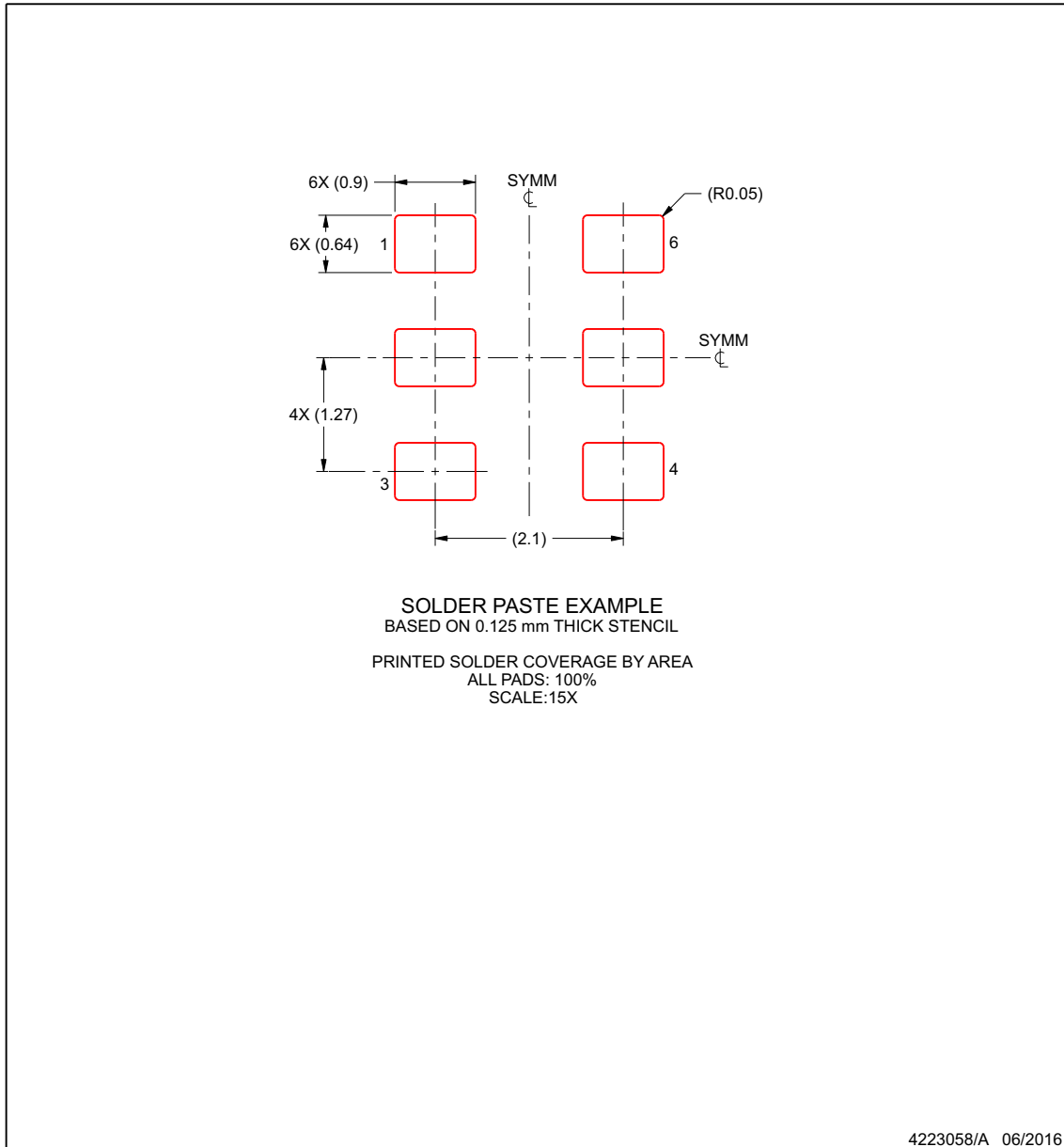
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EXAMPLE STENCIL DESIGN

SIA0006B

QFM - 1.1 mm max height

QUAD FLAT MODULE



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|----------------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMK62A2-100M00SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 | Samples |
| LMK62A2-100M00SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 10000 | Samples |
| LMK62A2-150M00SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 | Samples |
| LMK62A2-150M00SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15000 | Samples |
| LMK62A2-156M25SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS (In Work) & Green (In Work) | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 | Samples |
| LMK62A2-156M25SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS (In Work) & Green (In Work) | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 15625 | Samples |
| LMK62A2-200M00SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 | Samples |
| LMK62A2-200M00SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 20000 | Samples |
| LMK62A2-266M66SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 | Samples |
| LMK62A2-266M66SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62A2 26666 | Samples |
| LMK62E0-156M25SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS (In Work) & Green (In Work) | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 | Samples |
| LMK62E0-156M25SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E0 15625 | Samples |
| LMK62E2-100M00SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 | Samples |
| LMK62E2-100M00SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 10000 | Samples |
| LMK62E2-156M25SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMK62E2-156M25SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62E2 15625 | Samples |
| LMK62I0-100M00SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 | Samples |
| LMK62I0-100M00SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 10000 | Samples |
| LMK62I0-156M25SIAR | ACTIVE | QFM | SIA | 6 | 2500 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 | Samples |
| LMK62I0-156M25SIAT | ACTIVE | QFM | SIA | 6 | 250 | RoHS & Green | NIAU | Level-3-260C-168 HR | -40 to 85 | 62I0 15625 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK62A2-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-150M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-150M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-200M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-200M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-266M66SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62A2-266M66SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E0-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E0-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK62E2-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK6210-100M00SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK6210-100M00SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK6210-156M25SIAR | QFM | SIA | 6 | 2500 | 330.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LMK6210-156M25SIAT | QFM | SIA | 6 | 250 | 180.0 | 12.4 | 3.5 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK62A2-100M00SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62A2-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-150M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-150M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-200M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62A2-200M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62A2-266M66SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62A2-266M66SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E0-156M25SIAR | QFM | SIA | 6 | 2500 | 367.0 | 367.0 | 35.0 |
| LMK62E0-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E2-100M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62E2-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62E2-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62E2-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |
| LMK62I0-100M00SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK62I0-100M00SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK6210-156M25SIAR | QFM | SIA | 6 | 2500 | 346.0 | 346.0 | 33.0 |
| LMK6210-156M25SIAT | QFM | SIA | 6 | 250 | 210.0 | 185.0 | 35.0 |

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