

LMR14010A 4V~40V 1A 降圧コンバータ、高効率 Eco-mode 搭載

1 特長

- 入力電圧範囲: 4V~40V、最大 45V までの過渡保護
- 0.7MHz のスイッチング周波数
- Eco-mode により軽負荷時に極めて高い効率を実現
- 低ドロップアウト動作
- 最大 1A の出力電流
- 高精度イネーブル入力
- 過電流保護
- 内部補償
- 内部ソフトスタート
- 設計サイズ全体の小型化 (TSOT-6L パッケージ)
- WEBENCH® Power Designer により LMR14010A を使用するカスタム設計を作成

2 アプリケーション

- スマート メーター
- 家電製品
- エレベータ / エスカレータ
- カメラ

3 概要

LMR14010A は PWM DC/DC バック(降圧型)レギュレータです。入力電圧範囲が 4V~40V と広く、産業用から車載用まで幅広いアプリケーション向けに設計されています。極めて低い 1 μ A のシャットダウン電流により、バッテリー駆動時間の延長が可能です。動作周波数は 0.7MHz に固定され、小型の外付け部品の使用が可能である一方、出力リップル電圧を最小限に抑えることができます。またソフトスタートおよび補償回路を内蔵しているため、外付け部品の数も抑えることができます。

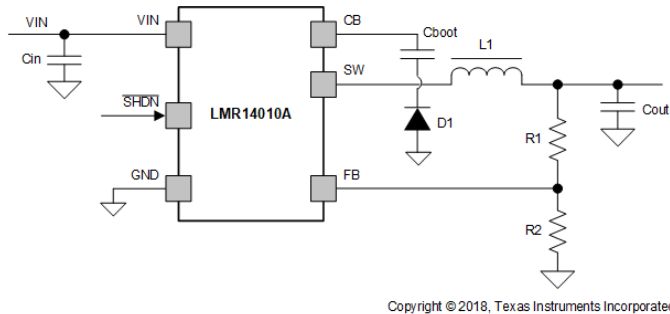
LMR14010A は最大 1A の負荷電流に対して最適化されています。このデバイスの公称帰還電圧は 0.765V です。

このデバイスには、パルス単位の電流制限、熱センシング、過剰な消費電力によるサーマル シャットダウンなどの保護機能が組み込まれています。LMR14010A は薄型の TSOT-6L パッケージ(2.9mm×1.6mm×0.85mm)で供給されます。

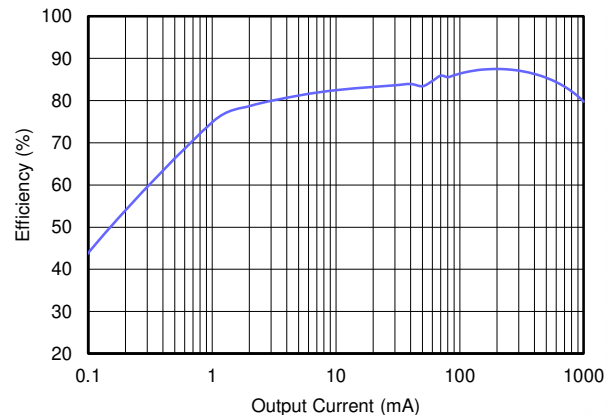
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMR14010A	DDC (SOT-23-THIN, 6)	2.9mm × 2.8mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



効率と電流との関係 ($f_{SW} = 0.7\text{MHz}$ 、 $V_{IN} = 12\text{V}$ 、 $V_{OUT} = 3.3\text{V}$)



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4 Pin Configuration and Functions

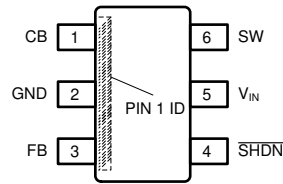


図 4-1. DDC Package, 6-Pin SOT-23-THIN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CB	1	I	SW FET gate bias voltage. Connect C_{boot} capacitor between CB and SW.
FB	3	I	Feedback Pin. Set feedback voltage divider ratio with $V_{OUT} = V_{FB} (1+(R1/R2))$.
GND	2	G	Ground connection.
SHDN	4	I	Enable and disable input pin(high voltage tolerant). Internal pull-up current source. Pull below 1.25 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
SW	6	O	Switch node. Connect to inductor, diode and C_{boot} capacitor.
VIN	5	I	Power input voltage pin. Input for internal supply and drain node input for internal high-side MOSFET.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Input Voltages	V _{IN} to GND	-0.3	45	V
	SHDN to GND	-0.3	45	V
	FB to GND	-0.3	7	V
	CB to SW	-0.3	7	V
Output Voltages	SW to GND	-1	45	V
	SW to GND less than 30-ns transients	-2	45	V
Operating junction temperature, T _J		-40	150	°C
Storage temperature range, T _{stg}		-55	165	°C

- (1) Stresses at or beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Buck regulator	V _{in}	4	40	V
	CB		46	
	CB to SW		6	
	SW	-0.7	40	
	FB	0	5	
Control	SHDN	0	40	
Temperature	Operating junction temperature, T _J	-40	125	°C

5.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		LMR14010A	UNIT
		SOT (DDC)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	102	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	36.9	
ψ _{JB}	Junction-to-board characterization parameter	28.4	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

- (2) All numbers apply for packages soldered directly onto a 3" × 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, number of thermal vias, board size, ambient temperature, and air flow.

5.5 Electrical Characteristics

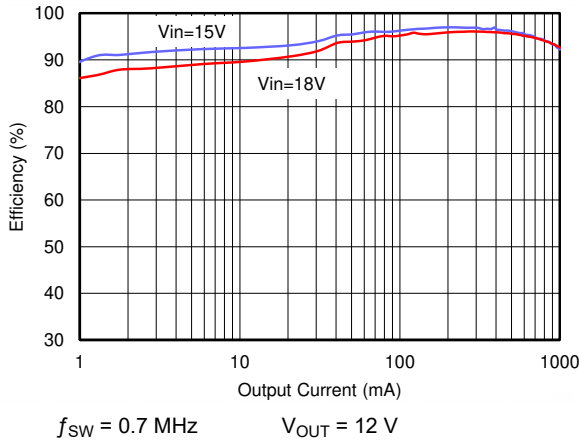
$V_{IN} = 12\text{ V}$, $\overline{\text{SHDN}} = V_{IN}$, $T_J = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT POWER SUPPLY						
V_{IN}	Operating input voltage		4		40	V
	Shutdown supply current	EN = 0 V		1	3	μA
	Undervoltage lockout thresholds	Rising			4	V
		Falling	3			V
I_Q		Eco-mode, no load, $V_{IN} = 12\text{ V}$, not switching		30		μA
SHDN AND UVLO						
	Rising $\overline{\text{SHDN}}$ Threshold Voltage		1.05	1.25	1.38	V
	$\overline{\text{SHDN}}$ PIN current	$\overline{\text{SHDN}} = 2.3\text{ V}$		-4.2		μA
		$\overline{\text{SHDN}} = 0.9\text{ V}$		-1		μA
	Hysteresis current			-3		μA
HIGH-SIDE MOSFET						
	On-resistance	$V_{IN} = 12\text{ V}$, CB to SW = 5.8 V		500		m Ω
t_{ON-MIN}	(1)			95		ns
D_{MAX}	: Maximum duty cycle(1)			96%		
V_{FB}	: Feedback voltage		0.74	0.765	0.79	V
CURRENT LIMIT						
	Current limit threshold	$V_{IN} = 12\text{ V}$		1500		mA
f_{SW}	Switching frequency		550	700	850	kHz
THERMAL PERFORMANCE						
$T_{SHUTDOWN}$	Thermal shutdown trip point(1)			170		$^\circ\text{C}$
T_{HYS}	(1)	Hysteresis		10		$^\circ\text{C}$

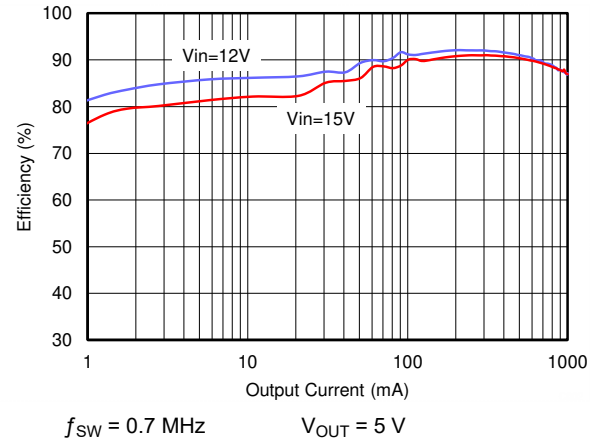
(1) Specified by design.

5.6 Typical Characteristics

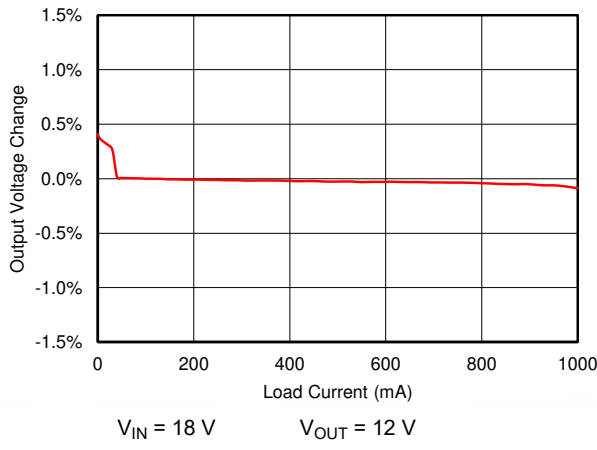
Unless otherwise noted, $V_{IN} = 12\text{ V}$, $L = 22\ \mu\text{H}$, $C_{OUT} = 22\ \mu\text{F}$, $T_A = 25^\circ\text{C}$



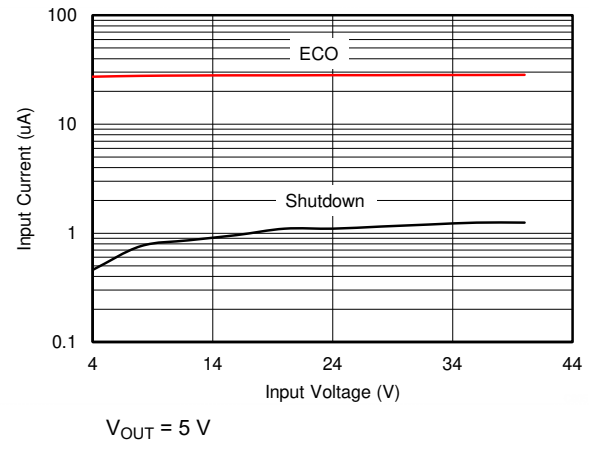
5-1. Efficiency vs Load Current



5-2. Efficiency vs Load Current



5-3. Load Regulation



5-4. Supply Current vs Input Voltage (No Load)

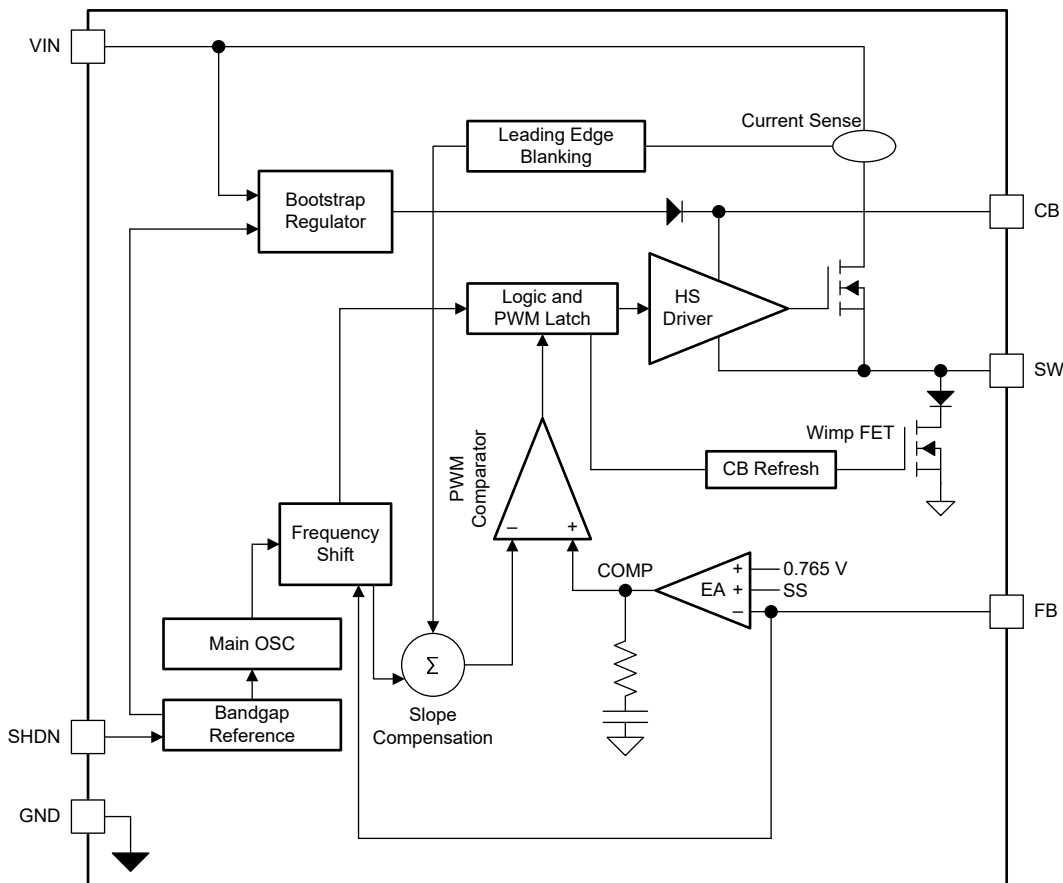
6 Detailed Description

6.1 Overview

The LMR14010A device is a 40-V, 1-A step-down (buck) regulator. The buck regulator has a very low-quiescent current during the light load to prolong the battery life.

The LMR14010A improves performance during line and load transients by implementing a constant frequency, current mode control which reduces output capacitance and simplifies frequency compensation design. The LMR14010A reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high side MOSFET off when the boot voltage falls below a preset threshold. The LMR14010A can operate at high duty cycles because of the boot UVLO and small refresh FET. The output voltage can be stepped down to as low as the 0.765-V reference. Internal soft start is featured to minimize inrush currents.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Fixed Frequency PWM Control

The LMR14010A operates at a fixed frequency, and it implements peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

6.3.2 Bootstrap Voltage (CB)

The LMR14010A has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts.

To improve drop out, the LMR14010A is designed to operate at 96% duty cycle as long as the CB to SW pin voltage is greater than 3.2 V. When the voltage from CB to SW drops below 3.2 V, the high-side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Because the supply current sourced from the CB capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

6.3.3 Setting the Output Voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765 V, so the ratio of the feedback resistors sets the output voltage according to the following equation: $V_{OUT} = 0.765 \text{ V} (1 + (R1/R2))$. Typically R2 will be given as 1 k Ω to 100 k Ω for a starting value. To solve for R1 given R2 and V_{OUT} uses $R1 = R2 ((V_{OUT}/0.765 \text{ V}) - 1)$.

6.3.4 Enable ($\overline{\text{SHDN}}$) and V_{IN} Undervoltage Lockout

The LMR14010A $\overline{\text{SHDN}}$ pin is a high-voltage tolerant input with an internal pullup circuit. The device can be enabled even if the $\overline{\text{SHDN}}$ pin is floating. The regulator can also be turned on using 1.25-V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints it can be used. TI recommends a 100-k Ω or larger resistor between the applied voltage and the $\overline{\text{SHDN}}$ pin to protect the device. When $\overline{\text{SHDN}}$ is pulled down to 0 V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1 μA . If the shutdown function is not to be used, the $\overline{\text{SHDN}}$ pin can be tied to V_{IN} . The maximum voltage to the $\overline{\text{SHDN}}$ pin must not exceed 40 V.

The LMR14010A has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This makes sure that the regulator is not latched into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the UVLO voltage level. If there is a requirement for a higher UVLO voltage, the $\overline{\text{SHDN}}$ can be used to adjust the input voltage UVLO by using external resistors.

6.3.5 Current Limit

The LMR14010A implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle by cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

6.3.6 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C typical. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. After the junction temperature decreases below 160°C typical, the device reinitiates the power-up sequence.

6.4 Device Functional Modes

6.4.1 Continuous Conduction Mode

The LMR14010A steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between VIN and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor, the load current is supplied by C_{OUT} and the current through the inductor is rising. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: $D = V_{OUT}/V_{IN}$ and $D' = (1-D)$ where D is the duty cycle of the switch, D and D' will be required for design calculations.

6.4.2 Eco-mode

The LMR14010A operates in Eco-mode at light-load currents to improve efficiency by reducing switching and gate drive losses. For Eco-mode operation, the LMR14010A senses peak current, not average or load current, so the load current where the device enters Eco-mode is dependent on V_{IN}, V_{OUT} and the output inductor value. When the load current is low and the output voltage is within regulation, the device enters Eco-mode (see [Figure 7-8](#)) and draws only 28-μA input quiescent current.

7 Application and Implementation

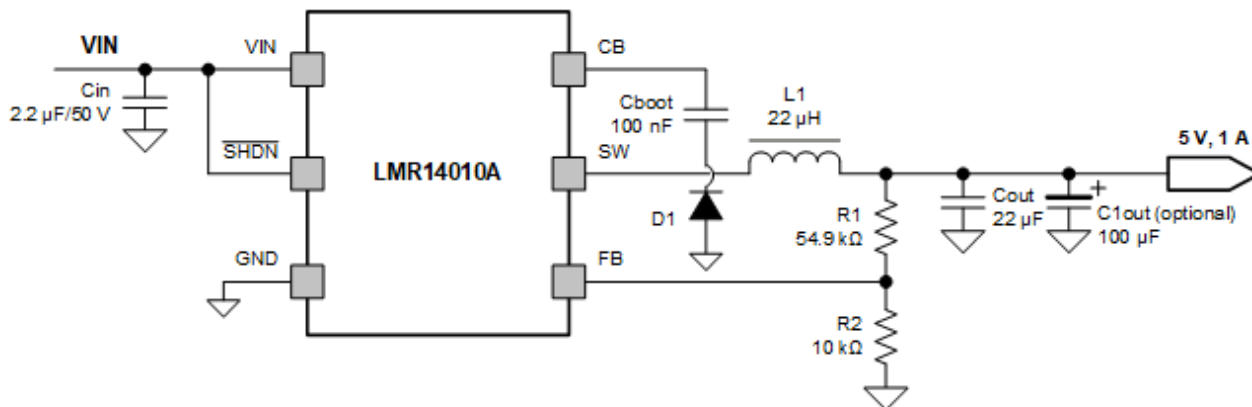
注

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7.1 Application Information

The LMR14010A is a step down DC-to-DC regulator. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMR14010A. This section presents a simplified discussion of the design process.

7.2 Typical Application



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図 7-1. LMR14010A Application Circuit, 5-V Output

7.2.1 Design Requirements

7.2.1.1 Step-By-Step Design Procedure

This example details the design of a high-frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

PARAMETER		VALUE
Input voltage, V_{IN}		9 V to 16 V, typical 12 V
Output voltage, V_{OUT}		5.0 V \pm 3%
Maximum output current example I_{O_max}		1 A
Minimum output current example I_{O_min}		0.1 A
Transient response 0.03 A to 0.6 A		5%
Output voltage ripple		1%
Switching frequency f_{SW}		700 kHz
Target during load transient	Overshoot peak value	106% of output voltage
	Undershoot value	91% of output voltage

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMR14010A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Because the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. 式 1 is used to calculate the minimum value of the output inductor, where K_{IND} is ripple current percentage. A reasonable value is setting the ripple current to be 30% (K_{IND}) of the DC output current. For this design example, the minimum inductor value is calculated to be 16.4 μH , and a nearest standard value was chosen: 22 μH . For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 式 3 and 式 4. The inductor ripple current is 0.22 A, and the RMS current is 1 A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is 22 μH with a 1.6-A current rating. Using a rating near 1.6 A will enable the LMR14010A to current limit without saturating the inductor. This is preferable to the LMR14010A going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o \min} = \frac{V_{in \max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in \max} \times f_{sw}} \quad (1)$$

$$I_{ripple} = \frac{V_{out} \times (V_{in \max} - V_{out})}{V_{in \max} \times L_o \times f_{sw}} \quad (2)$$

$$I_{L-RMS} = \sqrt{I_o^2 + \frac{1}{12} I_{ripple}^2} \quad (3)$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \quad (4)$$

7.2.2.3 Output Capacitor Selection

The selection of C_{OUT} is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. For this example, the transient load response is specified as a 3% change in V_{out} for a load step from 0.1 A to 1 A (full load). For this example, $\Delta I_{OUT} = 1 - 0.1 = 0.9$ A and $\Delta V_{OUT} = 0.03 \times 5 = 0.15$ V. Using these numbers gives a minimum capacitance of 17.1 μ F. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that must be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst case load step will be from 1 A to 0.1 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3 % of the output voltage. This will make $V_{o_overshoot} = 1.03 \times 5 = 5.15$ V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 14.3 μ F.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, V_{o_ripple} is the maximum allowable output voltage ripple, and I_{L_ripple} is the inductor ripple current. Equation 7 yields 0.26 μ F.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR must be less than 680 m Ω . Additional capacitance de-ratings for aging, temperature and dc bias must be factored in which will increase this minimum value. For this example, 22 μ F ceramic capacitors will be used. Capacitors in the range of 4.7 μ F to 100 μ F are a good starting point with an ESR of 0.7 Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \quad (5)$$

$$C_{out} > L_o \times \frac{(I_{oh}^2 - I_{ol}^2)}{(V_f^2 - V_i^2)} \quad (6)$$

$$C_{out} > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{o_ripple}}{I_{L_ripple}}} \quad (7)$$

$$R_{ESR} < \frac{V_{o_ripple}}{I_{L_ripple}} \quad (8)$$

7.2.2.4 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. In the target application, the current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is not much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately

$(1-D) \times I_{OUT}$, however the peak current rating must be higher than the maximum load current. A 1-A to 2-A rated diode is a good starting point.

7.2.2.5 Input Capacitor Selection

A low ESR ceramic capacitor is needed between the VIN pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 1- μ F to 10- μ F value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor value can decrease up to 50% of the nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LMR14010A. The input ripple current can be calculated using below Equations.

For this example design, one 2.2- μ F, 50-V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, $I_{OUTMAX} = 1$ A, $C_{IN} = 2.2$ μ F, $f_{SW} = 700$ kHz, yields an input voltage ripple of 162 mV and an rms input ripple current of 0.5 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\ min}} \times \frac{(V_{in\ min} - V_{out})}{V_{in\ min}}} \quad (9)$$

$$\Delta V_{in} = \frac{I_{out\ max} \times 0.25}{C_{in} \times f_{sw}} \quad (10)$$

7.2.2.6 Bootstrap Capacitor Selection

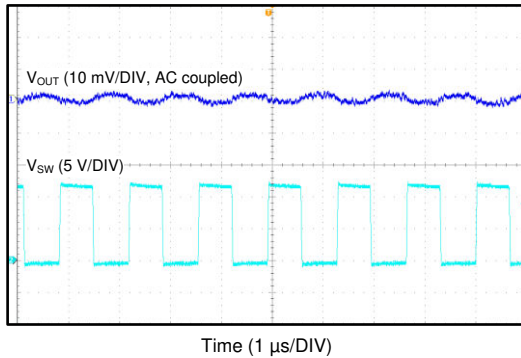
TI recommends a 0.1- μ F ceramic capacitor or larger for the bootstrap capacitor (C_{boot}). For applications where the input voltage is close to output voltage, TI recommends a larger capacitor, generally 0.1 μ F to 1 μ F to make sure of plenty of gate drive for the internal switches and a consistently low $R_{DS(ON)}$. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

Below are the recommended typical output voltage inductor, capacitor combinations for optimized total design size.

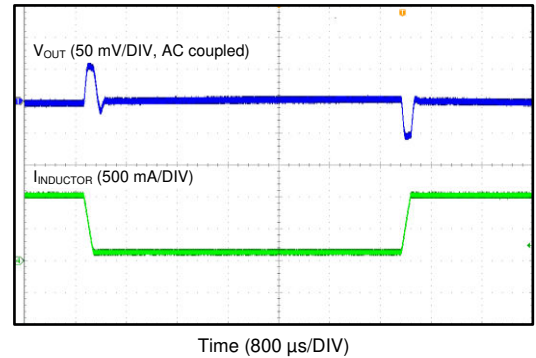
P/N	V _{OUT} (V)	R1 (k Ω)	R2 (k Ω)	L (μ H)	C _{OUT} (μ F)
LMR14010A	5	54.9 (1%)	10 (1%)	22	22
LMR14010A	5.7	64.9 (1%)	10 (1%)	22	22
LMR14010A	12	147 (1%)	10 (1%)	22	10

7.2.3 Application Performance Curves

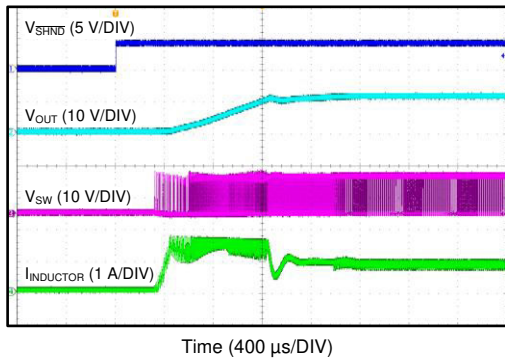
Unless otherwise noted, $V_{IN} = 12\text{ V}$, $L = 22\ \mu\text{H}$, $C_{OUT} = 22\ \mu\text{F}$, $T_A = 25^\circ\text{C}$.



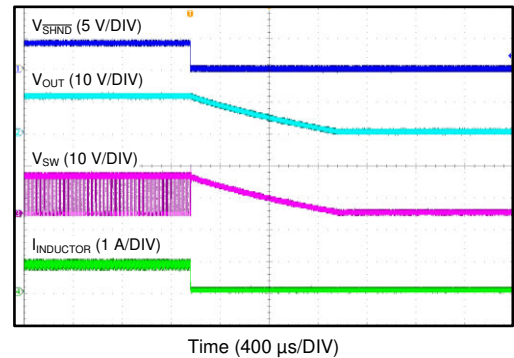
7-2. Switching Node and Output Voltage Waveform ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{Load} = 1\text{ A}$)



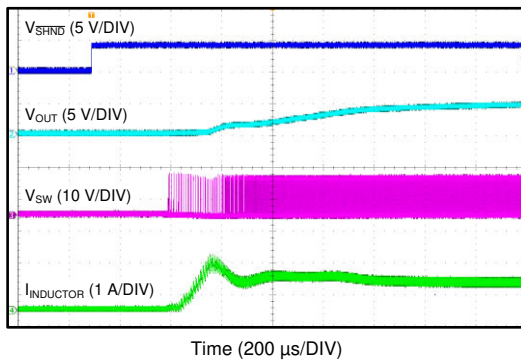
7-3. Load Transient Between 0.1 A and 1 A ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$)



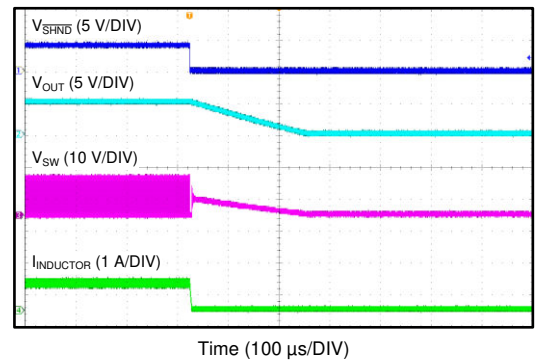
7-4. Start-up Waveform ($V_{IN} = 18\text{ V}$, $V_{OUT} = 12\text{ V}$, $I_{Load} = 800\text{ mA}$)



7-5. Shutdown Waveform ($V_{IN} = 18\text{ V}$, $V_{OUT} = 12\text{ V}$, $I_{Load} = 800\text{ mA}$)



7-6. Start-Up Waveform ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{Load} = 800\text{ mA}$)



7-7. Shutdown Waveform ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_{Load} = 800\text{ mA}$)

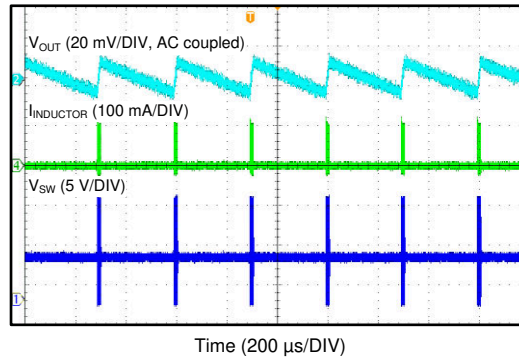


図 7-8. Eco-mode Operation ($V_{IN} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$, No Load)

7.3 Power Supply Recommendations

The LMR14010A is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 4 V. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR14010A supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR14010A, additional bulk capacitance can be required in addition to the ceramic input capacitors.

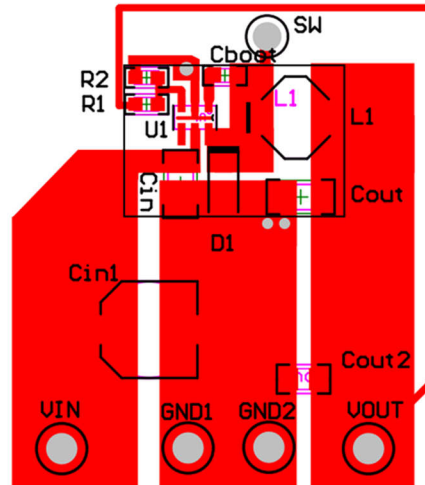
7.4 Layout

7.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Keep the feedback network, resistors R1 and R2, close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin.
2. Place the input capacitor C_{IN} close to the V_{IN} pin. This action reduces copper trace inductance which effects input voltage ripple of the device.
3. Place the inductor L1 close to the SW pin to reduce magnetic and electrostatic noise.
4. Place the output capacitor C_{OUT} close to the junction of L1 and the diode D1. The L1, D1 and C_{OUT} trace must be as short as possible to reduce conducted and radiated noise.
5. Tie the ground connection for the diode, C_{IN} and C_{OUT} to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.

7.4.2 Layout Example



7-9. LMR14010A Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LMR14010A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WBENCH.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2018) to Revision A (January 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• 商標の情報を更新.....	1
• Changed the operating junction temperature MIN from 0 to –40.....	4
• Added table note to the <i>Thermal Information</i> table.....	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR14010ADDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N72	Samples
LMR14010ADDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1N72	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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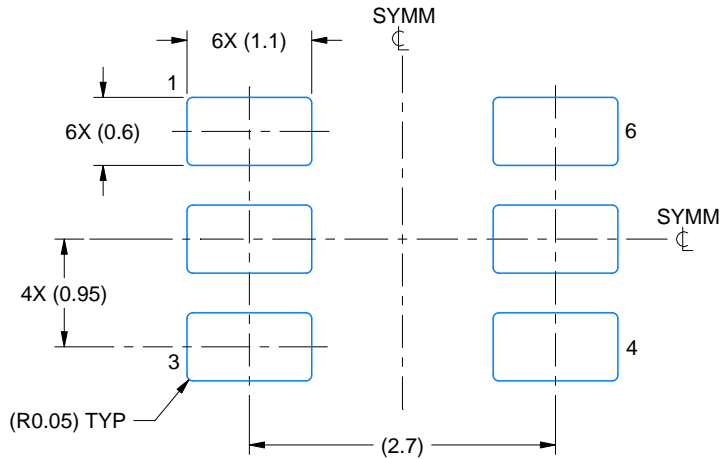
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

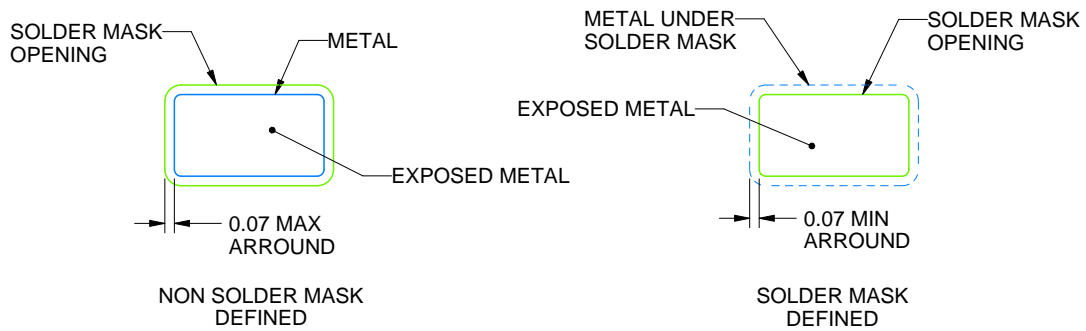
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDEMASK DETAILS

4214841/D 06/2024

NOTES: (continued)

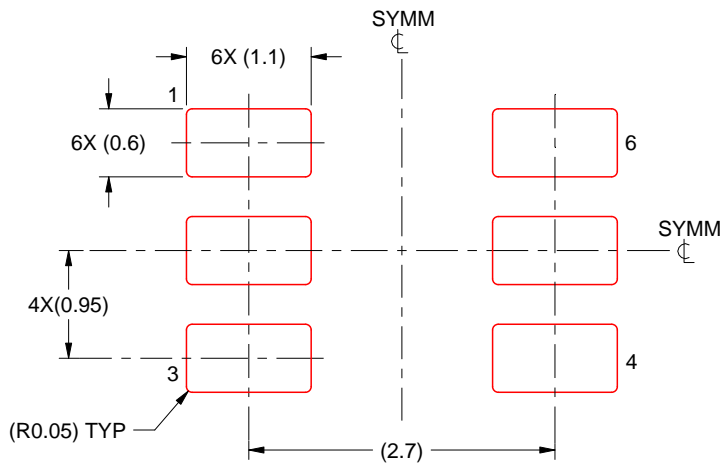
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/D 06/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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