LMR36506-Q1 3V～65V、0.6A、サイズと軽負荷時効率を最適化した同期整流降圧型コンバータ

ADVANCE INFORMATION

1 特長

- **車載アプリケーション用の AEC-Q100 認定取得済み：**
  - デバイス温度グレード 1：–40°C～+125°C、T_A
- **80% を超える効率 (1mA 時)**
  - I_q：4µA (スイッチング時、24V_{IN}、3.3V_{OUT}、固定出力オプション)
- **小さなソリューション・サイズとわずかな部品コスト**
  - 超小型の 2mm × 2mm HotRod™ウェッタブル・フランク付きパッケージ
  - 内部補償による高い電力密度と外付け部品数の低減
- **車載用途向けの設計**
  - 接合部温度範囲：–40℃～+150℃
  - CISPR 25 EMI 規格に最適化
  - 広い入力電圧範囲：3.0V (立ち下がりスレッショルド) ～65V
  - 可変、3.3V/5V 固定の出力電圧を選択可能
  - MODE/SYNC ピンで同期可能なバリアント
  - PFM と強制 PWM を選択可能 (MODE/SYNC ピン・バリアントの場合)
  - 可変スイッチング周波数：200kHz～2.2MHz (RT ピンのバリアント)
  - LMR36503-Q1 (65V、300mA) とピン互換

2 アプリケーション

- 先進運転支援システム (ADAS)
- ボディ・エレクトロニクスとライティング
- インフォテインメント / クラスタ

3 概要

LMR36506-Q1 は業界で最も小さな 65V、0.6A 同期整流降圧型 DC/DC コンバータであり、2mm × 2mm の HotRod™パッケージで供給されます。この堅牢で信頼性の高いコンバータは、非常に少ない外付け部品と簡単な PCB レイアウトで最大 70V の入力過渡電圧に対応でき、非常に優れた EMI 性能を備え、固定 3.3V、5V とその他の可変出力電圧をサポートしています。

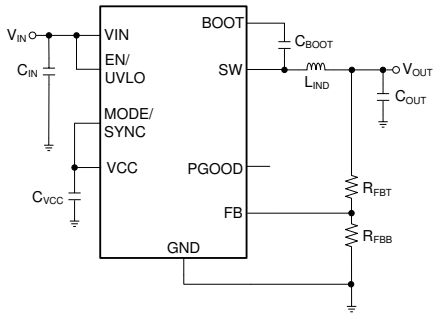
LMR36506-Q1 は、内部補償付きピーク電流モード制御アーキテクチャを使用して、200kHz～2.2MHz という広いスイッチング周波数範囲にわたり最小限の出力容量で安定した動作を維持します。LMR36506-Q1 は入力電圧が最低 3V に低下しても動作するため、過酷なコールド・クランク開始インパルスに耐えるよう設計される入力範囲の広い車載用電源に最適です。LMR36506-Q1 のオープン・ドレイン PGOOD 出力は、グリッチ・フィルタと遅延付き解除によって出力電圧の実際の状態を示すため、外部のスーパーバイザは不要です。FPWM から PFM へのシームレスな移行と、非常に小さいスタンバイ時静止電流により、極めて低い出力負荷でも高い効率を実現します。MODE/SYNC ピン・バリアントは、LMR36506-Q1 を外部クロックに同期させ、またはパルス幅変調 (PFM) モードを選択することで、きわめて低い出力負荷での効率を向上させるのに役立ちます。LMR36506-Q1 の小さなソリューション・サイズと豊富な機能セットは、広範な車載用最終機器を簡単に実装できるように設計されています。

製品情報(1)

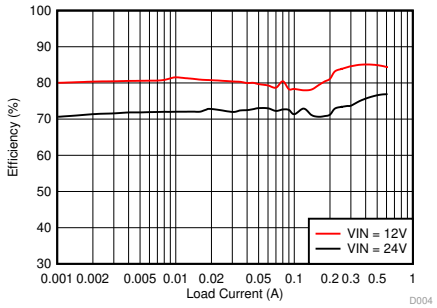
型番	パッケージ	本体サイズ (公称)
LMR36506-Q1	VQFN-HR (9)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



効率と出力電流の関係
V_{OUT} = 3.3V (固定)、2.2MHz



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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• 最初の公開リリース	1

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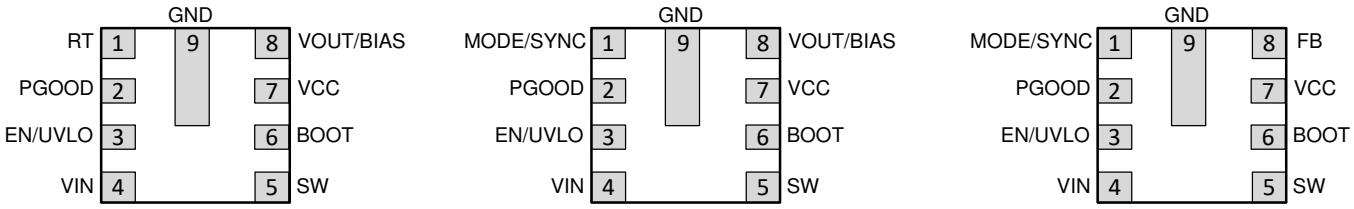
5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
LMR36506MSCQRPERQ1	Adjustable	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36506MSC5RPERQ1	5-V Fixed	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36506MSC3RPERQ1	3.3-V Fixed	Yes (PFM/FPWM Selectable)	Fixed 2.2 MHz	Yes
LMR36506RS3QRPERQ1	3.3-V Fixed	No (Default PFM at light load)	Adjustable with RT resistor	Yes

ADVANCE INFORMATION

6 Pin Configuration and Functions

RPE Package
9-Pin VQFN-HR
Top View (All variants)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RT or MODE/SYNC	A	When the part is trimmed as the RT pin variant, the switching frequency in the part can be adjusted from 200 kHz to 2.2 MHz based on the resistor value connected between RT and GND. When the pin is trimmed as the MODE/SYNC variant, the part can operate in user-selectable PFM/FPWM operation. In FPWM, the part can be synchronized to an external clock. Clock triggers on rising edge of applied external clock. Do not float this pin.
2	PGOOD	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. It goes low when EN = low. It can be open or grounded when not used.
3	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float.*
4	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND.
5	SW	P	Regulator switch node. Connect to power inductor.
6	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin.
7	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
8	VOUT/BIAS or FB	A	Fixed output options are available with the VOUT/BIAS pin variant. Connect to output voltage node for fixed VOUT. Check the *Device Comparison Table* for more details. The FB pin variant can help adjust the output voltage. Connect to tap point of feedback voltage divider. Do not float the pin.
9	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
A = Analog, P = Power, G = Ground			

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Voltages	VIN to GND	–0.3	70	V
	EN to GND	–0.3	70.3	V
	SW to GND	–0.3	70.3	V
	MODE/SYNC to GND (MODE/SYNC variant)	–0.3	5.5	V
	RT to GND (RT variant)	–0.3	5.5	V
	PGOOD to GND	0	20	V
	BIAS to GND (Fixed output variant)	–0.3	20	V
	FB to GND - (Adjustable VOUT)	–0.3	20	V
	BOOT to SW	–0.3	5.5	V
	VCC to GND	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD (Automotive) Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Clasification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD clasiffication Level C5	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 °C to 150 °C (unless otherwise noted)(1)(2)

		MIN	TYP	MAX	UNIT
Input voltage	Input Voltage Range after startup	3.6		65	V
Output current	Load current range(3)	0		0.6	A
Frequency setting	Selectable Frequency Range with RT (with RT variant only)	0.2		2.2	MHz
	Set Frequency Value with RT connected to GND (with RT variant only)		2.2		MHz
	Set Frequency Value with RT connected to VCC (with RT variant only)		1		MHz
	Fixed Internal Frequency Trim options (with MODE/SYNC variant only)	0.4	1	2.2	MHz
	External Sync CLK (with MODE/SYNC variant only)	0.2		2.2	MHz

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics table.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125℃
(3) Maximum continuous DC current may be derated when operating with high switching frequency and/or high ambient temperature. See Application section for details.

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7.4 Thermal Information

THERMAL METRIC(1)		LMR36506-Q1 VQFN (RPE) 9 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application. For design information see the **Maximum Ambient Temperature** section.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_R}	Minimum operating Input Voltage (Rising)	Rising Threshold	3.4	3.5	3.6	V
V_{IN_F}	Minimum operating Input Voltage (Falling)	Once Operating; Falling Threshold	2.87	3.0		V
$I_{Q\_13p5\_Fixed}$	Non-switching input current; measured at VIN pin (3)	V_{IN} = V_{EN} = 13.5V ; $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed Output Option	0.55	0.7	0.855	µA
$I_{Q\_13p5\_Adj}$	Non-switching input current; measured at VIN pin (3)	V_{IN} = V_{EN} = 13.5V ; V_{FB} = 1.5V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Adjustable Output Option	13.5	17.5	21.5	µA
$I_{Q\_24p0\_Fixed}$	Non-switching input current; measured at VIN pin (3)	V_{IN} = V_{EN} = 24V ; $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed Output Option	1.05	1.2	1.4	µA
$I_{Q\_24p0\_Adj}$	Non-switching input current; measured at VIN pin (3)	V_{IN} = V_{EN} = 24V ; V_{FB} = 1.5V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Adjustable Output Option	14.9	18	21.5	µA
I_{B_13p5}	Current into VOUT/BIAS pin (not switching)(3)	V_{IN} = 13.5V, $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed Output Option	14.75	17	20.65	µA
I_{B_24p0}	Current into VOUT/BIAS pin (not switching)(3)	V_{IN} = 24V, $V_{OUT/BIAS}$ = 5.25V, $V_{MODE/SYNC}$ = V_{RT} = 0V; Fixed Output Option	14.5	17.5	20.5	µA
I_{SD_13p5}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0; V_{IN} = 13.5V	0.4	0.5	0.685	µA
I_{SD_24p0}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0; V_{IN} = 24V	0.873	1	1.2	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	Enable wake-up threshold		0.4			V
$V_{EN-VOUT}$	Precision enable high level for VOUT		1.16	1.263	1.36	V
$V_{EN-HYST}$	Enable threshold hysteresis below $V_{EN-VOUT}$		0.3	0.35	0.38	V
I_{LKG-EN}	Enable input leakage current	VEN = 3.3 V	0.1	0.2	2	nA
INTERNAL LDO						
V_{CC}	Internal VCC voltage	3.6 V ≤ VIN ≤ 65 V; Adjustable Output Option	3.125	3.15	3.22	V

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Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Internal VCC voltage	3.6 V ≤ VIN ≤ 65 V; $V_{OUT/BIAS}$ = 3.3 V	3.12	3.15	3.24	V
I_{CC}	Bias regulator current limit		25	85	135	mA
$V_{CC-UVLO}$	Internal VCC undervoltage lockout	VCC rising under voltage threshold	3.1	3.2	3.5	V
$V_{CC-UVLO-HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below $V_{CC-UVLO}$	0.54	0.7	1.1	V
CURRENT LIMITS						
I_{SC-0p6}	Short circuit high side current Limit	0.6A Version	0.87	1	1.11	A
$I_{LS-LIMIT-0p6}$	Low side current limit	0.6A Version	0.64	0.7	0.752	A
$I_{PEAK-MIN-0p6}$	Minimum Peak Inductor Current	PFM operation, 0.6A Version; Duty Factor = 0	0.14	0.18	0.225	A
I_{ZC}	Zero Cross Current	PFM Operation	0	0.01	0.022	A
I_{L-NEG}	Negative current limit	FPWM operation	–0.4	–0.5	–0.6	A
POWER GOOD						
V_{PG-OV}	PGOOD upper threshold - Rising	% of FB voltage	105	107	110	%
V_{PG-UV}	PGOOD lower threshold - Falling	% of FB voltage	92	94	96.5	%
V_{PG-HYS}	PGOOD hysteresis	% of FB voltage	1	1.5	2	%
$V_{PG-VALID}$	Minimum input voltage for proper PG function		0.75	1	2	V
$R_{PG-EN5p0}$	$R_{DS(ON)}$ PG output	VEN = 5.0V, 1mA pull-up current	20	40	70	Ω
R_{PG-EN0}	$R_{DS(ON)}$ PG output	VEN = 0 V, 1mA pull-up current	10	17	30	Ω
OSCILLATOR (MODE/SYNC)						
$V_{SYNC-HIGH}$	Sync input and mode high level threshold				1.8	V
$V_{SYNC-HYS}$	Sync input hysteresis		230	285	365	mV
$V_{SYNC-LOW}$	Sync input and mode low level threshold		0.8			V
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 0.3 A		550	860	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 0.3 A		275	430	mΩ
$V_{CBOOT-UVLO}$	Cboot - SW UVLO threshold		2.2	2.3	2.4	V
VOLTAGE REFERENCE						
$V_{FB\_Fixed3p3}$	Initial VOUT voltage accuracy for 3.3 V	V_{IN} = 3.6V to 60V FPWM Mode	3.25	3.3	3.34	V
$V_{FB\_Fixed5p0}$	Initial VOUT voltage accuracy for 5 V	V_{IN} = 5.5V to 60V FPWM Mode	4.93	5	5.07	V
V_{REF}	Internal reference voltage	V_{IN} = 3.6V to 60V FPWM Mode	0.985	1	1.015	V
I_{FB}	FB input current	Adjsutable output voltage versions only, FB = 1V		85	100	nA

7.6 Timing Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START					

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Timing Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Time from first SW pulse to V_{FB} at 90%, of V_{REF}	V_{IN} ≥ 3.6V	2.2	2.67	3.21	ms
POWER GOOD						
t_{RESET_FILTER}	Glitch filter time constant for PG function		15	25	40	µs
t_{PGOOD_ACT}	Delay time to PG high signal		1.7	2	2.1	ms
OSCILLATOR (MODE/SYNC)						
$t_{PULSE\_SYNC\_MIN}$	Minimum Pulse duration to sync to external CLK		11	25	100	ns
$t_{PULSE\_SYNC\_MAX}$	Maximum Pulse duration to sync to external CLK		6.4	8.5	11	µs
t_{MODE_DELAY}	Time delay from MODE pin pulled LOW to part transitioning from FPWM to Auto Mode		5		18	µs

7.7 Switching Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW)						
t_{ON-MIN}	Minimum switch on-time	VIN =24V I_{OUT} = 0.3A	45	55	82	ns
$t_{OFF-MIN}$	Minimum switch off-time		45	50	77	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	7.4	8.5	9.4	µs
OSCILLATOR (RT)						
f_{OSC_2p2MHz}	Internal oscillator frequency	RT = GND	2.1	2.2	2.3	MHz
f_{OSC_1p0MHz}	Internal oscillator frequency	RT = VCC	0.95	1	1.05	MHz
f_{ADJ_400kHz}		RT = 39.2kΩ (with RT variant only)	0.34	0.4	0.46	MHz

7.8 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 13.5 V, $V_{OUT/BIAS}$ = 3.3 V, I_{OUT} = 0 A, PFM mode		6.5		µA
D_{MAX}	Maximum switch duty cycle(2)			98%		
VOLTAGE REFERENCE (FB or VOUT/BIAS)						
$V_{OUT\_5p0V\_ACC}$	V_{OUT} = 5 V, V_{IN} = 5.5 V to 65 V, I_{OUT} = 0 A to full load (1)		–1.5		2.5	
$V_{OUT\_3p3V\_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 to full load (1)	FPWM Operation	–1.5		1.5	%
	V_{OUT} = 3.3 V, V_{IN} = 3.6V to 65 V, I_{OUT} = 0 A to full load (1)	PFM operation	–1.5		2.5	

ADVANCE INFORMATION

System Characteristics (continued)

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPREAD SPECTRUM						
f_{PSS}	Spread spectrum pseudo random pattern frequency	Spread spectrum active, Fsw= 2.2MHz		0.98	1.5	Hz
f_{SSS}	Spread spectrum pseudo random pattern frequency	Spread spectrum active	-3		3	%
THERMAL SHUTDOWN						
T_{SD-R}	Thermal shutdown rising	Shutdown threshold	158	168	180	°C
T_{SD-F}	Thermal shutdown falling	Recovery threshold	150	158	165	°C
T_{SD-HYS}	Thermal shutdown hysteresis		8	10	15	°C

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

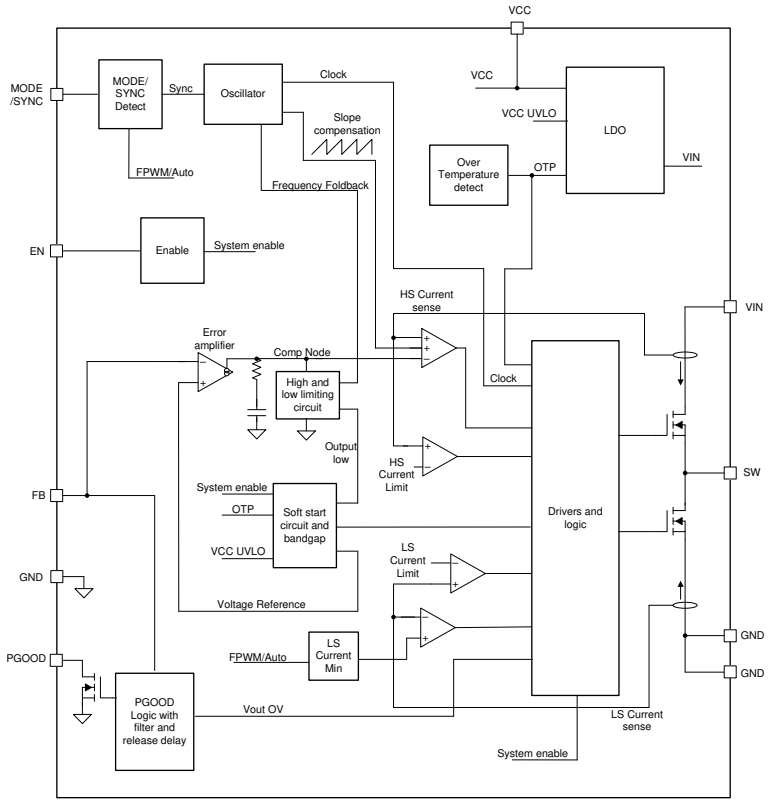
The LMR36506-Q1 is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of switching frequencies and duty ratios. If the minimum ON-time or OFF-time cannot support the desired duty ratio, the switching frequency gets reduced automatically, maintaining the output voltage regulation. With the right internal loop compensation the system design time with the LMR36506-Q1 reduces significantly with minimal external components compared to other externally compensated buck regulators.

The LMR36506-Q1 is designed to minimize end-product component cost and solution size while operating in all demanding automotive environments. The LMR36506-Q1 can be set to operate from 200 kHz through 2.2 MHz with the correct resistor selection from RT pin to ground. In addition, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR36506-Q1 is designed to reduce EMI/EMC emissions. It includes a pseudo-random spread spectrum scheme, has a low pin inductance flip chip on the lead (HotRod) package, and is available with MODE/SYNC, which can be synchronized to an external clock when needed. Together, these features eliminate the need for any common-mode choke, shielding, and input filter inductor, greatly reducing the complexities and cost of the EMI/EMC mitigation measures.

To be reliably used in all environments, the LMR36506-Q1 has a package designed with enlarged corner terminals for improved BLR performance over varied PCB thickness. In addition, the LMR36506-Q1 in a 2-mm x 2-mm QFN package comes with wettable flanks as well, allowing for quick optical inspection of all solder joints.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Voltage Selection

For adjustable output voltage variants in the LMR36506-Q1, a resistor divider between the output voltage and the IC FB pin can be used to set the output voltage value. The LMR36506-Q1 uses a 1-V internal reference voltage.

$$R_{FBB} = \frac{R_{FBT}}{V_{OUT} - 1} \quad (1)$$

When using the LMR36506-Q1 as fixed-output options, simply connect FB (or VOUT/BIAS here) to the output. Check the *Device Comparison Table* for more details about the fixed-output variants.

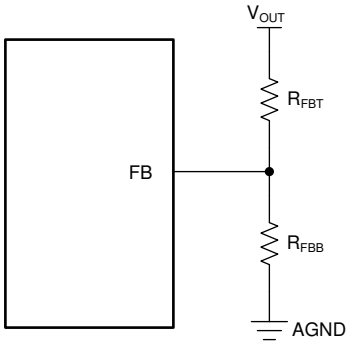


図 1. Setting Output Voltage for Adjustable Output Variant

For adjustable output options, an addition feedforward capacitor, C_{FF}, in parallel with the R_{FBT} can be needed to optimize the transient response. No additional resistor divider or feedforward capacitor, C_{FF}, is needed in case of fixed-output variants.

8.3.2 Enable and Start-up

Voltage on the EN pin controls the ON or OFF functionality of the LMR36506-Q1. The part stays in shutdown mode as long as the EN pin voltage is less than $V_{EN-WAKE}$ = 0.4 V. During the shutdown mode, the input current drawn by the device typically drops down to 1 µA. Applying a voltage at the EN pin greater than the $V_{EN-WAKE}$ causes the device to enter the standby mode, powering up the internal LDO to generate VCC. As the EN voltage further approaches $V_{EN-VOUT}$, the device finally starts switching, allowing it to enter the start-up mode and begin the soft-start period. During the shutdown process, when the EN input is brought below $V_{EN-VOUT}$ by $V_{EN-HYST}$, the regulator stops switching and re-enters the standby mode. Any further decrease in the EN pin voltage below $V_{EN-WAKE}$ finally shuts down the device. The EN input pin can be connected directly to VIN input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The limits of various EN thresholds values listed here can be found in the *Electrical Characteristics* table.

ADVANCE INFORMATION

Feature Description (continued)

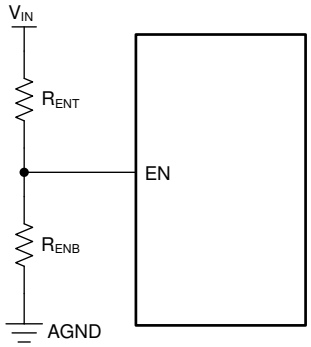


図 2. VIN UVLO Using the EN pin

8.3.3 External CLK SYNC (with MODE/SYNC)

It is often desirable to synchronize the operation of multiple regulators in a single system. This technique results in better defined EMI and can reduce the need for capacitance on some power rails. The LMR36506-Q1 device provides a MODE/SYNC pin variant, which allows synchronization with an external clock. The LMR36506-Q1 implements an in-phase locking scheme – the rising edge of the clock signal provided to the input of the LMR36506-Q1 corresponds to the turning on of the high-side device. This function is implemented using phase locking over a limited frequency range, eliminating large glitches upon initial application of an external clock. The clock fed into the LMR36506-Q1 replaces the internal free-running clock, but does not affect frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

8.3.4 Adjustable Switching Frequency (with RT)

A resistor tied to the LMR36506-Q1 RT pin and GND is used to set the desired operating frequency between 200 kHz and 2.2 MHz. See 図 3 to determine the resistor value needed for the desired switching frequency. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal.

1. Connecting the RT pin directly to GND sets the LMR36506-Q1 default F_{SW} to 2.2 MHz.

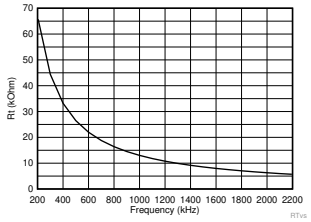


図 3. Setting Clock Frequency

8.3.5 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR36506-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 4. During initial power up, a total delay of 5 ms (typical) is encountered from the time the $V_{EN-VOUT}$ is triggered to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

Feature Description (continued)

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin must be grounded. When the EN pin is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage is ≥ 2 V (maximum). Limit the current into this pin to ≤ 4 mA.

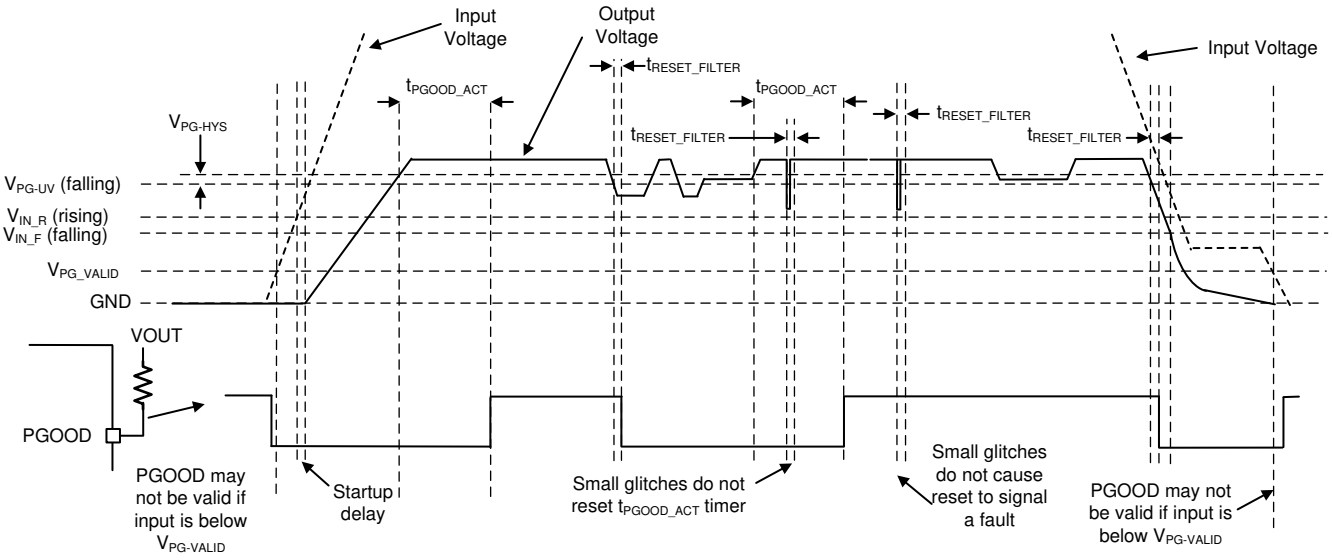


図 4. Power-Good Operation

8.3.6 Internal LDO, VCC UVLO, and VOUT/BIAS Input

The LMR36506-Q1 uses the VCC pin for all the internal power supply. The VCC pin draws power either from the VIN (for adjustable output variants) or the VOUT/BIAS (for fixed output variants). In fixed output variants, once the LMR36506-Q1 is active, the VCC continues to draw power from the input voltage, VIN, when the VOUT/BIAS voltage measures less than 3.15 V (during start-up and other transient conditions) or from the VOUT/BIAS itself when VOUT/BIAS measures is more than 3.15 V (once the device has reached steady state). VCC typically measures 3.3 V under most conditions. To prevent unsafe operation, VCC has an undervoltage lockout, which prevents switching if the internal voltage is too low. See V_{VCC_UVLO} and $V_{VCC\_UVLO\_HYST}$ in the *Electrical Characteristics* table. During start-up, VCC momentarily exceeds the normal operating voltage until VCC_UVLO_HYST is exceeded, then drops to the normal operating voltage. Note that these undervoltage lockout values, when combined with the LDO dropout and while powering the LMR36506-Q1, are used to derive the minimum rising operating voltage and the subsequent falling threshold.

8.3.7 Bootstrap Voltage and $V_{CBOOT-UVLO}$ (CBOOT Terminal)

The driver of the power switch (HS switch) requires bias higher than VIN when the HS switch is turned ON. The capacitor connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT terminal to (SW+VCC). The boot diode is integrated on the LMR36506-Q1 die to minimize physical solution size. A 100 nF capacitor rated for 6.3-V or higher is recommended for CBOOT. The CBOOT rail has a UVLO to protect the chip from operation with too little bias. This UVLO has a threshold of V_{CBOOT_UVLO} and is typically set at 2.1 V. If the CBOOT capacitor is not charged above this voltage with respect to SW, then the part initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

8.3.8 Spread Spectrum

For the LMR36506-Q1, spread spectrum is a factory option. To find which parts have spread spectrum enabled, see the *Device Comparison Table*.

ADVANCE INFORMATION

Feature Description (continued)

The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. In most systems containing the LMR36506-Q1, low-frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics, which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LMR36506-Q1 uses a ±3% spread of frequencies which can spread energy smoothly across the FM and TV bands, but is small enough to limit subharmonic emissions below the switching frequency of the part. Peak emissions at the switching frequency of the part are only reduced slightly, by less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The LMR36506-Q1 uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats at less than 1.5 Hz, which is below the audio band.

The spread spectrum is only available while the clock of the LMR36506-Q1 device is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on-time reaches minimum on-time. See the *Timing Characteristics*.
- The clock is synchronized with an external clock.

8.3.9 Soft Start and Recovery from Dropout

When designing with the LMR36506-Q1, slow rise in output voltage due to recovery from dropout and soft start must be considered a separate phenomena. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection.
- Power is applied to the VIN of the IC or VCC pin, releasing undervoltage lockout.

Once soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a pre-bias start-up.

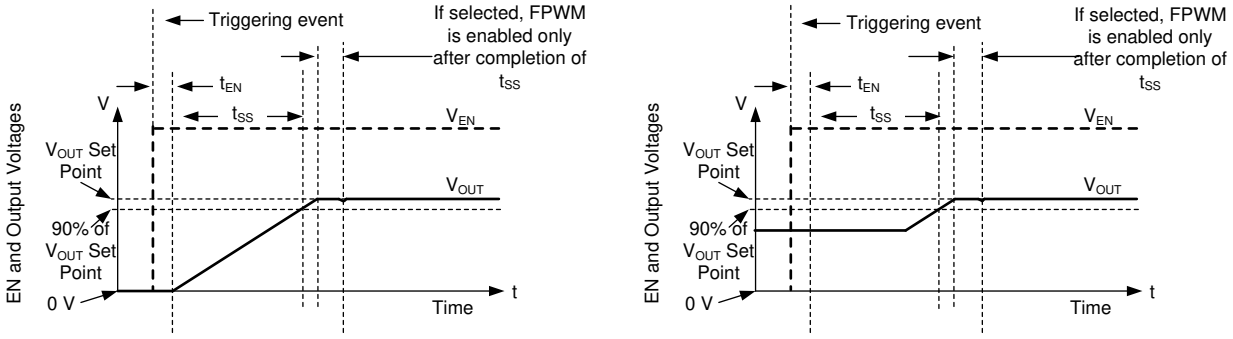


図 5. Soft Start with and without Prebias Voltage

8.3.9.1 Recovery from Dropout

Any time output voltage is more than a few percent low for any reason, output voltage slowly ramps up. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- FPWM mode is allowed during recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMR36506-Q1 can pull down on the output. Note that all protections that are present

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Feature Description (continued)

during normal operation are in place, preventing destruction if output is shorted to a high voltage or ground.

- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. It is not started from zero.

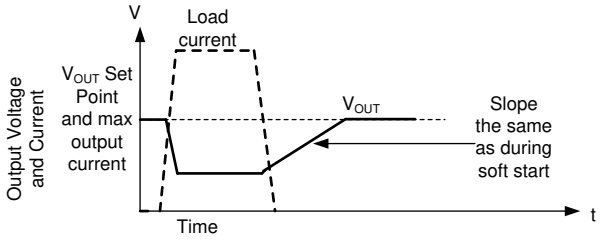

図 6. Recovery from Dropout

Whether output voltage falls due to high load or low input voltage, once the condition that causes output to fall below its set point is removed, output climbs at the same speed as during start-up.

8.3.10 Current Limit and Short Circuit

The LMR36506-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Since the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turnoff commanded by the internal error amplifier loop. In the case of the low-side device, turnoff is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turnoff current is allowed to be. This is called the low-side current limit, $I_{LS-LIMIT}$ (or I_{L-LS} in 図 7). If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not be turned on. The LS switch is turned off once the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

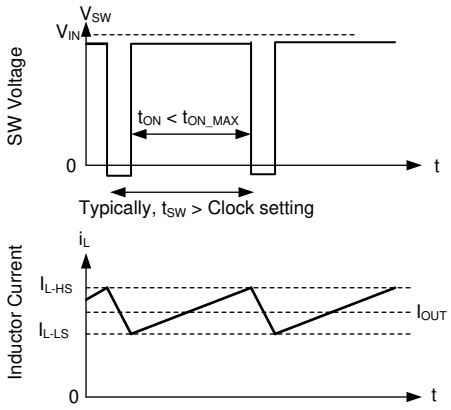

図 7. Current Limit Waveforms

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Feature Description (continued)

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Also, since the current waveform assumes values between I_{SC} (or I_{L-HS} in 図 7) and $I_{LS-LIMIT}$, output current is very close to the average of these two values unless duty factor is very high. Once operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty factor is very high, current ripple must be very low in order to prevent instability. Since current ripple is low, the part is able to deliver full current. The current delivered is very close to $I_{LS-LIMIT}$.

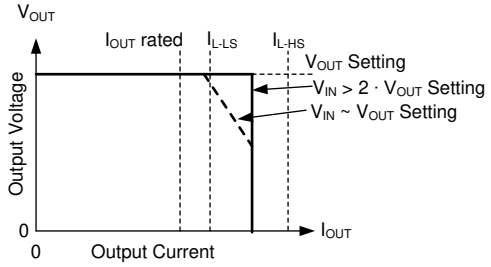

図 8. Output Voltage versus Output Current

Under most conditions, current is limited to the average of I_{L-HS} and I_{L-LS}, which is approximately 1.4 times the maximum-rated current. If input voltage is low, current can be limited to approximately IL-LS. Also note that current does not exceed the average of I_{L-HS} and I_{L-LS}. Once the overload is removed, the part recovers as though in soft start.

8.3.11 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 158°C (typical). When the junction temperature falls below 158°C (typical), the LMR36506-Q1 attempts another soft start.

While the LMR36506-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides ON/OFF control of the device. When the EN pin voltage is below the $V_{EN-WAKE}$ threshold, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the input current drops down to 1 µA (typical).

8.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the regulator. When the EN pin voltage is above the $V_{EN-WAKE}$ threshold but below the precision enable rising threshold for the output voltage, the internal LDO clamps the VCC voltage at 5.5 V typically. The precision enable circuitry is ON once VCC is above its VCC-UVLO. The internal power MOSFET of the SW node remains off unless the voltage on the EN terminal goes above its precision enable threshold. The LMR36506-Q1 also employs undervoltage lockout protection. If the VCC voltage is below its UVLO level, the output of the regulator is turned off.

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Device Functional Modes (continued)

8.4.3 Active Mode

The LMR36506-Q1 is in active mode whenever the EN pin and UVLO high threshold levels are satisfied. The simplest way to enable the operation of any of these devices is to connect the EN pin to VIN, which allows self start-up when the applied input voltage exceeds internal UVLO levels. Refer to the *External UVLO* section and precision enable feature section for details on setting these operating levels.

In active mode, depending on the load current, the LMR36506-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency
- Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple
- Light Load Mode where the parts uses Pulse Frequency Modulation (PFM) and lowers the switching frequency at load under half of $I_{PEAK-MIN}$ to improve efficiency
- Forced Pulse Width Modulation (FPWM) is similar to CCM with fixed switching frequency, but extends the fixed frequency range of operation from full to no load.
- Dropout mode when switching frequency is reduced to minimize drop out
- Recovery from dropout is similar to other modes of operation except the output voltage set point is gradually moved up until the programmed set point is reached.

8.4.4 Continuous Conduction Mode (CCM)

Continuous Conduction Mode (CCM) operation is employed when the load current is higher than a half of the peak-to-peak inductor current. If the load current is decreased, the part enters DCM mode. In CCM operation, the frequency of operation is constant and fixed unless the minimum t_{ON_MIN} or t_{OFF_MIN} are exceeded, which causes the part to enter foldback mode. In both these cases, CCM operation is still maintained, but the frequency of operation is folded back (reduced) to maintain proper regulation.

8.4.5 Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode (DCM) operation is employed when the load current is lower than half of the peak-to-peak inductor current. In DCM operation, also known as Diode Emulation Mode, the LS FET is turned off when the inductor current drops below 0 A to keep operation as efficient as possible by reducing switching losses and preventing negative current conduction.

8.4.6 Pulse Frequency Modulation (PFM)

At light output current loads, Pulse Frequency Modulation (PFM) mode is activated for the highest possible efficiency. When the inductor current does not reach $I_{PEAK-MIN}$ during a switching cycle, the on-time is increased and the switching frequency reduces as needed to maintain proper regulation. The on-time has a maximum value of approximately 8 µs to avoid large output voltage ripple in dropout conditions. Efficiency is greatly improved by reducing switching and gate drive losses. During this mode of operation, the LMR36506-Q1 can convert with a minimum quiescent current of 6.5 µA (typical) when unloaded.

8.4.7 Forced Pulse Width Modulation Mode (FPWM)

The part operates in Forced Pulse Width Modulation (FPWM) mode when the MODE/SYNC pin is pulled high (connected to V_{CC}) or synchronized to an external clock among the MODE/SYNC pin trimmed variants or when the RT pin variants are factory pre-set with the inductor zero cross disabled. In this mode, diode emulation is turned off and the part remains in CCM over the full-load range. In FPWM operation, the frequency of operation is constant and fixed unless the minimum t_{ON_MIN} or t_{OFF_MIN} are exceeded, which causes the part to enter DCM. In these cases, the FPWM operation is still maintained, but the switching frequency is folded back (reduced) in order to maintain proper output voltage regulation.

8.4.8 Dropout Mode

Foldback protection modes are entered when the duty cycle exceeds the minimum on and off times of the part. At very high duty cycles, where the minimum off-time is not satisfied, the frequency folds back to allow more time for the peak current command to be reached. The maximum on-time is 8 µs (typical), which limits the maximum duty cycle in dropout to 98% (typical).

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9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR36506-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 0.6 A. The following design procedure can be used to select components for the LMR36506-Q1.

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All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

9.2 Typical Application

図 9 shows a typical application circuit for the LMR36506-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick-start guide, 表 1 provides typical component values for a range of the most common output voltages.

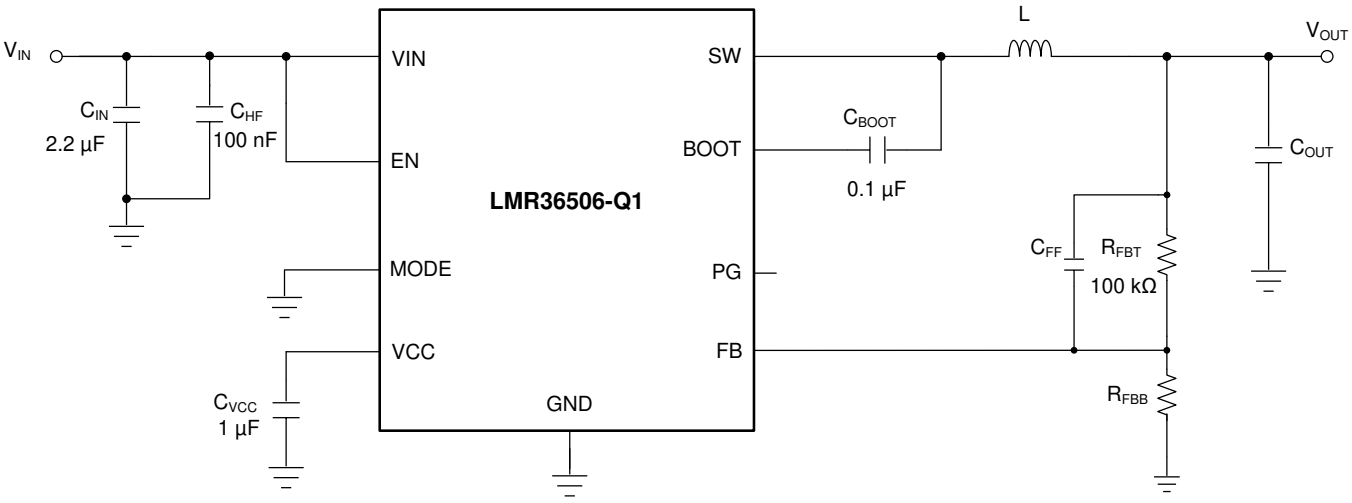

図 9. Example Application Circuit

表 1. Typical External Component Values(1)

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} (RATED CAPACITANCE)	MINIMUM C_{OUT} (RATED CAPACITANCE)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN}	C_{BOOT}	C_{VCC}
400	3.3	33	1 x 47 µF	1 x 22 µF	100 k	43.2 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	3.3	6.8	1 × 22 µF	1 x 10 µF	100 k	43.2 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
400	5	47	1 x 47 µF	1 × 22 µF	100 k	24.9 k	2.2 µF + 1 × 100 nF	100 nF	1 µF
2200	5	6.8	1 × 22 µF	1 x 10 µF	100 k	24.9 k	2.2 µF + 1 × 100 nF	100 nF	1 µF

(1) Inductor values are calculated based on typical V_{IN} = 13.5 V.

9.2.1 Design Requirements

Detailed Design Procedure provides a detailed design procedure based on 表 2.

表 2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5 V (6 V to 60 V)
Output voltage	5 V
Maximum output current	0 A to 0.6 A
Switching frequency	2200 kHz

9.2.2 Detailed Design Procedure

The following design procedure applies to 図 9 and 表 1.

9.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 2200 kHz is used.

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9.2.2.2 Setting the Output Voltage

For the fixed output voltage versions, pin 8 (VOUT/BIAS) of the device must be connected directly to the output voltage node. This output sensing point is normally located near the top of the output capacitor. If the sensing point is located further away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor can be needed at the sensing point.

9.2.2.2.1 FB for Adjustable Output

In an adjustable output voltage version, pin 8 of the device is FB. The output voltage of LMR36506-Q1 is externally adjustable using an external resistor divider network. The range of recommended output voltage is found in the . The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ with a maximum value of 1 MΩ. Once R_{FBT} is selected, 式 2 is used to select R_{FBB}. V_{REF} is nominally 1 V.

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{2}$$

For this 5-V example, R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ.

9.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. 式 3 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 5.96 µH. Select the next standard value of 6.8 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{3}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC}. This ensures that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

9.2.2.4 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. 式 4 can be used to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient. Use as a starting point to determine the required output capacitor for each design.

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$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = ripple factor from *Inductor Selection*

(4)

Once the output capacitor and ESR have been calculated, use 式 5 to check the output voltage ripple.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$

where

- V_r = peak-to-peak output voltage ripple

(5)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 2.2-µF is required on the input of the LMR36506-Q1. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 2.2-µF, 100-V, X7R (or better) ceramic capacitor is chosen. The 100 nF must also be rated at 100-V with an X7R dielectric.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from 式 6 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

(6)

ADVANCE INFORMATION

9.2.2.6 C_{BOOT}

The LMR36506-Q1 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

9.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see the *Power-Good Flag Output* section). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V.

9.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help mitigate this effect. Use 式 7 to estimate the value of C_{FF}. The value found with 式 7 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{7}$$

9.2.2.8.1 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in 図 10. The input voltage at which the device turns on is designated as V_{ON} while the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 8 is used to calculate R_{ENT} and V_{OFF}.

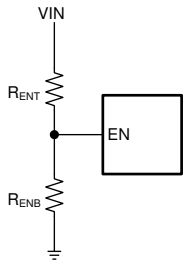

図 10. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN}} \right)$$

where

- V_{ON} = V_{IN} turnon voltage
- V_{OFF} = V_{IN} turnoff voltage

(8)

ADVANCE INFORMATION

9.2.2.9 Maximum Ambient Temperature

As with any power conversion device, the LMR36506-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LMR36506-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 9 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the values given in the *Thermal Information* section are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (9)$$

where

- η = efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

Due to the ultra-miniature size of the VQFN-HR (RPE) package, a DAP is not available. This means that this package exhibits a somewhat greater $R_{\theta JA}$.

Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*

9.3 What to Do and What Not to Do

- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.

ADVANCE INFORMATION

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Specifications* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 10.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (10)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kind of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 11. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 12 shows a recommended layout for the critical components of the LMR36506-Q1.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. Route the SW pin to the N/C pin and used to connect the BOOT capacitor to SW.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
6. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. *Provide enough PCB area for proper heat-sinking.* As stated in the *Maximum Ambient Temperature* section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

ADVANCE INFORMATION

Layout Guidelines (continued)

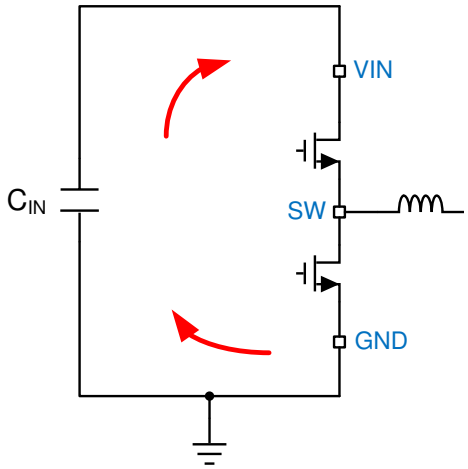

図 11. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET switch and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by using the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10-mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

11.2 Layout Example

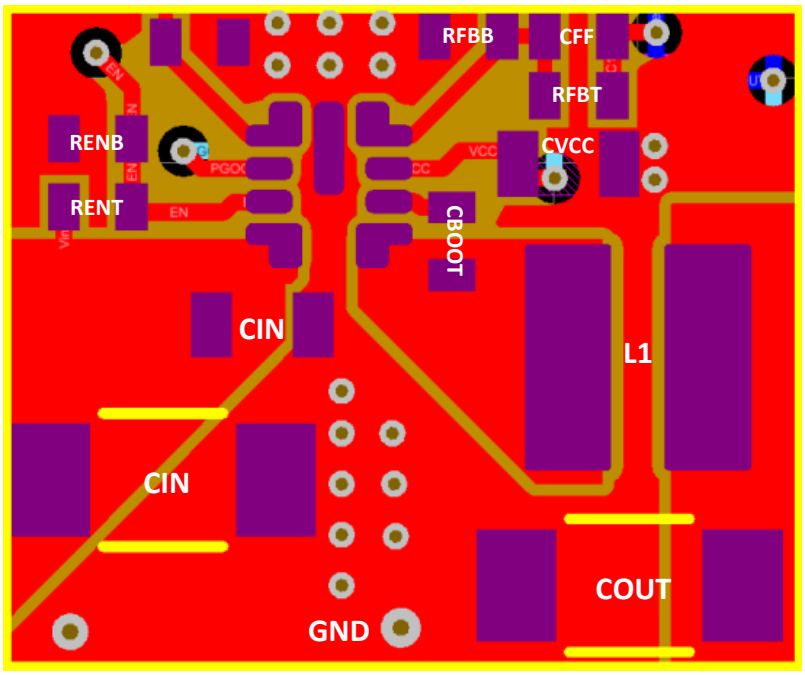

図 12. Example Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『AN-2020 Thermal Design By Insight, Not Hindsight』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ*『AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『Semiconductor and IC Package Thermal Metrics』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『Thermal Design made Simple with LM43603 and LM46002』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『PowerPAD™ Thermally Enhanced Package』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『PowerPAD™ Made Easy』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『Using New Thermal Metrics』アプリケーション・レポート* (英語)
- テキサス・インスツルメンツ、*『AN-1149 Layout Guidelines for Switching Power Supplies』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ*『AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines』アプリケーション・レポート (英語)*
- テキサス・インスツルメンツ、*『Constructing Your Power Supply — Layout Considerations』セミナー (英語)*
- テキサス・インスツルメンツ、*『Low Radiated EMI Layout Made Simple with LM4360x and LM4600x』アプリケーション・レポート (英語)*

12.2 ドキュメントの更新通知を受け取る方法

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12.3 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

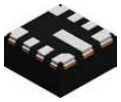
13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

ADVANCE INFORMATION

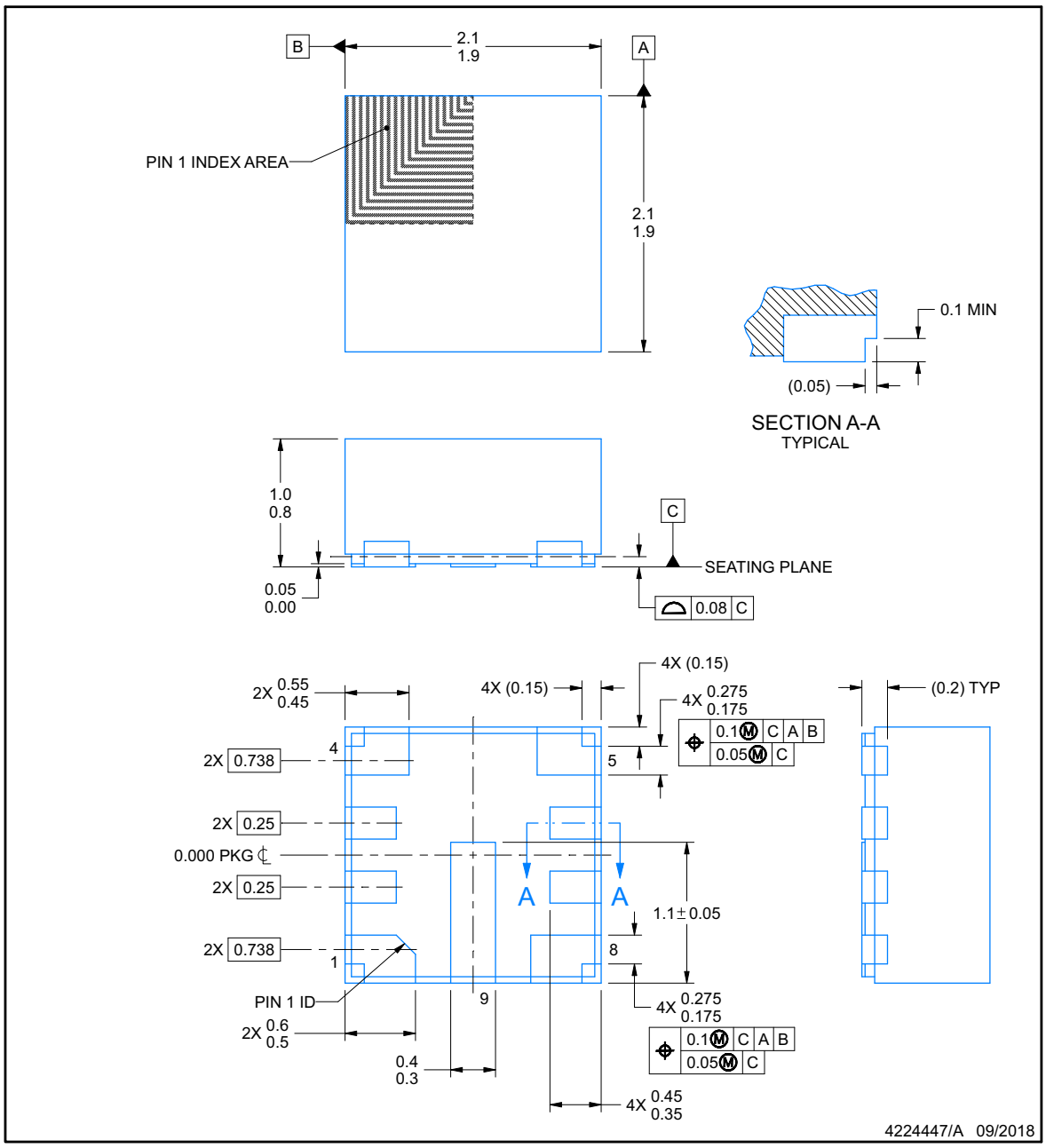
PACKAGE OUTLINE

RPE0009A



VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

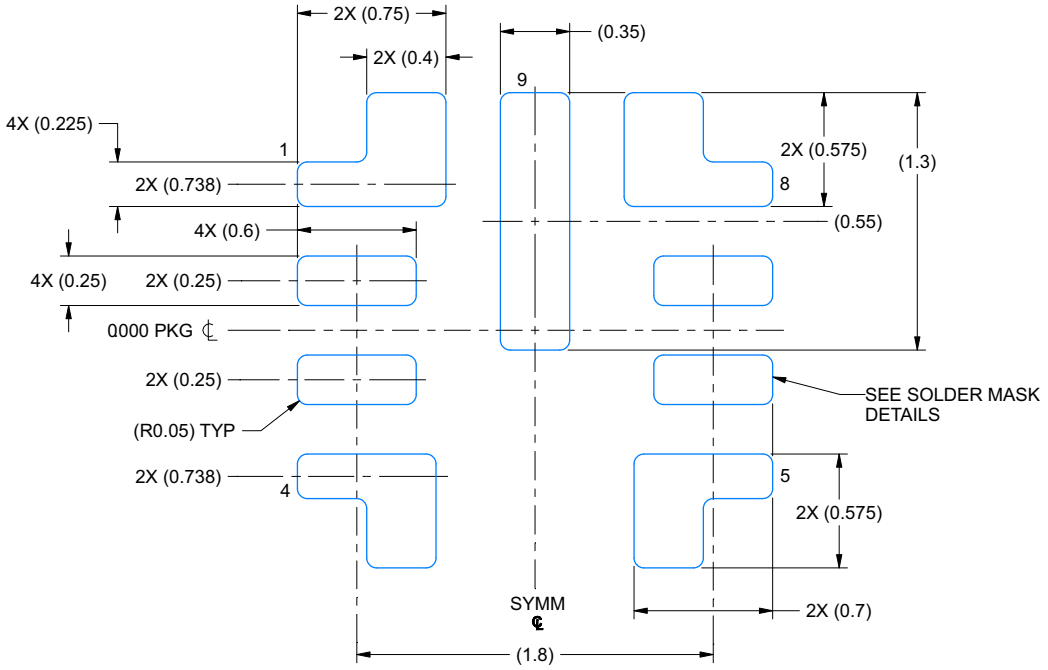
ADVANCE INFORMATION

ADVANCE INFORMATION

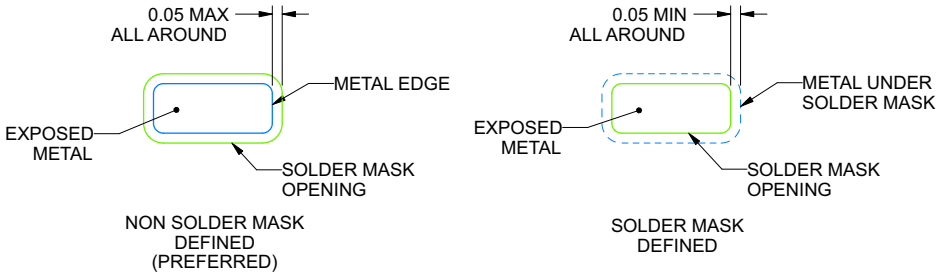
EXAMPLE BOARD LAYOUT

RPE0009A — **VQFN-HR - 1.0 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4224447/A 09/2018

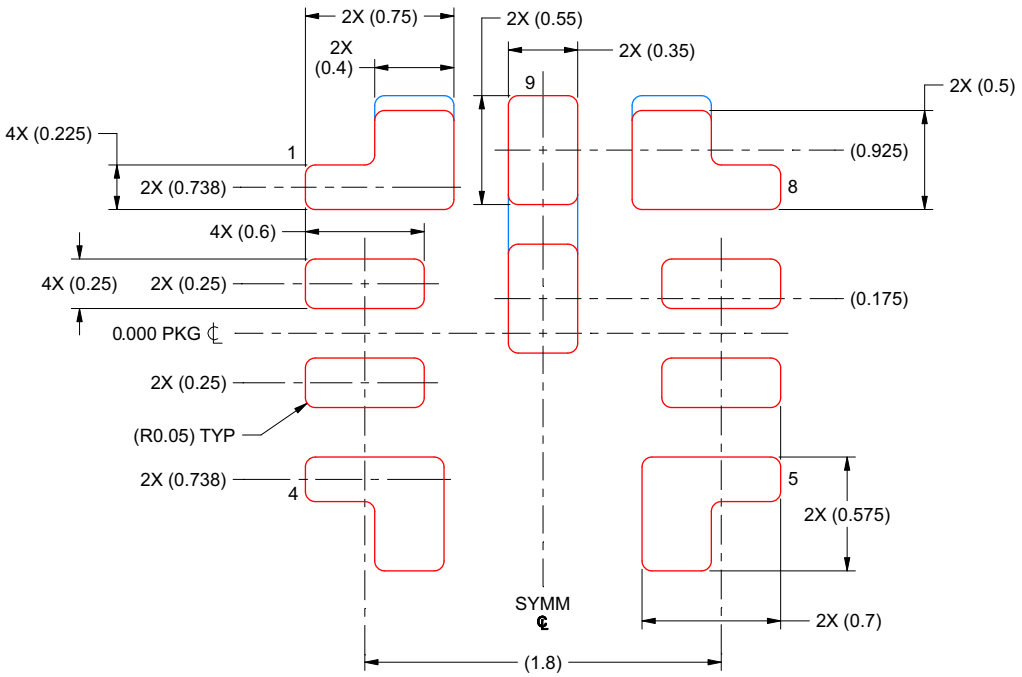
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPE0009A — **VQFN-HR - 1.0 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5 MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR36506MSC3RPERQ1	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	MCCQ	Samples
LMR36506MSC5RPERQ1	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	MCBQ	Samples
LMR36506MSCQRPERQ1	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	MCAQ YMJ	Samples
LMR36506RS3QRPERQ1	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	MCDQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMR36506-Q1 :

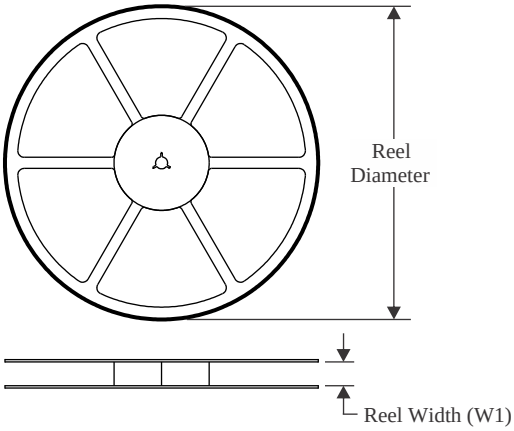
- Catalog : LMR36506

NOTE: Qualified Version Definitions:

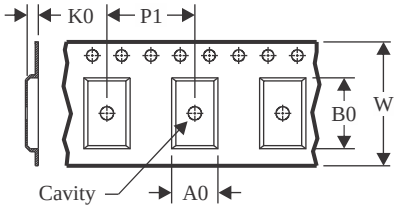
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

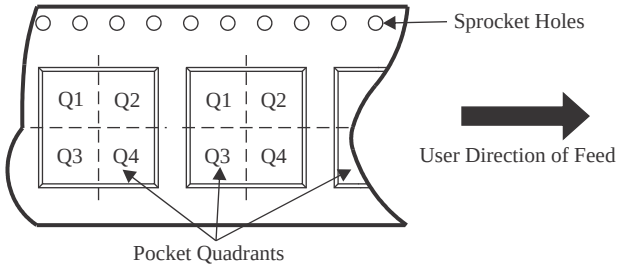


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

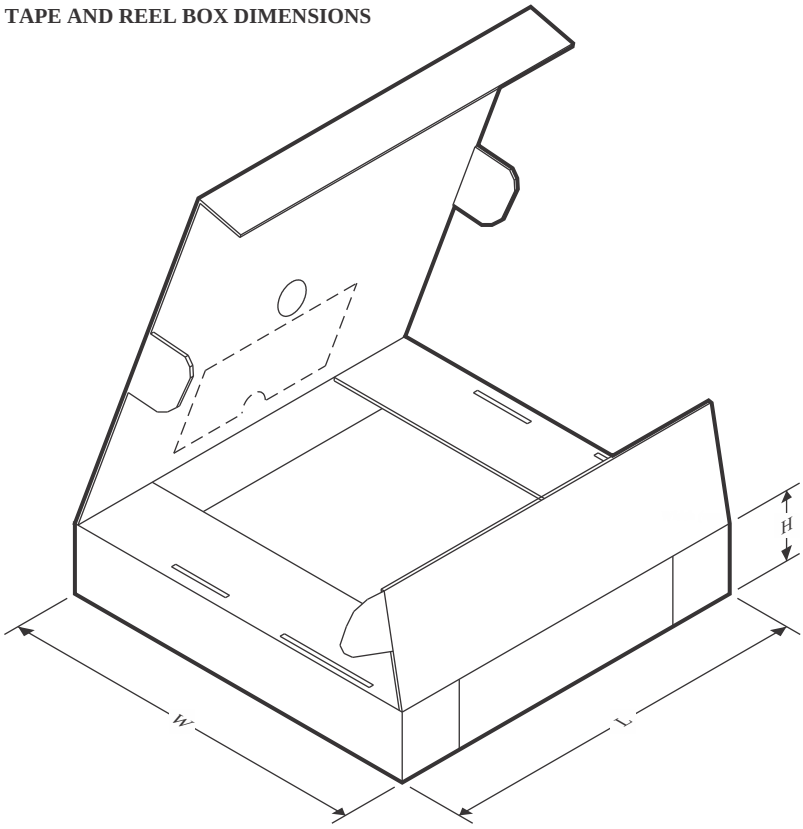
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR36506MSC3RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36506MSC5RPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36506MSCQRPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
LMR36506RS3QRPERQ1	VQFN-HR	RPE	9	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR36506MSC3RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36506MSC5RPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36506MSCQRPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0
LMR36506RS3QRPERQ1	VQFN-HR	RPE	9	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

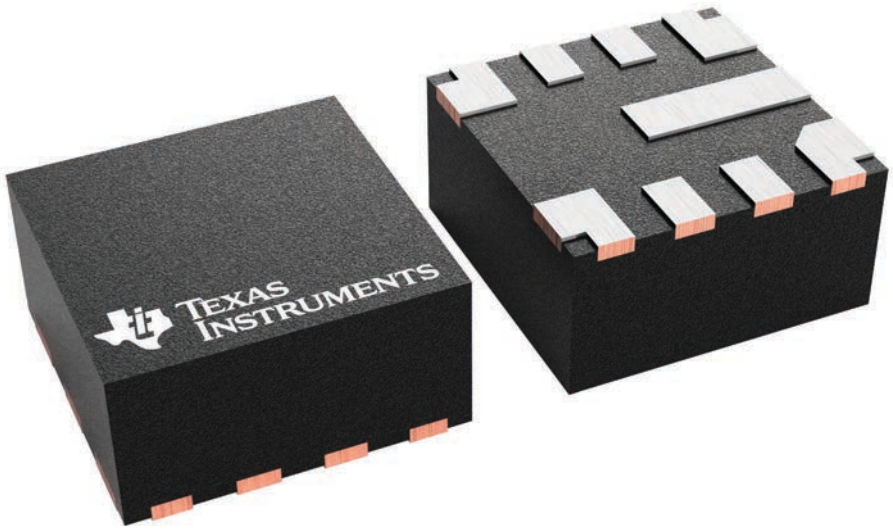
RPE 9

VQFN-HR - 1.0 mm max height

2 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



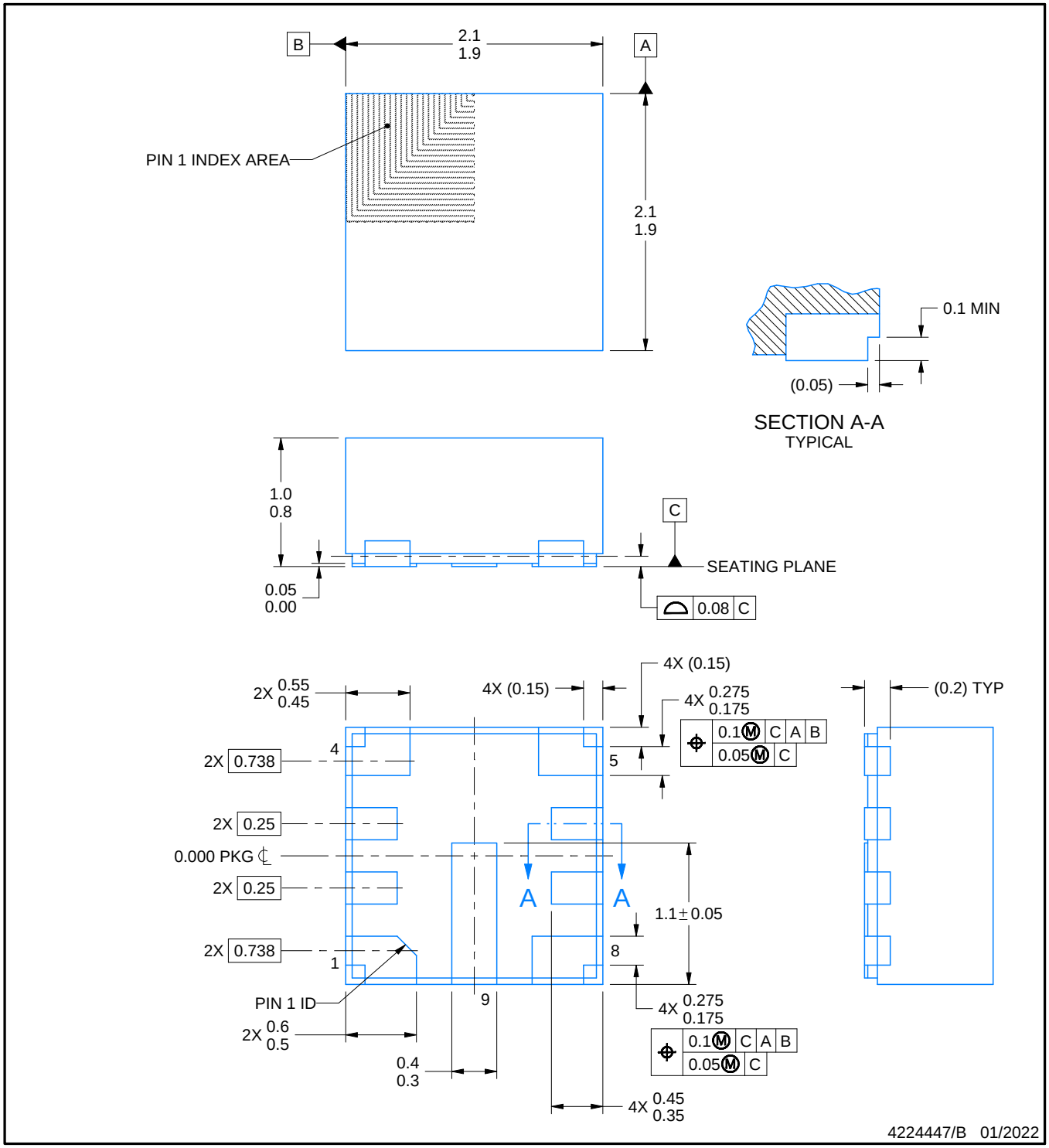
4227057/A

PACKAGE OUTLINE

RPE0009A

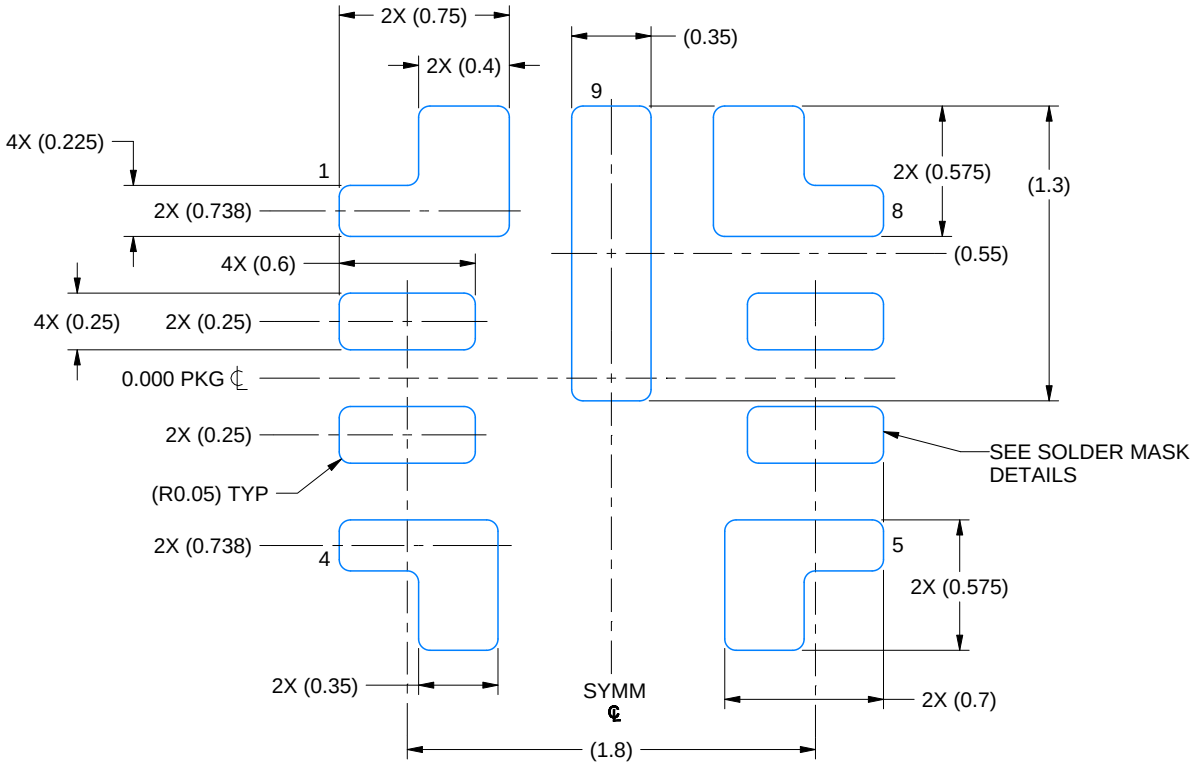
VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

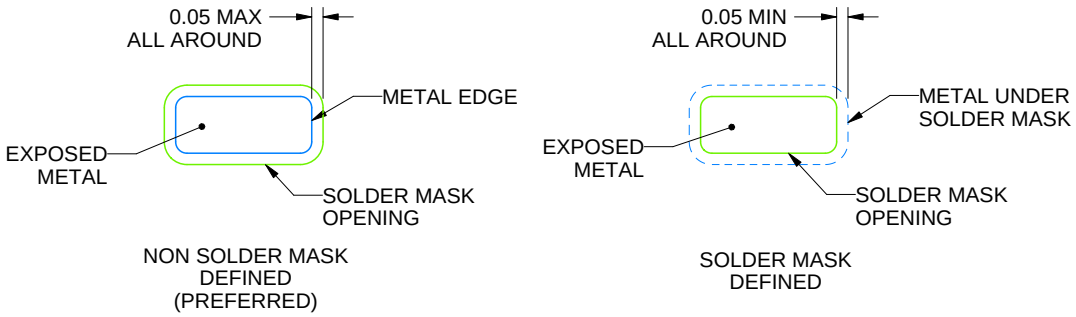


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4224447/B 01/2022

NOTES: (continued)

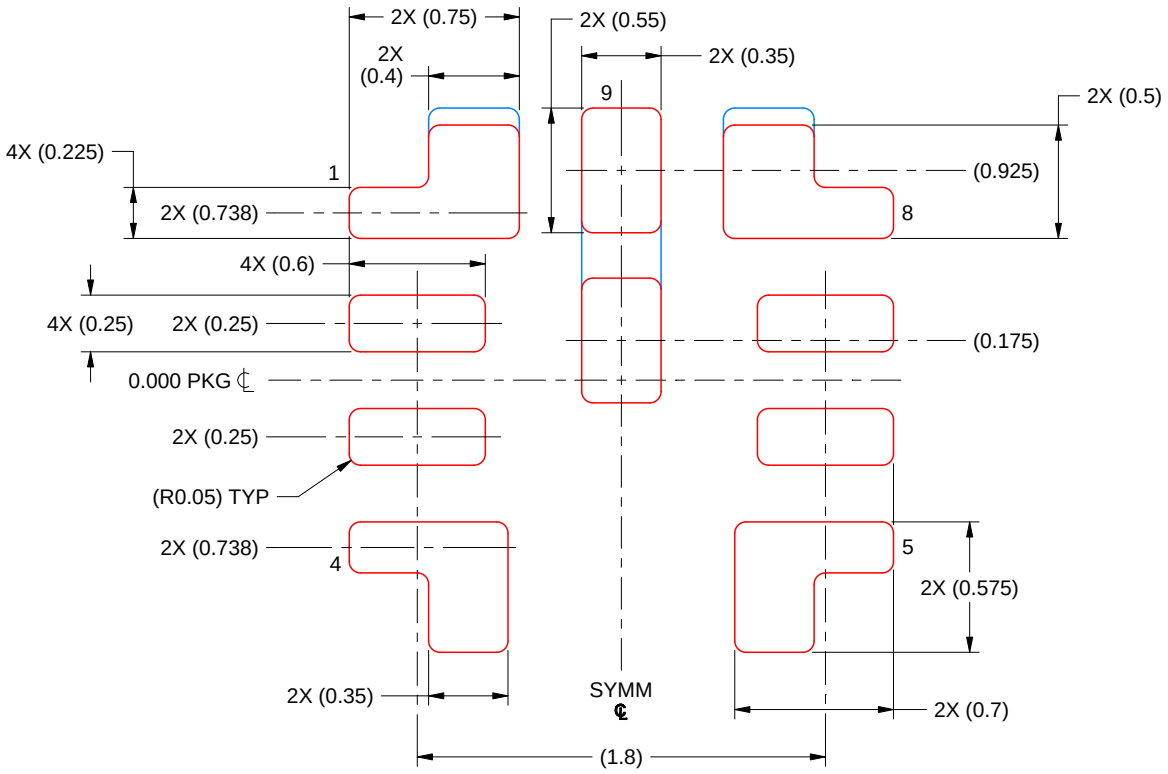
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPE0009A

VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5 MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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