LMX1205 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider

1 Features

- Output frequency: 300MHz to 12.8GHz
- Noiseless adjustable input delay up to 60ps with 1.1ps resolution
- Individual adjustable output delays up to 55ps with 0.9ps resolution
- Ultra-low noise
  - Noise floor: –159dBc/Hz at 6GHz output
  - Additive jitter (DC to f_{CLK}): 36fs
  - Additive jitter (100Hz to 100MHz): 10fs
- Four high-frequency clocks with corresponding SYSREF outputs
  - Shared divide by 1 (Bypass), 2, 3, 4, 5, 6, 7, and 8
  - Shared programmable multiplier x2, x3, x4, x5, x6, x7 and x8
- LOGICLK output with corresponding SYSREF output
  - On separate divide bank
  - 1, 2, 4 pre-divider
  - 1 (bypass), 2, …, 1023 post divider
  - Second logic clock option with additional divider 1, 2, 4 & 8
- Six programmable output power levels
- Synchronized SYSREF clock outputs
  - 508 delay step adjustments of less than 2.5ps at 12.8GHz
  - Generator, repeater and repeater retime modes
  - Windowing feature for SYSREFREQ pins to optimize timing
- SYNC feature to all divides and multiple devices
- Operating voltage: 2.5V
- Operating temperature: –40ºC to +85ºC

2 Applications

- Test & Measurement:
  - Oscilloscope
  - Wireless equipment testers
  - Wideband digitizers
- Aerospace & Defense:
  - Radar
  - Electronic warfare
  - Seeker Front end
  - Munitions
  - Phase array antenna / Beam forming
- General Purpose:
  - Data converter clocking
  - Clock buffer distribution / division

3 Description

The high frequency capability, extremely low jitter and programmable clock input and output delay of this device, makes a great approach to clock high precision, high-frequency data converters without degradation of signal-to-noise ratio. Each of the four high frequency clock outputs and additional LOGICLK outputs with larger divider range, is paired with a SYSREF output clock signal. The SYSREF signal for JESD204B/C interfaces can either be internally generated or passed in as an input and re-clocked to the device clocks. The noiseless delay adjustment at input path of the high frequency clock input and individual clock output paths insures low skew clocks in multi-channel system. For data converter clocking application, having the jitter of the clock less than the aperture jitter of the data converter is important. In applications where more than four data converters need to be clocked, a variety of cascading architectures can be developed using multiple devices to distribute all the high frequency clocks and SYSREF signals required. This device, combined with an ultra-low noise reference clock source, is an exemplary choice for clocking data converters, especially when sampling above 3GHz.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMX1205	RHA (VQFN, 40)	6mm × 6mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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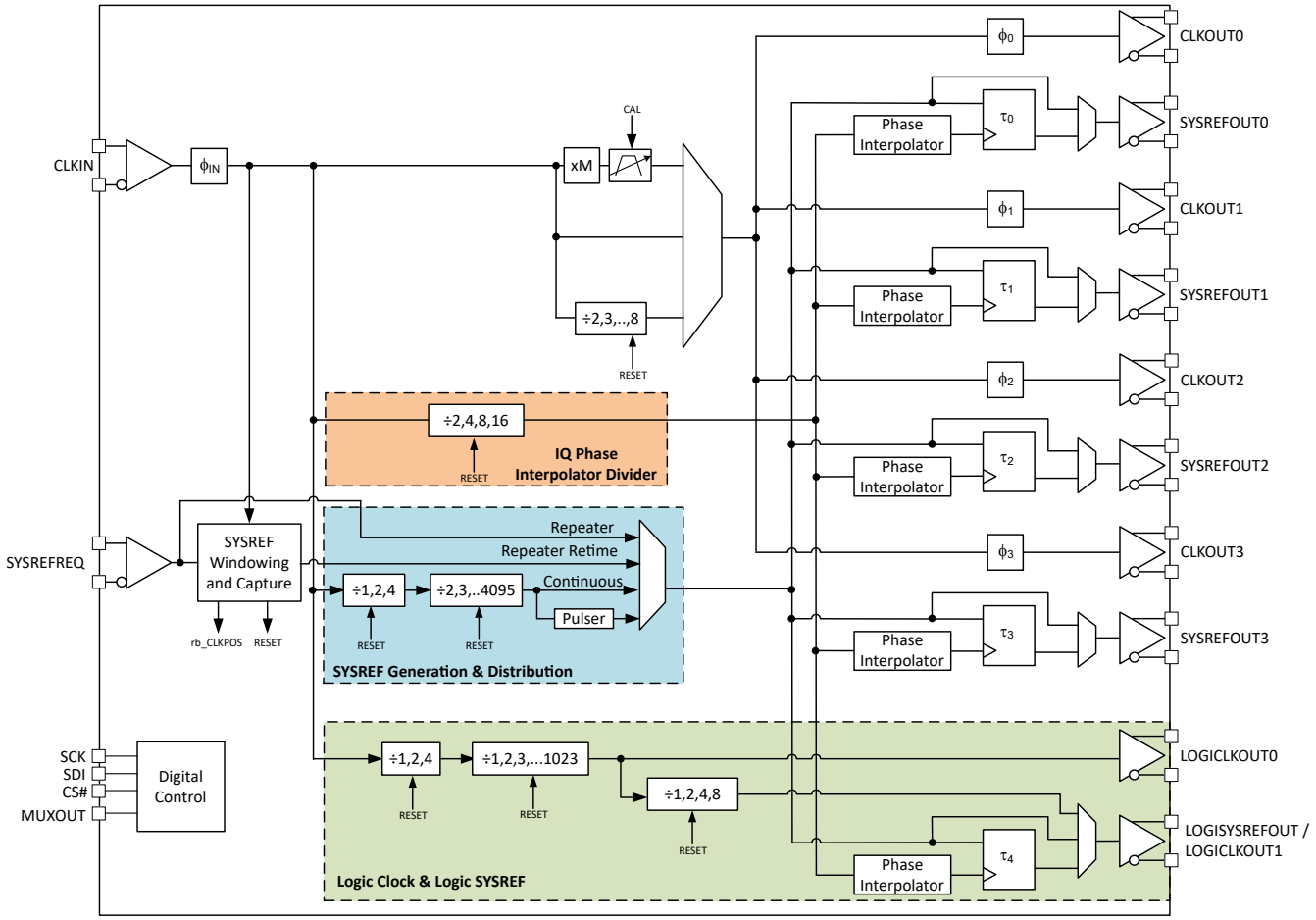

Block Diagram

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4 Pin Configuration and Functions

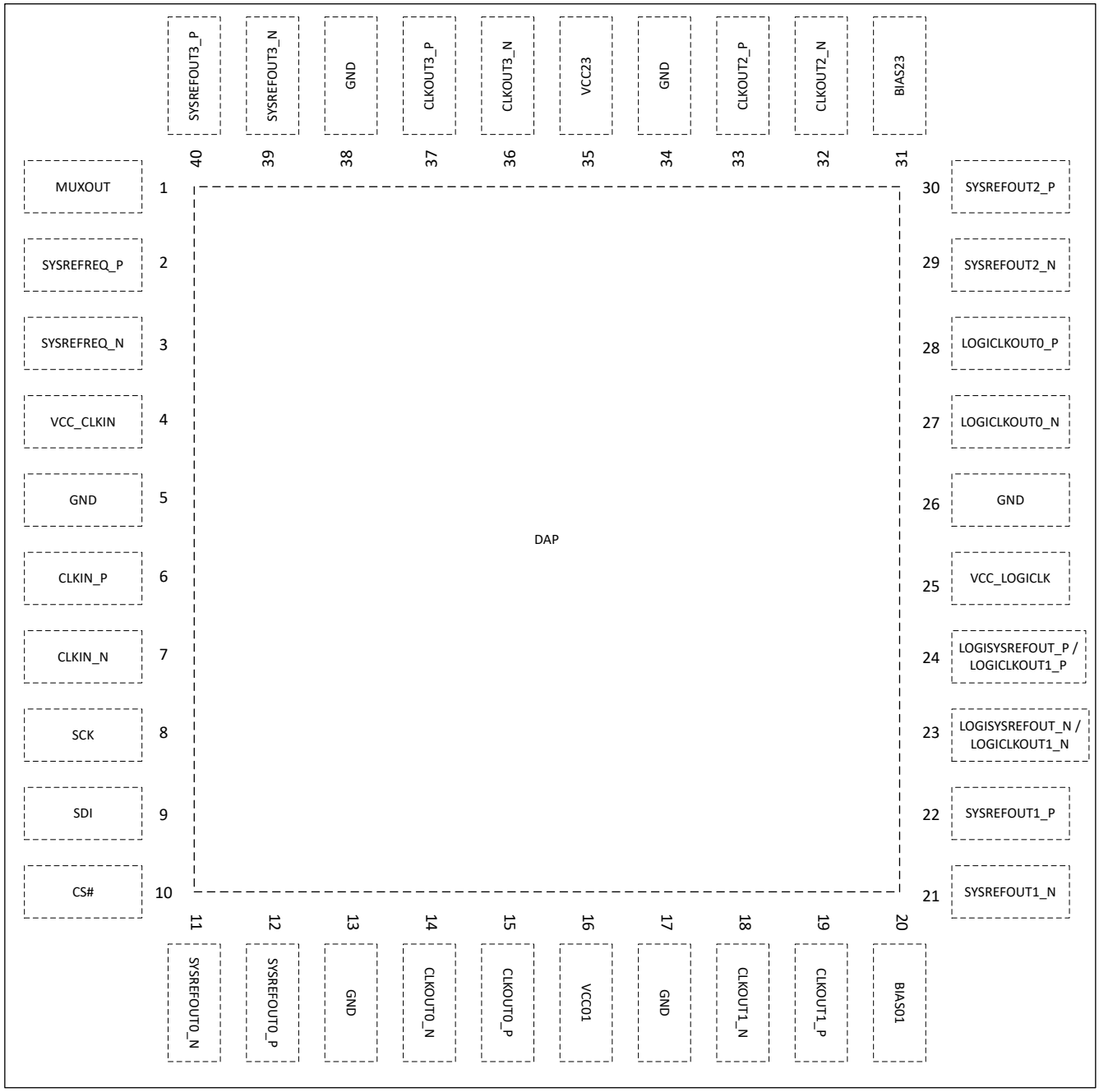

Figure 4-1. RHA Package 40-Pin VQFN Top View

Table 4-1. Pin Functions

NAME	NO.	TYPE(1)	DESCRIPTION
BIAS01	20	BYP	If not using the multiplier, this pin can be left open. If using the multiplier, bypass this pin to GND with a 10nF capacitor for optimal noise performance.
BIAS23	31	BYP	If not using the multiplier, this pin can be left open. If using the multiplier, bypass this pin to GND with a 10µF and 0.1µF capacitor for optimal noise performance.
CLKIN_N	7	I	Differential clock input pair. Internal 50Ω termination at each pin. AC-couple with a capacitor appropriate to the input frequency (typically 0.1µF or smaller). If using single-ended, provide the input at CLKIN_N pin and terminate unused CLKIN_P with a series AC-coupling capacitor and 50Ω resistor to GND.
CLKIN_P	6		
CLKOUT0_N	14	O	Differential clock output pairs. Each pin is an open-collector output with internally integrated 50Ω resistor with programmable output swing. AC coupling is required. The pin expects 100Ω differential load or 50Ω load at each pin.
CLKOUT0_P	15		
CLKOUT1_N	18		
CLKOUT1_P	19		
CLKOUT2_N	32		
CLKOUT2_P	33		
CLKOUT3_N	36		
CLKOUT3_P	37		
CS#	10	I	SPI chip select. High impedance CMOS input. Accepts up to 3.3V. This pin requires 200Ω resistor in series.
DAP	DAP	GND	Ground these pins.
GND	5,13,17,26,34,38		
LOGICLKOUT0_N	27	O	Differential Logic clock output pair. Selectable CML or LVDS format. LVDS format has programmable common-mode voltage. CML format requires external pull resistors.
LOGICLKOUT0_P	28		
LOGISYSREFOUT_N / LOGICLKOUT1_N	23	O	Differential Logic clock output pair. Selectable CML or LVDS format. LVDS format has programmable common-mode voltage. CML format requires external pull resistors.
LOGISYSREFOUT_P / LOGICLKOUT1_P	24		
MUXOUT	1	O	Multiplexed pin serial data readback and lock status of the multiplier.
SCK	8	I	SPI clock. High impedance CMOS input. Accepts up to 3.3V. This pin requires 200Ω resistor in series.
SDI	9	I	SPI data input. High impedance CMOS input. Accepts up to 3.3V. This pin requires 200Ω resistor in series.
SYSREFREQ_N	3	I	Differential SYSREF request input for JESD204B/C support. Internal 50Ω termination at each pin. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2V to 2V.
SYSREFREQ_P	2		
SYSREFOUT0_N	11	O	Differential SYSREF CML output pairs for JESD204B/C support. Supports AC and DC coupling with programmable common-mode voltage of 0.5V to 1.5V. The pin expects a 100Ω differential load.
SYSREFOUT0_P	12		
SYSREFOUT1_N	21		
SYSREFOUT1_P	22		
SYSREFOUT2_N	29		
SYSREFOUT2_P	30		
SYSREFOUT3_N	39		
SYSREFOUT3_P	40		
VCC_CLKIN	4	PWR	Connect to a 2.5V supply. Recommend a shunt high frequency capacitor (typically 0.1µF or smaller) closest to the pin in parallel with larger capacitors (typically 1µF and 10µF).
VCC_LOGICLK	25		
VCC01	16		
VCC23	35		

(1) BYP = Bypass; GND = Ground; I = Input; O = Output; PWR = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Power supply voltage	–0.3	2.75	V
V_{IN}	DC Input Voltage (SCK, SDI, CSB)	GND	3.6	V
V_{IN}	DC Input Voltage (SYSREFREQ)	GND	V_{DD} + 0.3	V
V_{IN}	AC Input Voltage (CLKIN)		V_{DD}	Vpp
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.4	2.5	2.6	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

SYMBOL	THERMAL METRIC(1)	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ TA ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Consumption							
I_{CC}	Supply Current (1)	Powered up, all Clock outputs and SYSREFs on			1130		mA
		Powered up, all Clock outputs on, all SYSREF off			700		
		Powered up, all Clock outputs and SYSREF off			370		
		Powered down			13.5		
I_{ADD}	Additive output current	OUTx_PWR = 6			64		mA
	Multiplier current	Divide, CLK_DIV = 8			60		
		Multiplier, CLK_MULT = x8			360		
	SYSREF current	Running at 100MHz Generation mode, all outputs on			425		
	LOGICLK current	LOGICLK enabled with LOGISYSREF			85		
SYSREF							
f_{SYSREF}	SYSREF output frequency	Generator mode	Generator mode			200	MHz
f_{SYSREF}	SYSREF output frequency	Repeater mode	Repeater mode			100	MHz
T_{SYNC}	Pulse width required for SYNC signal	Tsync = 6xT of f_{CLKIN} , f_{CLKIN} = 6GHz		1000			ps
Δt	SYSREF delay step size	Δt = SYSREF_DLY_DIV/ (508 x f_{CLKIN}), f_{CLKIN} = 12.8GHz			3		ps
t_{RISE}	Rise time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		65		ps
			LVDS		120	175	ps
t_{FALL}	Fall time (20% to 80%)	SYSREFOUT			45		ps
		LOGISYSREFOUT	CML		65		ps
			LVDS		120	175	ps
V_{OD}DIFF	Differential pk-pk output voltage	SYSREFOUT, SYSREFx_PWR = 4, SYSREFx_VCM = 10			0.9		Vpp
		LOGISYSREFOUT	CML		0.9		Vpp
			LVDS		0.7		Vpp
$V_{SYSREFCM}$	Common mode voltage	SYSREFOUT	CML SYSREFx_VCM=41 , 100Ω Differential Load	1.35	1.5	1.65	V
			CML SYSREFx_VCM=4, 100Ω Differential Load	0.45	0.5	0.55	V
		LOGISYSREFOUT	LVDS 100Ω Differential Load	0.75		1.4	V
SYSREFREQ Pins							
$V_{SYSREFIN}$	Differential pk-pk Voltage input range	AC differential voltage		0.8		2	Vpp
$V_{SYSREFIN}$	Single-ended voltage input range	AC Coupled to SYSREFREQ_P; SYSREFREQ_N AC coupled to GND	AC Coupled to SYSREFREQ_P; SYSREFREQ_N AC coupled to GND	0.6		1.7	Vpp
V_{CM}	Input common mode voltage	Differential 100Ω Termination, DC coupled Set externally		1.2	1.3	2	V
Clock Input							

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2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ TA ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{IN}	Input frequency			0.3		12.8	GHz
P_{IN}	Input power	Single-ended power at CLKIN_P or CLKIN_N		0		10	dBm
ϕ_{IN}	Input delay range				60		ps
Δ_{IN}	Input delay programmable step				1.1		ps
Clock Outputs							
f_{OUT}	Output frequency	Divide-by-2		0.15		6.4	GHz
f_{OUT}	Output frequency	Buffer Mode		0.3		12.8	
f_{OUT}	Output frequency	Multiplier Mode		6.4		12.8	
f_{OUT}	Output frequency	LOGICLK output		1		800	MHz
t_{CAL}	Calibration-time	Multiplier calibration time	f_{IN} = 6.4GHz; x2 f_{SMCLK} = 28 MHz		750		µs
p_{OUT}	Output power	Single-Ended	$f_{CLKLOUT}$= 6GHz OUTx_PWR = 6		4.8		dBm
t_{RISE}	Rise time (20% to 80%)	f_{CLKOUT} = 300 MHz			45		ps
t_{FALL}	Fall time (20% to 80%)	f_{CLKOUT} = 300 MHz			45		ps
$V_{LOGICLKCM}$	Common mode voltage	LOGICLKOUT0	LVDS	0.7	1.2	1.5	V
ϕ_{IN}	Output delay range				55		ps
$\Delta\phi_{IN}$	Output delay programmable step size				0.9		ps
Propagation Delay and Skew							
| t_{SKEW} |	Magnitude of skew between outputs	CLKOUTx to CLKOUTy, not LOGICLK			1	10	ps
| t_{SKEW} |	Magnitude of skew between CLKOUT and SYSREF	SYSREF Continuous/ Pulse Mode	SYSREF delay gen bypass		60		ps
| t_{SKEW} |	Magnitude of skew between CLKOUT and SYSREF	SYSREF Repeater retime Mode	SYSREF delay gen bypass		100		ps
$\Delta t_{DLY}/\Delta T$	Propagation delay variation over temperature	Buffer mode		0.02	0.06	0.10	ps/°C
t_{DLY}	Propagation delay	Buffer mode	T_A = 25°C		165		ps
		Divider Mode			175		ps
		Multiplier Mode			155		ps
t_{DLY}	Propagation delay	SYSREF out Repeater mode	T_A = 25°C		185		ps
Noise, Jitter, and Spurs							
σ_{CLKOUT}	CLKOUT Additive jitter	Additive Jitter. 100Hz to 100MHz integration bandwidth.	Buffer Mode		10		fs, rms
			x2 Multiplier		21		
			x3 Multiplier		25		
			x4 Multiplier		33		
			x5 Multiplier		35		
			x6 Multiplier		48		
			x7 Multiplier		50		
			x8 Multiplier		60		
$1/f_{CLKOUT}$	1/f flicker noise	Slew Rate > 8 V/ns, f_{CLK}=6GHz	Buffer Mode		–154		dBc/Hz
NF_{CLKOUT}	Noise Floor	f_{OUT} = 6.4GHz; f_{Offset} =100MHz	Buffer Mode		–159		dBc/Hz
			Divide-by-2		–158.5		
			Multiplier (x2,x3,x4,x5,x6,x7,x8)		–159.5		

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2.4 V ≤ VCC ≤ 2.6 V, –40°C ≤ TA ≤ +85°C. Typical values are at VCC = 2.5 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$NF_{LOGICLK}$	Noise Floor	LOGICLK output, 300 MHz	CML		–150.5		dBc/Hz
			LVDS		–151.5		
H2	Second harmonic	Buffer Mode f_{OUT}=6.4GHz	Differential		–25		dBc
			Single-Ended		–15		
		Divide by 2 f_{OUT}=6.4GHz	Single-Ended		–17		
$H_{1/M}$	Input clock leakage spur	f_{OUT} = 12GHz (differential)	x2 (f_{SPUR} = 6GHz)		–40		dBc
		f_{OUT} = 12GHz (differential)	x3 (f_{SPUR} = 4GHz)		–40		
		f_{OUT} = 12GHz (differential)	x4 (f_{SPUR} = 3GHz)		–50		
		f_{OUT} = 12GHz (differential)	x6 (f_{SPUR} = 2GHz)		-50		
		f_{OUT} = 10GHz (differential)	x5 (f_{SPUR} = 2GHz)		-50		
		f_{OUT} = 10.5GHz (differential)	x7 (f_{SPUR} = 1.5GHz)		-52		
		f_{OUT} = 12GHz (differential)	x8 (f_{SPUR} = 1.5GHz)		-55		
$P_{crosstalk}$	LOGICLK to CLKOUT	f_{SPUR} = 300MHz (differential)			–70		dBc
	SYSREFOUT to CLKOUT	Generation mode			-70		dBc
		repeater mode			-65		dBc
P_{LEAK}	CLKIN to CLKOUT Leakage in Buffer Mode	Differential Input			-70		dBc
Digital Interface (SCK, SDI, CS#, MUXOUT)							
V_{IH}	High-level input voltage	SCK, SDI, CS#		1.4		3.3	V
V_{IL}	Low-level input voltage			0		0.4	
V_{OH}	High-level output voltage	I_{OH} = 5mA		1.4		Vcc	
		I_{OH} = 0.1mA		2.2		Vcc	
V_{OL}	Low-level output voltage	I_{OL} = 5mA				0.45	
I_{IH}	High-level input current			–42		42	µA
I_{IL}	Low-level input current			–25		25	

(1) Unless Otherwise Stated, f_{CLKIN}=6.4GHz, CLK_MUX=Buffer, All clocks on with OUTx_PWR=6, SYSREFREQ_MODE=1

5.6 Timing Requirements

			MIN	NOM	MAX	UNIT
Timing Requirements						
f_{SPI}	SPI Read/Write Speed				20	MHz
t_{CE}	Clock to enable low time		20			ns
t_{CS}	Clock to data wait time		10			ns
t_{CH}	Clock to data hold time		5			ns
t_{CWH}	Clock pulse width high		10			ns
t_{CWL}	Clock pulse width low		10			ns
t_{CES}	Enable to clock setup time		15			ns
t_{EWH}	Enable pulse width high		15			ns
t_{CD}	Falling clock edge to data wait time		40			ns

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5.7 Timing Diagram

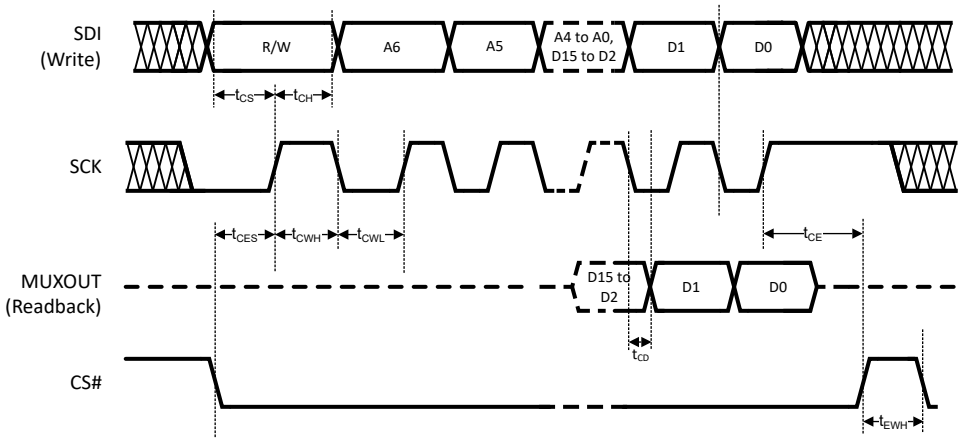

Figure 5-1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CS# must be held low for data to be clocked. The device ignores clock pulses if CS# is held high.
- Recommended SPI settings for this device are CPOL=0 and CPHA=0.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CS# line high on the device that is not to be clocked.

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin remains tri-stated for the address portion of the transaction.
- The data on MUXOUT is clocked out at the falling edge of SCK. In other words, the readback data is available at the MUXOUT pin t_{CD} after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.
- The MUXOUT pin is automatically enabled during the readback transaction. After readback activity is over, it is automatically tri-stated. MUXOUT pin has dual functionality in multiplier mode, as multiplier lock status is also indicated on MUXOUT pin. When sharing the SPI bus readback pin with other devices, make sure to set LD_DIS=1, if readback is required in multiplier mode.
- If READBACK_CTRL is set to 0, the values read back even for R/W bits are not always the value written but rather an internal device state that takes into account the programmed value as well as other factors, such as pin states.

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5.8 Typical Characteristics

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

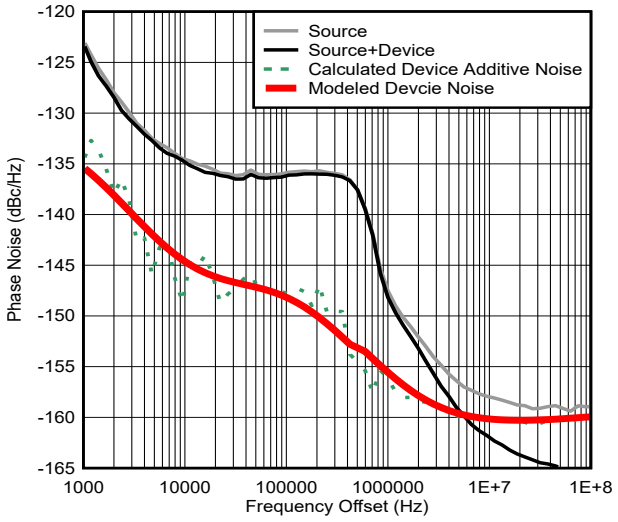


Figure 5-2. Phase Noise Plot in Buffer Mode at 6.4GHz Output

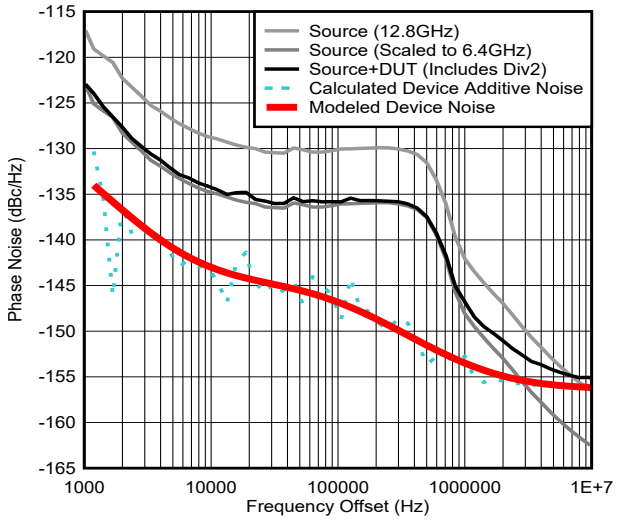


Figure 5-3. Phase Noise Plot in Divider Mode at 6.4GHz Output

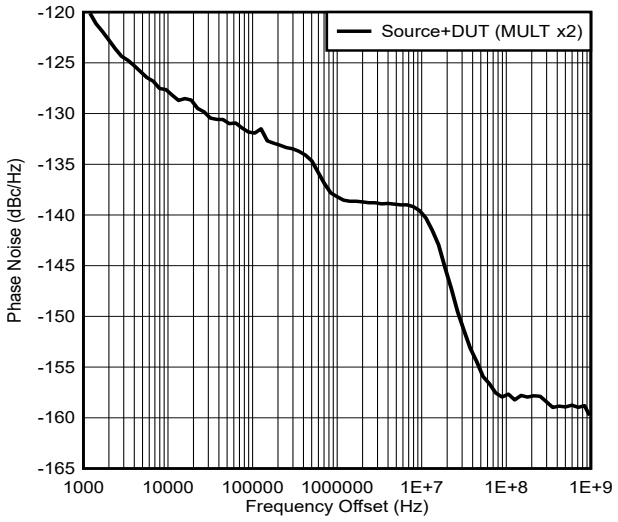


Figure 5-4. Phase Noise Plot in Multiplier Mode at 6.4GHz Output

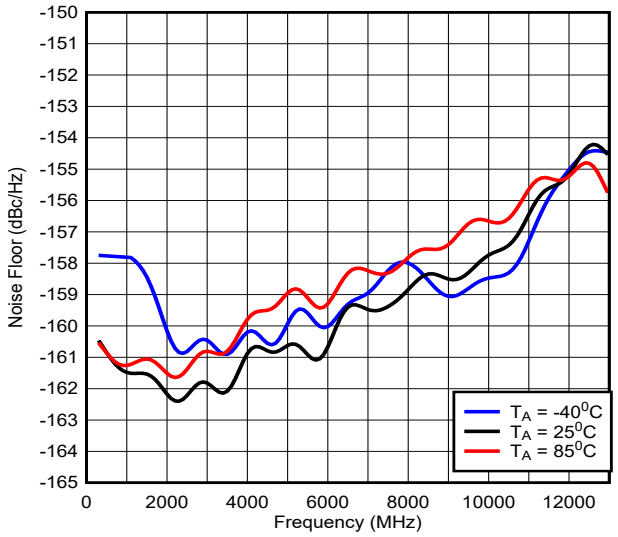


Figure 5-5. Noise Floor in Buffer Mode

ADVANCE INFORMATION

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

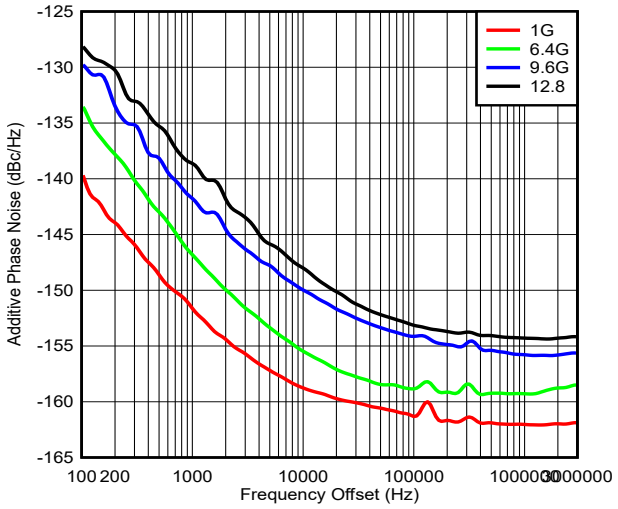
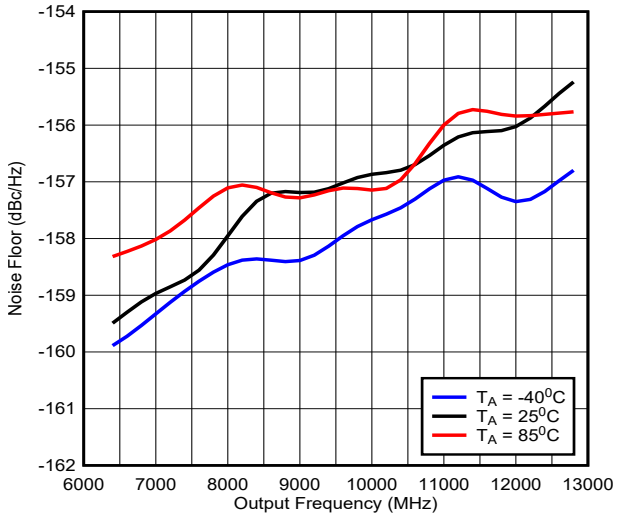
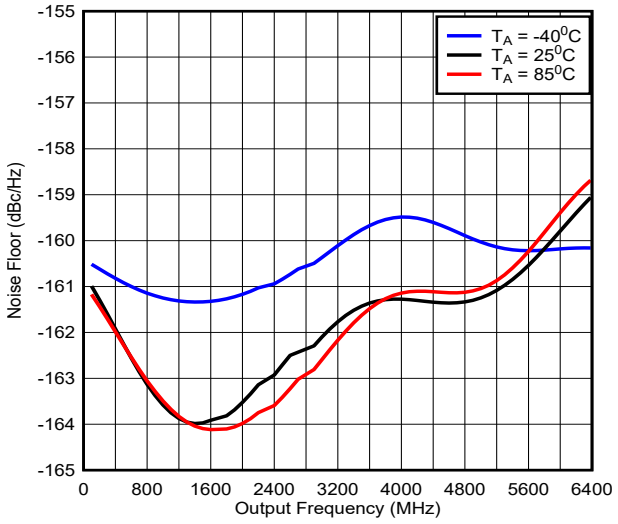


Figure 5-6. Flicker Noise in Buffer Mode



Multiplier value x2

Figure 5-7. Noise Floor in Multiplier Mode



Divider value - 2

Figure 5-8. Noise Floor in Divider Mode

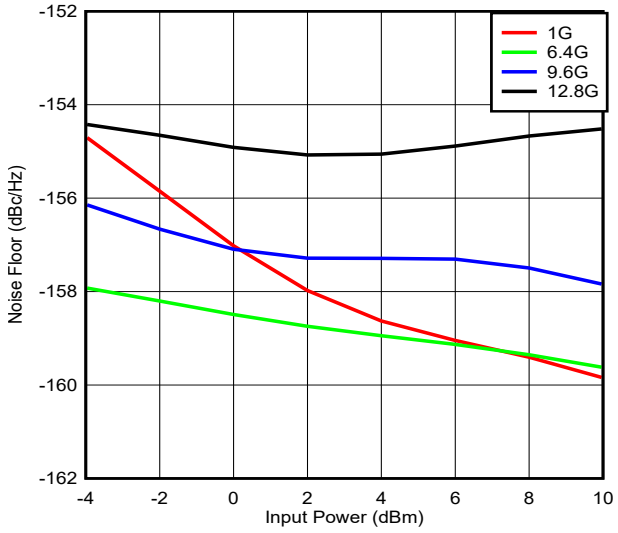


Figure 5-9. Noise Floor in Buffer Mode

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

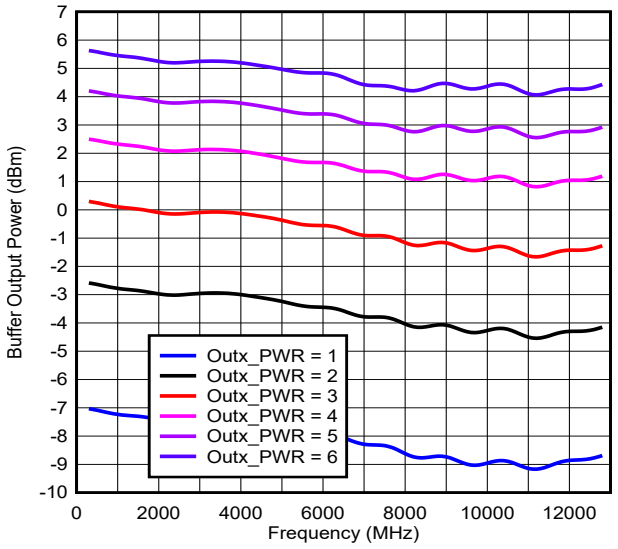


Figure 5-10. Single-Ended Output Power

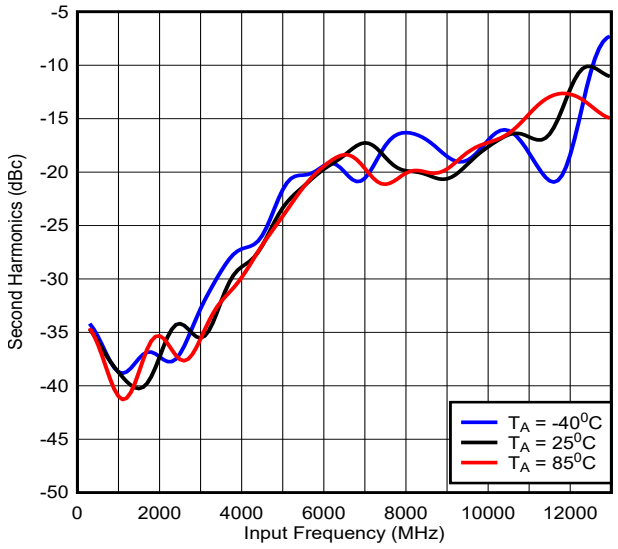
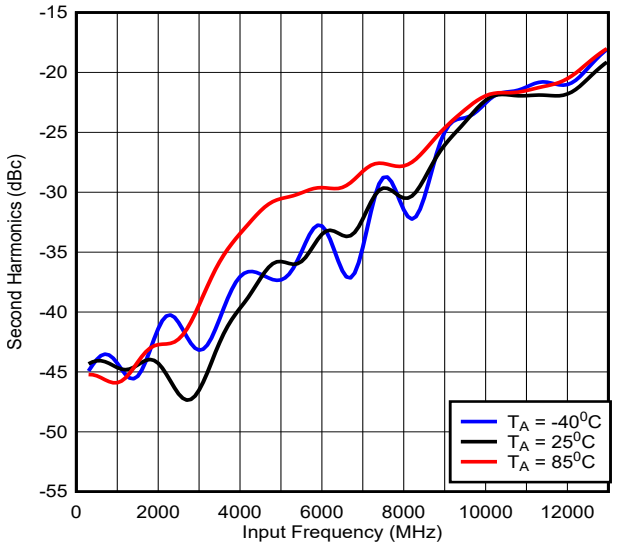
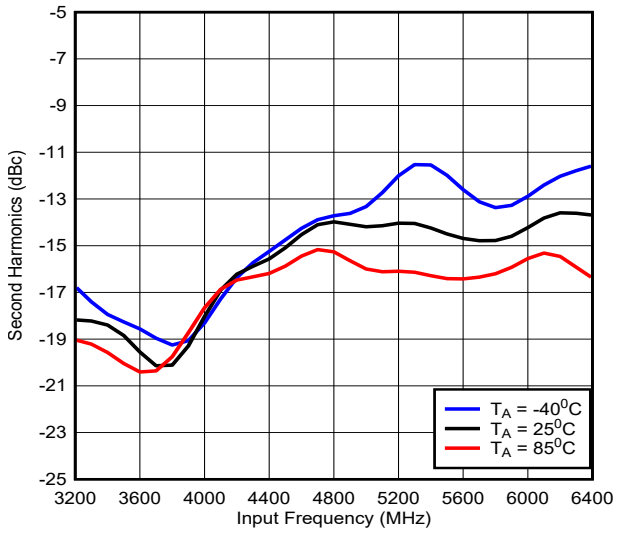


Figure 5-11. Second Harmonic in Buffer Mode



Divider value: by2

Figure 5-12. Second Harmonic in Divider Mode



Multiplier value: x2

Figure 5-13. Second Harmonic in Multiplier Mode

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5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

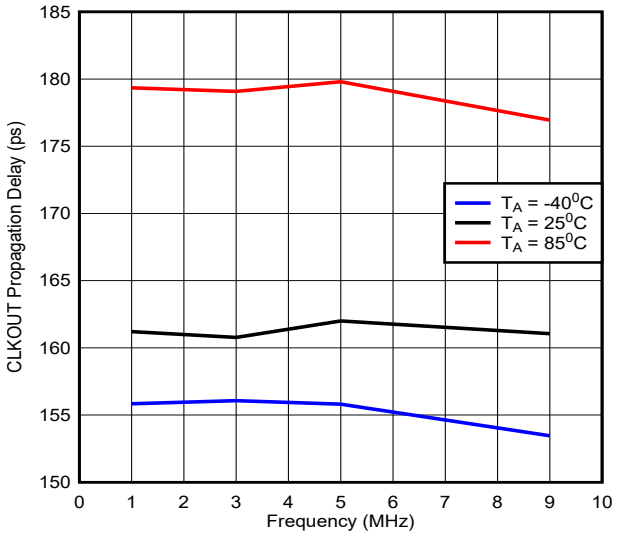


Figure 5-14. CLKOUT Propagation Delay in Buffer Mode

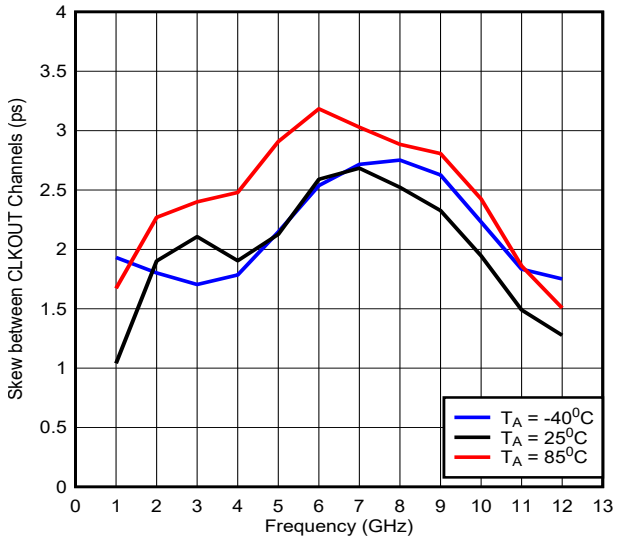


Figure 5-15. Skew Between CLKOUT Channels

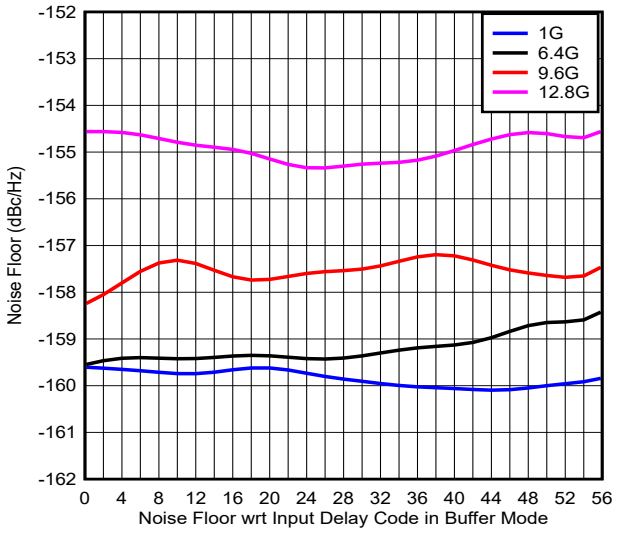


Figure 5-16. Noise Floor wrt Input Delay Code in Buffer Mode

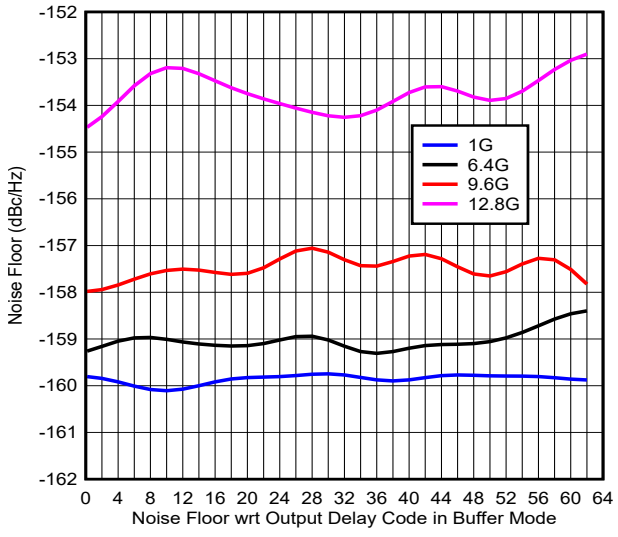


Figure 5-17. Noise Floor wrt Output Delay Code in Buffer Mode

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

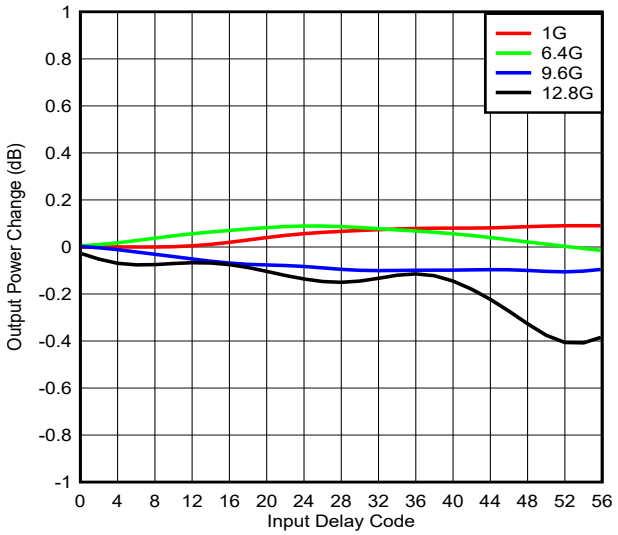


Figure 5-18. Output Power wrt Input Delay Code

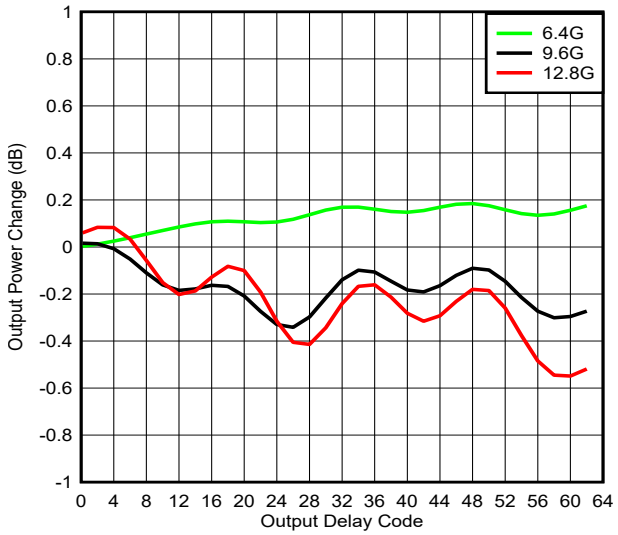
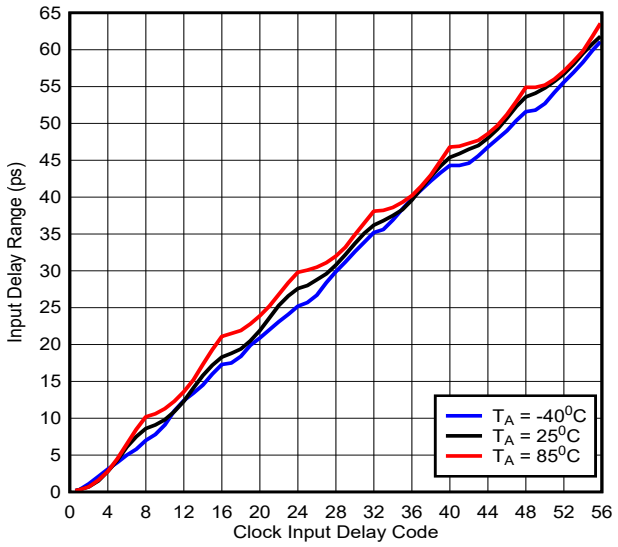
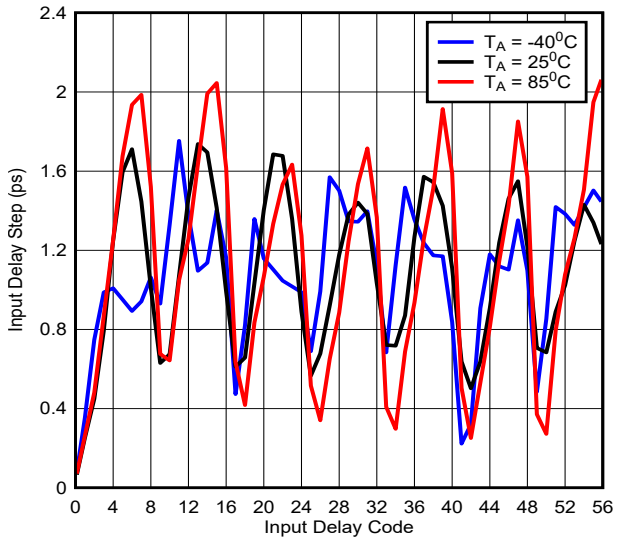


Figure 5-19. Output Power wrt Output Delay Code



CLKIN Frequency = 9GHz

Figure 5-20. Clock Input Delay Range



CLKIN Frequency = 9GHz

Figure 5-21. Clock Input Delay Step Size

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5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.

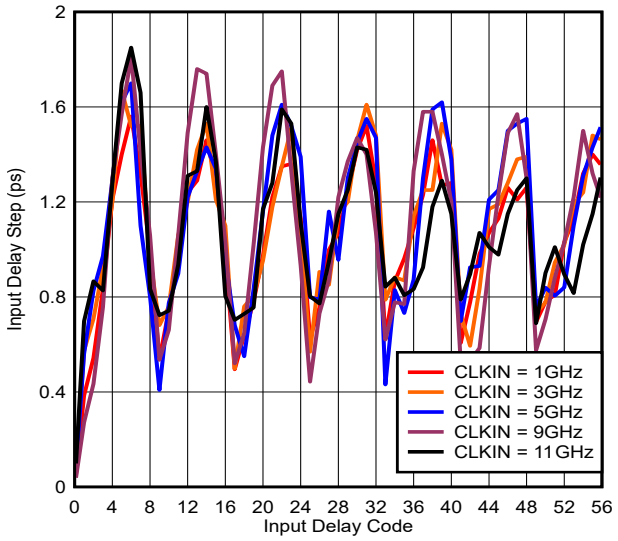


Figure 5-22. Clock Input Delay Step Size

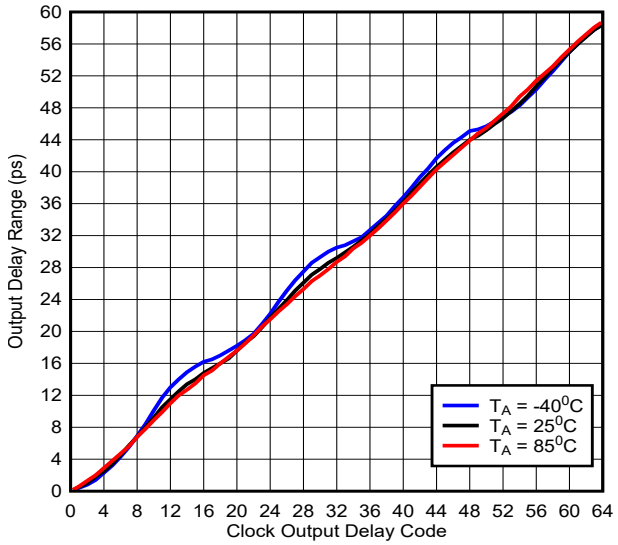


Figure 5-23. Clock Output Delay Range

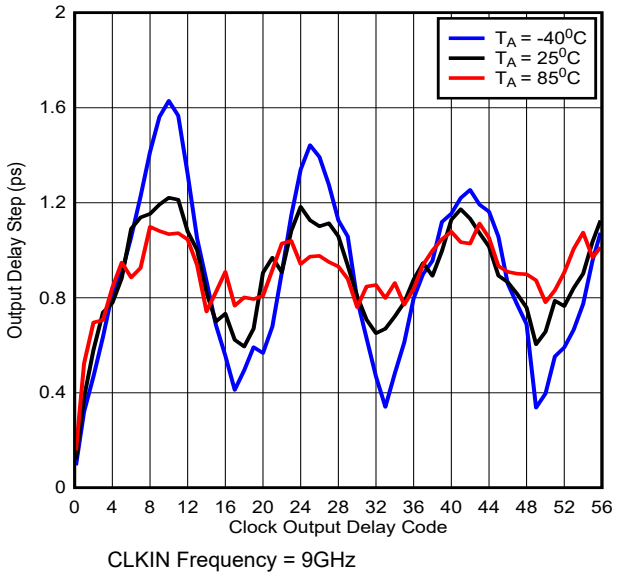


Figure 5-24. Clock Output Delay Step Size

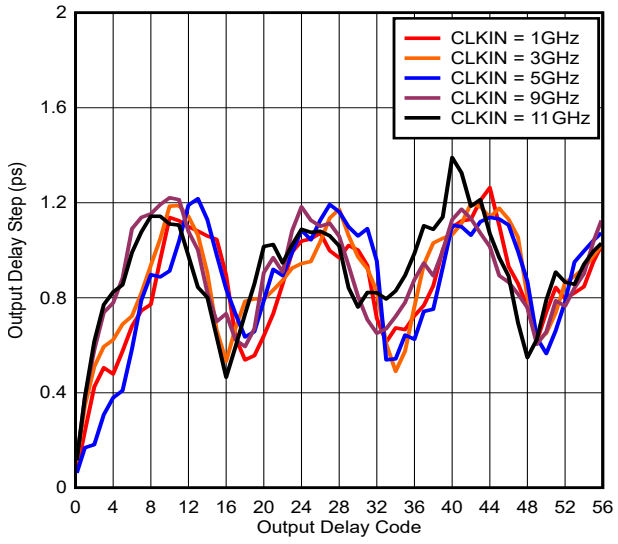
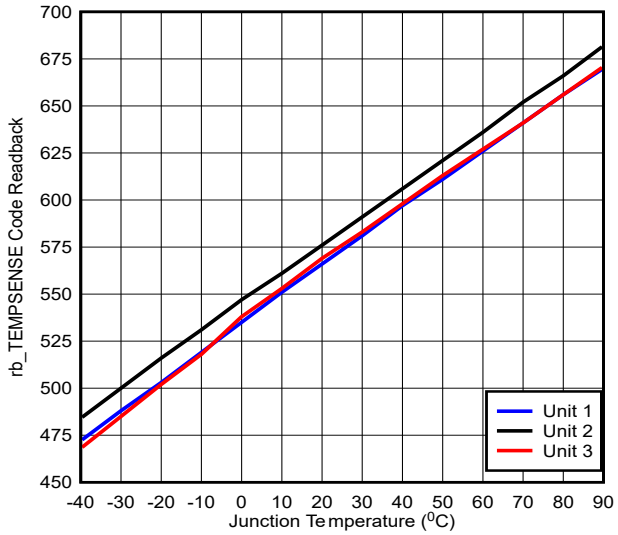


Figure 5-25. Clock Output Delay Step Size

5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5V, OUTx_PWR=6, CLKIN_N driven single ended with 10dBm at pin. Signal source used is SMA100B with ultra-low noise option B711. Phase noise analyzer is FSWP50.



Measured in power-down mode to make Junction Temperature = Ambient Temperature

Figure 5-26. Temperature Sensor Readback

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6 Detailed Description

6.1 Overview

The LMX1205 has four main clock outputs and one LOGICLK output. The main clock outputs are all the same frequency. This frequency can be the same, divided, or multiplied relative to the input clock. Each of these clock outputs has independent programmable power level. The LOGICLK output frequency can be divided or same frequency as clock input and has programmable output format (CML and LVDS) and power level. Second LOGICLK can be generated at LOGISYSREF output pin with the additional division of 1, 2, 4 and 8 at the LOGICLK0 path.

The SYSREF can be generated by either repeating the input from the SYSREFREQ pins, or internally generated. There is an internal SYSREF windowing feature that allows the internal timing of the device to be adjusted to optimize setup/hold times of the SYSREFREQ input with respect to the CLKIN input. This feature requires that the delay between the SYSREF edge and the next rising clock edge is consistent. Each of the five outputs has a corresponding SYSREF output that has individual programmable delays and programmable common mode. For the LOGISYSREF output, the output format is programmable as CML and LVDS.

6.1.1 Range of Dividers and Multiplier

Frequency dividers allow the main and LOGICLK outputs to be a divided value of the input clock. SYSREF dividers are used to divide the input clock for purposes of SYSREF generation and delays. The multiplier allows the output clocks to be a higher frequency than the input clock.

Table 6-1. Range of Dividers and Multiplier

CATEGORY			RANGE	COMMENTS
Main Clocks	Buffer			
	Divider		2, 3, 4, 5, 6, 7, 8	Odd divides (except 1) do not have 50% duty cycle
	Multiplier		2, 3, 4, 5, 6, 7, 8	
LOGICLK	Divide	PreDivide	1, 2, 4	TotalDivide = PreDivide × Divide0 Odd divides (except 1) do not have 50% duty cycle Logic CLK2 TotalDivide = PreDivide x Divide0 x Divide1
		Divide0	1, 2, 3, … 1023	
		Divide1	1, 2, 4, 8	
SYSREF	Divide for frequency generation	PreDivide	1,2, 4	Pre-divides clock for SYSREF generation. TotalDivide = PreDivide×Divide Odd divides do not have 50% duty cycle
		Divide	2, 3, 4,… 4095	
	Divide for delay generation	Divide	2, 4, 8, 16	This divide is for phase interpolator and set according to the input frequency.

6.2 Functional Block Diagram

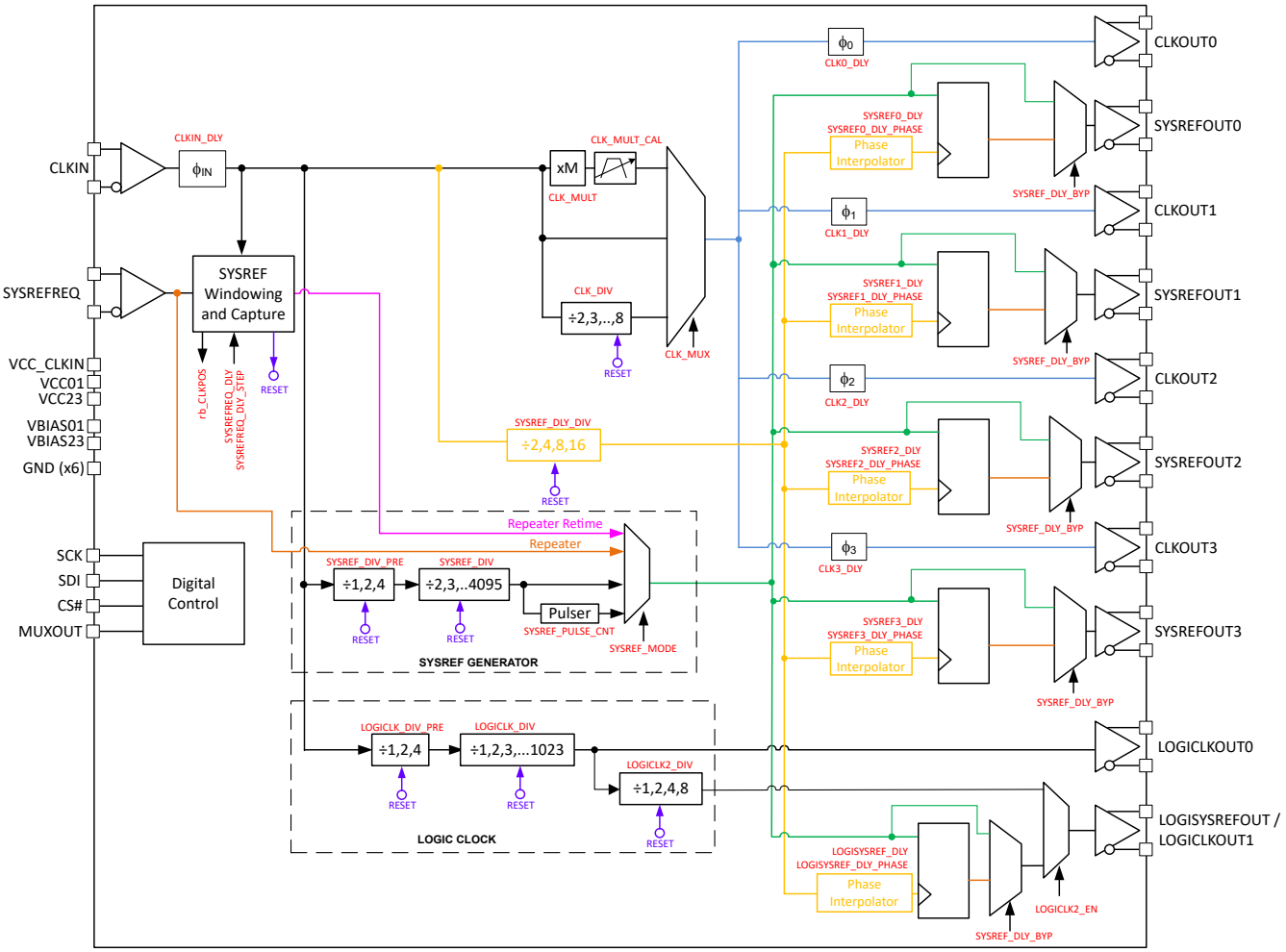

Figure 6-1. Functional Block Diagram

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6.3 Feature Description

6.3.1 Power On Reset

When the device is powered up, the power on reset (POR) resets all registers to a default state as well as resets all state machines and dividers. For the power on reset state, all SYSREF outputs are disabled and all the dividers are bypassed; the device functions as a 4-output buffer. Users must wait 100µs after the power supply rails before programming other registers to verify that the RESET is finished. If the power on reset happens when there is no device clock present, the device functions properly, however, the current changes once an input clock is presented.

\Performing a software power on reset by writing RESET=1 in the SPI bus is both possible and generally good practice. The RESET bit self-clears once any other register is written to. The SPI bus can be used to override these states to the desired settings.

Although the device does have an automatic power on reset, the device can be impacted by different ramp rates on the different supply pins, especially in the presence of a strong input clock signal. Performing a software reset after POR is recommended. This reset can be done by programming RESET=1. The reset bit can be cleared by programming any other register or setting RESET back to zero. Even at maximum allowed SPI bus speed, the software reset event always completes before the subsequent SPI write.

6.3.2 Temperature Sensor

The junction temperature can be read back for purposes such as characterization or to make adjustments based on temperature. Such adjustments can include adjusting CLKx_PWR to make the output power more stable or using external or digital delays to compensate for changes in propagation delay over temperature.

The junction temperature is typically higher than the ambient temperature due to power dissipation from the outputs and other functions on the device. Equation 1 shows the relationship between the code read back and the junction temperature.

$$\text{Temperature} = 0.65 \times \text{Code} - 351 \quad (1)$$

Equation 1 is based on a best-fit line created from three devices from slow, nominal, and fast corner lots (nine parts total). The worst-case variation of the actual temperature from the temperature predicted by the best-fit line is 13°C, which works out to 20 codes.

6.3.3 Clock Input

Clock input to the CLKIN_P and CLKIN_N pins must be AC coupled. For single ended clock input, provide the input at CLKIN_N pin for optimal phase noise performance.

Based on the device internal architecture, for optimal device performance, a voltage offset between pin CLKIN_P and CLKIN_N required. To create a offset, the CLKIN_P and CLKIN_N pins must be biased using external resistors. The bias network circuits should be as below. The recommendated resistor values are R2 = 9.5k, R3 = 7.5K and make R1 and R4 as do not populate.

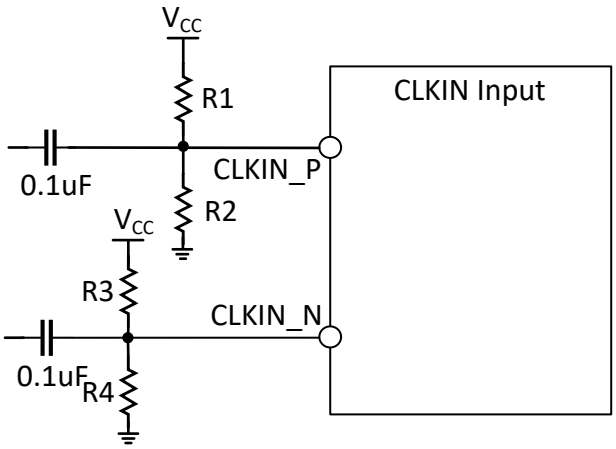

Figure 6-2. CLKIN Input Pins External Bias Network

6.3.3.1 Clock Input Adjustable Delay

The clock input allows the user to add an adjustable delay of 0 to 60ps range with the typical average step size of 1.1ps.

6.3.4 Clock Outputs

This device has four main output clocks which share a common frequency. This does not include the additional lower frequency LOGICLKs output.

6.3.4.1 Clock Output Buffers

The output buffers have a format that is open collector with an integrated pullup resistor, similar to CML.

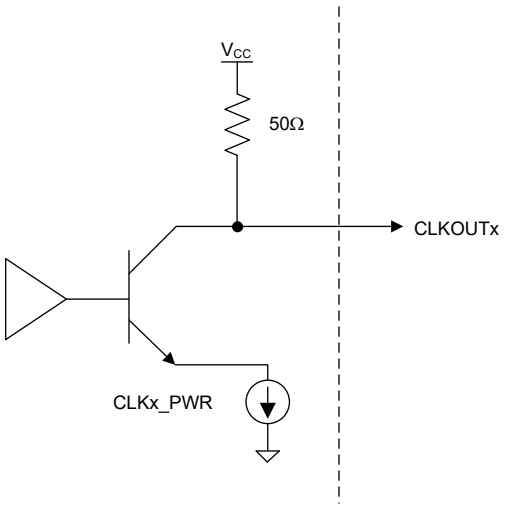

Figure 6-3. CLKOUT Output Buffer

The CLKx_EN bits can enable the output buffers. The output power of the buffers can be individually set with the CLKx_PWR field. However, these fields only control the output buffer, not the internal channel path that drives this buffer. To power down the entire path, disable the CHx_EN bit.

Table 6-2. Clock Output Power

CHx_EN	INTERNAL CHANNEL PATH	CLKx_EN	CLKx_PWR	OUTPUT BUFFER
0	Powered Down	Don't Care	Don't Care	Powered Down

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Table 6-2. Clock Output Power (continued)

CHx_EN	INTERNAL CHANNEL PATH	CLKx_EN	CLKx_PWR	OUTPUT BUFFER
1	Powered Up	0	Don't Care	Powered Down
		1	0	Minimum
			1	
			...	
			6	Maximum

6.3.4.2 Clock Output Adjustable Delay

The clock outputs all have individually programmable delays that can be set from 0 to 55ps range with the typical average step size of 0.9ps. For best noise performance below 1.5GHz output frequency, it is recommended to use output delay code >= 4.

6.3.4.3 Clock MUX

The four main clocks must be the same frequency, but this frequency can be bypassed, multiplied, or divided. This is determined by the CLK_MUX word.

Table 6-3. Clock MUX

CLK_MUX	OPTION	VALUES SUPPORTED
0	Buffer Mode	÷1 (bypass)
1	Divider Mode	÷2, 3, 4, 5, 6, 7, and 8
2	Multiplier Mode	x2, x3, x4, x5, x6, x7, x8

6.3.4.4 Clock Divider

Set the CLK_MUX to Divided to a divide value by 2, 3, 4, 5, 6, 7, or 8. This is set by the CLK_DIV word. When using the clock divider, any change to the input frequency requires the CLK_DIV_RST bit to be toggled from 1 to 0.

Table 6-4. Clock Divider

CLK_DIV	DIVIDE	DUTY CYCLE
0	Reserved	n/a
1	2	50%
2	3	33%
3	4	50%
4	5	40%
5	6	50%
6	7	43%
7	8	50%

6.3.4.5 Clock Multiplier

6.3.4.5.1 General Information About the Clock Multiplier

The clock multiplier can be used to multiply up the input clock frequency by a factor of ×2, ×3, ×4, ×5, ×6, ×7 or ×8. The multiply value is set by the CLK_MULT field. As the multiplier is PLL-based and includes an integrated VCO, the multiplier has a state machine clock, requires calibration and has a lock detect feature.

6.3.4.5.2 State Machine Clock for the Clock Multiplier

The state machine clock frequency (f_{SMCLK}) is derived by dividing down the input clock frequency by a programmed divider value. The state machine clock is also necessary for the multiplier calibration and lock detect. If there are concerns about the state machine clock creating spurs, then the state machine clock can be shut off, provided that the multiplier calibration is not running and the lock detect feature is not in use.

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6.3.4.5.2.1 State Machine Clock

A valid state machine clock is required (SMCLK_EN=1 and signal present at CLKIN pins) in below circumstances:

1. Multiplier is being calibrated.
2. Lock Detect from the multiplier is being monitored.
3. Clock divide value is being changed to 6 or 8.
4. For the device to perform a proper power on reset.
   a. Note that SMCLK_EN=1 is enabled by the power on reset, but an input clock is also required to allow the power on reset before SMCLK_EN can be set to 0.

When the state machine clock is enabled, the clock needs to be less than 30MHz and the frequency is as follows:

$f_{SMCLK} = f_{CLKIN} / (SMCLK\_DIV\_PRE * SMCLK\_DIV)$

When the state machine clock is not required, the clock can be disabled by setting SMCLK_EN=0 to minimize crosstalk and spurs.

6.3.4.5.3 Calibration for the Clock Multiplier

For optimal phase noise, the VCO in the multiplier divides up the frequency range into many different bands and cores and has optimized amplitude settings for each band and core. For this reason, upon initial use or whenever the frequency is changed, the user must run a calibration routine to determine the correct core, frequency band, and amplitude setting. Program the R0 register with a valid input signal to perform a calibration. To provide reliable multiplier calibration, the state machine clock frequency must be at least twice the SPI write speed, but no more than 30MHz. Whenever the CLK_MUX mode is changed or the multiplier is calibrated for the first time, the calibration time is substantially longer, on the order of 5ms.

6.3.4.5.4 Lock Detect for the Clock Multiplier

The lock detect status of the multiplier can be read back through the rb_LOCK_DETECT field or from the MUXOUT pin. The state machine clock must be running for the lock detect to work properly.

6.3.5 LOGICLK Outputs

The two LOGICLK outputs can be used to drive devices using lower frequency clocks, such as FPGAs. If only one LOGICLK required, the corresponding SYSREF output also be used as JESD204B/C interface clock. The LOGICLK output has a programmable output format and a corresponding SYSREF output.

6.3.5.1 LOGICLK Output Format

The LOGICLKOUT0 & LOGICLKOUT1 output format can be programmed to LVDS and CML modes. Depending on the format, the common mode can be programmable or external components can be required (see Table 6-5).

LOGICLKOUT1 output common mode and format can be programmable as shown LOGISYSREFOUT configuration.

Table 6-5. LOGICLKOUT0 Formats and Properties

LOGICLK_FMT	FORMAT	EXTERNAL COMPONENTS REQUIRED	OUTPUT LEVEL	COMMON MODE
0	LVDS	None	Programmable through LOGICLK_PWR	Programmable through LOGICLK_VCM.
2	CML	Pullup Resistors 50Ω to V_{CC}	Programmable through LOGICLK_PWR	LOGICLK_VCM has no impact, but this changes with LOGICLK_PWR.

table shows the logic clock LVDS format single ended swing and supported common mode voltage over programmable LOGICLK_VCM settings.

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Table 6-6. LOGICLK LVDS Common Mode Voltage vs LOGICLK_VCM

LOGICLK_VCM	LOGICLK VOD swing - Single ended pk-pk (V)	LOGICLK Common Mode Voltage (V)
6	0.37	0.81
5	0.36	0.90
4	0.35	0.99
3	0.34	1.09
2	0.33	1.18
1	0.31	1.27

The following table shows the logic clock LVDS format supported LOGICLK_VCM range corresponding to LOGICLK_PWR setting.

Table 6-7. Supported LOGICLK_VCM settings

LOGICLK_PWR	LOGICLK VOD swing - Single ended pk-pk (V)	Supported VOCM range	Supported LOGICLK_VCM range	
			Min code	Max code
0	0.1	0.8 to 1.4	0	6
1	0.15	0.8 to 1.4	0	6
2	0.2	0.8 to 1.4	0	6
3	0.25	0.75 to 1.35	0	6
4	0.3	0.8 to 1.3	1	6
5	0.35	0.8 to 1.3	1	6
6	0.4	0.9 to 1.3	2	6
7	0.5	0.9 to 1.2	3	6

6.3.5.2 LOGICLK Dividers

The LOGICLK_DIV_PRE divider, LOGICLK_DIV and LOGICLK2_DIV dividers are used for the LOGICLK outputs. The LOGICLK_DIV_PRE divider is necessary to divide the frequency down to verify that the input to the LOGICLK_DIV divider is 3.2GHz or less. The LOGICLK2_DIV is an additional divider to generate LOGICLKOUT1 output. When LOGICLK_DIV is not even and not bypassed, the duty cycle is not 50%. All the LOGICLK dividers are synchronized by the SYNC feature, which allows synchronization across multiple devices.

Table 6-8. Minimum N-Divider Restrictions

f_{CLKIN} (MHz)	LOGICLK_DIV_PRE	LOGICLK_DIV	LOGICLK2_DIV	LOGICLKOUT0 TOTAL DIVIDE RANGE	LOGICLKOUT1 TOTAL DIVIDE RANGE
$f_{CLKIN} \leq 3.2GHz$	÷1, 2, 4	÷1, 2, 3, …1023	÷1, 2, 4, 8	[1, 2, ...1023] [2, 4, ... 2046] [4, 8, ...4092]	[1, 2, ...32736]
$3.2GHz < f_{CLKIN} \leq 6.4GHz$	÷2, 4	÷1, 2, 3, …1023	÷1, 2, 4, 8	[2, 4, ... 2046] [4, 8, ...4092]	[2, 4, ...32736]
$f_{CLKIN} > 6.4GHz$	÷4	1, 2, 3, …1023	÷1, 2, 4, 8	[4, 8, ...4092]	[4, 8, ...32736]

6.3.6 SYSREF

SYSREF allows a low frequency JESD204B/C compliant signal to be produced that is reclocked to a main clock outputs or LOGICLK outputs. The delays between the CLKOUT and SYSREF outputs are adjustable with software. The SYSREF output can be configured as a generator using the internal SYSREF divider, or as a

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repeater duplicating the signal on the SYSREFREQ pins. The SYSREF generator for both the main clocks and the LOGICLK output are the same.

Table 6-9. SYSREF Modes

SYSREF_MODE	DESCRIPTION
0	**Generator Mode** Internal generator creates a continuous stream of SYSREF pulses. The SYSREFREQ_INPUT bits setting used to gate the SYSREF divider through SYSREFREQ pins or logic high from the channels for improved noise isolation without disrupting the synchronization of the SYSREF dividers. The SYSREFREQ_INPUT bits must be set for SYSREFREQ pins input or force high with changing bit from SYSREFREQ_INPUT[1] → 0 to 1 for a SYSREF output to come out.
1	**Pulser** Internal generator generates a burst of 1 - 16 pulses that is set by SYSREF_PULSE_CNT that occurs with the SYSREFREQ_INPUT settings for rising edge on the SYSREFREQ pins or force high with changing bit from SYSREFREQ_INPUT[1] → 0 to 1
2	**Repeater Mode** SYSREFREQ pins input are bypass to the SYSREFOUT outputs pins. If the delay is needed, the SYSREFREQ pins input are reclocked to clock outputs accordance to the SYSREF_DLY_BYP field before sent to the SYSREFOUT output pins.
3	**Repeater Retime Mode** SYSREFREQ pins input are reclocked to clock input and then delayed in accordance to the SYSREF_DLY_BYP field before sent to the SYSREFOUT output pins.

Below figures show the functional block diagrams for different SYSREF modes.

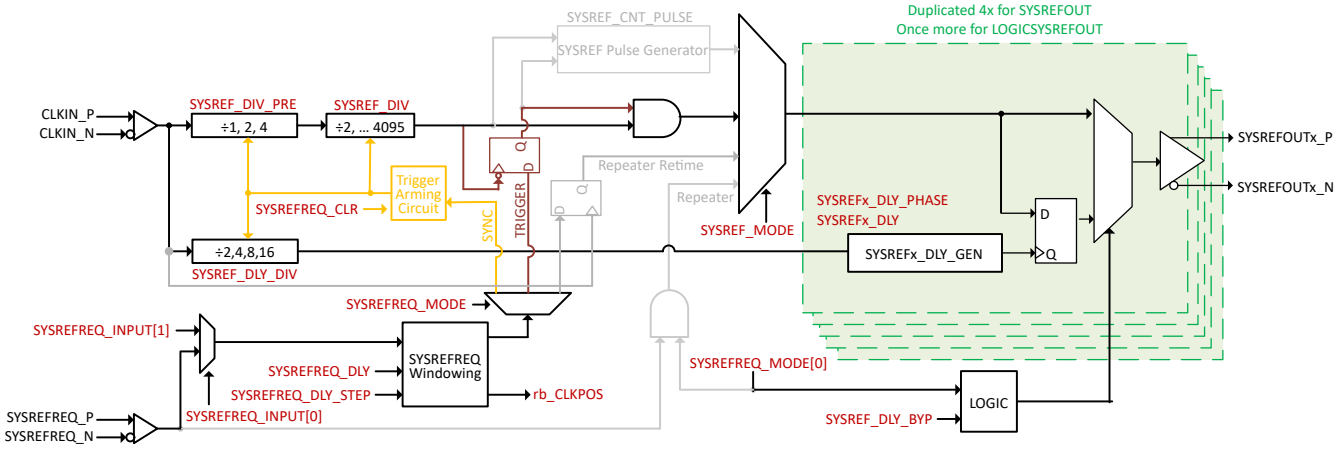

Figure 6-4. Functional Block Diagram of SYSREF Circuitry in Generator Mode

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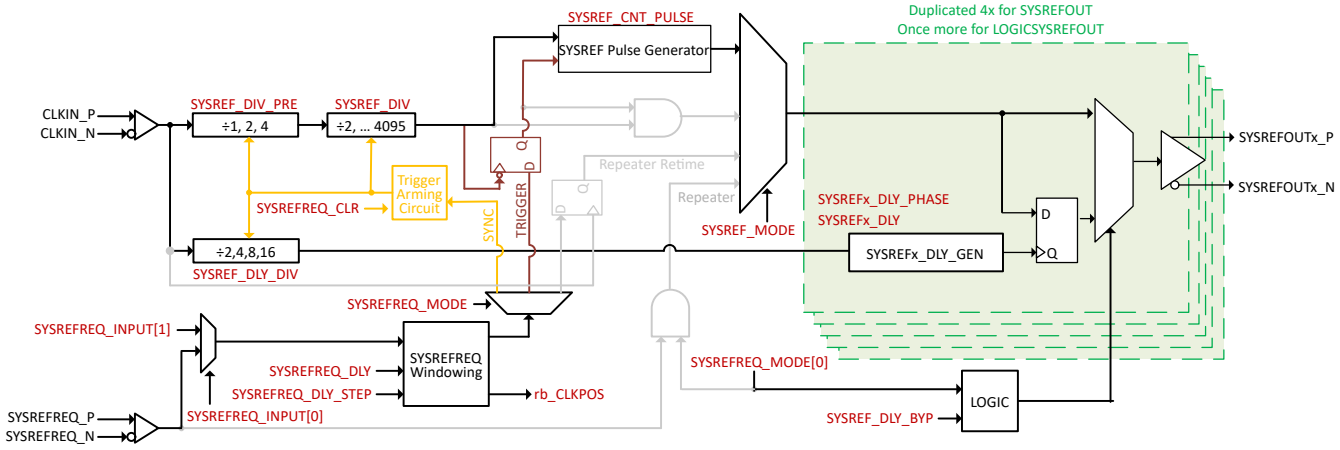

Figure 6-5. Functional Block Diagram of SYSREF Circuitry in Pulser Mode

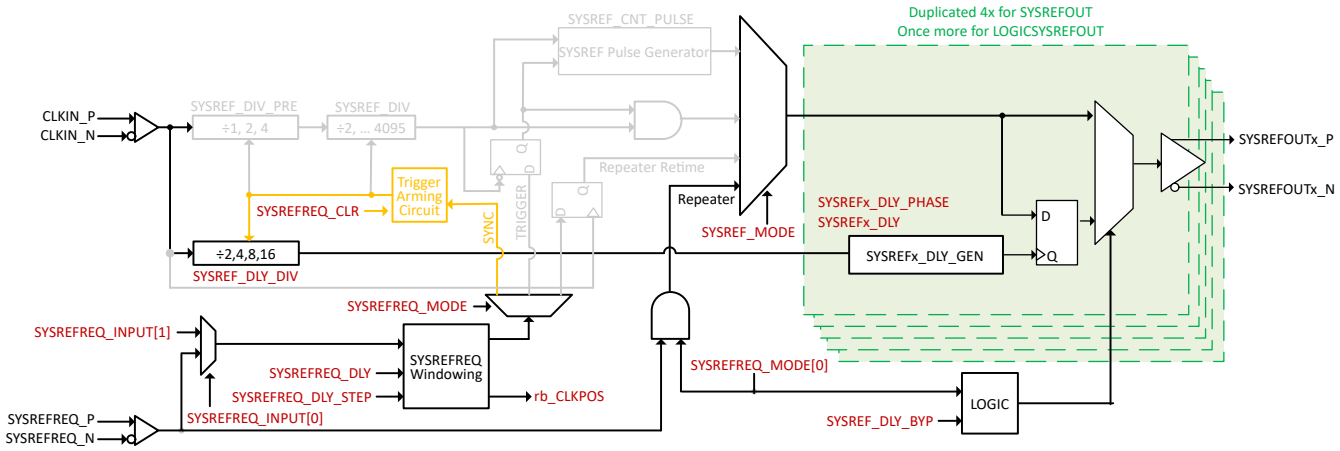

Figure 6-6. Functional Block Diagram of SYSREF Circuitry in Repeater Mode

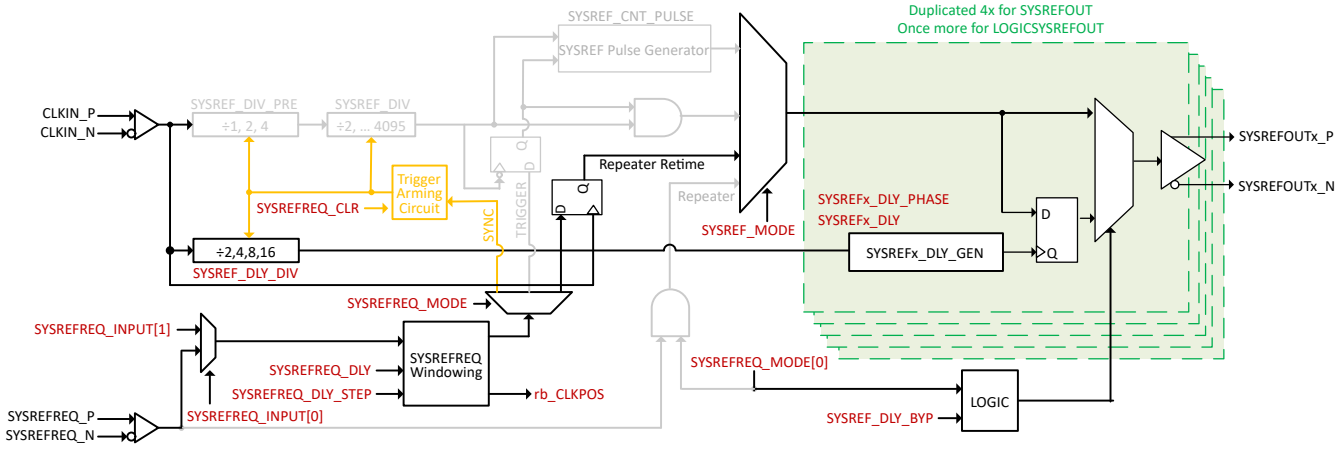

Figure 6-7. Functional Block Diagram of SYSREF Circuitry in Repeater Retime Mode

6.3.6.1 SYSREF Output Buffers

6.3.6.1.1 SYSREF Output Buffers for Main Clocks (SYSREFOUT)

The SYSREF outputs within the clock output channels have the same output buffer structure as the clock output buffer, with the addition of circuitry to adjust the common-mode voltage. The SYSREF outputs are CML outputs

with a common-mode voltage that can be adjusted with the SYSREFx_VCM field, and the output level that can be programmed with the SYSREFx_PWR field. This feature is to allow DC coupling. Note that the CLKOUT outputs do not have adjustable common-mode voltage and must be AC coupled for optimal noise performance.

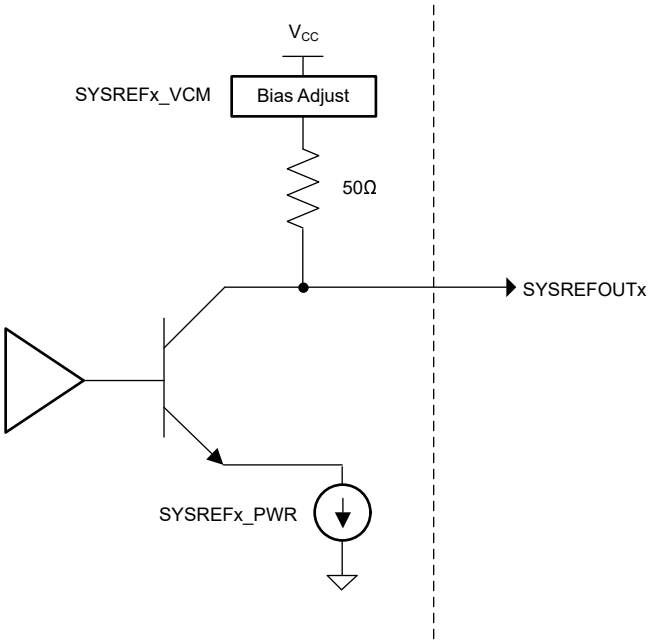

Figure 6-8. SYSREF Output Buffer

The common-mode voltage and output power can be simulated assuming a 100Ω differential load and no DC path to ground. The SYSREF output swing and corresponding supported common mode voltage as shown below. For each SYSREFx_VCM settings, the output common mode voltage variation can be within ±10% of change value.

SYSREFx_PWR	Swing VOD (single ended pk-pk)		Supported SYSREFx_VCM code				Supported VCM range (V)			
	SYSREFx_PWR_LOW = 1 Low Power (V)	SYSREFx_PWR_LOW = 0 High Power (V)	SYSREFx_PWR_LOW = 1 Low Power (V)		SYSREFx_PWR_LOW = 0 High Power (V)		SYSREFx_PWR_LOW = 1 Low Power (V)		SYSREFx_PWR_LOW = 0 High Power (V)	
			Min code	Max code	Min code	Max code	Min VCM	Max VCM	Min VCM	Max VCM
0	0.23	0.46	4	44	10	44	0.500	1.500	0.650	1.500
1	0.29	0.58	6	44	12	42	0.550	1.500	0.700	1.450
2	0.35	0.69	7	44	15	40	0.575	1.500	0.775	1.400
3	0.40	0.79	8	44	18	36	0.600	1.500	0.850	1.300
4	0.46	0.89	10	44	20	31	0.650	1.500	0.900	1.175
5	0.51	0.97	11	44	22	26	0.675	1.500	0.950	1.050
6	0.57	1.04	12	44	23		0.700	1.500	0.975	
7	0.62		13	41			0.725	1.425		

6.3.6.1.2 LOGISYSREF Output Buffer

The LOGISYSREFOUT / LOGICLKOUT1 output supports LVDS and CML output formats. The LOGISYSREF_EN enables the output buffer and LOGISYSREF_FMT sets the format. LVDS mode allows programmable output power and common mode voltage. CML output format require external components and allows programmable output power.

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Table 6-10. LOGISYSREFOUT / LOGICLKOUT1 Output Buffer Configuration

LOGISYSREF_EN	LOGISYSREF_FMT	LOGISYSREF FORMAT	EXTERNAL TERMINIATION REQUIRED	OUTPUT POWER	OUTPUT COMMON MODE
0	Powered Down				
1	0	LVDS	None	Programmable through LOGISYSREF_PWR	Programmable through LOGISYSREF_VCM.
	1	Reserved			
	2	CML	Pullup resistors 50Ω to V_{CC}	Programmable through LOGISYSREF_PWR	LOGISYSREF_VCM has no impact, but this changes with LOGISYSREF_PWR.
	3	Reserved			

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6.3.6.1.3 SYSREF Frequency and Delay Generation

For the frequency of the SYSREF output in generator mode, the SYSREF_DIV_PRE divider is necessary to verify that the input of the SYSREF_DIV divider is not more than 3.2GHz.

Table 6-11. SYSREF_DIV_PRE Setup

f_{CLKIN}	SYSREF_DIV_PRE	TOTAL SYSREF DIVIDE RANGE
3.2GHz or Less	÷1, 2, or 4	÷2, 3, 4, ...16380
3.2GHz < f_{CLKIN} ≤ 6.4GHz	÷2 or 4	÷4, 6, 8, … 16380
f_{CLKIN} > 6.4GHz	÷4	÷8, 12, 16, … 16380

For the delay, the input clock frequency is divided by SYSREF_DLY_DIV to generate $f_{INTERPOLATOR}$. This has a restricted range as shown in Table 6-12. Note also that when SYSREF_DLY_BYP = 1 (delaygen engaged) and SYSREF_MODE = 0 or 1 (a generator mode) the SYSREF output frequency must be a multiple of the phase interpolator frequency.

$f_{INTERPOLATOR}$ % f_{SYSREF} = 0.

Table 6-12. SYSREF Delay Setup

f_{CLKIN}	SYSREF_DLY_DIV	SYSREF_DLY_SCALE	$f_{INTERPOLATOR}$
6.4GHz < f_{CLKIN} ≤ 12.8GHz	16	0	0.4GHz to 0.8GHz
3.2GHz < f_{CLKIN} ≤ 6.4GHz	8	0	0.4GHz to 0.8GHz
1.6GHz < f_{CLKIN} ≤ 3.2GHz	4	0	0.4GHz to 0.8GHz
0.8GHz < f_{CLKIN} ≤ 1.6GHz	2	0	0.4GHz to 0.8GHz
0.4GHz < f_{CLKIN} ≤ 0.8GHz	2	1	0.2GHz to 0.4GHz
0.3GHz < f_{CLKIN} ≤ 0.4GHz	2	2	0.15GHz to 0.2GHz

The maximum delay is equal to the phase interpolator period and there are 4 × 127 = 508 different delay steps. Use Equation 2 to calculate the size of each step.

$$\text{DelayStepSize} = 1 / (f_{INTERPOLATOR} \times 508) = \text{SYSREF\_DLY\_DIV} / (f_{CLKIN} \times 508) \quad (2)$$

Use Equation 3 to calculate the total delay.

$$\text{TotalDelay} = \text{DelayStepSize} \times \text{StepNumber} \quad (3)$$

Table 6-13 shows the number of steps for each delay.

Below table can be used to program the desired delay step number.

Table 6-13. Calculation of StepNumber

Step Number Range	SYSREFx_DLY_PHASE	SYSREFx_DLY
0 - 127 (127 - SYSREFx_DLY)	0	127 to 0
127 - 254 (127 + SYSREFx_DLY)	1	0 to 127
254 - 381 (381 - SYSREFx_DLY)	3	127 to 0
381 - 508 (381 + SYSREFx_DLY)	2	0 to 127

The SYSREF_DLY_BYP field selects the delay path in SYSREF generation output and repeater retime mode.

Below table shows the unusable step number for the SYSREF delay in different SYSREF_MODE and SYSREF dividers settings.

Table 6-14. SYSREF Delay Unusable Step Numbers

SYSREF_MODE	SYSREF_DIV_PRE	SYSREF_DIV	SYSREF_DLY_DIV	Unusable Step Number
Continuous Or Pulsed	1	2 or 3	2	Invalid Combination
			4	
			8	
			16	
	2		2	15 to 45
			4	Invalid Combination
			8	
			16	
	4		2	10 to 45
			4	140 to 175
			8	Invalid Combination
			16	
	1	>= 4	2	10 to 45
			4	390 to 430
			8	215 to 240
			16	Invalid Combination
	2		2	265 to 300
			4	
			8	390 to 430
			16	280 to 300
	4		2	265 to 300
			4	
			8	140 to 175
			16	390 to 430
Repeater Retime	x	x	2	20 to 50
			4	145 to 180
			8	85 to 125
			16	120 to 160

Figure shows an example of unusable delay step positions, where SYSREF rising edge lies around the phase interpolator rising edge.

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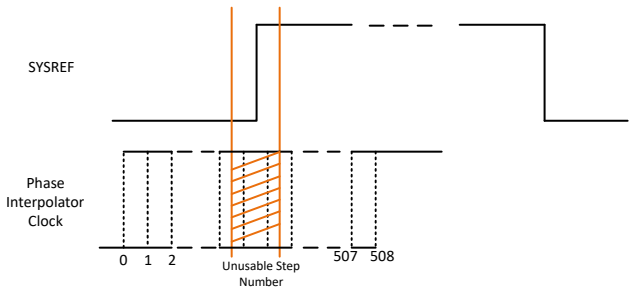

Figure 6-9. Unusable Delay Step Numbers

Table shows the SYSREF output delay step size and it varies with the phase interpolator frequency.

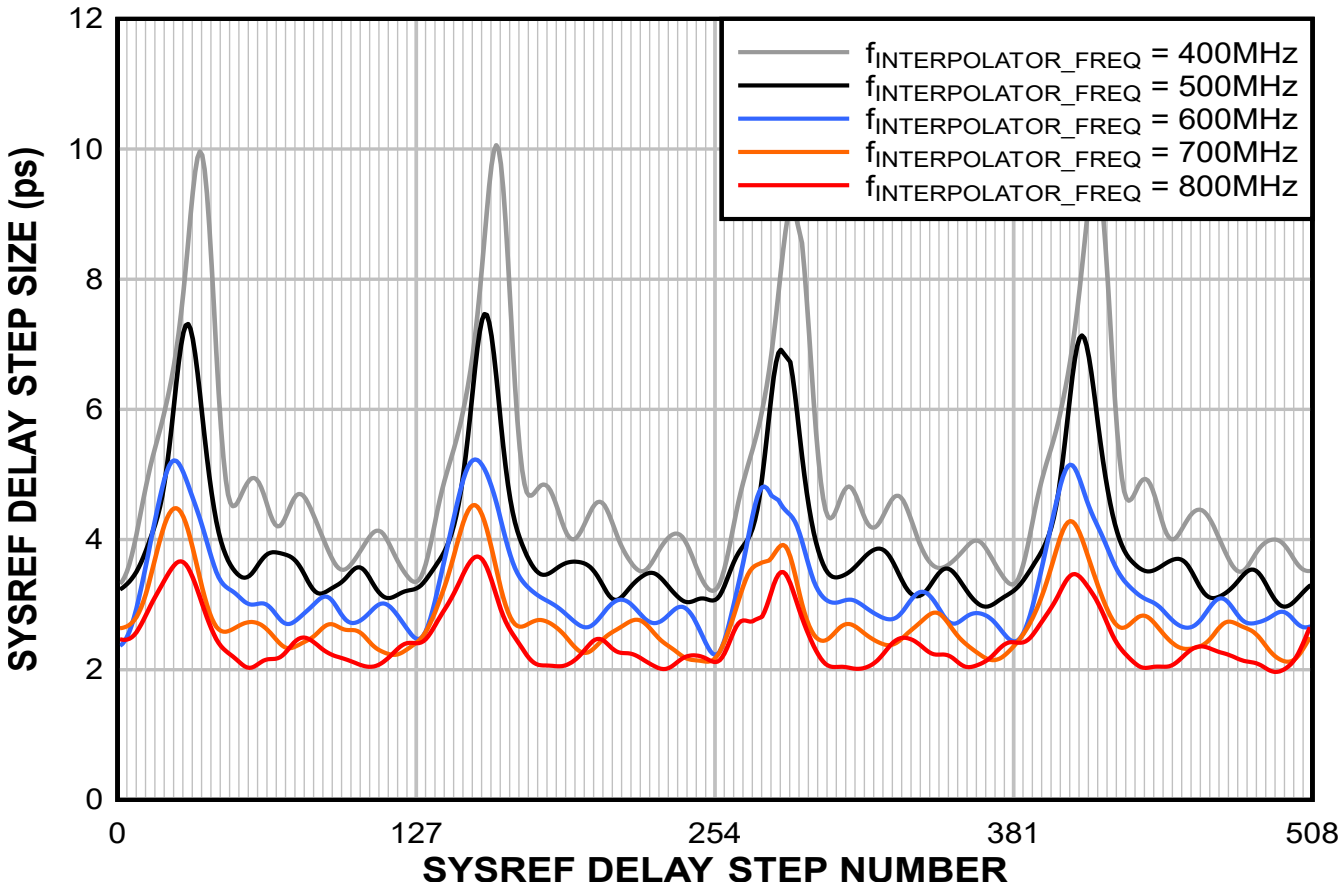

Figure 6-10. SYSREF Delay Step Size

6.3.6.1.4 SYSREFREQ Pins and SYSREFREQ SPI Controlled Fields

The SYSREFREQ pins are multipurpose and can be used for SYNC, SYSREF requests, and SYSREF windowing. These pins can be DC or AC coupled and have individual 50Ω, single-ended termination with programmable common-mode support.

In addition to these pins, the SYSREFREQ_INPUT fields can be set to select the SYSREFREQ pin inputs or force internally to logic "Low" or "High" to emulate the same effect as forcing these pins, simplifying hardware in some cases.

6.3.6.1.4.1 SYSREFREQ Pins Common-Mode Voltage

The SYSREFREQ_P and SYSREFREQ_N pins can be driven either AC or DC coupled. When driven AC coupled or using the internal biasing, the common-mode voltage can be adjusted with the SYSREFREQ_VCM bits.

Table 6-15. SYSREFREQ Pin Common-Mode Voltage

SYSREFREQ_VCM	SYSREFREQ Input Pins CM Voltage
0	Zero offset between pins (AC coupled)
1	Pin P is biased higher than pin N (AC coupled)
2	Pin N is biased higher than pin P (AC coupled)
3	No Bias (DC Coupled)

When there is no input during the AC coupled, the common mode voltage offset have to be created to avoid the chattering at the pins. SYSREFREQ_VCM_OFFSET fields help to set the offset between the pins.

Table 6-16. SYSREFREQ Pin Common-Mode Voltage Offset

SYSREFREQ_VCM_OFFSET	Common Mode Voltage Offset Between The Pins
0	25mV
1	50mV
2	100mV
3	150mV

6.3.6.1.4.2 SYSREFREQ Windowing Feature

The SYSREF windowing can be used to internally calibrate the timing between the SYSREFREQ and CLKIN pins to optimize setup and hold timing and trim out any mismatches between SYSREFREQ and CLKIN paths. This feature requires that the timing from the SYSREFREQ rising edge to the CLKIN rising edge is consistent. The timing from the SYSREFREQ rising edge to the CLKIN rising edges can be tracked with the rb_CLKPOS field. Once the timing to the rising edge of the CLKIN pin is found, then the SYSREFREQ rising edge can be internally adjusted with the SYSREFREQ_DLY_STEP and SYSREFREQ_DLY fields to optimize setup or hold times.

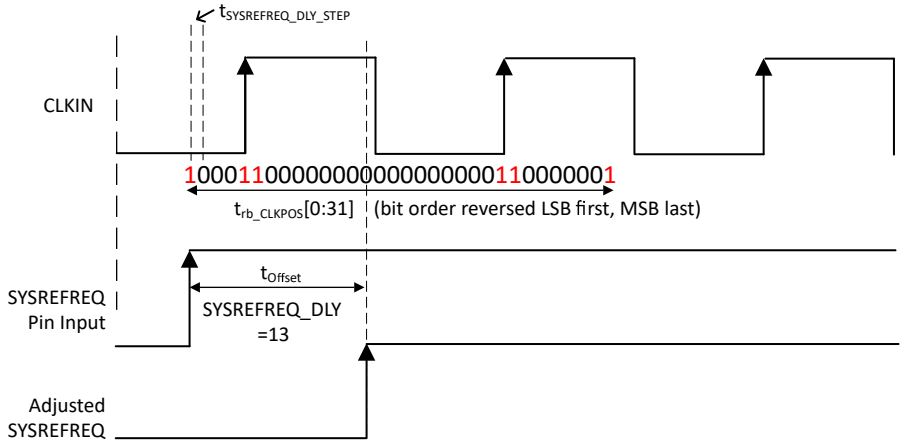

Figure 6-11. SYSREFREQ Internal Timing Adjustment

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6.3.6.1.4.2.1 General Procedure Flowchart for SYSREF Windowing Operation

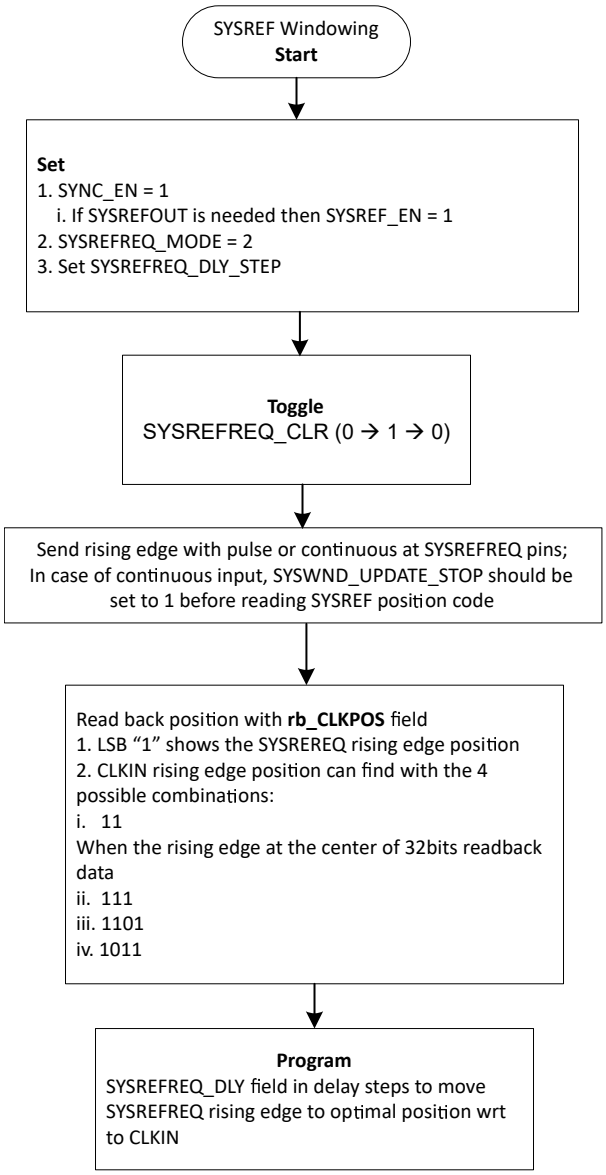

Figure 6-12. Flowchart for SYSREF Windowing Operation

Table 6-17. SYSREFREQ_DELAY_STEP

INPUT FREQUENCY	RECOMMENDED SYSREFREQ_DLY_STEP	DELAY (ps)
1.4GHz < f_{CLKIN} ≤ 2.7GHz	0	22.25
2.4GHz < f_{CLKIN} ≤ 4.7GHz	1	13
3.1GHz < f_{CLKIN} ≤ 5.7GHz	2	10.5
f_{CLKIN} ≥ 4.5GHz	3	7.75

6.3.6.1.4.2.2 Other Guidance For SYSREF Windowing

- The SYSREFREQ pins must be held high for a minimum time of $3/f_{CLKIN}$ + 1.6ns and only after this time rb_CLKPOS field is valid.
- If the user infers multiple valid SYSREFREQ_DLY values from rb_CLKPOS registers to avoid setup and hold time violations. TI recommends to choose the lowest valid SYSREFREQ_DLY to minimize variation over temperature.

- The programmed SYSREFREQ_DLY for optimized setup and hold time after SYSREF windowing adjusts the internal SYSREFREQ, but the SYSREFREQ_DLY does not show the movement in SYSREF windowing readback code. SYSREF windowing always evaluates the signals at the pins.

6.3.6.1.4.2.3 For Glitch-Free Output

- Keep the same state for the SYSREFREQ pin when switching from request mode to windowing mode and back to request mode. For example, if the SYSREFREQ pin is high (or low) when windowing mode starts, make sure the pin state is high (or low) again after windowing mode ends before programing SYSREFREQ_MODE field to other mode.
- The SYSREFREQ pin must be set low when switching from or to SYNC mode.

6.3.6.1.4.2.4 If Using SYNC Feature

- Only one SYSREFREQ pin rising edge is permitted per 75 input clock cycles
- SYSREFREQ has to stay high for more than 6 clock cycles

6.3.6.1.4.2.5 SYNC Feature

The SYNC feature allows the user to synchronize the CLK_DIV, LOGICLK_DIV, LOGICLK1_DIV, LOGICLK_DIV_PRE, SYSREF_DIV, SYSREF_DIV_PRE, and SYSREF_DLY_DIV dividers so that the phase offset can be made consistent between power cycles. This allows users to synchronize multiple devices. In multiple devices, the dividers synchronization should be done through the SYSREFREQ pin and single device dividers sync can be done using the SPI.

6.3.7 Power-Up Timing

To power up the device, some power sequencing is required.

1. Apply power to the device and verify that the VCC pins reach proper levels.
2. Although the power-on reset happens automatically, users can do a software reset by toggling the RESET bit from 1 to 0. Make sure the time between programming these two commands be at least 1µs.
3. Program the registers as desired.
4. Program DEV_IOPT_CTRL field to 0x6.

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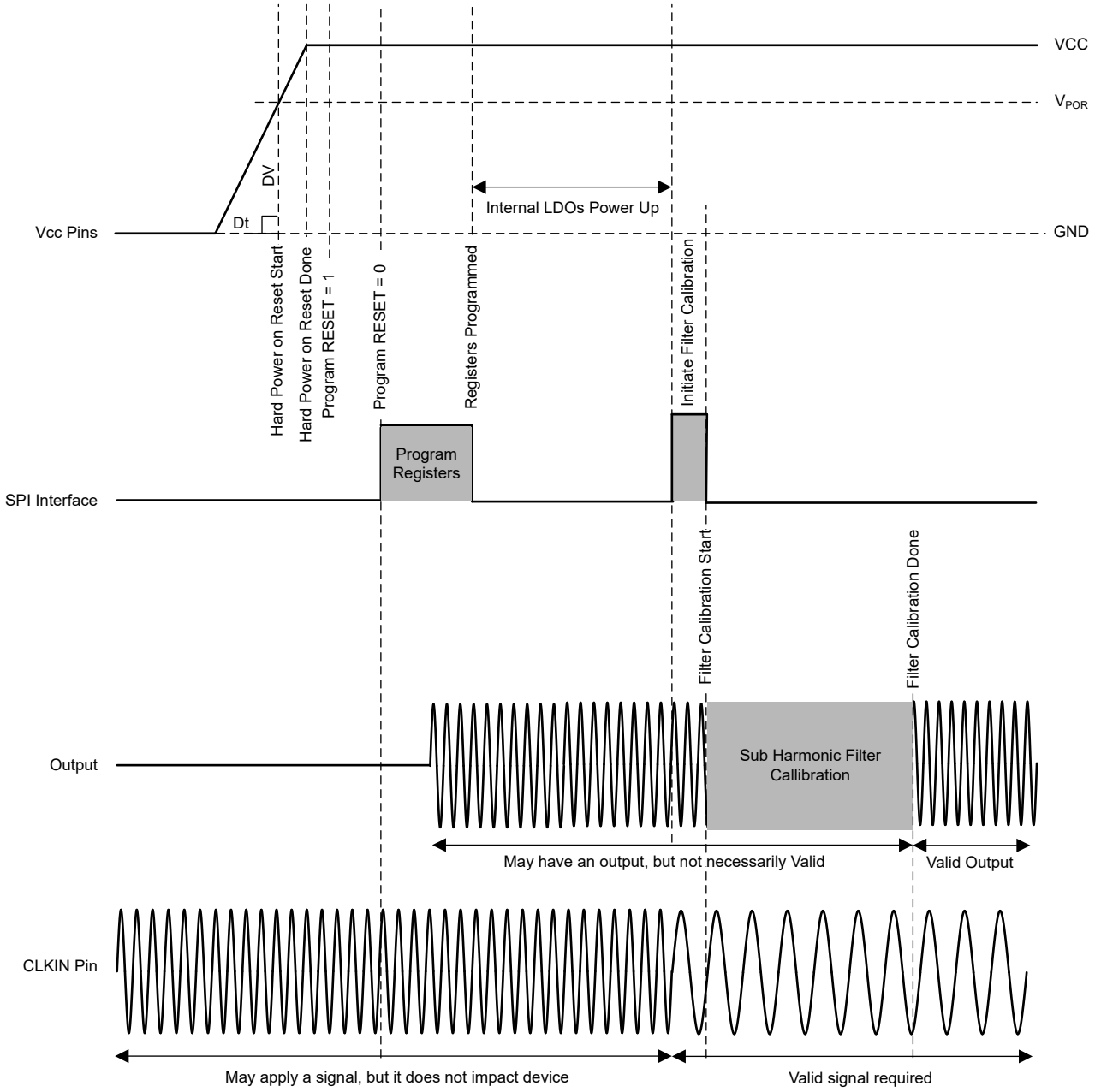

Figure 6-13. Power-Up Timing

6.3.8 Treatment of Unused Pins

In many cases, not all pins are needed. Table 6-18 gives recommendation on handling of these unused pins.

Table 6-18. Treatment of Unused or Partially Used Pins

PIN	TREATMENT
All Vcc Pins	These pins must always be connected to the supply. If the block that the power supply (as implied by the pin name) is not used, then the supply decaps can be minimized or eliminated.

Table 6-18. Treatment of Unused or Partially Used Pins (continued)

PIN	TREATMENT
SYSREFREQ	If driving single-ended AC coupled, the complimentary input must have a AC-coupling capacitor to ground. If driving single-ended DC coupled, complimentary input must be externally biased at required VCM with Thevenin's equivalent. If using continuous SYSREF Generator mode, these pins can be either used to turn the output buffers on and off or can be left floating. If left floating, use SYSREFREQ_INPUT[1] to control the output gating. If not using SYSREF at all, pins can be left open.
CLKIN Complementary Input	If driving single-ended, the complementary input must have a AC-coupling capacitor and 50Ω to ground.
BIAS01 and BIAS23	These pins can be left open if multiplier is not used.
CLKOUT SYSREFOUT	Placing a 100Ω differential resistor across the output pins is recommended. If using single ended output, the complementary output pin must have a AC-coupling capacitor and 50Ω to ground.
LOGICLKOUT LOGISYSREFOUT	These pins can be left open if not used.

6.4 Device Functional Modes Configurations

The device can configure in high frequency clock buffer, divider or multiplier mode. Each mode requires the below register configurations for functioning.

Table 6-19. Configurations for Device Functional Modes

REGISTER ADDRESS	BIT	FIELD	FUNCTION	BUFFER	DIVIDER	MULTIPLIER
R27	2:0	CLK_MUX	Select the mode	1	2	3
R27	5:3	CLK_DIV / CLK_MULT	Select the division or multiplication value	x	CLK_DIV 0x1 = ÷2 0x2 = ÷3 0x3 = ÷4 0x4 = ÷5 0x5 = ÷6 0x6 = ÷7 0x7 = ÷8	CLK_MULT 0x2 = x2 0x3 = x3 0x4 = x4 0x5 = x5 0x6 = x6 0x7 = x7 0x8 = x8
R26	0	SMCLK_EN	Enables the state machine clock generator	x	x	1
R26	4:1	SMCLK_DIV_PRE	Sets pre-divider for state machine clock	x	x	Pre-clock divider for state machine clock 0x2 = ÷2 0x4 = ÷4 0x8 = ÷8
R26	7:5	SMCLK_DIV	Sets state machine clock divider	x	x	Additional SMCLK divider to keep output frequency must be ≤ 30 MHz. 0x0 = ÷1 0x1 = ÷2 0x2 = ÷4 0x3 = ÷8 0x4 = ÷16 0x5 = ÷32 0x6 = ÷64 0x7 = ÷128

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Table 6-19. Configurations for Device Functional Modes (continued)

REGISTER ADDRESS	BIT	FIELD	FUNCTION	BUFFER	DIVIDER	MULTIPLIER
R0	All	Calibrate Multiplier	Calibrate the PLL based multiplier	x	x	Write R0 for calibrate multiplier

7 Register Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POWER DOWN	RESET
R1	0	0	0	0	0	0	0	0	0	0	0	LD_DIS	READBACK_CTRL	0	1	1
R2	0	0	0	0	0	0	TEMPSENSE_EN	SYNC_EN	1	SYSREF_EN	1	LOGIC_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R3	0	0	0	0	0	0	0	0	0	CLKIN_DLY						
R4	0	0	0	0	0	CLK0_DLY							CLK0_PWR			CLK0_EN
R5	0	0	0	0	0	CLK1_DLY							CLK1_PWR			CLK1_EN
R6	0	0	0	0	0	CLK2_DLY							CLK2_PWR			CLK2_EN
R7	0	0	0	0	0	CLK3_DLY							CLK3_PWR			CLK3_EN
R8	0	SYSREF0_PWR_LOW	SYSREF0_AC	1	1	1	SYSREF0_VCM						SYSREF0_PWR			SYSREF0_EN
R9	0	SYSREF1_PWR_LOW	SYSREF1_AC	1	1	1	SYSREF1_VCM						SYSREF1_PWR			SYSREF1_EN
R10	0	SYSREF2_PWR_LOW	SYSREF2_AC	1	1	1	SYSREF2_VCM						SYSREF2_PWR			SYSREF2_EN
R11	0	SYSREF3_PWR_LOW	SYSREF3_AC	1	1	1	SYSREF3_VCM						SYSREF3_PWR			SYSREF3_EN
R12	0	0	0	LOGICLK_FMT		0	0	LOGICLK_VCM					LOGICLK_PWR			LOGICLK_EN
R13	0	0	0	LOGISYSREF_FMT		0	0	LOGISYSREF_VCM					LOGISYSREF_PWR			LOGISYSREF_EN
R14	LOGICLK_DIV_RST	0	0	LOGICLK_DIV										LOGICLK_DIV_PRE		
R15	0	0	0	0	0	0	0	0	0	0	0	0	0	LOGICLK2_DIV		LOGICLK2_EN

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	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R16	0	0	0	0	0	0	0	0	SYSREF_DLY_SCALE		SYSREFREQ_DLY_STEP		SYSREFREQ_VCM_OFFSET		SYSREFREQ_VCM	
R17	0	0	0	0	0	0	0	0	SYSREFREQ_INPUT		SYSWND_UPDATE_STOP	SYNC_STOP	SYSWND_LATCH	SYSREFREQ_CLR	SYSREFREQ_MODE	
R18	0	0	0	0	0	0	0	0	0	0	SYSREFREQ_DLY					
R19	0	0	0	0	0	0	0	0	0	SYSREF_DLY_BYP	SYSREF_PULSE_CNT				SYSREF_MODE	
R20	SYSREF_DLY_DIV		SYSREF_DIV												SYSREF_DIV_PRE	
R21	0	0	0	0	0	0	0	SYSREF0_DLY							SYSREF0_DLY_PHASE	
R22	0	0	0	0	0	0	0	SYSREF1_DLY							SYSREF1_DLY_PHASE	
R23	0	0	0	0	0	0	0	SYSREF2_DLY							SYSREF2_DLY_PHASE	
R24	0	0	0	0	0	0	0	SYSREF3_DLY							SYSREF3_DLY_PHASE	
R25	0	0	0	0	0	0	0	LOGISYSREF_DLY							LOGISYSREF_DLY_PHASE	
R26	0	0	0	0	0	0	0	0	SMCLK_DIV			SMCLK_DIV_PRE				SMCLK_EN
R27	0	1	1	0	MULT_HIPFD_EN	1	FCAL_EN	0	0	CLK_DIV_RST	CLK_DIV			CLK_MUX		
R29	rb_CLKPOS[31:16]															
R30	rb_CLKPOS[15:0]															
R31	0	0	0	0	0	rb_TEMPSENSE										
R32	rb_VER_ID															
R36	1	0	0	0	1	0	1	1	0	0	0	1	0	1	1	0
R37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	rb_LOCK_DETECT
R39	0	1	1	1	1	0	0	1	0	1	1	0	0	0	0	1
R40	0	1	1	1	1	0	0	1	0	1	1	0	0	0	1	1
R41	0	1	1	1	0	1	0	1	0	1	0	0	0	0	0	1
R42	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	1
R43	0	1	1	1	0	1	1	1	0	1	0	0	0	0	0	1

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	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R44	0	1	1	1	0	1	0	1	0	1	1	0	0	0	0	1
R45	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
R54	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
R55	0	0	0	0	0	0	0	0	0	0	DEV_IOPT_CTRL					
R77	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

ADVANCE INFORMATION

7.1 Device Registers

Table 7-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 7-1 must be considered as reserved locations and the register contents must not be modified.

Table 7-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	R0	Powerdown and Reset	Section 7.1.1
1h	R1	Software reset, MUXOUT pin setting	Section 7.1.2
2h	R2	Channels, Logic Clock, SYSREF, SYNC and Temp Sensor Enable	Section 7.1.3
3h	R3	CLKIN Delay	Section 7.1.4
4h	R4	CLKOUT0 Enables, Power and Delay	Section 7.1.5
5h	R5	CLKOUT1 Enables, Power and Delay	Section 7.1.6
6h	R6	CLKOUT2 Enables, Power and Delay	Section 7.1.7
7h	R7	CLKOUT3 Enables, Power and Delay	Section 7.1.8
8h	R8	SYSREFOUT0 Enables, Power, VCM	Section 7.1.9
9h	R9	SYSREFOUT1 Enables, Power, VCM	Section 7.1.10
Ah	R10	SYSREFOUT2 Enables, Power, VCM	Section 7.1.11
Bh	R11	SYSREFOUT3 Enables, Power, VCM	Section 7.1.12
Ch	R12	LOGICLK Enables, Power, VCM and Output Formats	Section 7.1.13
Dh	R13	LOGISYSREF Enables, Power, VCM and Output Formats	Section 7.1.14
Eh	R14	LOGICLK Dividers	Section 7.1.15
Fh	R15	LOGICLK2 Enables, Dividers	Section 7.1.16
10h	R16	SYSREFREQ Input	Section 7.1.17
11h	R17	SYSREFREQ Input	Section 7.1.18
12h	R18	SYSREFREQ Input	Section 7.1.19
13h	R19	SYSREF Output	Section 7.1.20
14h	R20	SYSREF Output Dividers	Section 7.1.21
15h	R21	SYSREFOUT0 Delay	Section 7.1.22
16h	R22	SYSREFOUT1 Delay	Section 7.1.23
17h	R23	SYSREFOUT2 Delay	Section 7.1.24
18h	R24	SYSREFOUT3 Delay	Section 7.1.25
19h	R25	LOGISYSREFOUT Delay	Section 7.1.26
1Ah	R26	State Machine Clock	Section 7.1.27
1Bh	R27	Clock MUX, Clock Dividers/Multiplier	Section 7.1.28
1Dh	R29	SYSREFREQ Windowing (readback)	Section 7.1.29
1Eh	R30	SYSREFREQ Windowing (readback)	Section 7.1.30
1Fh	R31	Temperature Sensor (readback)	Section 7.1.31
20h	R32	Device Version ID (readback)	Section 7.1.32
24h	R36	Multiplier Mode (Reserved)	
25h	R37	Lock Detect (readback)	Section 7.1.34
27h	R39	Multiplier Mode (Reserved)	
28h	R40	Multiplier Mode (Reserved)	
29h	R41	Multiplier Mode (Reserved)	
2Ah	R42	Multiplier Mode (Reserved)	
2Bh	R43	Multiplier Mode (Reserved)	
2Ch	R44	Multiplier Mode (Reserved)	
2Dh	R45	Multiplier Mode (Reserved)	

Table 7-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
36h	R54	Multiplier Mode (Reserved)	
37h	R55	Current Optimization	Section 7.1.43
4Dh	R77	Multiplier Mode (Reserved)	

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1.1 R0 Register (Offset = 0h) [Reset = 0000h]

R0 is shown in Table 7-3.

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Table 7-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	UNDISCLOSED	R	0h	Program this field to 0x0.
1	POWERDOWN	R/W	0h	Sets the device in a low-power state. The states of other registers are maintained.
0	RESET	R/W	0h	Soft Reset. Resets the entirie logic and reigsters (equivalent to power-on reset). Self-clearing on next register write.

7.1.2 R1 Register (Offset = 1h) [Reset = 000Ah]

R1 is shown in Table 7-4.

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Table 7-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	UNDISCLOSED	R/W	0h	Program this field to 0x0.
4	LD_DIS	R/W	0h	If set to 0x1, disables the lock detect status coming out at MUXOUT pin in multiplier mode. This bit must be set to 1, when interfacing multiple devices and wants to perform a readback operation in multiplier mode. 0h = Lock Detect 1h = Readback
3	READBACK_CTRL	R/W	1h	Set this field to 0x1 to readback the written register values. Set this field to 0x0 to readback the value set by device internal state machine.
2-0	UNDISCLOSED	R/W	2h	Program this field to 0x2.

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7.1.3 R2 Register (Offset = 2h) [Reset = 00BFh]

R2 is shown in Table 7-5.

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Table 7-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	UNDISCLOSED	R	0h	Program this field to 0x0.
9	TEMPSENSE_EN	R/W	0h	Temperature sensor enable override bit
8	SYNC_EN	R/W	0h	Enables synchronization path for the dividers and allows the clock position capture circuitry to be enabled. Used for multi-device synchronization. Redundant if SYSREF_EN = 0x1.
7	UNDISCLOSED	R/W	1h	Program this field to 0x1.
6	SYSREF_EN	R/W	0h	Enables SYSREF subsystem (and SYNC subsystem when SYSREFREQ_MODE = 0x0). Setting this bit to 0x0 completely disables all SYNC, SYSREF, and clock position capture circuitry, overriding the state of other powerdown/enable bits except SYNC_EN. If SYNC_EN = 0x1, the SYNC path and clock position capture circuitry are still enabled, regardless of the state of SYSREF_EN.
5	UNDISCLOSED	R/W	1h	Program this field to 0x1.
4	LOGIC_EN	R/W	1h	Enables LOGICLK subsystem (LOGICLKOUT, LOGISYSREFOUT). Setting this bit to 0x0 completely disables all LOGICLKOUT and LOGISYSREFOUT circuitry, overriding the state of other powerdown/enable bits.
3	CH3_EN	R/W	1h	Enables CH3 (CLKOUT3, SYSREFOUT3). Setting this bit to 0 completely disables CH3, overriding the state of other powerdown/enable bits.
2	CH2_EN	R/W	1h	Enables CH2 (CLKOUT2, SYSREFOUT2). Setting this bit to 0 completely disables CH2, overriding the state of other powerdown/enable bits.
1	CH1_EN	R/W	1h	Enables CH1 (CLKOUT1, SYSREFOUT1). Setting this bit to 0 completely disables CH1, overriding the state of other powerdown/enable bits.
0	CH0_EN	R/W	1h	Enables CH0 (CLKOUT0, SYSREFOUT0). Setting this bit to 0 completely disables CH0, overriding the state of other powerdown/enable bits.

7.1.4 R3 Register (Offset = 3h) [Reset = 0000h]

R3 is shown in Table 7-6.

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Table 7-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6-0	CLKIN_DLY	R/W	0h	Sets the delay at input clock. Delay range - 60ps and step size - 1.1ps

7.1.5 R4 Register (Offset = 4h) [Reset = 000Dh]

R4 is shown in Table 7-7.

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Table 7-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	0h	Program this field to 0x0.
10-4	CLK0_DLY	R/W	0h	Sets the delay at CLKOUT0 output clock. Delay range - 55ps and step size - 0.9ps
3-1	CLK0_PWR	R/W	6h	Sets the output power of CLKOUT0. Larger values correspond to higher output power.
0	CLK0_EN	R/W	1h	Enables CLKOUT0 output buffer.

7.1.6 R5 Register (Offset = 5h) [Reset = 000Dh]

R5 is shown in Table 7-8.

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Table 7-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	0h	Program this field to 0x0.
10-4	CLK1_DLY	R/W	0h	Sets the delay at CLKOUT1 output clock. Delay range - 55ps and step size - 0.9ps
3-1	CLK1_PWR	R/W	6h	Sets the output power of CLKOUT1. Larger values correspond to higher output power.
0	CLK1_EN	R/W	1h	Enables CLKOUT1 output buffer.

7.1.7 R6 Register (Offset = 6h) [Reset = 000Dh]

R6 is shown in Table 7-9.

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Table 7-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	0h	Program this field to 0x0.
10-4	CLK2_DLY	R/W	0h	Sets the delay at CLKOUT2 output clock. Delay range - 55ps and step size - 0.9ps
3-1	CLK2_PWR	R/W	6h	Sets the output power of CLKOUT2. Larger values correspond to higher output power.
0	CLK2_EN	R/W	1h	Enables CLKOUT2 output buffer.

7.1.8 R7 Register (Offset = 7h) [Reset = 000Dh]

R7 is shown in Table 7-10.

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Table 7-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	0h	Program this field to 0x0.
10-4	CLK3_DLY	R/W	0h	Sets the delay at CLKOUT3 output clock. Delay range - 55ps and step size - 0.9ps
3-1	CLK3_PWR	R/W	6h	Sets the output power of CLKOUT3. Larger values correspond to higher output power.
0	CLK3_EN	R/W	1h	Enables CLKOUT3 output buffer.

7.1.9 R8 Register (Offset = 8h) [Reset = 5CA9h]

R8 is shown in Table 7-11.

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Table 7-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	SYSREF0_PWR_LOW	R/W	1h	Sets the SYSREFOUT0 output deriver at low power. Set to value 0 for single ended higher swing.
13	SYSREF0_AC	R/W	0h	Enables SYSREFOUT0 AC coupled mode.
12-10	UNDISCLOSED	R/W	7h	Program this field to 0x7.
9-4	SYSREF0_VCM	R/W	Ah	Sets the output common mode of SYSREFOUT0 with 25mV step size. SYSREF0_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	SYSREF0_PWR	R/W	4h	Sets the output power of SYSREFOUT0. Larger values corespond to higher output power. SYSREFOUT0_VCM must be set properly to bring the output common mode voltage within permissible limits.
0	SYSREF0_EN	R/W	1h	Enables SYSREFOUT0 output buffer.

7.1.10 R9 Register (Offset = 9h) [Reset = 5CA9h]

R9 is shown in Table 7-12.

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Table 7-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	SYSREF1_PWR_LOW	R/W	1h	Sets the SYSREFOUT1 output deriver at low power. Set to value 0 for single ended higher swing.
13	SYSREF1_AC	R/W	0h	Enables SYSREFOUT1 AC coupled mode.
12-10	UNDISCLOSED	R/W	7h	Program this field to 0x7.
9-4	SYSREF1_VCM	R/W	Ah	Sets the output common mode of SYSREFOUT1 with 25mV step size. SYSREF1_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	SYSREF1_PWR	R/W	4h	Sets the output power of SYSREFOUT1. Larger values corespond to higher output power. SYSREFOUT1_VCM must be set properly to bring the output common mode voltage within permissible limits.
0	SYSREF1_EN	R/W	1h	Enables SYSREFOUT1 output buffer.

7.1.11 R10 Register (Offset = Ah) [Reset = 5CA9h]

R10 is shown in Table 7-13.

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Table 7-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	SYSREF2_PWR_LOW	R/W	1h	Sets the SYSREFOUT2 output deriver at low power. Set to value 0 for single ended higher swing.
13	SYSREF2_AC	R/W	0h	Enables SYSREFOUT2 AC coupled mode.

Table 7-13. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	UNDISCLOSED	R/W	7h	Program this field to 0x7.
9-4	SYSREF2_VCM	R/W	Ah	Sets the output common mode of SYSREFOUT2 with 25mV step size. SYSREF2_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	SYSREF2_PWR	R/W	4h	Sets the output power of SYSREFOUT2. Larger values corespond to higher output power. SYSREFOUT2_VCM must be set properly to bring the output common mode voltage within permissible limits.
0	SYSREF2_EN	R/W	1h	Enables SYSREFOUT2 output buffer.

7.1.12 R11 Register (Offset = Bh) [Reset = 5CA9h]

R11 is shown in Table 7-14.

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Table 7-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	SYSREF3_PWR_LOW	R/W	1h	Sets the SYSREFOUT3 output deriver at low power. Set to value 0 for single ended higher swing.
13	SYSREF3_AC	R/W	0h	Enables SYSREFOUT3 AC coupled mode.
12-10	UNDISCLOSED	R/W	7h	Program this field to 0x7.
9-4	SYSREF3_VCM	R/W	Ah	Sets the output common mode of SYSREFOUT3 with 25mV step size. SYSREF3_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	SYSREF3_PWR	R/W	4h	Sets the output power of SYSREFOUT3. Larger values corespond to higher output power. SYSREFOUT3_VCM must be set properly to bring the output common mode voltage within permissible limits.
0	SYSREF3_EN	R/W	1h	Enables SYSREFOUT3 output buffer.

7.1.13 R12 Register (Offset = Ch) [Reset = 002Bh]

R12 is shown in Table 7-15.

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Table 7-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R/W	0h	Program this field to 0x0.
12-11	LOGICLK_FMT	R/W	0h	Selects the output driver format of the LOGICLKOUT output. 0h = LVDS 1h = Reserved 2h = CML 3h = Reserved
10-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-4	LOGICLK_VCM	R/W	2h	Sets the output common mode voltage of LOGICLKOUT in LVDS output format. LOGICLK_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	LOGICLK_PWR	R/W	5h	Sets the output power of LOGICLKOUT. Larger values correspond to higher output power.

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Table 7-15. R12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOGICLK_EN	R/W	1h	Enables the logic clock output buffer.

7.1.14 R13 Register (Offset = Dh) [Reset = 002Bh]

R13 is shown in Table 7-16.

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Table 7-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R/W	0h	Program this field to 0x0.
12-11	LOGISYSREF_FMT	R/W	0h	Selects the output driver format of the LOGISYSREFOUT output. 0h = LVDS 1h = Reserved 2h = CML 3h = Reserved
10-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-4	LOGISYSREF_VCM	R/W	2h	Sets the output common mode voltage of LOGISYSREFOUT in LVDS output format. LOGISYSREF_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
3-1	LOGISYSREF_PWR	R/W	5h	Sets the output power of LOGISYSREFOUT. Larger values correspond to higher output power.
0	LOGISYSREF_EN	R/W	1h	Enables the logic SYSREF output buffer.

7.1.15 R14 Register (Offset = Eh) [Reset = 0084h]

R14 is shown in Table 7-17.

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Table 7-17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOGICLK_DIV_RST	R/W	0h	Manual reset for logic clock divider.
14-13	UNDISCLOSED	R/W	0h	Program this field to 0x0.
12-3	LOGICLK_DIV	R/W	10h	Sets LOGICLK divider value. Maximum input frequency from LOGICLK_DIV_PRE must be ≤ 3200MHz. The maximum LOGICLKOUT frequency must be ≤ 800MHz to avoid amplitude degradation. 0h = Reserved 1h = Reserved 2h = /2 3h = /3 3FFh = /1023

Table 7-17. R14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LOGICLK_DIV_PRE	R/W	4h	Sets pre-divider value for logic clock divider. Output of the pre-divider must be ≤ 3.2GHz. Values other than those listed below are reserved. 1h = /1 2h = /2 4h = /4

7.1.16 R15 Register (Offset = Fh) [Reset = 0002h]

R15 is shown in Table 7-18.

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Table 7-18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	UNDISCLOSED	R/W	0h	Program this field to 0x0.
2-1	LOGICLK2_DIV	R/W	1h	Sets the divider value for LOGICLKOUT1 logic clock.
0	LOGICLK2_EN	R/W	0h	Enables the LOGICLKOUT1 0h = LOGISYSREFOUT 1h = LOGICLKOUT1

7.1.17 R16 Register (Offset = 10h) [Reset = 0030h]

R16 is shown in Table 7-19.

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Table 7-19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	UNDISCLOSED	R	0h	Program this field to 0x0.
7-6	SYSREF_DLY_SCALE	R/W	0h	Sets the frequency range of the SYSREFOUT delay generator. Set according to phase interpolator frequency. 0h = 400MHz to 800MHz 1h = 200MHz to 400MHz 2h = 150MHz to 200MHz 3h = Reserved
5-4	SYSREFREQ_DLY_STEP	R/W	3h	Sets the step size of the delay element used in the SYSREFREQ path, both for SYSREFREQ input delay and for clock position captures. The recommended frequency range for each step size creates the maximum number of usable steps for a given CLKIN frequency. The ranges include some overlap to account for process and temperature variations. If the CLKIN frequency is covered by an overlapping span, larger delay step sizes improve the likelihood of detecting a CLKIN rising edge during a clock position capture. However, since larger values include more delay steps, larger step sizes have greater total delay variation across PVT relative to smaller step sizes. 0h = 28ps (1.4GHz to 2.7GHz) 1h = 15ps (2.4GHz to 4.7GHz) 2h = 11ps (3.1GHz to 5.7GHz) 3h = 8ps (4.5GHz to 12.8GHz)

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Table 7-19. R16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	SYSREFREQ_VCM_OFFSET	R/W	0h	Sets the voltage offset at SYSREFREQ P vs N 0h = 25mV 1h = 50mV 2h = 100mV 3h = 150mV
1-0	SYSREFREQ_VCM	R/W	0h	Sets the SYSREFREQ input pins common mode voltage 0h = Zero offset (AC coupled) 1h = Pin P biased higher than pin N (AC coupled) 2h = Pin N higher than pin P (AC coupled) 3h = No Bias (DC coupled)

7.1.18 R17 Register (Offset = 11h) [Reset = 0005h]

R17 is shown in Table 7-20.

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Table 7-20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R	0h	Program this field to 0x0.
11-8	UNDISCLOSED	R/W	0h	Program this field to 0x0.
7-6	SYSREFREQ_INPUT	R/W	0h	Sets the functionality of the SYSREFREQ block 0h = SYSREFREQ Pin 1h = Force Low 2h = Reserved 3h = Force High
5	SYSWND_UPDATE_STOP	R/W	0h	Stops the windowing after setting bit to high.
4	SYNC_STOP	R/W	0h	Stops the reset generation after setting bit to high.
3	SYSWND_LATCH	R/W	0h	Sets the SYSREF Windowing at first rising edge of the SYNC input
2	SYSREFREQ_CLR	R/W	1h	Reset synchronization path timing for SYSREFREQ signal. Holding this bit high keeps internal SYSREFREQ signal low in all modes except SYSREF repeater mode, overriding the state of SYSREFREQ_INPUT[0]. This bit must be set and cleared once before the SYNC or clock position capture operations are performed.
1-0	SYSREFREQ_MODE	R/W	1h	Sets the SYSREFREQ input mode function 0h = SYNC 1h = SYSREFREQ 2h = SYSREF Windowing 3h = Reserved

7.1.19 R18 Register (Offset = 12h) [Reset = 0000h]

R18 is shown in Table 7-21.

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Table 7-21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	UNDISCLOSED	R	0h	Program this field to 0x0.
5-0	SYSREFREQ_DLY	R/W	0h	Sets the delay line step for the external SYSREFREQ signal. Each delay line step delays the SYSREFREQ signal by an amount equal to SYSREFREQ_DLY x SYSREFREQ_DLY_STEP. In SYNC mode, the value for this field can be determined based on the rb_CLKPOS value to satisfy the internal setup and hold time of the SYNC signal with respect to the CLKIN signal. In SYSREF Repeater Mode, the value for this field can be used as a coarse global delay. Values greater than 0x3F are invalid. Since larger values include more delay steps, larger values have greater total step size variation across PVT relative to smaller values. Refer to the data sheet or the device TICS Pro profile for detailed description of the delay step computation procedure.

7.1.20 R19 Register (Offset = 13h) [Reset = 0004h]

R19 is shown in Table 7-22.

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Table 7-22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	UNDISCLOSED	R	0h	Program this field to 0x0.
6	SYSREF_DLY_BYP	R/W	0h	Sets the SYSREF delay bypass
5-2	SYSREF_PULSE_CNT	R/W	1h	Programs the number of pulses generated in pulser mode. The pulser is a counter gating the SYSREF divider; consequently, the pulse duration and frequency are equal to the duty cycle and frequency of the SYSREF divider output, respectively. 0h = Reserved 1h = 1 pulse 2h = 2 pulses Fh = 15 pulses
1-0	SYSREF_MODE	R/W	0h	Controls how the SYSREF signal is generated and is also impacted by the SYSREF_DLY_BYP field. Continuous mode generates a continuous SYSREF clock that is derived from the SYSREF divider and delay. In pulser mode, a pulse at the SYSREFREQ pin causes a specific number (determined by SYSREF_PULSE_CNT) of pulses to be generated for the SYSREF outputs. In Repeater mode, a pulse at the SYSREFREQ pins generates a single pulse at the SYSREF outputs and only the propagation delay through the device is added. 0h = Continuous 1h = Pulser 2h = Repeater 3h = Repeater Retime

7.1.21 R20 Register (Offset = 14h) [Reset = 8082h]

R20 is shown in Table 7-23.

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Table 7-23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SYSREF_DLY_DIV	R/W	2h	Sets the delay generator clock division, determining fINTERPOLATOR and the delay generator resolution. 0h = /2 (≤ 1.6GHz) 1h = /4 (1.6GHz to 3.2GHz) 2h = /8 (3.2GHz to 6.4GHz) 4h = /16 (6.4GHz to 12.8GHz)
13-2	SYSREF_DIV	R/W	20h	Sets the SYSREF divider. Maximum input frequency from SYSREF_DIV_PRE must be ≤ 3200MHz. Maximum output frequency must be ≤ 100MHz. Odd divides (with duty cycle < 50%) are only allowed when the delay generators are bypassed. 0h = Reserved 1h = Reserved 2h = /2 3h = /3 FFFh = /4095
1-0	SYSREF_DIV_PRE	R/W	2h	Sets the SYSREF pre-divider. Maximum output frequency must be ≤ 3.2GHz. 0h = /1 1h = /2 2h = /4 3h = Reserved

7.1.22 R21 Register (Offset = 15h) [Reset = 01FCh]

R21 is shown in Table 7-24.

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Table 7-24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-2	SYSREF0_DLY	R/W	7Fh	Sets the delay step for the SYSREFOUT0 delay generator. In each quadrant, delay has 127 steps.
1-0	SYSREF0_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT0 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = ICLK 3h = QCLK

7.1.23 R22 Register (Offset = 16h) [Reset = 01FCh]

R22 is shown in Table 7-25.

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Table 7-25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.

Table 7-25. R22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-2	SYSREF1_DLY	R/W	7Fh	Sets the delay step for the SYSREFOUT1 delay generator. In each quadrant, delay has 127 steps.
1-0	SYSREF1_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT1 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK

7.1.24 R23 Register (Offset = 17h) [Reset = 01FCh]

R23 is shown in Table 7-26.

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Table 7-26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-2	SYSREF2_DLY	R/W	7Fh	Sets the delay step for the SYSREFOUT2 delay generator. In each quadrant, delay has 127 steps.
1-0	SYSREF2_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT2 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK

7.1.25 R24 Register (Offset = 18h) [Reset = 01FCh]

R24 is shown in Table 7-27.

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Table 7-27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-2	SYSREF3_DLY	R/W	7Fh	Sets the delay step for the SYSREFOUT3 delay generator. In each quadrant, delay has 127 steps.
1-0	SYSREF3_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the SYSREFOUT3 delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK

7.1.26 R25 Register (Offset = 19h) [Reset = 01FCh]

R25 is shown in Table 7-28.

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Table 7-28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8-2	LOGISYSREF_DLY	R/W	7Fh	Sets the delay step for the LOGISYSREF delay generator. In each quadrant, delay has 127 steps.
1-0	LOGISYSREF_DLY_PHASE	R/W	0h	Sets the quadrature phase of the interpolator clock used for the LOGISYSREFOUT delay generator retimer. 0h = ICLK' 1h = QCLK' 2h = QCLK 3h = ICLK

7.1.27 R26 Register (Offset = 1Ah) [Reset = 00D1h]

R26 is shown in Table 7-29.

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Table 7-29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	UNDISCLOSED	R/W	0h	Program this field to 0x0.
7-5	SMCLK_DIV	R/W	6h	Sets state machine clock divider. Further divides the output of the state machine clock pre-divider. Input frequency from SMCLK_DIV_PRE must be ≤ 1600MHz. Output frequency must be ≤ 30MHz. Divide value is 2^{SMCLK_DIV}. 0h = /1 1h = /2 2h = /4 3h = /8 4h = /16 5h = /32 6h = /64 7h = /128
4-1	SMCLK_DIV_PRE	R/W	8h	Pre-divider for State Machine clock (one hot divider).The state machine clock is divided from the input clock. The output of the pre-divider must be ≤1600MHz. Values other than those listed are reserved. 2h = /2 4h = /4 8h = /8
0	SMCLK_EN	R/W	1h	Enables the state machine clock generator. Only required to calibrate the multiplier, and for multiplier lock detect (including on MUXOUT pin). If the multiplier is not used, or if the multiplier lock detect feature is not used, the state machine clock generator can be disabled to minimize crosstalk.

7.1.28 R27 Register (Offset = 1Bh) [Reset = 3609h]

R27 is shown in Table 7-30.

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Table 7-30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	3h	Program this field to 0x3.
11	MULT_HIPFD_EN	R/W	0h	Above 4.2GHz frequency in multiplier mode, to optimized the current, toggle this bit low to high along with R0. To set the bit high without R0, increase a current with 20mA.
10	UNDISCLOSED	R/W	1h	Program this field to 0x1.
9	FCAL_EN	R/W	1h	Enables Frequency calibration. Writing this register with this bit high triggers a multiplier frequency calibration. If the multiplier is unused, set to 0.
8-7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6	CLK_DIV_RST	R/W	0h	Resets the main clock divider. If the clock divider value is changed during operation, set this bit high then low after setting the new divider value. Synchronizing the device with the SYSREFREQ pins in SYSREFREQ_MODE = 0x0 and SYNC_EN = 0x1 also resets the main clock divider. This bit has no effect when outside of Divider Mode.
5-3	CLK_DIV	R/W	1h	CLK_DIV and CLK_MULT are aliases for the same field. When CLK_MUX=1 (Buffer Mode), this field is ignored. When CLK_MUX = 2 (Divider Mode), the clock divider is CLK_DIV + 1. Valid range for CLK_DIV is 1 to 7. Setting this to 0 disables the main clock divider and reverts to buffer mode. When CLK_MUX = 3 (Multiplier Mode), CLK_MULT the multiplier vaue is CLK_MULT. Valid range is 1 to 7.
2-0	CLK_MUX	R/W	1h	Selects the function for the main clock outputs 0h = Reserved 1h = Buffer 2h = Dividers 3h = Multiplier

7.1.29 R29 Register (Offset = 1Dh) [Reset = 0000h]

R29 is shown in Table 7-31.

Return to the Summary Table.

Table 7-31. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_CLKPOS[31:16]	R	0h	Stores a snapshot of the CLKIN signal rising edge positions relative to a SYSREFREQ rising edge, with the snapshot starting from the LSB and ending at the MSB. Each bit represents a sample of the CLKIN signal, separated by a delay determined by the SYSREFREQ_DLY_STEP field. The first and last bits of rb_CLKPOS are always set, indicating uncertainty at the capture window boundary conditions. CLKIN rising edges are represented by every sequence of two set bits from LSB to MSB, including bits at the boundary conditions. The position of the CLKIN rising edges in the snapshot, along with the CLKIN signal period and the delay step size, can be used to compute the value of SYSREFREQ_DLY_STEP which maximizes setup and hold times for SYNC signals on the SYSREFREQ pins.

7.1.30 R30 Register (Offset = 1Eh) [Reset = 0000h]

R30 is shown in Table 7-32.

Return to the Summary Table.

Table 7-32. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_CLKPOS	R	0h	LSBs of rb_CLKPOS field.

7.1.31 R31 Register (Offset = 1Fh) [Reset = 0000h]

R31 is shown in Table 7-33.

Return to the Summary Table.

Table 7-33. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UNDISCLOSED	R	0h	Program this field to 0x0.
13-11	UNDISCLOSED	R	0h	Program this field to 0x0.
10-0	rb_TEMPSENSE	R	0h	Readback value of on-die temperature sensor.

7.1.32 R32 Register (Offset = 20h) [Reset = 0000h]

R32 is shown in Table 7-34.

Return to the Summary Table.

Table 7-34. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_VER_ID	R	0h	Version ID.

7.1.33 R36 Register (Offset = 24h) [Reset = 84A3h]

R36 is shown in Table 7-35.

Return to the Summary Table.

Table 7-35. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	UNDISCLOSED	R/W	21h	Program this field to 0x42.
9-8	UNDISCLOSED	R/W	0h	Program this field to 0x3.
7-6	UNDISCLOSED	R/W	2h	Program this field to 0x0.
5-0	UNDISCLOSED	R/W	23h	Program this field to 0x16.

7.1.34 R37 Register (Offset = 25h) [Reset = 0000h]

R37 is shown in Table 7-36.

Return to the Summary Table.

Table 7-36. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R	0h	Program this field to 0x0.
14-1	UNDISCLOSED	R	0h	Program this field to 0x0.
0	rb_LOCK_DETECT	R	0h	Reads back the lock detect status in multiplier mode 0h = Unlock 1h = Lock Detect

7.1.35 R39 Register (Offset = 27h) [Reset = 78E1h]

R39 is shown in Table 7-37.

Return to the Summary Table.

Table 7-37. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	4h	Program this field to 0x4.
8-4	UNDISCLOSED	R/W	Eh	Program this field to 0x16.
3-0	UNDISCLOSED	R/W	1h	Program this field to 0x1.

7.1.36 R40 Register (Offset = 28h) [Reset = 78E1h]

R40 is shown in Table 7-38.

Return to the Summary Table.

Table 7-38. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	4h	Program this field to 0x4.
8-4	UNDISCLOSED	R/W	Eh	Program this field to 0x16.
3-0	UNDISCLOSED	R/W	1h	Program this field to 0x3.

7.1.37 R41 Register (Offset = 29h) [Reset = 78F3h]

R41 is shown in Table 7-39.

Return to the Summary Table.

Table 7-39. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	4h	Program this field to 0x2.
8-4	UNDISCLOSED	R/W	Fh	Program this field to 0x14.
3-0	UNDISCLOSED	R/W	3h	Program this field to 0x1.

7.1.38 R42 Register (Offset = 2Ah) [Reset = 76F3h]

R42 is shown in Table 7-40.

Return to the Summary Table.

Table 7-40. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	3h	Program this field to 0x3.
8-4	UNDISCLOSED	R/W	Fh	Program this field to 0x14.
3-0	UNDISCLOSED	R/W	3h	Program this field to 0x1.

7.1.39 R43 Register (Offset = 2Bh) [Reset = 7707h]

R43 is shown in Table 7-41.

Return to the Summary Table.

Table 7-41. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	3h	Program this field to 0x3.
8-4	UNDISCLOSED	R/W	10h	Program this field to 0x14.
3-0	UNDISCLOSED	R/W	7h	Program this field to 0x1.

7.1.40 R44 Register (Offset = 2Ch) [Reset = 7707h]

R44 is shown in Table 7-42.

Return to the Summary Table.

Table 7-42. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	7h	Program this field to 0x7.
11-9	UNDISCLOSED	R/W	3h	Program this field to 0x2.
8-4	UNDISCLOSED	R/W	10h	Program this field to 0x16.
3-0	UNDISCLOSED	R/W	7h	Program this field to 0x1.

7.1.41 R45 Register (Offset = 2Dh) [Reset = 2ABFh]

R45 is shown in Table 7-43.

Return to the Summary Table.

Table 7-43. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UNDISCLOSED	R/W	2h	Program this field to 0x2.
11-10	UNDISCLOSED	R/W	2h	Program this field to 0x3.
9-8	UNDISCLOSED	R/W	2h	Program this field to 0x3.
7-6	UNDISCLOSED	R/W	2h	Program this field to 0x3.
5-4	UNDISCLOSED	R/W	3h	Program this field to 0x3.
3-2	UNDISCLOSED	R/W	3h	Program this field to 0x3.
1-0	UNDISCLOSED	R/W	3h	Program this field to 0x3.

7.1.42 R54 Register (Offset = 36h) [Reset = 0000h]

R54 is shown in Table 7-44.

Return to the Summary Table.

Table 7-44. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	UNDISCLOSED	R	0h	Program this field to 0x0.
13-4	UNDISCLOSED	R/W	0h	Program this field to 0x0.
3-2	UNDISCLOSED	R/W	0h	Program this field to 0x3.

Table 7-44. R54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	UNDISCLOSED	R/W	0h	Program this field to 0x2.

7.1.43 R55 Register (Offset = 37h) [Reset = 0000h]

R55 is shown in Table 7-45.

Return to the Summary Table.

Table 7-45. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	UNDISCLOSED	R/W	0h	Program this field to 0x0.
5-0	DEV_IOPT_CTRL	R/W	0h	Set this field to 0x6 in all modes, also in powerdown. Set this field to 0x6 before calibration in multiplier mode and changed to 0x1 after calibration

7.1.44 R77 Register (Offset = 4Dh) [Reset = 0000h]

R77 is shown in Table 7-46.

Return to the Summary Table.

Table 7-46. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	UNDISCLOSED	R/W	0h	Program this field to 0x0.
1-0	UNDISCLOSED	R/W	0h	Program this field to 0x2.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Reference

8.1.1 Typical Application

For this application, the additive noise impact of using the LMX1205 as a buffer is explored when added to the LMX2820 6.4GHz output clock. This particular setup uses a single-ended clock to drive the LMX1205 to combine two EVMs together, but driving the setup differentially is generally recommended.

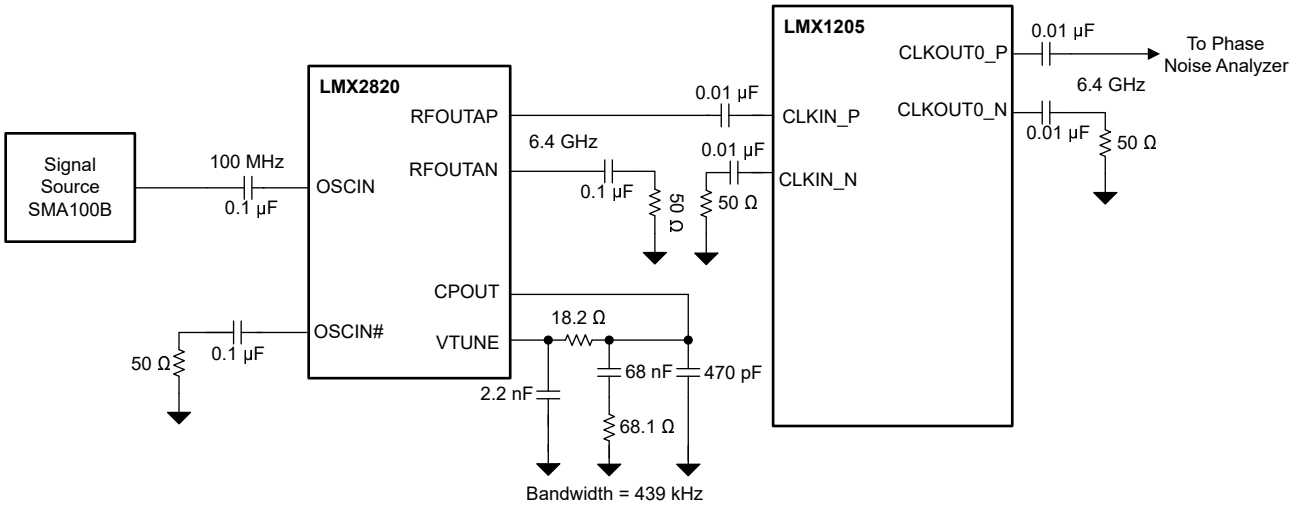

Figure 8-1. Typical Application Schematic

8.1.1.1 Design Requirements

Table 8-1 shows the design parameters for this example.

If not all outputs are used, TI recommends to compress the layout to minimize trace lengths, especially that of the input trace.

Table 8-1. Design Parameters

PARAMETER	VALUE
LMX2820 Input Frequency	100MHz
LMX2820 Output Frequency	6.4GHz
LMX1205 Input Clock Frequency	6.4GHz
LMX1205 Output Clock Frequency	6.4GHz
LMX1205	Buffer Mode

8.1.1.2 Detailed Design Procedure

In this example, a 6.4GHz input clock is being buffered at output clock. The external components do not change that much based on internal configuration. The TICS Pro software is very useful in calculating the necessary register values and configuring the device.

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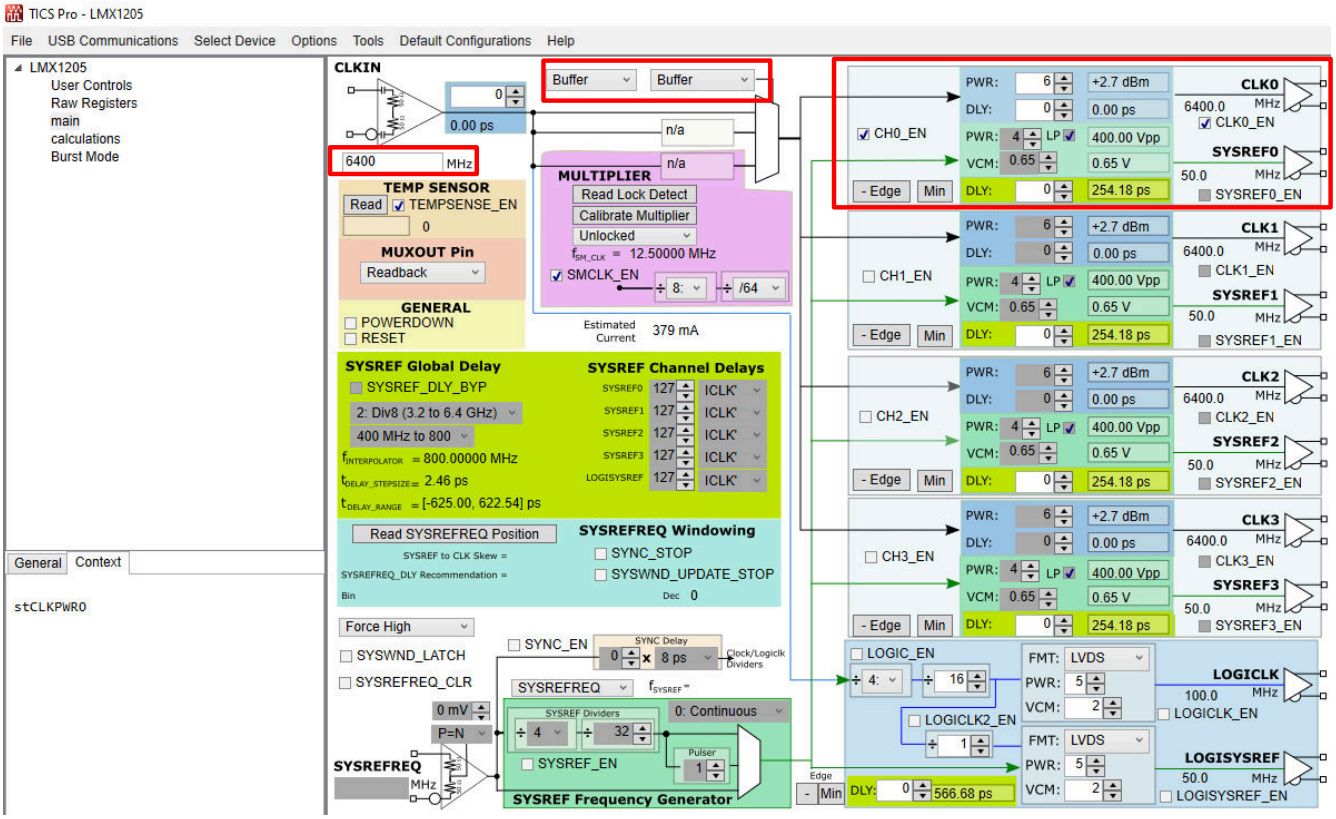

Figure 8-2. LMX1205 TICS Pro Setup

8.1.1.3 Application Plots

Below Figure shows the total plot is the sum of the noise of the LMX1205 in buffer mode and the LMX2820 6.4GHz output. LMX1205 follow the same noise curve of LMX2820.

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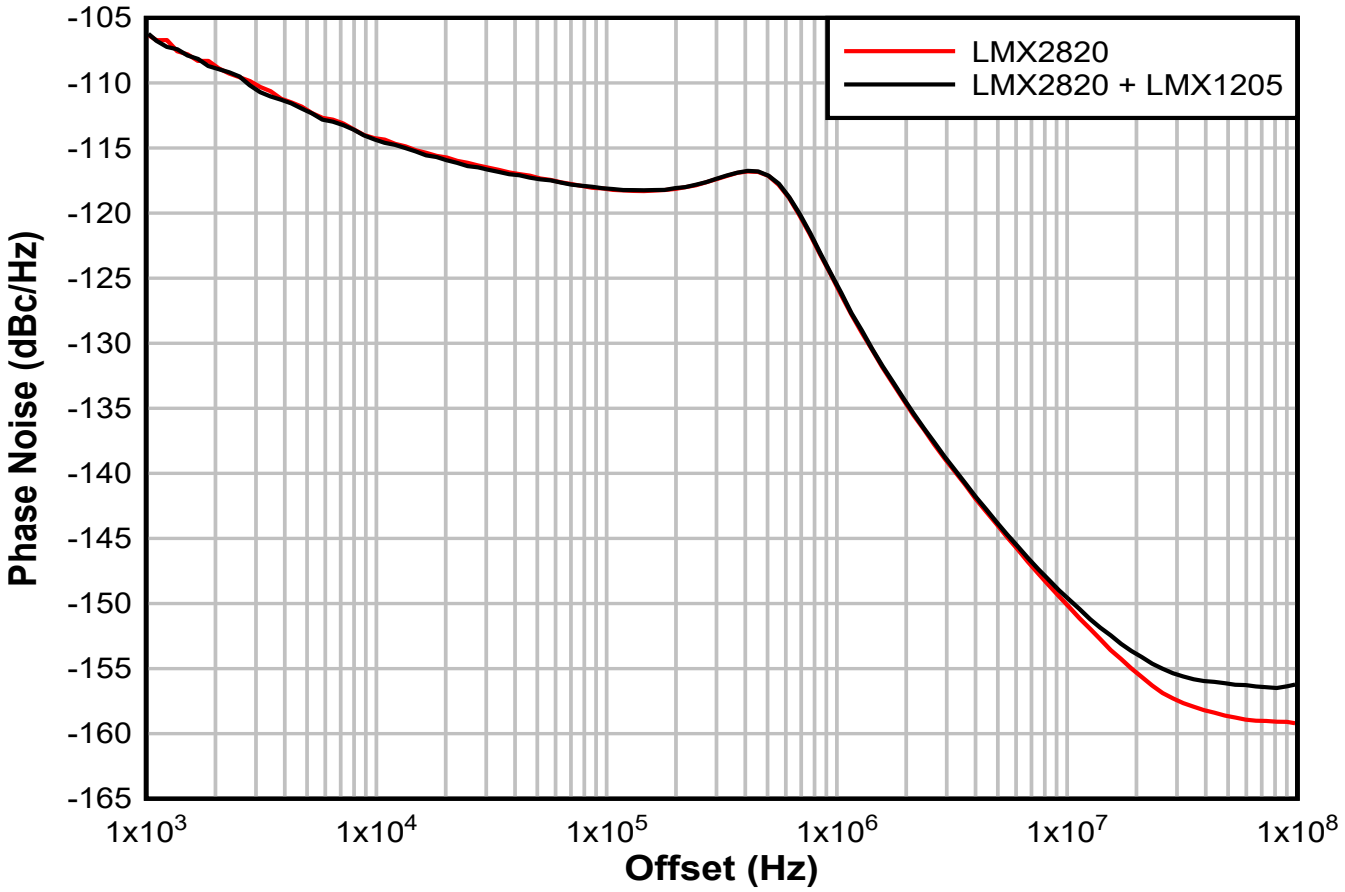

Figure 8-3. LMX1205 Buffer Mode Output

8.2 Power Supply Recommendations

This devices uses a 2.5V supply for the whole device. A direct connection to a switching power supply likely results in unwanted spurs at the output. Bypassing can be done individually at all the power pins. TI recommends placing smaller capacitors with higher frequency of minimum impedance on the same layer as the device, as close to the pins as possible. The frequencies of nearly all signals in the device are 100MHz or greater, therefore larger value bypass capacitors with low frequency of minimum impedance are only used for internal LDO stability, and the distance to the device (and the loop inductance of the bypass path) can be larger. Isolate the supply pins for the clocks and the LOGICLK with a small resistor or ferrite bead if both are being used simultaneously. See the *Pin Configuration and Functions* section for additional recommendations for each pin.

Note

This device has minimal PSRR due to the low operating voltage and internal filtering by LDOs. Connecting this device to a low noise supply that does not have excessive spurious noise is important.

8.3 Layout

8.3.1 Layout Guidelines

- If using an output single-ended, terminate the complementary side so that the impedance as seen looking out from the complementary side is similar to side that is used.
- GND pins on the outer perimeter of the package can be routed on the package back to the DAP.
- Minimize the length of the CLKIN trace for optimal phase noise. Poor matching can degrade the noise floor.
- Verify that the DAP on device is well-grounded with many vias.

- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- Be aware that if all the outputs and SYSREF are operating, the current consumption can be high enough to exceed the recommended internal junction temperature of 125°C; a heat sink can be necessary.

8.3.2 Layout Example

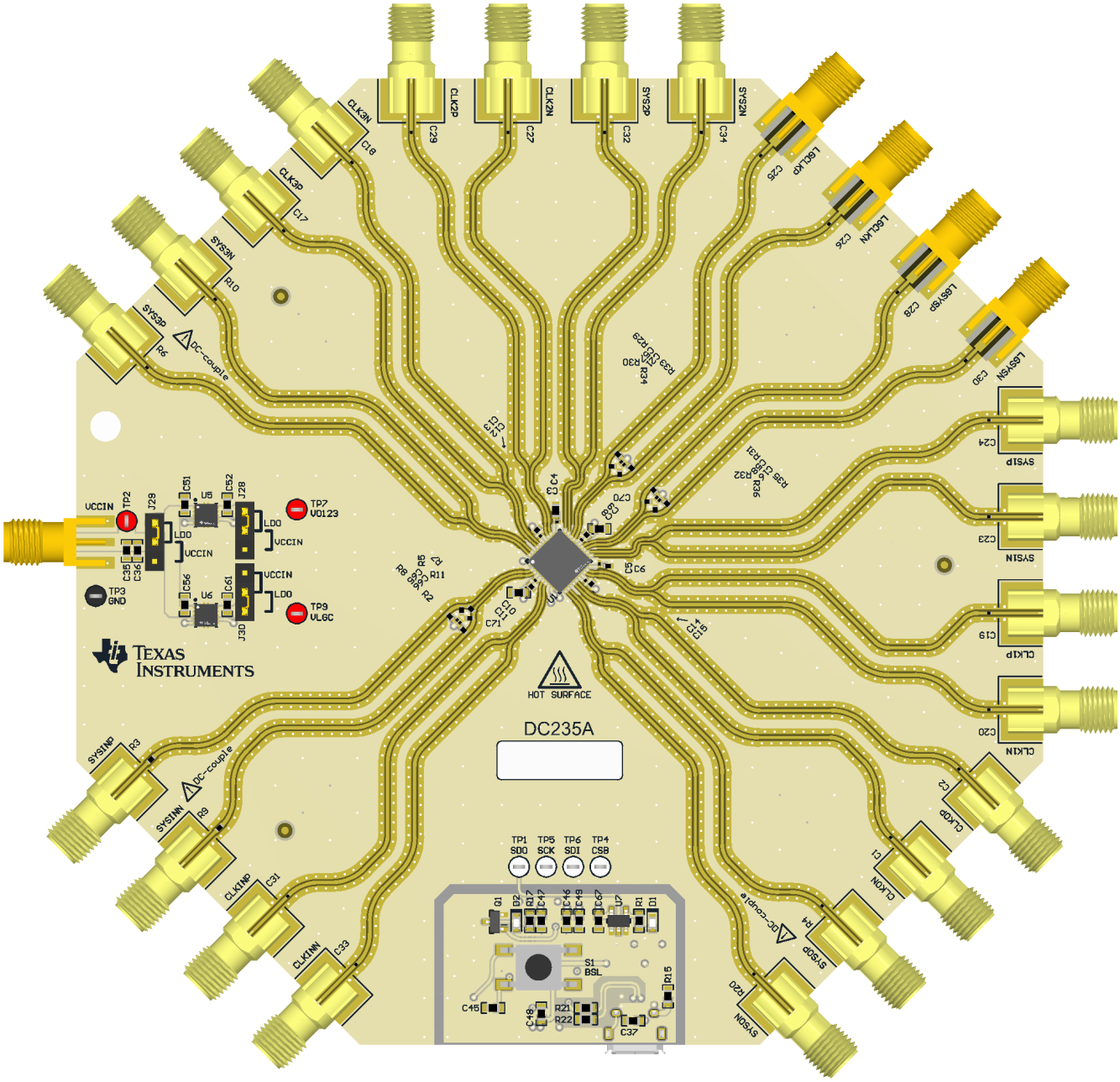

Figure 8-4. Layout Example

9 Device and Documentation Support

9.1 Device Support

TI offers an extensive line of development tools and software to simulate the device performance and program the device.

ADVANCE INFORMATION

Table 9-1. Development Tools and Software

TOOL	TYPE	DESCRIPTION
PLLatinum™ Sim	Software	Simulates phase noise in all modes
TICS Pro	Software	Programs the device with a user-friendly GUI with interactive feedback and hex register export.

9.2 Documentation Support

9.2.1 Related Documentation

Texas Instruments, *LMX1205 Evaluation Module*, EVM user's guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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