LMZ10504 最大入力電圧 5.5V の 4A パワー・モジュール

1 特長

- シールド付きインダクタを内蔵
- 外部のソフトスタート、トラッキング、高精度イネーブルによる柔軟なスタートアップ・シーケンシング
- 突入電流と、入力UVLOや出力短絡などのフォルトに対する保護
- 単一の露出パッドと標準ピン配置により取り付けと製造が容易
- 他のデバイスとピン単位で互換
  - LMZ10503 (最大3A/15W)
  - LMZ10505 (最大5A/25W)
- WEBENCH®およびPower Designerに完全対応
- 電気的特性
  - 最大合計出力電力: 20W
  - 最大4Aの出力電流
  - 入力電圧範囲: 2.95V～5.5V
  - 出力電圧範囲: 0.8V～5V
  - 温度範囲全体にわたって±1.63%の帰還電圧精度
- 性能上の利点
  - 高い周囲温度で動作
  - 最大96%の高効率によるシステム発熱の低減
  - EN55022 Class B標準でテスト済みの低い放射性エミッション(EMI) (EN 55022:2006、+A1:2007、FCC Part 15 Subpart B: 2007。テスト対象のデバイスの情報については、Table 9および「レイアウト」を参照)
  - 10V/m放射耐性EMIテスト標準EN61000 4-3に合格
  - FPGAやASICへの電源供給に適した高速な過渡応答
- WEBENCH® Power Designerにより、LMZ10504を使用するカスタム設計を作成

2 アプリケーション

- 3.3Vおよび5Vレールからのポイント・オブ・ロード(POL)変換
- スペースに制約のあるアプリケーション
- ノイズに敏感なアプリケーション(トランシーバや医療用など)

3 概要

LMZ10504 電源モジュールは使いやすい包括的な DC-DC ソリューションで、非常に優れた電力変換効率、出力電圧精度、ラインおよび負荷レギュレーションにより、最大 4A の負荷を駆動できます。LMZ10504の革新的なパッケージは、熱特性を強化するとともに、人手でも機械でもハンダ付けできます。

LMZ10504は2.95V～5.5Vの範囲の入力電圧レールを受け付け、最低0.8Vの可変出力電圧を高精度で供給できます。1MHzの固定周波数PWMスイッチングにより、EMI特性が予測可能です。2つの外付け補償部品を調整することで、最短の応答時間を設定でき、セラミックや電解出力コンデンサも使用できます。外部でプログラム可能なソフトスタート・コンデンサにより、制御されたスタートアップを容易に実現できます。LMZ10504は信頼性が高く堅牢なソリューションで、無損失のサイクル単位ピーク電流制限による過電流または短絡フォルト保護、サーマル・シャットダウン、入力低電圧誤動作防止、プリバイアス・スタートアップの機能があります。

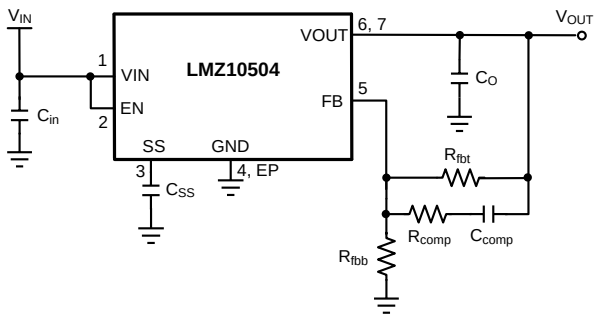
製品情報(1)(2)

型番	パッケージ	本体サイズ(公称)
LMZ10504	TO-PMOD (7)	9.85mm×10.16mm

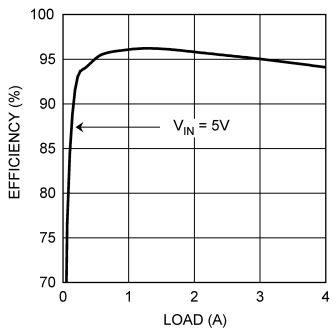
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) ピーク・リフロー温度は245℃です。詳細については、『*Design Summary LMZ1xxx and LMZ2xxx Power Module Family*』(英語) を参照してください。

代表的なアプリケーション回路



V_{OUT} = 3.3Vでの効率



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision O (June 2017) から Revision P に変更 **Page**

- 編集上の変更のみ、技術上の変更なし ... 1

Revision N (September 2015) から Revision O に変更 **Page**

- データシートにWEBENCHのコンテンツおよびリンクを追加、WEBENCHリスト項目の内容を 変更 ... 1

Revision M (October 2013) から Revision N に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

Revision L (April 2013) から Revision M に変更 **Page**

- Deleted 10 mils ... 4
- Changed 10 mils ... 23
- Changed 10 mils ... 26
- Added *Power Module SMT Guidelines* ... 27

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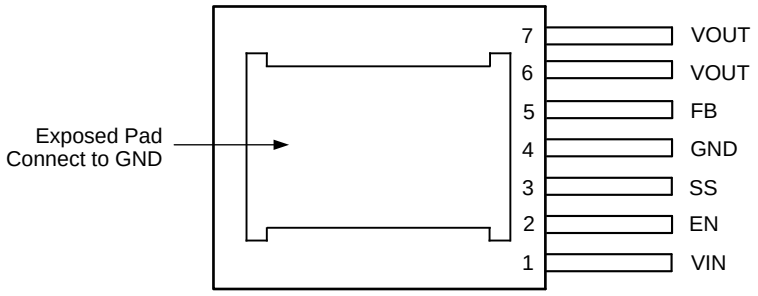
5 Pin Configuration and Functions

NDW Package
7-Lead TO-PMOD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Analog	Active-high enable input for the device.
Exposed Pad	—	Ground	Exposed pad is used as a thermal connection to remove heat from the device. Connect this pad to the PCB ground plane in order to reduce thermal resistance value. EP must also provide a direct electrical connection to the input and output capacitors ground terminals. Connect EP to pin 4.
FB	5	Analog	Feedback pin. This is the inverting input of the error amplifier used for sensing the output voltage. Keep the copper area of this node small.
GND	4	Ground	Power ground and signal ground. Provide a direct connection to the EP. Place the bottom feedback resistor as close as possible to GND and FB pin.
SS	3	Analog	Soft-start control pin. An internal 2-µA current source charges an external capacitor connected between SS and GND pins to set the output voltage ramp rate during start-up. The SS pin can also be used to configure the tracking feature.
VIN	1	Power	Power supply input. A low-ESR input capacitance should be located as close as possible to the VIN pin and exposed pad (EP).
VOUT	6, 7	Power	The output terminal of the internal inductor. Connect the output filter capacitor between VOUT pin and EP.

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6 Specifications

6.1 Absolute Maximum Ratings[1][2][3]

	MIN	MAX	UNIT
VIN, VOUT, EN, FB, SS to GND	–0.3	6	V
Power dissipation	Internally Limited		
Junction temperature		150	°C
Peak reflow case temperature (30 s)		245	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, refer to the *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. Test method is per JESD22-AI14S.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN to GND	2.95	5.5	V
Junction temperature (T_J)	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMZ10504 NDW (TO-PMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	20	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (no air flow)	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) $R_{\theta JA}$ measured on a 2.25-in × 2.25-in (5.8 cm × 5.8 cm) 4-layer board, with 1-oz. copper, thirty six thermal vias, no air flow, and 1-W power dissipation. Refer to *Layout Examples* or *AN-2022 LMZ1050x Evaluation Board* (SNVA421).

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6.5 Electrical Characteristics

Specifications are for T_J = 25°C unless otherwise specified. Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = V_{EN} = 3.3 V, unless otherwise indicated in the conditions column.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS							
V_{FB}	Total feedback voltage variation including line and load regulation	V_{IN} = 2.95 V to 5.5 V V_{OUT} = 2.5 V I_{OUT} = 0 A to 4 A			0.8		V
			over the operating junction temperature range T_J of –40°C to 125°C	0.78		0.82	
V_{FB}	Feedback voltage variation	V_{IN} = 3.3 V, V_{OUT} = 2.5 V I_{OUT} = 0 A			0.8		V
			over the operating junction temperature range T_J of –40°C to 125°C	0.787		0.812	
V_{FB}	Feedback voltage variation	V_{IN} = 3.3 V, V_{OUT} = 2.5 V I_{OUT} = 4 A			0.798		V
			over the operating junction temperature range T_J of –40°C to 125°C	0.785		0.81	
$V_{IN(UVLO)}$	Input UVLO threshold (measured at VIN pin)	Rising			2.6		V
			over the operating junction temperature range T_J of –40°C to 125°C			2.95	
		Falling			2.4		
			over the operating junction temperature range T_J of –40°C to 125°C	1.95			
I_{SS}	Soft-start current	Charging Current			2		µA
I_Q	Non-switching input current	V_{FB} = 1 V			1.7		mA
			over the operating junction temperature range T_J of –40°C to 125°C			3	
I_{SD}	Shutdown quiescent current	V_{IN} = 5.5 V, V_{EN} = 0 V			260		µA
			over the operating junction temperature range T_J of –40°C to 125°C			500	
I_{OCL}	Output current limit (average current)	V_{OUT} = 2.5 V			5.5		A
			over the operating junction temperature range T_J of –40°C to 125°C	4.1		6.7	
f_{FB}	Frequency foldback	In current limit			250		kHz
PWM SECTION							
f_{SW}	Switching frequency				1000		kHz
		over the operating junction temperature range T_J of –40°C to 125°C		750		1160	
D_{range}	PWM duty cycle range	over the operating junction temperature range T_J of –40°C to 125°C		0%		100%	
ENABLE CONTROL							
V_{EN-IH}	EN pin rising threshold				1.23		V
		over the operating junction temperature range T_J of –40°C to 125°C				1.8	
V_{EN-IF}	EN pin falling threshold				1.06		V
		over the operating junction temperature range T_J of –40°C to 125°C		0.8			

(1) Minimum and maximum limits are 100% production tested at an ambient temperature (T_A) of 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

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Electrical Characteristics (continued)

Specifications are for T_J = 25°C unless otherwise specified. Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = V_{EN} = 3.3 V, unless otherwise indicated in the conditions column.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
THERMAL CONTROL						
T_{SD}	T_J for thermal shutdown			145		°C
T_{SD-HYS}	Hysteresis for thermal shutdown			10		°C
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output voltage ripple	Refer to Table 1 V_{OUT} = 2.5 V Bandwidth Limit = 2 MHz		10		mV_{pk-pk}
		Refer to Table 5 bandwidth limit = 20 MHz		5		
ΔV_{FB} / V_{FB}	Feedback voltage line regulation	ΔV_{IN} = 2.95 V to 5.5 V I_{OUT} = 0 A		0.04%		
		I_{OUT} = 0 A to 4 A		0.25%		
ΔV_{OUT} / V_{OUT}	Output voltage line regulation	ΔV_{IN} = 2.95 V to 5.5 V I_{OUT} = 0 A, V_{OUT} = 2.5 V		0.04%		
		I_{OUT} = 0 A to 4 A V_{OUT} = 2.5 V		0.25%		
EFFICIENCY						
η	Peak efficiency (1 A) V_{IN} = 5 V	V_{OUT} = 3.3 V		96.1%		
		V_{OUT} = 2.5 V		94.8%		
		V_{OUT} = 1.8 V		93.1%		
		V_{OUT} = 1.5 V		92%		
		V_{OUT} = 1.2 V		90.4%		
		V_{OUT} = 0.8 V		86.8%		
η	Peak efficiency (1 A) V_{IN} = 3.3 V	V_{OUT} = 2.5 V		95.7%		
		V_{OUT} = 1.8 V		94.1%		
		V_{OUT} = 1.5 V		93%		
		V_{OUT} = 1.2 V		91.6%		
		V_{OUT} = 0.8V		88.3%		
η	Full load efficiency (4 A) V_{IN} = 5 V	V_{OUT} = 3.3 V		94.1%		
		V_{OUT} = 2.5 V		92.4%		
		V_{OUT} = 1.8 V		90%		
		V_{OUT} = 1.5 V		88.3%		
		V_{OUT} = 1.2 V		86.1%		
		V_{OUT} = 0.8 V		80.8%		
η	Full load efficiency (4 A) V_{IN} = 3.3 V	V_{OUT} = 2.5 V		91.4%		
		V_{OUT} = 1.8 V		90%		
		V_{OUT} = 1.5 V		87.2%		
		V_{OUT} = 1.2 V		84.9%		
		V_{OUT} = 0.8 V		79.3%		

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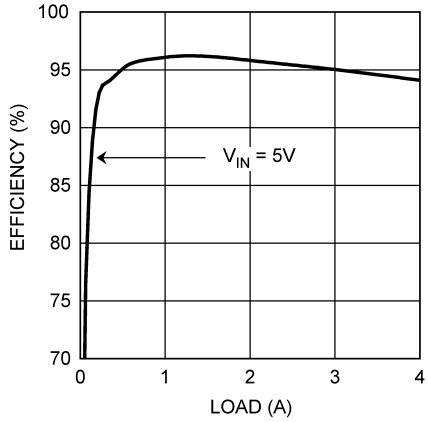
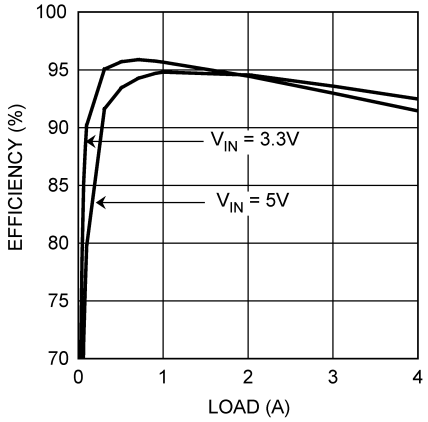
6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = V_{EN} = 5 V, C_{IN} is 47-µF 10-V X5R ceramic capacitor; T_A = 25°C for efficiency curves and waveforms.



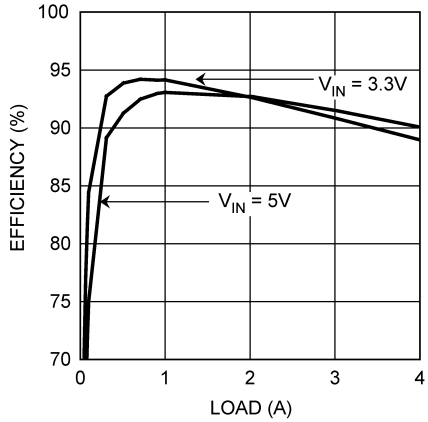
V_{OUT} = 3.3 V

Figure 1. Efficiency



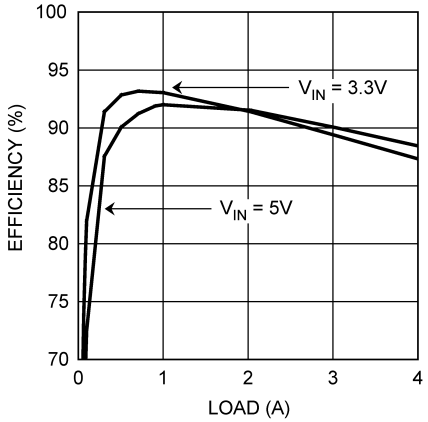
V_{OUT} = 2.5 V

Figure 2. Efficiency



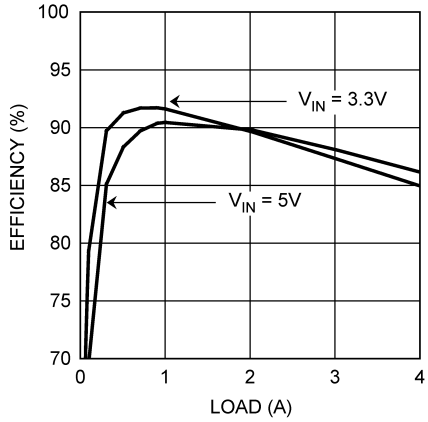
V_{OUT} = 1.8 V

Figure 3. Efficiency



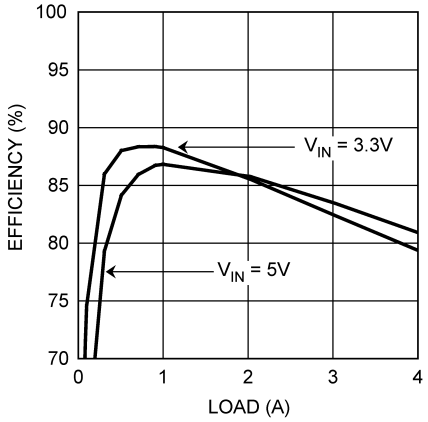
V_{OUT} = 1.5 V

Figure 4. Efficiency



V_{OUT} = 1.2 V

Figure 5. Efficiency



V_{OUT} = 0.8 V

Figure 6. Efficiency

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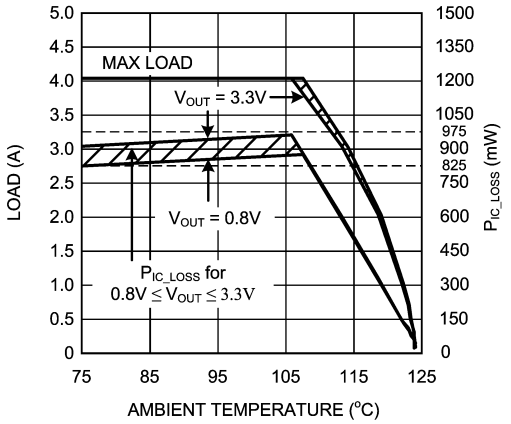
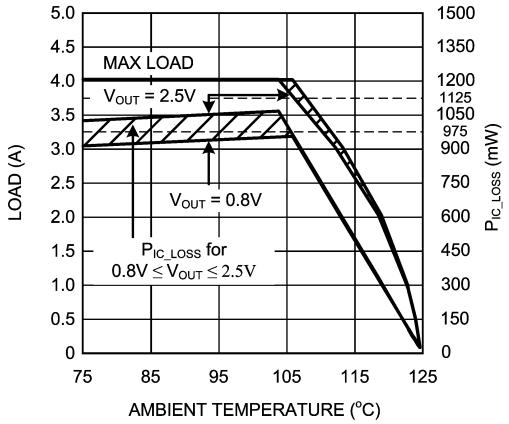
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = V_{EN} = 5 V, C_{IN} is 47-µF 10-V X5R ceramic capacitor; T_A = 25°C for efficiency curves and waveforms.



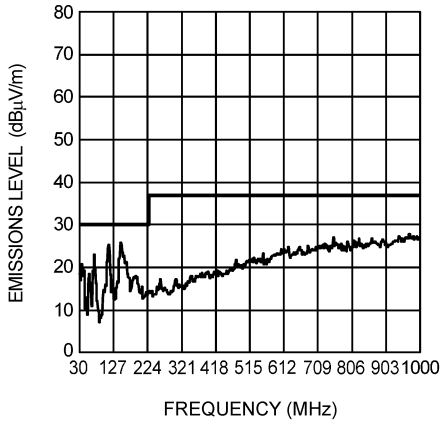
V_{IN} = 5 V, $R_{\theta JA}$ = 20°C/W

Figure 7. Current Derating



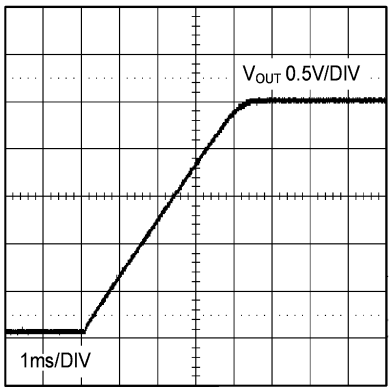
V_{IN} = 3.3 V, $R_{\theta JA}$ = 20°C/W

Figure 8. Current Derating



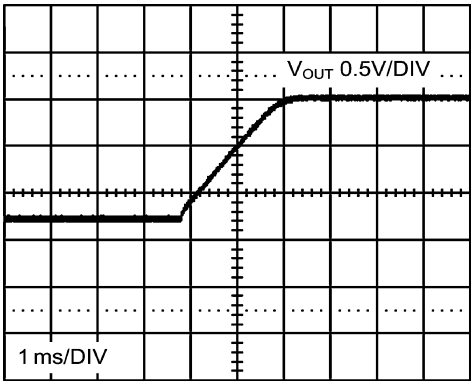
V_{IN} = 5 V, V_{OUT} = 2.5 V, I_{OUT} = 4 A Evaluation Board

Figure 9. Radiated Emissions (EN 55022, Class B)



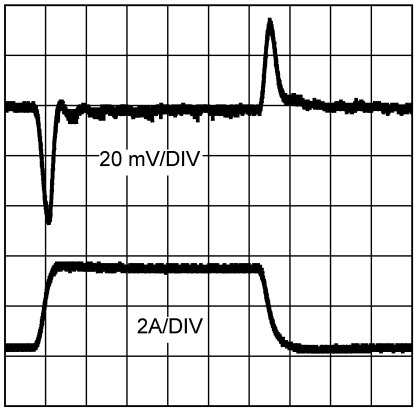
V_{OUT} = 2.5 V, I_{OUT} = 0 A

Figure 10. Start-Up



V_{OUT} = 2.5 V, I_{OUT} = 0 A

Figure 11. Prebiased Start-Up



50 µs/DIV

V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{OUT} = 0.4-A to 3.6-A to 0.4-A step
20 mV/DIV, 20-MHz Bandwidth Limited
Refer to Table 5 for BOM, includes optional components

Figure 12. Load Transient Response

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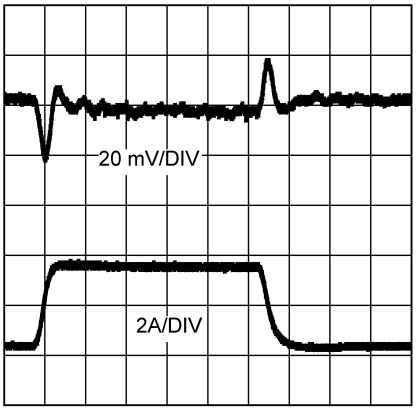
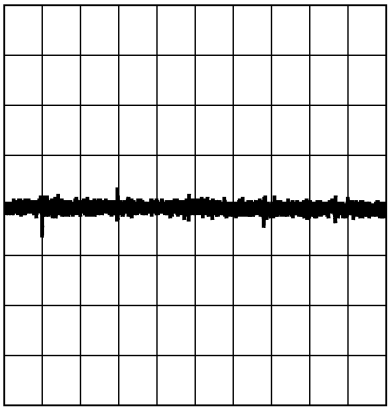
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = V_{EN} = 5 V, C_{IN} is 47-µF 10-V X5R ceramic capacitor; T_A = 25°C for efficiency curves and waveforms.



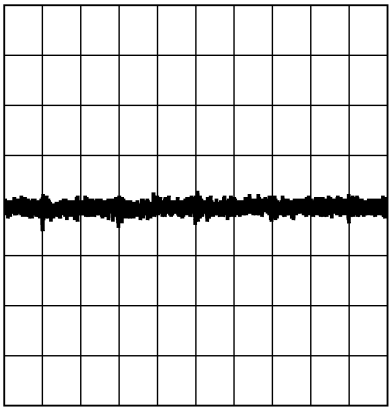
50 µs/DIV
V_{IN} = 5.0 V, V_{OUT} = 2.5 V, I_{OUT} = 0.4-A to 3.6-A to 0.4-A step
20 mV/DIV, 20-MHz Bandwidth Limited
Refer to Table 5 for BOM, includes optional components

Figure 13. Load Transient Response



500 ns/DIV
V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{OUT} = 4 A, 20 mV/DIV
Refer to Table 5 for BOM

Figure 14. Output Voltage Ripple



500 ns/DIV
V_{IN} = 5.0 V, V_{OUT} = 2.5 V, I_{OUT} = 4 A,
20 mV/DIV, Refer to Table 5 for BOM

Figure 15. Output Voltage Ripple

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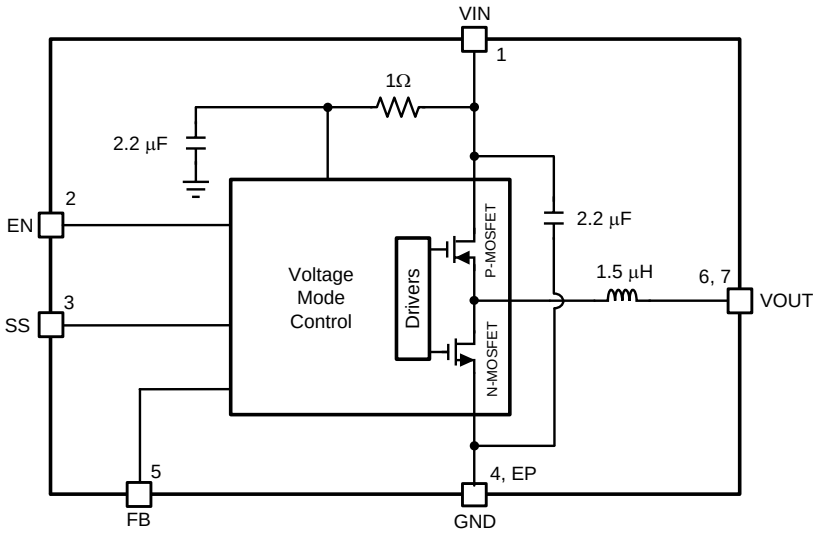
7 Detailed Description

7.1 Overview

The LMZ10504 power module is a complete, easy-to-use DC-DC solution capable of driving up to a 4-A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. The LMZ10504 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering. The LMZ10504 is a reliable and robust solution with the following features: lossless cycle-by-cycle peak current limit to protect for overcurrent or short-circuit fault, thermal shutdown, input undervoltage lockout, and prebiased start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

The LMZ10504 features an enable (EN) pin and associated comparator to allow the user to easily sequence the LMZ10504 from an external voltage rail, or to manually set the input UVLO threshold. The turnon or rising threshold and hysteresis for this comparator are typically 1.23 V and 0.15 V, respectively. The precise reference for the enable comparator allows the user to ensure that the LMZ10504 will be disabled when the system demands it to be.

The EN pin should not be left floating. For always-on operation, connect EN to VIN.

7.3.2 Enable and UVLO

Using a resistor divider from VIN to EN as shown in the schematic diagram below, the input voltage at which the part begins switching can be increased above the normal input UVLO level according to:

$$V_{IN(UVLO)} = 1.23\,V \times \frac{R_{ent} + R_{enb}}{R_{enb}} \quad (1)$$

For example, suppose that the required input UVLO level is 3.69 V. Choosing R_{enb} = 10 kΩ, then we calculate R_{ent} = 20 kΩ.

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Feature Description (continued)

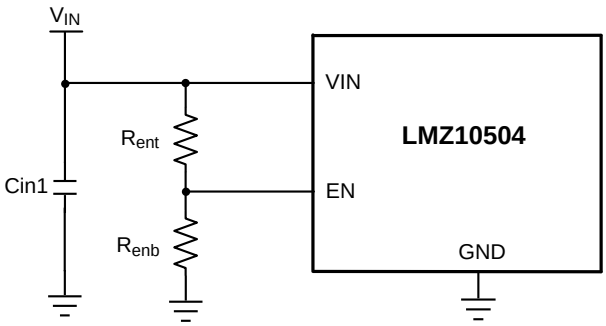

Figure 16. Setting Enable and UVLO

Alternatively, the EN pin can be driven from another voltage source to cater to system sequencing requirements commonly found in FPGA and other multi-rail applications. Figure 17 shows an LMZ10504 that is sequenced to start based on the voltage level of a master system rail (V_{OUT1}).

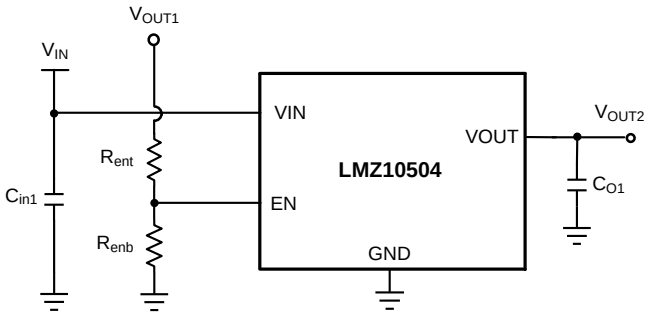

Figure 17. Setting Enable and UVLO Using External Power Supply

7.3.3 Soft-Start

The LMZ10504 begins to operate when both the VIN and EN, voltages exceed the rising UVLO and enable thresholds, respectively. A controlled soft-start eliminates inrush currents during start-up and allows the user more control and flexibility when sequencing the LMZ10504 with other power supplies.

In the event of either VIN or EN decreasing below the falling UVLO or enable threshold respectively, the voltage on the soft-start pin is collapsed by discharging the soft-start capacitor by a 14-µA (typical) current sink to ground.

7.3.4 Soft-Start Capacitor

Determine the soft-start capacitance with the following relationship:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{FB}} \quad (2)$$

where

- V_{FB} is the internal reference voltage (nominally 0.8 V),
- I_{SS} is the soft-start charging current (nominally 2 µA)
- and C_{SS} is the external soft-start capacitance.

Thus, the required soft-start capacitor per unit output voltage start-up time is given by:

$$C_{SS} = 2.5\,nF / ms \quad (3)$$

For example, a 4-ms soft-start time will yield a 10-nF capacitance. The minimum soft-start capacitance is 680 pF.

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Feature Description (continued)

7.3.5 Tracking

The LMZ10504 can track the output of a master power supply during soft-start by connecting a resistor divider to the SS pin. In this way, the output voltage slew rate of the LMZ10504 will be controlled by a master supply for loads that require precise sequencing. When the tracking function is used, a small value soft-start capacitor should be connected to the SS pin to alleviate output voltage overshoot when recovering from a current limit fault.

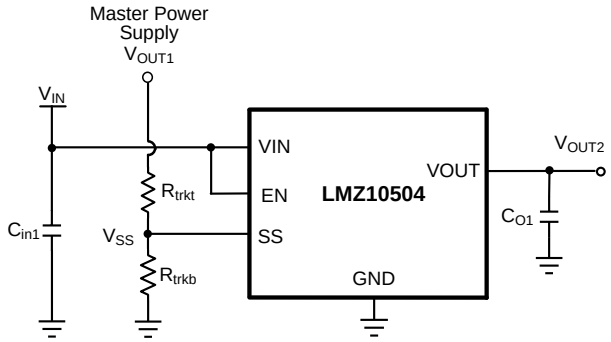

Figure 18. Tracking Using External Power Supply

7.3.6 Tracking - Equal Soft-Start Time

One way to use the tracking feature is to design the tracking resistor divider so that the master supply output voltage, V_{OUT1}, and the LMZ10504 output voltage, V_{OUT2}, both rise together and reach their target values at the same time. This is termed ratiometric start-up. For this case, the equation governing the values of tracking divider resistors R_{trkb} and R_{trkt} is given by:

$$R_{trkb} = \frac{R_{trkt}}{V_{OUT1} - 1.0\,V} \tag{4}$$

The above equation includes an offset voltage, of 200 mV, to ensure that the final value of the SS pin voltage exceeds the reference voltage of the LMZ10504. This offset will cause the LMZ10504 output voltage to reach regulation slightly before the master supply. For a value of 33 kΩ, 1% is recommended for R_{trkt} as a compromise between high-precision and low-quiescent current through the divider while minimizing the effect of the 2-µA soft-start current source.

For example, if the master supply voltage V_{OUT1} is 3.3 V and the LMZ10504 output voltage was 1.8 V, then the value of R_{trkb} needed to give the two supplies identical soft-start times would be 14.3 kΩ. Figure 19 shows an example of tracking using the equal soft-start time.

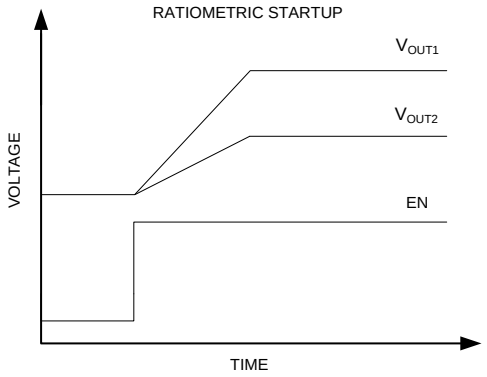

Figure 19. Timing Diagram for Tracking Using Equal Soft-Start Time

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Feature Description (continued)

7.3.7 Tracking - Equal Slew Rates

Alternatively, the tracking feature can be used to have similar output voltage ramp rates. This is referred to as simultaneous start-up. In this case, the tracking resistors can be determined based on Equation 5:

$$R_{trkb} = \frac{0.8\,V}{V_{OUT\,2} - 0.8\,V} \times R_{trkt} \tag{5}$$

and to ensure proper overdrive of the SS pin

$$V_{OUT\,2} < 0.8 \times V_{OUT1} \tag{6}$$

For the example case of V_{OUT1} = 5 V and V_{OUT2} = 2.5 V, with R_{trkt} set to 33 kΩ as before, R_{trkb} is calculated from the above equation to be 15.5 kΩ. Figure 20 shows an example of tracking using the equal slew rates.

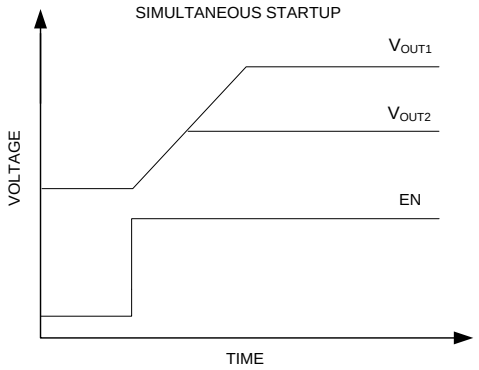

Figure 20. Timing Diagram for Tracking Using Equal Slew Rates

7.3.8 Current Limit

When a current greater than the output current limit (I_{OCL}) is sensed, the ON-time is immediately terminated and the low-side MOSFET is activated. The low-side MOSFET stays on for the entire next four switching cycles. During these skipped pulses, the voltage on the soft-start pin is reduced by discharging the soft-start capacitor by a current sink on the soft-start pin of nominally 14 µA. Subsequent overcurrent events will drain more and more charge from the soft-start capacitor, effectively decreasing the reference voltage as the output droops due to the pulse skipping. Reactivation of the soft-start circuitry ensures that when the overcurrent situation is removed, the part will resume normal operation smoothly.

7.3.9 Overtemperature Protection

When the LMZ10504 senses a junction temperature greater than 145°C (typical), both switching MOSFETs are turned off and the part enters a standby state. Upon sensing a junction temperature below 135°C (typical), the part will re-initiate the soft-start sequence and begin switching once again.

7.4 Device Functional Modes

7.4.1 Prebias Start-Up Capability

At start-up, the LMZ10504 is in a prebiased state when the output voltage is greater than zero. This often occurs in many multi-rail applications such as when powering an ASIC, FPGA, or DSP. The output can be prebiased in these applications through parasitic conduction paths from one supply rail to another. Even though the LMZ10504 is a synchronous converter, it will not pull the output low when a prebias condition exists. The LMZ10504 will not sink current during start-up until the soft-start voltage exceeds the voltage on the FB pin. Because the device does not sink current it protects the load from damage that might otherwise occur if current is conducted through the parasitic paths of the load.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ10504 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 4 A. The following design procedure can be used to select components for the LMZ10504. Alternately, the WEBENCH software may be used to generate complete designs. When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application

This section provides several application solutions with an associated bill of materials. The compensation for each solution was optimized to work over the full input range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point.

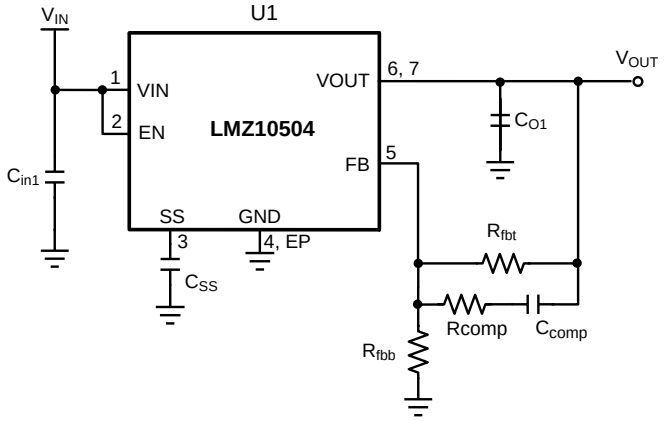

Figure 21. Typical Applications Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} = 5 V
- V_{OUT} = 2.5 V
- I_{OUT} = 4 A
- ΔV_{OUT} = 20 mV_{pk-pk}
- ΔV_{o_tran} = ±20 mV_{pk-pk}

Table 1. Bill of Materials, V_{IN} = 3.3 V to 5 V, V_{OUT} = 2.5 V, $I_{OUT\ (MAX)}$ = 4 A, Optimized for Electrolytic Input and Output Capacitance

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
U1	Power Module	PFM-7	Texas Instruments	LMZ10504TZ-ADJ	1
C_{in1}	150 µF, 6.3 V, 18 mΩ	C2, 6.0 x 3.2 x 1.8 mm	Sanyo	6TPE150MIC2	1
C_{O1}	330 µF, 6.3 V, 18 mΩ	D3L, 7.3 x 4.3 x 2.8 mm	Sanyo	6TPE330MIL	1
R_{fbt}	100 kΩ	0603	Vishay Dale	CRCW0603100KFKEA	1

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Typical Application (continued)

Table 1. Bill of Materials, V_{IN} = 3.3 V to 5 V, V_{OUT} = 2.5 V, $I_{OUT\ (MAX)}$ = 4 A, Optimized for Electrolytic Input and Output Capacitance (continued)

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
R_{fbb}	47.5 kΩ	0603	Vishay Dale	CRCW060347K5FKEA	1
R_{comp}	15 kΩ	0603	Vishay Dale	CRCW060315K0FKEA	1
C_{comp}	330 pF, ±5%, C0G, 50 V	0603	TDK	C1608C0G1H331J	1
C_{SS}	10 nF, ±10%, X7R, 16 V	0603	Murata	GRM188R71C103KA01	1

Table 2. Bill of Materials, V_{IN} = 3.3 V, V_{OUT} = 0.8 V, $I_{OUT\ (MAX)}$ = 4 A, Optimized for Solution Size and Transient Response(1)

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
U1	Power Module	PFM-7	Texas Instruments	LMZ10504TZ-ADJ	1
C_{in1}, C_{O1}	47 µF, X5R, 6.3 V	1206	TDK	C3216X5R0J476M	2
R_{fbt}	110 kΩ	0402	Vishay Dale	CRCW0402100KFKED	1
R_{comp}	1.0 kΩ	0402	Vishay Dale	CRCW04021K00FKED	1
C_{comp}	27 pF, ±5%, C0G, 50 V	0402	Murata	GRM1555C1H270JZ01	1
C_{SS}	10 nF, ±10%, X7R, 16 V	0402	Murata	GRM155R71C103KA01	1

(1) In the case where the output voltage is 0.8 V, TI recommends removing R_{fbb} and keep R_{fbt}, R_{comp}, and C_{comp} for a type III compensation.

8.2.2 Detailed Design Procedure

LMZ10504 is fully supported by WEBENCH and offers the following: component selection, performance, electrical, and thermal simulations as well as the Build-It board, for a reduced design time. On the other hand, all external components can be calculated by following the design procedure below.

1. Determine the input voltage and output voltage. Also, make note of the ripple voltage and voltage transient requirements.
2. Determine the necessary input and output capacitance.
3. Calculate the feedback resistor divider.
4. Select the optimized compensation component values.
5. Estimate the power dissipation and board thermal requirements.
6. Follow the PCB design guideline.
7. Learn about the LMZ10504 features such as enable, input UVLO, soft start, tracking, prebiased start-up, current limit, and thermal shutdown.

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ10504 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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8.2.2.2 Input Capacitor Selection

A 22-µF or 47-µF high-quality dielectric (X5R, X7R) ceramic capacitor rated at twice the maximum input voltage is typically sufficient. The input capacitor must be placed as close as possible to the VIN pin and GND exposed pad to substantially eliminate the parasitic effects of any stray inductance or resistance on the PCB and supply lines.

Neglecting capacitor equivalent series resistance (ESR), the resultant input capacitor AC ripple voltage is a triangular waveform. The minimum input capacitance for a given peak-to-peak value (ΔV_{IN}) of V_{IN} is specified as follows:

$$C_{in} \geq \frac{I_{OUT} \times D \times (1-D)}{f_{sw} \times \Delta V_{IN}}$$

where

- the PWM duty cycle, D, is given by Equation 8 (7)

$$D = \frac{V_{OUT}}{V_{IN}} \quad (8)$$

If ΔV_{IN} is 1% of V_{IN}, this equals to 50 mV and f_{SW} = 1 MHz.

$$C_{in} \geq \frac{4\,A \times \left(\frac{2.5\,V}{5\,V}\right) \times \left(1-\frac{2.5\,V}{5\,V}\right)}{1\ MHz\ \times\ 50\,mV} \geq 20\,\mu F \quad (9)$$

A second criteria before finalizing the C_{in} bypass capacitor is the RMS current capability. The necessary RMS current rating of the input capacitor to a buck regulator can be estimated by:

$$I_{Cin(RMS)} = I_{OUT} \times \sqrt{D(1-D)} \quad (10)$$

$$I_{Cin(RMS)} = 4\,A \times \sqrt{\frac{2.5\,V}{5\,V}\left(1-\frac{2.5\,V}{5\,V}\right)} = 2\,A \quad (11)$$

With this high AC current present in the input capacitor, the RMS current rating becomes an important parameter. The maximum input capacitor ripple voltage and RMS current occur at 50% duty cycle. Select an input capacitor rated for at least the maximum calculated $I_{Cin(RMS)}$.

Additional bulk capacitance with higher ESR may be required to damp any resonance effects of the input capacitance and parasitic inductance.

8.2.2.3 Output Capacitor Selection

In general, 22-µF to 100-µF, high-quality dielectric (X5R, X7R) ceramic capacitor rated at twice the maximum output voltage is sufficient given the optimal high-frequency characteristics and low ESR of ceramic dielectrics. Although, the output capacitor can also be of electrolytic chemistry for increased capacitance density.

Two output capacitance equations are required to determine the minimum output capacitance. One equation determines the output capacitance (C_O) based on PWM ripple voltage. The second equation determines C_O based on the load transient characteristics. Select the largest capacitance value of the two.

The minimum capacitance, given the maximum output voltage ripple (ΔV_{OUT}) requirement, is determined by the following equation:

$$C_O \geq \frac{\Delta i_L}{8 \times f_{sw} \times \left[\Delta V_{OUT} - (\Delta i_L \times R_{ESR})\right]}$$

where

- the peak to peak inductor current ripple (Δi_L) is equal to Equation 13: (12)

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{sw}} \quad (13)$$

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R_{ESR} is the total output capacitor ESR, L is the inductance value of the internal power inductor, where L = 1.5 µH, and f_{SW} = 1 MHz. Therefore, per the design example:

$$\Delta i_L = \frac{(5\,V - 2.5\,V) \times \frac{2.5\,V}{5\,V}}{1.5\ \mu H\ \times\ 1\ MHz} = 833\ mA \tag{14}$$

The minimum output capacitance requirement due to the PWM ripple voltage is:

$$C_O \geq \frac{833\,mA}{8 \times 1\ MHz \times \left[20\,mV - (833\,mA \times 3\,m\Omega)\right]} \tag{15}$$

$$C_O \geq 6\ \mu F \tag{16}$$

Three mΩ is a typical R_{ESR} value for ceramic capacitors.

Equation 17 provides a good first pass capacitance requirement for a load transient:

$$C_O \geq \frac{I_{step} \times V_{FB} \times L \times V_{IN}}{4 \times V_{OUT} \times (V_{IN} - V_{OUT}) \times \Delta Vo\_tran} \tag{17}$$

where

- I_{step} is the peak to peak load step,
- V_{FB} = 0.8 V,
- and ΔV_{o_tran} is the maximum output voltage deviation, which is ±20 mV.

Therefore the capacitance requirement for the given design parameters is:

$$C_O \geq \frac{3.2\,A \times 0.8\,V \times 1.5\,\mu H \times 5\,V}{4 \times 2.5\,V \times (5\,V - 2.5\,V) \times 20\,mV} \tag{18}$$

$$C_O \geq 39\ \mu F \tag{19}$$

In this particular design the output capacitance is determined by the load transient requirements.

Table 3 lists some examples of commercially available capacitors that can be used with the LMZ10504.

Table 3. Recommended Output Filter Capacitors

C_O (µF)	VOLTAGE (V), R_{ESR} (mΩ)	MAKE	MANUFACTURER	PART NUMBER	CASE SIZE
22	6.3, < 5	Ceramic, X5R	TDK	C3216X5R0J226M	1206
47	6.3, < 5	Ceramic, X5R	TDK	C3216X5R0J476M	1206
47	6.3, < 5	Ceramic, X5R	TDK	C3225X5R0J476M	1210
47	10.0, < 5	Ceramic, X5R	TDK	C3225X5R1A476M	1210
100	6.3, < 5	Ceramic, X5R	TDK	C3225X5R0J107M	1210
100	6.3, 50	Tantalum	AVX	TPSD157M006#0050	D, 7.5 × 4.3 × 2.9 mm
100	6.3, 25	Organic Polymer	Sanyo	6TPE100MPB2	B2, 3.5 × 2.8 × 1.9 mm
150	6.3, 18	Organic Polymer	Sanyo	6TPE150MIC2	C2, 6.0 × 3.2 × 1.8 mm
330	6.3, 18	Organic Polymer	Sanyo	6TPE330MIL	D3L, 7.3 × 4.3 × 2.8 mm
470	6.3, 23	Niobium Oxide	AVX	NOME37M006#0023	E, 7.3 × 4.3 × 4.1 mm

8.2.2.3.1 Output Voltage Setting

A resistor divider network from V_{OUT} to the FB pin determines the desired output voltage as follows:

$$V_{OUT} = 0.8\,V \times \frac{R_{fbt} + R_{fbb}}{R_{fbb}} \tag{20}$$

R_{fbt} is defined based on the voltage loop requirements and R_{fbb} is then selected for the desired output voltage. Resistors are normally selected as 0.5% or 1% tolerance. Higher accuracy resistors such as 0.1% are also available.

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The feedback voltage (at V_{OUT} = 2.5 V) is accurate to within –2.5% / +2.5% over temperature and over line and load regulation. Additionally, the LMZ10504 contains error nulling circuitry to substantially eliminate the feedback voltage variation over temperature as well as the long-term aging effects of the internal amplifiers. In addition the zero nulling circuit dramatically reduces the 1/f noise of the bandgap amplifier and reference. The manifestation of this circuit action is that the duty cycle will have two slightly different but distinct operating points, each evident every other switching cycle.

8.2.2.4 Loop Compensation

The LMZ10504 preserves flexibility by integrating the control components around the internal error amplifier while using three small external compensation components from V_{OUT} to FB. An integrated type II (two pole, one zero) voltage-mode compensation network is featured. To ensure stability, an external resistor and small value capacitor can be added across the upper feedback resistor as a pole-zero pair to complete a type III (three pole, two zero) compensation network. The compensation components recommended in Table 4 provide type III compensation at an optimal control loop performance. The typical phase margin is 45° with a bandwidth of 80 kHz. Calculated output capacitance values not listed in Table 4 should be verified before designing into production. The detailed application note *AN-2013 LMZ1050x/LMZ1050xEXT SIMPLE SWITCHER Power Module* (SNVA417) is available to provide verification support. . In general, calculated output capacitance values below the suggested value will have reduced phase margin and higher control loop bandwidth. Output capacitance values above the suggested values will experience a lower bandwidth and increased phase margin. Higher bandwidth is associated with faster system response to sudden changes such as load transients. Phase margin changes the characteristics of the response. Lower phase margin is associated with underdamped ringing and higher phase margin is associated with overdamped response. Losing all phase margin will cause the system to be unstable; an optimized area of operation is 30° to 60° of phase margin, with a bandwidth of 100 kHz ±20 kHz.

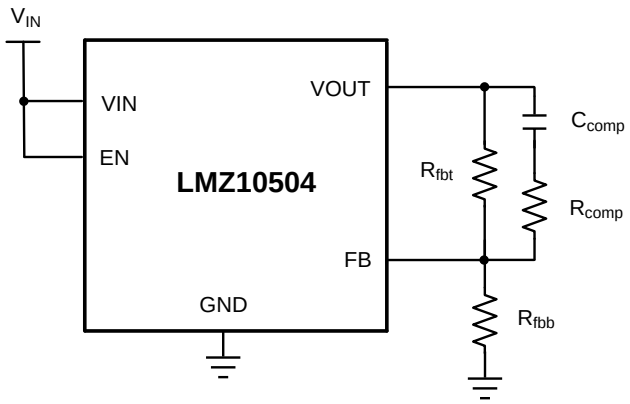

Figure 22. Loop Compensation Control Components

Table 4. LMZ10504 Compensation Component Values

V_{IN} (V)	C_O (µF)	ESR (mΩ)		R_{fbt} (kΩ)(1)	C_{comp} (pF)(1)	R_{comp} (kΩ)(1)
		MIN	MAX			
5	22	2	20	200	27	1.5
	47	2	20	124	68	1.4
	100	1	10	82.5	150	0.681
	150	1	5	63.4	220	1
	150	10	25	63.4	220	3.48
	150	26	50	226	62	12.1
	220	15	30	150	100	6.98
	220	31	60	316	560	14

(1) In the special case where the output voltage is 0.8 V, TI recommends to remove R_{fbb} and keep R_{fbt}, R_{comp}, and C_{comp} for a type III compensation.

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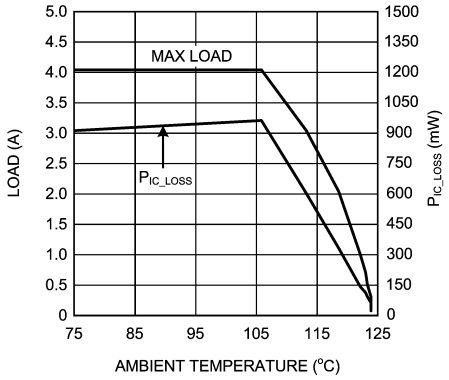
Table 4. LMZ10504 Compensation Component Values (continued)

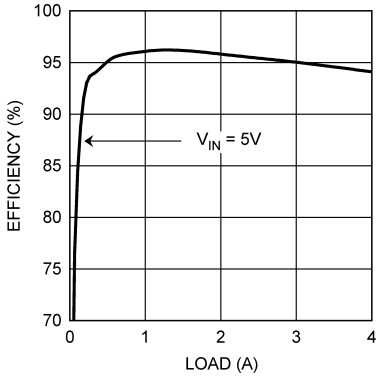
V_{IN} (V)	C_O (µF)	ESR (mΩ)		R_{fbt} (kΩ)(1)	C_{comp} (pF)(1)	R_{comp} (kΩ)(1)
		MIN	MAX			
3.3	22	2	20	118	43	9.09
	47	2	20	76.8	100	3.32
	100	1	10	49.9	180	2.49
	150	1	5	40.2	330	1
	150	10	25	43.2	330	4.99
	150	26	50	143	100	7.5
	220	15	30	100	180	4.99
	220	31	60	200	100	8.06

8.2.3 Application Curves



V_{OUT} = 3.3 V

Figure 23. Current Derating



V_{OUT} = 3.3 V

Figure 24. Efficiency

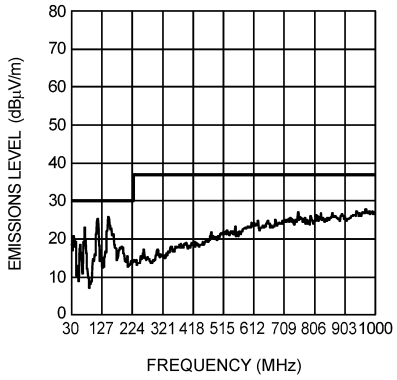


Figure 25. Radiated Emissions (EN 55022, Class B)

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8.3 System Examples

8.3.1 Application Schematic for 3.3-V to 5-V Input and 2.5-V Output With Optimized Ripple and Transient Response

The compensation for each solution was optimized to work over the stated input range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point. This schematic is intended to serve as a helpful starting point towards an optimized design.

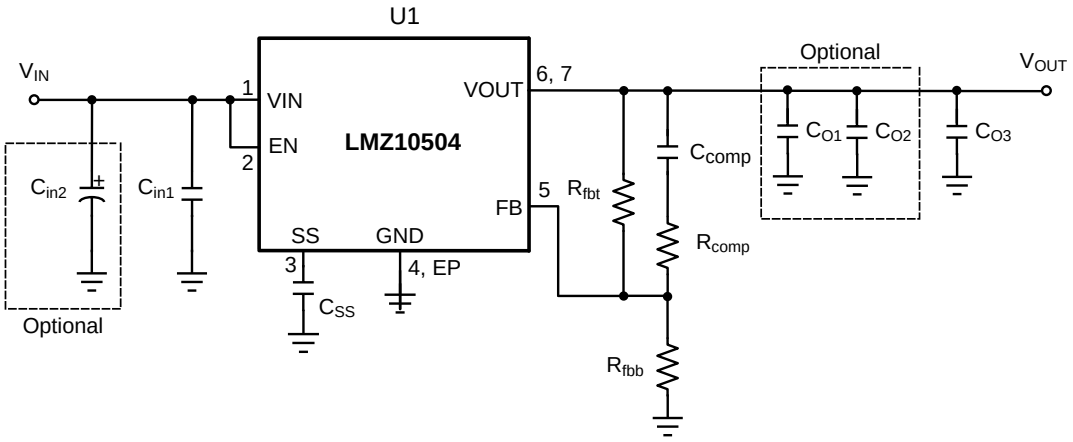

Figure 26. Schematic for 2.5-V Output Based on 3.3-V to 5-V Input

Table 5. Bill of Materials, V_{IN} = 3.3 V to 5 V, V_{OUT} = 2.5 V, $I_{OUT\ (MAX)}$ = 4 A, Optimized for Low Input and Output Ripple Voltage and Fast Transient Response(1)

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
U1	Power Module	PFM-7	Texas Instruments	LMZ10504TZ-ADJ	1
C_{in1}	22 µF, X5R, 10 V	1210	AVX	1210ZD226MAT	2
C_{in2}	220 µF, 10 V, AL-Elec	E	Panasonic	EEE1AA221AP	1*
C_{O1}	4.7 µF, X5R, 10 V	0805	AVX	0805ZD475MAT	1*
C_{O2}	22 µF, X5R, 6.3 V	1206	AVX	12066D226MAT	1*
C_{O3}	100 µF, X5R, 6.3 V	1812	AVX	18126D107MAT	1
R_{fbt}	75 kΩ	0402	Vishay Dale	CRCW040275K0FKED	1
R_{fbb}	34.8 kΩ	0402	Vishay Dale	CRCW040234K8FKED	1
R_{comp}	1.0 kΩ	0402	Vishay Dale	CRCW04021K00FKED	1
C_{comp}	100 pF, ±5%, C0G, 50 V	0402	Murata	GRM1555C1H101JZ01	1
C_{SS}	10 nF, ±10%, X7R, 16 V	0402	Murata	GRM155R71C103KA01	1

(1) * Optional components, include for low input and output voltage ripple.

Table 6. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

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8.3.2 Application Schematic for 3.3-V to 5-V Input and 2.5-V Output

The compensation for each solution was optimized to work over the stated input range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point. This schematic is intended to serve as a helpful starting point towards an optimized design.

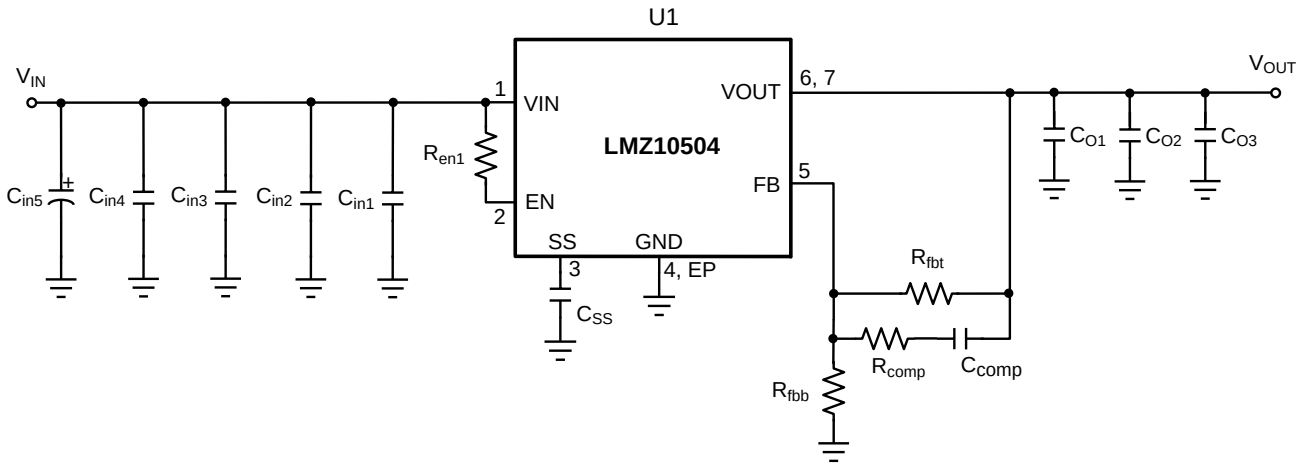

Figure 27. Schematic for 2.5-V Output Based on 3.3-V to 5-V Input

Table 7. Bill of Materials, V_{IN} = 3.3 V to 5 V, V_{OUT} = 2.5 V, $I_{OUT\ (MAX)}$ = 4 A

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
U1	Power Module	PFM-7	Texas Instruments	LMZ10504TZ-ADJ	1
C_{in1}	1 µF, X7R, 16 V	0805	TDK	C2012X7R1C105K	1
C_{in2}, C_{O1}	4.7 µF, X5R, 6.3 V	0805	TDK	C2012X5R0J475K	2
C_{in3}, C_{O2}	22 µF, X5R, 16 V	1210	TDK	C3225X5R1C226M	2
C_{in4}	47 µF, X5R, 6.3 V	1210	TDK	C3225X5R0J476M	1
C_{in5}	220 µF, 10 V, AL-Elec	E	Panasonic	EEE1AA221AP	1
C_{O3}	100 µF, X5R, 6.3 V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50 V	0603	TDK	C1608C0G1H181J	1
R_{en1}	100 kΩ	0805	Vishay Dale	CRCW0805100KFKEA	1
C_{SS}	10 nF, ±5%, C0G, 50 V	0805	TDK	C2012C0G1H103J	1

Table 8. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
3.3 V	23.7 kΩ
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

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8.3.3 EMI Tested Schematic for 2.5-V Output Based on 3.3-V to 5-V Input

The compensation for each solution was optimized to work over the stated input range. Many applications have a fixed input voltage rail. It is possible to modify the compensation to obtain a faster transient response for a given input voltage operating point. This schematic is intended to serve as a helpful starting point towards an optimized design.

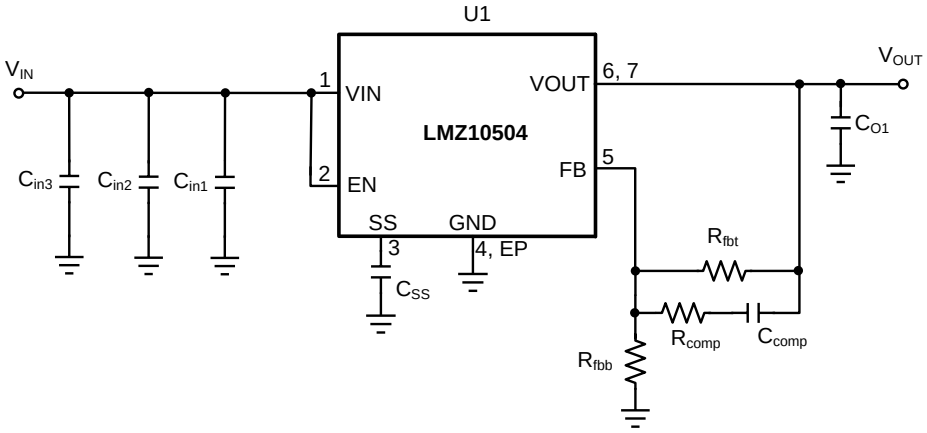

Figure 28. EMI Tested Schematic for 2.5-V Output Based on 3.3-V to 5-V Input

Table 9. Bill of Materials, V_{IN} = 5 V, V_{OUT} = 2.5 V, $I_{OUT\ (MAX)}$ = 4 A, Tested With EN55022 Class B Radiated Emissions

DESIGNATOR	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N	QUANTITY
U1	Power Module	PFM-7	Texas Instruments	LMZ10504TZ-ADJ	1
C_{in1}	1 µF, X7R, 16 V	0805	TDK	C2012X7R1C105K	1
C_{in2}	4.7 µF, X5R, 6.3 V	0805	TDK	C2012X5R0J475K	1
C_{in3}	47 µF, X5R, 6.3 V	1210	TDK	C3225X5R0J476M	1
C_{O1}	100 µF, X5R, 6.3 V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50 V	0603	TDK	C1608C0G1H181J	1
C_{SS}	10 nF, ±5%, C0G, 50 V	0805	TDK	C2012C0G1H103J	1

Table 10. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
3.3 V	23.7 kΩ
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

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9 Power Supply Recommendations

The LMZ10504 device is designed to operate from an input voltage supply range between 2.95 V and 5.5 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ10504 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ10504, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt current paths. The high current that does not overlap contains high di/dt, see Figure 29. Therefore physically place input capacitor (C_{in1}) as close as possible to the LMZ10504 VIN pin and GND exposed pad to avoid observable high-frequency noise on the output pin. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed only to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly placed, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{fbt} and R_{fbb}, and the compensation components, R_{comp} and C_{comp}, should be located close to the FB pin. Since the FB node is high impedance, keep the copper area as small as possible. This is most important as relatively high-value resistors are used to set the output voltage.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made at the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

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10.2 Layout Examples

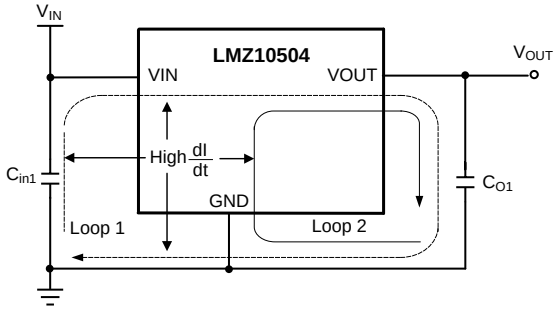

Figure 29. Critical Current Loops to Minimize

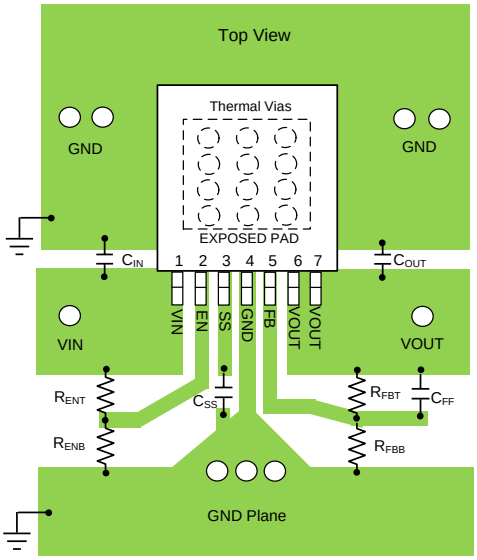

Figure 30. PCB Layout Guide

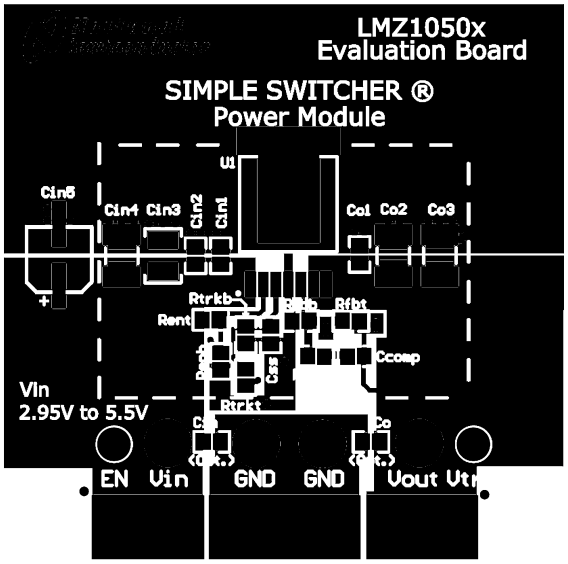

Figure 31. Top Copper

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Layout Examples (continued)

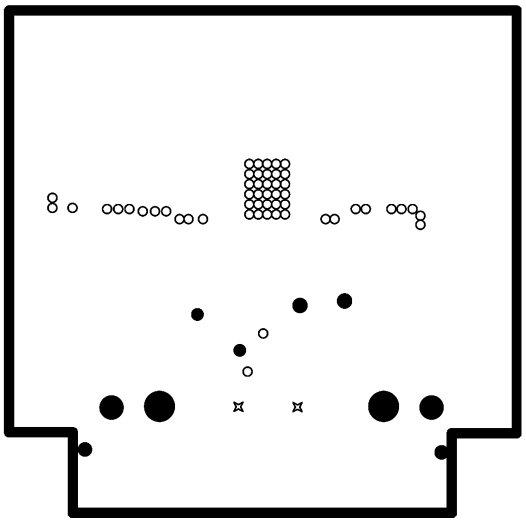

Figure 32. Internal Layer 1 (Ground)

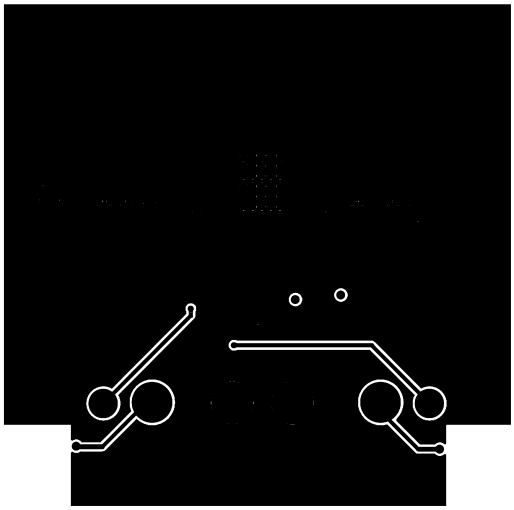

Figure 33. Internal Layer 2 (Ground and Signal Traces)

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Layout Examples (continued)

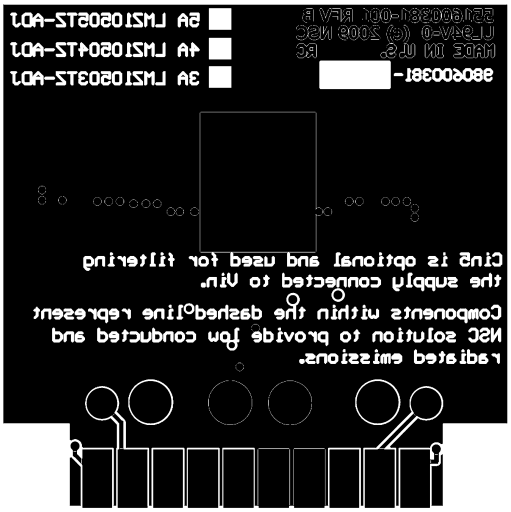

Figure 34. Bottom Copper

10.3 Estimate Power Dissipation and Thermal Considerations

Use the current derating curves in the *Typical Characteristics* section to obtain an estimate of power loss (P_{IC_LOSS}). For the design case of V_{IN} = 5 V, V_{OUT} = 2.5 V, I_{OUT} = 4 A, $T_{A(MAX)}$ = 85°C , and $T_{J(MAX)}$ = 125°C, the device must see a thermal resistance from case-to-ambient (θ_{CA}) of less than:

$$\theta_{CA} \geq \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{IC\_LOSS}} - \theta_{JC} \tag{21}$$

$$\text{Board Area\_cm}^2 \geq \frac{500}{41^\circ\text{C}} \times \frac{^\circ\text{C} \times \text{cm}^2}{\text{W}} \tag{22}$$

Given the typical thermal resistance from junction to case (θ_{JC}) to be 1.9°C/W (typical). Continuously operating at a T_J greater than 125°C will have a shorten life span.

To reach θ_{CA} = 41°C/W, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1-oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 \geq \frac{500}{\theta_{CA}} \times \frac{^\circ\text{C} \times \text{cm}^2}{\text{W}} \tag{23}$$

$$\text{Board Area\_cm}^2 \geq \frac{500}{41^\circ\text{C}} \times \frac{^\circ\text{C} \times \text{cm}^2}{\text{W}} \tag{24}$$

As a result, approximately 12 square cm of 1-oz. copper on top and bottom layers is required for the PCB design.

The PCB copper heat sink must be connected to the exposed pad (EP). Approximately thirty six, 8 mils thermal vias spaced 59 mils (1.5 mm) apart must connect the top copper to the bottom copper. For an extended discussion and formulations of thermal rules of thumb, refer to *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419) and for an example of a high thermal performance PCB layout, refer to the evaluation board application note *AN-2022 LMZ1050x Evaluation Board* (SNVA421).

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10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly.

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Maximum number of reflows allowed is one
- Refer to *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214) for reflow information.

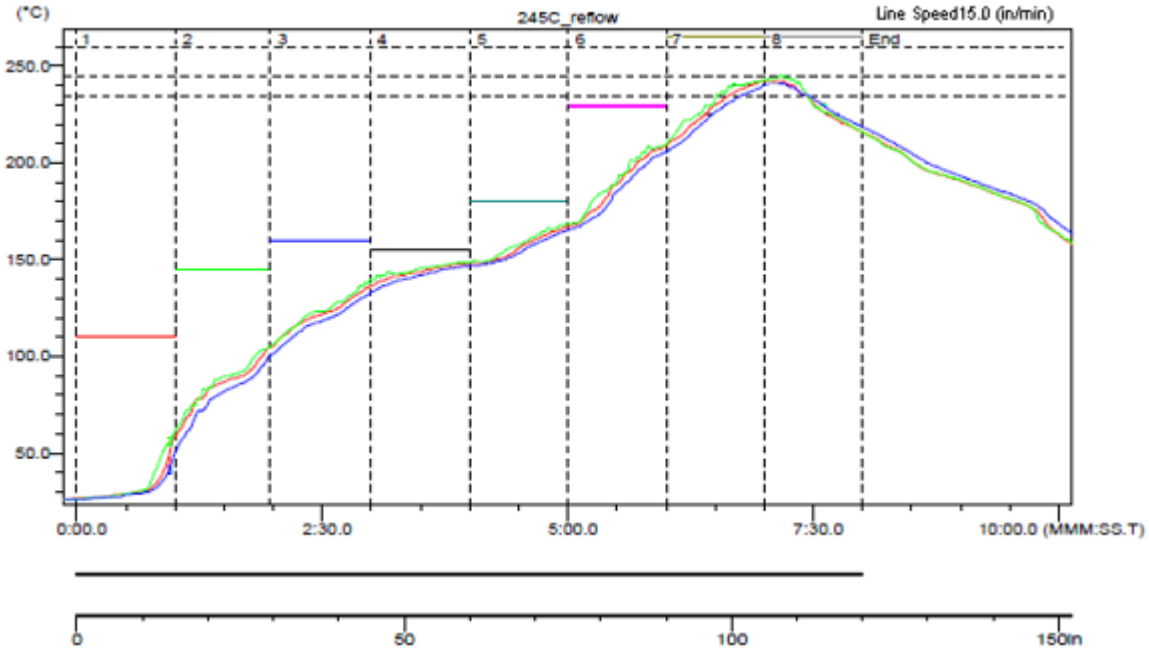

Figure 35. Sample Reflow Profile

Table 11. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

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11.1.2 開発サポート

11.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LMZ10504を使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『AN-2027 LMZ14203 SIMPLE SWITCHER電源モジュール用の反転アプリケーション』*(SNVA425)
- *『ハンダ付けの絶対最大定格』*(SNOA549)
- *『AN-2013 LMZ1050x/LMZ1050xEXT SIMPLE SWITCHER電源モジュール』*(SNVA417)
- *『AN-2022 LMZ1050x評価ボード』*(SNVA421)
- *『AN-2024 LMZ1420x/LMZ1200x評価ボード』*(SNVA422)
- *『AN-2020 システムの基本設計に応じた熱設計』*(SNVA419)
- *『AN-2026 SIMPLE SWITCHER電源モジュールの熱特性に対するPCB設計の影響』*(SNVA424)
- *『LMZ1xxxおよびLMZ2xxx電源モジュール・ファミリの設計概要』*(SNAA214)

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ10504TZ-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	250	RoHS Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ10504 TZ-ADJ	Samples
LMZ10504TZE-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	45	RoHS Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ10504 TZ-ADJ	Samples
LMZ10504TZX-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	500	RoHS Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ10504 TZ-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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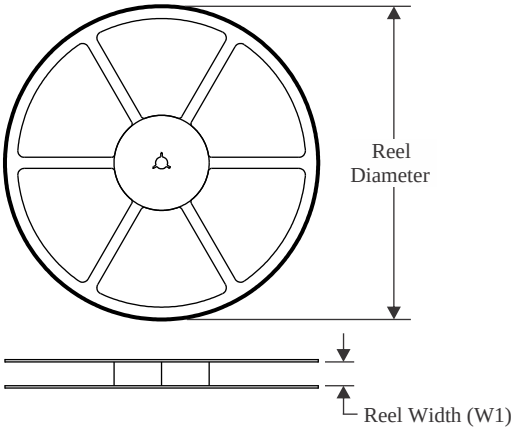
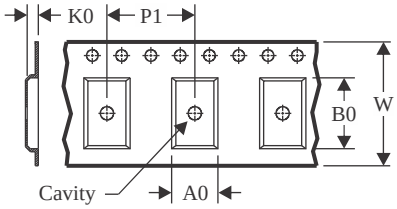
TAPE AND REEL INFORMATION

REEL DIMENSIONS

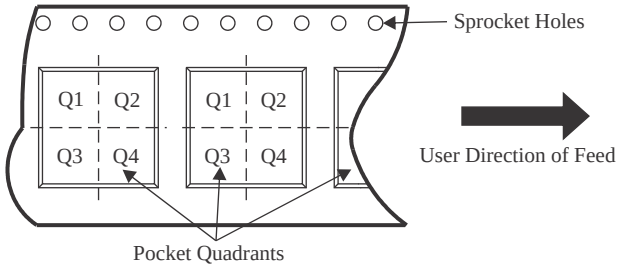


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

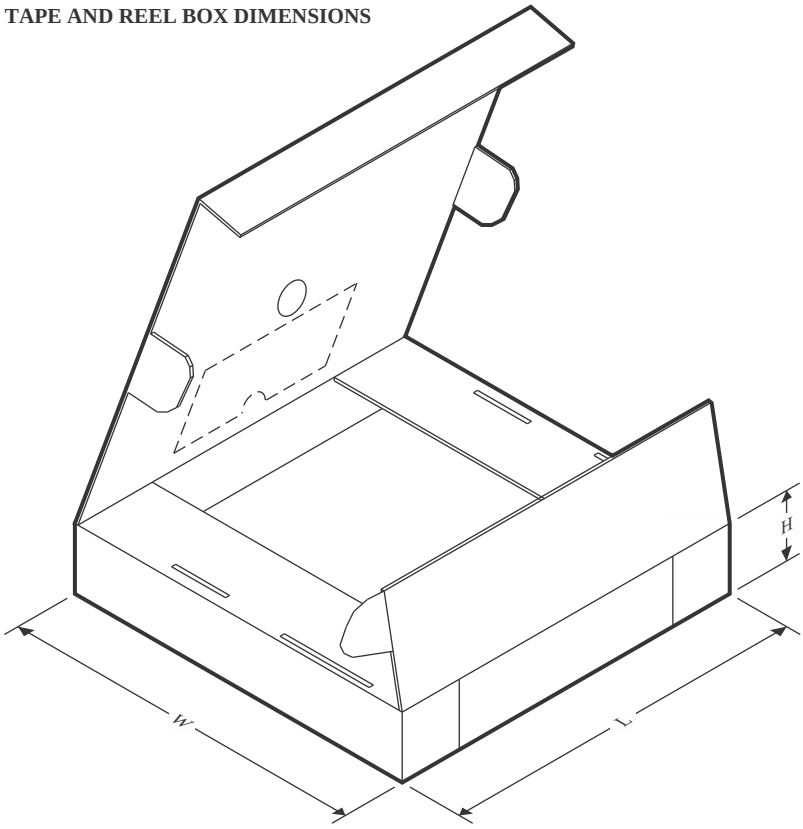
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ10504TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ10504TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

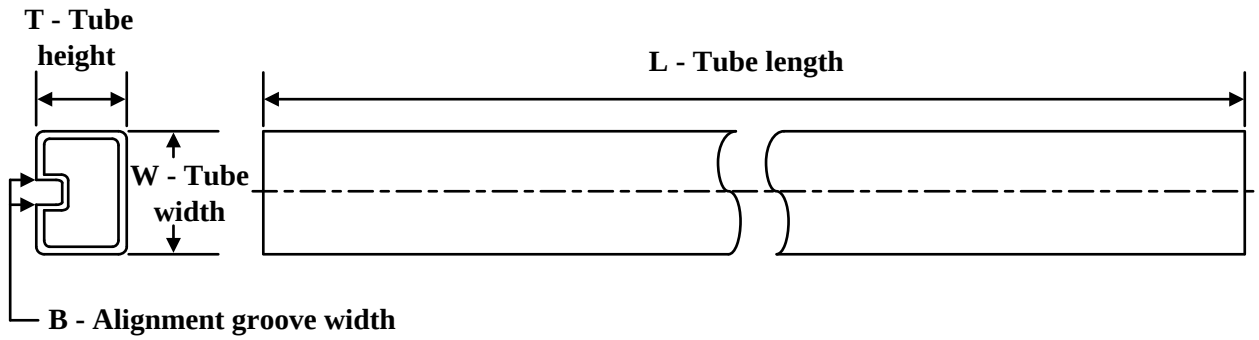
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ10504TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ10504TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

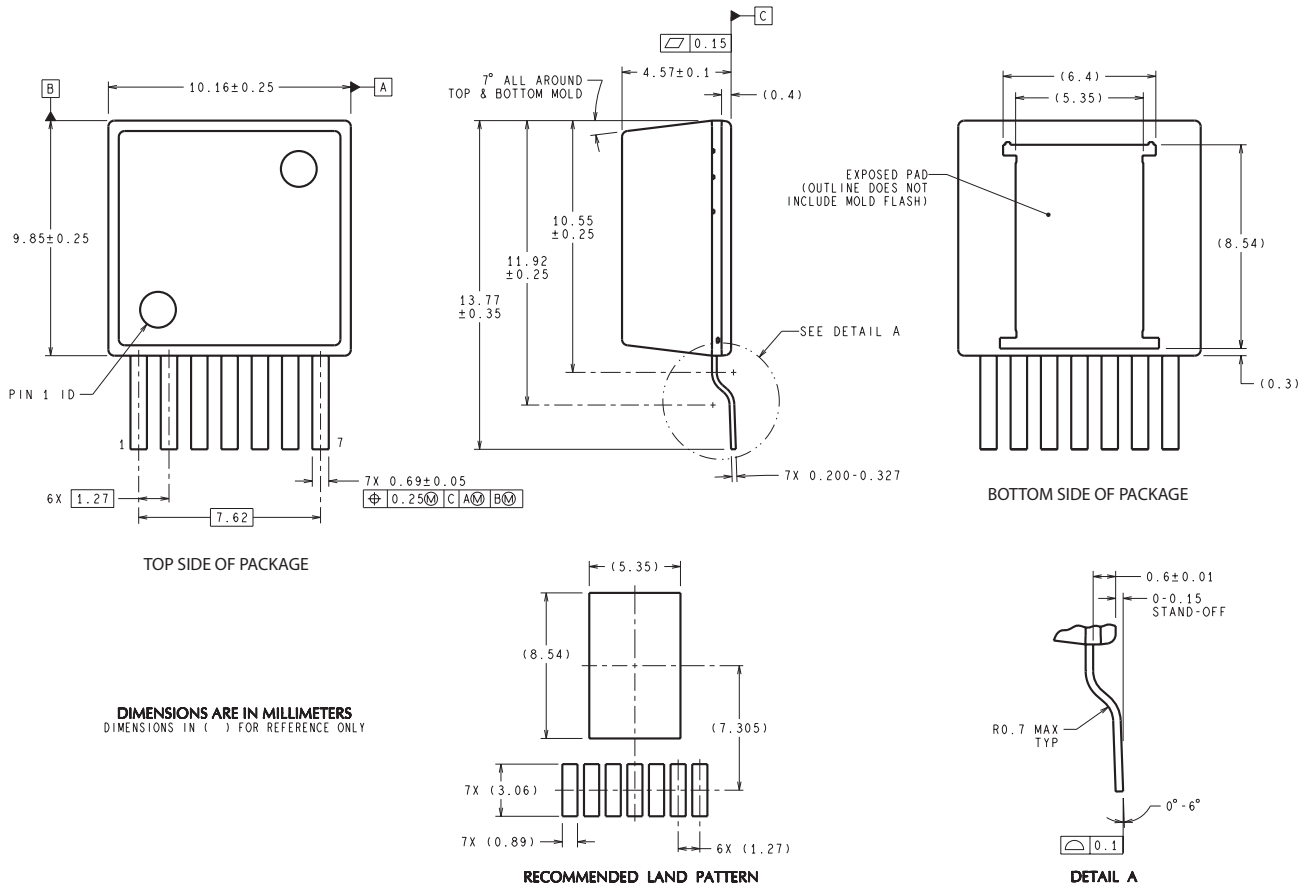
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ10504TZE-ADJ/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



TZA07A (Rev D)

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