

## LP3875-ADJ 1.5A、高速、超低ドロップアウトLDO

### 1 特長

- 入力電圧範囲: 2.5V~7V
- 非常に低いドロップアウト電圧
- 低いグラウンド・ピン電流
- 0.06%の負荷レギュレーション
- シャットダウン・モードで10nAの静止電流
- 定格出力電流1.5A DC
- 出力コンデンサの要件が最小限
- 過熱/過電流保護
- 接合部温度範囲: -40°C~+125°C
- DDPAK/TO-263およびSOT-223パッケージで供給

### 2 アプリケーション

- マイクロプロセッサの電源
- GTL、GTL+、BTL、SSTLバス・ターミネータ
- DSP用の電源
- SCSIターミネータ
- ポスト・レギュレータ
- 高効率リニア・レギュレータ
- バッテリ充電器
- その他バッテリ駆動のアプリケーション

### 3 概要

LP3875-ADJ高速、超低ドロップアウトLDOは、2.5V~7Vの入力電源電圧で動作します。この超低ドロップアウトLDOは、負荷のステップ変化に対して非常に迅速に応答するため、低電圧のマイクロプロセッサ・アプリケーションに適しています。LP3875-ADJはCMOSプロセスで開発されているため、出力負荷電流にかかわらず、低い静止電流での動作が可能です。また、このCMOSプロセスにより、LP3875-ADJは非常に低いドロップアウトの状況でも動作できます。

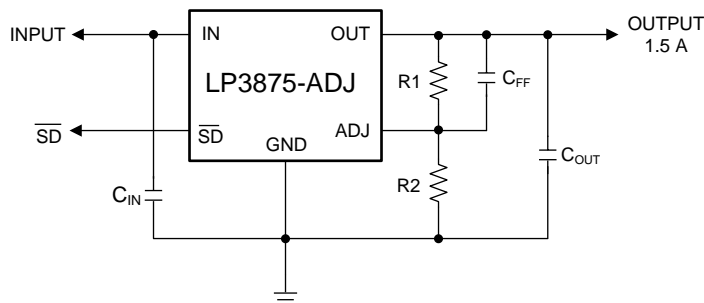
- ドロップアウト電圧: 非常に低いドロップアウト電圧、負荷電流150mAで標準値38mV、負荷電流1.5Aで380mV
- グラウンド・ピン電流: 負荷電流1.5Aで標準値6mA
- シャットダウンモード:  $\overline{SD}$ ピンがLOWのとき、静止電流の標準値10nA
- 可変出力電圧: 出力電圧は、2個の外付け抵抗を使用してプログラム可能

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LP3875-ADJ	SOT-223 (5)	6.50mm×3.56mm
	TO-263 (5)	10.16mm×8.42mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision D (April 2013) から Revision E に変更

Page

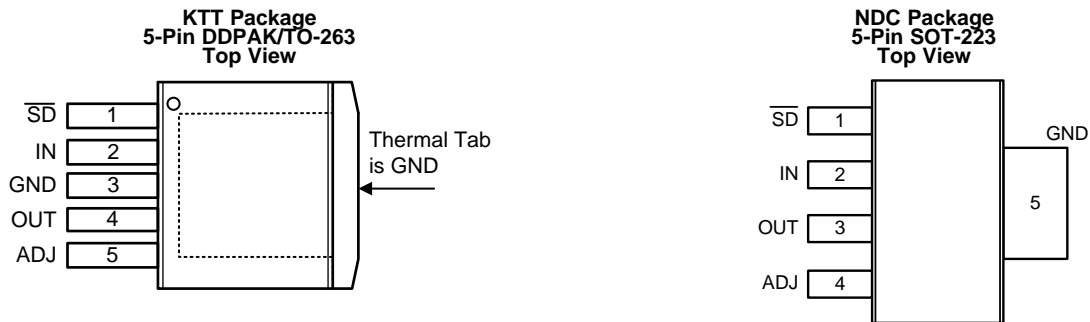
• 「製品情報」表、「ピン構成および機能」セクション、「ESD定格」および「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• タイトルおよびページ1のテキストの「リニア・レギュレータ」を「LDO」に変更	1
• 非推奨になったTO-220パッケージに関するすべての情報を削除	1
• 図および本文で、VINおよびVOUTピン名をすべてINおよびOUTに変更	1
• Deleted "(survival)" from <i>Abs Max</i> rows	4
• Changed Changed $R_{\theta JA}$ values: SOT-223 package from "90°C/W" to "65.2°C/W", DPAK/TO-263 package from "60°C/W" to "40.3°C/W"	4
• Added updated <i>Thermal Values</i> table and footnotes	4
• Deleted all "Heatsinking" subsections as they have out-of-date information; added <i>Power Dissipation and Estimating Junction Temperature</i>	12

### Revision C (April 2013) から Revision D に変更

Page

• Changed layout of National Semiconductor data sheet to TI format	15
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## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN NUMBER		I/O	DESCRIPTION
	NUMBER			
	DDPAK/TO-263	SOT-223		
ADJ	5	4	O	The ADJ pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2.
GND	3	5	—	Ground
IN	2	2	I	Input supply
OUT	4	3	O	Output voltage
$\overline{SD}$	1	1	I	Shutdown

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
IN pin to GND pin voltage	-0.3	7.5	V
Shutdown ( $\overline{SD}$ ) pin to GND pin voltage	-0.3	7.5	V
OUT pin to GND pin voltage <sup>(3), (4)</sup>	-0.3	6	V
$I_{OUT}$	Short-circuit protected		
Power dissipation <sup>(5)</sup>	Internally limited		
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
- (3) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
- (4) The output PMOS structure contains a diode between the IN and OUT pins. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200 mA of DC current and 1 A of peak current.
- (5) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heat sink values (if a heat sink is used). If power dissipation causes the junction temperature to exceed specified limits, the device goes into thermal shutdown.

### 6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
$V_{IN}$ supply voltage <sup>(1)</sup>	2.5	7	V
Shutdown ( $\overline{SD}$ ) voltage	-0.3	7	V
Maximum operating current (DC) $I_{OUT}$		1.5	A
Junction temperature	-40	125	°C

- (1) The minimum operating value for  $V_{IN}$  is equal to either [ $V_{OUT(NOM)} + V_{DROPOUT}$ ] or 2.5 V, whichever is greater.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LP3875-ADJ		UNIT
	NDC (SOT-223)	KTT (TO-263)	
	5 PINS	5 PINS	
$R_{\theta JA}$ <sup>(2)</sup> Junction-to-ambient thermal resistance, High K	65.2	40.3	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	47.2	43.4	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	9.9	23.1	°C/W
$\psi_{JT}$ Junction-to-top characterization parameter	3.4	11.5	°C/W
$\psi_{JB}$ Junction-to-board characterization parameter	9.7	22	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	n/a	1	°C/W

- (1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
- (2) Thermal resistance value  $R_{\theta JA}$  is based on the EIA/JEDEC High-K printed circuit board defined by JESD51-7 - *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

## 6.5 Electrical Characteristics

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{O(NOM)} + 1\text{ V}$ ,  $I_L = 10\text{ mA}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $V_{SD} = 2\text{ V}$ .

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$V_{ADJ}$ ADJ pin voltage	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$ $10\text{ mA} \leq I_L \leq 1.5\text{ A}$	1.198	1.216	1.234	V
	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$ $10\text{ mA} \leq I_L \leq 1.5\text{ A}$ $-40^\circ\text{C}$ to $125^\circ\text{C}$	1.180	1.216	1.253	V
$I_{ADJ}$ ADJ pin input current	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$ $10\text{ mA} \leq I_L \leq 1.5\text{ A}$		10		nA
	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$ $10\text{ mA} \leq I_L \leq 1.5\text{ A}$ $-40^\circ\text{C}$ to $125^\circ\text{C}$			100	nA
$\Delta V_{OL}$ Output voltage line regulation <sup>(3)</sup>	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$		0.02%		
	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 7\text{ V}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.06%		
$\frac{\Delta V_O}{\Delta I_{OUT}}$ Output voltage load regulation <sup>(3)</sup>	$10\text{ mA} \leq I_L \leq 1.5\text{ A}$		0.06%		
	$10\text{ mA} \leq I_L \leq 1.5\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.12%		
$V_{IN} - V_{OUT}$ Dropout voltage <sup>(4)</sup>	$I_L = 150\text{ mA}$		38	50	mV
	$I_L = 150\text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			60	
	$I_L = 1.5\text{ A}$		380	450	
	$I_L = 1.5\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			550	
$I_{GND}$ Ground pin current in normal operation mode	$I_L = 150\text{ mA}$		5	9	mA
	$I_L = 150\text{ mA}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			10	
	$I_L = 1.5\text{ A}$		6	14	
	$I_L = 1.5\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			15	
$I_{GND}$ Ground pin current in shutdown mode	$V_{SD} \leq 0.3\text{ V}$		0.01	10	$\mu\text{A}$
	$-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$			50	
$I_{O(PK)}$ Peak output current	$V_{OUT} \geq V_{O(NOM)} - 4\%$		1.8		A
<b>SHORT CIRCUIT PROTECTION</b>					
$I_{SC}$ Short-circuit current			3.2		A

(1) Limits are specified by testing, design, or statistical correlation.

(2) Typical numbers are at  $25^\circ\text{C}$  and represent the most likely parametric norm.

(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5 V and above. For output voltages below 2.5 V, the dropout voltage is nothing but the input to output differential, because the minimum input voltage is 2.5 V.

**Electrical Characteristics (continued)**

 Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = V_{O(NOM)} + 1\text{ V}$ ,  $I_L = 10\text{ mA}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $V_{SD} = 2\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
<b>SHUTDOWN INPUT</b>						
$V_{SDT}$	Shutdown threshold	Output = high		$V_{IN}$		V
		Output = high, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	2			
		Output = low		0		
		Output = low, $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$			0.3	
$T_{d(OFF)}$	Turnoff delay	$I_L = 1.5\text{ A}$		20		$\mu\text{s}$
$T_{d(ON)}$	Turnon delay	$I_L = 1.5\text{ A}$		25		$\mu\text{s}$
$I_{SD}$	$\overline{SD}$ input current	$V_{SD} = V_{IN}$		1		nA
<b>AC PARAMETERS</b>						
PSRR	Ripple rejection	$V_{IN} = V_{OUT} + 1\text{ V}$ , $C_{OUT} = 10\ \mu\text{F}$ $V_{OUT} = 3.3\text{ V}$ , $f = 120\text{ Hz}$		73		dB
		$V_{IN} = V_{OUT} + 0.5\text{ V}$ , $C_{OUT} = 10\ \mu\text{F}$ $V_{OUT} = 3.3\text{ V}$ , $f = 120\text{ Hz}$		57		
$\rho_{n(f)}$	Output noise density	$f = 120\text{ Hz}$		0.8		$\mu\text{V}$
$e_n$	Output noise voltage	$BW = 10\text{ Hz} - 100\text{ kHz}$ , $V_{OUT} = 2.5\text{ V}$		150		$\mu\text{V}_{RMS}$
		$BW = 300\text{ Hz} - 300\text{ kHz}$ , $V_{OUT} = 2.5\text{ V}$		100		

### 6.6 Typical Characteristics

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $\overline{\text{SD}}$  pin is tied to  $V_{IN}$ ,  $V_{OUT} = 2.5\ \text{V}$ ,  $V_{IN} = V_{O(NOM)} + 1\ \text{V}$ ,  $I_L = 10\ \text{mA}$

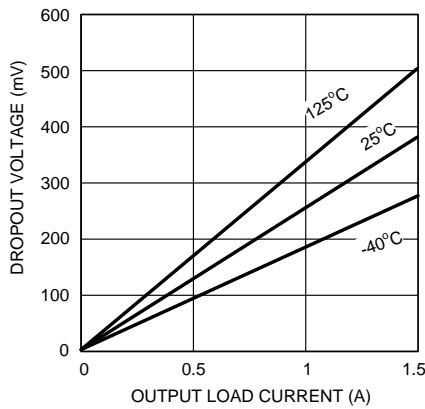
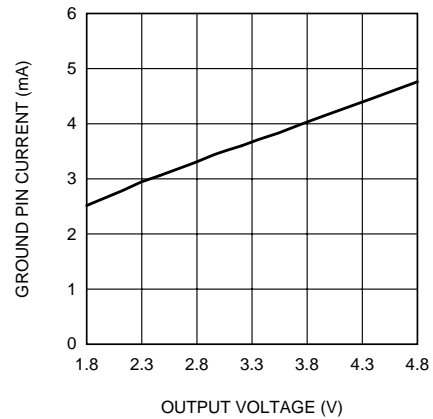


Figure 1. Dropout Voltage vs Output Load Current



$I_L = 1.5\ \text{A}$

Figure 2. Ground Current vs Output Voltage

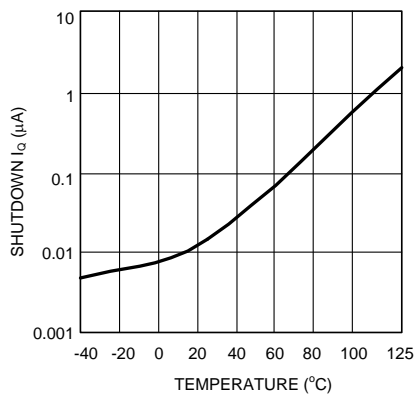


Figure 3. Shutdown  $I_Q$  vs Junction Temperature

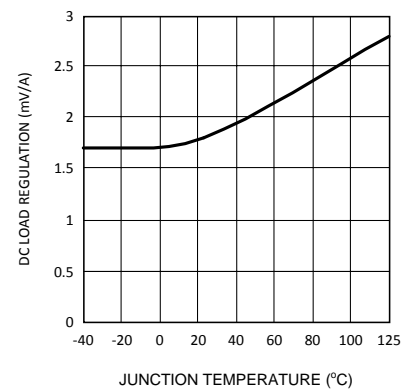


Figure 4. DC Load Regulation vs Junction Temperature

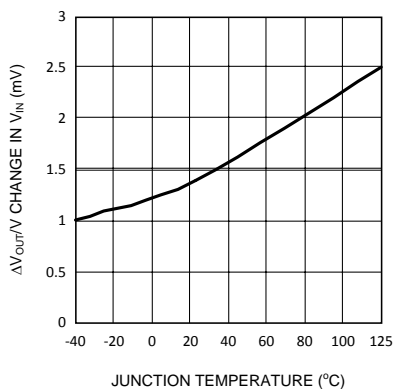


Figure 5. DC Line Regulation vs Temperature

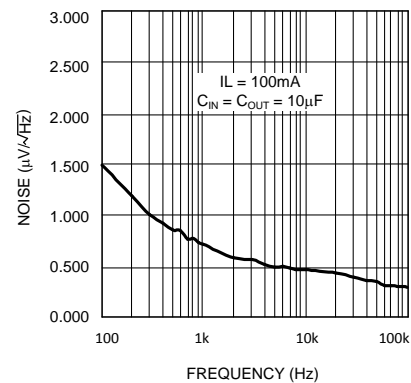


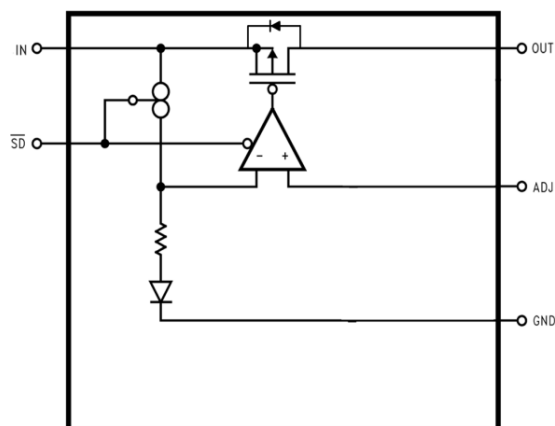
Figure 6. Noise vs Frequency

## 7 Detailed Description

### 7.1 Overview

The LP3875-ADJ linear regulator is designed to provide an ultra-low-dropout voltage with excellent transient response and load/line regulation. For battery-powered always-on type applications, the very low quiescent current of the LP3875-ADJ in shutdown mode helps reduce battery drain.

### 7.2 Functional Block Diagram



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### 7.3 Feature Description

#### 7.3.1 Shutdown ( $\overline{SD}$ )

The LM3875-ADJ device has a shutdown feature that turns the device off and reduces the quiescent current to 10 nA (typical).

#### 7.3.2 Short-Circuit Protection

The LP3875-ADJ is short-circuit protected and, in the event of a peak overcurrent condition, the short-circuit control loop rapidly drives the output PMOS pass element off. Once the power pass element shuts down, the control loop rapidly cycles the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Refer to [Power Dissipation](#) for power dissipation calculations.

#### 7.3.3 Dropout Voltage

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the  $R_{DS(ON)}$  of the internal MOSFET.

### 7.4 Device Functional Modes

#### 7.4.1 Shutdown Mode

A CMOS logic low level signal at the shutdown ( $\overline{SD}$ ) pin turns off the regulator. The  $\overline{SD}$  pin must be actively terminated through a 10-k $\Omega$  pullup resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail-to-rail comparator), the pullup resistor is not required. This pin must be tied to  $V_{IN}$  if not used.

#### 7.4.2 Active Mode

When voltage at  $\overline{SD}$  pin of the LP3875-ADJ device is at logic high level, the device is in normal mode of operation.



## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

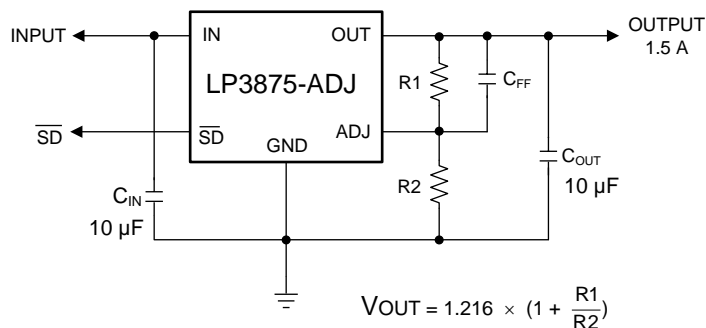
### 8.1 Application Information

The LP3875-ADJ device is an LDO linear regulator designed to provide high load current of up to 1.5 A, low dropout voltage, and low quiescent current in shutdown mode. Figure 7 shows the typical application circuit for this device.

#### 8.1.1 Reverse Current Path

The internal MOSFET in the LP3875-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200-mA continuous and 1-A peak.

### 8.2 Typical Application



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Figure 7. LP3875-ADJ Typical Application Circuit

#### 8.2.1 Design Requirements

For typical linear regulator LDO applications, use the parameters listed in Table 1:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 7 V
Output voltage	1.8 V
Output current	1.5 A
Output capacitor	10 µF
Input capacitor	10 µF
Output capacitor ESR range	100 mΩ to 4 Ω

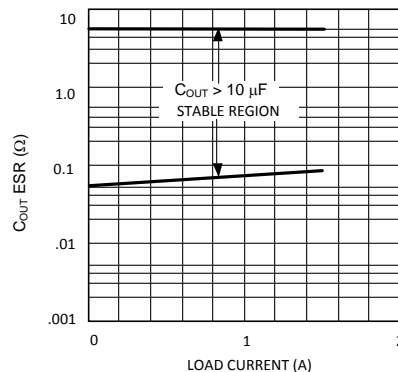
## 8.2.2 Detailed Design Procedure

### 8.2.2.1 External Capacitors

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

- Input Capacitor: An input capacitor of at least 10  $\mu\text{F}$  is required. Ceramic, tantalum, or electrolytic capacitors may be used, and capacitance may be increased without limit.
- Output Capacitor: An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see [Layout](#)).

The minimum value of output capacitance that can be used for stable full-load operation is 10  $\mu\text{F}$ , but it may be increased without limit. The output capacitor must have an equivalent series resistance (ESR) value as shown in [Figure 8](#). TI recommends tantalum capacitors for the output capacitor.



**Figure 8. ESR Curve**

### 8.2.2.2 $C_{FF}$ (Feed Forward Capacitor)

The capacitor  $C_{FF}$  is required to add phase lead and help improve loop compensation. The correct amount of capacitance depends on the value selected for  $R1$  (see [Figure 7](#)). Select a capacitor such that the zero frequency as given by the equation shown below is approximately 45 kHz:

$$F_z = 45,000 = 1 / ( 2 \times \pi \times R1 \times C_{FF} ) \quad (1)$$

Use a good-quality ceramic with X5R or X7R dielectric for the  $C_{FF}$  capacitor.

### 8.2.2.3 Selecting a Capacitor

Capacitance tolerance and variation with temperature must be considered when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good tantalum capacitor shows very little capacitance variation with temperature, but a ceramic capacitor may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is how the ESR of a capacitor changes with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see [Capacitor Characteristics](#)).

### 8.2.2.4 Capacitor Characteristics

#### 8.2.2.4.1 Ceramic

For values of capacitance in the 10- $\mu\text{F}$  to 100- $\mu\text{F}$  range, ceramics are usually larger and more costly than tantalum capacitors but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 m $\Omega$ ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

If ceramic capacitors are used, TI recommends X7R and X5R dielectric ceramic capacitors as they typically maintain a capacitance range within  $\pm 20\%$  of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

#### 8.2.2.4.2 Tantalum

TI recommends using solid tantalum capacitors on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good-quality tantalum typically shows a capacitance value that varies less than 10-15% across the full temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . ESR varies only about 2x going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

#### 8.2.2.4.3 Aluminum

Aluminium capacitors offer the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and equivalent series inductance (ESL).

Compared by size, the ESR of an aluminum electrolytic is higher than either tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50x when going from  $25^{\circ}\text{C}$  down to  $-40^{\circ}\text{C}$ .

Also note that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high-frequency performance. Use only aluminum electrolytics that have an impedance specified at a higher frequency (from 20 kHz to 100 kHz) for the LP3875-ADJ. Derating must be applied to the manufacturer's ESR specification, because it is typically only valid at room temperature.

Any applications using aluminum electrolytics must be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

#### 8.2.2.5 Setting The Output Voltage

The output voltage is set using the resistors R1 and R2 (see [Figure 7](#)). The output is also dependent on the reference voltage (typically 1.216 V) which is measured at the ADJ pin. The output voltage is given by the equation:

$$V_{\text{OUT}} = V_{\text{ADJ}} \times (1 + R1 / R2) \quad (2)$$

This equation does not include errors due to the bias current flowing in the ADJ pin which is typically about 10 nA. This error term is negligible for most applications. If R1 is  $> 100\text{k}\Omega$ , a small error may be introduced by the ADJ bias current.

The tolerance of the external resistors used contributes a significant error to the output voltage accuracy, with 1% resistors typically adding a total error of approximately 1.4% to the output voltage (this error is in addition to the tolerance of the reference voltage at  $V_{\text{ADJ}}$ ).

#### 8.2.2.6 Turnon Characteristics for Output Voltages Programmed to 2 V or Less

As  $V_{\text{IN}}$  increases during start-up, the regulator output will track the input until  $V_{\text{IN}}$  reaches the minimum operating voltage (typically about 2.2 V). For output voltages programmed to 2 V or less, the regulator output may momentarily exceed its programmed output voltage during start-up. Outputs programmed to voltages above 2 V are not affected by this behavior.

### 8.2.2.7 RFI/EMI Susceptibility

Radio frequency interference (RFI) and electromagnetic interference (EMI) can degrade the performance of any device because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the device regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the device.

If a load is connected to the device output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the device output. Because the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the device at frequencies above 100 kHz is determined only by the output capacitors.

In applications where the load is switching at high speed, the output of the device may need RF isolation from the load. TI recommends that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, because RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from *clean* circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multilayer PCB applications, care must be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

### 8.2.2.8 Output Noise

Noise is specified in two ways:

- Spot Noise (or Output Noise Density): the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- Total Output Noise (or Broad-Band Noise): the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention must be paid to the units of measurement. Spot noise is measured in units  $\mu\text{V}/\sqrt{\text{Hz}}$  or  $\text{nV}/\sqrt{\text{Hz}}$  and total output noise is measured in  $\mu\text{V}_{(\text{RMS})}$ .

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area decreases the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (GND pin current). Using an optimized trade-off of the GND pin current and die size, the LP3875-ADJ achieves low noise performance and low quiescent-current operation.

The total output noise specification for LP3875-ADJ is presented in the [Electrical Characteristics](#). The output noise density at different frequencies is represented by a curve under [Typical Characteristics](#).

### 8.2.2.9 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with [Equation 3](#).

$$P_{D(\text{MAX})} = (V_{\text{IN}(\text{MAX})} - V_{\text{OUT}}) \times I_{\text{OUT}} \quad (3)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage ( $V_{\text{DO}}$ ). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the TO-263 (KTT) package, the primary conduction path for heat is through the thermal tab into the PCB. In this package, the die is connected directly to the thermal pad and the heat generated in the die (junction) has a direct path through the large thermal tab into the PCB copper area.

In the SOT-223 (NDC) package, the primary conduction path for heat is through the GND Tab (pin 5) into the PCB. While the die (junction) is connected directly to the GND tab metal, this thermal path is longer and has a higher thermal resistance value than the TO-263.

To ensure the best thermal performance, place as large of a copper area directly under the thermal tab as is possible, and connect the thermal tab, through multiple thermal vias, to an internal ground plane with an appropriate amount of copper PCB area.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ), according to [Equation 4](#) or [Equation 5](#):

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (4)$$

$$P_{D(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (5)$$

Unfortunately, this  $R_{\theta JA}$  is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The  $R_{\theta JA}$  recorded in [Thermal Information](#) is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout for the TO-263 (KTT),  $R_{\theta JA}$  is actually the sum of the package junction-to-case (bottom) thermal resistance ( $R_{\theta JCbot}$ ) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

### 8.2.2.10 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi ( $\Psi$ ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) are given in [Thermal Information](#) and are used in accordance with [Equation 6](#) or [Equation 7](#).

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- $P_{D(MAX)}$  is explained in [Equation 5](#)
- $T_{TOP}$  is the temperature measured at the center-top of the device package. (6)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

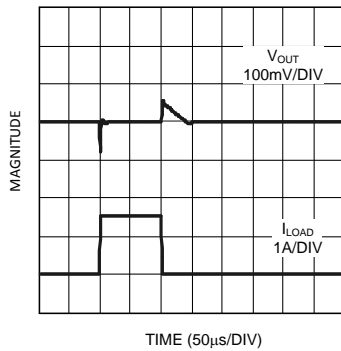
where

- $P_{D(MAX)}$  is explained in [Equation 5](#).
- $T_{BOARD}$  is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (7)

For more information about the thermal characteristics  $\Psi_{JT}$  and  $\Psi_{JB}$ , see [Semiconductor and IC Package Thermal Metrics](#); for more information about measuring  $T_{TOP}$  and  $T_{BOARD}$ , see [Using New Thermal Metrics](#); and for more information about the EIA/JEDEC JESD51 PCB used for validating  $R_{\theta JA}$ , see the [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#). These application notes are available at [www.ti.com](http://www.ti.com).

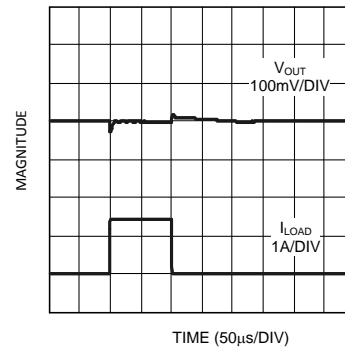
### 8.2.3 Application Curves

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $\overline{\text{SD}}$  pin is tied to  $V_{IN}$ ,  $V_{OUT} = 2.5\ \text{V}$ ,  $V_{IN} = V_{O(NOM)} + 1\ \text{V}$ ,  $I_L = 10\ \text{mA}$



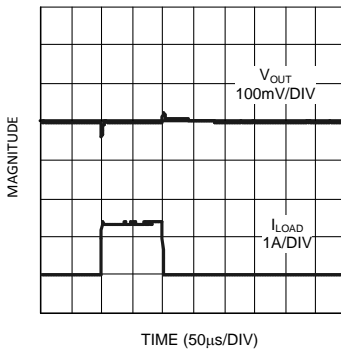
$C_{IN} = C_{OUT} = 10\ \mu\text{F}$ , Oscon

**Figure 9. Load Transient Response**



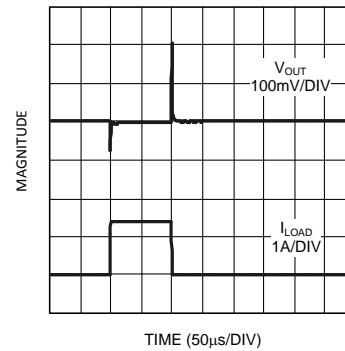
$C_{IN} = C_{OUT} = 100\ \mu\text{F}$ , Oscon

**Figure 10. Load Transient Response**



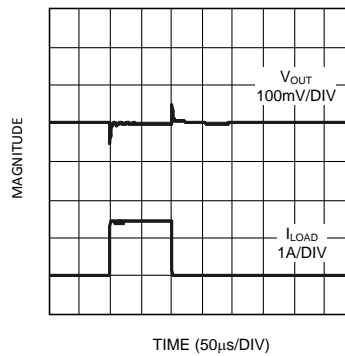
$C_{IN} = C_{OUT} = 100\ \mu\text{F}$ , POSCAP

**Figure 11. Load Transient Response**



$C_{IN} = C_{OUT} = 10\ \mu\text{F}$ , Tantalum

**Figure 12. Load Transient Response**



$C_{IN} = C_{OUT} = 100\ \mu\text{F}$ , Tantalum

**Figure 13. Load Transient Response**

## 9 Power Supply Recommendations

The LP3875-ADJ device is designed to operate from an input supply voltage range of 2.5 V to 7 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP3875-ADJ output voltage is well regulated, the input supply must be at least  $V_{OUT} + 0.5$  V, or 2.5 V, whichever is higher. A minimum capacitor value of 10  $\mu$ F is required to be within 1 cm of the IN pin.

## 10 Layout

### 10.1 Layout Guidelines

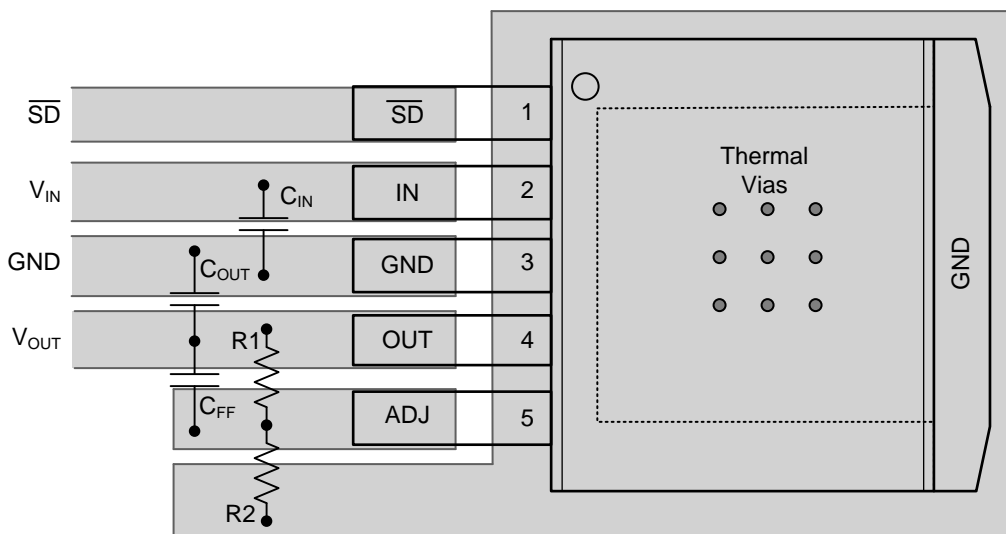
Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the IN, OUT, and GND pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out  $C_{IN}$  and  $C_{OUT}$  near the device with short traces to the IN, OUT, and GND pins. Connect the GND pin to the external circuit ground so that the regulator and its capacitors have a single-point ground.

Note that stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the device and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single-point ground technique for the regulator and its capacitors solved the problem.

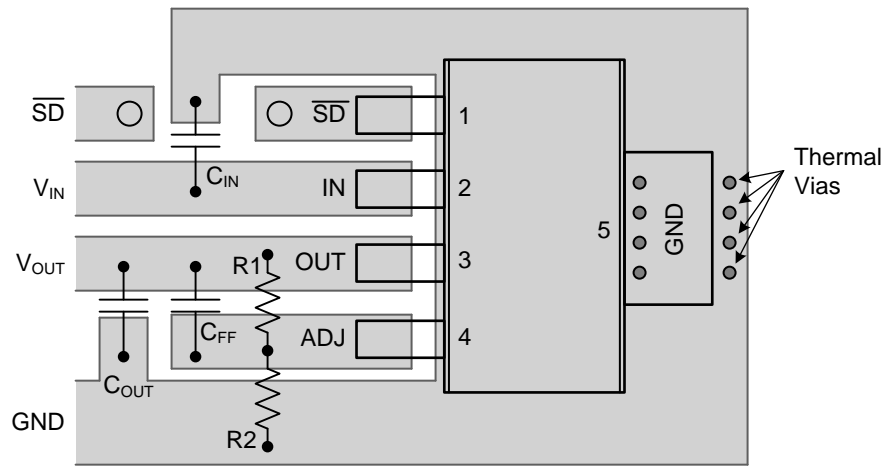
Because high current flows through the traces going into  $V_{IN}$  and coming from  $V_{OUT}$ , Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

### 10.2 Layout Examples



**Figure 14. Layout Example for DDPAK/TO-263 Package**

**Layout Examples (continued)**



**Figure 15. Layout Example for SOT-223 Package**



## 11 デバイスおよびドキュメントのサポート

### 11.1 関連資料

詳細情報については、以下を参照してください。

- 『[半導体およびICパッケージの熱指標](#)』
- 『[新しい温度指標の使用](#)』
- 『[JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性](#)』

### 11.2 ドキュメントの更新通知を受け取る方法

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### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3875EMP-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LHSB	<a href="#">Samples</a>
LP3875EMPX-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LHSB	<a href="#">Samples</a>
LP3875ES-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES ADJ	<a href="#">Samples</a>
LP3875ESX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3875ES ADJ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3875EMP-ADJ/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875EMPX-ADJ/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3875ESX-ADJ/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3875EMP-ADJ/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3875EMPX-ADJ/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3875ESX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LP3875ES-ADJ/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19



KTT0005B



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