

# LP5861T 18 チャンネル大電流 LED ドライバ、8 ビット・アナログおよび 8/16 ビット PWM 調光付き

## 1 特長

- 動作電圧範囲:
  - $V_{CC}/V_{LED}$  範囲: 2.7V~5.5V
  - 1.8V、3.3V、5V と互換性のあるロジック・ピン
- 18 個の大電流および高精度定電流シンク:
  - 電流シンクあたり 125mA ( $V_{CC} \geq 3.3V$ )
  - デバイス間誤差:  $\pm 5\%$
  - チャンネル間誤差:  $\pm 5\%$
  - 位相シフトによる過渡電力の平衡化
- 極めて低い消費電力:
  - シャットダウン・モード:  $I_{CC} \leq 2\mu A$  (EN = Low 時)
  - スタンバイ・モード:  $I_{CC} \leq 10\mu A$  (EN = High および CHIP\_EN = 0 (データ保持) 時)
  - アクティブ・モード:  $I_{CC} = 5mA$  (代表値、チャンネル電流 = 12.5mA)
- 柔軟な調光オプション:
  - 各 LED ドットを個別にオン / オフ制御
  - アナログ調光 (電流ゲイン制御)
    - すべての LED ドットに対するグローバル 3 ビット最大電流 (MC) 設定
    - 3 グループの 7 ビット・カラー電流 (CC) 設定 (赤、緑、青)
    - 各 LED ドットに対する個別の 8 ビット・ドット電流 (DC) 設定
  - 可聴ノイズが発生しない周波数を使った PWM 調光
    - すべての LED ドットに対するグローバル 8 ビット PWM 調光
    - LED ドットの任意マッピングのための 8 ビット PWM 調光のプログラム可能な 3 つのグループ
    - 各 LED ドットに対する個別の 8 ビットまたは 16 ビット PWM 調光
- データ通信量を最小限に抑えるための完全にアドレス指定可能な SRAM
- 個別の LED ドット開放 / 短絡検出
- ゴースト除去および低輝度補償機能
- インターフェイス・オプション:
  - 1MHz (最大値) の I<sup>2</sup>C インターフェイス (IFS = LOW 時)
  - 12MHz (最大値) の SPI インターフェイス (IFS = HIGH 時)

## 2 アプリケーション

- LED アニメーションおよび表示:
  - 大型およびスマート家電

- グローバル RGB キーボードのバックライト
- 屋外キーパッドのバックライト
- ビデオ監視および IP カメラ用 IR モジュール
- 光学モジュール内のレーザー・ダイオード

## 3 概要

LP5861T は、大電流で高性能の LED マトリクス・ドライバです。本デバイスは  $N \times 18$  の LED ドットまたは  $N \times 6$  の RGB LED をサポートするための  $N$  個 ( $N = 6/8/11$ ) のスイッチング MOSFET を備えた 18 個の定電流シンクを内蔵しています。LP5861T は、18 個の LED ドットまたは 6 個の RGB LED をサポートする直接駆動バージョンです。

LP5861T はアナログ調光法と PWM 調光法の両方をサポートしています。アナログ調光の場合、各 LED ドットを 256 ステップで調整できます。PWM 調光の場合、内蔵の 8 ビットまたは 16 ビット構成可能 PWM ジェネレータが、滑らかで可聴ノイズの発生しない調光制御を実現します。各 LED ドットを 8 ビット・グループ PWM に任意に割り当てることで、調光制御をまとめて行うこともできます。

LP5861T デバイスは、データ通信量を最小限に抑えるために、完全にアドレス指定可能な SRAM を実装しています。上側と下側のゴーストを除去するため、ゴースト・キャンセル回路を内蔵しています。LP5861T は LED 開放 / 短絡検出機能もサポートしています。LP5861T では、1MHz (最大値) の I<sup>2</sup>C と 12MHz (最大値) の SPI が使用できます。

### パッケージ情報

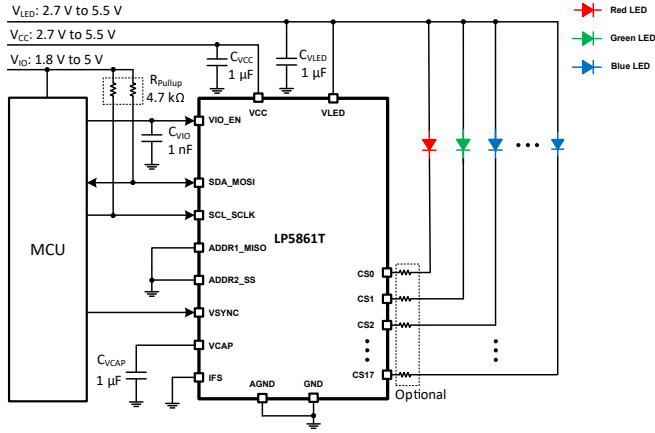
部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
LP5861T	RSM (VQFN, 32)	4.00mm × 4.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



**LP5861T**

JAJSOY5A – MAY 2023 – REVISED AUGUST 2023



**概略回路図**

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### 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (August 2023)	Page
• マーケティング・ステータスを「事前情報」から「量産データ」に変更.....	1

## 5 Device Comparison

PART NUMBER	MATERIAL	LED DOT NUMBER	MAX CURRENT PER CS	PACKAGE <sup>(2)</sup>	SOFTWARE COMPATIBLE
LP5861T	LP5861TRSMR	18 × 1 = 18	125 mA	VQFN-32	Yes
LP5866T	LP5866TRKPR	18 × 6 = 108	100 mA	VQFN-40	
LP5868T	LP5868TRKPR	18 × 8 = 144			
LP5860T	LP5860TRKPR	18 × 11 = 198			
LP5861	LP5861RSMR	18 × 1 = 18	50 mA	VQFN-32	
LP5862	LP5862RSMR	18 × 2 = 36		VQFN-32	
	LP5862DBTR			TSSOP-38	
LP5864	LP5864RSMR	18 × 4 = 72		VQFN-32	
	LP5864MRSR <sup>1</sup>			VQFN-40	
LP5866	LP5866RKPR	18 × 6 = 108		TSSOP-38	
	LP5866DBTR			VQFN-40	
	LP5866MDBTR <sup>1</sup>			VQFN-40	
LP5868	LP5868RKPR	18 × 8 = 144		VQFN-40	
LP5860	LP5860RKPR	18 × 11 = 198		VQFN-40	
	LP5860MRKPR <sup>1</sup>				

(1) Extended Temperature devices, supporting –55°C to approximately 125°C operating ambient temperature.

(2) The same packages are hardware compatible.

## 6 Pin Configuration and Functions

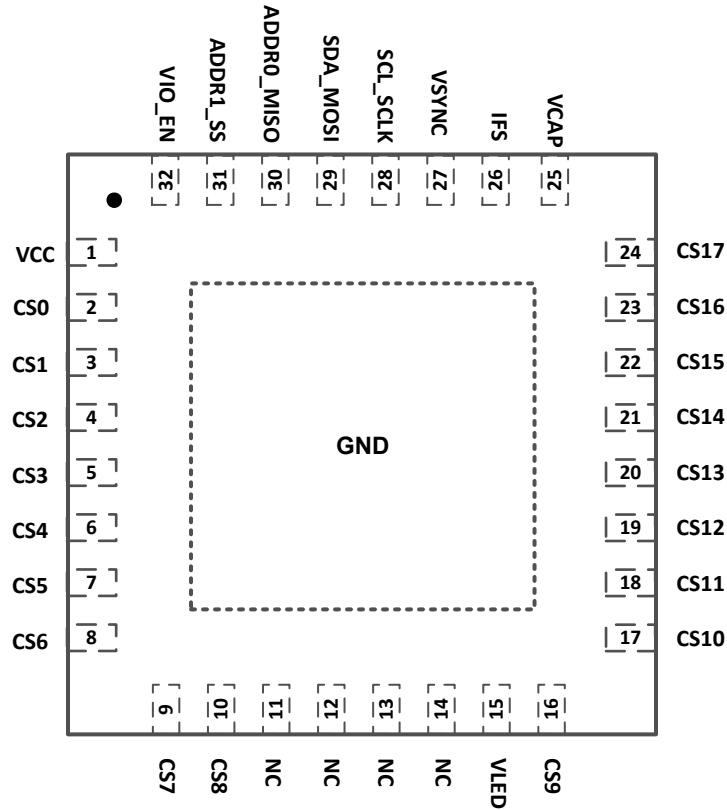


图 6-1. LP5861T RSM Package 32-Pin VQFN with Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	Power	Power supply for device. A 1- $\mu$ F capacitor must be connected between this pin with GND and be placed as close to the device as possible.
2	CS0	O	Current sink 0. If not used, this pin can be floating.
3	CS1	O	Current sink 1. If not used, this pin can be floating.
4	CS2	O	Current sink 2. If not used, this pin can be floating.
5	CS3	O	Current sink 3. If not used, this pin can be floating.
6	CS4	O	Current sink 4. If not used, this pin can be floating.
7	CS5	O	Current sink 5. If not used, this pin can be floating.
8	CS6	O	Current sink 6. If not used, this pin can be floating.
9	CS7	O	Current sink 7. If not used, this pin can be floating.
10	CS8	O	Current sink 8. If not used, this pin can be floating.
11/12/13/14	NC	O	No connection. This pin must be floating.
15	VLED	Power	Power input for high-side switches.
16	CS9	O	Current sink 9. If not used, this pin can be floating.
17	CS10	O	Current sink 10. If not used, this pin can be floating.
18	CS11	O	Current sink 11. If not used, this pin can be floating.
19	CS12	O	Current sink 12. If not used, this pin can be floating.
20	CS13	O	Current sink 13. If not used, this pin can be floating.

表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
21	CS14	O	Current sink 14. If not used, this pin can be floating.
22	CS15	O	Current sink 15. If not used, this pin can be floating.
23	CS16	O	Current sink 16. If not used, this pin can be floating.
24	CS17	O	Current sink 17. If not used, this pin can be floating.
25	VCAP	O	Internal LDO output. A 1- $\mu$ F capacitor must be connected between this pin with GND. Place the capacitor as close to the device as possible.
26	IFS	I	Interface type select. I <sup>2</sup> C is selected when IFS is low. SPI is selected when IFS is high. A resistor must be connected between VIO and this pin.
27	VSYNC	I	External synchronize signal for display mode 2 and mode 3.
28	SCL_SCLK	I	I <sup>2</sup> C clock input or SPI clock input. Pull up to VIO when configured as I <sup>2</sup> C.
29	SDA_MOSI	I/O	I <sup>2</sup> C data input or SPI leader output follower input. Pull up to VIO when configured as I <sup>2</sup> C.
30	ADDR0_MISO	I/O	I <sup>2</sup> C address select 0 or SPI leader input follower output
31	ADDR1_SS	I	I <sup>2</sup> C address select 1 or SPI follower select
32	VIO_EN	Power,I	Power supply for digital circuits and chip enable. A 1-nF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
Exposed Thermal Pad	GND	Ground	Common ground plane

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage on V <sub>CC</sub> / V <sub>LED</sub> / VIO / EN / CS / SW / SDA / SCL / SCLK / MOSI / MISO / SS / ADDR0 / ADDR1 / VSYNC / IFS		-0.3	6	V
Voltage on VCAP		-0.3	2	V
T <sub>J</sub>	Junction temperature	-55	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage on V <sub>CC</sub>	Supply voltage	2.7		5.5	V
Input voltage on V <sub>LED</sub>	LED supply voltage	2.7		5.5	V
Input voltage on VIO_EN		1.65		5.5	V
Voltage on SDA / SCL / SCLK / MOSI / MISO / SS / ADDR <sub>x</sub> / VSYNC / IFS				VIO	V
T <sub>A</sub>	Operating ambient temperature	-40		85	°C
T <sub>A</sub>	Operating ambient temperature - LP5861TMRSMR	-55		125	°C

### 7.4 Thermal Information

THERMAL METRIC		LP5861T	UNIT
		RSM (VQFN)	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	32.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	29.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	12.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.7	°C/W

## 7.5 Electrical Characteristics

$V_{CC} = 3.3V$ ,  $V_{LED} = 5V$ ,  $V_{IO} = 1.8V$  and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  ( $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  for LP5861TMRSMR); Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power supplies</b>						
$V_{CC}$	Device supply voltage		2.7		5.5	V
$V_{UVR}$	Undervoltage restart	$V_{CC}$ rising, Test mode			2.5	V
$V_{UVF}$	Undervoltage shutdown	$V_{CC}$ falling, Test mode	1.9			V
$V_{UV\_HYS}$	Undervoltage shutdown hysteresis			0.3		V
$V_{CAP}$	Internal LDO output	$V_{CC} = 2.7V$ to $5.5V$		1.78		V
$I_{CC}$	Shutdown supply current $I_{SHUTDOWN}$	$V_{EN} = 0$ , $CHIP\_EN = 0$ (bit), $ADDx = 0$ ; measure the total current from $V_{CC}$ and $V_{LED}$		0.1	1.5	$\mu A$
	Standby supply current $I_{STANDBY}$	$V_{EN} = 3.3V$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$		5.5	12	$\mu A$
	Active mode supply current $I_{NORMAL}$	$V_{EN} = 3.3V$ , $CHIP\_EN = 1$ (bit), all channels $I_{OUT} = 12.5$ mA (MC = 1, CC = 127, DC = 256), measure the current from $V_{CC}$		4.3	6	mA
$V_{LED}$	LED supply voltage		2.7		5.5	V
$V_{VIO}$	VIO supply voltage		1.65		5.5	V
$I_{VIO}$	VIO supply current	Interface idle			5	$\mu A$
<b>Output Stages</b>						
$I_{CS}$	Constant current sink output range (CS0 – CS17)	$2.7 \leq V_{CC} < 3.3V$ , PWM = 100%	0.1		75	mA
		$V_{CC} \geq 3.3V$ PWM = 100%	0.1		125	mA
$I_{LKG}$	Leakage current (CS0 – CS17)	channels off, up_degghost = 0, $V_{CS} = 5V$		0.1	1	$\mu A$
$I_{ERR\_DD}$	Device to device current error, $I_{ERR\_DD} = (I_{AVE} - I_{SET}) / I_{SET} \times 100\%$	All channels ON. Current set to 1 mA. MC = 0 CC = 17 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 25 mA. MC = 2 CC = 127 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 50 mA. MC = 4 CC = 127 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 75 mA. MC = 5 CC = 64 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 100 mA. MC = 7 CC = 127 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 125 mA. MC = 7 CC = 127 DC = 255 PWM = 100% (not apply to LP5861TMRSMR)	-7		7	%
$I_{ERR\_CC}$	Channel to channel current error, $I_{ERR\_CC} = (I_{OUTX} - I_{AVE}) / I_{AVE} \times 100\%$	All channels ON. Current set to 1 mA. MC = 0 CC = 17 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 25 mA. MC = 2 CC = 127 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 50 mA. MC = 4 CC = 127 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 75 mA. MC = 5 CC = 64 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 100 mA. MC = 5 CC = 64 DC = 255 PWM = 100%	-5		5	%
		All channels ON. Current set to 125 mA. MC = 7 CC = 127 DC = 255 PWM = 100% (not apply to LP5861TMRSMR)	-7		7	%
$f_{PWM}$	LED PWM frequency	PWM_Fre = 1		62.5		KHz
		PWM_Fre = 0		125		KHz



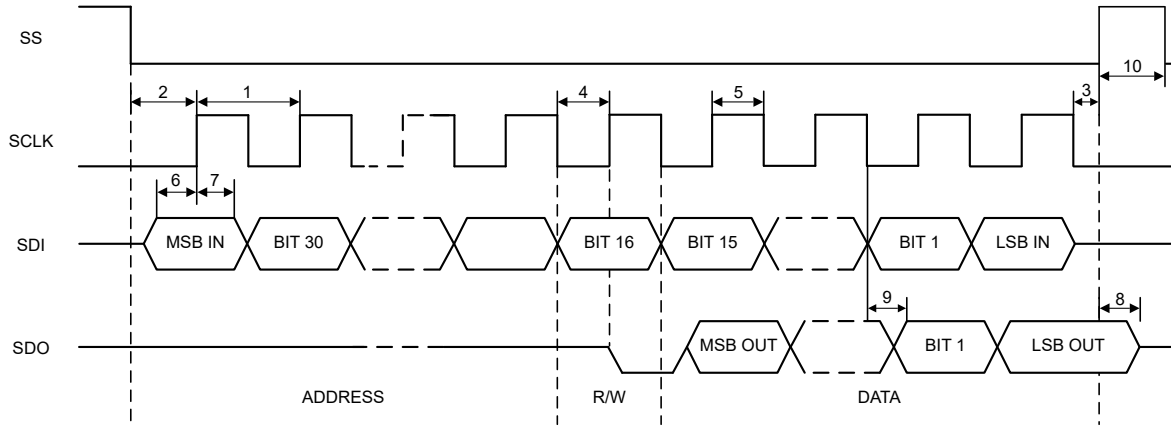
$V_{CC} = 3.3V$ ,  $V_{LED} = 5V$ ,  $V_{IO} = 1.8V$  and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  ( $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  for LP5861TMRSMR); Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SAT}$	Output saturation voltage	$I_{OUT} = 125mA$ , decreasing output voltage, when the LED current has dropped 5% (not apply to LP5861TMRSMR)			1	V
		$I_{OUT} = 100mA$ , decreasing output voltage, when the LED current has dropped 5% (only apply to LP5861TMRSMR)			0.8	V
		$I_{OUT} = 100mA$ , decreasing output voltage, when the LED current has dropped 5% (only apply to LP5861TRSMR)			0.7	V
		$I_{OUT} = 75mA$ , decreasing output voltage, when the LED current has dropped 5%			0.6	V
		$I_{OUT} = 25mA$ , decreasing output voltage, when the LED current has dropped 5%			0.5	V
<b>Logic Interfaces</b>						
$V_{LOGIC\_IL}$	Low-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS			0.3 x $V_{IO}$		V
$V_{LOGIC\_IH}$	High-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS		0.7 x $V_{IO}$			V
$V_{EN\_IL}$	Low-level input voltage of EN			0.4		V
$V_{EN\_IH}$	High-level input voltage of EN	When $V_{CAP}$ powered up	1.4			V
$I_{LOGIC\_I}$	Input current, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub>		-1		1	$\mu A$
$V_{LOGIC\_OL}$	Low-level output voltage, SDA, MISO	$I_{PULLUP} = 3 mA$			0.4	V
$V_{LOGIC\_OH}$	High-level output voltage, MISO	$I_{PULLUP} = -3 mA$	0.7 x $V_{IO}$			V
<b>Protection Circuits</b>						
$V_{LOD\_TH}$	Thershold for channel open detection			0.25		V
$V_{LSD\_TH}$	Thershold for channel short detection			$V_{LED} - 1$		V
$T_{TSD}$	Thermal-shutdown junction temperature			150		$^{\circ}C$
$T_{HYS}$	Thermal shutdown temperature hysteresis			15		$^{\circ}C$

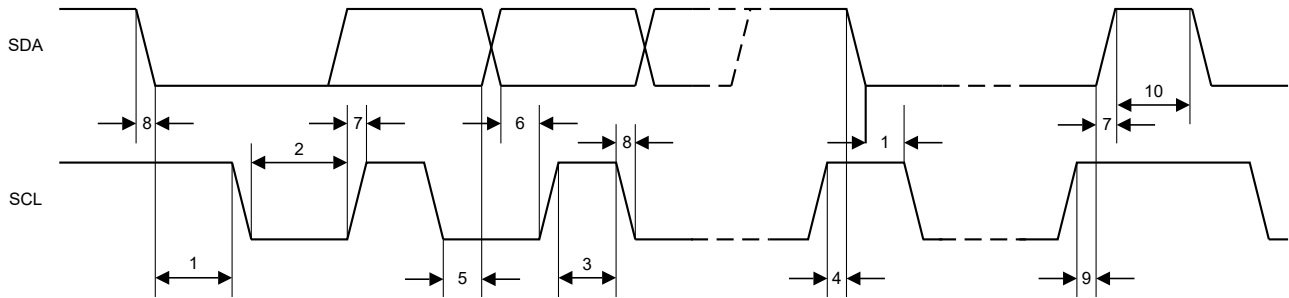
## 7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>MISC. Timing Requirements</b>					
$f_{OSC}$	Internal oscillator frequency		31.2		MHz
$f_{OSC\_ERR}$	Device to device oscillator frequency error	-3%		3%	
$t_{POR\_H}$	Wait time from UVLO disactive to device NORMAL			500	$\mu s$
$t_{CHIP\_EN}$	Wait time from setting Chip_EN (Register) =1 to device NORMAL			100	$\mu s$
$t_{RISE}$	LED output rise time		10		ns
$t_{FALL}$	LED output fall time		15		ns
$t_{VSYNC\_H}$	The minimum high-level pulse width of VSYNC	200			$\mu s$
<b>SPI timing requirements</b>					
$f_{SCLK}$	SPI Clock frequency			12	MHz
1	Cycle time	83.3			ns
2	SS active lead-time	50			ns
3	SS active leg time	50			ns

		MIN	NOM	MAX	UNIT
4	SS inactive time	50			ns
5	SCLK low time	36			ns
6	SCLK high time	36			ns
7	MOSI set-up time	20			ns
8	MOSI hold time	20			ns
9	MISO disable time			30	ns
10	MISO data valid time			35	ns
C <sub>b</sub>	Bus capacitance	5		40	pF
<b>I<sup>2</sup>C fast mode timing requirements</b>					
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	600			ns
2	Clock low time	1300			ns
3	Clock high time	600			ns
4	Setup time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data setup time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Setup time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			μs
<b>I<sup>2</sup>C fast mode plus timing requirements</b>					
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	0		1000	KHz
1	Hold time (repeated) START condition	260			ns
2	Clock low time	500			ns
3	Clock high time	260			ns
4	Setup time for a repeated START condition	260			ns
5	Data hold time	0			ns
6	Data setup time	50			ns
7	Rise time of SDA and SCL			120	ns
8	Fall time of SDA and SCL			120	ns
9	Setup time for STOP condition	260			ns
10	Bus free time between a STOP and a START condition	0.5			μs

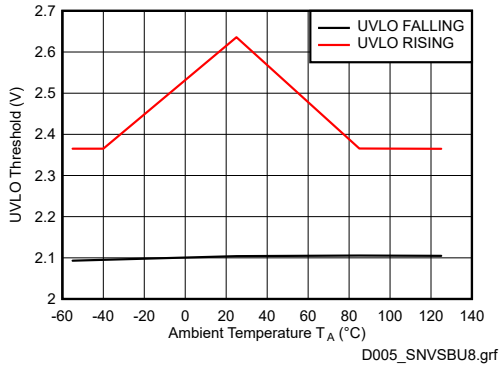


**7-1. SPI Timing Parameters**

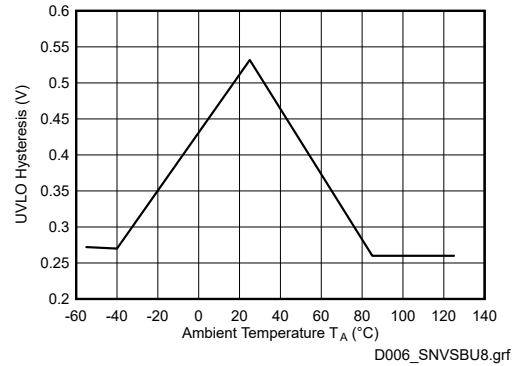


**7-2. I<sup>2</sup>C Timing Parameters**

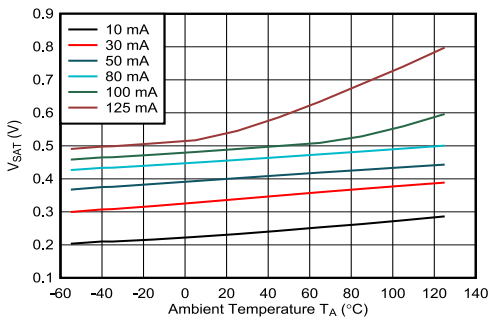
### 7.7 Typical Characteristics



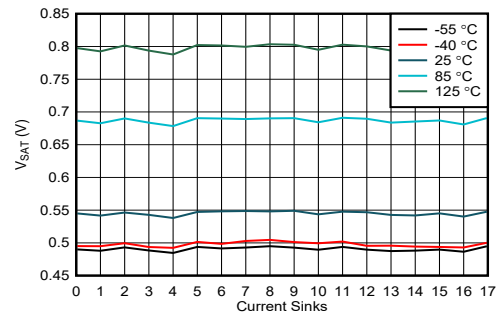
7-3. V<sub>CC</sub> UVLO Rising and Falling Thresholds



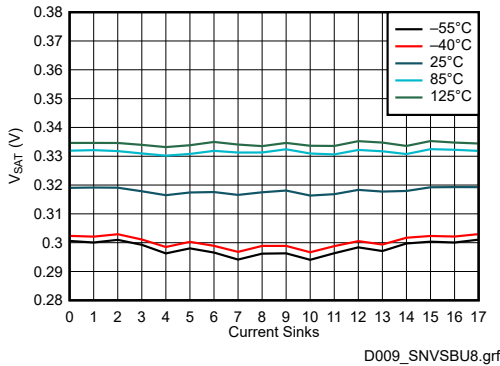
7-4. V<sub>CC</sub> UVLO Hysteresis



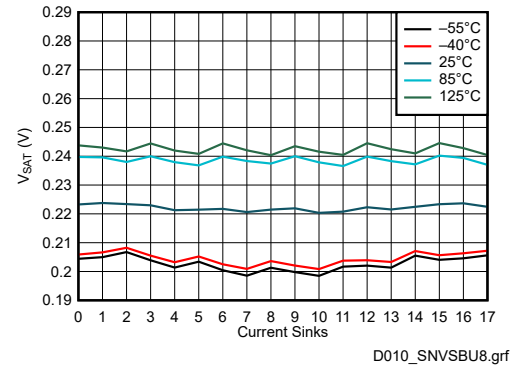
7-5. V<sub>SAT</sub> vs Temperature



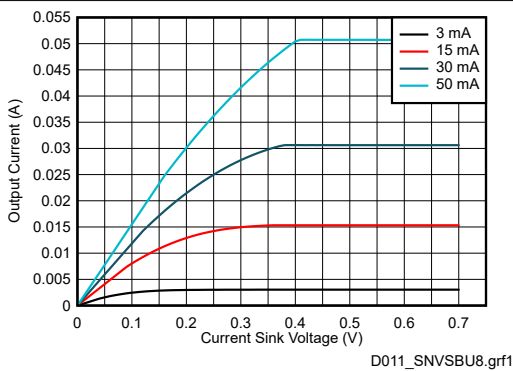
7-6. V<sub>SAT</sub> vs Current Sinks (125 mA)



7-7. V<sub>SAT</sub> vs Current Sinks (30 mA)

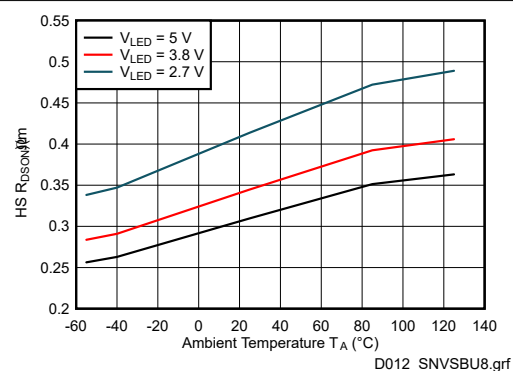


7-8. V<sub>SAT</sub> vs Current Sinks (10 mA)



T<sub>A</sub> = 25°C

7-9. Current Sinks Voltage vs Current



7-10. High Side Switch R<sub>DS(on)</sub>

## 8 Detailed Description

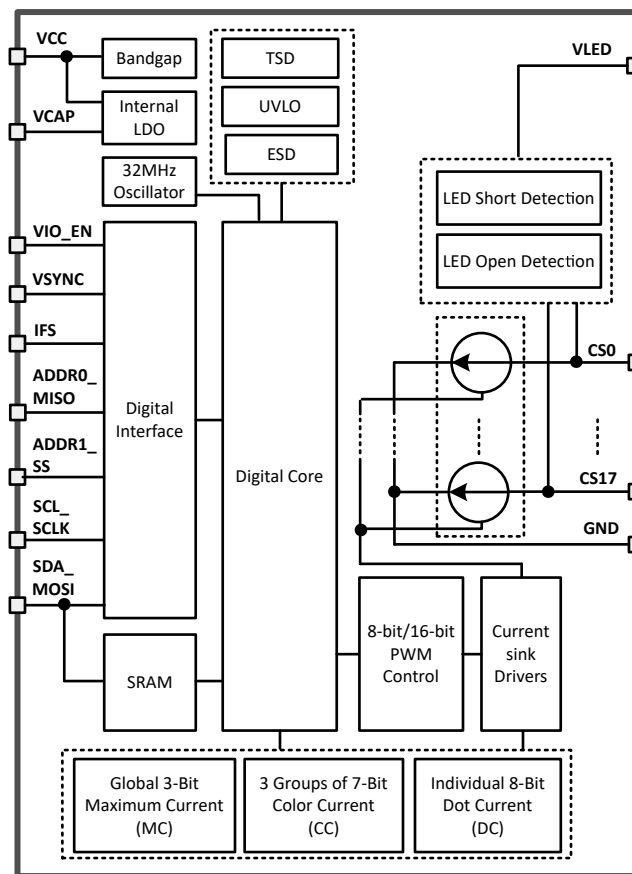
### 8.1 Overview

The LP5861T is an 18 channels high power LED driver. The device integrates 18 high-precision constant-current sinks. One LP5861T device can drive up to 18 LED dots or 6 RGB pixels by directly driving the LEDs.

The LP5861T supports both analog dimming and PWM dimming methods. For analog dimming, the current gain of each individual LED dot can be adjusted with 256 steps through 8-bits dot correction. For PWM dimming, the integrated 8-bits or 16-bits configurable, > 20-KHz PWM generators for each LED dot enable smooth, vivid animation effects without audible noise. Each LED can also be mapped into a 8-bits group PWM to achieve the group control with minimum data traffic.

The LP5861T device implements full addressable SRAM. The device supports entire SRAM data refresh and partial SRAM data update on demand to minimize the data traffic. The LP5861T implements the ghost cancellation circuit to eliminate both upside and downside ghosting. The LP5861T also uses low brightness compensation technology to support high density LED pixels. Both 1-MHz (maximum) I<sup>2</sup>C and 12-MHz (maximum) SPI interfaces are available in the LP5861T.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Analog Dimming (Current Gain Control)

Analog dimming of LP5861T is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 3-bits Maximum Current (MC) setting without external resistor
- 3 Groups of 7-bits Color Current (CC) setting
- Individual 8-bit Dot Current (DC) setting

## 注

When setting to small output current in low brightness situation, adjusting MC to a small value firstly can get smaller output saturation voltage.

### Global 3-Bits Maximum Current (MC) Setting

The MC is used to set the maximum current  $I_{OUT\_MAX}$  for each current sink and this current is the maximum peak current for each LED dot. The MC can be set with 3-bit (8 steps) from 7.5 mA to 125 mA. When the device is powered on, the MC data is set to default value 37.5 mA.

For data refresh [Mode 1](#), MC data is effective immediately after new data updated. For [Mode 2](#) and [Mode 3](#), to avoid unexpected MC data change during high speed data refreshing, MC data must be changed when all channels are off and new MC data is only be updated when the 'Chip\_EN' bit in Chip\_en register is set to 0, and after the 'Chip\_EN' returns to 1, the new MC data is effective. 'Down\_Deghost' and 'Up\_Deghost' in Dev\_config3 work in the similar way with MC.

表 8-1. Maximum Current (MC) Register Setting

3-BITS MAXIMUM_CURRENT REGISTER		$I_{OUT\_MAX}$
Binary	Decimal	mA
000	0	7.5
001	1	12.5
010	2	25
011 (default)	3 (default)	37.5 (default)
100	4	50
101	5	75
110	6	100
111	7	125

### 3 Groups of 7-Bits Color Current (CC) Setting

The LP5861T device is able to adjust the output current of three color groups separately. For each color, the device has 7-bits data in 'CC\_Group1', 'CC\_Group2', and 'CC\_Group3'. Thus, all color group currents can be adjusted in 128 steps from 0% to 100% of the maximum output current,  $I_{OUT\_MAX}$ .

The 18 current sinks have fixed mapping to the three color groups:

- CC-Group 1: CS0, CS3, CS6, CS9, CS12, CS15
- CC-Group 2: CS1, CS4, CS7, CS10, CS13, CS16
- CC-Group 3: CS2, CS5, CS8, CS11, CS14, CS17

表 8-2. 3 Groups of 7-bits Color Current (CC) Setting

7-BITS CC_GROUP1/CC_GROUP2/CC_GROUP3 REGISTER		RATIO OF OUTPUT CURRENT TO $I_{OUT\_MAX}$
Binary	Decimal	%
000 0000	0	0
000 0001	1	0.79
000 0010	2	1.57
---	---	---
100 0000 (default)	64 (default)	50.4 (default)
---	---	---
111 1101	125	98.4
111 1110	126	99.2
111 1111	127	100

### Individual 8-bit Dot Current (DC) Setting

The LP5861T can individually adjust the output current of each LED by using dot current function through DC setting. The device allows the brightness deviations of the LEDs to adjusted be individually. Each output DC is programmed with a 8-bit depth, so the value can be adjusted with 256 steps within the range from 0% to 100% of ( $I_{OUT\_MAX} \times CC/127$ ).

**表 8-3. Individual 8-bit Dot Current (DC) Setting**

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO $I_{OUT\_MAX} \times CC/127$
Binary	Decimal	%
0000 0000	0	0
0000 0001	1	0.39
0000 0010	2	0.78
---	---	---
1000 0000 (default)	128 (default)	50.2 (default)
---	---	---
1111 1101	253	99.2
1111 1110	254	99.6
1111 1111	255	100

In summary, the current gain of each current sink can be calculated as below:

$$I_{OUT} \text{ (mA)} = I_{OUT\_MAX} \times (CC/127) \times (DC/255) \quad (1)$$

### 8.3.2 PWM Dimming

There are several methods to control the PWM duty cycle of each LED dot.

- **Individual 8-bit / 16-bit PWM for Each LED Dot**

Every LED has an individual 8-bit or 16-bit PWM register that is used to change the LED brightness by PWM duty. The LP5861T uses an enhanced spectrum PWM (ES-PWM) algorithm to achieve 16-bit depth with high refresh rate and this can avoid flicker under high speed camera. Comparing with conventional 8-bit PWM, 16-bit PWM can help to achieve ultimate high dimming resolution in LED animation applications.

- **3 Programmable Groups of 8-bit PWM Dimming**

The group PWM Control is used to select LEDs into one to three groups where each group has a separate register for duty cycle control. Every LED has 2-bit selection in LED\_DOT\_GROUP Registers ( $x = 0, 1, \dots, 4$ ) to select whether the LED dot belongs to one of the three groups or not:

- 00: not a member of any group
- 01: member of group 1
- 10: member of group 2
- 11: member of group 3

- **8-bit PWM for Global Dimming**

The Global PWM Control function affects all LEDs simultaneously.

The final PWM duty cycle can be calculated as below:

$$PWM\_Final(8 \text{ bit}) = PWM\_Individual(8 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(8 \text{ bit}) \quad (2)$$

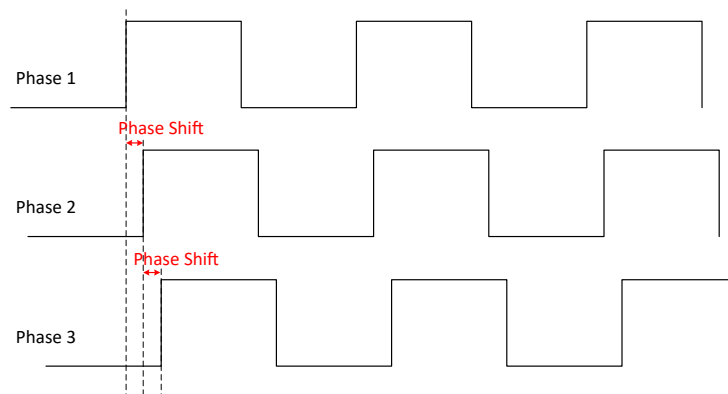
$$PWM\_Final(16 \text{ bit}) = PWM\_Individual(16 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(8 \text{ bit}) \quad (3)$$

The LP5861T supports 125-kHz or 62.5-kHz PWM output frequency. The PWM frequency is selected by configuring the 'PWM\_Fre' in Dev\_initial register. An internal 32-MHz oscillator is used for generating PWM

outputs. The oscillator's high accuracy design ( $f_{OSC\_ERR} \leq \pm 2\%$ ) enables a better synchronization if multiple LP5861T devices are connected together.

A PWM phase-shifting scheme is implemented in each current sink to avoid the current overshoot when turning on simultaneously. As the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. This scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases. By configuring the 'PWM\_Phase\_Shift' in Dev\_config1 register, which is default off, the LP5861T supports  $t_{phase\_shift} = 125\text{-ns}$  shifting time shown in [Figure 8-1](#).

- Phase 1: CS0, CS3, CS6, CS9, CS12, CS15
- Phase 2: CS1, CS4, CS7, CS10, CS13, CS16
- Phase 3: CS2, CS5, CS8, CS11, CS14, CS17

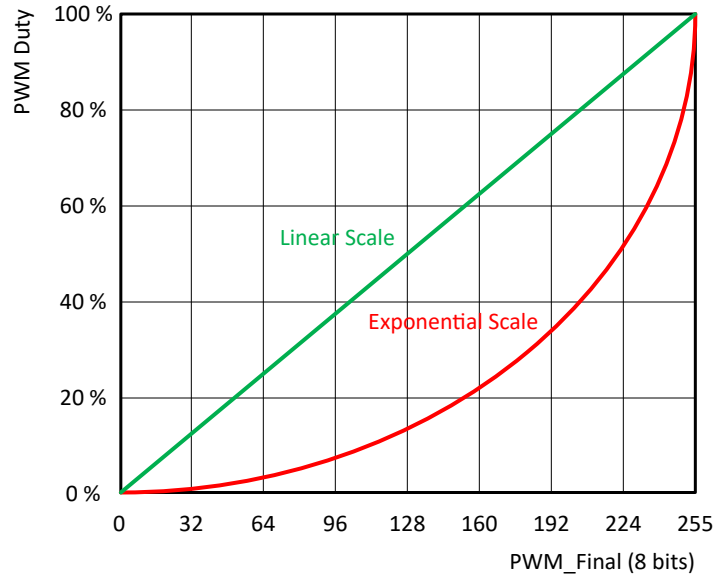


**Figure 8-1. Phase Shift**

- **Low Brightness Compensation:** three groups compensation are implemented to overcome the color-shift and non-uniformity in low brightness conditions. The compensation capability can be through 'Comp\_Group1', 'Comp\_Group2', and 'Comp\_Group3' in Dev\_config2 register.
  - Compensation\_group 1: CS0, CS3, CS6, CS9, CS12, CS15
  - Compensation\_group 2: CS1, CS4, CS7, CS10, CS13, CS16
  - Compensation\_group 3: CS2, CS5, CS8, CS11, CS14, CS17

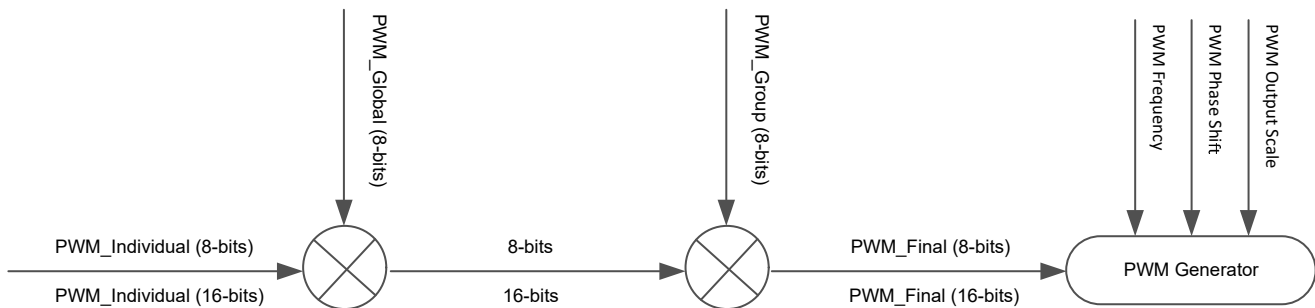
The LP5861T allows users to configure the dimming scale either exponentially (Gamma Correction) or linearly through the 'PWM\_Scale\_Mode' in Dev\_config1 register. If a human-eye-friendly dimming curve is desired, using the internal fixed exponential scale is an easy approach. If a special dimming curve is desired, using the linear scale with software correction is recommended. The LP5861T supports both linear and exponential dimming curves under 8-bit and 16-bit PWM depth. [Figure 8-2](#) is an example of 8-bit PWM depth.





8-2. Linear and Exponential Dimming Curves

In summary, the PWM control method is illustrated as 8-3:



8-3. PWM Control Scheme

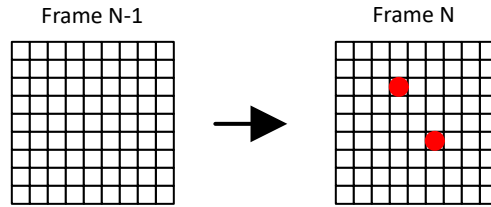
### 8.3.3 ON and OFF Control

The LP5861T device supports the individual ON and OFF control of each LED. For indication purpose, users can turn on and off the LED directly by writing 1-bit ON and OFF data to the corresponding Dot\_onoffx (x = 0, 1, ... , 2) register.

### 8.3.4 Data Refresh Mode

The LP5861T supports three data refresh modes: Mode 1, Mode 2, and Mode 3, by configuring 'Data\_Ref\_Mode' in Dev\_initial register.

**Mode 1:** 8-bit PWM data without VSYNC command. Data is sent out for display instantly after received. With Mode 1, users can refresh the corresponding dots' data only instead of updating the whole SRAM. It is called 'on demand data refresh', which can save the total data volume effectively. As shown in 8-4, the red LED dots can be refreshed after sending the corresponding data while the others kept the same with last frame.

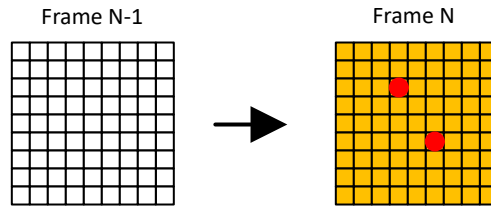


**图 8-4. On Demand Data Refresh – Mode 1**

**Mode 2:** 8-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

**Mode 3:** 16-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

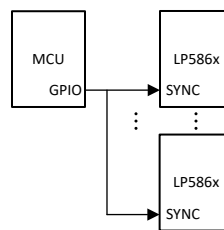
Frame control is implemented in Mode 2 and Mode 3. Instead of refreshing the output instantly after data is received (Mode 1), the device holds the data and refreshes the whole frame data by a fixed frame rate,  $f_{VSYNC}$ . Usually, 24 Hz, 50 Hz, 60 Hz, 120 Hz or even higher frame rate is selected to achieve vivid animation effects. Whole SRAM Data Refresh is shown in [图 8-5](#), a new frame is updated after receiving the VSYNC command.



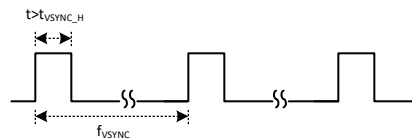
**图 8-5. Whole SRAM Data Refresh**

Comparing with Mode 1, Mode 2 and Mode 3 provide a better synchronization when multiple LP5861T devices used together. A high-level pulse width longer than  $t_{VSYNC\_H}$  is required at the beginning of each VSYNC frame.

[图 8-6](#) shows the VSYNC connections and [图 8-7](#) shows the timing requirements.



**图 8-6. Multiple Devices Sync**



**图 8-7. VSYNC Timing**

[Table 8-4](#) is the summary of the three data refresh modes.

**表 8-4. Data Refresh Mode**

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 1	8 bits	Data update instantly	No

表 8-4. Data Refresh Mode (continued)

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 2	8 bits	Data update by frame	Yes
Mode 3	16 bits		

### 8.3.5 Full Addressable SRAM

SRAM is implemented inside the LP5861T device to support data writing and reading at the same time.

Although data refresh mechanisms are not the same for Mode 1 and Mode 2 and 3, the data writing and reading follow the same method. Uses can update partial of the SRAM data only or the whole SRAM page simultaneously. The LP5861T supports auto-increment function to minimize data traffic and increase data transfer efficiency.

Please note that 16-bit PWM (Mode 3) and 8-bit PWM (Mode 1 and Mode 2) are assigned with different SRAM addresses.

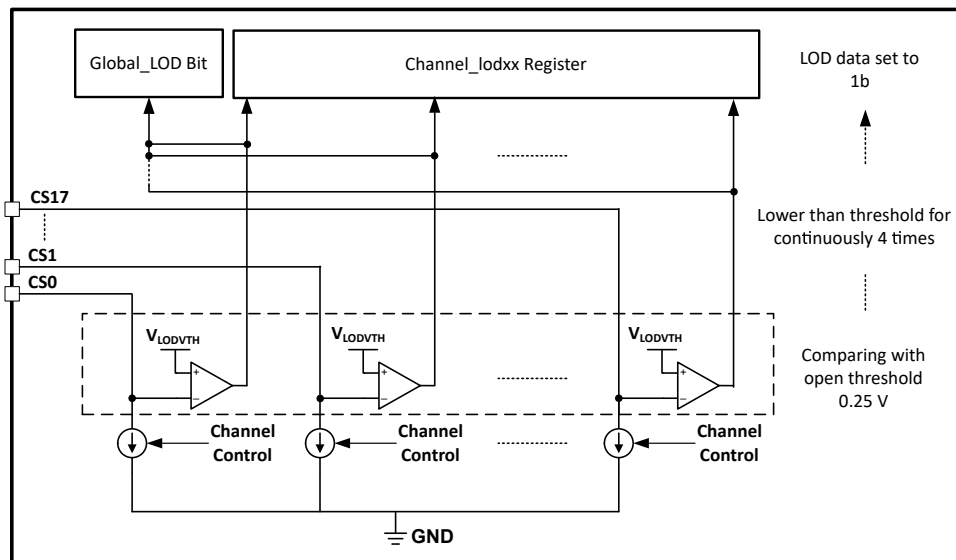
### 8.3.6 Protections and Diagnostics

#### LED Open Detection

The LP5861T includes LED open detection (LOD) for the fault caused by any opened LED dot. The threshold for LED open is 0.25-V typical. LED open detection is only performed when PWM ≥ 25 (Mode 1 and Mode 2) or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected lower than open threshold for continuously 4 sub-periods.

☒ 8-8 shows the detection circuit of LOD function. When open fault is detected, 'Global\_LOD' bit in Fault\_state register is set to 1 and detailed fault state for each LED is also monitored in register Dot\_lodxx (x = 0, 1, ... , 2). All open fault indicator bits can be cleared by setting LOD\_clear = 0Fh after the open condition is removed.

LOD removal function can be enabled by setting 'LOD\_removal' bit in Dev\_config2 register to 1. This function turns off the current sink of the open channel when scanning to the line where the opened LED is included.



☒ 8-8. LOD Circuits

#### LED Short Detection

The LP5861T includes LED short detection (LSD) for the fault caused by any shorted LED. Threshold for channel short is (VLED – 1) V typical. LED short detection only performed when PWM ≥ 25 (Mode 1 and Mode 2) or PWM ≥ 6400 (Mode 3) and voltage on CSn is detected higher than short threshold for continuously 4 sub-

periods. As there is parasitic capacitance for the current sink, to make sure the LSD result is correct, TI recommends to set the LED current higher than 0.5 mA.

Figure 8-9 shows the detection circuit of LSD function. When short fault is detected, 'Global\_LSD bit' in Fault\_state register is set to 1 and detailed fault state for every channel is also monitored in register Dot\_Isdx ( $x = 0, 1, \dots, 2$ ). All short fault indicator bits can be cleared by setting LSD\_clear = 0Fh after the short condition is removed.

LSD removal function can be enabled by setting 'LSD\_removal' bit in Dev\_config2 register to 1. This function turns off the upside deghosting function of the scan line where short LED is included.

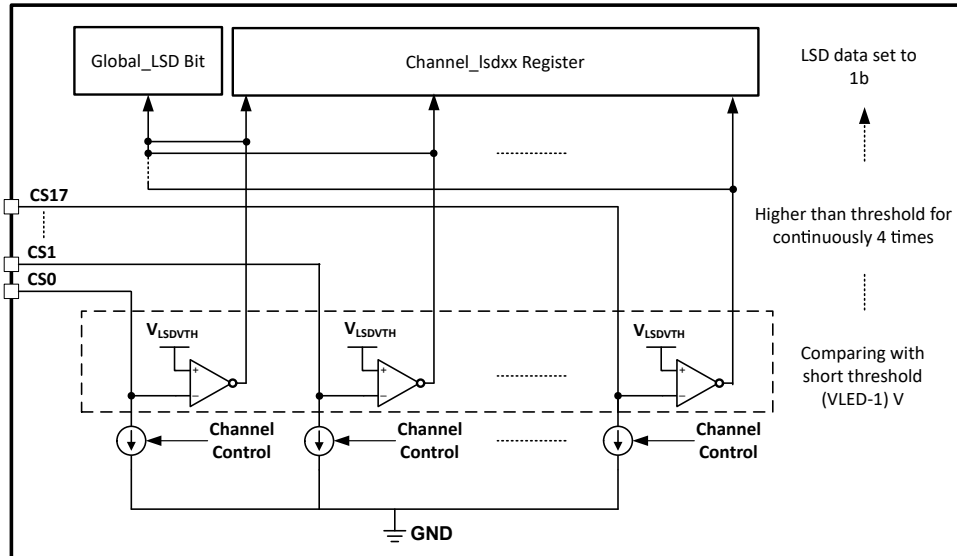


Figure 8-9. LSD Circuit

### Thermal Shutdown

The LP5861T device implements thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160 °C (typical) and above, the device switches into shutdown mode. The LP5861T exits thermal shutdown when the junction temperature of the device drops to 145 °C (typical) and below.

### UVLO (Undervoltage Lockout)

The LP5861T has an internal comparator that monitors the voltage at VCC. When VCC is below V<sub>UVF</sub>, reset is active and the LP5861T enters INITIALIZATION state.

## 8.4 Device Functional Modes

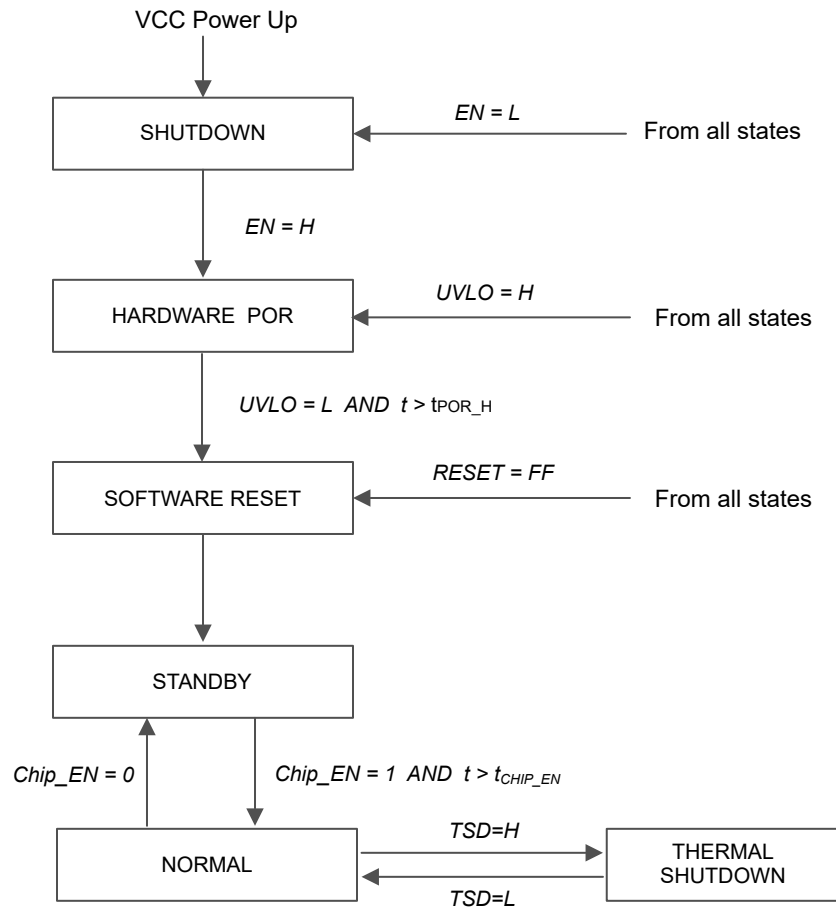


图 8-10. Device Functional Modes

- Shutdown: The device enters into shutdown mode from all states on VCC power up or EN pin is low.
- Hardware POR: The device enters into hardware POR when Enable pin is high or VCC fall under  $V_{UVF}$  causing  $UVLO = H$  from all states.
- Software reset: The device enters into software reset mode when VCC rise higher than  $V_{UVR}$  with the time  $t > t_{POR\_H}$ . In this mode, all the registers are reset. Entry can also be from any state when the RESET (register) = FFh or UVLO is low.
- Standby: The device enters the standby mode when Chip\_EN (register) = 0. In this mode, the device enters into low power mode, but the I<sup>2</sup>C/SPI are still available for Chip\_EN only and the registers' data are retained.
- Normal: The device enters the normal mode when 'Chip\_EN' = 1 with the time  $t > t_{CHIP\_EN}$ .
- Thermal shutdown: The device automatically enters the thermal shutdown mode when the junction temperature exceeds 160°C (typical). If the junction temperature decreases below 145°C (typical), the device returns to the normal mode.

## 8.5 Programming

### Interface Selection

The LP5861T supports two communication interfaces: I<sup>2</sup>C and SPI. If IFS is high, it enters into SPI mode. If IFS is low, it enters into I<sup>2</sup>C mode.

表 8-5. Interface Selection

INTERFACE TYPE	ENTRY CONDITION
I <sup>2</sup> C	IFS = Low

**表 8-5. Interface Selection (continued)**

INTERFACE TYPE	ENTRY CONDITION
SPI	IFS = High

**I<sup>2</sup>C Interface**

The LP5861T is compatible with I<sup>2</sup>C standard specification. The device supports both fast mode (400-KHz maximum) and fast plus mode (1-MHz maximum).

**I<sup>2</sup>C Data Transactions**

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

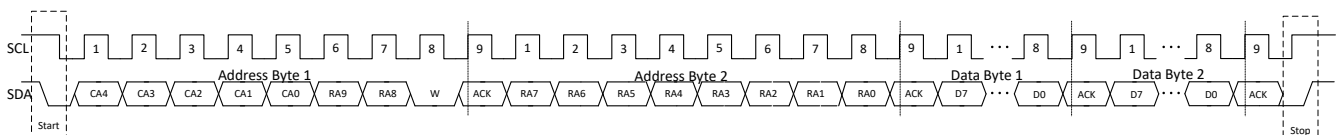
There is one exception to the acknowledge after every byte rule. When the leader is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

**I<sup>2</sup>C Data Format**

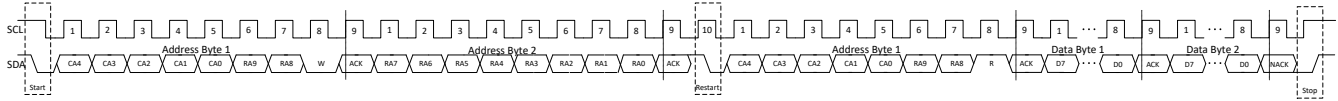
The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5-bits of the chip address, 2 higher bits of the register address, and 1 read and write bit. The other 8 lower bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

**表 8-6. I<sup>2</sup>C Data Format**

Address Byte1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	0	ADDR1	ADDR0	9 <sup>th</sup> bit	8 <sup>th</sup> bit	R: 1 W: 0
Broadcast	1	0	1	0	1			
Address Byte 2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit	1 <sup>th</sup> bit	0 <sup>th</sup> bit



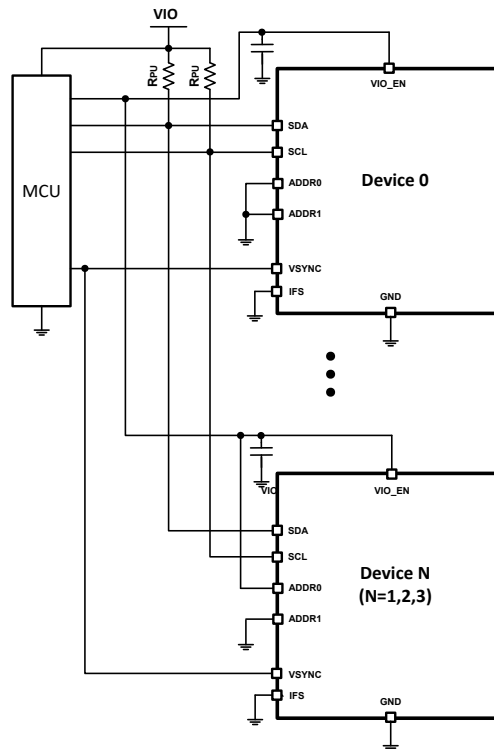
**图 8-11. I<sup>2</sup>C Write Timing**



**8-12. I<sup>2</sup>C Read Timing**

### Multiple Devices Connection

The LP5861T enters into I<sup>2</sup>C mode if IFS is connected to GND. The ADDR0/1 pin is used to select the unique I<sup>2</sup>C follower address for each device. The SCL and SDA lines must each have a pullup resistor (4.7 KΩ for 400 KHz, 2 KΩ for 1 MHz) placed somewhere on the line and remain HIGH even when the bus is idle. VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO\_EN pin as possible. Up to four LP5861T follower devices can share the same I<sup>2</sup>C bus by the different ADDR configurations.



**8-13. I<sup>2</sup>C Multiple Devices Connection**

### SPI Interface

The LP5861T is compatible with SPI serial-bus specification, and it operates as a follower. The maximum frequency supported by LP5861T is 12 MHz.

### SPI Data Transactions

MISO output is normally in a high impedance state. When the follower-select pin SS for the device is active (low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. The follower-select signal SS must be low during the cycle transmission. SS resets the interface when high. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

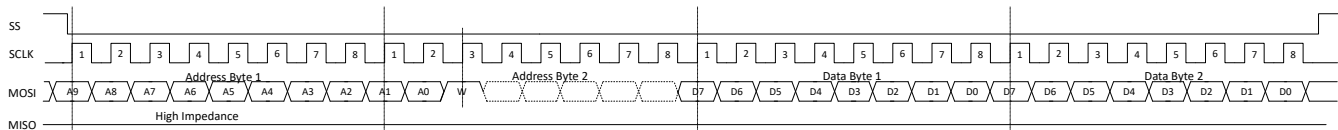
### SPI Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which contains 8 higher bits of the register address. The Address Byte 2 is started with 2 lower bits of the register address and 1 read and write bit. The auto-increment feature allows writing and

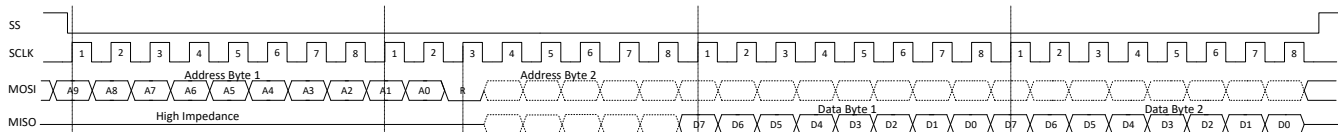
reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

**表 8-7. SPI Data Format**

Address Byte 1	Register Address								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
	9 <sup>th</sup> bit	8 <sup>th</sup> bit	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit	
Address Byte 2	Register Address								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
	1 <sup>th</sup> bit	0 <sup>th</sup> bit	R: 0 W: 1	Don't Care					



**图 8-14. SPI Write Timing**



**图 8-15. SPI Read Timing**

**Multiple Devices Connection**

The device enters into SPI mode if IFS is pulled high to VIO through a pullup resistor (4.7K Ω recommended). VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO\_EN pin as possible. In SPI mode host can address as many devices as there are follower select pins on host.



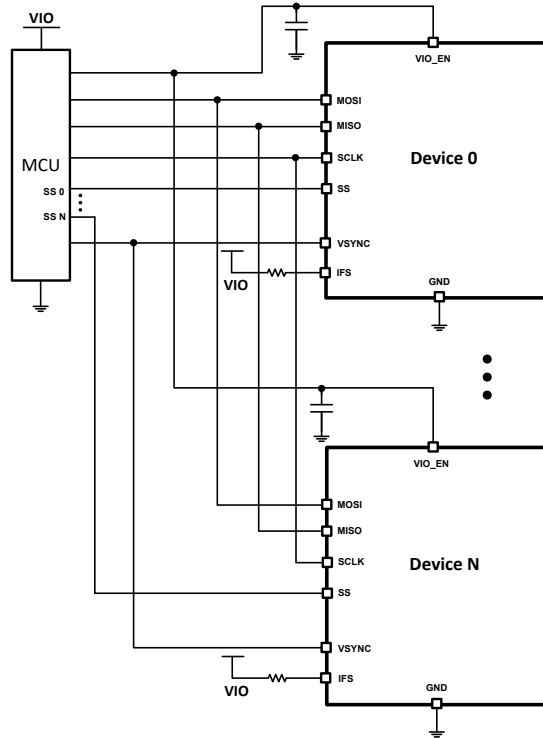


図 8-16. SPI Multiple Devices Connection

## 8.6 Register Maps

表 8-8 lists the memory-mapped registers of the device.

表 8-8. Register Section/Block Access Type Codes

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0
<b>Write Type</b>		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Chip_en	000h	R/W	Reserved								Chip_EN	00h
Dev_initial	001h	R/W	Reserved						Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved						PWM_Sc ale_Mode	PWM_Ph ase_Shift	Reserved	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		Reserved		00h	
Dev_config3	004h	R/W	Reserved				Maximum_Current			Reserved	47h	

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Register	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Global_bri	005h	R/W	PWM_Global									FFh
Group0_bri	006h	R/W	PWM_Group1									FFh
Group1_bri	007h	R/W	PWM_Group2									FFh
Group2_bri	008h	R/W	PWM_Group3									FFh
R_current_set	009h	R/W	Reserved	CC_Group1								40h
G_current_set	00Ah	R/W	Reserved	CC_Group2								40h
B_current_set	00Bh	R/W	Reserved	CC_Group3								40h
Dot_grp_sel0	00Ch	R/W	Dot CS3 group		Dot CS2 group		Dot CS1 group		Dot CS0 group		00h	
Dot_grp_sel1	00Dh	R/W	Dot CS7 group		Dot CS6 group		Dot CS5 group		Dot CS4 group		00h	
Dot_grp_sel2	00Eh	R/W	Dot CS11 group		Dot CS10 group		Dot CS9 group		Dot CS8 group		00h	
Dot_grp_sel3	00Fh	R/W	Dot CS15 group		Dot CS14 group		Dot CS13 group		Dot CS12 group		00h	
Dot_grp_sel4	010h	R/W	Reserved				Dot CS17 group		Dot CS16 group		00h	
Dot_onoff0	043h	R/W	Dot CS7 onoff	Dot CS6 onoff	Dot CS5 onoff	Dot CS4 onoff	Dot CS3 onoff	Dot CS2 onoff	Dot CS1 onoff	Dot CS0 onoff	FFh	
Dot_onoff1	044h	R/W	Dot CS15 onoff	Dot CS14 onoff	Dot CS13 onoff	Dot CS12 onoff	Dot CS11 onoff	Dot CS10 onoff	Dot CS9 onoff	Dot CS8 onoff	FFh	
Dot_onoff2	045h	R/W	Reserved						Dot CS17 onoff	Dot CS16 onoff	03h	
Fault_state	064h	R	Reserved						Global_L OD	Global_L SD	00h	
Dot_lod0	065h	R	Dot CS7 LOD	Dot CS6 LOD	Dot CS5 LOD	Dot CS4 LOD	Dot CS3 LOD	Dot CS2 LOD	Dot CS1 LOD	Dot CS0 LOD	00h	
Dot_lod1	066h	R	Dot CS15 LOD	Dot CS14 LOD	Dot CS13 LOD	Dot CS12 LOD	Dot CS11 LOD	Dot CS10 LOD	Dot CS9 LOD	Dot CS8 LOD	00h	
Dot_lod2	067h	R	Reserved						Dot CS17 LOD	Dot CS16 LOD	00h	
Dot_lsd0	086h	R	Dot CS7 LSD	Dot CS6 LSD	Dot CS5 LSD	Dot CS4 LSD	Dot CS3 LSD	Dot CS2 LSD	Dot CS1 LSD	Dot CS0 LSD	00h	
Dot_lsd1	087h	R	Dot CS15 LSD	Dot CS14 LSD	Dot CS13 LSD	Dot CS12 LSD	Dot CS11 LSD	Dot CS10 LSD	Dot CS9 LSD	Dot CS8 LSD	00h	
Dot_lsd2	088h	R	Reserved						Dot CS17 LSD	Dot CS16 LSD	00h	
LOD_clear	0A7h	W	Reserved				LOD_Clear				00h	
LSD_clear	0A8h	W	Reserved				LSD_Clear				00h	
Reset	0A9h	W	Reset									00h
DC0	100h	R/W	LED dot current setting for Dot CS0									80h
DC1	101h	R/W	LED dot current setting for Dot CS1									80h
DC2	102h	R/W	LED dot current setting for Dot CS2									80h
DC3	103h	R/W	LED dot current setting for Dot CS3									80h
DC4	104h	R/W	LED dot current setting for Dot CS4									80h
DC5	105h	R/W	LED dot current setting for Dot CS5									80h
DC6	106h	R/W	LED dot current setting for Dot CS6									80h
DC7	107h	R/W	LED dot current setting for Dot CS7									80h
DC8	108h	R/W	LED dot current setting for Dot CS8									80h
DC9	109h	R/W	LED dot current setting for Dot CS9									80h
DC10	10Ah	R/W	LED dot current setting for Dot CS10									80h
DC11	10Bh	R/W	LED dot current setting for Dot CS11									80h
DC12	10Ch	R/W	LED dot current setting for Dot CS12									80h
DC13	10Dh	R/W	LED dot current setting for Dot CS13									80h

Register	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
DC14	10Eh	R/W	LED dot current setting for Dot CS14								80h
DC15	10Fh	R/W	LED dot current setting for Dot CS15								80h
DC16	110h	R/W	LED dot current setting for Dot CS16								80h
DC17	111h	R/W	LED dot current setting for Dot CS17								80h
pwm_bri0	200h	R/W	8-bit PWM for Dot CS0 OR 16-bit PWM lower 8 bits [7:0] for Dot CS0								00h
pwm_bri1	201h	R/W	8-bit PWM for Dot CS1 OR 16-bit PWM higher 8 bits [15:8] for Dot CS0								00h
pwm_bri2	202h	R/W	8-bit PWM for Dot CS2 OR 16-bit PWM lower 8 bits [7:0] for Dot CS1								00h
pwm_bri3	203h	R/W	8-bit PWM for Dot CS3 OR 16-bit PWM higher 8 bits [15:8] for Dot CS1								00h
pwm_bri4	204h	R/W	8-bit PWM for Dot CS4 OR 16-bit PWM lower 8 bits [7:0] for Dot CS2								00h
pwm_bri5	205h	R/W	8-bit PWM for Dot CS5 OR 16-bit PWM higher 8 bits [15:8] for Dot CS2								00h
pwm_bri6	206h	R/W	8-bit PWM for Dot CS6 OR 16-bit PWM lower 8 bits [7:0] for Dot CS3								00h
pwm_bri7	207h	R/W	8-bit PWM for Dot CS7 OR 16-bit PWM higher 8 bits [15:8] for Dot CS3								00h
pwm_bri8	208h	R/W	8-bit PWM for Dot CS8 OR 16-bit PWM lower 8 bits [7:0] for Dot CS4								00h
pwm_bri9	209h	R/W	8-bit PWM for Dot CS9 OR 16-bit PWM higher 8 bits [15:8] for Dot CS4								00h
pwm_bri10	20Ah	R/W	8-bit PWM for Dot CS10 OR 16-bit PWM lower 8 bits [7:0] for Dot CS5								00h
pwm_bri11	20Bh	R/W	8-bit PWM for Dot CS11 OR 16-bit PWM higher 8 bits [15:8] for Dot CS5								00h
pwm_bri12	20Ch	R/W	8-bit PWM for Dot CS12 OR 16-bit PWM lower 8 bits [7:0] for Dot CS6								00h
pwm_bri13	20Dh	R/W	8-bit PWM for Dot CS13 OR 16-bit PWM higher 8 bits [15:8] for Dot CS6								00h
pwm_bri14	20Eh	R/W	8-bit PWM for Dot CS14 OR 16-bit PWM lower 8 bits [7:0] for Dot CS7								00h
pwm_bri15	20Fh	R/W	8-bit PWM for Dot CS15 OR 16-bit PWM higher 8 bits [15:8] for Dot CS7								00h
pwm_bri16	210h	R/W	8-bit PWM for Dot CS16 OR 16-bit PWM lower 8 bits [7:0] for Dot CS8								00h
pwm_bri17	211h	R/W	8-bit PWM for Dot CS17 OR 16-bit PWM higher 8 bits [15:8] for Dot CS8								00h
pwm_bri18	212h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS9								00h
pwm_bri19	213h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS9								00h
pwm_bri20	214h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS10								00h
pwm_bri21	215h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS10								00h
pwm_bri22	216h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS11								00h
pwm_bri23	217h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS11								00h
pwm_bri24	218h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS12								00h
pwm_bri25	219h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS12								00h
pwm_bri26	21Ah	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS13								00h
pwm_bri27	21Bh	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS13								00h
pwm_bri28	21Ch	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS14								00h
pwm_bri29	21Dh	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS14								00h
pwm_bri30	21Eh	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS15								00h
pwm_bri31	21Fh	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS15								00h
pwm_bri32	220h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS16								00h
pwm_bri33	221h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS16								00h
pwm_bri34	222h	R/W	16-bit PWM lower 8 bits [7:0] for Dot CS17								00h
pwm_bri35	223h	R/W	16-bit PWM higher 8 bits [15:8] for Dot CS17								00h

### 8.6.1 CONFIG Registers

表 8-9 lists the CONFIG registers. All register offset addresses not listed in 表 8-9 must be considered as reserved locations and the register contents must not be modified.

表 8-9. CONFIG Registers

Address	Acronym	Register Name	Section
0h	Chip_en	Chip enable	<a href="#">Go</a>
1h	Dev_initial	Device initialization	<a href="#">Go</a>
2h	Dev_config1	Device configuration register 1	<a href="#">Go</a>
3h	Dev_config2	Device configuration register 2	<a href="#">Go</a>
4h	Dev_config3	Device configuration register 3	<a href="#">Go</a>

### 8.6.1.1 Chip\_en Register (Address = 0h) [Default = 0h]

Chip\_en is shown in [図 8-17](#) and described in [表 8-10](#).

Return to the [Summary table](#).

图 8-17. Chip\_en Register

7	6	5	4	3	2	1	0
RESERVED							Chip_EN
R-0h							R/W-0h

表 8-10. Chip\_en Register Field Descriptions

Bit	Field	Type	Default	Description
7-1	RESERVED	R	0h	Reserved
0	Chip_EN	R/W	0h	Chip enable 0h = Disabled 1h = Enabled

### 8.6.1.2 Dev\_initial Register (Address = 1h) [Default = 5Eh]

Dev\_initial is shown in [図 8-18](#) and described in [表 8-11](#).

Return to the [Summary table](#).

图 8-18. Dev\_initial Register

7	6	5	4	3	2	1	0
RESERVED					Data_Ref_Mode	PWM_Fre	
R-Bh					R/W-3h	R/W-0h	

表 8-11. Dev\_initial Register Field Descriptions

Bit	Field	Type	Default	Description
7-3	RESERVED	R	Bh	Reserved
2-1	Data_Ref_Mode	R/W	3h	Data refresh mode selection 0h = Mode 1 1h = Mode 2 2h = Mode 3 3h = Mode 3
0	PWM_Fre	R/W	0h	Output PWM frequency setting 0h = 125kHz 1h = 62.5kHz

### 8.6.1.3 Dev\_config1 Register (Address = 2h) [Default = 0h]

Dev\_config1 is shown in [図 8-19](#) and described in [表 8-12](#).

Return to the [Summary table](#).

**8-19. Dev\_config1 Register**

7	6	5	4	3	2	1	0
RESERVED					PWM_Scale_Mode	PWM_Phase_Shift	RESERVED
R-0h					R/W-0h	R/W-0h	R-0h

**表 8-12. Dev\_config1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-3	RESERVED	R	0h	Reserved
2	PWM_Scale_Mode	R/W	0h	Dimming scale setting of final PWM generator 0h = Linear scale dimming curve 1h = Exponential scale dimming curve
1	PWM_Phase_Shift	R/W	0h	PWM phase shift selection 0h = Phase shift off 1h = Phase shift on
0	RESERVED	R	0h	Reserved

### 8.6.1.4 Dev\_config2 Register (Address = 3h) [Default = 0h]

Dev\_config2 is shown in [图 8-20](#) and described in [表 8-13](#).

Return to the [Summary table](#).

**图 8-20. Dev\_config2 Register**

7	6	5	4	3	2	1	0
Comp_Group3		Comp_Group2		Comp_Group1		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R-0h	

**表 8-13. Dev\_config2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	Comp_Group3	R/W	0h	Low brightness compensation clock shift number setting for group1 0h = off 1h = 1 clock 2h = 2 clock 3h = 3 clock
5-4	Comp_Group2	R/W	0h	Low brightness compensation clock shift number setting for group2 0h = off 1h = 1 clock 2h = 2 clock 3h = 3 clock
3-2	Comp_Group1	R/W	0h	Low brightness compensation clock shift number setting for group3 0h = off 1h = 1 clock 2h = 2 clock 3h = 3 clock
1-0	RESERVED	R	0h	Reserved

### 8.6.1.5 Dev\_config3 Register (Address = 4h) [Default = 57h]

Dev\_config3 is shown in [图 8-21](#) and described in [表 8-14](#).

Return to the [Summary table](#).

**图 8-21. Dev\_config3 Register**

7	6	5	4	3	2	1	0
RESERVED				Maximum_Current		RESERVED	
R-5h				R/W-3h		R-1h	

**表 8-14. Dev\_config3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-4	RESERVED	R	5h	Reserved
3-1	Maximum_Current	R/W	3h	Maximum current setting (MC) 0h = 7.5 mA 1h = 12.5 mA 2h = 25 mA 3h = 37.5 mA (Default) 4h = 50 mA 5h = 75 mA 6h = 100 mA 7h = 125 mA
0	RESERVED	R	1h	Reserved

## 8.6.2 GROUP Registers

表 8-15 lists the GROUP registers. All register offset addresses not listed in 表 8-15 must be considered as reserved locations and the register contents must not be modified.

**表 8-15. GROUP Registers**

Address	Acronym	Register Name	Section
5h	Master_bri	Global PWM configuration	<a href="#">Go</a>
6h	Group0_bri	Group1 PWM configuration	<a href="#">Go</a>
7h	Group1_bri	Group2 PWM configuration	<a href="#">Go</a>
8h	Group2_bri	Group3 PWM configuration	<a href="#">Go</a>
9h	R_current_set	Group1 current configuration	<a href="#">Go</a>
Ah	G_current_set	Group2 current configuration	<a href="#">Go</a>
Bh	B_current_set	Group3 current configuration	<a href="#">Go</a>

### 8.6.2.1 Master\_bri Register (Address = 5h) [Default = FFh]

Master\_bri is shown in 図 8-22 and described in 表 8-16.

Return to the [Summary Table](#).

**図 8-22. Master\_bri Register**

7	6	5	4	3	2	1	0
PWM_Global							
R/W-FFh							

**表 8-16. Master\_bri Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PWM_Global	R/W	FFh	Global PWM setting

### 8.6.2.2 Group0\_bri Register (Address = 6h) [Default = FFh]

Group0\_bri is shown in 図 8-23 and described in 表 8-17.

Return to the [Summary Table](#).

**図 8-23. Group0\_bri Register**

7	6	5	4	3	2	1	0
PWM_Group1							
R/W-FFh							

**表 8-17. Group0\_bri Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PWM_Group1	R/W	FFh	Group1 PWM setting

### 8.6.2.3 Group1\_bri Register (Address = 7h) [Default = FFh]

Group1\_bri is shown in 図 8-24 and described in 表 8-18.

Return to the [Summary Table](#).

**図 8-24. Group1\_bri Register**

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

### 图 8-24. Group1\_bri Register (continued)

PWM_Group2
R/W-FFh

**表 8-18. Group1\_bri Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PWM_Group2	R/W	FFh	Group2 PWM setting

#### 8.6.2.4 Group2\_bri Register (Address = 8h) [Default = FFh]

Group2\_bri is shown in 图 8-25 and described in 表 8-19.

Return to the [Summary Table](#).

### 图 8-25. Group2\_bri Register

7	6	5	4	3	2	1	0
PWM_Group3							
R/W-FFh							

**表 8-19. Group2\_bri Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	PWM_Group3	R/W	FFh	Group3 PWM setting

#### 8.6.2.5 R\_current\_set Register (Address = 9h) [Default = 40h]

R\_current\_set is shown in 图 8-26 and described in 表 8-20.

Return to the [Summary Table](#).

### 图 8-26. R\_current\_set Register

7	6	5	4	3	2	1	0
RESERVED							CC_Group1
R-0h							R/W-40h

**表 8-20. R\_current\_set Register Field Descriptions**

Bit	Field	Type	Default	Description
7	RESERVED	R	0h	Reserved
6-0	CC_Group1	R/W	40h	Color-group current setting (CC) of group 1 (CS0, CS3, CS6, CS9, CS12, CS15)

#### 8.6.2.6 G\_current\_set Register (Address = Ah) [Default = 40h]

G\_current\_set is shown in 图 8-27 and described in 表 8-21.

Return to the [Summary Table](#).

### 图 8-27. G\_current\_set Register

7	6	5	4	3	2	1	0
RESERVED							CC_Group2
R-0h							R/W-40h



表 8-21. G\_current\_set Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0h	Reserved
6-0	CC_Group2	R/W	40h	Color-group current setting (CC) of group 2 (CS1, CS4, CS7, CS10, CS13, CS16)

### 8.6.2.7 B\_current\_set Register (Address = Bh) [Default = 40h]

B\_current\_set is shown in 図 8-28 and described in 表 8-22.

Return to the [Summary Table](#).

図 8-28. B\_current\_set Register

7	6	5	4	3	2	1	0
RESERVED	CC_Group3						
R-0h	R/W-40h						

表 8-22. B\_current\_set Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0h	Reserved
6-0	CC_Group3	R/W	40h	Color-group current setting (CC) of group 3 (CS2, CS5, CS8, CS11, CS14, CS17)

### 8.6.3 DOTGROUP Registers

表 8-23 lists the DOTGROUP registers. All register offset addresses not listed in 表 8-23 must be considered as reserved locations and the register contents must not be modified.

表 8-23. DOTGROUP Registers

Address	Acronym	Register Name	Section
Ch	Dot_grp_sel0	LED dot group selection register 0	<a href="#">Go</a>
Dh	Dot_grp_sel1	LED dot group selection register 1	<a href="#">Go</a>
Eh	Dot_grp_sel2	LED dot group selection register 2	<a href="#">Go</a>
Fh	Dot_grp_sel3	LED dot group selection register 3	<a href="#">Go</a>
10h	Dot_grp_sel4	LED dot group selection register 4	<a href="#">Go</a>

#### 8.6.3.1 Dot\_grp\_sel0 Register (Address = Ch) [Default = 0h]

Dot\_grp\_sel0 is shown in 図 8-29 and described in 表 8-24.

Return to the [Summary Table](#).

図 8-29. Dot\_grp\_sel0 Register

7	6	5	4	3	2	1	0
CS3_group	CS2_group		CS1_group		CS0_group		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		

表 8-24. Dot\_grp\_sel0 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	CS3_group	R/W	0h	CS3 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
5-4	CS2_group	R/W	0h	CS2 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
3-2	CS1_group	R/W	0h	CS1 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
1-0	CS0_group	R/W	0h	CS0 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

### 8.6.3.2 Dot\_grp\_sel1 Register (Address = Dh) [Default = 0h]

Dot\_grp\_sel1 is shown in [图 8-30](#) and described in [表 8-25](#).

Return to the [Summary Table](#).

图 8-30. Dot\_grp\_sel1 Register

7	6	5	4	3	2	1	0
CS7_group		CS6_group		CS5_group		CS4_group	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 8-25. Dot\_grp\_sel1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	CS7_group	R/W	0h	CS7 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
5-4	CS6_group	R/W	0h	CS6 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
3-2	CS5_group	R/W	0h	CS5 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
1-0	CS4_group	R/W	0h	CS4 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

### 8.6.3.3 Dot\_grp\_sel2 Register (Address = Eh) [Default = 0h]

Dot\_grp\_sel2 is shown in [图 8-31](#) and described in [表 8-26](#).

Return to the [Summary Table](#).

**图 8-31. Dot\_grp\_sel2 Register**

7	6	5	4	3	2	1	0
CS11_group		CS10_group		CS9_group		CS8_group	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

**表 8-26. Dot\_grp\_sel2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	CS11_group	R/W	0h	CS11 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
5-4	CS10_group	R/W	0h	CS10 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
3-2	CS9_group	R/W	0h	CS9 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
1-0	CS8_group	R/W	0h	CS8 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

### 8.6.3.4 Dot\_grp\_sel3 Register (Address = Fh) [Default = 0h]

Dot\_grp\_sel3 is shown in [图 8-32](#) and described in [表 8-27](#).

Return to the [Summary Table](#).

**图 8-32. Dot\_grp\_sel3 Register**

7	6	5	4	3	2	1	0
CS15_group		CS14_group		CS13_group		CS12_group	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

**表 8-27. Dot\_grp\_sel3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-6	CS15_group	R/W	0h	CS15 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
5-4	CS14_group	R/W	0h	CS14 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

表 8-27. Dot\_grp\_sel3 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-2	CS13_group	R/W	0h	CS13 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
1-0	CS12_group	R/W	0h	CS12 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

### 8.6.3.5 Dot\_grp\_sel4 Register (Address = 10h) [Default = 0h]

Dot\_grp\_sel4 is shown in [図 8-33](#) and described in [表 8-28](#).

Return to the [Summary Table](#).

図 8-33. Dot\_grp\_sel4 Register

7	6	5	4	3	2	1	0
RESERVED				CS17_group		CS16_group	
R-0h				R/W-0h		R/W-0h	

表 8-28. Dot\_grp\_sel4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0h	Reserved
3-2	CS17_group	R/W	0h	CS17 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3
1-0	CS16_group	R/W	0h	CS16 group PWM control setting 0h = No group 1h = Group 1 2h = Group 2 3h = Group 3

### 8.6.4 DOTONOFF Registers

[表 8-29](#) lists the DOTONOFF registers. All register offset addresses not listed in [表 8-29](#) must be considered as reserved locations and the register contents must not be modified.

表 8-29. DOTONOFF Registers

Address	Acronym	Register Name	Section
43h	Dot_onoff0	LED dot ON/OFF selection register 0	<a href="#">Go</a>
44h	Dot_onoff1	LED dot ON/OFF selection register 1	<a href="#">Go</a>
45h	Dot_onoff2	LED dot ON/OFF selection register 2	<a href="#">Go</a>

#### 8.6.4.1 Dot\_onoff0 Register (Address = 43h) [Default = FFh]

Dot\_onoff0 is shown in [図 8-34](#) and described in [表 8-30](#).

Return to the [Summary Table](#).

**图 8-34. Dot\_onoff0 Register**

7	6	5	4	3	2	1	0
CS7_onoff	CS6_onoff	CS5_onoff	CS4_onoff	CS3_onoff	CS2_onoff	CS1_onoff	CS0_onoff
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

**表 8-30. Dot\_onoff0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS7_onoff	R/W	1h	LED CS7 on/off setting 0h = Off 1h = On
6	CS6_onoff	R/W	1h	LED CS6 on/off setting 0h = Off 1h = On
5	CS5_onoff	R/W	1h	LED CS5 on/off setting 0h = Off 1h = On
4	CS4_onoff	R/W	1h	LED CS4 on/off setting 0h = Off 1h = On
3	CS3_onoff	R/W	1h	LED CS3 on/off setting 0h = Off 1h = On
2	CS2_onoff	R/W	1h	LED CS2 on/off setting 0h = Off 1h = On
1	CS1_onoff	R/W	1h	LED CS1 on/off setting 0h = Off 1h = On
0	CS0_onoff	R/W	1h	LED CS0 on/off setting 0h = Off 1h = On

#### 8.6.4.2 Dot\_onoff1 Register (Address = 44h) [Default = FFh]

Dot\_onoff1 is shown in [图 8-35](#) and described in [表 8-31](#).

Return to the [Summary Table](#).

**图 8-35. Dot\_onoff1 Register**

7	6	5	4	3	2	1	0
CS15_onoff	CS14_onoff	CS13_onoff	CS12_onoff	CS11_onoff	CS10_onoff	CS1_onoff	CS0_onoff
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

**表 8-31. Dot\_onoff1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS15_onoff	R/W	1h	LED CS15 on/off setting 0h = Off 1h = On
6	CS14_onoff	R/W	1h	LED CS14 on/off setting 0h = Off 1h = On
5	CS13_onoff	R/W	1h	LED CS13 on/off setting 0h = Off 1h = On

表 8-31. Dot\_onoff1 Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4	CS12_onoff	R/W	1h	LED CS12 on/off setting 0h = Off 1h = On
3	CS11_onoff	R/W	1h	LED CS11 on/off setting 0h = Off 1h = On
2	CS10_onoff	R/W	1h	LED CS10 on/off setting 0h = Off 1h = On
1	CS1_onoff	R/W	1h	LED CS9 on/off setting 0h = Off 1h = On
0	CS0_onoff	R/W	1h	LED CS8 on/off setting 0h = Off 1h = On

### 8.6.4.3 Dot\_onoff2 Register (Address = 45h) [Default = 3h]

Dot\_onoff2 is shown in [图 8-36](#) and described in [表 8-32](#).

Return to the [Summary Table](#).

图 8-36. Dot\_onoff2 Register

7	6	5	4	3	2	1	0
RESERVED						CS17_onoff	CS16_onoff
R-0h						R/W-1h	R/W-1h

表 8-32. Dot\_onoff2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0h	Reserved
1	CS17_onoff	R/W	1h	LED CS17 on/off setting 0h = Off 1h = On
0	CS16_onoff	R/W	1h	LED CS16 on/off setting 0h = Off 1h = On

### 8.6.5 FAULT Registers

[表 8-33](#) lists the FAULT registers, including Fault\_state registers, LOD registers and LSD registers. All register offset addresses not listed in [表 8-33](#) must be considered as reserved locations and the register contents must not be modified.

表 8-33. FAULT Registers

Address	Acronym	Register Name	Section
64h	Fault_state	Global LOD/LSD indication register	<a href="#">Go</a>
65h	Dot_lod0	LED dot LOD indication register 0	<a href="#">Go</a>
66h	Dot_lod1	LED dot LOD indication register 1	<a href="#">Go</a>
67h	Dot_lod2	LED dot LOD indication register 2	<a href="#">Go</a>
86h	Dot_lsd0	LED dot LSD indication register 0	<a href="#">Go</a>
87h	Dot_lsd1	LED dot LSD indication register 1	<a href="#">Go</a>
88h	Dot_lsd2	LED dot LSD indication register 2	<a href="#">Go</a>

### 8.6.5.1 Fault\_state Register (Address = 64h) [Default = 0h]

Fault\_state is shown in [図 8-37](#) and described in [表 8-34](#).

Return to the [Summary Table](#).

**図 8-37. Fault\_state Register**

7	6	5	4	3	2	1	0
RESERVED						Global_LOD	Global_LSD
R-0h						R-0h	R-0h

**表 8-34. Fault\_state Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0h	Reserved
1	Global_LOD	R	0h	LOD indication bit if there is open fault detected at any LED dot 0h = Not open 1h = Open
0	Global_LSD	R	0h	LSD indication bit if there is short fault detected at any LED dot 0h = Not short 1h = Short

### 8.6.5.2 Dot\_lod0 Register (Address = 65h) [Default = 0h]

Dot\_lod0 is shown in [Figure 8-38](#) and described in [Table 8-35](#).

Return to the [Summary Table](#).

**Figure 8-38. Dot\_lod0 Register**

7	6	5	4	3	2	1	0
CS7_LOD_state	CS6_LOD_state	CS5_LOD_state	CS4_LOD_state	CS3_LOD_state	CS2_LOD_state	CS1_LOD_state	CS0_LOD_state
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

**Table 8-35. Dot\_lod0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS7_LOD_state	R	0h	CS7 LOD state 0h = Not open 1h = Open
6	CS6_LOD_state	R	0h	CS6 LOD state 0h = Not open 1h = Open
5	CS5_LOD_state	R	0h	CS5 LOD state 0h = Not open 1h = Open
4	CS4_LOD_state	R	0h	CS4 LOD state 0h = Not open 1h = Open
3	CS3_LOD_state	R	0h	CS3 LOD state 0h = Not open 1h = Open
2	CS2_LOD_state	R	0h	CS2 LOD state 0h = Not open 1h = Open
1	CS1_LOD_state	R	0h	CS1 LOD state 0h = Not open 1h = Open
0	CS0_LOD_state	R	0h	CS0 LOD state 0h = Not open 1h = Open

### 8.6.5.3 Dot\_lod1 Register (Address = 66h) [Default = 0h]

Dot\_lod1 is shown in [Figure 8-39](#) and described in [Table 8-36](#).

Return to the [Summary Table](#).

**Figure 8-39. Dot\_lod1 Register**

7	6	5	4	3	2	1	0
CS15_LOD_state	CS14_LOD_state	CS13_LOD_state	CS12_LOD_state	CS11_LOD_state	CS10_LOD_state	CS9_LOD_state	CS8_LOD_state
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

**Table 8-36. Dot\_lod1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS15_LOD_state	R	0h	CS15 LOD state 0h = Not open 1h = Open



**表 8-36. Dot\_lod1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	CS14_LOD_state	R	0h	CS14 LOD state 0h = Not open 1h = Open
5	CS13_LOD_state	R	0h	CS13 LOD state 0h = Not open 1h = Open
4	CS12_LOD_state	R	0h	CS12 LOD state 0h = Not open 1h = Open
3	CS11_LOD_state	R	0h	CS11 LOD state 0h = Not open 1h = Open
2	CS10_LOD_state	R	0h	CS10 LOD state 0h = Not open 1h = Open
1	CS9_LOD_state	R	0h	CS9 LOD state 0h = Not open 1h = Open
0	CS8_LOD_state	R	0h	CS8 LOD state 0h = Not open 1h = Open

#### 8.6.5.4 Dot\_lod2 Register (Address = 67h) [Default = 0h]

Dot\_lod2 is shown in [図 8-40](#) and described in [表 8-37](#).

Return to the [Summary Table](#).

**図 8-40. Dot\_lod2 Register**

7	6	5	4	3	2	1	0
RESERVED						CS17_LOD_state	CS16_LOD_state
R-0h						R-0h	R-0h

**表 8-37. Dot\_lod2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0h	Reserved
1	CS17_LOD_state	R	0h	CS17 LOD state 0h = Not open 1h = Open
0	CS16_LOD_state	R	0h	CS16 LOD state 0h = Not open 1h = Open

### 8.6.5.5 Dot\_Isd0 Register (Address = 86h) [Default = 0h]

Dot\_Isd0 is shown in [Figure 8-41](#) and described in [Table 8-38](#).

Return to the [Summary Table](#).

**Figure 8-41. Dot\_Isd0 Register**

7	6	5	4	3	2	1	0
CS7_LSD_state	CS6_LSD_state	CS5_LSD_state	CS4_LSD_state	CS3_LSD_state	CS2_LSD_state	CS1_LSD_state	CS0_LSD_state
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

**Table 8-38. Dot\_Isd0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS7_LSD_state	R	0h	CS7 LSD state 0h = Not short 1h = Short
6	CS6_LSD_state	R	0h	CS6 LSD state 0h = Not short 1h = Short
5	CS5_LSD_state	R	0h	CS5 LSD state 0h = Not short 1h = Short
4	CS4_LSD_state	R	0h	CS4 LSD state 0h = Not short 1h = Short
3	CS3_LSD_state	R	0h	CS3 LSD state 0h = Not short 1h = Short
2	CS2_LSD_state	R	0h	CS2 LSD state 0h = Not short 1h = Short
1	CS1_LSD_state	R	0h	CS1 LSD state 0h = Not short 1h = Short
0	CS0_LSD_state	R	0h	CS0 LSD state 0h = Not short 1h = Short

### 8.6.5.6 Dot\_Isd1 Register (Address = 87h) [Default = 0h]

Dot\_Isd1 is shown in [Figure 8-42](#) and described in [Table 8-39](#).

Return to the [Summary Table](#).

**Figure 8-42. Dot\_Isd1 Register**

7	6	5	4	3	2	1	0
CS15_LSD_state	CS14_LSD_state	CS13_LSD_state	CS12_LSD_state	CS11_LSD_state	CS10_LSD_state	CS9_LSD_state	CS8_LSD_state
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

**Table 8-39. Dot\_Isd1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7	CS15_LSD_state	R	0h	CS15 LSD state 0h = Not short 1h = Short

**表 8-39. Dot\_Isd1 Register Field Descriptions (continued)**

Bit	Field	Type	Default	Description
6	CS14_LSD_state	R	0h	CS14 LSD state 0h = Not short 1h = Short
5	CS13_LSD_state	R	0h	CS13 LSD state 0h = Not short 1h = Short
4	CS12_LSD_state	R	0h	CS12 LSD state 0h = Not short 1h = Short
3	CS11_LSD_state	R	0h	CS11 LSD state 0h = Not short 1h = Short
2	CS10_LSD_state	R	0h	CS10 LSD state 0h = Not short 1h = Short
1	CS9_LSD_state	R	0h	CS9 LSD state 0h = Not short 1h = Short
0	CS8_LSD_state	R	0h	CS8 LSD state 0h = Not short 1h = Short

### 8.6.5.7 Dot\_Isd2 Register (Address = 88h) [Default = 0h]

Dot\_Isd2 is shown in [図 8-43](#) and described in [表 8-40](#).

Return to the [Summary Table](#).

**図 8-43. Dot\_Isd2 Register**

7	6	5	4	3	2	1	0
RESERVED						CS17_LSD_state	CS16_LSD_state
R-0h						R-0h	R-0h

**表 8-40. Dot\_Isd2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-2	RESERVED	R	0h	Reserved
1	CS17_LSD_state	R	0h	CS17 LSD state 0h = Not short 1h = Short
0	CS16_LSD_state	R	0h	CS16 LSD state 0h = Not short 1h = Short

### 8.6.6 RESET Registers

[表 8-41](#) lists the RESET registers, including LOD\_CLR registers, LSD\_CLR registers and Reset registers. All register offset addresses not listed in [表 8-41](#) must be considered as reserved locations and the register contents must not be modified.

**表 8-41. RESET Registers**

Address	Acronym	Register Name	Section
A7h	LOD_clear	LOD flag clear register	<a href="#">Go</a>
A8h	LSD_clear	LSD flag clear register	<a href="#">Go</a>

表 8-41. RESET Registers (continued)

Address	Acronym	Register Name	Section
A9h	Reset	Software reset register	<a href="#">Go</a>

### 8.6.6.1 LOD\_clear Register (Address = A7h) [Default = 0h]

LOD\_clear is shown in [图 8-44](#) and described in [表 8-42](#).

Return to the [Summary Table](#).

图 8-44. LOD\_clear Register

7	6	5	4	3	2	1	0
RESERVED				LOD_Clear			
R-0h				W-0h			

表 8-42. LOD\_clear Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0h	Reserved
3-0	LOD_Clear	W	0h	Write Fh to clear all LOD indication bits

### 8.6.6.2 LSD\_clear Register (Address = A8h) [Default = 0h]

LSD\_clear is shown in [图 8-45](#) and described in [表 8-43](#).

Return to the [Summary Table](#).

图 8-45. LSD\_clear Register

7	6	5	4	3	2	1	0
RESERVED				LSD_Clear			
R-0h				W-0h			

表 8-43. LSD\_clear Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	RESERVED	R	0h	Reserved
3-0	LSD_Clear	W	0h	Write Fh to clear all LSD indication bits

### 8.6.6.3 Reset Register (Address = A9h) [Default = 0h]

Reset is shown in [图 8-46](#) and described in [表 8-44](#).

Return to the [Summary Table](#).

图 8-46. Reset Register

7	6	5	4	3	2	1	0
Reset							
W-0h							

表 8-44. Reset Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reset	W	0h	Write FFh to reset the device

### 8.6.7 DC Registers

表 8-45 lists the DC registers. All register offset addresses not listed in 表 8-45 must be considered as reserved locations and the register contents must not be modified.

**表 8-45. DC Registers**

Address	Acronym	Register Name	Section
100h	DC0	LED dot current setting for Dot L0-CS0	<a href="#">Go</a>
101h	DC1	LED dot current setting for Dot L0-CS1	<a href="#">Go</a>
102h	DC2	LED dot current setting for Dot L0-CS2	<a href="#">Go</a>
103h	DC3	LED dot current setting for Dot L0-CS3	<a href="#">Go</a>
104h	DC4	LED dot current setting for Dot L0-CS4	<a href="#">Go</a>
105h	DC5	LED dot current setting for Dot L0-CS5	<a href="#">Go</a>
106h	DC6	LED dot current setting for Dot L0-CS6	<a href="#">Go</a>
107h	DC7	LED dot current setting for Dot L0-CS7	<a href="#">Go</a>
108h	DC8	LED dot current setting for Dot L0-CS8	<a href="#">Go</a>
109h	DC9	LED dot current setting for Dot L0-CS9	<a href="#">Go</a>
10Ah	DC10	LED dot current setting for Dot L0-CS10	<a href="#">Go</a>
10Bh	DC11	LED dot current setting for Dot L0-CS11	<a href="#">Go</a>
10Ch	DC12	LED dot current setting for Dot L0-CS12	<a href="#">Go</a>
10Dh	DC13	LED dot current setting for Dot L0-CS13	<a href="#">Go</a>
10Eh	DC14	LED dot current setting for Dot L0-CS14	<a href="#">Go</a>
10Fh	DC15	LED dot current setting for Dot L0-CS15	<a href="#">Go</a>
110h	DC16	LED dot current setting for Dot L0-CS16	<a href="#">Go</a>
111h	DC17	LED dot current setting for Dot L0-CS17	<a href="#">Go</a>

### 8.6.7.1 DC0 Register (Address = 100h) [Default = 80h]

DC0 is shown in [图 8-47](#) and described in [表 8-46](#).

Return to the [Summary Table](#).

**图 8-47. DC0 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS0							
R/W-80h							

**表 8-46. DC0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS0	R/W	80h	8-bits constant current value for CS0

### 8.6.7.2 DC1 Register (Address = 101h) [Default = 80h]

DC1 is shown in [图 8-48](#) and described in [表 8-47](#).

Return to the [Summary Table](#).

**图 8-48. DC1 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS1							
R/W-80h							

**表 8-47. DC1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS1	R/W	80h	8-bits constant current value for CS1

### 8.6.7.3 DC2 Register (Address = 102h) [Default = 80h]

DC2 is shown in [图 8-49](#) and described in [表 8-48](#).

Return to the [Summary Table](#).

**图 8-49. DC2 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS2							
R/W-80h							

**表 8-48. DC2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS2	R/W	80h	8-bits constant current value for CS2

### 8.6.7.4 DC3 Register (Address = 103h) [Default = 80h]

DC3 is shown in [图 8-50](#) and described in [表 8-49](#).

Return to the [Summary Table](#).

**☒ 8-50. DC3 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS3							
R/W-80h							

**表 8-49. DC3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS3	R/W	80h	8-bits constant current value for CS3

#### 8.6.7.5 DC4 Register (Address = 104h) [Default = 80h]

DC4 is shown in [☒ 8-51](#) and described in [表 8-50](#).

Return to the [Summary Table](#).

**☒ 8-51. DC4 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS4							
R/W-80h							

**表 8-50. DC4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS4	R/W	80h	8-bits constant current value for CS4

#### 8.6.7.6 DC5 Register (Address = 105h) [Default = 80h]

DC5 is shown in [☒ 8-52](#) and described in [表 8-51](#).

Return to the [Summary Table](#).

**☒ 8-52. DC5 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS5							
R/W-80h							

**表 8-51. DC5 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS5	R/W	80h	8-bits constant current value for CS5

#### 8.6.7.7 DC6 Register (Address = 106h) [Default = 80h]

DC6 is shown in [☒ 8-53](#) and described in [表 8-52](#).

Return to the [Summary Table](#).

**☒ 8-53. DC6 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS6							
R/W-80h							

### ☒ 8-53. DC6 Register (continued)

#### 表 8-52. DC6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS6	R/W	80h	8-bits constant current value for CS6

#### 8.6.7.8 DC7 Register (Address = 107h) [Default = 80h]

DC7 is shown in ☒ 8-54 and described in 表 8-53.

Return to the [Summary Table](#).

#### ☒ 8-54. DC7 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS7							
R/W-80h							

#### 表 8-53. DC7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS7	R/W	80h	8-bits constant current value for CS7

#### 8.6.7.9 DC8 Register (Address = 108h) [Default = 80h]

DC8 is shown in ☒ 8-55 and described in 表 8-54.

Return to the [Summary Table](#).

#### ☒ 8-55. DC8 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS8							
R/W-80h							

#### 表 8-54. DC8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS8	R/W	80h	8-bits constant current value for CS8

#### 8.6.7.10 DC9 Register (Address = 109h) [Default = 80h]

DC9 is shown in ☒ 8-56 and described in 表 8-55.

Return to the [Summary Table](#).

#### ☒ 8-56. DC9 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS9							
R/W-80h							



表 8-55. DC9 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS9	R/W	80h	8-bits constant current value for CS9

#### 8.6.7.11 DC10 Register (Address = 10Ah) [Default = 80h]

DC10 is shown in [図 8-57](#) and described in [表 8-56](#).

Return to the [Summary Table](#).

図 8-57. DC10 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS10							
R/W-80h							

表 8-56. DC10 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS10	R/W	80h	8-bits constant current value for CS10

#### 8.6.7.12 DC11 Register (Address = 10Bh) [Default = 80h]

DC11 is shown in [図 8-58](#) and described in [表 8-57](#).

Return to the [Summary Table](#).

図 8-58. DC11 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS11							
R/W-80h							

表 8-57. DC11 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS11	R/W	80h	8-bits constant current value for CS11

#### 8.6.7.13 DC12 Register (Address = 10Ch) [Default = 80h]

DC12 is shown in [図 8-59](#) and described in [表 8-58](#).

Return to the [Summary Table](#).

図 8-59. DC12 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS12							
R/W-80h							

表 8-58. DC12 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS12	R/W	80h	8-bits constant current value for CS12

### 8.6.7.14 DC13 Register (Address = 10Dh) [Default = 80h]

DC13 is shown in [图 8-60](#) and described in [表 8-59](#).

Return to the [Summary Table](#).

**图 8-60. DC13 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS13							
R/W-80h							

**表 8-59. DC13 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS13	R/W	80h	8-bits constant current value for CS13

### 8.6.7.15 DC14 Register (Address = 10Eh) [Default = 80h]

DC14 is shown in [图 8-61](#) and described in [表 8-60](#).

Return to the [Summary Table](#).

**图 8-61. DC14 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS14							
R/W-80h							

**表 8-60. DC14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS14	R/W	80h	8-bits constant current value for CS14

### 8.6.7.16 DC15 Register (Address = 10Fh) [Default = 80h]

DC15 is shown in [图 8-62](#) and described in [表 8-61](#).

Return to the [Summary Table](#).

**图 8-62. DC15 Register**

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS15							
R/W-80h							

**表 8-61. DC15 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_f or_CS15	R/W	80h	8-bits constant current value for CS15

### 8.6.7.17 DC16 Register (Address = 110h) [Default = 80h]

DC16 is shown in [图 8-63](#) and described in [表 8-62](#).

Return to the [Summary Table](#).

☒ 8-63. DC16 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS16							
R/W-80h							

表 8-62. DC16 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_for_CS16	R/W	80h	8-bits constant current value for CS16

#### 8.6.7.18 DC17 Register (Address = 111h) [Default = 80h]

DC17 is shown in ☒ 8-64 and described in 表 8-63.

Return to the [Summary Table](#).

☒ 8-64. DC17 Register

7	6	5	4	3	2	1	0
LED_dot_current_setting_for_CS17							
R/W-80h							

表 8-63. DC17 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	LED_dot_current_setting_for_CS17	R/W	80h	8-bits constant current value for CS17

#### 8.6.8 PWM Registers

表 8-64 lists the PWM registers. All register offset addresses not listed in 表 8-64 must be considered as reserved locations and the register contents must not be modified.

表 8-64. PWM Registers

Address	Acronym	Register Name	Section
200h	pwm_bri0	8-bits PWM for CS0 OR 16-bits PWM lower 8 bits [7:0] for CS0	<a href="#">Go</a>
201h	pwm_bri1	8-bits PWM for CS1 OR 16-bits PWM higher 8 bits [15:8] for CS0	<a href="#">Go</a>
202h	pwm_bri2	8-bits PWM for CS2 OR 16-bits PWM lower 8 bits [7:0] for CS1	<a href="#">Go</a>
203h	pwm_bri3	8-bits PWM for CS3 OR 16-bits PWM higher 8 bits [15:8] for CS1	<a href="#">Go</a>
204h	pwm_bri4	8-bits PWM for CS4 OR 16-bits PWM lower 8 bits [7:0] for CS2	<a href="#">Go</a>
205h	pwm_bri5	8-bits PWM for CS5 OR 16-bits PWM higher 8 bits [15:8] for CS2	<a href="#">Go</a>
206h	pwm_bri6	8-bits PWM for CS6 OR 16-bits PWM lower 8 bits [7:0] for CS3	<a href="#">Go</a>
207h	pwm_bri7	8-bits PWM for CS7 OR 16-bits PWM higher 8 bits [15:8] for CS3	<a href="#">Go</a>
208h	pwm_bri8	8-bits PWM for CS8 OR 16-bits PWM lower 8 bits [7:0] for CS4	<a href="#">Go</a>
209h	pwm_bri9	8-bits PWM for CS9 OR 16-bits PWM higher 8 bits [15:8] for CS4	<a href="#">Go</a>

表 8-64. PWM Registers (continued)

Address	Acronym	Register Name	Section
20Ah	pwm_bri10	8-bits PWM for CS10 OR 16-bits PWM lower 8 bits [7:0] for CS5	<a href="#">Go</a>
20Bh	pwm_bri11	8-bits PWM for CS11 OR 16-bits PWM higher 8 bits [15:8] for CS5	<a href="#">Go</a>
20Ch	pwm_bri12	8-bits PWM for CS12 OR 16-bits PWM lower 8 bits [7:0] for CS6	<a href="#">Go</a>
20Dh	pwm_bri13	8-bits PWM for CS13 OR 16-bits PWM higher 8 bits [15:8] for CS6	<a href="#">Go</a>
20Eh	pwm_bri14	8-bits PWM for CS14 OR 16-bits PWM lower 8 bits [7:0] for CS7	<a href="#">Go</a>
20Fh	pwm_bri15	8-bits PWM for CS15 OR 16-bits PWM higher 8 bits [15:8] for CS7	<a href="#">Go</a>
210h	pwm_bri16	8-bits PWM for CS16 OR 16-bits PWM lower 8 bits [7:0] for CS8	<a href="#">Go</a>
211h	pwm_bri17	8-bits PWM for CS17 OR 16-bits PWM higher 8 bits [15:8] for CS8	<a href="#">Go</a>
212h	pwm_bri18	16-bits PWM lower 8 bits [7:0] for CS9	<a href="#">Go</a>
213h	pwm_bri19	16-bits PWM higher 8 bits [15:8] for CS9	<a href="#">Go</a>
214h	pwm_bri20	16-bits PWM lower 8 bits [7:0] for CS10	<a href="#">Go</a>
215h	pwm_bri21	16-bits PWM higher 8 bits [15:8] for CS10	<a href="#">Go</a>
216h	pwm_bri22	16-bits PWM lower 8 bits [7:0] for CS11	<a href="#">Go</a>
217h	pwm_bri23	16-bits PWM higher 8 bits [15:8] for CS11	<a href="#">Go</a>
218h	pwm_bri24	16-bits PWM lower 8 bits [7:0] for CS12	<a href="#">Go</a>
219h	pwm_bri25	16-bits PWM higher 8 bits [15:8] for CS12	<a href="#">Go</a>
21Ah	pwm_bri26	16-bits PWM lower 8 bits [7:0] for CS13	<a href="#">Go</a>
21Bh	pwm_bri27	16-bits PWM higher 8 bits [15:8] for CS13	<a href="#">Go</a>
21Ch	pwm_bri28	16-bits PWM lower 8 bits [7:0] for CS14	<a href="#">Go</a>
21Dh	pwm_bri29	16-bits PWM higher 8 bits [15:8] for CS14	<a href="#">Go</a>
21Eh	pwm_bri30	16-bits PWM lower 8 bits [7:0] for CS15	<a href="#">Go</a>
21Fh	pwm_bri31	16-bits PWM higher 8 bits [15:8] for CS15	<a href="#">Go</a>
220h	pwm_bri32	16-bits PWM lower 8 bits [7:0] for CS16	<a href="#">Go</a>
221h	pwm_bri33	16-bits PWM higher 8 bits [15:8] for CS16	<a href="#">Go</a>
222h	pwm_bri34	16-bits PWM lower 8 bits [7:0] for CS17	<a href="#">Go</a>
223h	pwm_bri35	16-bits PWM higher 8 bits [15:8] for CS17	<a href="#">Go</a>

### 8.6.8.1 pwm\_bri0 Register (Address = 200h) [Default = 0h]

pwm\_bri0 is shown in [図 8-65](#) and described in [表 8-65](#).

Return to the [Summary Table](#).

**図 8-65. pwm\_bri0 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS0_OR_16-bits_PWM_lower_8_bits_7:0_for_CS0							
R/W-0h							

**表 8-65. pwm\_bri0 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS0_OR_16-bits_PWM_lower_8_bits_7:0_for_CS0	R/W	0h	8-bits PWM for CS0 OR 16-bits PWM lower 8 bits [7:0] for CS0

### 8.6.8.2 pwm\_bri1 Register (Address = 201h) [Default = 0h]

pwm\_bri1 is shown in [図 8-66](#) and described in [表 8-66](#).

Return to the [Summary Table](#).

**図 8-66. pwm\_bri1 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS1_OR_16-bits_PWM_higher_8_bits_15:8_for_CS0							
R/W-0h							

**表 8-66. pwm\_bri1 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS1_OR_16-bits_PWM_higher_8_bits_15:8_for_CS0	R/W	0h	8-bits PWM for CS1 OR 16-bits PWM higher 8 bits [15:8] for CS0

### 8.6.8.3 pwm\_bri2 Register (Address = 202h) [Default = 0h]

pwm\_bri2 is shown in [図 8-67](#) and described in [表 8-67](#).

Return to the [Summary Table](#).

**図 8-67. pwm\_bri2 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS2_OR_16-bits_PWM_lower_8_bits_7:0_for_CS1							
R/W-0h							

**表 8-67. pwm\_bri2 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS2_OR_16-bits_PWM_lower_8_bits_7:0_for_CS1	R/W	0h	8-bits PWM for CS2 OR 16-bits PWM lower 8 bits [7:0] for CS1

**8.6.8.4 pwm\_bri3 Register (Address = 203h) [Default = 0h]**

pwm\_bri3 is shown in [図 8-68](#) and described in [表 8-68](#).

Return to the [Summary Table](#).

**図 8-68. pwm\_bri3 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS3_OR_16-bits_PWM_higher_8_bits_15:8_for_CS1							
R/W-0h							

**表 8-68. pwm\_bri3 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS3_OR_16-bits_PWM_higher_8_bits_15:8_for_CS1	R/W	0h	8-bits PWM for CS3 OR 16-bits PWM higher 8 bits [15:8] for CS1

**8.6.8.5 pwm\_bri4 Register (Address = 204h) [Default = 0h]**

pwm\_bri4 is shown in [図 8-69](#) and described in [表 8-69](#).

Return to the [Summary Table](#).

**図 8-69. pwm\_bri4 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS4_OR_16-bits_PWM_lower_8_bits_7:0_for_CS2							
R/W-0h							

**表 8-69. pwm\_bri4 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS4_OR_16-bits_PWM_lower_8_bits_7:0_for_CS2	R/W	0h	8-bits PWM for CS4 OR 16-bits PWM lower 8 bits [7:0] for CS2

**8.6.8.6 pwm\_bri5 Register (Address = 205h) [Default = 0h]**

pwm\_bri5 is shown in [図 8-70](#) and described in [表 8-70](#).

Return to the [Summary Table](#).

**図 8-70. pwm\_bri5 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS5_OR_16-bits_PWM_higher_8_bits_15:8_for_CS2							

☒ 8-70. pwm\_bri5 Register (continued)

R/W-0h

表 8-70. pwm\_bri5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8- bits_PWM_for_CS5_OR_ 16- bits_PWM_higher_8_bits_ _15:8__for_CS2	R/W	0h	8-bits PWM for CS5 OR 16-bits PWM higher 8 bits [15:8] for CS2

8.6.8.7 pwm\_bri6 Register (Address = 206h) [Default = 0h]

pwm\_bri6 is shown in ☒ 8-71 and described in 表 8-71.

Return to the [Summary Table](#).

☒ 8-71. pwm\_bri6 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS6_OR_16-bits_PWM_lower_8_bits__7:0__for_CS3							
R/W-0h							

表 8-71. pwm\_bri6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8- bits_PWM_for_CS6_OR_ 16- bits_PWM_lower_8_bits_ 7:0__for_CS3	R/W	0h	8-bits PWM for CS6 OR 16-bits PWM lower 8 bits [7:0] for CS3

8.6.8.8 pwm\_bri7 Register (Address = 207h) [Default = 0h]

pwm\_bri7 is shown in ☒ 8-72 and described in 表 8-72.

Return to the [Summary Table](#).

☒ 8-72. pwm\_bri7 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS7_OR_16-bits_PWM_higher_8_bits__15:8__for_CS3							
R/W-0h							


表 8-72. pwm\_bri7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8- bits_PWM_for_CS7_OR_ 16- bits_PWM_higher_8_bits_ _15:8__for_CS3	R/W	0h	8-bits PWM for CS7 OR 16-bits PWM higher 8 bits [15:8] for CS3

8.6.8.9 pwm\_bri8 Register (Address = 208h) [Default = 0h]

pwm\_bri8 is shown in ☒ 8-73 and described in 表 8-73.

Return to the [Summary Table](#).

 **8-73. pwm\_bri8 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS8_OR_16-bits_PWM_lower_8_bits_7:0_for_CS4							
R/W-0h							

**表 8-73. pwm\_bri8 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS8_OR_16-bits_PWM_lower_8_bits_7:0_for_CS4	R/W	0h	8-bits PWM for CS8 OR 16-bits PWM lower 8 bits [7:0] for CS4

**8.6.8.10 pwm\_bri9 Register (Address = 209h) [Default = 0h]**

pwm\_bri9 is shown in [图 8-74](#) and described in [表 8-74](#).

Return to the [Summary Table](#).

 **8-74. pwm\_bri9 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS9_OR_16-bits_PWM_higher_8_bits_15:8_for_CS4							
R/W-0h							


**表 8-74. pwm\_bri9 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS9_OR_16-bits_PWM_higher_8_bits_15:8_for_CS4	R/W	0h	8-bits PWM for CS9 OR 16-bits PWM higher 8 bits [15:8] for CS4

**8.6.8.11 pwm\_bri10 Register (Address = 20Ah) [Default = 0h]**

pwm\_bri10 is shown in [图 8-75](#) and described in [表 8-75](#).

Return to the [Summary Table](#).

 **8-75. pwm\_bri10 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS10_OR_16-bits_PWM_lower_8_bits_7:0_for_CS5							
R/W-0h							

**表 8-75. pwm\_bri10 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS10_OR_16-bits_PWM_lower_8_bits_7:0_for_CS5	R/W	0h	8-bits PWM for CS10 OR 16-bits PWM lower 8 bits [7:0] for CS5

**8.6.8.12 pwm\_bri11 Register (Address = 20Bh) [Default = 0h]**

pwm\_bri11 is shown in [图 8-76](#) and described in [表 8-76](#).



Return to the [Summary Table](#).

☒ 8-76. pwm\_bri11 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS11_OR_16-bits_PWM_higher_8_bits__15:8__for_CS5							
R/W-0h							

表 8-76. pwm\_bri11 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS11_OR_16-bits_PWM_higher_8_bits__15:8__for_CS5	R/W	0h	8-bits PWM for CS11 OR 16-bits PWM higher 8 bits [15:8] for CS5

#### 8.6.8.13 pwm\_bri12 Register (Address = 20Ch) [Default = 0h]

pwm\_bri12 is shown in ☒ 8-77 and described in 表 8-77.

Return to the [Summary Table](#).

☒ 8-77. pwm\_bri12 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS12_OR_16-bits_PWM_lower_8_bits__7:0__for_CS6							
R/W-0h							

表 8-77. pwm\_bri12 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS12_OR_16-bits_PWM_lower_8_bits__7:0__for_CS6	R/W	0h	8-bits PWM for CS12 OR 16-bits PWM lower 8 bits [7:0] for CS6

#### 8.6.8.14 pwm\_bri13 Register (Address = 20Dh) [Default = 0h]

pwm\_bri13 is shown in ☒ 8-78 and described in 表 8-78.

Return to the [Summary Table](#).

☒ 8-78. pwm\_bri13 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS13_OR_16-bits_PWM_higher_8_bits__15:8__for_CS6							
R/W-0h							

表 8-78. pwm\_bri13 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS13_OR_16-bits_PWM_higher_8_bits__15:8__for_CS6	R/W	0h	8-bits PWM for CS13 OR 16-bits PWM higher 8 bits [15:8] for CS6

### 8.6.8.15 pwm\_bri14 Register (Address = 20Eh) [Default = 0h]

pwm\_bri14 is shown in [图 8-79](#) and described in [表 8-79](#).

Return to the [Summary Table](#).

**图 8-79. pwm\_bri14 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS14_OR_16-bits_PWM_lower_8_bits__7:0__for_CS7							
R/W-0h							

**表 8-79. pwm\_bri14 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS14_OR_16-bits_PWM_lower_8_bits__7:0__for_CS7	R/W	0h	8-bits PWM for CS14 OR 16-bits PWM lower 8 bits [7:0] for CS7

### 8.6.8.16 pwm\_bri15 Register (Address = 20Fh) [Default = 0h]

pwm\_bri15 is shown in [图 8-80](#) and described in [表 8-80](#).

Return to the [Summary Table](#).

**图 8-80. pwm\_bri15 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS15_OR_16-bits_PWM_higher_8_bits__15:8__for_CS7							
R/W-0h							

**表 8-80. pwm\_bri15 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	8-bits_PWM_for_CS15_OR_16-bits_PWM_higher_8_bits__15:8__for_CS7	R/W	0h	8-bits PWM for CS15 OR 16-bits PWM higher 8 bits [15:8] for CS7

### 8.6.8.17 pwm\_bri16 Register (Address = 210h) [Default = 0h]

pwm\_bri16 is shown in [图 8-81](#) and described in [表 8-81](#).

Return to the [Summary Table](#).

**图 8-81. pwm\_bri16 Register**

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS16_OR_16-bits_PWM_lower_8_bits__7:0__for_CS8							
R/W-0h							

表 8-81. pwm\_bri16 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8- bits_PWM_for_CS16_OR _16- bits_PWM_lower_8_bits__ 7:0__for_CS8	R/W	0h	8-bits PWM for CS16 OR 16-bits PWM lower 8 bits [7:0] for CS8

#### 8.6.8.18 pwm\_bri17 Register (Address = 211h) [Default = 0h]

pwm\_bri17 is shown in [図 8-82](#) and described in [表 8-82](#).

Return to the [Summary Table](#).

図 8-82. pwm\_bri17 Register

7	6	5	4	3	2	1	0
8-bits_PWM_for_CS17_OR_16-bits_PWM_higher_8_bits__15:8__for_CS8							
R/W-0h							

表 8-82. pwm\_bri17 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	8- bits_PWM_for_CS17_OR _16- bits_PWM_higher_8_bits__ _15:8__for_CS8	R/W	0h	8-bits PWM for CS17 OR 16-bits PWM higher 8 bits [15:8] for CS8

#### 8.6.8.19 pwm\_bri18 Register (Address = 212h) [Default = 0h]

pwm\_bri18 is shown in [図 8-83](#) and described in [表 8-83](#).

Return to the [Summary Table](#).

図 8-83. pwm\_bri18 Register

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS9							
R/W-0h							

表 8-83. pwm\_bri18 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits__ 7:0__for_CS9	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS9

#### 8.6.8.20 pwm\_bri19 Register (Address = 213h) [Default = 0h]

pwm\_bri19 is shown in [図 8-84](#) and described in [表 8-84](#).

Return to the [Summary Table](#).

図 8-84. pwm\_bri19 Register

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits__15:8__for_CS9							
R/W-0h							

### ☒ 8-84. pwm\_bri19 Register (continued)

#### 表 8-84. pwm\_bri19 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	16-bits_PWM_higher_8_bits__15:8__for_CS9	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS9

#### 8.6.8.21 pwm\_bri20 Register (Address = 214h) [Default = 0h]

pwm\_bri20 is shown in ☒ 8-85 and described in 表 8-85.

Return to the [Summary Table](#).

#### ☒ 8-85. pwm\_bri20 Register

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS10							
R/W-0h							

#### 表 8-85. pwm\_bri20 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	16-bits_PWM_lower_8_bits__7:0__for_CS10	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS10

#### 8.6.8.22 pwm\_bri21 Register (Address = 215h) [Default = 0h]

pwm\_bri21 is shown in ☒ 8-86 and described in 表 8-86.

Return to the [Summary Table](#).

#### ☒ 8-86. pwm\_bri21 Register

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits__15:8__for_CS10							
R/W-0h							

#### 表 8-86. pwm\_bri21 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	16-bits_PWM_higher_8_bits__15:8__for_CS10	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS10

#### 8.6.8.23 pwm\_bri22 Register (Address = 216h) [Default = 0h]

pwm\_bri22 is shown in ☒ 8-87 and described in 表 8-87.

Return to the [Summary Table](#).

#### ☒ 8-87. pwm\_bri22 Register

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS11							
R/W-0h							

**表 8-87. pwm\_bri22 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits_ 7:0_for_CS11	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS11

#### 8.6.8.24 pwm\_bri23 Register (Address = 217h) [Default = 0h]

pwm\_bri23 is shown in [図 8-88](#) and described in [表 8-88](#).

Return to the [Summary Table](#).

**図 8-88. pwm\_bri23 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits_15:8_for_CS11							
R/W-0h							

**表 8-88. pwm\_bri23 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ 15:8_for_CS11	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS11

#### 8.6.8.25 pwm\_bri24 Register (Address = 218h) [Default = 0h]

pwm\_bri24 is shown in [図 8-89](#) and described in [表 8-89](#).

Return to the [Summary Table](#).

**図 8-89. pwm\_bri24 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits_7:0_for_CS12							
R/W-0h							

**表 8-89. pwm\_bri24 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits_ 7:0_for_CS12	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS12

#### 8.6.8.26 pwm\_bri25 Register (Address = 219h) [Default = 0h]

pwm\_bri25 is shown in [図 8-90](#) and described in [表 8-90](#).

Return to the [Summary Table](#).

**図 8-90. pwm\_bri25 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits_15:8_for_CS12							
R/W-0h							

**表 8-90. pwm\_bri25 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ _15:8__for_CS12	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS12

**8.6.8.27 pwm\_bri26 Register (Address = 21Ah) [Default = 0h]**

 pwm\_bri26 is shown in [図 8-91](#) and described in [表 8-91](#).

 Return to the [Summary Table](#).

**図 8-91. pwm\_bri26 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS13							
R/W-0h							

**表 8-91. pwm\_bri26 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits__ 7:0__for_CS13	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS13

**8.6.8.28 pwm\_bri27 Register (Address = 21Bh) [Default = 0h]**

 pwm\_bri27 is shown in [図 8-92](#) and described in [表 8-92](#).

 Return to the [Summary Table](#).

**図 8-92. pwm\_bri27 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits__15:8__for_CS13							
R/W-0h							

**表 8-92. pwm\_bri27 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ _15:8__for_CS13	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS13

**8.6.8.29 pwm\_bri28 Register (Address = 21Ch) [Default = 0h]**

 pwm\_bri28 is shown in [図 8-93](#) and described in [表 8-93](#).

 Return to the [Summary Table](#).

**図 8-93. pwm\_bri28 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS14							
R/W-0h							

**表 8-93. pwm\_bri28 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits_ 7:0_for_CS14	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS14

### 8.6.8.30 pwm\_bri29 Register (Address = 21Dh) [Default = 0h]

pwm\_bri29 is shown in [図 8-94](#) and described in [表 8-94](#).

Return to the [Summary Table](#).

**図 8-94. pwm\_bri29 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits_15:8_for_CS14							
R/W-0h							

**表 8-94. pwm\_bri29 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ 15:8_for_CS14	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS14

### 8.6.8.31 pwm\_bri30 Register (Address = 21Eh) [Default = 0h]

pwm\_bri30 is shown in [図 8-95](#) and described in [表 8-95](#).

Return to the [Summary Table](#).

**図 8-95. pwm\_bri30 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits_7:0_for_CS15							
R/W-0h							

**表 8-95. pwm\_bri30 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits_ 7:0_for_CS15	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS15

### 8.6.8.32 pwm\_bri31 Register (Address = 21Fh) [Default = 0h]

pwm\_bri31 is shown in [図 8-96](#) and described in [表 8-96](#).

Return to the [Summary Table](#).

**図 8-96. pwm\_bri31 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits_15:8_for_CS15							
R/W-0h							

**表 8-96. pwm\_bri31 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ _15:8__for_CS15	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS15

**8.6.8.33 pwm\_bri32 Register (Address = 220h) [Default = 0h]**

pwm\_bri32 is shown in [図 8-97](#) and described in [表 8-97](#).

Return to the [Summary Table](#).

**図 8-97. pwm\_bri32 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS16							
R/W-0h							

**表 8-97. pwm\_bri32 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits__ 7:0__for_CS16	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS16

**8.6.8.34 pwm\_bri33 Register (Address = 221h) [Default = 0h]**

pwm\_bri33 is shown in [図 8-98](#) and described in [表 8-98](#).

Return to the [Summary Table](#).

**図 8-98. pwm\_bri33 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits__15:8__for_CS16							
R/W-0h							

**表 8-98. pwm\_bri33 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ _15:8__for_CS16	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS16

**8.6.8.35 pwm\_bri34 Register (Address = 222h) [Default = 0h]**

pwm\_bri34 is shown in [図 8-99](#) and described in [表 8-99](#).

Return to the [Summary Table](#).

**図 8-99. pwm\_bri34 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_lower_8_bits__7:0__for_CS17							
R/W-0h							



**表 8-99. pwm\_bri34 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_lower_8_bits_ 7:0_for_CS17	R/W	0h	16-bits PWM lower 8 bits [7:0] for CS17

**8.6.8.36 pwm\_bri35 Register (Address = 223h) [Default = 0h]**

pwm\_bri35 is shown in [図 8-100](#) and described in [表 8-100](#).

Return to the [Summary Table](#).

**図 8-100. pwm\_bri35 Register**

7	6	5	4	3	2	1	0
16-bits_PWM_higher_8_bits_15:8_for_CS17							
R/W-0h							

**表 8-100. pwm\_bri35 Register Field Descriptions**

Bit	Field	Type	Default	Description
7-0	16- bits_PWM_higher_8_bits_ _15:8_for_CS17	R/W	0h	16-bits PWM higher 8 bits [15:8] for CS17

## 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The LP5861T integrates 18 high-power constant current sinks, which can drive up to 18 LED dots or 6 RGB pixels and achieve great dimming effect. In smart home, gaming keyboards, and other human-machine interaction applications, the device can greatly improve user experience with a small amount of components.

### 9.2 Typical Application

#### 9.2.1 Application

图 9-1 shows an example of typical application, which uses one LP5861T to drive 6 common-anode RGB LEDs through I<sup>2</sup>C communication.

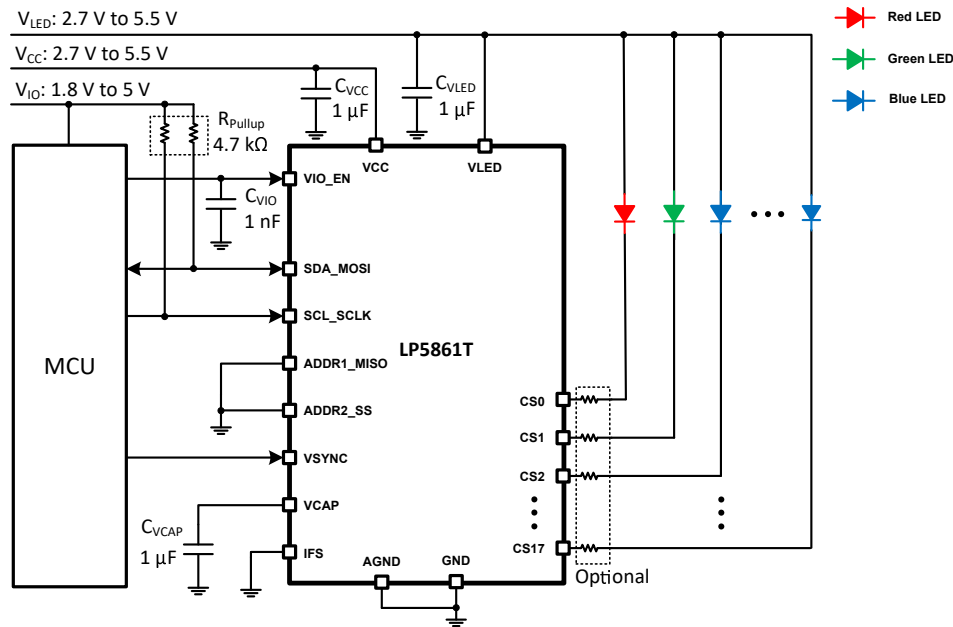


图 9-1. Typical Application - LP5861T Driving 6 RGB LEDs

#### 9.2.2 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
VCC / VIO	3.3 V
VLED	5 V
RGB LED count	6
Interface	I <sup>2</sup> C
LED maximum peak current (red, green, blue)	100 mA, 100 mA, 100 mA

### 9.2.3 Detailed Design Procedure

LP5861T requires an external capacitor  $C_{V_{CAP}}$ , whose value is  $1\ \mu\text{F}$  connected from  $V_{CAP}$  to GND for proper operation of internal LDO. The external capacitor must be placed as close to the device as possible.

TI recommends  $1\text{-}\mu\text{F}$  capacitors to be placed between VCC / VLED with GND, and  $1\text{-nF}$  capacitor placed between VIO with GND. Place the capacitors as close to the device as possible.

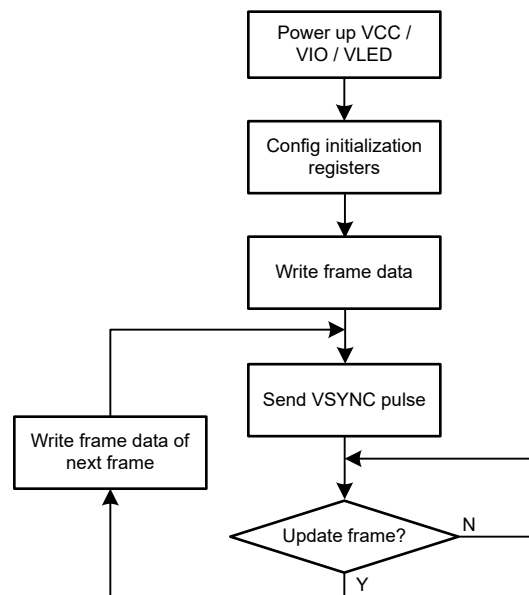
Pullup resistors  $R_{\text{pull-up}}$  are requirement for SCL and SDA when using I<sup>2</sup>C as communication method. In typical applications, TI recommends  $1.8\text{-k}\Omega$  to  $4.7\text{-k}\Omega$  resistors.

To decrease thermal dissipation from device to ambient, resistors  $R_{CS}$  an optionally be placed in serial with the LED. Voltage drop on these resistors must leave enough margins for VSAT to ensure the device work normally.

#### 9.2.3.1 Program Procedure

When selecting data refresh Mode 1, outputs are refreshed instantly after data is received.

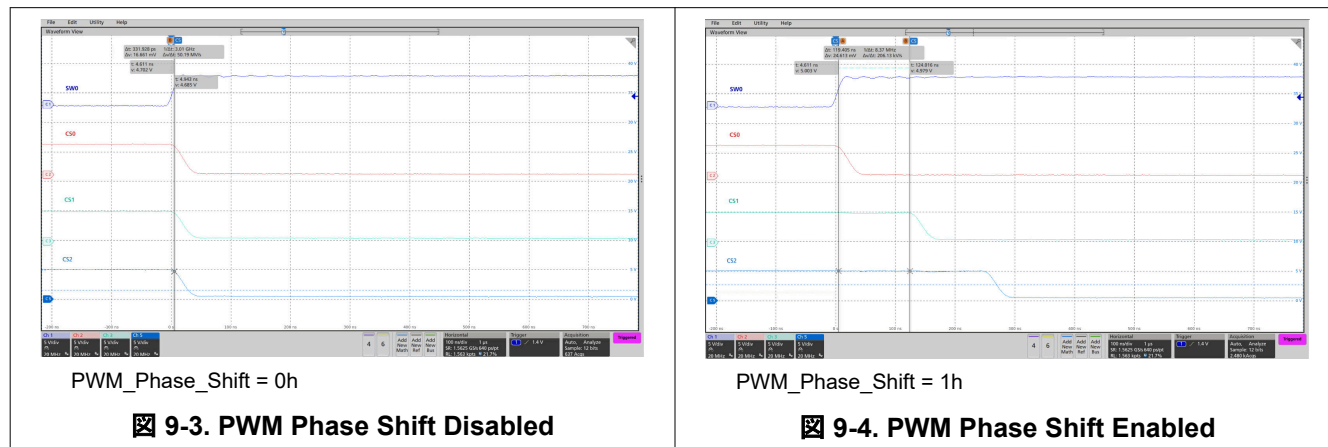
When selecting data refresh Mode 2 and 3, VSYNC signal is required for synchronized display. Programming flow is showed as [9-2](#). To display full pixel of last frame, VSYNC pulse must be sent to the device after the end of last PWM. Time between two pulses  $t_{\text{VSYNC}}$  must be larger than the whole PWM time of all Dots  $t_{\text{frame}}$ . Common selection like 60 Hz, 90 Hz, 120 Hz or even higher refresh frequency can be supported. High pulse width longer than  $t_{\text{VSYNC\_H}}$  is required at the beginning of each VSYNC frame, and data must not be write to PWM registers during high pulse width.



**9-2. Program Procedure**

## 9.2.4 Application Performance Plots

The following figures show the application performance plots.



## 9.3 Power Supply Recommendations

### VDD Input Supply Recommendations

LP5861T is designed to operate from a 2.7-V to 5.5-V VDD voltage supply. This input supply must be well regulated and be able to provide the peak current required by the LED matrix. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LP5861T VDD supply voltage to drop below the maximum POR voltage.

### VLED Input Supply Recommendations

LP5861T is designed to operate with a 2.7-V to 5.5-V VLED voltage supply. The VLED supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop, under load transients like start-up or rapid brightness change. The resistance of the input supply rail must be low enough so that the input current transient does not cause the VLED supply voltage to drop below LED  $V_f + V_{SAT}$  voltage.

### VIO Input Supply Recommendations

LP5861T is designed to operate with a 1.65-V to 5.5-V VIO\_EN voltage supply. The VIO\_EN supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients like start-up or rapid brightness change.

## 9.4 Layout

### 9.4.1 Layout Guidelines

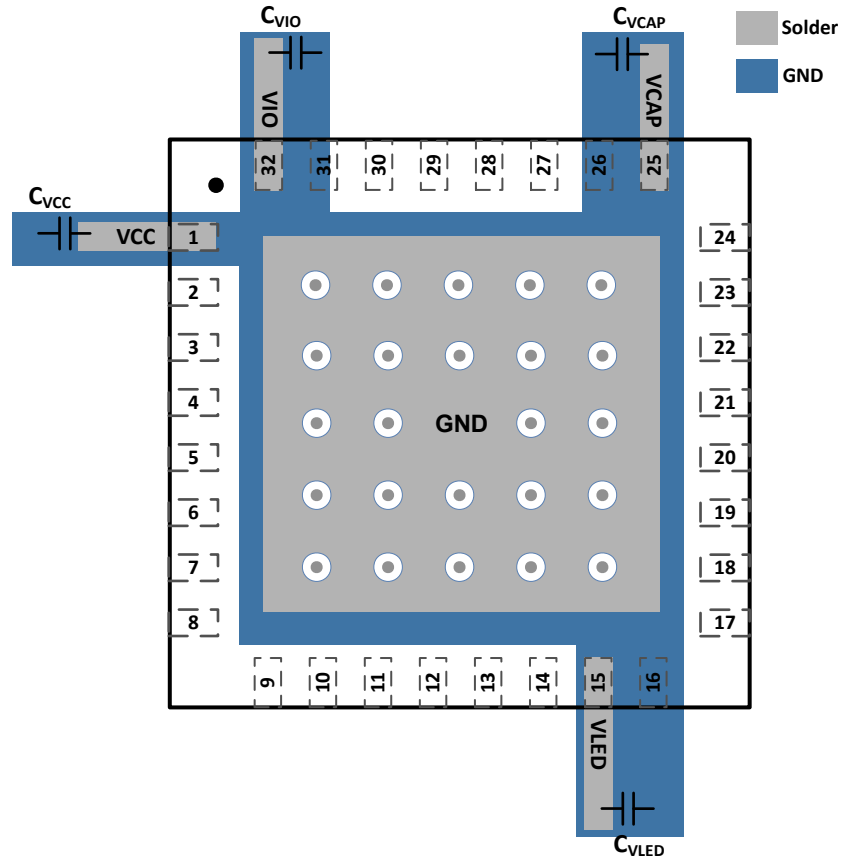
The below guidelines for layout design can help to get a better on-board performance.

- The decoupling capacitors  $C_{VCC}$  and  $C_{VLED}$  for power supply must be close to the chip to have minimized the impact of high-frequency noise and ripple from power.  $C_{VCAP}$  for internal LDO must be put as close to chip as possible. GND plane connections to  $C_{VLED}$  and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane.  $C_{VIO}$  for internal enable block also must be put as close to chip as possible.
- The exposed thermal pad must be well soldered to the board, which can have better mechanical reliability. This action can optimize heat transfer so that increasing thermal performance. AGND pin must be connected to thermal pad and system ground.
- The major heat flow path from the package to the ambient is through copper on the PCB. Several methods can help thermal performance. Below exposed thermal pad of IC, putting much vias through the PCB to other

ground layer can dissipate more heat. Maximizing the copper coverage on the PCB can increase the thermal conductivity of the board.

- Low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of VLED – SWx must be short and wide and avoid parallel wiring and narrow trace. Transient current in SWx pins is much larger than CSy pins, so that trace for SWx must be wider than CSy.

### 9.4.2 Layout Example



9-5. LP5861T Layout Example

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](https://www.ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 10.3 Trademarks

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### 10.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5861TMRSR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	5861TM	<a href="#">Samples</a>
LP5861TRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LP5861T	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





## GENERIC PACKAGE VIEW

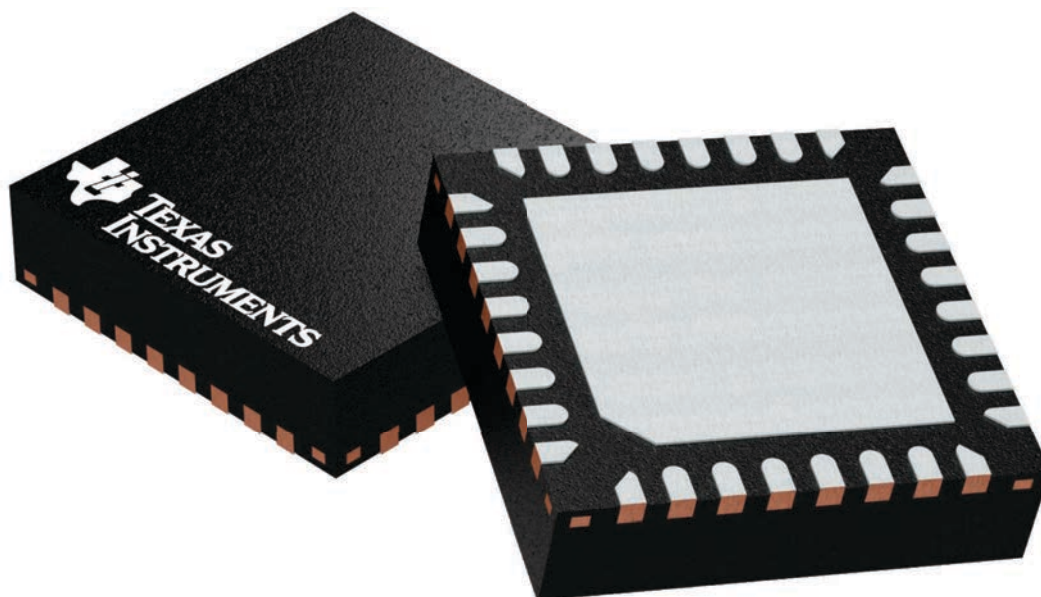
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

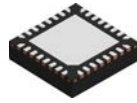
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

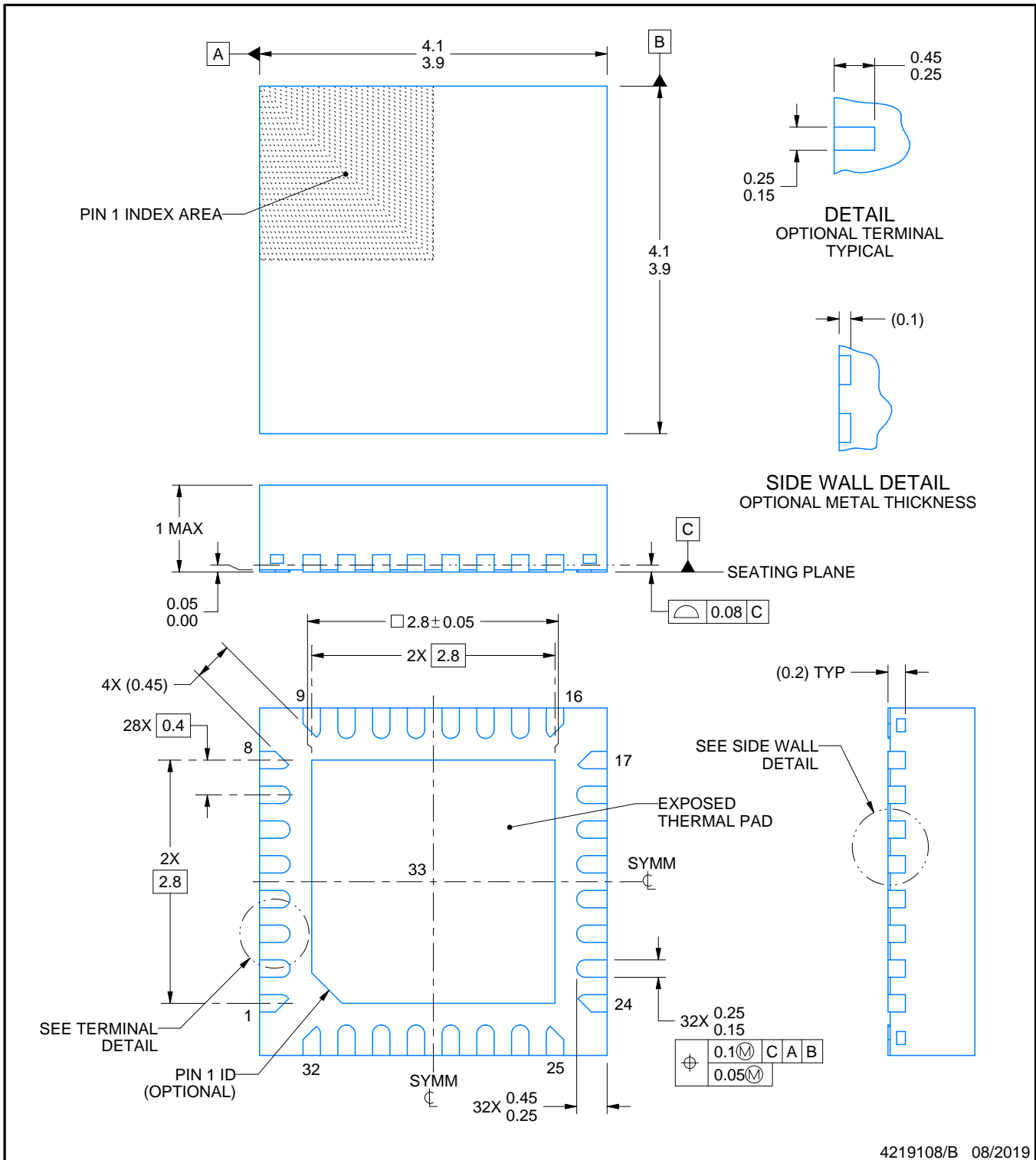
# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



### NOTES:

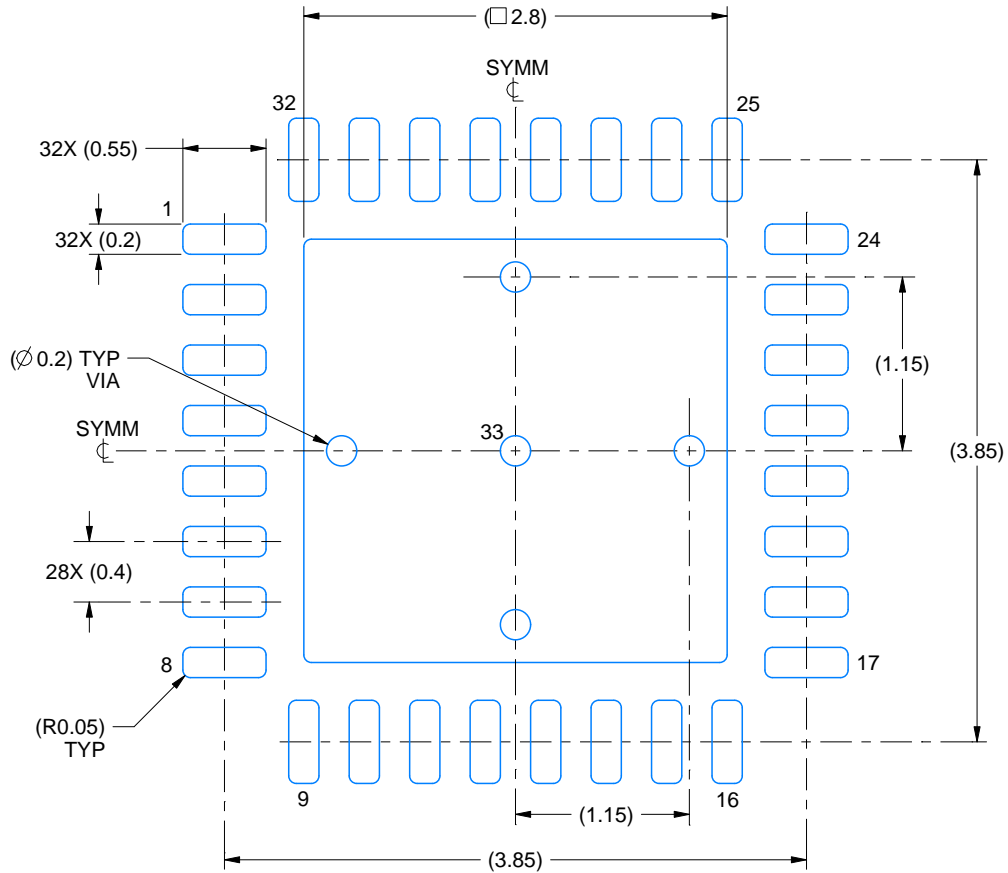
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

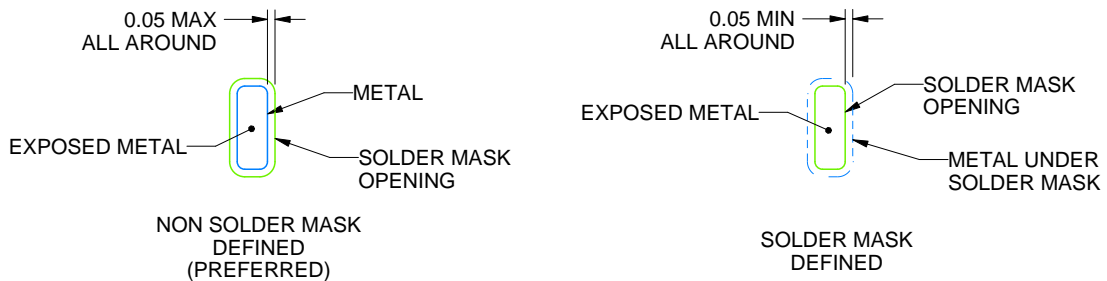
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

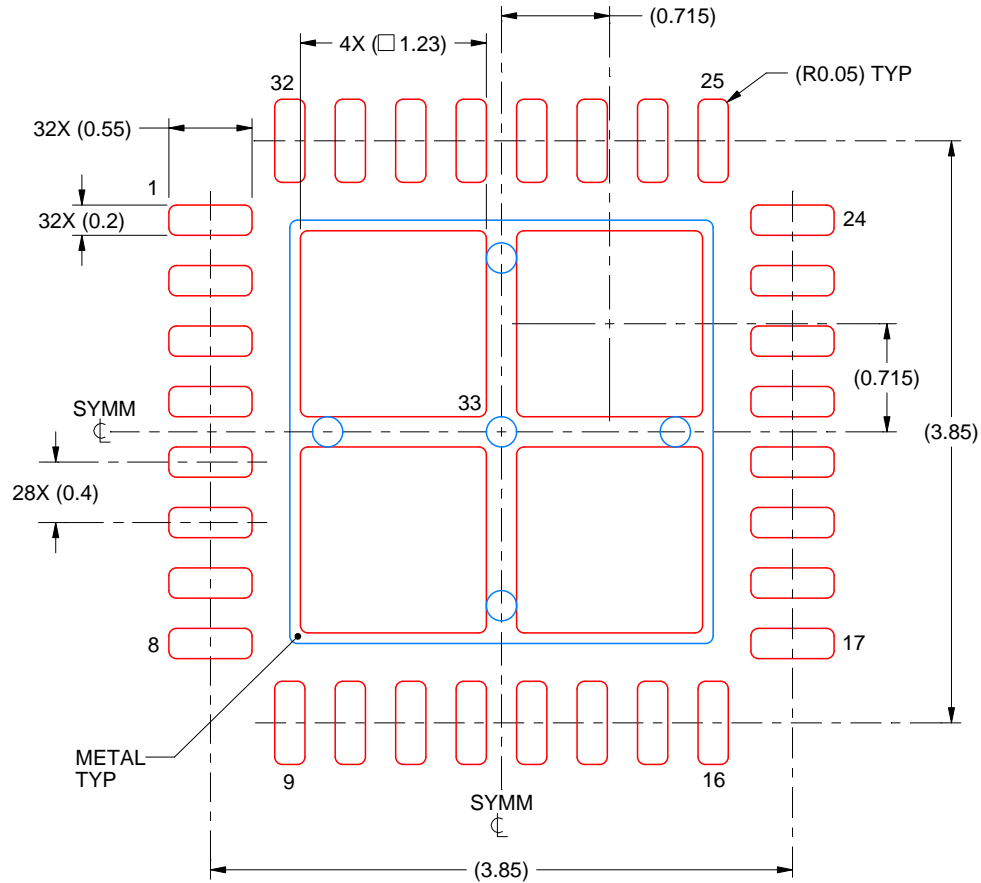
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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