

LP8769-Q1 高周波、クワッド降圧 DC/DC コンバータ

1 特長

- 下記内容で AEC-Q100 認定済み:
 - 入力電圧: 2.8 V ~ 5.5 V
 - デバイス温度グレード 1: -40°C ~ +125°C の動作時周囲温度範囲
 - デバイス HBM ESD 分類レベル 2
 - デバイス CDM ESD 分類レベル C4B
- 機能安全準拠
 - 機能安全アプリケーション向けに開発
 - ASIL-D までの ISO 26262 システムの設計に役立つ資料を提供
 - SIL-3 までの IEC 61508 システムの設計に役立つ資料を提供
 - ASIL-D までの決定論的能力
 - ASIL-D までのハードウェア安全度
 - 電圧および過電流のウィンドウ・モニタ
 - トリガ / Q&A モードを選択可能なウォッチドッグ
 - レベルまたは PWM エラー信号モニタ (ESM)
 - 温度監視と高温警告およびサーマル・シャットダウン
 - 構成レジスタと不揮発性メモリ (NVM) のビット整合性 (CRC) エラー検出
- 4 つの高効率降圧 DC/DC コンバータ:
 - 出力電圧: 0.3V ~ 3.34V (多相出力で 0.3V ~ 1.9V)
 - 最大出力電流: 1 相あたり 5A、4 相構成で最大 20A
 - 出力電圧のスルーレートをプログラム可能: 0.5mV/μs ~ 33mV/μs
 - スwitching 周波数: 2.2MHz または 4.4MHz
- 設定が可能な 10 個の汎用 I/O (GPIO)
- マルチ PMIC 同期用 SPMI インターフェイス
- 入力過電圧保護 (OVP) および低電圧誤動作防止 (UVLO)

2 アプリケーション

- 先進運転支援システム (ADAS)
- フロント・カメラ
- サラウンド・ビュー・システムの ECU
- 長距離レーダー
- センサ・フュージョン
- ドメイン・コントローラ

3 説明

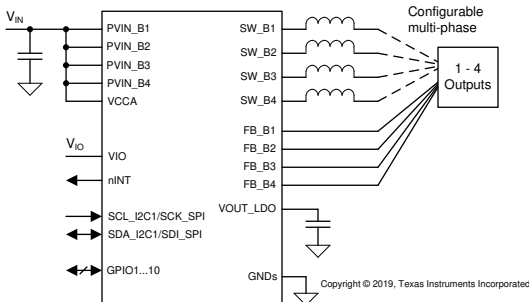
LP8769x-Q1 デバイスは、さまざまな車載用および産業用の安全関連アプリケーションで、最新のプロセッサおよびプラットフォームの電力管理要件を満たすよう設計されています。このデバイスには 4 つの降圧 DC/DC コンバータ・コアがあり、この出力は、5 種類の相構成が可能で、1 つの 4 相出力から 4 つの単相出力までを選択できます。デバイス設定は、I²C 互換のシリアル・インターフェイス、または SPI シリアル・インターフェイスにより変更可能です。

自動 PFM/PWM (AUTO モード) 動作と、自動相加算および相減算により、広い範囲の出力電流について最大の効率が得られます。LP8769x-Q1 デバイスは、多相出力のリモート差動電圧センシングに対応しており、レギュレータ出力とポイント・オブ・ロード (POL) との間の IR 降下を補償することで出力電圧の精度を高めることができます。Switching・クロックを強制的に PWM モードに設定することができ、位相をインターリーブします。Switching を外部クロックと同期させることができ、拡散スペクトラム・モードを有効にすることにより、外乱による変動を最小限に抑えられます。

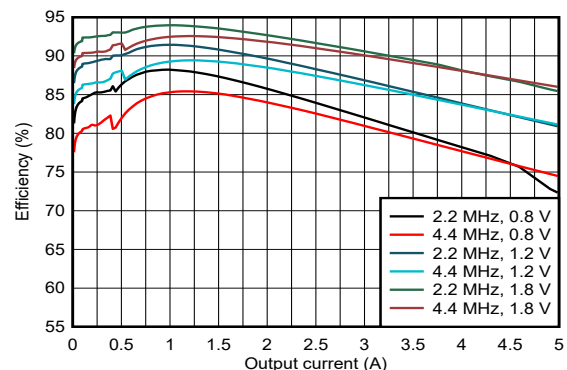
製品情報⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
LP8769-Q1	VQFN-HR (32)	5.50mm × 5.00mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



効率と出力電流との関係 (1 相)



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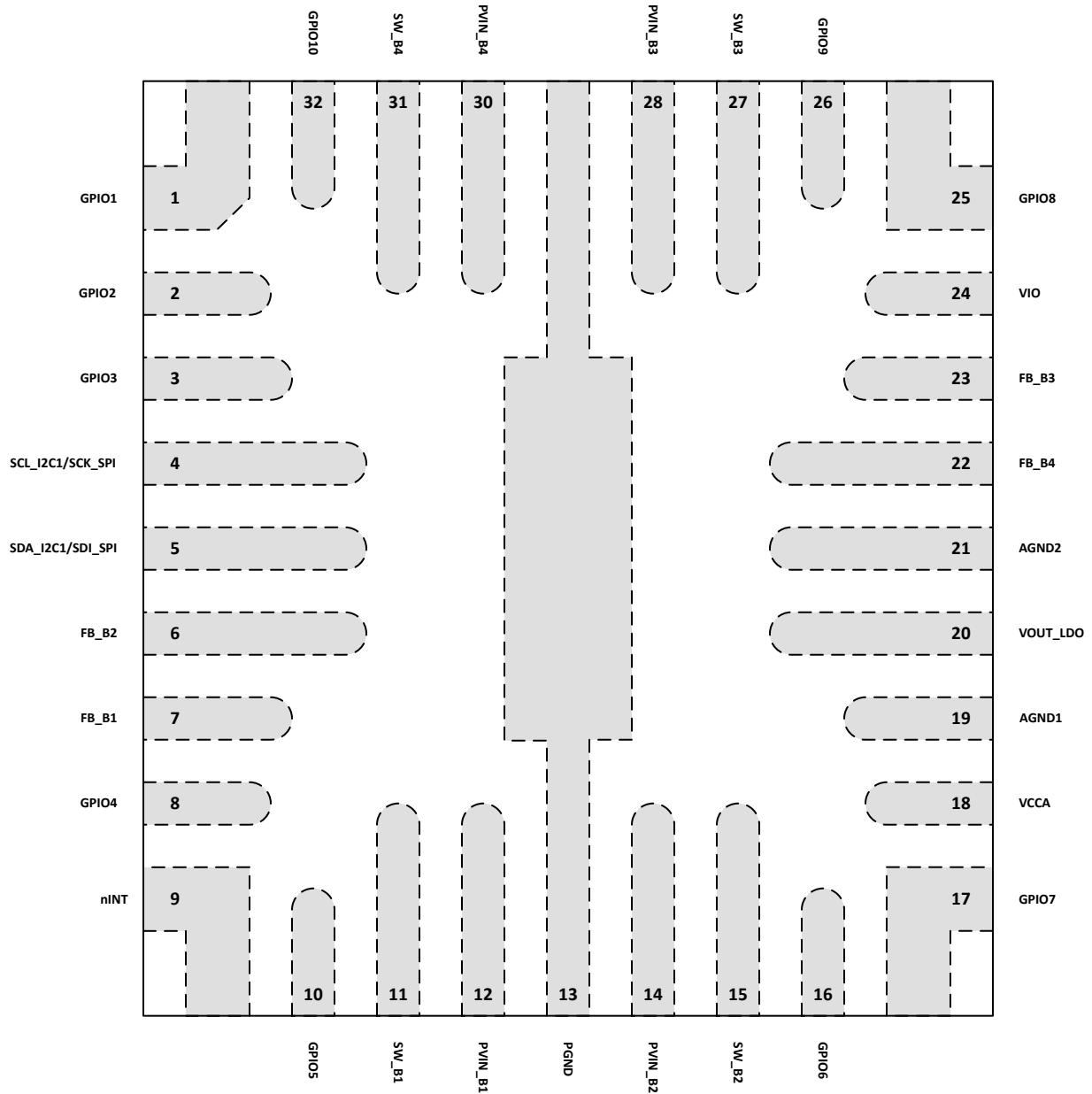
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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2022	*	Initial release

5 Pin Configuration and Functions



5-1. RQK Package 32-Pin VQFN-HR Top View

表 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	GPIO1	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: EN_DRV - Enable Drive output pin to indicate the device entering safe state (set low when ENABLE_DRV bit is '0').	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
2	GPIO2	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SCL_I2C2 - Serial interface clock input for I2C access.	Ground
		I	Digital	Alternative programmable function: CS_SPI - Serial interface Chip Select signal for SPI access.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
3	GPIO3	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDA_I2C2 - Serial interface data input and output for I2C access.	Ground
		O	Digital	Alternative programmable function: SDO_SPI - Serial interface data output signal for SPI access.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
4	SCL_I2C1/ SCK_SPI	I	Digital	If SPI is not used: SCL_I2C1 - Serial interface clock input for I2C access.	Ground
		I	Digital	If SPI is used: SCK_SPI - Serial interface clock input for SPI access.	Ground
5	SDA_I2C1/ SDI_SPI	I/O	Digital	If SPI is not used: SDA_I2C1 - Serial interface data input and output for I2C access.	Ground
		I	Digital	If SPI is used: SDI_SPI - Serial interface data input signal for SPI access.	Ground
6	FB_B2	—	Analog	Output voltage feedback (positive) for BUCK2. Alternatively ground feedback for BUCK1 in multiphase configuration.	Ground
7	FB_B1	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
8	GPIO4	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: ENABLE - External power-on control.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		—	Analog	Alternative programmable function: BUCK1_VMON - Voltage monitoring input for BUCK1 regulator.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
9	nINT	O	Digital	Open-drain interrupt output, active LOW.	Floating
10	GPIO5	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
11	SW_B1	—	Analog	BUCK1 switch node.	Floating
12	PVIN_B1	—	Power	Power input for BUCK1. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
13	PGND	—	Ground	Power ground for Buck regulators.	Ground
14	PVIN_B2	—	Power	Power input for BUCK2. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
15	SW_B2	—	Analog	BUCK2 switch node.	Floating
16	GPIO6	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
17	GPIO7	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Analog	Alternative programmable function: REFOUT - Buffered bandgap output.	Floating
		I	Analog	Alternative programmable function: VMON1 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
18	VCCA	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bx pins must be connected together in the application and be locally bypassed.	System supply
19	AGND1	—	Ground	Ground	Ground
20	VOUT_LDO	—	Power	LDO regulator filter node. LDO is used for internal purposes.	—
21	AGND2	—	Ground	Ground	Ground
22	FB_B4	—	Analog	Output voltage feedback (positive) for BUCK4. Alternatively ground feedback for BUCK3 in dualphase configuration.	Ground
23	FB_B3	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
24	VIO	—	Power	Supply voltage for selected digital outputs.	Ground
25	GPIO8	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SCLK_SPMI - Multi-PMIC SPMI serial interface clock signal. This pin is an output pin for the master SPMI device, and an input pin for the slave SPMI device.	Ground
		I	Analog	Alternative programmable function: VMON2 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
26	GPIO9	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDATA_SPMI - Multi-PMIC SPMI serial interface bidirectional data signal	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
27	SW_B3	—	Analog	BUCK3 switch node.	Floating
28	PVIN_B3	—	Power	Power input for BUCK3. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
30	PVIN_B4	—	Power	Power input for BUCK4. The separate power pins PVIN_Bx are not connected together internally – PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
31	SW_B4	—	Analog	BUCK4 switch node.	Floating
32	GPIO10	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: nRSTOUT - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 サポート・リソース

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6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP876924C3RQKRQ1	ACTIVE	VQFN-HR	RQK	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LP8769 24C3-Q1	Samples
LP876940C0RQKRQ1	ACTIVE	VQFN-HR	RQK	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LP8769 40C0-Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

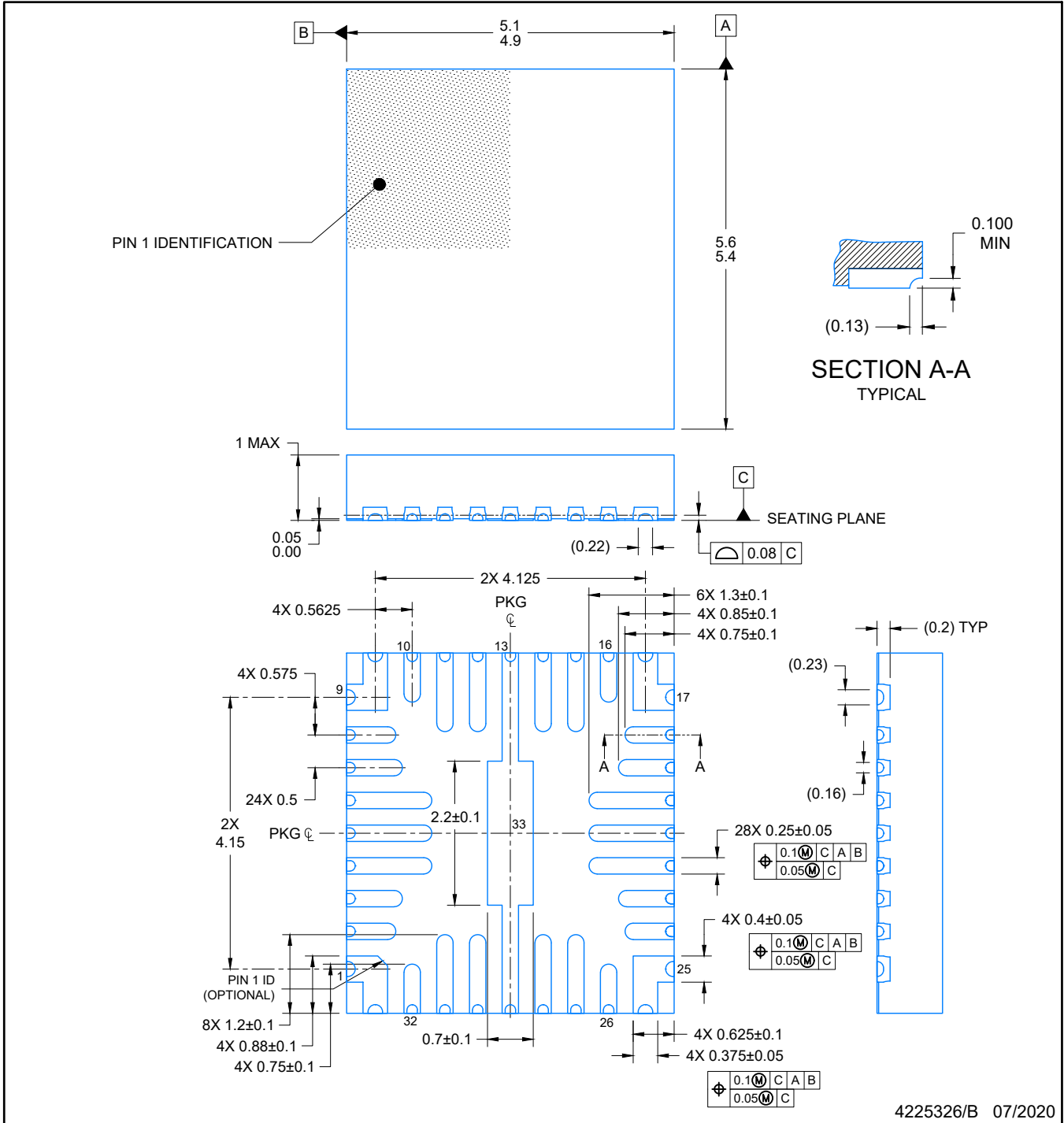
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

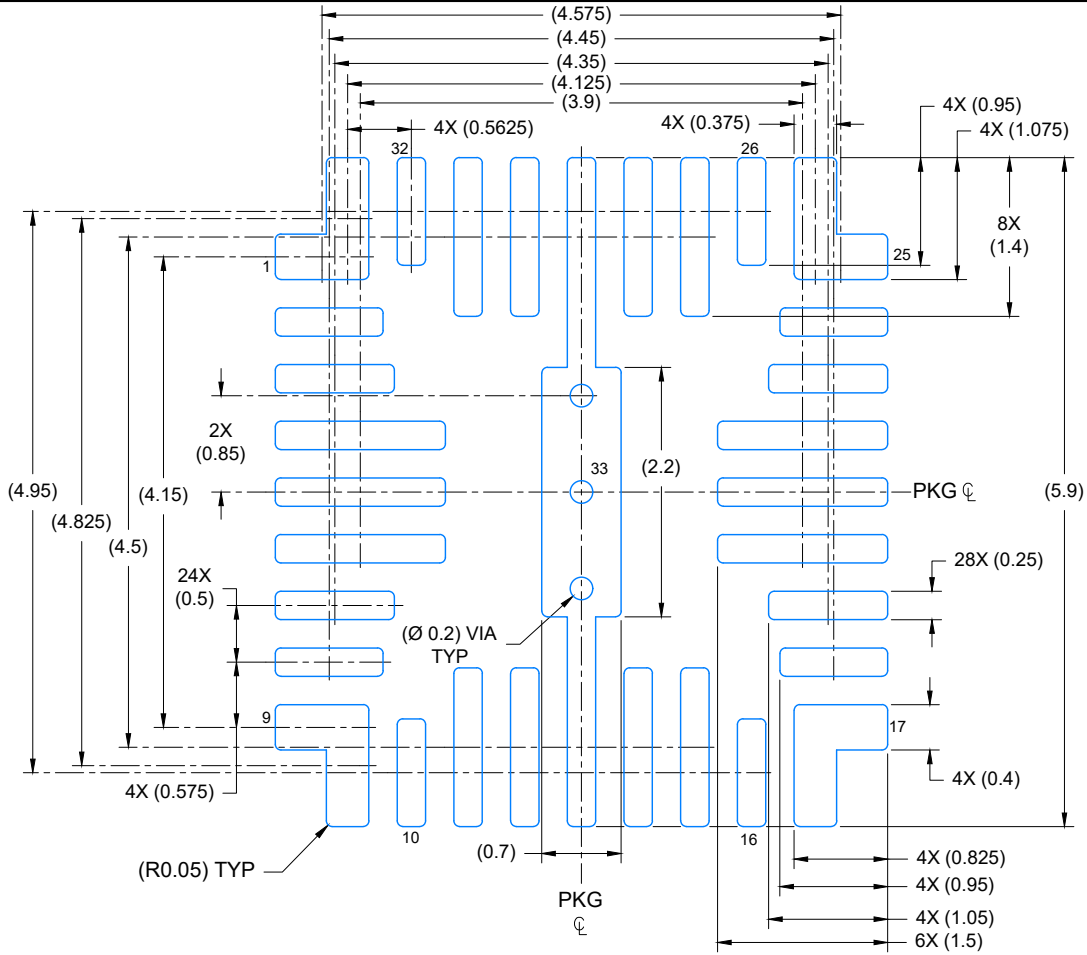
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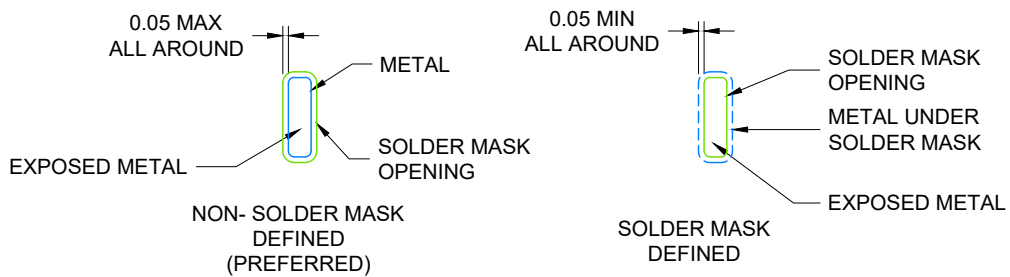


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

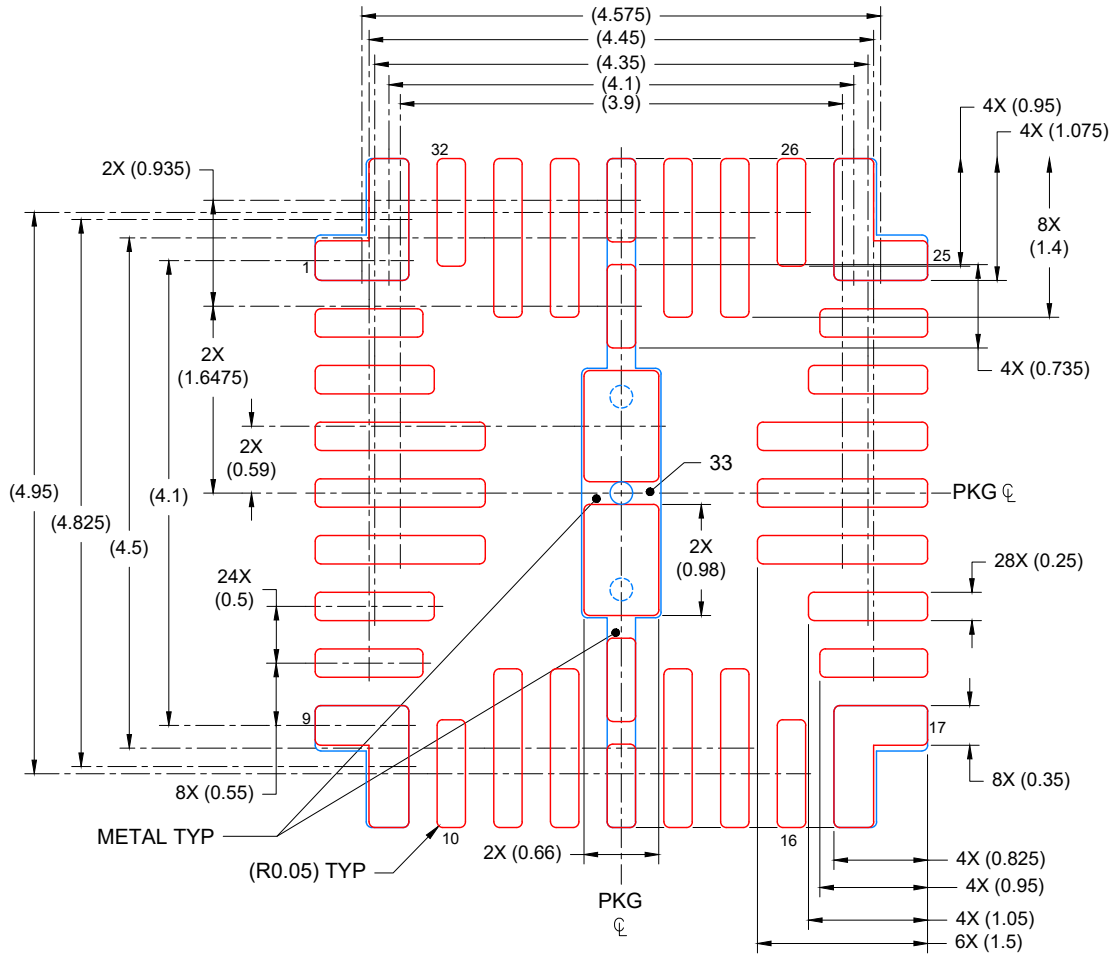


SOLDER MASK DETAILS
NOT TO SCALE

4225326/B 07/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.1mm THICK STENCIL

PIN 1,9,16 & 25: 93%; PIN 13& 29: 79%; PIN 33: 84%
 SCALE: 15X

4225326/B 07/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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