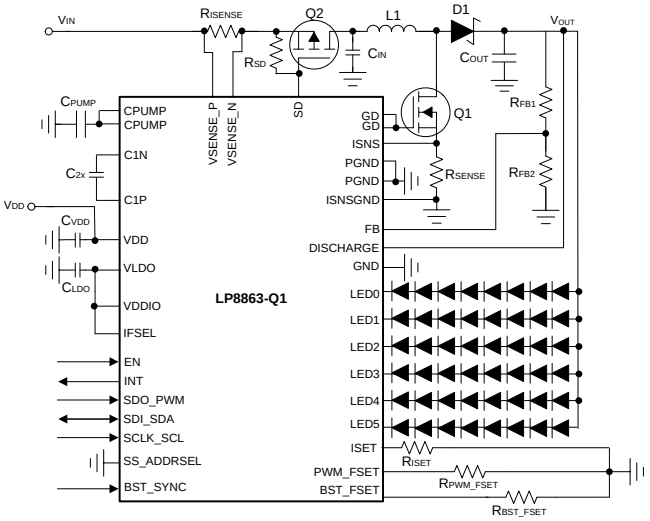
LP8863-Q1 6つの150mAチャネルを搭載した車載用ディスプレイLEDバックライト・ドライバ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～+125°C
- 動作入力電圧範囲: 3V～48V
- 6つの高精度電流シンク
  - 電流マッチング1% (標準値)
  - 152HzのLED出力PWM周波数を使用して、32,000:1の調光率
  - SPI、I2C、PWM入力により、最大16ビットのLED調光分解能
  - 使用中のLEDストリングを自動的に検出し、LEDチャネルの位相シフトを調整
  - チャネルごとに独立した電流制御
- ハイブリッドPWMおよび電流調光機能
- 最高47V の V_{OUT} 昇圧またはSEPIC DC/DCコントローラ
  - スイッチング周波数: 300kHz～2.2MHz
  - 昇圧拡散スペクトラムによるEMIの低減
  - 昇圧同期入力により、外部クロックから昇圧スイッチング周波数を設定
  - 内蔵のチャージ・ポンプはコールド・クランクなど低 V_{IN} の状況に対応
  - 昇圧のディセーブル時に出力電圧を自動的に放電
- 包括的なフォルト診断

概略回路図



2 アプリケーション

- 次の応用でのバックライト
  - 車載インフォテインメント
  - 車載用計器盤
  - スマート・ミラー
  - ヘッドアップ・ディスプレイ(HUD)
  - 集中情報ディスプレイ(CID)
  - オーディオ・ビデオ・ナビゲーション(AVN)

3 概要

LP8863-Q1は、昇圧コントローラ付きの車載用高効率LEDドライバです。6つの高精度電流シンクは位相シフトをサポートし、使用されているチャネル数に基づいて自動的に調整されます。電流シンクの輝度は、SPIまたはI2Cインターフェイスにより個別に、またはグローバルに制御できます。また、PWM入力によってグローバルに制御することもできます。

昇圧コントローラには、LED電流シンクのヘッドルーム電圧に基づいた、アダプティブ出力電圧制御が搭載されています。この機能により、あらゆる状況で十分な最低レベルに電圧を調整し、消費電力を最小化できます。周波数を広範囲に調整可能なため、LP8863-Q1はAMラジオ周波数帯の妨害を回避できます。

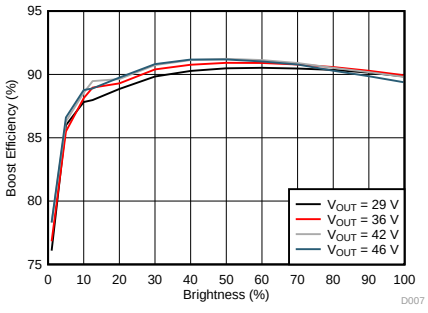
LP8863-Q1は組み込みのハイブリッドPWMおよび電流調光をサポートしているため、EMIの削減、LEDの寿命の延長、総合的な光効率の向上を実現します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LP8863-Q1	HTSSOP (38)	9.70mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

システム効率



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- Changed to "000h - 0FFh = 0 °C to 255 °C, 100h - 1FFh = –256 °C to –1 °C" from "0h = –1 to –255 °C" 58
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2017年3月発行のものから更新 **Page**

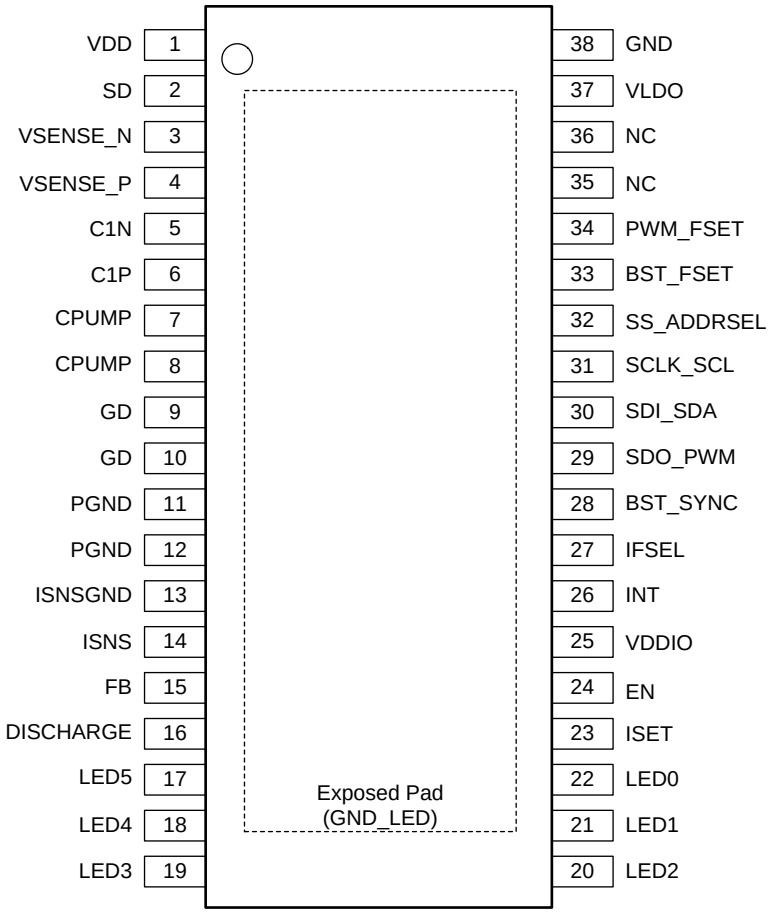
- 完全なデータシートの公開初版 1

5 Device Comparison Table

	LP8863-Q1	LP8860-Q1	LP8862-Q1	LP8861-Q1	TPS61193-Q1	TPS61194-Q1	TPS61196-Q1
V_{IN} range	3 V to 48 V	3 V to 48 V	4.5 V to 45 V	4.5 V to 45 V	4.5 V to 45 V	4.5 V to 45 V	8 V to 30 V
Number of LED channels	6	4	2	4	3	4	6
LED current / channel	150 mA	150 mA	160 mA	100 mA	100 mA	100 mA	200 mA
I2C/SPI support	Yes	Yes	No	No	No	No	No
SEPIC support	Yes	No	Yes	Yes	Yes	Yes	No

6 Pin Configuration and Functions

DCP Package
38-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD	Power	Power input for LDO, charge pump, and analog blocks - a 4.7–µF decoupling capacitor is recommended.
2	SD	Analog	Power line FET control. If unused, leave this pin floating.
3	VSENSE_N	Analog	Pin for input current sense. If input current sense is not used tie to VSENSE_P.
4	VSENSE_P	Analog	Pin for OVP/UVLO protection and input current sense.
5	C1N	Analog	Negative pin for charge pump flying capacitor. If feature not used, leave this pin floating.
6	C1P	Analog	Positive pin for charge pump flying capacitor. If feature not used, leave this pin floating.
7	CPUMP	Power	Charge pump output pin. If charge pump is not used connect to VDD. TI recommends a 10–µF decoupling capacitor.
8	CPUMP	Power	Charge pump output pin. If charge pump is not used connect to VDD.
9	GD	Analog	Gate driver output for boost FET
10	GD	Analog	Gate driver output for boost FET
11	PGND	Ground	Power ground
12	PGND	Ground	Power ground
13	ISNSGND	Ground	Current sense resistor GND of boost controller
14	ISNS	Analog	Boost current sense pin
15	FB	Analog	Boost feedback input
16	DISCHARGE	Analog	Boost output voltage discharge pin. Leave floating if unused.
17	LED5	Analog	LED current sink output. If unused tie to ground.
18	LED4	Analog	LED current sink output. If unused tie to ground.
19	LED3	Analog	LED current sink output. If unused tie to ground.
20	LED2	Analog	LED current sink output. If unused tie to ground.
21	LED1	Analog	LED current sink output. If unused tie to ground.
22	LED0	Analog	LED current sink output. If unused tie to ground.
23	ISET	Analog	LED current setting input
24	EN	Input	Enable input
25	VDDIO	Power	Supply input for digital IO pins - a 4.7–µF decoupling capacitor is recommended.
26	INT	Output	LP8863-Q1 device fault interrupt output, open drain. Requires an external pullup resistor to VDDIO - a 10-kΩ pullup resistor is recommended.
27	IFSEL	Input	Serial control interface selection: low = SPI, high = I2C
28	BST_SYNC	Input	Input for synchronizing boost. When synchronization is not used, connect this pin to ground to disable spread spectrum or to VDDIO to enable spread spectrum.
29	SDO_PWM	Input/Output	IFSEL=GND, slave data output for SPI. IFSEL=VDDIO, PWM input for brightness control. Tie to GND if unused.
30	SDI_SDA	Input	IFSEL=GND, slave data input for SPI; IFSEL=VDDIO, serial data for I2C
31	SCLK_SCL	Input	IFSEL=GND, serial clock for SPI; IFSEL=VDDIO, serial clock for I2C
32	SS_ADDRSEL	Input	IFSEL=GND, slave select for SPI; IFSEL=VDDIO, I2C address selection
33	BST_FSET	Analog	Resistor for setting boost FSW frequency. Do not leave floating.
34	PWM_FSET	Analog	Resistor for setting LED PWM frequency. Do not leave floating.
35	NC	N/A	No connect — leave floating.
36	NC	N/A	No connect — leave floating.
37	VLDO	Power	Internal 1.8-V LDO output. Connect bypass capacitor to this pin - a 10–µF decoupling capacitor is recommended.
38	GND	Ground	Ground for LDO — charge pump and analog blocks
DAP	GND_LED	Ground	LED ground connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	V_SENSE_P, VSENSE_N, SD, LED0 to LED5, FB, DISCHARGE	-0.3	50	V
	VDD, EN, ISNS	-0.3	5.5	
Voltage on pins	VDDIO, SCLK_SCL, SDI_SDA, SDO_PWM, SS_ADDRSEL, INT, IFSEL, BST_FSET, PWM_FSET, ISET	-0.3	3.6	V
	C1P, C1N, CPUMP (2) , GD	-0.3	12	
	VLDO	-0.3	2	
Thermal	Continuous power dissipation	Internally limited	Internally limited	
	Ambient temperature	-40	125	°C
	Junction temperature	-40	150	°C
	Maximum lead temperature (soldering)		260	°C
	Storage temperature, Tstg	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When internal charge pump is disabled and CPUMP pin is used as an input, maximum rating is 5.5 V same as VDD.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002, (1)		±2000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±500	
		Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). All voltages are with respect to the potential at the GND pins.

		MIN	NOM	MAX	UNIT
Voltage on pins	V_SENSE_P, VSENSE_N, SD	3	12	48	V
	Voltage on pins	0		48	
	EN, ISNS	0		5.5	
	VDD	2.7	3.3/5	5.5	
	VDDIO, SCLK_SCL, SDI_SDA, SDO_PWM, SS_ADDRSEL, INT, IFSEL, BST_FSET, PWM_FSET, ISET	1.65	1.8/3.3	3.6	
	VLDO	0	1.8	2	
	C1P, C1N, CPUMP (1) , GD	0	6.6/10	11	
Thermal	Ambient temperature	-40		125	°C

(1) When internal charge pump is disabled and CPUMP pin is used as an input, maximum rating is 5.5 V same as VDD.

7.4 Thermal Information

THERMAL METRIC(1)		LP8863 DCP (HTSSOP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Shutdown mode current, VDD pin	V_{DD} < V_{POR}, EN = L		0.3	2	µA
	Standby mode current, VDD pin	V_{DD} > V_{POR}, EN = L		75	300	µA
	Active mode current , VDD pin	LP8863-Q1 enabled, boost enabled (I_{LED} = 150mA), CP enabled, V_{DD} = 3.3V, f_{SW} = 300kHz, Boost FET - IPD25N06S4L-30		15	40(1)	mA
V_{POR}	Power-on reset threshold	VDD pin voltage.			2.65	V

(1) Ensured by design.

7.6 Protection Electrical Characteristics

Limits apply over the full operating ambient temperature range –40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3 V, V_{IN} = 12 V, V_{DDIO} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{UVLO}	V_{DD} UVLO threshold	V_{DD} falling	2.6	2.7	2.8	V
VDD_{UVLO_H}	V_{DD} UVLO hysteresis			0.1		V
VIN_{UVLO}	V_{IN} UVLO threshold	V_{IN} falling	2.7	2.8	2.9	V
VIN_{UVLO_H}	V_{IN} UVLO hysteresis			0.35		V
VIN_{OVP}	V_{IN} OVP threshold	V_{IN} rising	40.8	43	45.2	V
VIN_{OVP_H}	V_{IN} OVP hysteresis			2.5		V
T_{TSD}	Thermal shutdown threshold	Temperature rising	155	165	175	°C
T_{TSD_H}	Thermal shutdown hysteresis	Temperature falling from TSD threshold		20		°C
T_{TWR_H}	Thermal high warning threshold	temperature_limit_high = 0x07D	115	125	135	°C
T_{TWR_L}	Thermal low warning threshold	temperature_limit_low = 0x069	95	105	115	°C
V_{DDIO}	V_{DDIO} supply voltage		1.65		3.6	V
$VDDIOI_Q$	V_{DDIO} supply current			1		µA
V_{LDO}	LDO output voltage			1.8		V

7.7 LED Current Sink and LED PWM Electrical Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3 V, V_{IN} = 12 V, V_{DDIO} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs LED0 to LED5 = V_{OUT} = 45 V, EN = Low		0.1	2.5	µA
I_{MAX}	Max LED sink current	LED0 to LED5		150		mA
I_{ACC}	LED sink current accuracy(1)	I_{OUT} = 150 mA, PWM duty =100%	−4%		4%	
I_{MATCH}	LED sink current matching(1)	I_{OUT} = 150 mA, PWM duty =100%		1%	3.5%	
V_{SAT}	Saturation voltage (2)	I_{OUT} = 150 mA		0.4	0.79	V
$f_{PWM\_OUT\_MIN}$	Minimum LED PWM output frequency			0.152		kHz
$f_{PWM\_OUT\_MAX}$	Maximum LED PWM output frequency			19.5		kHz
DIM	Dimming ratio	f_{PWM_OUT} = 152 Hz		32000:1		
		f_{PWM_OUT} = 4.8 kHz with hybrid dimming		8000:1		
		f_{PWM_OUT} = 4.8 kHz		1000:1		
$V_{HEADROOM}$	LED sink headroom			0.55		V
$V_{HEADROOM\_HYST}$	LED sink headroom hysteresis			0.5		V
$V_{LEDSHORT}$	LED short detection threshold	shorted_led_thresh = 000		2.6		V
		shorted_led_thresh = 001		3.0		
		shorted_led_thresh = 010		3.5		
		shorted_led_thresh = 011		3.8		
		shorted_led_thresh = 100		4.1		
		shorted_led_thresh = 101		4.6		
		shorted_led_thresh = 110		5.2		
		shorted_led_thresh = 111		5.9		
t_{PWM_OUT}	LED output minimum pulse			200		ns

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (LED0 to LED5), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1 V headroom voltage. Note that some manufacturers have different definitions in use.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

7.8 Power-Line FET and R_{ISENSE} Electrical Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3 V, V_{IN} = 12 V, V_{DDIO} = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCP}	Input over current threshold	R_{ISENSE} = 20 mΩ	9.35	11	12.65	A
$I_{LEAK\_VSENSE\_P}$	VSENSE_P pin leakage current	V_{SENSE_P} = 48 V		1		µA
$I_{LEAK\_VSENSE\_N}$	VSENSE_N pin leakage current	V_{SENSE_N} = 48 V		1		µA
I_{LEAK_SD}	SD pin leakage current	V_{SD} = 48 V		1		µA
t_{SOFT_START}	Power line FET soft start	When R_{ISENSE} is used		50		ms
I_{SD}	SD Pull-down current	R_{SD} = 20 kΩ	325		450	µA

7.9 Input PWM Electrical Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM_IN}	PWM input frequency		100		20 000	Hz
$t_{PWM\_MIN\_ON}$	PWM input minimum on time			200		ns
$INPWM_{RES}$	PWM input resolution	f_{PWM_IN} = 100 Hz		16		bit
		f_{PWM_IN} = 20 kHz		10		

7.10 Boost Converter Electrical Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		3		48	V
V_{OUT}	Output voltage	Boost mode (R_{FBTOP} = 910 kΩ, R_{FBBOT} = 100 kΩ)	20		47	V
		SEPIC mode (R_{FBTOP} = 560 kΩ, R_{FBBOT} = 170 kΩ)	6		24	
f_{SW}	Switching frequency	BST_FSET = 3.93 kΩ		303		kHz
		BST_FSET = 4.75 kΩ		400		
		BST_FSET = 5.76 kΩ		606		
		BST_FSET = 7.87 kΩ		800		
		BST_FSET = 11 kΩ		1000		
		BST_FSET = 17.8 kΩ		1250		
		BST_FSET = 42.2 kΩ		1667		
		BST_FSET = 140 kΩ		2200		
V_{OUT}/V_{IN}	Max conversion ratio	Boost mode, I_{OUT} = 6 x 150 mA			5.5(1)	
		Boost mode, I_{OUT} = 6 x 85 mA			10(1)	
		SEPIC mode	0.2		5(1)	
I_{MAX}	Boost switching current limit	R_{SENSE} = 20 mΩ	9	10	11	A
V_{GD}	External FET gate drive voltage	VDD = 5 V +/-10%, CP Disabled	4.5	5	5.5	V
		VDD = 3.3 V +/-10%, CP Enabled	6	6.6	7.2	
		VDD = 5 V +/-10%, CP Enabled	9	10	11	
GDR_{DSONH}	R_{DSON} of internal high side FET to drive gate of external FET	Source, V_{GD}/(GDR_{DSON} + Total resistance to gate input of SW FET) must not be higher than 2.5A		1.4		Ω
GDR_{DSONL}	R_{DSON} of internal low side FET to drive gate of external FET	Sink, V_{GD}/(GDR_{DSON} + Total resistance to gate input of SW FET) must not be higher than 2.5A		0.75		Ω
$t_{START-UP}$	Start-up time	Delay from beginning of boost soft start to when LED drivers can begin		50		ms
T_{ON}	Minimum switch on time			120		ns
T_{OFF}	Minimum switch off time			70		ns
V_{BST_OVPL}	BOOST_OVP low threshold at FB pin			1.423		V
V_{BST_OVPH}	BOOST_OVP high threshold at FB pin			1.76		V

(1) Ensured by design

7.11 Oscillator

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency		18.6	20	21.4	MHz

7.12 Charge Pump

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CP}	Charge pump switching frequency		387	417	447	kHz

7.13 Logic Interface Characteristics

Limits apply over the full operating ambient temperature range -40°C ≤ T_A ≤ +125°C, Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 12V, V_{DDIO} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT EN						
VEN_{IL}	Input low level				0.4	V
VEN_{IH}	Input high level		1.2			V
IENI	Input current			5	30	µA
R_{PDEN}	EN pin internal pull-down resistance			5		MΩ
LOGIC INPUT SCLK_SCL, SDI_SDA, SS_ADDRSEL, PWM, IF_SEL, BST_SYNC						
V_{IL}	Input low level				0.2 x VDDIO	V
V_{IH}	Input high level		0.8 x VDDIO			V
I_I	Input current				5	µA
$VSDO_{OL}$	Output low level	I_{OUT} = 3 mA		0.3	0.5	V
$VSDO_{OH}$	Output high level	I_{OUT} = –2 mA	0.7 x VDDIO	0.9 x VDDIO		V
LOGIC OUTPUT SDA						
$VSDA_{OL}$	Output low level	I = 3 mA		0.3	0.5	V
$ISDA_{LEAKAGE}$	Output leakage current	V = 5.5 V			1	µA
LOGIC OUTPUT INT						
$VINT_{OL}$	Output low level	I_{OUT} = 3 mA		0.3	0.5	V
$IINT_{LEAK}$	Output leakage current				1	µA

7.14 Timing Requirements for SPI Interface

		MIN	NOM	MAX	UNIT
1	Cycle time	100			ns
2	Enable lead time	50			ns
3	Enable lag time	50			ns
4	Clock low time	45			ns
5	Clock high time	45			ns
6	Data setup time	20			ns
7	Data hold time	20			ns
8	Disable time			30	ns
9	Data valid			35	ns
10	SS inactive time	50			ns
C_b	Bus capacitance	5		40	pF

7.15 Timing Requirements for I²C Interface

		MIN	NOM	MAX	UNIT
f_{SCLK}	Clock frequency			400	kHz
1	Hold time (repeated) START Condition	0.6			µs
2	Clock low time	1.3			µs
3	Clock high time	600			ns
4	Set-up time for a repeated START condition	600			ns
5	Data hold time	50			ns
6	Data setup time	100			ns
7	Rise Time of SDA and SCL			300	ns
8	Fall Time of SDA and SCL			300	ns
9	Set-up time for STOP condition	600			ns
10	Bus free time between a STOP and a START Condition	1.3			µs

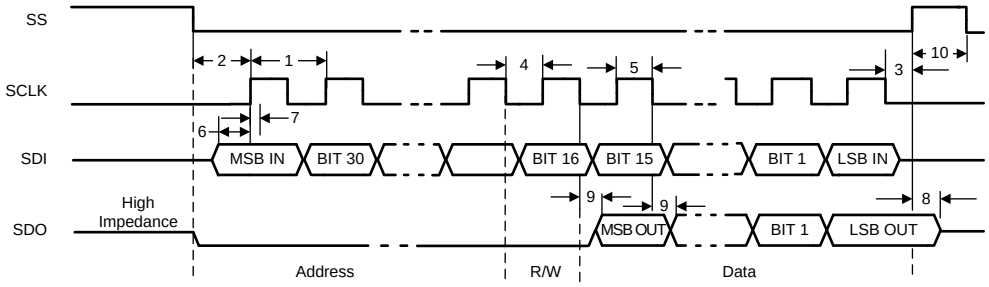


図 1. SPI Timing Diagram

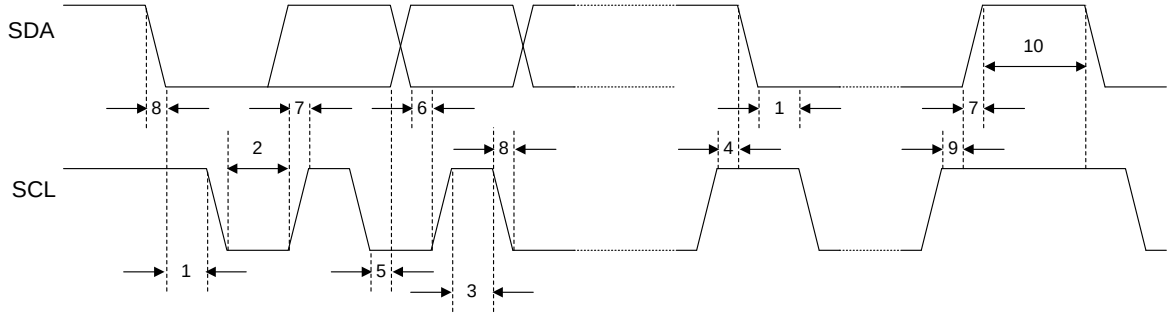
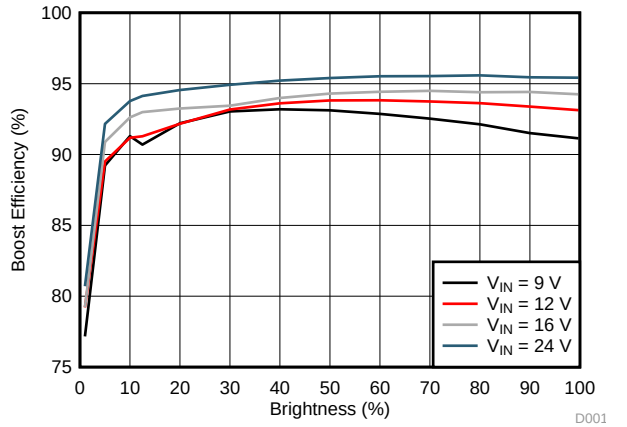


図 2. I2C Timing Diagram

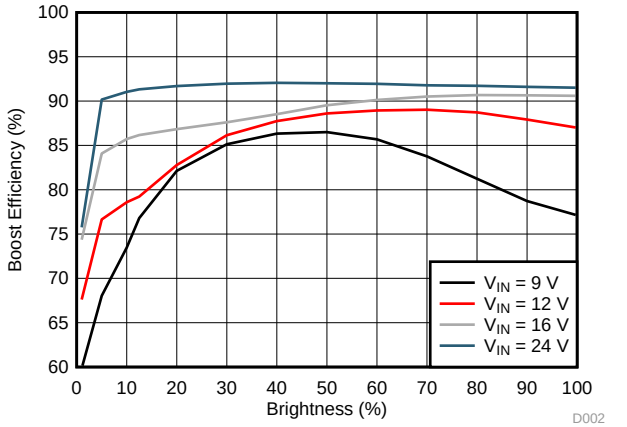
7.16 Typical Characteristics

Unless otherwise specified: $C_{IN} = C_{OUT}$ = 2 × 10-µF ceramic and 2 × 33-µF electrolytic, V_{DD} = 3.3 V, charge pump enabled, T_A = 25°C



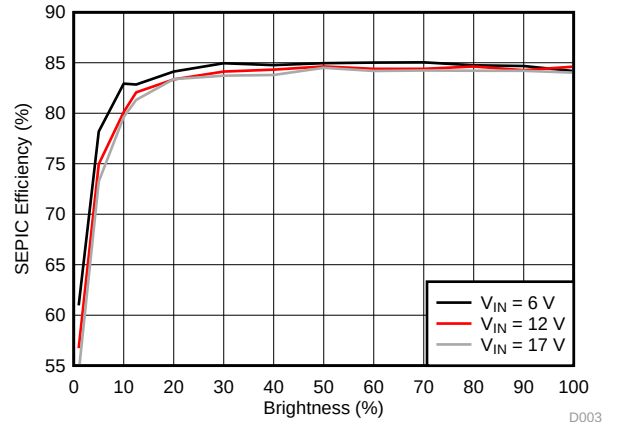
f_{SW} = 303 kHz | 8 LEDs/string | 150 mA/string
L1 = 22 µH | 6 strings

図 3. Boost Efficiency



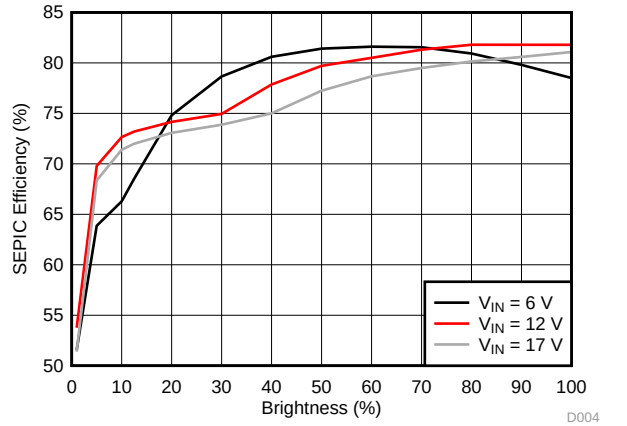
f_{SW} = 2.2 MHz | 8 LEDs/string | 150 mA/string
L1 = 10 µH | 6 strings

図 4. Boost Efficiency



f_{SW} = 303 kHz | 2 LEDs/string | 150 mA/string
L1 = 10 µH, L2 = 15 µH | 6 strings

図 5. SEPIC Efficiency



f_{SW} = 2.2 MHz | 2 LEDs/string | 150 mA/string
L1 = L2 = 4.7 µH | 6 strings

図 6. SEPIC Efficiency

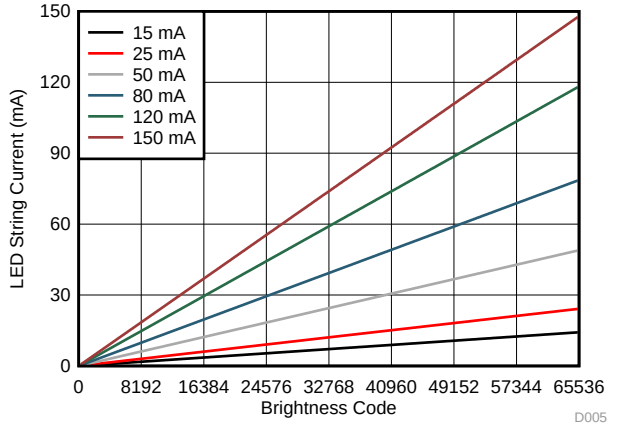


図 7. Current Linearity

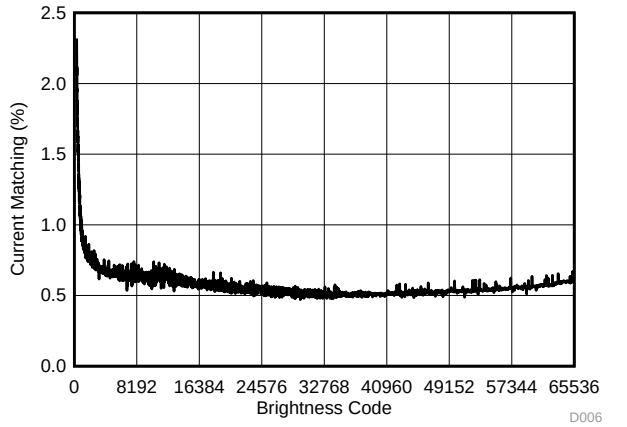


図 8. Current Matching

8 Detailed Description

8.1 Overview

The LP8863-Q1 device is a high-voltage LED driver for automotive infotainment, clusters, and other automotive display LED backlight applications. It supports conventional LED backlight applications and cluster-mode applications requiring independent duty and current control of each channel.

The LP8863-Q1 device uses the PWM input for brightness control by default. Alternatively, the brightness can also be controlled by I2C or SPI. When two LP8863-Q1 devices are used in the system, individual I2C addresses can be selected independently with the SS_ADDRSEL pin. In cluster-mode applications each of the six LED brightness levels can be individually controlled via the I2C or SPI interface.

The boost frequency, LED PWM frequency, and LED string current are configured with external resistors through the BST_FSET, PWM_FSET, and ISET pins. The INT pin is used to report faults to the system. Fault interrupt status can be cleared with the I2C, SPI interface, or is cleared on the falling edge of the VDD pin.

The LP8863-Q1 supports pure PWM dimming and hybrid dimming; that is, combined PWM and current brightness control. By default PWM dimming mode is enabled, but can be changed using the I2C or SPI interface.

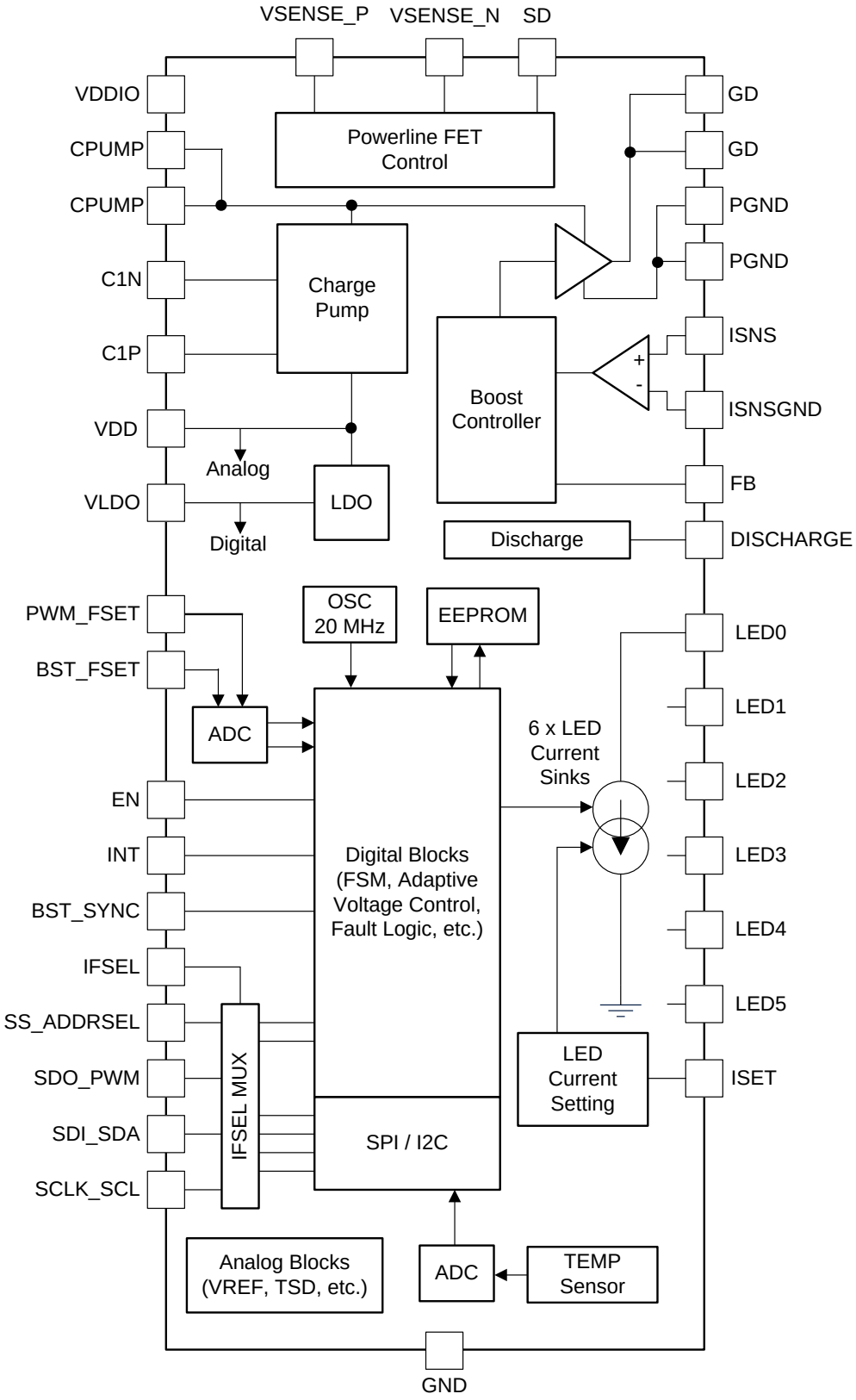
The six LED current drivers provide up to 150 mA per output and can be tied together to support higher current LEDs. The maximum output current of the LED drivers is set with the ISET resistor and can be optionally scaled by the LEDx_CURRENT[11:0] register bits with I2C or SPI interfaces. The LED output PWM frequency is set with a PWM_FSET resistor. The number of connected LED strings is automatically detected, and the device automatically selects the correct phase shift. For example, if four strings are connected, the LED outputs are phase shifted by 90 degrees (= 360 / 4); if 6 strings are connected, the LED outputs are phase shifted by 60 degrees (= 360 / 6). Outputs that are not used must be connected to GND. Unused outputs are disabled and excluded from adaptive voltage and do not generate open/short LED faults. When I2C is available, LED outputs can be re-configured in cluster mode to support up to 6 individually controlled channels or, alternatively, 3 to 5 channels for a display and 3 to 1 individual channels for indicator lights. In this mode all strings can be connected to the boost of LP8863-Q1 or an external boost can be used for indicator channels.

A resistor divider connected from V_{OUT} to the FB pin sets the maximum voltage of the boost. For best efficiency the boost voltage is adapted automatically to the minimum necessary level needed to drive the LED strings by monitoring all the LED output voltage drops in real time. The switching frequency of the boost regulator can be set between 300 kHz and 2.2 MHz by the BST_FSET resistor. The boost has a start-up feature that reduces the peak current from the power-line during start-up. The LP8863-Q1 also can control a power-line FET to reduce battery leakage when disabled and provide isolation and protection in the event of a fault.

Fault detection features of LP8863-Q1 include:

- Open-string and shorted LED detection
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- Boost overcurrent
- Boost overvoltage
- Device undervoltage protection
  - Threshold sensing from VDD pin
- V_{IN} input overvoltage protection (OVP)
  - Threshold sensing from VSENSE_P pin
- V_{IN} input undervoltage protection
  - Threshold sensing from VSENSE_P pin
- V_{IN} input overcurrent protection (OCP)
  - Threshold sensing across R_{ISENSE} resistor
- Thermal shutdown in case of die overtemperature
- Die temperature read-out and programmable thermal window detector

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Interface

Device control interface includes:

- EN is the enable input for the LP8863-Q1 device.
- INT is an open-drain fault output (indicating fault condition detection or thermal threshold crossing).
- IFSEL is used for selecting between I2C and SPI.
  - SPI is a 4-wire interface using SCL, SDI, SDO, and SS pins.
  - When SPI is selected the brightness must be controlled using the DISP_BRT and BRT_MODE registers.
  - I2C is a 2-wire interface using SCL and SDA pins.
  - When I2C is selected, the ADDRSEL pin is used to select between two alternate slave addresses.
  - When I2C is selected, the BRT_MODE register setting is used to select whether the brightness is controlled by the DISP_BRT register or PWM input pin. The PWM pin is selected by default so that an I2C interface is not required.
- BST_SYNC is used to input an external clock for the boost switching frequency and control the internal boost clock mode.
  - The external clock is auto detected at start-up and, if missing, the internal clock is used.
  - Optionally, the BST_SYNC can be tied to VDDIO to enable the boost spread spectrum function or tied to GND to disable it.
- ISET pin to set the maximum LED current level per string.
- BST_FSET pin to set the boost switching frequency.
- PWM_FSET pin to set the LED output PWM dimming frequency.

Control interface is selected with IF_SEL pin according to 表 1.

表 1. Control Interface Selection, SPI or I2C

IF_SEL	SERIAL INTERFACE
VDDIO (1)	I2C
GND (0)	SPI

In I2C mode the ADDRSEL is used to select between two unique slave addresses, and the PWM input may be used to control the brightness.

8.3.2 Boost Controller

The LP8863-Q1 current-mode-controlled boost DC/DC controller generates the bias voltage for the LEDs. The boost is a current-mode-controlled topology with an 8-A cycle by cycle current limit. The boost converter senses the switch current and across the external sense resistor connected between ISNS and ISNSGND. A 25-mΩ sense resistor results in an 8-A cycle by cycle current limit.. Maximum boost voltage is configured with external FB-pin resistor divider connected between V_{OUT} and FB. The FB-divider equation is described in *Boost Adaptive Voltage Control*.

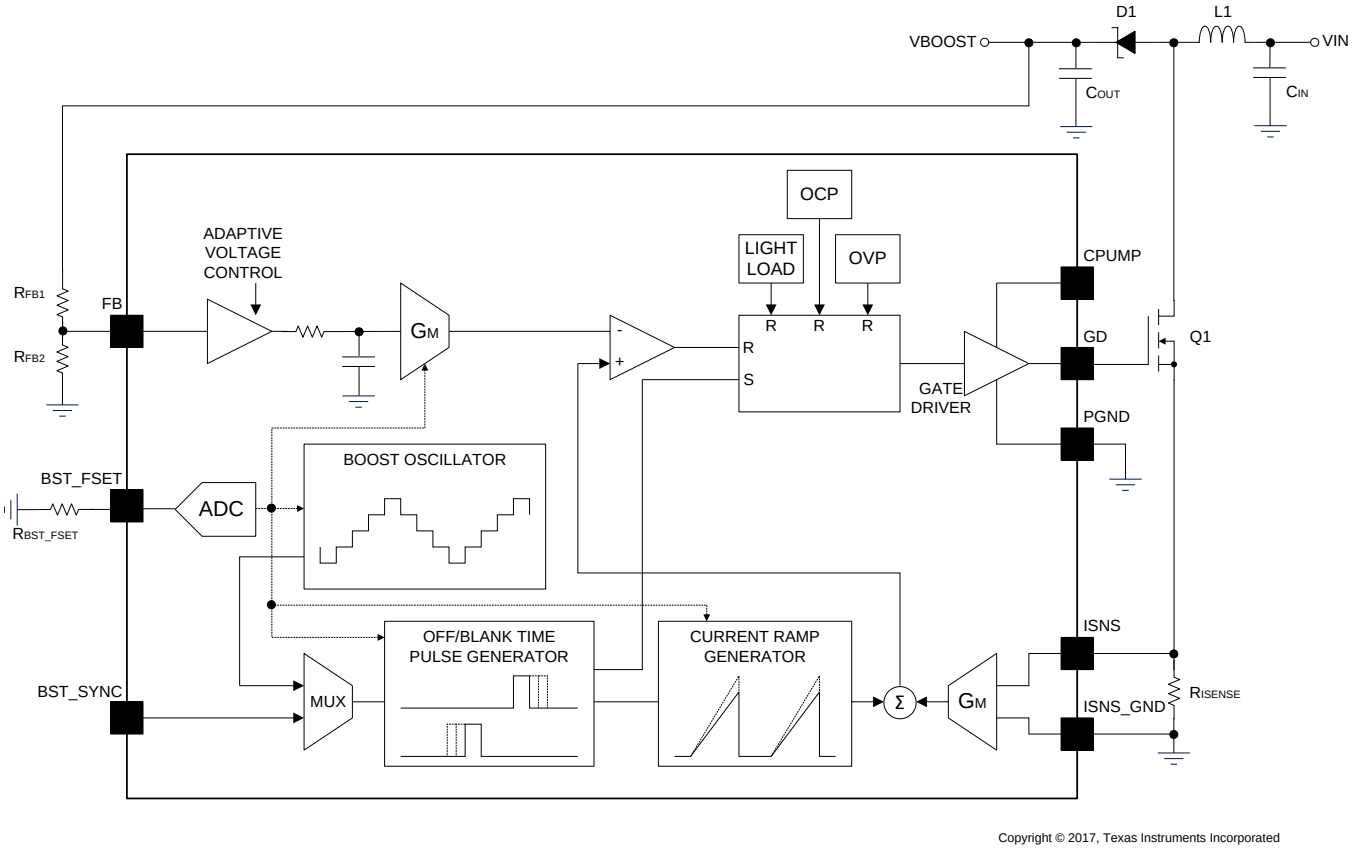


図 9. Boost Controller Block Diagram

The boost switching frequency is adjustable from 300 kHz to 2.2 MHz via an external resistor at BST_FSET (see 表 2).

表 2. Boost Frequency Selection

R_BST_FSET (kΩ)	BOOST FREQUENCY (kHz)
3.92	303
4.75	400
5.76	606
7.87	800
11	1000
17.8	1250
42.2	1667
140	2200

8.3.2.1 Boost Adaptive Voltage Control

The LP8863-Q1 boost DC/DC converter generates the bias voltage for the LEDs. During normal operation, boost output voltage is adjusted automatically based on the LED current sink headroom voltages. This is called adaptive boost control. The number of used LED outputs is auto detected and only the active LED outputs are monitored to control the adaptive boost voltage. Any LED strings with open or short faults are also removed from the adaptive voltage control loop. The LED driver pin voltages are periodically monitored by the control loop and the boost voltage is raised if any of the LED outputs falls below the low headroom threshold. The boost voltage is lowered if all the LED outputs are above the high headroom threshold. See 図 10 for how the low and high headroom thresholds automatically scale based on the LED string current and V_{SAT} level being used.

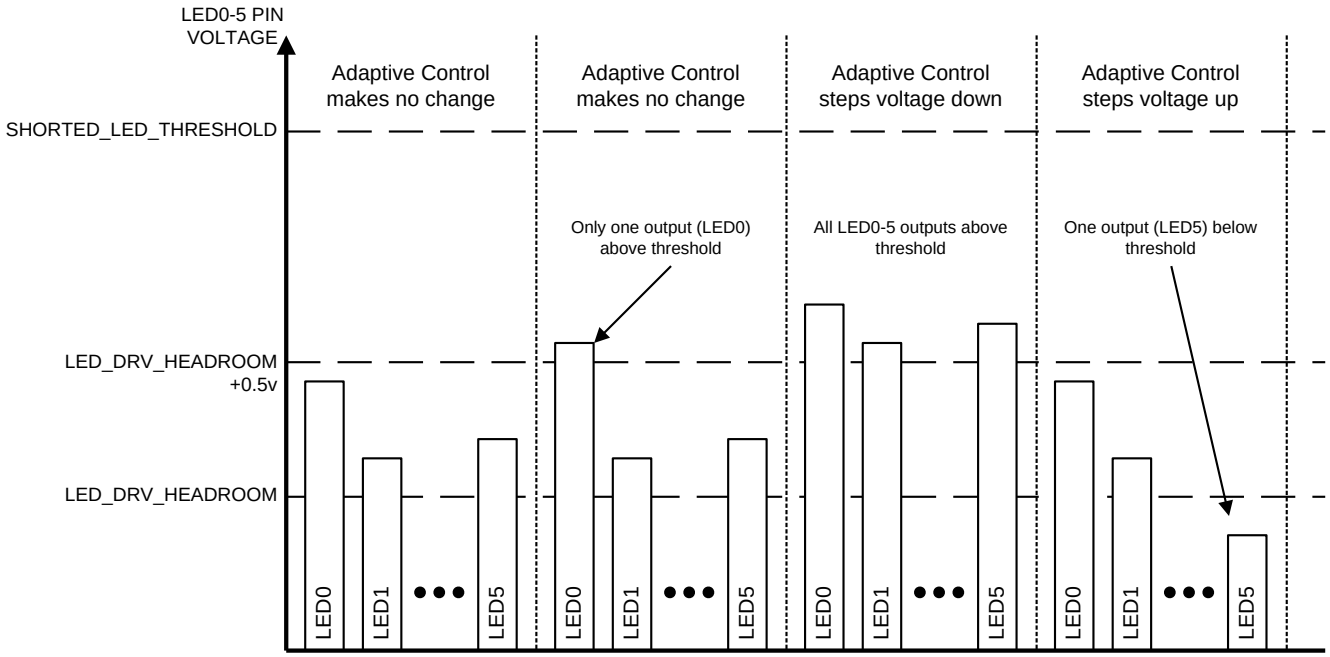


図 10. Adaptive Boost Voltage Control Loop Function

The external resistive divider (R_{FB1}, R_{FB2}) defines both the minimum and maximum adaptive boost voltage levels. The FB circuit operates the same in boost and SEPIC topologies. Choose maximum boost voltage based on the maximum LED string voltage specification. Before the LED drivers are active the boost starts up to the initial boost level. The initial boost voltage is approximately 90% of maximum boost voltage. Once the LED driver channels are active, the boost output voltage is adjusted automatically based on LED current sink headroom voltage. The FB pin resistor divider also scales the boost OVP and undervoltage levels.

8.3.2.1.1 FB Divider Using Two-Resistor Method

A typical FB-pin circuit uses a two-resistor divider circuit between the boost output voltage and ground.

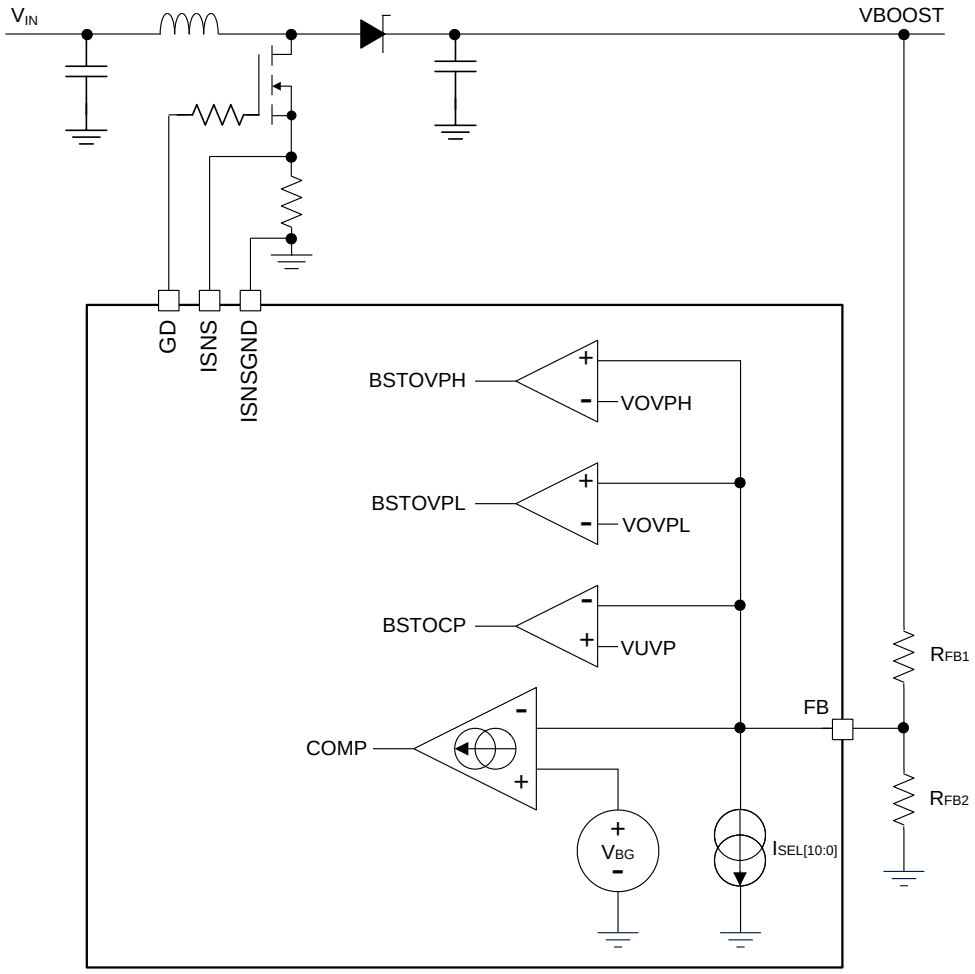


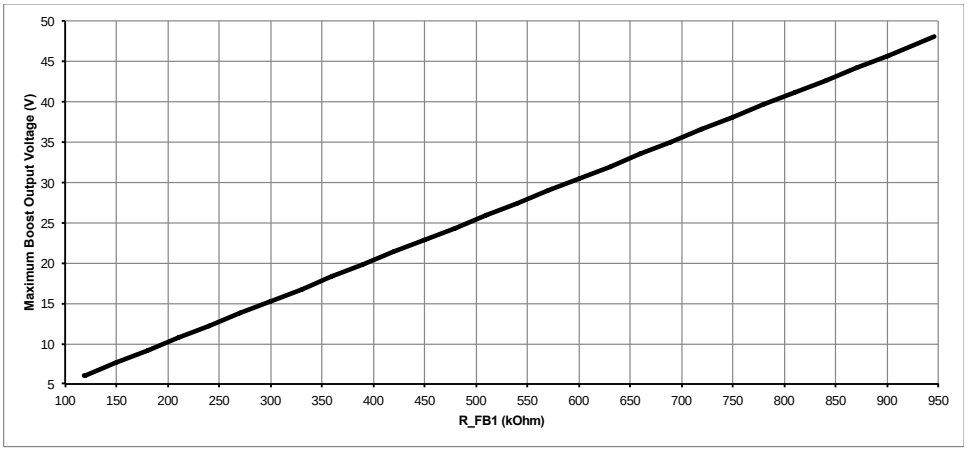
図 11. Two-Resistor FB Divider Circuit

Maximum boost voltage can be calculated with 式 1. The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{MAXBOOST} = \left(\left(\frac{V_{BG}}{R_{FB2}}\right) + I_{SEL\_MAX}\right) \times R_{FB1} + V_{BG} \quad (1)$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_{FB2} recommended value is 100 kΩ for boost operation and 170 kΩ for SEPIC operation.



R_{FB2} = 100 kΩ

図 12. Maximum Boost Output Voltage vs. RFB1 Resistor Value

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated with 式 2:

$$V_{MINBOOST} = (\frac{V_{BG}}{R_{FB2}}) \times R_{FB1} + V_{BG} \quad (2)$$

where

- V_{BG} = 1.21 V

When the boost OVP_LOW level is reached the boost controller stops switching the boost FET and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold is calculated with 式 3:

$$V_{BOOST\_OVP\_LOW} = ((\frac{V_{OVPL}}{R_{FB2}}) + I_{SEL\_MAX}) \times R_{FB1} + V_{OVPL} \quad (3)$$

where

- V_{OVPL} = 1.423 V
- I_{SEL_MAX} = 38.7 µA

When the boost OVP_HIGH level is reached the boost controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold is calculated with 式 4:

$$V_{BOOST\_OVP\_HIGH} = ((\frac{V_{OVPH}}{R_{FB2}}) + I_{SEL\_MAX}) \times R_{FB1} + V_{OVPH} \quad (4)$$

where

- V_{OVPH} = 1.76 V
- I_{SEL_MAX} = 38.7 µA

When the boost UVP level is reached the boost controller starts a 100-ms OCP counter. The LP8863-Q1 device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage when adaptive voltage control is at the maximum output voltage is calculated with 式 5:

$$V_{BOOST\_UVP} = ((\frac{V_{UVP}}{R_{FB2}}) + I_{SEL\_MAX}) \times R_{FB1} + V_{UVP} \quad (5)$$

where

- V_{UVP} = 0.886 V
- I_{SEL_MAX} = 38.7 µA

8.3.2.1.2 FB Divider Using Three-Resistor Method

A FB-pin circuit using a three-resistor divider circuit can be used for applications where less than 200-kΩ resistors are required.

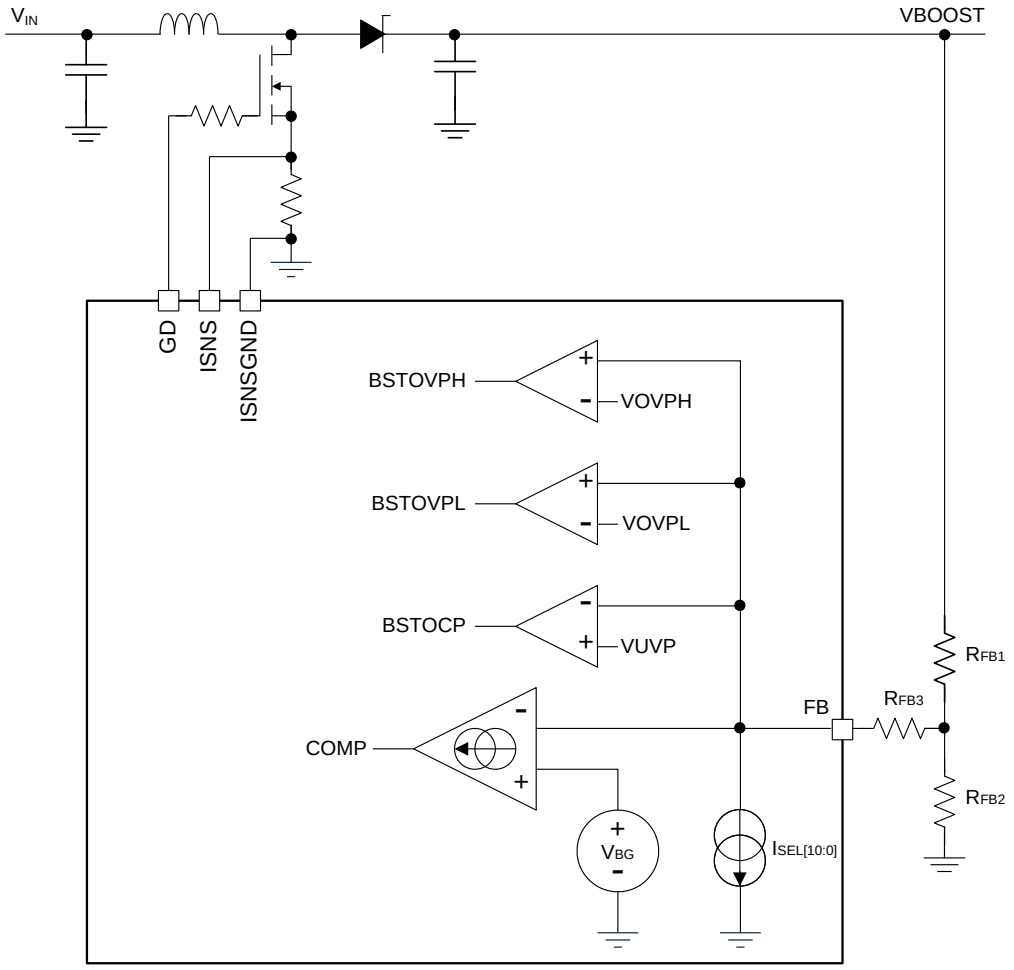


図 13. Three-Resistor FB Divider Circuit

Maximum boost voltage can be calculated with 式 6. The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{MAXBOOST} = \left[\left[\left[\left((I_{SEL\_MAX} \times R_{FB3}) + V_{BG}\right) \times \left(\frac{1}{R_{FB2}}\right)\right] + I_{SEL\_MAX}\right] \times R_{FB1}\right] + (I_{SEL\_MAX} \times R_{FB3}) + V_{BG} \quad (6)$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_{FB2} recommended value is 6 kΩ for boost operation and 10 kΩ for SEPIC operation
- R_{FB3} recommended value is 27 kΩ for boost operation and 30 kΩ for SEPIC operation

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated with 式 7:

$$V_{MINBOOST} = \left(V_{BG} \times \left(\frac{R_{FB1}}{R_{FB2}}\right)\right) + V_{BG} \quad (7)$$

When the boost OVP_LOW level is reached the boost controller stops switching the boost FET, and the BSTOVPL_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold is calculated with 式 8:

$$V_{BOOST\_OVP\_LOW} = \left[\left[\left[\left((I_{SEL\_MAX} \times R_{FB3}) + V_{OVPL}\right) \times \left(\frac{1}{R_{FB2}}\right)\right] + I_{SEL\_MAX}\right] \times R_{FB1}\right] + \left(I_{SEL\_MAX} \times R_{FB3}\right) + V_{OVPL}$$

where

- V_{OVPL} = 1.423 V
- I_{SEL_MAX} = 38.7 µA (8)

When the boost OVP_LOW level is reached the boost controller enters fault recovery mode, and the BSTOVPH_STATUS bit is set. The boost OVP high-voltage threshold is calculated with 式 9:

$$V_{BOOST\_OVP\_HIGH} = \left[\left[\left[\left((I_{SEL\_MAX} \times R_{FB3}) + V_{OVPH}\right) \times \left(\frac{1}{R_{FB2}}\right)\right] + I_{SEL\_MAX}\right] \times R_{FB1}\right] + \left(I_{SEL\_MAX} \times R_{FB3}\right) + V_{OVPH}$$

where

- V_{OVPH} = 1.76 V
- I_{SEL_MAX} = 38.7 µA (9)

When the boost UVP level is reached the boost controller starts a 100-ms OCP counter. The LP8863-Q1 device enters the fault recovery mode and sets the BSTOCP_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage is calculated with 式 10:

$$V_{BOOST\_UVP} = \left[\left[\left[\left((I_{SEL\_MAX} \times R_{FB3}) + V_{UVP}\right) \times \left(\frac{1}{R_{FB2}}\right)\right] + I_{SEL\_MAX}\right] \times R_{FB1}\right] + \left(I_{SEL\_MAX} \times R_{FB3}\right) + V_{UVP}$$

where

- V_{UVP} = 0.886 V
- I_{SEL_MAX} = 38.7 µA (10)

8.3.2.2 Boost Sync and Spread Spectrum

The boost controller can be clocked by an external BST_SYNC signal. If the external synchronization clock disappears the boost continues operation at the frequency defined by RBST_FSET resistor. If the external sync clock disappears while the SYNC pin level is low the boost continues operation without spread spectrum. If the external sync clock disappears, and BST_SYNC pin remains high the boost initially stops switching for approximately 256 µs and then begins switching with spread spectrum enabled.

If using the external BST_SYNC input, the external frequency must be between 1.2 and 1.5 times higher than the frequency defined by the R_{BST_SET} resistor.

The boost converter has also an internal spread spectrum function that reduces EMI noise around the switching frequency and its harmonic frequencies. The internal spread spectrum function modulates the boost frequency ±3% from the central frequency with a 1.875-kHz modulation frequency. The spread-spectrum function cannot be used when an external synchronization clock is used.

表 3. Boost Synchronization Mode

BST_SYNC PIN LEVEL	BOOST CLOCK MODE
Low (GND)	Spread spectrum disabled
High (VDDIO)	Spread spectrum enabled
300-kHz to 2200-kHz clock frequency	Spread spectrum disabled, external synchronization mode

8.3.2.3 Boost Output Discharge

When the boost is disabled, the discharge pin typically sinks 30-mA current in order to discharge the boost output voltage. The boost voltage discharge time depends on output capacitance. The discharge function is enabled for a maximum of 400 ms or until the output voltage falls below 3.3 V. The discharge state is entered when the EN pin goes low. If VDD falls below the power-on reset (POR) level, the LP8863-Q1 device exits the discharge state early and immediately enters the shutdown state. If the discharge feature is unused, leave the DISCHARGE pin floating.

8.3.3 2X Charge Pump

An integrated 2X charge pump can be used to supply the gate drive for the external FET of the boost controller. The charge pump is enabled or disabled by automatically detecting the presence of the external C_{2X} capacitor. If V_{DD} is < 4.5 V then use the charge pump to generate a high-enough gate voltage to drive the external boost switching FET. To use the charge pump, a 2.2-µF cap is placed between C1N and C1P. If the charge pump is not required, C1N and C1P must be left unconnected and CPUMP pins tied to VDD. A 10-µF C_{PUMP} capacitor is used to store energy for the gate driver. The C_{PUMP} capacitor is required to be used in both charge pump enabled and disabled conditions and must be placed as close as possible to the CPUMP pins. 図 14 and 図 15 show required connections for both use cases.

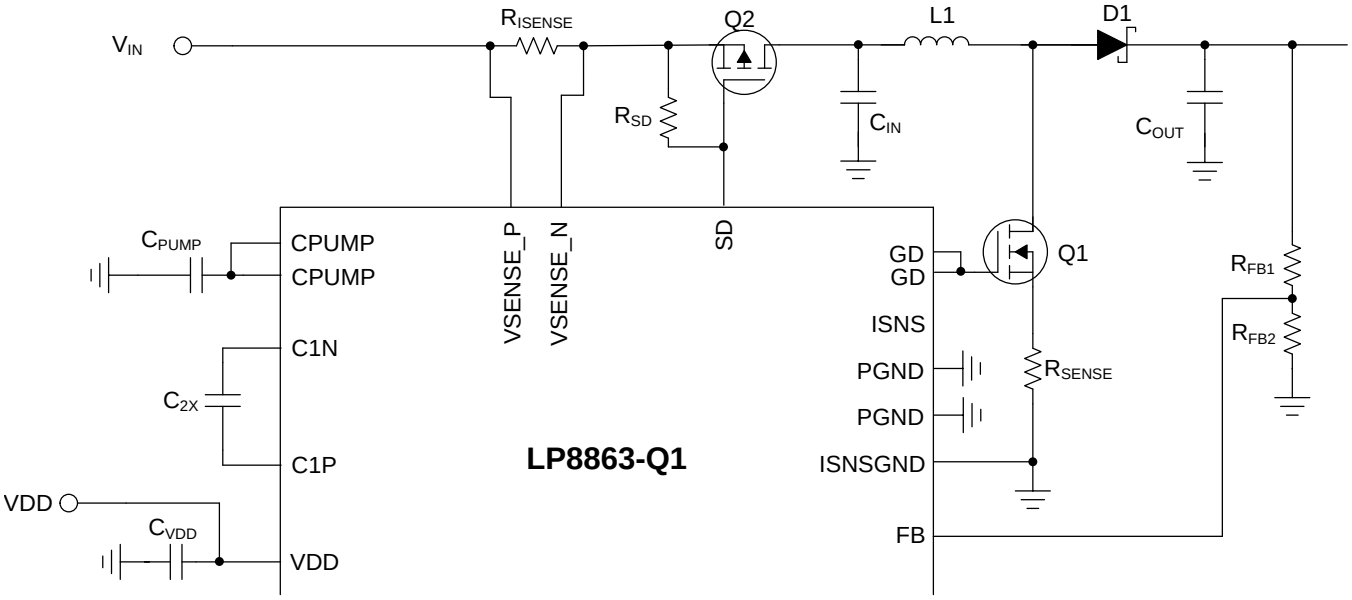


図 14. Charge Pump Enabled Circuit

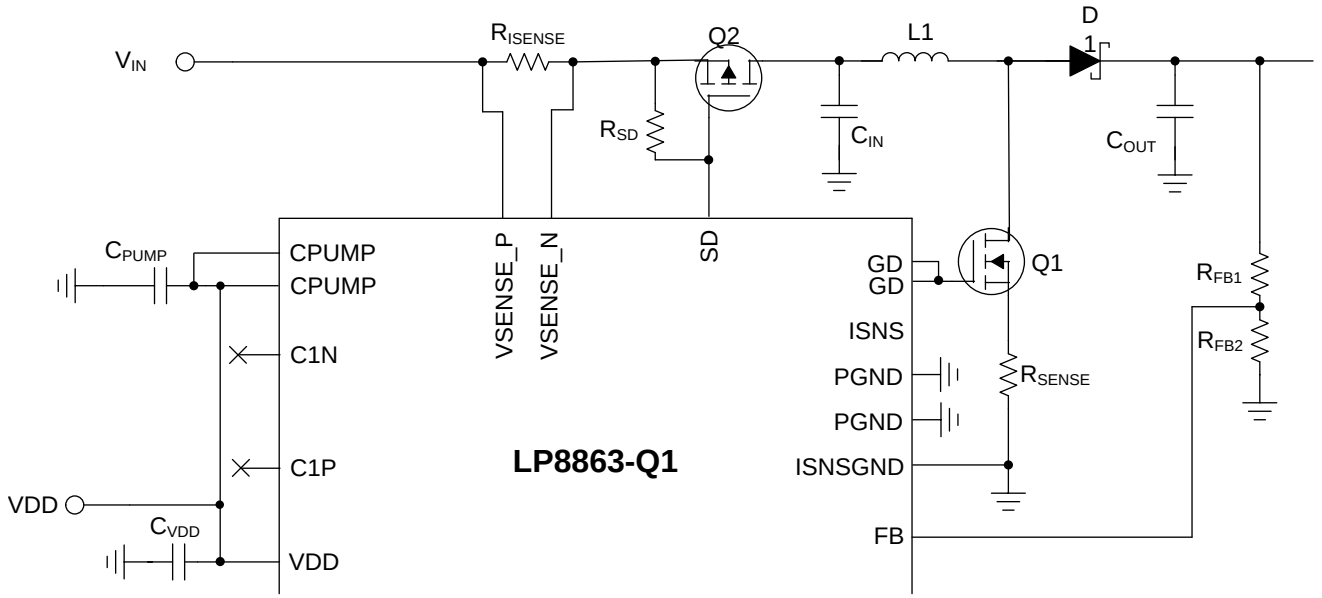


図 15. Charge Pump Disabled Circuit

The C2X_STAT status bit shows whether a C_{2X} capacitor was detected. The C2X_INT bit shows status of any charge pump faults and generates a INT signal. The C2X_INT bit can be used to prevent the charge-pump fault from causing an interrupt on the INT pin signal.

8.3.4 1.8-V LDO

The internal LDO regulator converts the input voltage at VDD to a 1.8-V output voltage at VLDO pin. The LDO regulator supplies internal circuitry. Bypass LDO with a ceramic capacitor of at least 4.7-µF capacitance to ground. Place capacitor as close as possible to the VLDO pin.

8.3.5 LED Current Sinks

8.3.5.1 LED Output Current Setting

The maximum output LED current is set by an external resistor value. The LEDx_CURRENT[11:0] registers can also be used to individually adjust each string's current down from this maximum. The default value for all the LEDx_CURRENT[11:0] registers is the maximum (4095). 式 11 is used to calculate the current setting of an individual string:

$$ILEDx = \frac{1.21\,V}{R_{ISET}} \times 2560 \times \frac{LEDx\_CURRENT[11:0]}{4095} \quad (11)$$

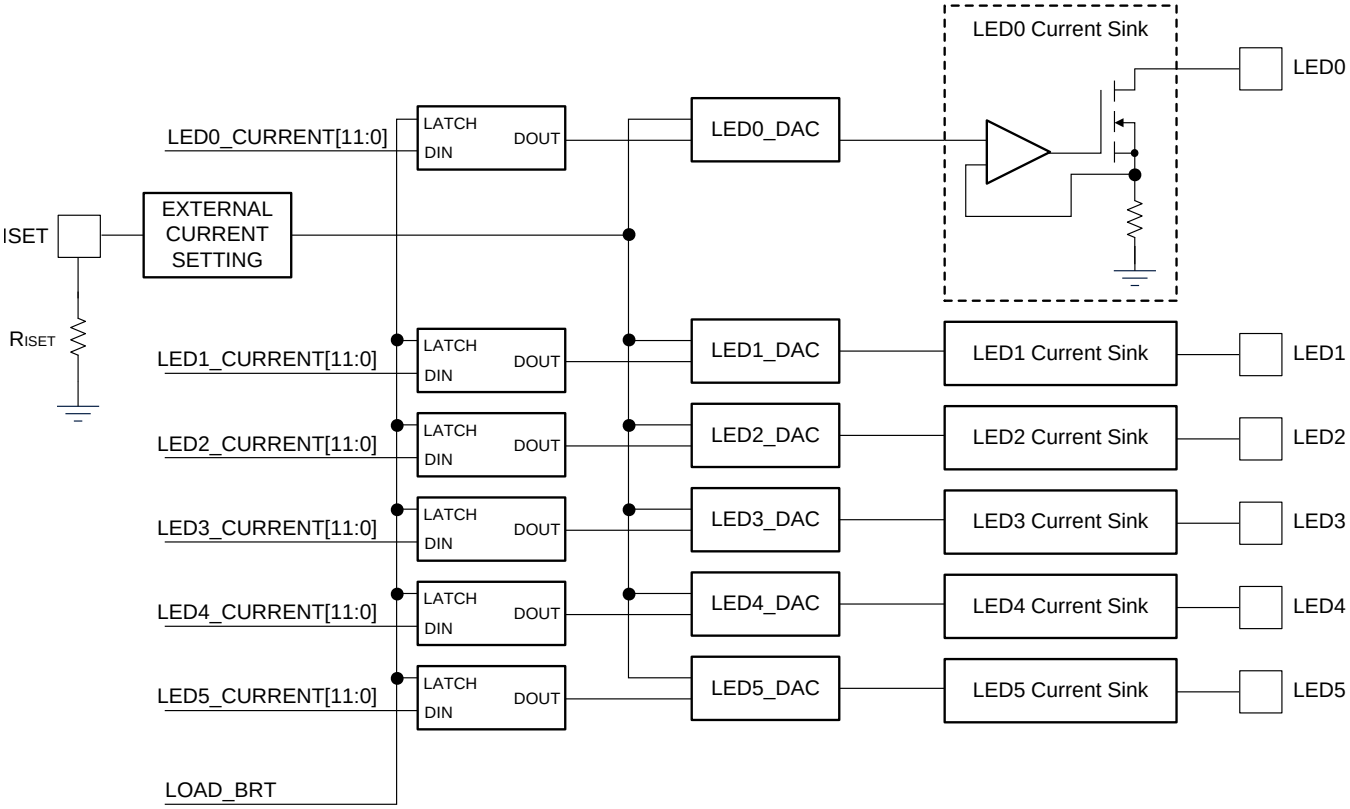


図 16. LED Driver Current Setting Circuit

The LEDx_CURRENT[11:0] registers updates are also latched by the LOAD_BRT_DB register similar to the individual brightness registers. This is done so all LED currents can be updated simultaneously. The default value for all the LEDx_CURRENT[11:0] registers is FFFh.

8.3.5.2 LED Output PWM Clock Generation

The LED PWM frequency is asynchronous from the input PWM frequency. The LED PWM frequency is generated from the internal 20-MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531 kHz. The PWM dimming resolution is highest when the lowest PWM frequency is used. The PWM_FSET resistor determines the LED PWM frequency based on 表 4. PWM resolution in 表 4 is with PWM dither disabled.

表 4. LED PWM Frequency Selection

R_PWM_FSET (kΩ)	LED PWM FREQUENCY (Hz)	PWM DIMMING RESOLUTION (bits)
3.92	152	16 (maximum)
4.75	305	16
5.76	610	15
7.87	1221	14
11	2441	13
17.8	4883	12
42.2	9766	11
140	19 531	10

8.3.5.3 LED Output String Configuration

The six LED driver channels of the LP8863-Q1 device can automatically support applications using six, five, four, three, and two LED strings. The driver channels can also be tied together in groups of two, three, or six channels. This allows the LP8863-Q1 device to drive three 300-mA LED strings, two 450-mA LED strings, or one 900-mA LED string. The LED strings are always appropriately phase shifted for their string configuration. This reduces the ripple seen at the boost output, which allows smaller output capacitors and reduces audible ringing in the capacitors. Phase shift increases the load frequency, which can move potential capacitor noise above the audible band while still keeping PWM frequency low to support a higher dimming ratio.

When the LP8863-Q1 device is first powered on the string configuration is automatically detected and the phases of each channel configured. The LED string configuration must not be changed unless the LP8863-Q1 is powered off in shutdown state. The string configurations in 表 5 are valid configurations for auto detection. Any other detected configuration defaults to *6 channel / 60 degree* mode. The detected string configuration can be read from the LED_STRING_CONF[2:0] register. Tie unused LEDx pins to ground.

表 5. LED Output String Configuration

CONFIGURATION	LED0	LED1	LED2	LED3	LED4	LED5	AUTOMATIC PHASE SHIFT
6 channels	150 mA	150 mA	150 mA	150 mA	150 mA	150 mA	60°
5 channels	150 mA	150 mA	150 mA	150 mA	150 mA	(Tied to GND)	72°
4 channels	150 mA	150 mA	150 mA	150 mA	(Tied to GND)	(Tied to GND)	90°
3 channels	150 mA	150 mA	150 mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	120°
2 channels	150 mA	150 mA	(Tied to GND)	(Tied to GND)	(Tied to GND)	(Tied to GND)	180°
3 channels, 300 mA /channel (tie LED pins together)	300 mA		300 mA		300 mA		120°
2 channels, 450 mA /channel (tie LED pins together)	450 mA			450 mA			180°
1 channel, 900 mA (tied LED pins together)	900 mA						None

8.3.5.3.1 Independent Cluster Brightness Control Mode

The LP8863-Q1 supports a cluster mode like that found in the LP8860-Q1 LED driver. This mode allows the brightness of each of the six driver channels to be controlled independently using the I2C or SPI interface. This is done by using the six CLUSTER_BRTx[15:0] registers, the six LEDx_GROUP registers and the LED_EXT_SUPPLY[5:0] register.

The LEDx_GROUP registers select which CLUSTER_BRTx or DISP_BRT register is used for each of the six LED driver channels. The LED_EXT_SUPPLY[5:0] register selects which channels are used by the adaptive boost voltage control loop. This allows the LP8863-Q1 to drive LED strings that powered with either the integrated boost controller or external supply. If a LED driver channel is driving a string powered from the boost then its corresponding LED_EXT_SUPPLY bit should be set to zero. By default all LED_EXT_SUPPLY bits are 0, and all LEDx_GROUP bits are 000.

An example of how the registers would be configured if the application calls for a display backlight with 4 strings and uses the remaining 2 current sinks to drive indicator LEDs where anodes are supplied externally (not from the boost of the LP8863-Q1 device) follows:

LED_EXT_SUPPLY[5:0] = 11000b	(LED5 and LED4 use external supply)
LED0_GROUP = 000b	(LED0 uses DISP_BRT register)
LED1_GROUP = 000b	(LED1 uses DISP_BRT register)
LED2_GROUP = 000b	(LED2 uses DISP_BRT register)
LED3_GROUP = 000b	(LED3 uses DISP_BRT register)
LED4_GROUP = 100b	(LED4 uses CLUSTER_BRT4 register)
LED5_GROUP = 101b	(LED5 uses CLUSTER_BRT5 register)

8.3.6 Brightness Control

The LP8863-Q1 supports global or individual brightness control for each LED string through individual PWM duty cycle control of the LED0 to LED5 driver channels via I2C/SPI registers. An internal 20-MHz clock is used for generating PWM outputs.

8.3.6.1 Brightness Control Signal Path

One display brightness path and five individual brightness paths can be used to control the LED driver channel brightness. The LEDx_GROUP registers select whether the display brightness path or the cluster 1 to 5 brightness paths control each LED output. The BRT_MODE register selects whether the input to the display brightness path is the PWM input pin or DISP_BRT register. The brightness control signal path diagram is shown in 図 17.

The display brightness path has sloper and hybrid dimming functions that can be enabled. By default the sloper function is enabled and hybrid dimming function disabled. Both functions can be controlled using the I2C or SPI interface. The sloper function is described in *Sloper* and hybrid dimming is described in *Hybrid Dimming*.

By default the LP8863-Q1 operates with LED0 to LED5 channels controlled by the display brightness path. To enable individual LED string brightness control the LEDx_GROUP registers must be reconfigured with the SPI/I2C interface.

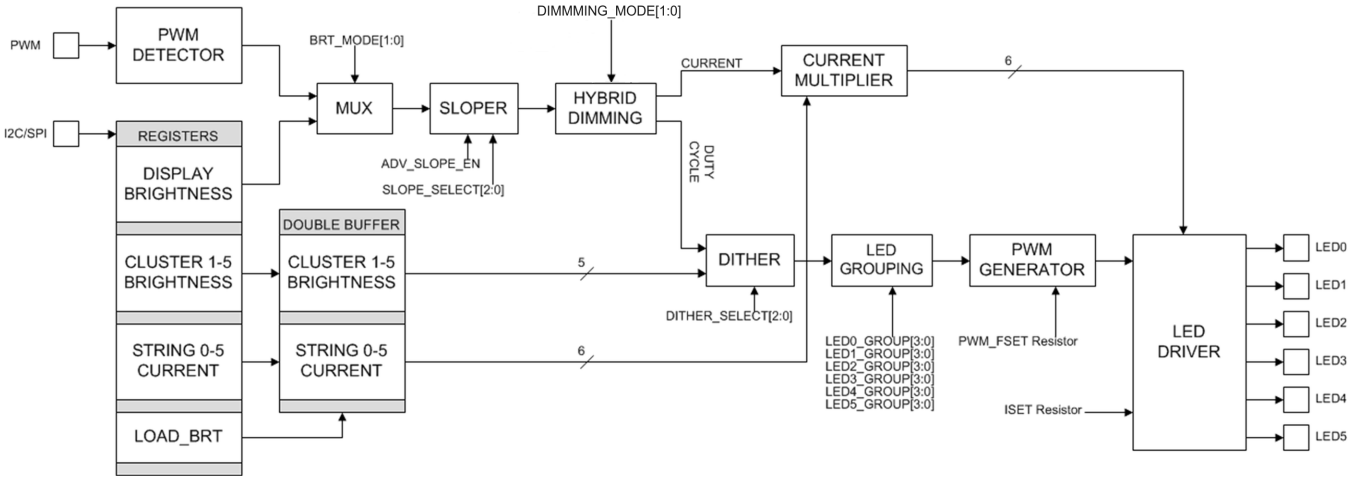


図 17. LP8863-Q1 Brightness Path Diagram

8.3.6.2 Hybrid Dimming

In addition to pure PWM dimming, LP8863-Q1 supports a hybrid-dimming mode. Hybrid dimming combines PWM and current modes for brightness control for the display brightness path. In hybrid mode PWM dimming is used for the low range of brightness, and current dimming is used for high brightness levels as shown in 図 18. Current dimming control enables improved optical efficiency due to increased LED efficiency at lower currents. PWM dimming control at low brightness levels ensures linear and accurate control.

Hybrid mode can be enabled with the DIMMING_MODE bit in USER_CONFIG1 register. The PWM and current modes transition threshold can be set at 12.5% or at 0% brightness with the DIMMING_MODE bits. The latter selection allows for pure current dimming control mode.

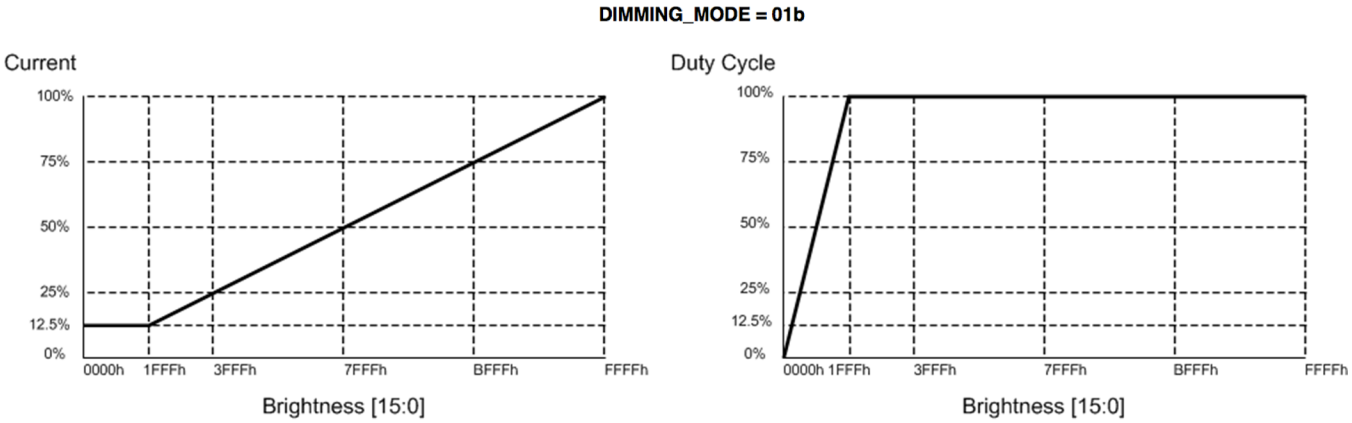


図 18. 12.5% PWM and Current Hybrid Dimming Diagram

8.3.6.3 Sloper

An optional sloper function makes the transition from one brightness value to another optically smooth. By default the advanced sloper is enabled with a 200-ms linear sloper duration. Transition time between two brightness values is programmed with the SLOPE_SELECT[2:0] bits (when 000, sloper is disabled). With advanced sloper enabled the brightness changes are further smoothed to be more pleasing to the human eye. Advanced slope is enabled with ADV_SLOPE_ENABLE register bit.

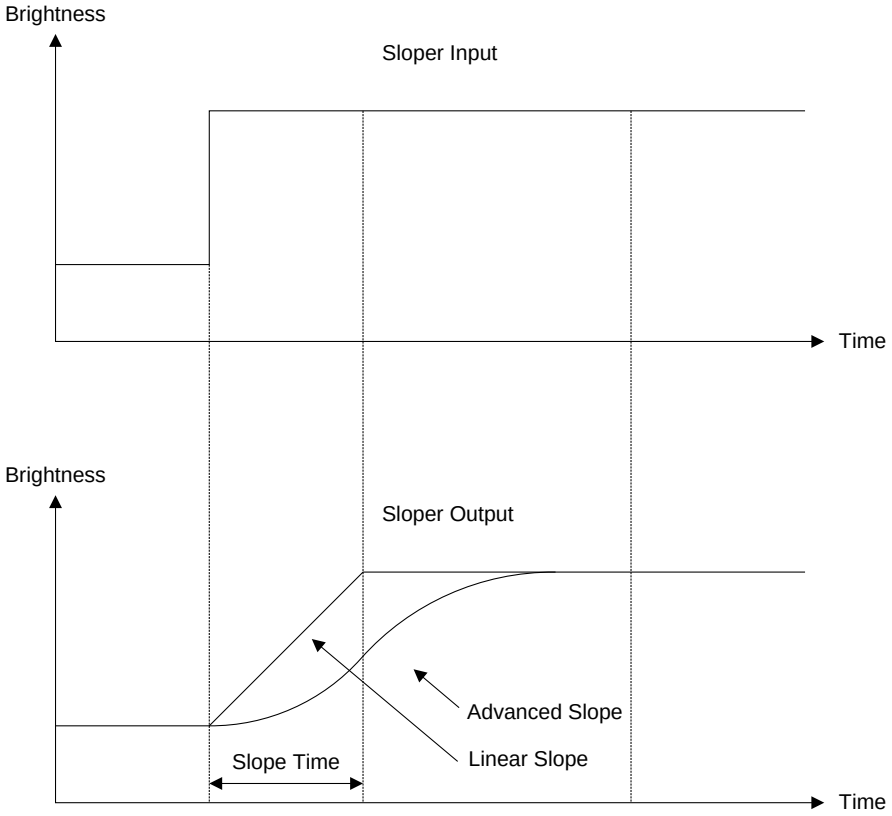


図 19. Brightness Sloper

8.3.6.4 Dither

The number of brightness steps when using LED output PWM dimming is equal to the 20-MHz oscillator frequency divided by the LED PWM frequency (set by PWM FSET resistor). The PWM duty cycle dither is a function the LP8863-Q1 uses to increase the number of brightness dimming steps beyond this oscillator clock limitation. The dither function modulates the LED driver output duty cycle over time to create more possible average brightness levels. The DITHER_SELECT[2:0] register bits control the level of dither, disabled, 1, 2, or up to 5 bits using the I2C or SPI interface. By default the dither has 3 bits enabled (default 011b).

When the 1-bit dither is selected, the width of every second PWM pulse is increased by one LSB (one 20-MHz clock period). When the 3-bit dither is selected, within a sequence of 8 PWM periods the number of pulses with increased length varies: dither value 000 - all 8 pulses at default length; 001 - one of the 8 pulses is longer; 010 - two of the 8 pulses are longer, etc., until at 111 seven of the 8 pulses have increased length. 図 20 shows one example of PWM output dither.

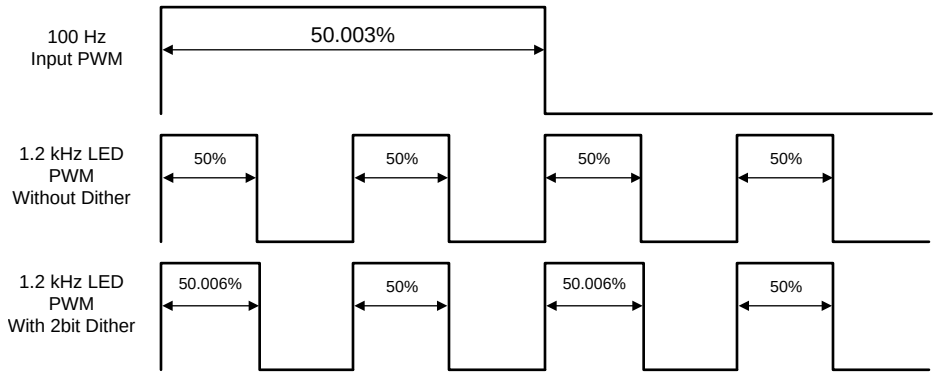


図 20. PWM Dither Example

The dither block also has an additional mode at low brightness levels when LED PWM duty cycle is less than the minimum pulse width (that is, less than the LED driver rise time). In this mode the dither block skips full PWM pulses to reduce the brightness further enabling very high dimming modes. The end result is the LED PWM frequency is reduced as more and more minimum pulses are skipped or dithered out. This function can be enabled using the I2C or SPI interface by programming the EN_MIN_PWM_LIMIT bit to 1. 図 21 shows how the 2-bit minimum brightness dithering works.

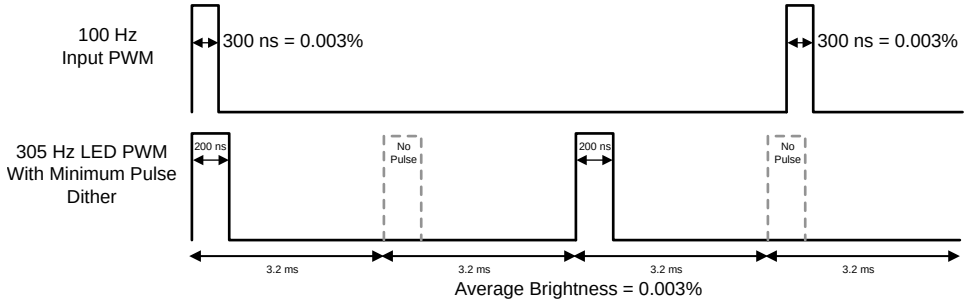


図 21. Minimum Brightness Dither Example

8.3.7 Die Temperature Read-Out and Thermal Window Detector

The LP8863-Q1 has two internal thermal sensors: one for protection purposes (device thermal shutdown) and one for die temperature monitoring. The die temperature monitor block includes a 9-bit ADC to convert the analog thermal-sensor output to a temperature reading available in the register JUNCTION_TEMPERATURE. First temperature result is available 2 ms after the activation of the block and conversion rate is 10 Hz. When the temperature monitor block is disabled register JUNCTION_TEMPERATURE content is –256°C.

The die temperature monitor also includes a thermal window detector. The TEMPERATURE_LIMIT_HIGH and TEMPERATURE_LIMIT_LOW bits set the high and low limits for the thermal window. These thresholds have ±1°C hysteresis: TEMPERATURE _LIMIT_HIGH + 1°C for increasing and TEMPERATURE_LIMIT_HIGH – 1°C for decreasing, for example. If the die temperature increases above the high limit or reduces below the low limit, a fault interrupt is generated. Die temperature monitor (ADC, thermal sensor, and window detector) can be disabled to minimize power dissipation in STANDBY mode. The thermal sensor for TSD is always active.

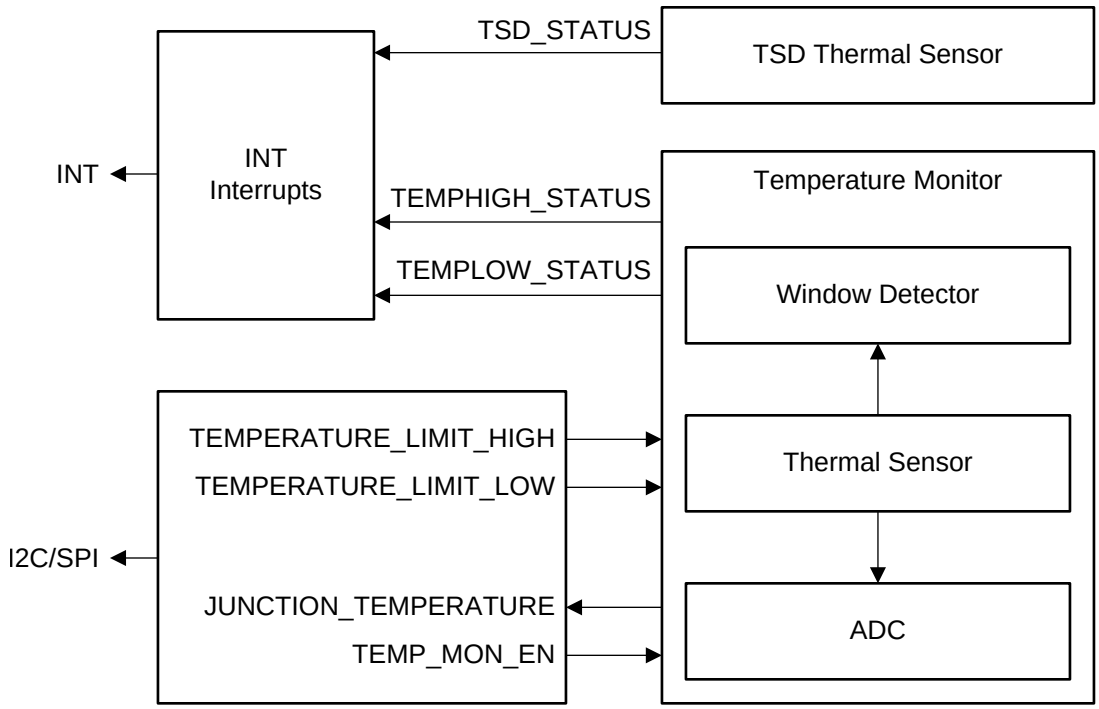


図 22. Thermal Shutdown and Sensor Block Diagram

図 23, 図 24, and 図 25 show the INT pin and status behaviors of the TSD, temperature high, and temperature low limits.

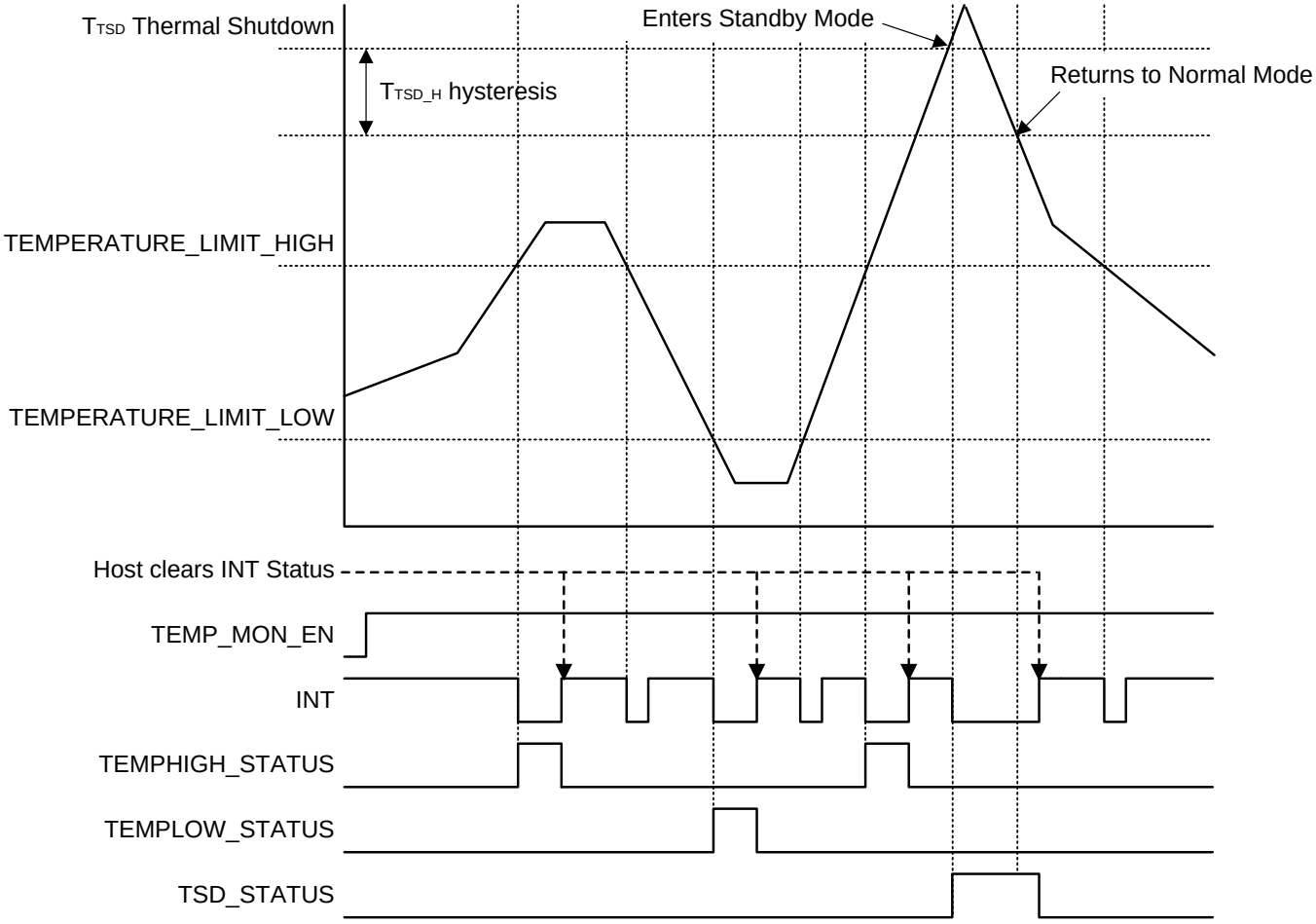


図 23. Thermal Shutdown and Sensor Example 1

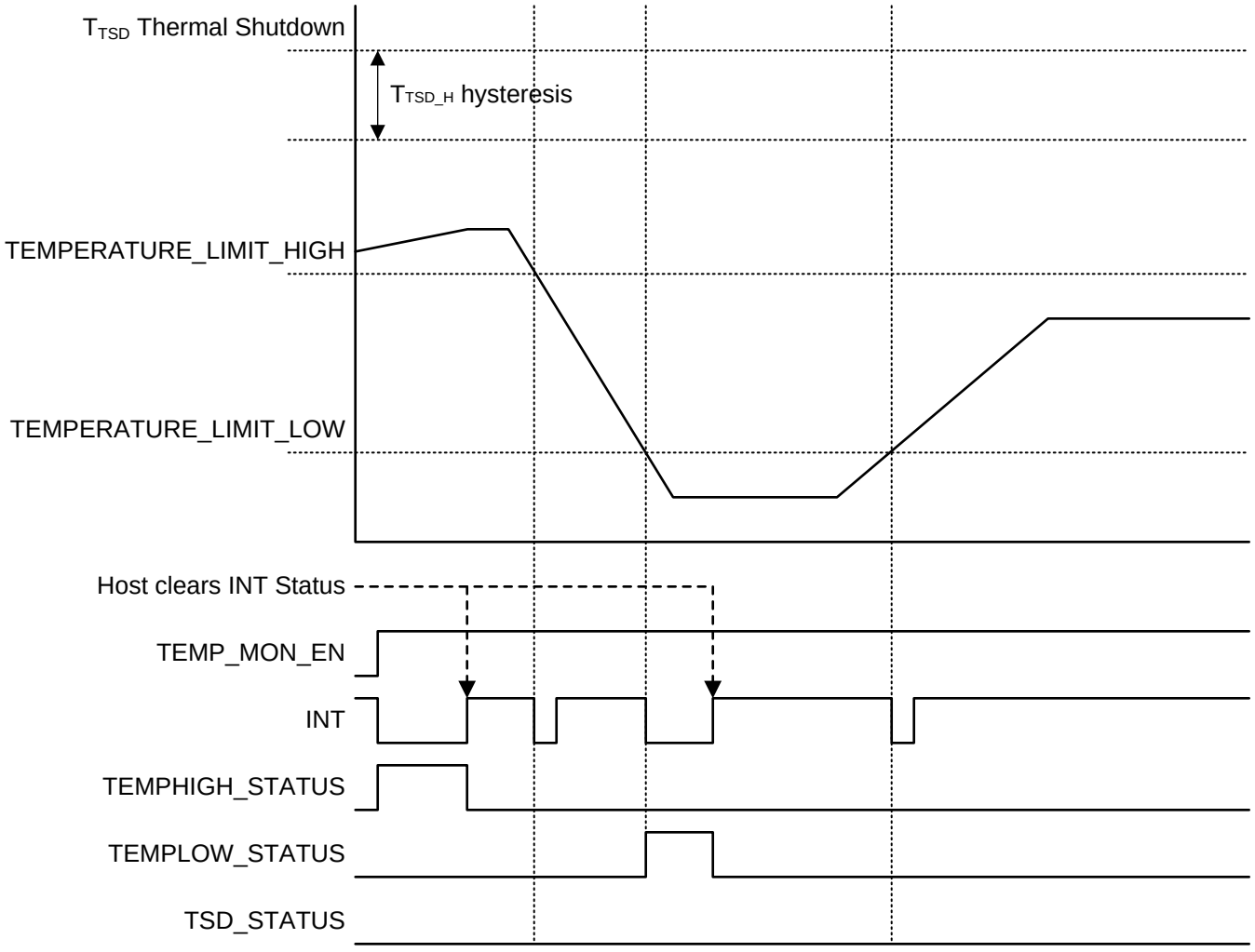


図 24. Thermal Shutdown and Sensor Example 2

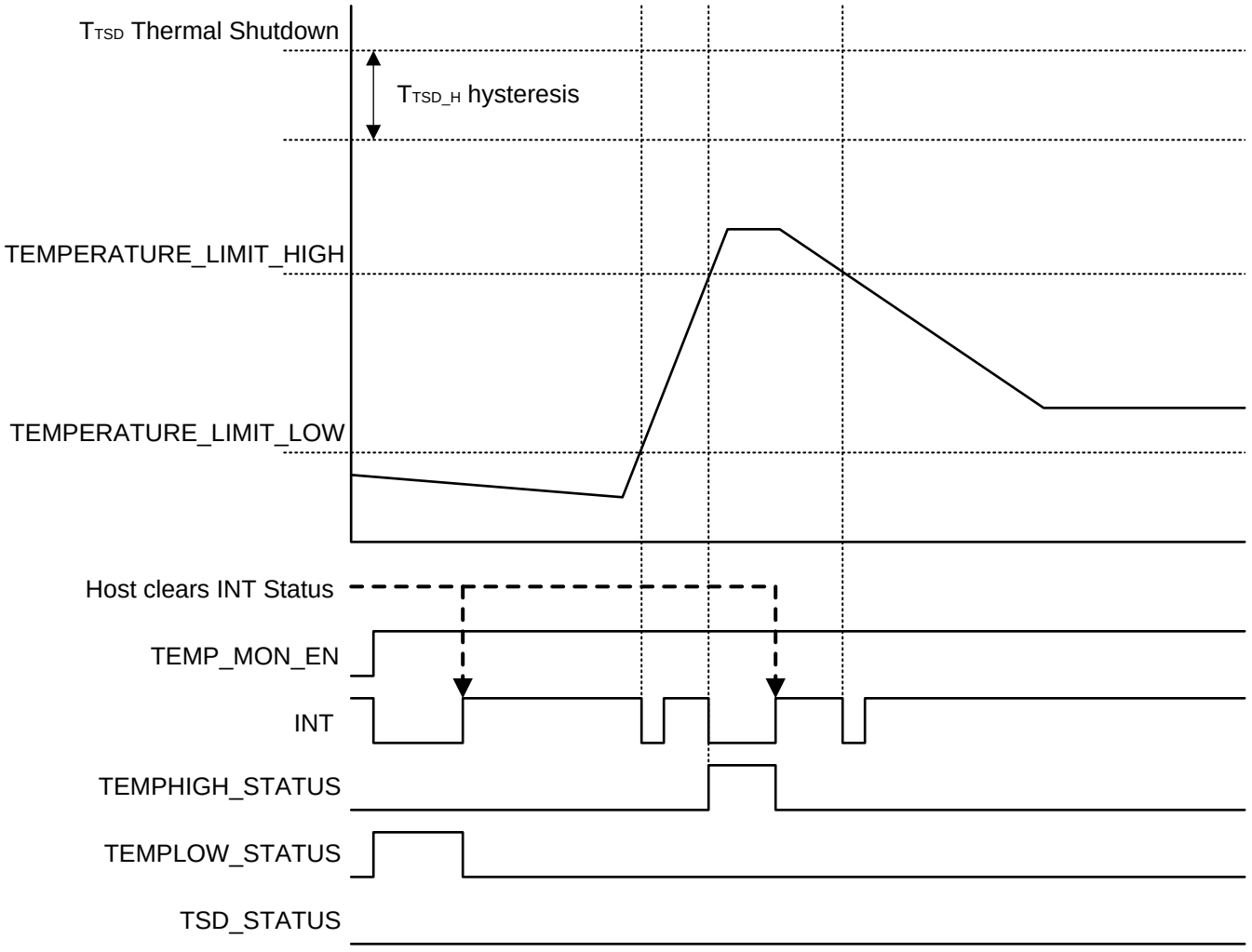


図 25. Thermal Shutdown and Sensor Example 3

8.3.8 Protection and Fault Detections

The LP8863-Q1 device includes fault detections for LED open and short conditions, boost input undervoltage, overvoltage and overcurrent, boost output overvoltage and overcurrent, VDD undervoltage and die overtemperature. Host can monitor the status of the faults in INTERRUPT_STATUS_1 and INTERRUPT_STATUS_2 registers.

8.3.8.1 LED Faults

During normal boost operation, boost voltage is raised if any of the LED outputs falls below the low headroom threshold level. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled. Any LED fault sets the status bit LED_STATUS and an interrupt is generated unless LED interrupt is disabled. Reason for the open LED faults can be read from bits OPEN_LED and LEDx_FAULT (x = 0...5, indicating the faulty LED) in INTERRUPT_STATUS_2 register. These bits maintain their value until device power-down while the LED_STATUS bit is cleared by the interrupt clearing procedure. If a new LED fault is detected, LED_STATUS is set and an interrupt generated again.

Shorted LED fault is detected if one or more LED outputs are above the SHORTED_LED_THRESHOLD setting and at least one LED output is inside the normal operation widow (see 図 26). Shorted string is disconnected from the boost adaptive control loop and the LED PWM output is disabled. LED_STATUS status bit is set and an interrupt generated similarly as in open LED case. Shorted LED fault reason can be read from bits SHORT_LED and LEDx_FAULT (x = 0...5, indicating the faulty LED) in INTERRUPT_STATUS_2 register.

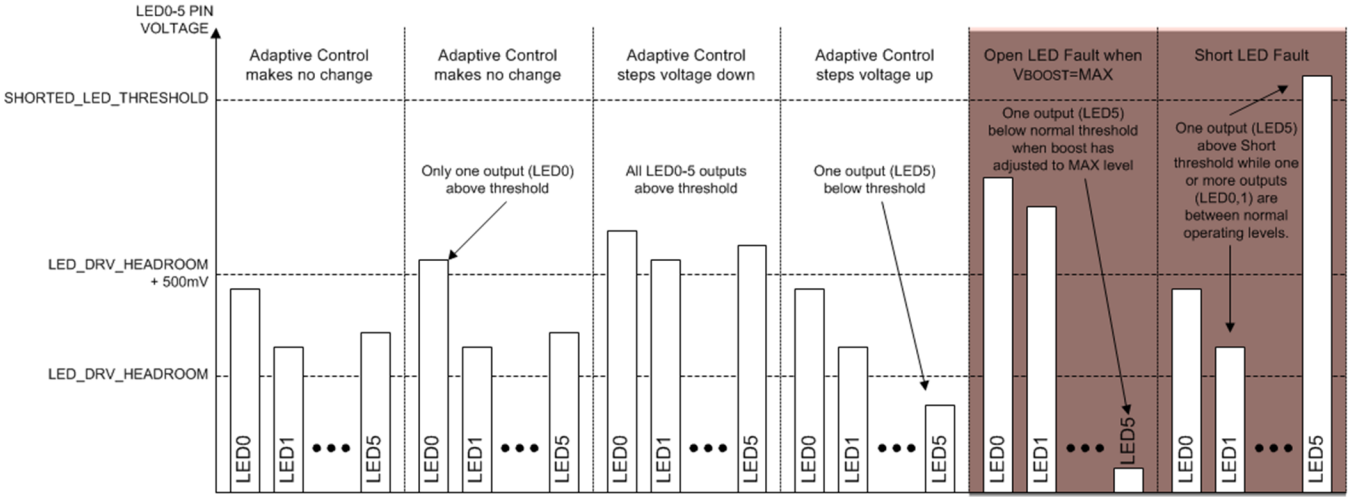


図 26. LED Open and Short Detection Logic

8.3.8.2 Boost Faults

Boost overvoltage is detected if the FB pin voltage exceeds the V_{OVPL} threshold. When boost overvoltage is detected, BSTOVPL_STATUS bit is set in the INTERRUPT_STATUS_1 register. The boost FET stops switching, and the output voltage is automatically limited. If the BSTOVPL_STATUS bit is continually set (that is, reappears after clearing), it may indicate an issue in the application. Boost overvoltage low is monitored during device normal operation (ACTIVE mode).

A second *boost overvoltage high* fault is detected if the FB pin voltage exceeds the V_{OVPH} threshold. The LP8863-Q1 device enters the fault recovery state to protect against excessive thermal dissipation caused by high headroom on the LED drivers. When boost overvoltage is detected, BSTOVPH_STATUS bit is set in the INTERRUPT_STATUS_1 register. A fault interrupt is also generated. If the BSTOVPH_STATUS bit is continually set (that is, reappears after clearing), it may indicate an issue in the application. Boost overvoltage high is monitored during device normal operation (ACTIVE mode).

Boost overcurrent is detected if the FB pin voltage drops below the V_{UVP} threshold. A boost OCP fault is detected if the undervoltage condition persists for longer than 110 ms. If the boost overcurrent timer expires before the output voltage recovers, the BSTOCP_STATUS bit is set in the INTERRUPT_STATUS_1 register. The fault recovery state is entered, and a fault interrupt is generated. If the BSTOCP_STATUS bit is permanently set, it may indicate an issue in the application. Boost overcurrent is monitored from the boost start, and fault may trigger during boost start-up.

8.3.8.3 Power-Line Faults

If during operation of the LP8863-Q1 device the V_{IN} (VSENSE_P pin) voltage falls below the VINUVLO falling level, the boost, LED outputs, and power-line FET are turned off, and the device enters STANDBY mode. The VINUVLO_STATUS bit is also set, and the INT pin is triggered. When the VINUVLO voltage rises above the rising threshold level the LP8863-Q1 device exits STANDBY and begins the start-up sequence.

If during LP8863-Q1 device operation V_{IN} (VSENSE_P pin) voltage rises above the VINOVP rising level, boost, LED outputs, and power-line FET are turned off, and the device enters STANDBY mode. The VINOVP_STATUS bit is also set, and the INT pin is triggered. When the VINOVP voltage falls below the falling threshold level the LP8863-Q1 exits STANDBY and begins the start-up sequence.

The VIN OCP protection detects overcurrent by measuring voltage of the R_{ISENSE} resistor connected between VSENSE_P and VSENSE_N pins. VIN OCP sensing begins once the LP8863-Q1 enters the PL FET soft-start state. Fault is detected if overcurrent condition duration lasts for at least 10 μs, minimum. The VINOCP_STATUS bit is also set, and the INT pin is triggered. To trip at a lower current limit a larger sense resistor can be used to create a 220-mV voltage difference across the sense resistor.

8.3.8.4 VDD Undervoltage Fault

If during LP8863-Q1 device operation VDD falls below VDDUVLO falling level, boost, PL FET, and LED outputs are turned off, and the device enters STANDBY mode. The VDDUVLO_STATUS fault bit is set, and the INT pin is triggered. The LP8863-Q1 recovers automatically to ACTIVE mode when VDD rises above VDDUVLO rising threshold.

If VDD falls below VPOR the LP8863-Q1 device enters SHUTDOWN mode.

8.3.8.5 Thermal Shutdown

If the die temperature of LP8863-Q1 reaches the thermal shutdown threshold T_{TSD}, the boost, PL FET, and LED outputs on LP8863-Q1 device shut down to protect the device from damage. Fault status bit TSD_STATUS bit is set, and the INT pin is triggered. The device restarts the PL FET, the boost, and LED outputs when temperature drops by T_{TSD_H} amount.

8.3.8.6 Overview of the Fault/Protection Schemes

FAULT NAME	STATUS BIT	CONDITION	TRIGGER FAULT INTERRUPT	ENTER FAULT RECOVERY	ACTION
Boost overcurrent	BSTOCP_STATUS	FB pin voltages falls below V_{UVP} level for > 110 ms	Yes	Yes	Device goes to standby and then attempts to restart 200 ms after fault occurs.
Boost overvoltage low	BSTOVPLOW_STATUS	FB pin voltages rises above V_{OVPL} level	No	No	Boost stops switching until boost voltage level falls. The device remains in normal mode with LED drivers operational.
Boost OVP high	BSTOVPH_STATUS	FB pin voltages rises above V_{OVPH} level	Yes	Yes	Device goes to standby and waits until output voltage falls below threshold before restarting.
Boost sync clock invalid	BSTSYNC_STATUS	Device is enabled while a valid external SYNC clock is running. Then SYNC stops or changes to invalid frequency. Valid range is 1.2× to 1.5× of frequency selected by BST_FSET resistor.	No	No	Device defaults to internal clock frequency selected by BST_FSET resistor. If SYNC input is held high then spread spectrum is enabled. If SYNC input is held low then spread spectrum is disabled.
V_{IN} overvoltage	VINOVP_STATUS	V_{IN} voltage rises above 43 V.	Yes	No	Device goes to standby and waits until output voltage falls below threshold before restarting.
V_{IN} undervoltage	VINUVLO_STATUS	V_{IN} voltage falls below 2.8 V.	Yes	No	Device goes to standby and then attempts to restart once the input voltage rises above threshold.
V_{IN} overcurrent	VINOCP_STATUS	Voltage across R_{ISENSE} exceeds 220 mV	Yes	Yes	Device goes to standby and then attempts to restart 200 ms after fault occurs.
V_{DD} undervoltage	VDDUVLO_STATUS	V_{DD} level falls below VDD_{UVLO} threshold.	Yes	No	Device restarts once VDD level rises above VDD_{UVLO} threshold.
Thermal shutdown	TSD_STATUS	Junction temperature rises above T_{TSD} threshold.	Yes	No	Device goes to standby and then attempts to restart once die temperature falls below threshold.
Open LED string	LED_STATUS OPEN_LED	Headroom voltage on one or more channels is below minimum level and boost has adapted to maximum level.	Yes	No	Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle.
Shorted LED	LED_STATUS	Headroom voltage on one or more channels is above the SHORTED_LED_THRESHOLD for > 5 ms while the headroom of at least one channel is still below this threshold.	Yes	No	Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle.
Invalid LED string detected	INVSTRING_STATUS	LED string detection does not match one of 8 valid configurations	Yes	No	Device defaults to six LED string phase shift mode. String detection reoccurs next power cycle.
FSET detection fault	FSET_STATUS	BST_FSET or PWM_FSET are missing or an invalid value	Yes	No	Boost does not start up. Fault is cleared by VDD cycling with correct resistor connection at FSET pin.
Charge pump fault	CP_STATUS	Charge pump voltage level is abnormal.	No	No	Device functions normally, if possible. If charge pump issue is severe, it is likely boost overcurrent fault will trip.

Charge pump components missing	CPCAP_STATUS	Charge pump is missing components.	No	No	Device functions normally, if possible. If charge pump issue is severe, it is likely boost overcurrent fault will trip.

8.4 Device Functional Modes

8.4.1 State Diagram

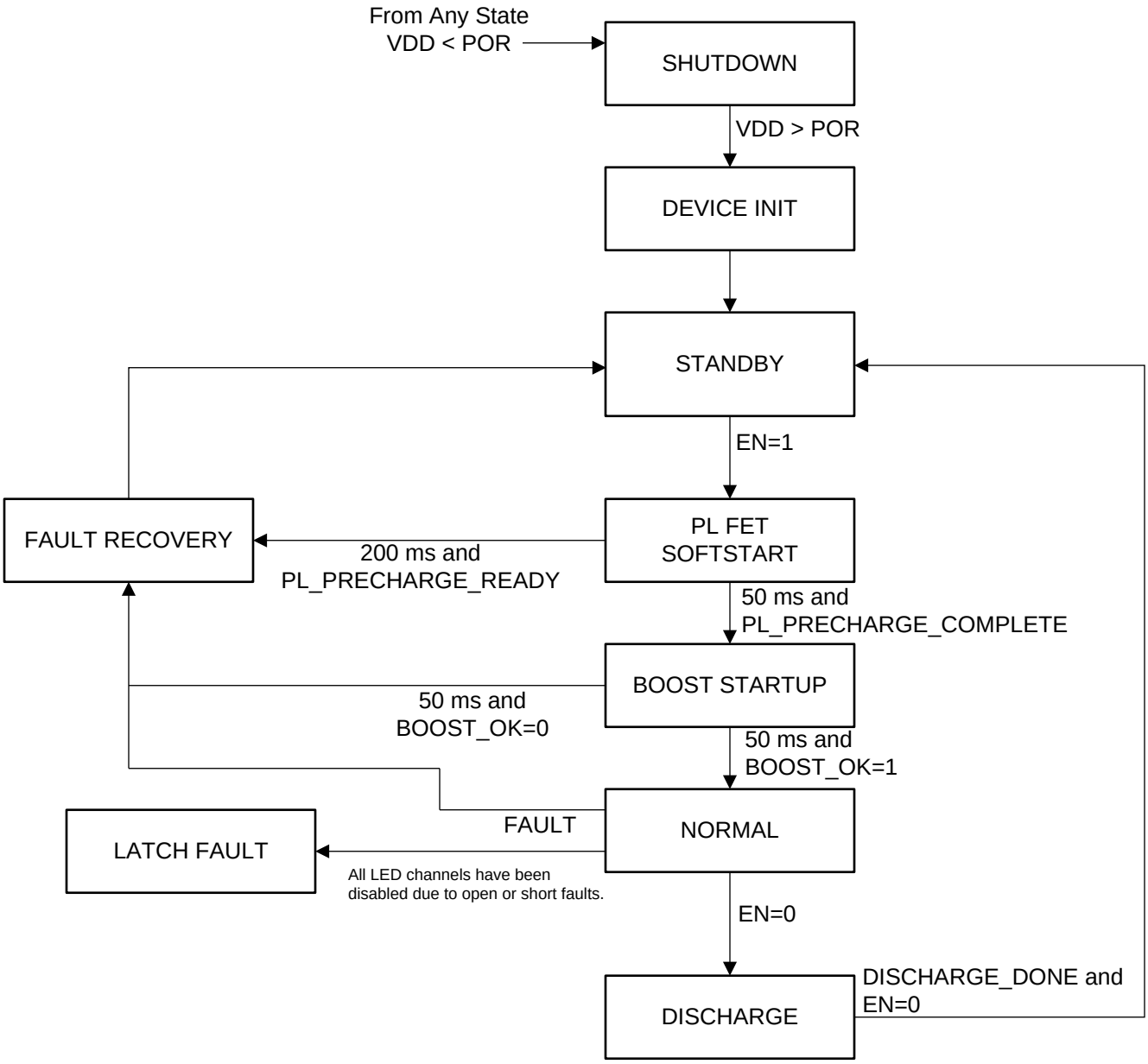


図 27. State Machine Diagram

8.4.2 Shutdown

When VDD is below POR threshold device is in shutdown state.

8.4.3 Device Initialization

After POR is released device initialization begins. During this state the LDO is started up, EEPROM default and trim configurations are loaded, BOOST_FSET and PWM_FSET resistors are detected, and the LED string configuration is detected.

Device Functional Modes (continued)

8.4.4 Standby Mode

In standby the LP8863-Q1 device can be accessed with I2C or SPI to change any configuration registers. Analog blocks are disabled to save power.

8.4.5 Power-line FET Soft Start

Power-line FET is enabled, and boost input and output capacitors are charged to V_{IN} level. V_{IN} faults for OCP, OVP, and UVP are enabled.

8.4.6 Boost Start-Up

Boost voltage is ramped to maximum voltage level with reduced current limit. Start-up exits when boost reaches initial target voltage. All boost faults are now enabled.

8.4.7 Normal Mode

LED drivers are enabled when brightness is greater than zero. All LED faults are active.

8.4.8 Discharge Mode

When EN goes low from normal mode the boost output voltage is discharged. This state exits when boost voltage falls below 3.3 V or when the 400-ms timer expires.

8.4.9 Fault Recovery

Non-LED faults can trigger fault recover state. LED drivers, boost converter, and power-line FET are disabled for 200 ms, and the device attempts to restart from standby mode if EN is still high.

8.4.10 Latch Fault

If all LED strings are disabled due to faults then the LP8863-Q1 enters the latch fault mode. This state can be exited by toggling the VDD pin.

Device Functional Modes (continued)

8.4.11 Start-Up Sequence

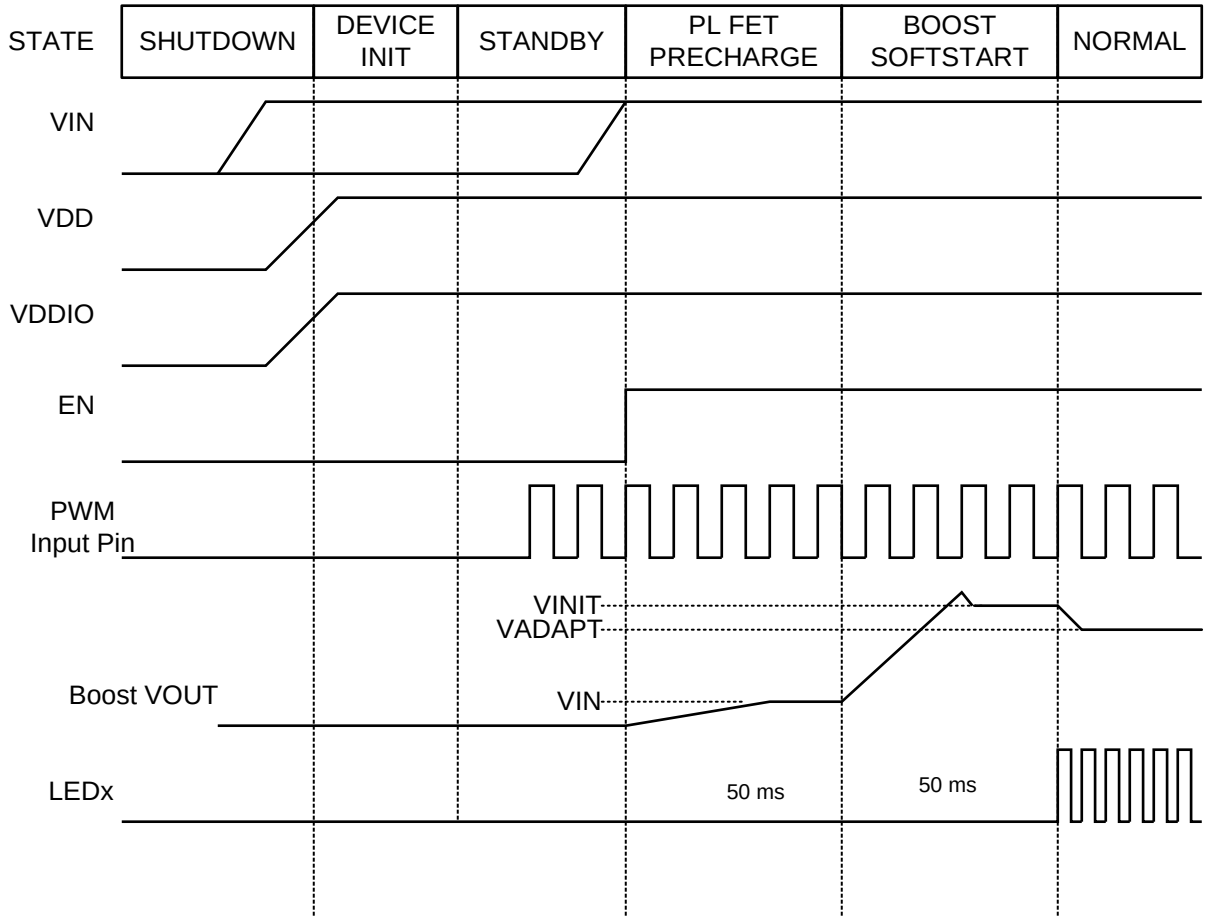


図 28. Start-Up Sequence Diagram

Device Functional Modes (continued)

8.4.12 Shutdown Sequence

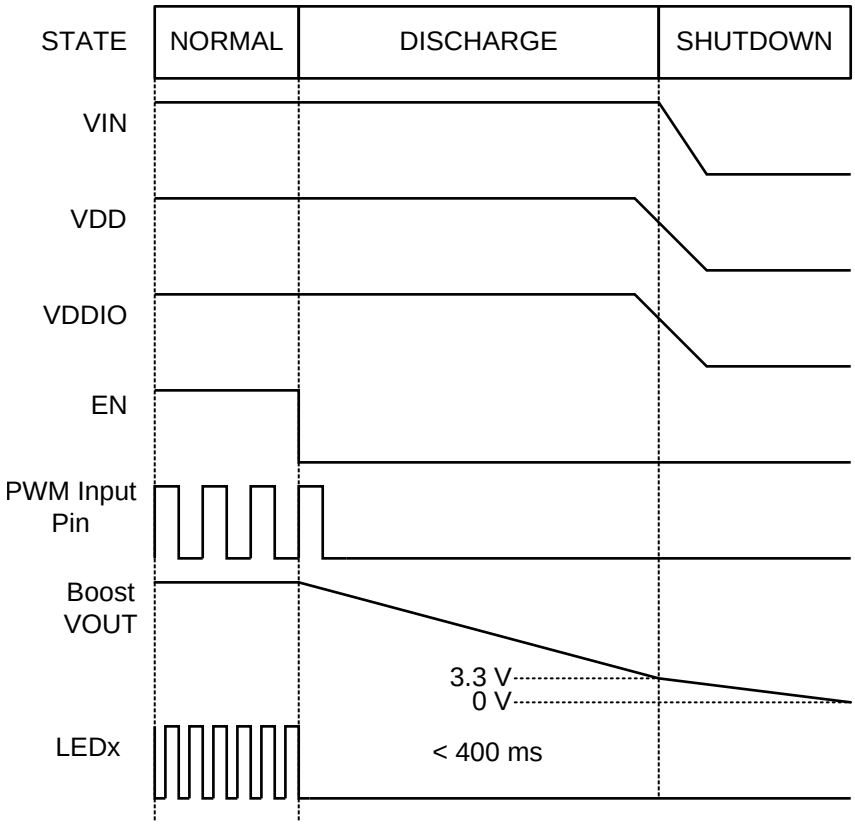


図 29. Shutdown Sequence Diagram

For proper operation of discharge function, pull the EN pin before VDD pin. VIN and VDDIO can be set low any time after EN low.

8.5 Programming

8.5.1 Serial Interface Selection

The serial interface type is selected by connecting the IFSEL pin to VDDIO or GND. The LP8863-Q1 device checks the IFSEL pin state as part of device startup. Device start-up occurs after VDD and VDDIO POR levels are reached. 表 6 shows how to connect the IFSEL pin to select between the SPI and I2C-compatible interfaces.

表 6. Serial Control Interface Selection

PIN NAME	IFSEL PIN = VDDIO	IFSEL PIN = GND
SS_ADDRSEL	ADDRSEL	SS
SCLK_SCL	SCL	SCLK
SDI_SDA	SDA	SDI
SDO_PWM	PWM	SDO

8.5.2 SPI Interface

In SPI mode host can address as many unique LP8863-Q1 devices as there are slave select pins on host. The complete 10-bit register space in LP8863-Q1 device can be accessed using SPI interface.

The LP8863-Q1 device is compatible with SPI serial-bus specification and operates as a slave device. The transmission consists of 32-bit write and read cycles. One cycle consists of a 15-bit register address (10 bits used), 1 read/write (R/W) bit and 16-bit data to maintain compatibility with 16-bit SPI.

The R/W bit high state defines a write cycle and low defines a read cycle. The SDO output is normally in a high-impedance state. When the slave-select pin SS for the device is active (that is, low) the SDO output is pulled low. During write cycle SDO stays in high-impedance state. The address and data bits are transmitted MSB first. The slave-select signal SS must be low during the cycle transmission. SS resets the interface when high, and it has to be taken high between successive cycles, except when using auto- increment mode. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

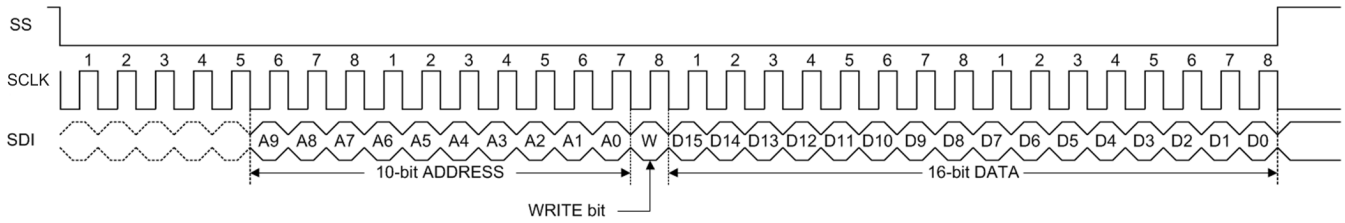


図 30. SPI Write

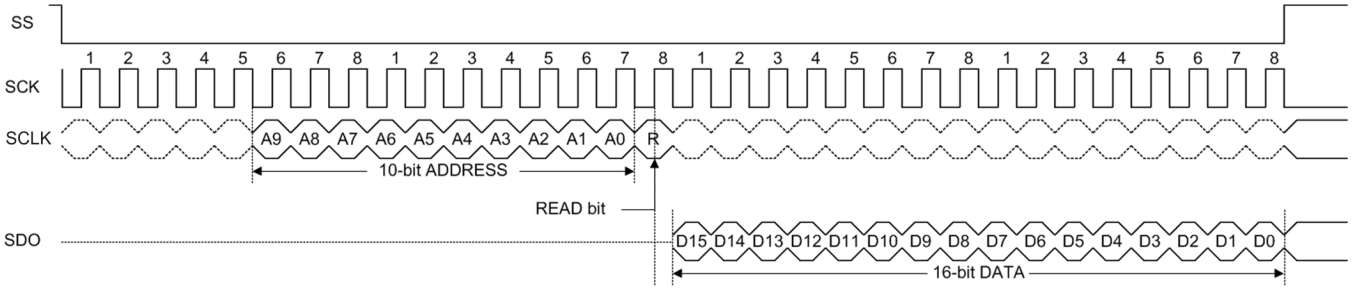


図 31. SPI Read

8.5.3 I2C-Compatible Interface

Two LP8863-Q1 slave devices may share the same I2C bus. The SS_ADDRSEL pin selects between the two possible base slave addresses.

表 7. I2C Address Selection

SS_ADDRSEL PIN	7-BIT I2C BASE SLAVE ADDRESS
GND	0x2C
VDDIO	0x3C

The LP8863-Q1 uses a 10-bit register address space. The 10-bit register address space is accessed as four separate 8-bit address spaces. Four different slave addresses are used to access each of the four 8-bit address register spaces.

表 8. I2C Address Registers Selection

SS_ADDRSEL PIN	7-BIT BASE ADDRESS	7-BIT SLAVE ADDRESS	ACCESSIBLE 10-BIT REGISTERS
GND	0x2C	0x2C	0x000 to 0x0FF
		0x2D	0x100 to 0x1FF
		0x2E	0x200 to 0x2FF
		0x2F	0x300 to 0x3FF
VDDIO	0x3C	0x3C	0x000 to 0x0FF
		0x3D	0x100 to 0x1FF
		0x3E	0x200 to 0x2FF
		0x3F	0x300 to 0x3FF

Write I2C transactions are made up of 4 bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8863-Q1 slave device and one of four 8-bit register address sections. The second byte includes eight LSB bits of the 10-bit register address. The last two bytes are the 16-bit register value.

Read I2C transactions are made up of five bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8863-Q1 slave device and one of four 8-bit register address sections. The second byte includes eight LSB bits of the 10-bit register address. The third byte includes the 7-bit slave address and Read bit. The last two bytes are the 16-bit register value returned from the slave.

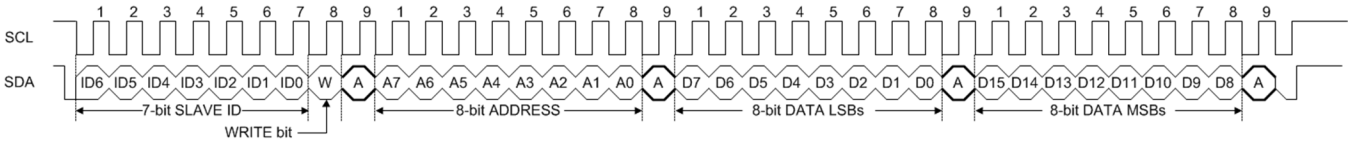


図 32. I2C Write

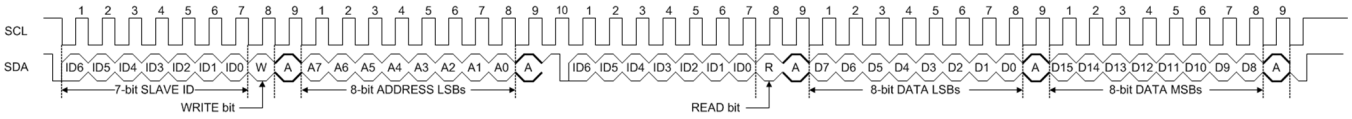


図 33. I2C Read

8.5.4 Programming Examples

8.5.4.1 General Configuration Registers

The LP8863-Q1 does not require any serial interface configuration. It can be simply controlled with the EN pin and PWM pin. Most of the device configuration is accomplished using external resistor values or automatic detection. If a serial interface is available then extended configuration is possible. The configuration registers can be written in standby state as shown in 表 9.

表 9. Configuration Registers

REGISTER NAME	FUNCTION
BRT_MODE	Selects PWM pin or DISPLAY_BRT register for brightness control.
SHORTED_LED_THRESHOLD	Selects voltage level for shorted LED Fault.
DITHER_SELECT	Selects up to 3 bits of PWM dither for added dimming resolution.
EN_MIN_PWM_LIMIT	Enables 200-ns PWM pulse limit and frequency dither to reach lower minimum brightness levels.
SLOPE_SELECT	Selects duration for linear brightness sloper.
ADV_SLOPE_ENABLE	Enables advance sloper S-shape smoothing function.
DIMMING_MODE	Select between PWM, hybrid or current LED ouput dimming types.
TEMP_MON_EN	Enables temperature window monitor function.
TEMPERATURE_LIMIT_HIGH	Sets HIGH threshold level for temperature window function.
TEMPERATURE_LIMIT_LOW	Sets LOW threshold level for temperature window function.

8.5.4.2 Clearing Fault Interrupts

The LP8863-Q1 has an INT pin to alert the host when a fault occurs. If a serial interface is available, the Interrupt Fault Status registers can be read back to learn which fault(s) have been detected. These status bits are located in the INTERRUPT_STATUS_1, INTERRUPT_STATUS_2, and INTERRUPT_STATUS_3 registers. Each interrupt status has a STATUS bit and a CLEAR bit. If a fault interrupt has been detected, a 1 is read back from its STATUS bit. To clear a fault interrupt status a 1 must be written to both the STATUS bit and CLEAR bit at the same time.

8.5.4.3 Disabling Fault Interrupts

By default most of the LP8863-Q1 faults trigger the INT pin. Each fault has two INT_EN bits. These bits are located in the INTERRUPT_ENABLE_1, INTERRUPT_ENABLE_2, and INTERRUPT_ENABLE_3 registers. If the INT_EN bit is read and returns a 1, the INT pin is triggered when that fault occurs. The fault interrupt can be disabled by writing 01 to its INT_EN bits, or it can be enabled by writing 11 to its INT_EN bits. There is also a GLOBAL fault interrupt that can be disabled to prevent any faults from triggering the INT pin.

8.5.4.4 Diagnostic Registers

The LP8863-Q1 contains several diagnostic registers than can be read with the serial interface for debugging or additional device information. 表 10 is a summary of the available registers.

表 10. Diagnostic Registers

REGISTER NAME	FUNCTION
JUNCTION_TEMPERATURE	9-bit die junction temperature in 2s complement form — 1°C per LSB
FSM_LIVE_STATUS	Current state of the functional state machine
PWM_INPUT_STATUS	Measured 6-bit duty cycle of the PWM pin input
LED_PWM_STATUS	16-bit LED0 PWM duty cycle from state machine
LED_CURRENT_STATUS	12-bit LED0 current DAC value from state machine
VBOOST_STATUS	10-bit value for adaptive boost voltage target — value is linear between VBOOST_MIN and VBOOST_MAX calculations
AUTO_PWM_FREQ_SEL	LED PWM frequency value from PWM_FSET detection
AUTO_BOOST_FREQ_SEL	Boost switching frequency value from PWM_FSET detection
AUTO_LED_STRING_CFG	LED string phase configuration detected from LED pin configuration

8.5.4.5 Cluster Mode Configuration and Control Registers

The LP8863-Q1 device supports a cluster mode where the duty cycles and LED current of the six LED current drivers can be controlled independently. This mode can also select which LED current driver's headroom levels are used by the adaptive boost voltage control loop. If the anode of an LED string is supplied by an external supply and not the integrated boost controller then its LED_EXT_SUPPLY bit is set to 1. The cluster mode configuration registers are summarized in 表 11. More details can be found in *Register Maps*.

表 11. Cluster Mode Configuration Registers

REGISTER NAME	FUNCTION
LED0_GROUP...LED5_GROUP	Selects which of the five CLUSTERx_BRT or DISPLAY_BRT registers control each LED current driver.
CLUSTER1_BRT…CLUSTER5_BRT	Five 16-bit brightness values that can be used in addition to the DISPLAY_BRT register.
LED0_CURRENT…LED5_CURRENT	Six 12-bit current registers allow LED current to be independently scaled from maximum level for LED current driver.
LOAD_BRT_DB	Load BRT bit is written to 1 in order to update the CLUSTERx_BRT and LEDx_CURRENT registers at the same time.
LED_EXT_SUPPLY	Six bits to select which LED current driver is powered from an external supply and not the boost converter.
LED0_SHORT_DISABLE… LED5_SHORT_DISABLE	Six bits to individually disable LED short detection for each LED current driver. Used if LED current value is set to lower value than other strings.

8.6 Register Maps

8.6.1 FullMap Registers

Table 12 lists the memory-mapped registers for the FullMap registers. All register offset addresses not listed in Table 12 should be considered as reserved locations and the register contents should not be modified.

Table 12. FULLMAP Registers

Offset	Acronym	Register Name	Section
20h	BL_MODE	Brightness Mode	Go
28h	DISP_BRT	Display Brightness	Go
30h	GROUPING1	Brightness Grouping 1	Go
32h	GROUPING2	Brightness Grouping 2	Go
40h	USER_CONFIG1	User Config 1	Go
42h	USER_CONFIG2	User Config 2	Go
4Eh	INTERRUPT_ENABLE_3	Fault Interrupt Enable 3	Go
50h	INTERRUPT_ENABLE_1	Fault Interrupt Enable 1	Go
52h	INTERRUPT_ENABLE_2	Fault Interrupt Enable 2	Go
54h	INTERRUPT_STATUS_1	Fault Interrupt Status 1	Go
56h	INTERRUPT_STATUS_2	Fault Interrupt Status 2	Go
58h	INTERRUPT_STATUS_3	Fault Interrupt Status 3	Go
E8h	JUNCTION_TEMPERATURE	Die Junction Temperature	Go
ECh	TEMPERATURE_LIMIT_HIGH	Temperature High Limit	Go
EEh	TEMPERATURE_LIMIT_LOW	Temperature Low Limit	Go
13Ch	CLUSTER1_BRT	Cluster 1 Brightness	Go
148h	CLUSTER2_BRT	Cluster 2 Brightness	Go
154h	CLUSTER3_BRT	Cluster 3 Brightness	Go
160h	CLUSTER4_BRT	Cluster 4 Brightness	Go
16Ch	CLUSTER5_BRT	Cluster 5 Brightness	Go
178h	BRT_DB_CONTROL	Cluster Brightness and Current Load Bit	Go
1C2h	LED0_CURRENT	LED0 Current	Go
1C4h	LED1_CURRENT	LED1 Current	Go
1C6h	LED2_CURRENT	LED2 Current	Go
1C8h	LED3_CURRENT	LED3 Current	Go
1CAh	LED4_CURRENT	LED4 Current	Go
1CCh	LED5_CURRENT	LED5 Current	Go
288h	BOOST_CONTROL	Boost Control	Go
28Ah	SHORT_THRESH	Shorted LED Threshold	Go
2A4h	FSM_DIAGNOSTICS	Device State Diagnostics	Go
2A6h	PWM_INPUT_DIAGNOSTICS	PWM Input Diagnostics	Go
2A8h	PWM_OUTPUT_DIAGNOSTICS	PWM Output Diagnostics	Go
2AAh	LED_CURR_DIAGNOSTICS	LED Current Diagnostics	Go
2ACh	ADAPT_BOOST_DIAGNOSTICS	Adaptive Boost Diagnostics	Go
2AEh	AUTO_DETECT_DIAGNOSTICS	Auto Detect Diagnstics	Go

Complex bit access types are encoded to fit into small table cells. Table 13 shows the codes that are used for access types in this section.

Table 13. FullMap Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

Table 13. FullMap Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 BL_MODE Register (Offset = 20h) [reset = 300h]

BL_MODE is shown in Figure 34 and described in Table 14.

Return to Summary Table.

Figure 34. BL_MODE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-C0h							
7	6	5	4	3	2	1	0
RESERVED						brightness_mode	
R/W-C0h						R/W-0h	

Table 14. BL_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	C0h	These bits are reserved.
1-0	brightness_mode	R/W	0h	0h = Brightness controlled by PWM Input 1h = Reserved 2h = Brightness controlled by DISPLAY_BRT Register 3h = Reserved

8.6.1.2 DISP_BRT Register (Offset = 28h) [reset = 0h]

DISP_BRT is shown in Figure 35 and described in Table 15.

Return to Summary Table.

Figure 35. DISP_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISPLAY_BRT															
R/W-0h															

Table 15. DISP_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DISPLAY_BRT	R/W	0h	Display Brightness Register

8.6.1.3 GROUPING1 Register (Offset = 30h) [reset = 0h]

GROUPING1 is shown in Figure 36 and described in Table 16.

Return to Summary Table.

Figure 36. GROUPING1 Register

15	14	13	12	11	10	9	8
LED3_GROUP				LED2_GROUP			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
LED1_GROUP				LED0_GROUP			
R/W-0h				R/W-0h			

Table 16. GROUPING1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LED3_GROUP	R/W	0h	LED Output 3 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT
11-8	LED2_GROUP	R/W	0h	LED Output 2 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT
7-4	LED1_GROUP	R/W	0h	LED Output 1 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT
3-0	LED0_GROUP	R/W	0h	LED Output 0 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT

8.6.1.4 GROUPING2 Register (Offset = 32h) [reset = 0h]

GROUPING2 is shown in Figure 37 and described in Table 17.

Return to Summary Table.

Figure 37. GROUPING2 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
LED5_GROUP				LED4_GROUP			
R/W-0h				R/W-0h			

Table 17. GROUPING2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	These bits are reserved.
7-4	LED5_GROUP	R/W	0h	LED Output 5 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT
3-0	LED4_GROUP	R/W	0h	LED Output 4 Brightness Control Mapping 0h = DISP_BRT/PWM 1h = CLUSTER1_BRT 2h = CLUSTER3_BRT 3h = CLUSTER3_BRT 4h = CLUSTER4_BRT 5h = CLUSTER5_BRT

8.6.1.5 USER_CONFIG1 Register (Offset = 40h) [reset = 8B0h]

USER_CONFIG1 is shown in Figure 38 and described in Table 18.

Return to Summary Table.

Figure 38. USER_CONFIG1 Register

15	14	13	12	11	10	9	8
DITHER_SELECT			RESERVED			TEMP_MON_EN	RESERVED
R/W-0h			R/W-2h			R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SLOPE_SELECT			ADV_SLOPE_ENABLE	RESERVED		DIMMING_MODE	
R/W-5h			R/W-1h	R/W-0h		R/W-0h	

Table 18. USER_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	DITHER_SELECT	R/W	0h	0h = Dither Disabled 1h = 1-bit Dither 2h = 2-bit Dither 3h = 3-bit Dither 4h = 4-bit Dither 5h = 5-bit Dither 6h = Unused 7h = Unused
12-10	RESERVED	R/W	2h	These bits are reserved.
9	TEMP_MON_EN	R/W	0h	0h = Temperature Monitor Disabled 1h = Temperature Monitor Enabled
8	RESERVED	R/W	0h	This bit is reserved.

Table 18. USER_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	SLOPE_SELECT	R/W	5h	0h = 0ms 1h = 1ms 2h = 2ms 3h = 50ms 4h = 100ms 5h = 200ms 6h = 300ms 7h = 500ms Times are for linear slope mode. Advanced sloper will increase durations while adding additional smoothing to brightness transitions. 1ms and 2ms sloper times are intended to be used only in linear mode. 50ms to 500ms sloper durations may be used with or without advanced sloper function.
4	ADV_SLOPE_ENABLE	R/W	1h	0h = Linear Sloping 1h = Advanced Sloping
3-2	RESERVED	R/W	0h	These bits are reserved.
1-0	DIMMING_MODE	R/W	0h	LED Output Dimming Mode 0h = PWM Mode 1h = 12.5% Hybrid Mode 2h = Unused 3h = 12-bit Constant Current Mode

8.6.1.6 USER_CONFIG2 Register (Offset = 42h) [reset = 0h]

USER_CONFIG2 is shown in Figure 39 and described in Table 19.

Return to Summary Table.

Figure 39. USER_CONFIG2 Register

15	14	13	12	11	10	9	8
EN_MIN_PWM_LIMIT	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 19. USER_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EN_MIN_PWM_LIMIT	R/W	0h	Allows PWM pulses to be dithered to reduce lower minimum brightness. When enabled brightness levels that map to less than 200ns pulse width will cause pulses to be skipped. 0h = Disabled 1h = Enabled
14-0	RESERVED	R/W	0h	These bits are reserved.

8.6.1.7 INTERRUPT_ENABLE_3 Register (Offset = 4Eh) [reset = 200Ah]

INTERRUPT_ENABLE_3 is shown in Figure 40 and described in Table 20.

Return to Summary Table.

Figure 40. INTERRUPT_ENABLE_3 Register

15	14	13	12	11	10	9	8
BSTSYNC_INT_EN		VINOCP_INT_EN		CPCAP_INT_EN		CP_INT_EN	
R/W-0h		R/W-2h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
FSET_INT_EN		INVSTRING_INT_EN		VINOVP_INT_EN		VINUVP_INT_EN	
R/W-0h		R/W-0h		R/W-2h		R/W-2h	

Table 20. INTERRUPT_ENABLE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	BSTSYNC_INT_EN	R/W	0h	Missing Boost Sync Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
13-12	VINOCP_INT_EN	R/W	2h	VIN Over-Current Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
11-10	CPCAP_INT_EN	R/W	0h	Charge Pump Cap Missing Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
9-8	CP_INT_EN	R/W	0h	Charge Pump Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
7-6	FSET_INT_EN	R/W	0h	Missing FSET Resistor Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
5-4	INVSTRING_INT_EN	R/W	0h	Invalid LED String Configuration Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

Table 20. INTERRUPT_ENABLE_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	VINOVP_INT_EN	R/W	2h	VIN Over-Voltage Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
1-0	VINUVP_INT_EN	R/W	2h	VIN Under-Voltage Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

8.6.1.8 INTERRUPT_ENABLE_1 Register (Offset = 50h) [reset = A02Ah]

INTERRUPT_ENABLE_1 is shown in Figure 41 and described in Table 21.

Return to Summary Table.

Figure 41. INTERRUPT_ENABLE_1 Register

15	14	13	12	11	10	9	8
GLOBAL_INT_EN		BSTOVPH_INT_EN		TEMP_INT_EN		RESERVED	
R/W-2h		R/W-2h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
BSTOVPL_INT_EN		BSTOCP_INT_EN		VDDUVLO_INT_EN		TSD_INT_EN	
R/W-0h		R/W-2h		R/W-2h		R/W-2h	

Table 21. INTERRUPT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	GLOBAL_INT_EN	R/W	2h	Global Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
13-12	BSTOVPH_INT_EN	R/W	2h	Boost OVP High Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
11-10	TEMP_INT_EN	R/W	0h	Temperature Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
9-8	RESERVED	R/W	0h	These bits are reserved.

Table 21. INTERRUPT_ENABLE_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	BSTOVPL_INT_EN	R/W	0h	Boost OVP Low Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
5-4	BSTOCP_INT_EN	R/W	2h	Boost Over-Current Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
3-2	VDDUVLO_INT_EN	R/W	2h	VDD UVLO Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
1-0	TSD_INT_EN	R/W	2h	Thermal Shutdown Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt

8.6.1.9 INTERRUPT_ENABLE_2 Register (Offset = 52h) [reset = 80h]

INTERRUPT_ENABLE_2 is shown in Figure 42 and described in Table 22.

Return to Summary Table.

Figure 42. INTERRUPT_ENABLE_2 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
LED_INT_EN		RESERVED					
R/W-2h		R/W-0h					

Table 22. INTERRUPT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	These bits are reserved.
7-6	LED_INT_EN	R/W	2h	LED Open / Short Interrupt Enable Read: 0h = Interrupt is currently disabled 2h = Interrupt is currently enabled Write: 1h = Disable Interrupt 3h = Enable Interrupt
5-0	RESERVED	R/W	0h	

8.6.1.10 INTERRUPT_STATUS_1 Register (Offset = 54h) [reset = 0h]

INTERRUPT_STATUS_1 is shown in Figure 43 and described in Table 23.

Return to Summary Table.

Figure 43. INTERRUPT_STATUS_1 Register

15	14	13	12	11	10	9	8
BSTOVPH_STATUS	BSTOVPH_CLEAR	TEMPHIGH_STATUS	TEMPHIGH_CLEAR	TEMPLOW_STATUS	TEMPLOW_CLEAR	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
BSTOVPL_STATUS	BSTOVPL_CLEAR	BSTOCP_STATUS	BSTOCP_CLEAR	VDDUVLO_STATUS	VDDUVLO_CLEAR	TSD_STATUS	TSD_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 23. INTERRUPT_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BSTOVPH_STATUS	R/W	0h	Boost OVP High Status 0h = No Fault 1h = Fault
14	BSTOVPH_CLEAR	R/W	0h	Boost OVP High Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
13	TEMPHIGH_STATUS	R/W	0h	Temperature High Status 0h = No Fault 1h = Fault
12	TEMPHIGH_CLEAR	R/W	0h	Temperature High Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
11	TEMPLOW_STATUS	R/W	0h	Temperature Low Status 0h = No Fault 1h = Fault
10	TEMPLOW_CLEAR	R/W	0h	Temperature Low Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
9-8	RESERVED	R/W	0h	These bits are reserved.
7	BSTOVPL_STATUS	R/W	0h	Boost OVP Low Status 0h = No Fault 1h = Fault
6	BSTOVPL_CLEAR	R/W	0h	Boost OVP Low Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
5	BSTOCP_STATUS	R/W	0h	Boost Over-Current Status 0h = No Fault 1h = Fault
4	BSTOCP_CLEAR	R/W	0h	Boost Over-Current Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
3	VDDUVLO_STATUS	R/W	0h	VDD UVLO Status 0h = No Fault 1h = Fault

Table 23. INTERRUPT_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	VDDUVLO_CLEAR	R/W	0h	VDD UVLO Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
1	TSD_STATUS	R/W	0h	Thermal Shutdown Status 0h = No Fault 1h = Fault
0	TSD_CLEAR	R/W	0h	Thermal Shutdown Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.

8.6.1.11 INTERRUPT_STATUS_2 Register (Offset = 56h) [reset = 0h]

INTERRUPT_STATUS_2 is shown in Figure 44 and described in Table 24.

Return to Summary Table.

Figure 44. INTERRUPT_STATUS_2 Register

15	14	13	12	11	10	9	8
LED5_FAULT	LED4_FAULT	LED3_FAULT	LED2_FAULT	LED1_FAULT	LED0_FAULT	OPEN_LED	SHORT_LED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
LED_STATUS	LED_CLEAR	RESERVED					
R/W-0h	R/W-0h	R/W-0h					

Table 24. INTERRUPT_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED5_FAULT	R/W	0h	LED5 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
14	LED4_FAULT	R/W	0h	LED4 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
13	LED3_FAULT	R/W	0h	LED3 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
12	LED2_FAULT	R/W	0h	LED2 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
11	LED1_FAULT	R/W	0h	LED1 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
10	LED0_FAULT	R/W	0h	LED0 Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit

Table 24. INTERRUPT_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	OPEN_LED	R/W	0h	LED Open Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
8	SHORT_LED	R/W	0h	LED Short Status 0h = No Fault 1h = Fault Status is cleared with LED_STATUS bit
7	LED_STATUS	R/W	0h	LED Open / Short Fault Status 0h = No Fault 1h = Fault
6	LED_CLEAR	R/W	0h	LED Open / Short Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
5-0	RESERVED	R/W	0h	These bits are reserved.

8.6.1.12 INTERRUPT_STATUS_3 Register (Offset = 58h) [reset = 0h]

INTERRUPT_STATUS_3 is shown in Figure 45 and described in Table 25.

Return to Summary Table.

Figure 45. INTERRUPT_STATUS_3 Register

15	14	13	12	11	10	9	8
BSTSYNC_STATUS	BSTSYNC_CLEAR	VINOCP_STATUS	VINOCP_CLEAR	CPCAP_STATUS	CPCAP_CLEAR	CP_STATUS	CP_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
FSET_STATUS	FSET_CLEAR	INVSTRING_STATUS	INVSTRING_CLEAR	VINOVP_STATUS	VINOVP_CLEAR	VINUVP_STATUS	VINUVP_CLEAR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25. INTERRUPT_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BSTSYNC_STATUS	R/W	0h	Missing Boost Sync Fault Status 0h = No Fault 1h = Fault
14	BSTSYNC_CLEAR	R/W	0h	Missing Boost Sync Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
13	VINOCP_STATUS	R/W	0h	VIN Over-Current Fault Status 0h = No Fault 1h = Fault
12	VINOCP_CLEAR	R/W	0h	VIN Over-Current Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
11	CPCAP_STATUS	R/W	0h	Missing Charge Pump Capacitor Fault Status 0h = No Fault 1h = Fault

Table 25. INTERRUPT_STATUS_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CPCAP_CLEAR	R/W	0h	Missing Charge Pump Capacitor Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
9	CP_STATUS	R/W	0h	Charge Pump Fault Status 0h = No Fault 1h = Fault
8	CP_CLEAR	R/W	0h	Charge Pump Fault Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
7	FSET_STATUS	R/W	0h	Missing Boost / PWM FSET Resistor Fault Status 0h = No Fault 1h = Fault
6	FSET_CLEAR	R/W	0h	Missing Boost / PWM FSET Resistor Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
5	INVSTRING_STATUS	R/W	0h	Invalid LED String Configuration Fault Status 0h = No Fault 1h = Fault
4	INVSTRING_CLEAR	R/W	0h	Invalid LED String Configuration Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
3	VINOVP_STATUS	R/W	0h	VIN Over-Voltage Fault Status 0h = No Fault 1h = Fault
2	VINOVP_CLEAR	R/W	0h	VIN Over-Voltage Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.
1	VINUVP_STATUS	R/W	0h	VIN Under-Voltage Fault Status 0h = No Fault 1h = Fault
0	VINUVP_CLEAR	R/W	0h	VIN Under-Voltage Fault Clear Write "1" to both Status bit and Clear bit at same time to clear interrupt register status and interrupt pin status.

8.6.1.13 JUNCTION_TEMPERATURE Register (Offset = E8h) [reset = 100h]

JUNCTION_TEMPERATURE is shown in Figure 46 and described in Table 26.

Return to Summary Table.

Figure 46. JUNCTION_TEMPERATURE Register

15	14	13	12	11	10	9	8
RESERVED							JUNCTION_TEMPERATURE
R-0h							R-100h
7	6	5	4	3	2	1	0
JUNCTION_TEMPERATURE							
R-100h							

Table 26. JUNCTION_TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	These bits are reserved.
8-0	JUNCTION_TEMPERATURE	R	100h	Junction Temperature ADC Measurement 2's complement number. 000h - 0FFh = 0 °C to 255 °C 100h - 1FFh = –256 °C to –1 °C

8.6.1.14 TEMPERATURE_LIMIT_HIGH Register (Offset = ECh) [reset = 7Dh]

TEMPERATURE_LIMIT_HIGH is shown in Figure 47 and described in Table 27.

Return to Summary Table.

Figure 47. TEMPERATURE_LIMIT_HIGH Register

15	14	13	12	11	10	9	8
RESERVED							TEMPERATURE_LIMIT_HIGH
R-0h							R/W-7Dh
7	6	5	4	3	2	1	0
TEMPERATURE_LIMIT_HIGH							
R/W-7Dh							

Table 27. TEMPERATURE_LIMIT_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	These bits are reserved.
8-0	TEMPERATURE_LIMIT_HIGH	R/W	7Dh	High Limit for Junction Temperature Monitor 2's complement number. 000h - 0FFh = 0 °C to 255 °C 100h - 1FFh = –256 °C to –1 °C

8.6.1.15 TEMPERATURE_LIMIT_LOW Register (Offset = EEh) [reset = 69h]

TEMPERATURE_LIMIT_LOW is shown in Figure 48 and described in Table 28.

Return to Summary Table.

Figure 48. TEMPERATURE_LIMIT_LOW Register

15	14	13	12	11	10	9	8
RESERVED							TEMPERATURE_LIMIT_LOW
R-0h							R/W-69h
7	6	5	4	3	2	1	0
TEMPERATURE_LIMIT_LOW							
R/W-69h							

Table 28. TEMPERATURE_LIMIT_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	These bits are reserved.
8-0	TEMPERATURE_LIMIT_LOW	R/W	69h	Low Limit for Junction Temperature Monitor 2's complement number. 000h - 0FFh = 0 °C to 255 °C 100h - 1FFh = –256 °C to –1 °C

8.6.1.16 CLUSTER1_BRT Register (Offset = 13Ch) [reset = FFFFh]

CLUSTER1_BRT is shown in Figure 49 and described in Table 29.

Return to Summary Table.

Figure 49. CLUSTER1_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUSTER1_BRT															
R/W-FFFFh															

Table 29. CLUSTER1_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLUSTER1_BRT	R/W	FFFFh	CLUSTER1 Brightness Control. This register controls LED output duty cycle for the LED outputs assigned to LED GROUP 1. This register is buffered, write LOAD_BRT_DB bit to update.

8.6.1.17 CLUSTER2_BRT Register (Offset = 148h) [reset = FFFFh]

CLUSTER2_BRT is shown in Figure 50 and described in Table 30.

Return to Summary Table.

Figure 50. CLUSTER2_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUSTER2_BRT															
R/W-FFFFh															

Table 30. CLUSTER2_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLUSTER2_BRT	R/W	FFFFh	CLUSTER2 Brightness Control. This register controls LED output duty cycle for the LED outputs assigned to LED GROUP 2. This register is buffered, write LOAD_BRT_DB bit to update.

8.6.1.18 CLUSTER3_BRT Register (Offset = 154h) [reset = FFFFh]

CLUSTER3_BRT is shown in Figure 51 and described in Table 31.

Return to Summary Table.

Figure 51. CLUSTER3_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUSTER3_BRT															
R/W-FFFFh															

Table 31. CLUSTER3_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLUSTER3_BRT	R/W	FFFFh	CLUSTER3 Brightness Control. This register controls LED output duty cycle for the LED outputs assigned to LED GROUP 3. This register is buffered, write LOAD_BRT_DB bit to update.

8.6.1.19 CLUSTER4_BRT Register (Offset = 160h) [reset = FFFFh]

CLUSTER4_BRT is shown in Figure 52 and described in Table 32.

Return to Summary Table.

Figure 52. CLUSTER4_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUSTER4_BRT															
R/W-FFFFh															

Table 32. CLUSTER4_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLUSTER4_BRT	R/W	FFFFh	CLUSTER4 Brightness Control. This register controls LED output duty cycle for the LED outputs assigned to LED GROUP 4. This register is buffered, write LOAD_BRT_DB bit to update.

8.6.1.20 CLUSTER5_BRT Register (Offset = 16Ch) [reset = FFFFh]

CLUSTER5_BRT is shown in Figure 53 and described in Table 33.

Return to Summary Table.

Figure 53. CLUSTER5_BRT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLUSTER5_BRT															
R/W-FFFFh															

Table 33. CLUSTER5_BRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLUSTER5_BRT	R/W	FFFFh	CLUSTER5 Brightness Control. This register controls LED output duty cycle for the LED outputs assigned to LED GROUP 5. This register is buffered, write LOAD_BRT_DB bit to update.

8.6.1.21 BRT_DB_CONTROL Register (Offset = 178h) [reset = 0h]

BRT_DB_CONTROL is shown in Figure 54 and described in Table 34.

Return to Summary Table.

Figure 54. BRT_DB_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							LOAD_BRT_DB
R/W-0h							R/W-0h

Table 34. BRT_DB_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0h	These bits are reserved.
0	LOAD_BRT_DB	R/W	0h	Write this bit to "1" to update CLUSTERx_BRT registers and LEDx_CURRENT registers (those registers are buffered).

8.6.1.22 LED0_CURRENT Register (Offset = 1C2h) [reset = FFFh]

LED0_CURRENT is shown in Figure 55 and described in Table 35.

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Figure 55. LED0_CURRENT Register

15	14	13	12	11	10	9	8
LED0_SHORT_DISABLE	RESERVED			LED0_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED0_CURRENT							
R/W-FFFh							

Table 35. LED0_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED0_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED0 0h = Short LED Faults are detected for LED0 output 1h = Short LED Faults are not detected for LED0 output
14-12	RESERVED	R/W	0h	
11-0	LED0_CURRENT	R/W	FFFh	Individual LED Current control for LED0 Output

8.6.1.23 LED1_CURRENT Register (Offset = 1C4h) [reset = FFFh]

LED1_CURRENT is shown in Figure 56 and described in Table 36.

Return to Summary Table.

Figure 56. LED1_CURRENT Register

15	14	13	12	11	10	9	8
LED1_SHORT_DISABLE	RESERVED			LED1_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED1_CURRENT							
R/W-FFFh							

Table 36. LED1_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED1_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED1 0h = Short LED Faults are detected for LED1 output 1h = Short LED Faults are not detected for LED1 output
14-12	RESERVED	R/W	0h	
11-0	LED1_CURRENT	R/W	FFFh	Individual LED Current control for LED1 Output

8.6.1.24 LED2_CURRENT Register (Offset = 1C6h) [reset = FFFh]

LED2_CURRENT is shown in Figure 57 and described in Table 37.

Return to Summary Table.

Figure 57. LED2_CURRENT Register

15	14	13	12	11	10	9	8
LED2_SHORT_DISABLE	RESERVED			LED2_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED2_CURRENT							
R/W-FFFh							

Table 37. LED2_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED2_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED2 0h = Short LED Faults are detected for LED2 output 1h = Short LED Faults are not detected for LED2 output
14-12	RESERVED	R/W	0h	
11-0	LED2_CURRENT	R/W	FFFh	Individual LED Current control for LED2 Output

8.6.1.25 LED3_CURRENT Register (Offset = 1C8h) [reset = FFFh]

LED3_CURRENT is shown in Figure 58 and described in Table 38.

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Figure 58. LED3_CURRENT Register

15	14	13	12	11	10	9	8
LED3_SHORT_DISABLE	RESERVED			LED3_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED3_CURRENT							
R/W-FFFh							

Table 38. LED3_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED3_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED3 0h = Short LED Faults are detected for LED3 output 1h = Short LED Faults are not detected for LED3 output
14-12	RESERVED	R/W	0h	
11-0	LED3_CURRENT	R/W	FFFh	Individual LED Current control for LED3 Output

8.6.1.26 LED4_CURRENT Register (Offset = 1CAh) [reset = FFFh]

LED4_CURRENT is shown in Figure 59 and described in Table 39.

Return to Summary Table.

Figure 59. LED4_CURRENT Register

15	14	13	12	11	10	9	8
LED4_SHORT_DISABLE	RESERVED			LED4_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED4_CURRENT							
R/W-FFFh							

Table 39. LED4_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED4_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED4 0h = Short LED Faults are detected for LED4 output 1h = Short LED Faults are not detected for LED4 output
14-12	RESERVED	R/W	0h	
11-0	LED4_CURRENT	R/W	FFFh	Individual LED Current control for LED4 Output

8.6.1.27 LED5_CURRENT Register (Offset = 1CCh) [reset = FFFh]

LED5_CURRENT is shown in Figure 60 and described in Table 40.

Return to Summary Table.

Figure 60. LED5_CURRENT Register

15	14	13	12	11	10	9	8
LED5_SHORT_DISABLE	RESERVED			LED5_CURRENT			
R/W-0h	R/W-0h			R/W-FFFh			
7	6	5	4	3	2	1	0
LED5_CURRENT							
R/W-FFFh							

Table 40. LED5_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LED5_SHORT_DISABLE	R/W	0h	Short Fault Disable for LED5 0h = Short LED Faults are detected for LED5 output 1h = Short LED Faults are not detected for LED5 output
14-12	RESERVED	R/W	0h	
11-0	LED5_CURRENT	R/W	FFFh	Individual LED Current control for LED5 Output

8.6.1.28 BOOST_CONTROL Register (Offset = 288h) [reset = 1C0h]

BOOST_CONTROL is shown in Figure 61 and described in Table 41.

Return to Summary Table.

Figure 61. BOOST_CONTROL Register

15	14	13	12	11	10	9	8
LED_EXT_SUPPLY						RESERVED	
R/W-0h						R/W-1C0h	
7	6	5	4	3	2	1	0
RESERVED							
R/W-1C0h							

Table 41. BOOST_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	LED_EXT_SUPPLY	R/W	0h	Selects whether external LED voltage supply is used for a LED output. Bit 15 = LED5 Bit 14 = LED4 Bit 13 = LED3 Bit 12 = LED2 Bit 11 = LED1 Bit 10 = LED0 0h = LP8863 Boost Converter Supply is used 1h = External Supply is used.
9-0	RESERVED	R/W	1C0h	These bits are reserved.

8.6.1.29 SHORT_THRESH Register (Offset = 28Ah) [reset = 2882h]

SHORT_THRESH is shown in Figure 62 and described in Table 42.

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Figure 62. SHORT_THRESH Register

15	14	13	12	11	10	9	8
RESERVED				SHORTED_LED_THRESHOLD			RESERVED
R/W-2h				R/W-4h			R/W-82h
7	6	5	4	3	2	1	0
RESERVED							
R/W-82h							

Table 42. SHORT_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	2h	This bit is reserved.
11-9	SHORTED_LED_THRESHOLD	R/W	4h	Threshold for detecting Shorted LED Fault on LED outputs. Fault is detected when LEDx pin voltage (referenced to ground) exceeds selected threshold when LED driver is enabled. 0h = 2.6V 1h = 3.0V 2h = 3.4V 3h = 3.8V 4h = 4.2V 5h = 4.8V 6h = 5.2V 7h = 6.0V
8-0	RESERVED	R/W	82h	These bits are reserved.

8.6.1.30 FSM_DIAGNOSTICS Register (Offset = 2A4h) [reset = 0h]

FSM_DIAGNOSTICS is shown in Figure 63 and described in Table 43.

Return to Summary Table.

Figure 63. FSM_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			FSM_LIVE_STATUS				
R-0h			R-0h				

Table 43. FSM_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	These bits are reserved.
4-0	FSM_LIVE_STATUS	R	0h	Current status of Device state machine. 1h = LDO_STARTUP 2h = EEPROM_READ 3h = STANDBY 4h - Ch = BOOST_START Dh = NORMAL Eh = DISCHARGE Fh = SHUTDOWN 10h = FAULT_RECOVERY 11h = ALL_LED_FAULT

8.6.1.31 PWM_INPUT_DIAGNOSTICS Register (Offset = 2A6h) [reset = 0h]

PWM_INPUT_DIAGNOSTICS is shown in Figure 64 and described in Table 44.

Return to Summary Table.

Figure 64. PWM_INPUT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_INPUT_STATUS															
R-0h															

Table 44. PWM_INPUT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PWM_INPUT_STATUS	R	0h	16bit value for detected duty cycle of PWM input signal.

8.6.1.32 PWM_OUTPUT_DIAGNOSTICS Register (Offset = 2A8h) [reset = 0h]

PWM_OUTPUT_DIAGNOSTICS is shown in Figure 65 and described in Table 45.

Return to Summary Table.

Figure 65. PWM_OUTPUT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LED_PWM_STATUS															
R-0h															

Table 45. PWM_OUTPUT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LED_PWM_STATUS	R	0h	16-bit PWM Duty Code that Brightness path is driving to LED0 output.

8.6.1.33 LED_CURR_DIAGNOSTICS Register (Offset = 2AAh) [reset = 0h]

LED_CURR_DIAGNOSTICS is shown in Figure 66 and described in Table 46.

Return to Summary Table.

Figure 66. LED_CURR_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED				LED_CURRENT_STATUS			
R-0h				R-0h			
7	6	5	4	3	2	1	0
LED_CURRENT_STATUS							
R-0h							

Table 46. LED_CURR_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	These bits are reserved.
11-0	LED_CURRENT_STATUS	R	0h	12-bit Current DAC Code that Brightness path is driving to LED0 output.

8.6.1.34 ADAPT_BOOST_DIAGNOSTICS Register (Offset = 2ACh) [reset = 0h]

ADAPT_BOOST_DIAGNOSTICS is shown in Figure 67 and described in Table 47.

Return to Summary Table.

Figure 67. ADAPT_BOOST_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED					VBOOST_STATUS		
R-0h					R-0h		
7	6	5	4	3	2	1	0
VBOOST_STATUS							
R-0h							

Table 47. ADAPT_BOOST_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	These bits are reserved.
10-0	VBOOST_STATUS	R	0h	11-bit Boost Voltage Code that Adaptive Voltage Control Loop is sending to Analog Boost Block. Boost Output Voltage = ((R_FB1/R_FB2)*1.2)+(R_FB1*18.75nA*VBOOST_STATUS)

8.6.1.35 AUTO_DETECT_DIAGNOSTICS Register (Offset = 2AEh) [reset = 0h]

AUTO_DETECT_DIAGNOSTICS is shown in Figure 68 and described in Table 48.

Return to Summary Table.

Figure 68. AUTO_DETECT_DIAGNOSTICS Register

15	14	13	12	11	10	9	8
RESERVED							AUTO_PWM_FREQ_SEL
R-0h							R-0h
7	6	5	4	3	2	1	0
AUTO_PWM_FREQ_SEL		AUTO_BOOST_FREQ_SEL			AUTO_LED_STRING_CFG		
R-0h		R-0h			R-0h		

Table 48. AUTO_DETECT_DIAGNOSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	These bits are reserved.
8-6	AUTO_PWM_FREQ_SEL	R	0h	PWM Frequency Setting based on PWM_FSET resistor detection. 0h = 152Hz 1h = 305Hz 2h = 610 Hz 3h = 1.22kHz 4h = 2.44kHz 5h = 4.88kHz 6h = 9.77kHz 7h = 19.53kHz
5-3	AUTO_BOOST_FREQ_SEL	R	0h	Boost Frequency Setting based on BST_FSET resistor detection. 0h = 303kHz 1h = 400kHz 2h = 606kHz 3h = 800kHz 4h = 1MHz 5h = 1.25 MHz 6h = 1.67MHz 7h = 2.2MHz
2-0	AUTO_LED_STRING_CFG	R	0h	Detected LED string configuration. 0h = 6 separate strings 1h = 5 separate strings 2h = 4 separate strings 3h = 3 separate strings 4h = 2 separate strings 5h = outputs connected in groups of 2 to drive 3 strings 6h = outputs connected in groups of 3 to drive 2 strings 7h = all outputs connected together to drive one string

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP8863-Q1 device is designed for automotive applications, and an input voltage V_{IN} is intended to be connected to the vehicle battery. Depending on the input voltage, the device may be used in either boost mode or SEPIC mode. The device is internally powered from the VDD pin, and voltage must be in 2.7-V to 5.5-V range. The device has flexible configurability through external components or by an SPI or I2C interface. If the VDD voltage is not high enough to drive an external nMOSFET gate, an internal charge pump must be used to power the gate driver (GD pin).

注

For applications where V_{IN} voltage is below the output voltage, use a boost converter topology. Maximum operating voltage for V_{IN} is 48 V, and the boost converter can achieve output voltage up to 47 V. Conversion ratio of 5.5 (full load) or 10 (half load) must be taken into account. If V_{IN} voltage is expected to be below or above output voltage, a SEPIC converter can be implemented. The SEPIC converter can achieve maximum output voltage up to 24 V, and maximum conversion ratio for SEPIC mode is 5.

9.2 Typical Applications

9.2.1 Full Feature Application for Display Backlight

図 69 shows a full application for the LP8863-Q1 device in a boost topology. It supports 6 LED strings in display mode, each at 100 mA, with an automatic 60° phase shift. Brightness control register is used for LED dimming method through I2C communication. The charge pump is enabled for a 400-kHz boost switching frequency with spread spectrum.

Typical Applications (continued)

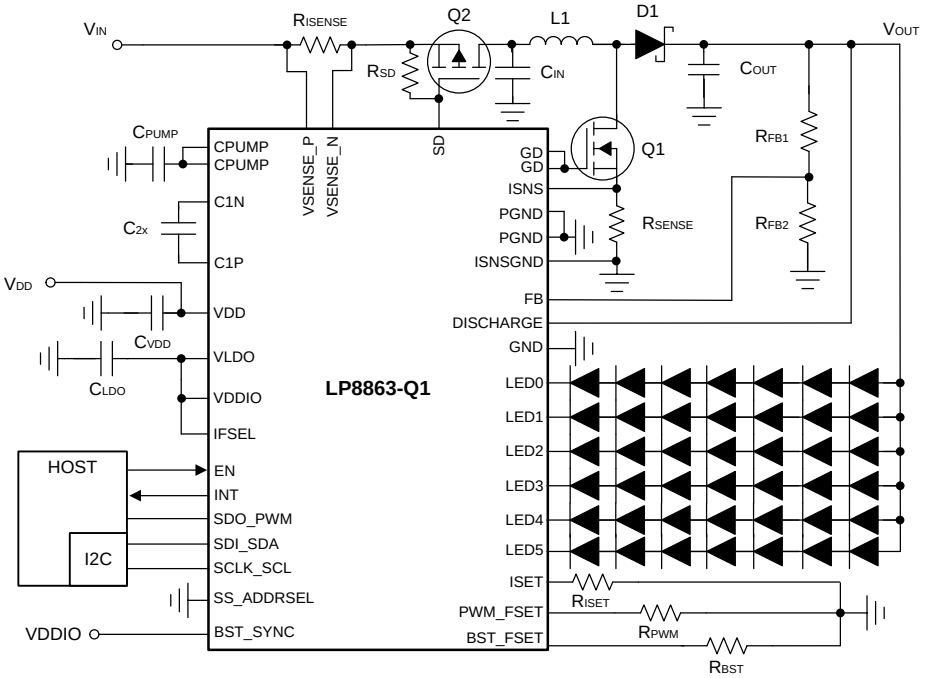


図 69. Full Feature Application for Display Backlight

9.2.1.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in 表 49:

表 49. LP8863-Q1 Full-Feature Design Parameters

DESIGN PARAMETER	VALUE
VIN voltage range	3 V to 20 V
VDD voltage	3.3 V
LED strings configuration	6 strings, 7 LEDs in series
Charge pump	Enabled
Brightness control	I2C
Output configuration	LED0 to LED5 are in display mode (phase shift 60°)
LED string current	100 mA
Boost frequency	400 kHz
Inductor	22 µH at 12-A saturation current
R_{ISENSE}	20 mΩ
Power-line FET	Enabled
R_{SENSE}	20 mΩ
Input/Output capacitors	C_{IN} and C_{OUT}: 2 × 33-µF electrolytic + 2 × 10-µF ceramic
Spread spectrum	Enabled
Discharge function	Enabled

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

There are a few things to consider when choosing an inductor: inductance, current rating, and DC resistance (DCR). 表 50 shows recommended inductor values for each operating frequency. The LP8863-Q1 device automatically sets internal boost compensation controls depending on the selected switching frequency.

表 50. Inductance Values for Boost Switching Frequencies

SW FREQUENCY (kHz)	INDUCTANCE (µH)
300	22
400	22
600	15
800	15
1000	10
1250	10
1667	10
2200	10

The current rating of inductor must be at least 25% higher than maximum boost switching current $I_{SW(max)}$, which can be calculated with 式 12. TI recommends a current rating of 12 A for most applications; use an inductor with low DCR to achieve good efficiency. Efficiency varies with load condition, switching frequency, and components, but 80% can be use as safe estimation. *Power Stage Designer™ Tools* can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{OUT(max)}}{1 - D} \quad (12)$$

where

- $\Delta I_L = V_{IN(min)} \times D / (f_{SW} \times L)$
- $D = 1 - V_{IN(min)} \times \eta / V_{OUT}$
- $I_{SW(max)}$: Maximum switching current
- ΔI_L: Inductor ripple current
- $I_{OUT(max)}$: Maximum output current
- D: Boost duty cycle
- $V_{IN(min)}$: Minimum input voltage
- f_{SW}: Minimum switching frequency of the converter
- L: Inductance
- V_{OUT}: Output voltage
- η: Efficiency of boost converter

9.2.1.2.2 Output Capacitor Selection

Recommended voltage rating for output capacitors is 50% higher than maximum output voltage level — 100-V voltage rating is recommended. Capacitance value determines voltage ripple and boost stability. The DC-bias effect can reduce the effective capacitance significantly, by up to 80%, a consideration for capacitance value selection. Effective capacitance must be at least 50 µF for full load/maximum conversion ratio applications and must be used to achieve good phase and gain margin levels. TI recommends using two 33-µF Al-polymer electrolytic capacitors and two 10-µF ceramic capacitors in parallel to reduce ripple, increase stability, and reduce ESR effect.

9.2.1.2.3 Input Capacitor Selection

Recommended input capacitance is the same as output capacitance although input capacitors are not as critical to boost operation. Input capacitance can be reduced but must ensure enough filtering for input power.

9.2.1.2.4 Charge Pump Output Capacitor

TI recommends a ceramic capacitor with at least 16-V voltage rating for the output capacitor of the charge pump. A 10-µF capacitor can be used for most applications.

9.2.1.2.5 Charge Pump Flying Capacitor

TI recommends a ceramic capacitor with at least 16-V voltage rating for the flying capacitor of the charge pump. One 2.2-µF capacitor connecting C1P and C1N pins can be used for most applications.

9.2.1.2.6 Output Diode

A Schottky diode must be used for the boost output diode. Current rating must be at least 25% higher than the maximum output current; TI recommends a 12-A current rating for most applications. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. At maximum current, the forward voltage must be as low as possible; less than 0.5 V is recommended. Reverse breakdown voltage of the Schottky diode must be significantly larger than the output voltage, 25% higher voltage rating is recommended. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause efficiency and load regulation to suffer.

9.2.1.2.7 Switching FET

Gate-drive voltage for the FET is V_{DD} with charge pump bypassed, or about double V_{DD}, if the charge pump is enabled. Switching FET is a critical component for determining power efficiency of the boost converter. Several aspects need to be considered when selecting switching FET such as voltage and current rating, R_{DSON}, power dissipation, thermal resistance and rise/fall times. An N type MOSFET with at least 25% higher voltage rating than maximum output voltage must be used. Current rating of switching FET should be same or higher than inductor rating. R_{DSON} must be as low as possible, less than 20 mΩ is recommended. Thermal resistance ($R_{\theta JA}$) must also be low to dissipate heat from power loss on switching FET. TI recommends typical rise/fall time values less than 10 ns.

9.2.1.2.8 Boost Sense Resistor

The R_{SENSE} resistor determines the boost overcurrent limit and is sensed every boost switching cycle. A high-power 20-mΩ resistor can be used for sensing the boost SW current and setting maximum current limit at 10 A (typical). R_{SENSE} can be increased to lower this limit and can be calculated with 式 13, but this should be done carefully because it may also affect stability. Boost overcurrent limit must not be set below 4 A, therefore R_{SENSE} must not exceed 50 mΩ. Power rating can be calculated from the inductor current and sense resistor resistance value.

$$R_{SENSE} = \frac{200\ mV}{I_{BOOST\_OCP}} \quad (13)$$

where

- R_{SENSE}: boost sense resistor (mΩ)
- I_{BOOST_OCP}: boost overcurrent limit

9.2.1.2.9 Power-Line FET

A power line FET can be used to disconnect input power from boost input to protect the LP8863-Q1 device and boost components in case an overcurrent event occurs. A P type MOSFET is used for the power-line FET. Voltage rating must be at least 25% higher than maximum input voltage level. Low R_{DSON} is important to reduce power loss on the FET — less than 20 mΩ is recommended. Current rating for the FET must be at least 25% higher than input peak current. Gate-to-source voltage (V_{GS}) for open transistor must be less than minimum input voltage; use a 20-kΩ resistor between the pFET gate and source.

9.2.1.2.10 Input Current Sense Resistor

A high-power resistor can be used for sensing the boost input current. Overcurrent condition is detected when the voltage across R_{ISENSE} reaches 220 mV. Typical 20 mΩ sense resistor is used to set 11-A input current limit. Sense resistor value can be increased to lower overcurrent limit for application as needed. Power rating can be calculated from the input current and resistance value.

9.2.1.2.11 Feedback Resistor Divider

Feedback resistors R_{FB1} and R_{FB2} determine the maximum boost output level. Output voltage can be calculated as in 式 14:

$$V_{OUT\_MAX} = \left(\frac{V_{BG}}{R_{FB2}} + I_{SEL\_MAX} \right) \times R_{FB1} + V_{BG} \quad (14)$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_{FB2} = 100 kΩ (recommended for boost mode)

9.2.1.2.12 Critical Components for Design

図 70 shows the critical part of circuitry: boost components, the LP8863-Q1 internal charge pump for gate-driver powering, and powering/grounding of LP8863-Q1. Schematic example is shown in 図 70.

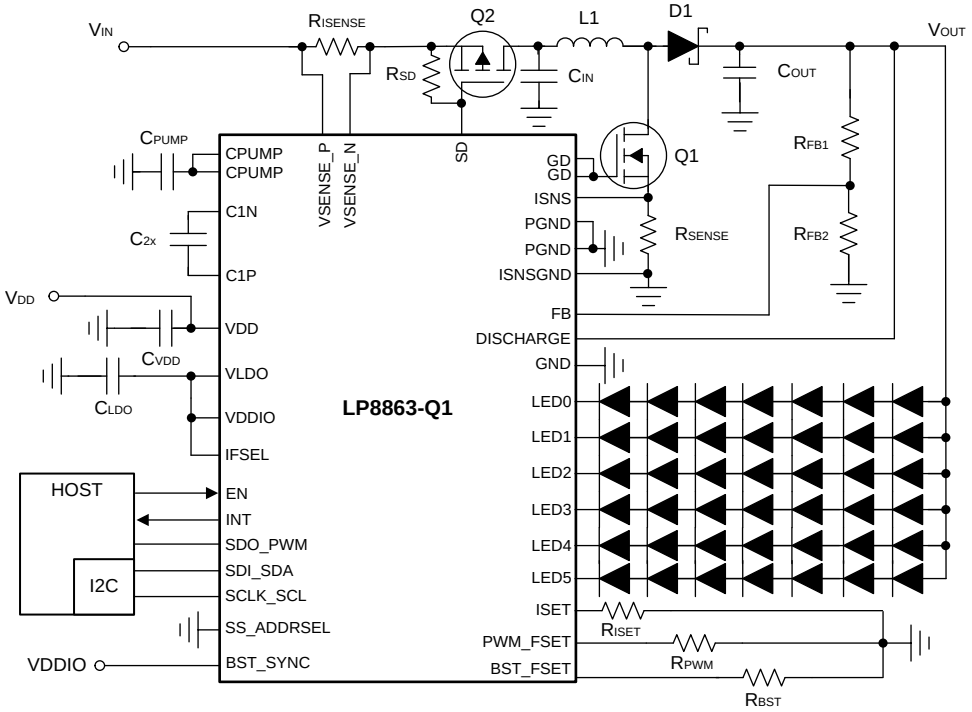
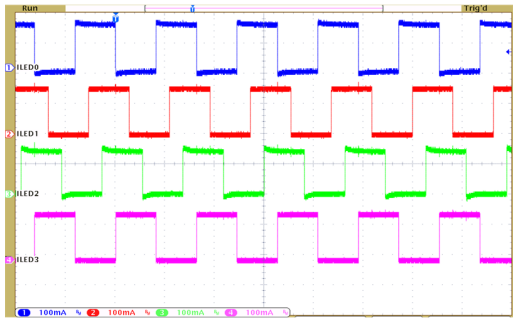


図 70. Critical Components for Full Feature Design

表 51. Recommended Component Values for Full Feature Design Example

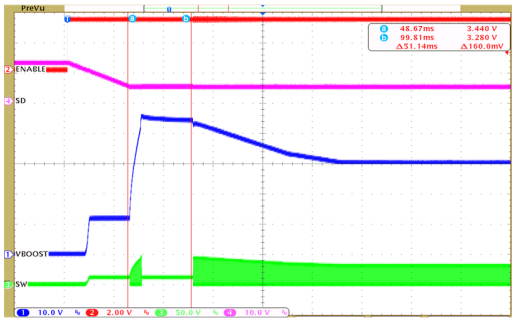
REFERENCE DESIGNATOR	DESCRIPTION	NOTE
R_{ISENSE}	20 mΩ, 3 W	Input current sensing resistor
R_{SD}	20 kΩ, 0.1 W	Power-line FET gate pullup resistor
R_{SENSE}	20 mΩ, 3 W	Boost current sensing resistor
R_{FB2}	100 kΩ, 0.1 W	Bottom feedback divider resistor
R_{FB1}	910 kΩ, 0.1 W	Top feedback divider resistor
R_{BST}	4.77 kΩ, 0.1 W	Boost frequency set resistor
R_{ISET}	31.2 kΩ, 0.1 W	Current set resistor for 100 mA maximum
R_{PWM}	42.2 kΩ, 0.1 W	Output PWM frequency set resistor
C_{PUMP}	10-µF, 16-V ceramic	Charge-pump output capacitor
C_{2X}	2.2-µF, 25-V ceramic	Flying capacitor
C_{VDD}	4.7-µF + 0.1-µF, 10-V ceramic	VDD bypass capacitor
C_{LDO}	4.7-µF + 0.1-µF, 10-V ceramic	VLDO bypass capacitor
C_{IN}	2 × 33-µF, 63-V electrolytic + 2 × 10-µF, 100-V ceramic	Boost input capacitor
C_{OUT}	2 × 33-µF, 63-V electrolytic + 2 × 10-µF, 100-V ceramic	Boost output capacitor
L1	22-µH saturation current 23 A	Boost inductor
D1	100 V, 10-A Schottky diode	Boost Schottky diode
Q1	60-V, 25-A nMOSFET	Boost nMOSFET
Q2	60-V, 30-A pMOSFET	Power-line FET

9.2.1.3 Application Curves



F_{LED_PWM} = 300 Hz Phase Shift 60° 6 Strings

図 71. LED String Currents Showing Phase Shift PWM Operation



f_{SW} = 400 kHz 100 mA/String
C_{IN} = C_{OUT} = 2 × 33 µF (electrolytic) + 2 × 10 µF (ceramic)

図 72. Typical Start-Up

9.2.2 Application With Basic/Minimal Operation

The LP8863-Q1 needs only a few external components for basic functionality if material cost and PCB area for a solution need to be minimized. In this example LP8863-Q1 is configured with external components and no I2C or SPI communication. The power-line FET is removed, as is input current sensing. Internal charge pump is not used, and all external synchronization functions and special features are disabled. Only 5 LED strings are enabled.

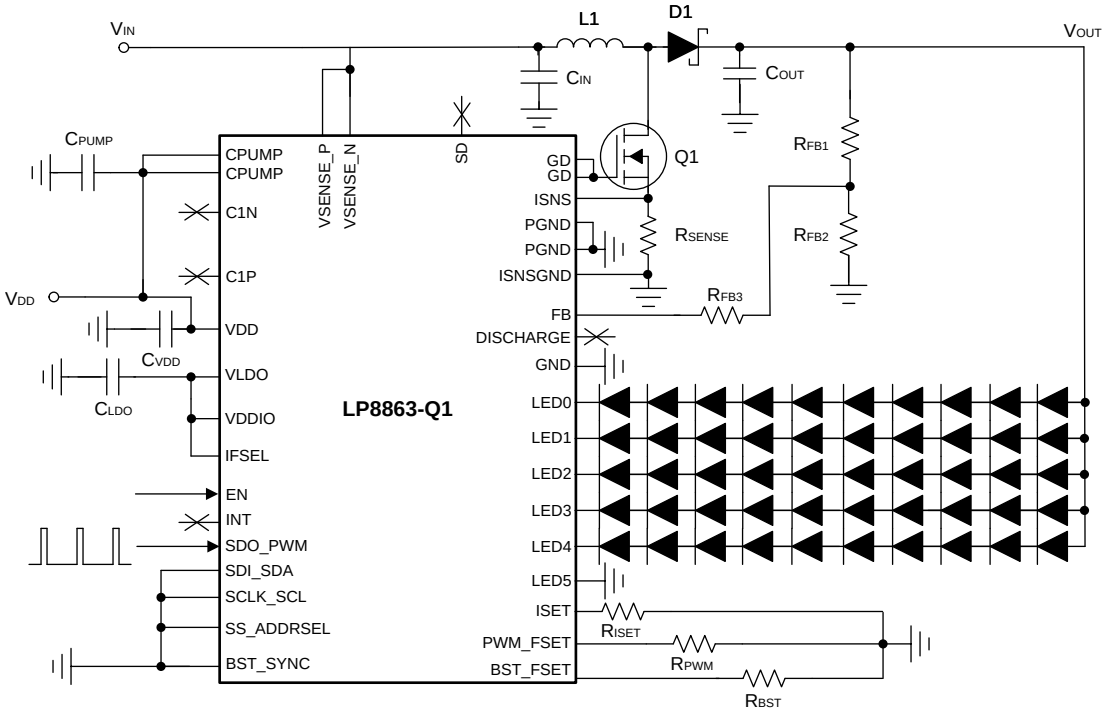


図 73. Minimal Solution/Minimum Components Application

9.2.2.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in 表 52:

表 52. LP8863-Q1 Minimal Solution Design Parameters

DESIGN PARAMETER	VALUE
V_{IN} voltage range	5 V to 30 V
V_{DD} voltage	5 V (note: 5 V required when charge pump disabled.)
LED strings configuration	5 strings, 10 LEDs in series
3-resistor feedback network	R_{FB1} = 100 kΩ, R_{FB2} = 6 kΩ , R_{FB3} = 27 kΩ (maximum output voltage set to 43.5 V)
Charge pump	Disabled
Brightness control	PWM input
Output configuration	LED0 to LED4 are in display mode (phase shift 72°); LED5 is not used (GND)
LED string current	150 mA
Boost frequency	300 kHz
Inductor	22 µH at 12-A saturation current
Power-line FET	Disabled
R_{SENSE}	20 mΩ
Power-line FET	Enabled
R_{SENSE}	20 mΩ
Input/Output capacitors	C_{IN} and C_{OUT}: 2 × 33-µF electrolytic + 2 × 10-µF ceramic
Spread spectrum	Disabled
Discharge function	Disabled

9.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure*

9.2.2.3 Application Curves

See *Application Curves*

9.2.3 SEPIC Mode Application

When LED string voltage can be above and below the input voltage level, use the SEPIC configuration. In SEPIC mode, the SW pin detects a maximum voltage equal to the sum of the input and output voltages, a consideration when selecting components. This fact limits the maximum output voltage to 24 V. External frequency can be used to synchronize boost or SEPIC switching frequency through the BST_SYNC pin.

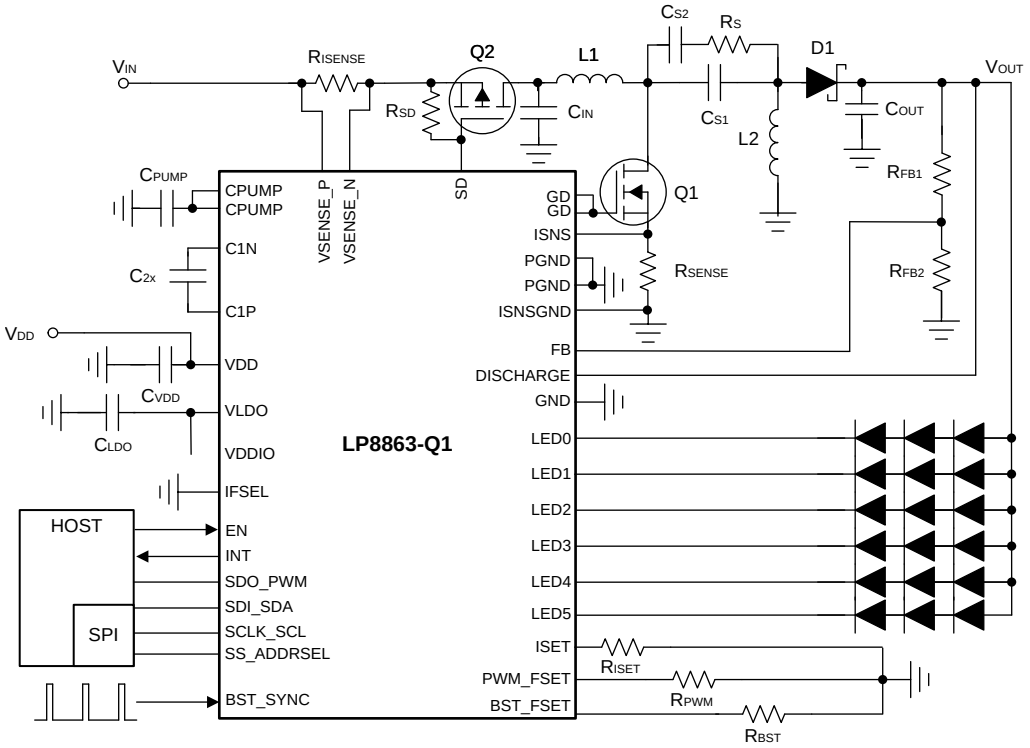


図 74. SEPIC Mode with Three LEDs in Series

9.2.3.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in 表 53:

表 53. LP8863-Q1 SEPIC Mode Design Parameters

DESIGN PARAMETER	VALUE
V_{IN} voltage range	3 V to 48 V
V_{DD} voltage	3.3 V
LED strings configuration	6 strings, 3 LEDs in series
Charge pump	Enabled
Brightness control	SPI
Output configuration	LED0 to LED5 are in display mode (phase shift 60°)
LED string current	150 mA
BST_SYNC external signal frequency	2.2 MHz (Note: BST_SYNC frequency must be 0.2 to 0.5% higher than frequency set by BST_FSET resistor.)
BST_FSET resistor	42.2 kΩ (sets boost frequency to 1.6 MHz)
Inductor	10 µH at 12-A saturation current
R_{ISENSE}	20 mΩ
Power-line FET	Enabled
R_{SENSE}	20 mΩ
Input/Output capacitors	C_{IN} and C_{OUT}: 2 × 33-µF electrolytic + 2 × 10-µF ceramic
Spread spectrum	Disabled
Discharge function	Enabled
Boost synchronization	Enabled

9.2.3.2 Detailed Design Procedure

9.2.3.2.1 Inductor Selection

Inductance for both inductors can be selected from 表 54, depending on operating frequency for the application. Current rating is recommended to be at least 25% higher than maximum inductor peak current. Peak-to-peak ripple current can be estimated to be approximately 40% of the maximum input current and and inductor peak current can be calculated with 式 15, 式 16, and 式 17:

表 54. Inductance Values for SEPIC Switching Frequencies

SW FREQUENCY (kHz)	INDUCTANCE (µH)
300	15
400	15
600	10
800	10
1000	6.8
1250	6.8
1667	4.7
2200	4.7

$$I_{L1(peak)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN(min)}} \times \left(1 + \frac{40\%}{2}\right)$$

where

- $I_{L1(peak)}$: Peak current for inductor 1
- I_{OUT}: Maximum output current
- V_{OUT}: Output voltage
- V_D: Diode forward voltage drop
- $V_{IN(min)}$: Minimum input voltage

(15)

$$I_{L2(peak)} = I_{OUT} \times \left(1 + \frac{40\%}{2}\right)$$

where

- $I_{L2(peak)}$: Peak current for inductor 2
- I_{OUT}: Maximum output current

(16)

$$\Delta I_L = I_{IN} \times 40\% = I_{OUT} \times \frac{V_{OUT}}{V_{IN(min)}} \times 40\%$$

where

- ΔI_L: Inductor ripple current
- I_{IN}: Input current
- V_{OUT}: Output voltage
- $V_{IN(min)}$: Minimum input voltage

(17)

9.2.3.2.2 Coupling Capacitor Selection

The coupling capacitors Cs isolate the input from the output and provide protection against a shorted load. The selection of SEPIC capacitors, Cs, depends mostly on the RMS current, which can be calculated with 式 18. The capacitors must be rated for a large RMS current relative to the output power; TI recommends at least 25% higher rating for I_{RMS}. When using uncoupled inductors, use one 10-µF ceramic capacitor in parallel with one 33-µF electrolytic capacitor and series 2-Ω resistor. If coupled inductors are used, then use only one 10-µF ceramic capacitor.

$$I_{Cs(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN(min)}}}$$

where

- $I_{Cs(rms)}$: RMS current of Cs capacitor
- I_{OUT}: Output current
- V_{OUT}: Output voltage
- V_D: Diode forward voltage drop
- $V_{IN(min)}$: Minimum input voltage

(18)

9.2.3.2.3 Output Capacitor Selection

See *Detailed Design Procedure*

9.2.3.2.4 Input Capacitor Selection

See *Detailed Design Procedure*

9.2.3.2.5 Charge Pump Output Capacitor

See *Detailed Design Procedure*

9.2.3.2.6 Charge Pump Flying Capacitor

See *Detailed Design Procedure*

9.2.3.2.7 Switching FET

Gate-drive voltage for the FET is V_{DD} or about 2 × V_{DD}, if the charge pump is enabled. Use an N-type MOSFET for the switching FET. The switching FET for SEPIC mode sees a maximum voltage of $V_{IN(max)}$ + V_{OUT}, 25% higher rating is recommended. Current rating is also recommended to be 25% higher than peak current, which can be calculated with 式 19. R_{DSON} must be as low as possible — less than 20 mΩ is recommended. Thermal resistance ($R_{\theta JA}$) must also be low to dissipate heat from power loss on switching FET. Typical rise/fall time values recommended are less than 10 ns.

$$I_{Q1(peak)} = I_{L1(peak)} + I_{L2(peak)}$$

where

- $I_{Q1(peak)}$: Peak current for switching FET
- $I_{L1(peak)}$: Peak current for inductor 1
- $I_{IL2(peak):}$: Peak current for inductor 2 BOOST_OCP (19)

9.2.3.2.8 Output Diode

A Schottky diode must be used for the SEPIC output diode. Current rating must be at least 25% higher than the maximum current, which is the same as switch peak current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. At maximum current, the forward voltage must be as low as possible; TI recommends less than 0.5 V. Reverse breakdown voltage of the Schottky diode must be able to withstand $V_{IN(max)}$ + $V_{OUT(max}$); at least 25% higher voltage rating is recommended. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause efficiency and load regulation to suffer.

9.2.3.2.9 Switching Sense Resistor

See *Detailed Design Procedure*

9.2.3.2.10 Power-Line FET

See *Detailed Design Procedure*

9.2.3.2.11 Input Current Sense Resistor

See *Detailed Design Procedure*

9.2.3.2.12 Feedback Resistor Divider

Feedback resistors R_{FB1} and R_{FB2} determine the maximum boost output level. Output voltage can be calculated as follows:

$$V_{OUT\_MAX} = \left(\frac{V_{BG}}{R_{FB2}} + I_{SEL\_MAX} \right) \times R_{FB1} + V_{BG}$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.7 µA
- R_{FB2} = 170 kΩ (recommended for SEPIC Mode) (20)

9.2.3.2.13 Critical Components for Design

図 75 shows the critical part of circuitry: SEPIC components, the LP8863-Q1 internal charge pump for gate-driver powering, and powering/grounding of LP8863-Q1. Schematic example is shown in 図 70.

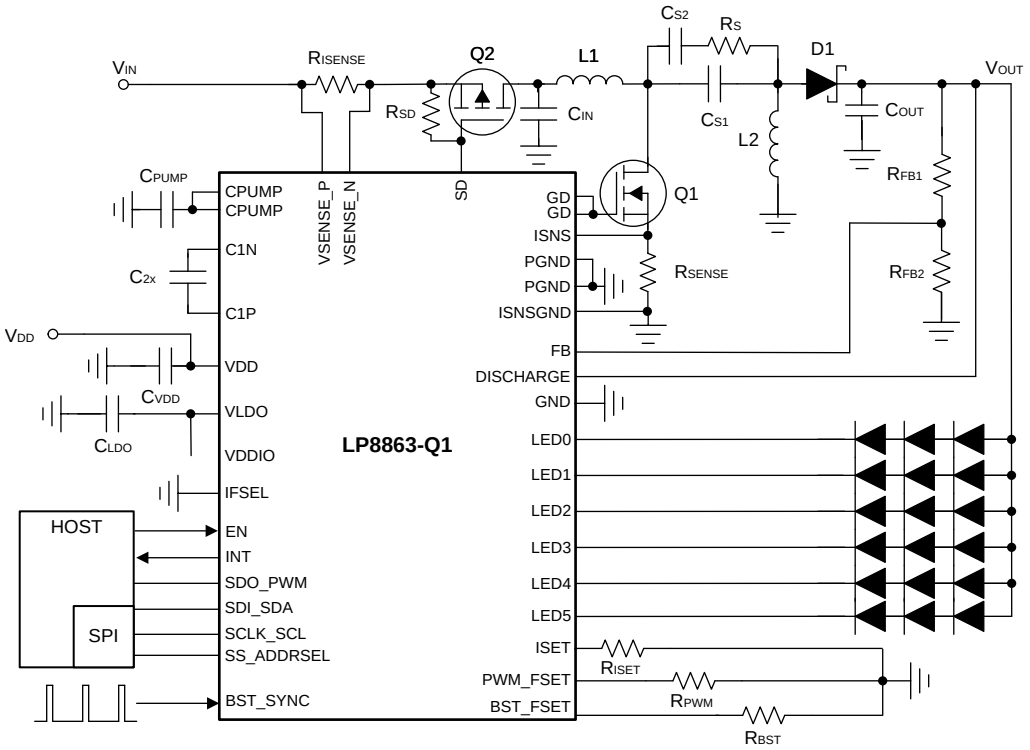


図 75. Critical Components for SEPIC Mode Design

表 55. Recommended Components for SEPIC Design Example

REFERENCE DESIGNATOR	DESCRIPTION	NOTE
R_{ISENSE}	20 mΩ, 3 W	Input current sensing resistor
R_{SD}	20 kΩ, 0.1 W	Power-line FET gate pullup resistor
R_{SENSE}	20 mΩ, 3 W	SEPIC current sensing resistor
R_{FB2}	170 kΩ, 0.1 W	Bottom feedback divider resistor
R_{FB1}	560 kΩ, 0.1 W	Top feedback divider resistor
R_{BST}	140 kΩ, 0.1 W	SEPIC frequency set resistor
R_{ISET}	20.5 kΩ, 0.1 W	Current set resistor for 150 mA max
R_{PWM}	140 kΩ, 0.1 W	Output PWM frequency set resistor
C_{PUMP}	10-µF, 16-V ceramic	Charge pump output capacitor
C2x	2.2-µF, 25-V ceramic	Flying capacitor
C_{VDD}	4.7-µF + 0.1-µF, 10-V ceramic	V_{DD} bypass capacitor
C_{LDO}	10-µF + 0.1-µF, 10-V ceramic	VLDO bypass capacitor
C_{IN}	2 × 33-µF, 63-V electrolytic	SEPIC input capacitor
C_{OUT}	2 × 33-µF, 63-V electrolytic	SEPIC output capacitor
C_{S1}	10-µF, 100-V ceramic	SEPIC coupling capacitor
C_{S2}	33-µF, 63-V electrolytic	SEPIC coupling capacitor
RS	2 Ω, 0.125 W	SEPIC resistor
L1	10-µH saturation current 15.5 A	SEPIC inductor
L2	10-µH saturation current 15.5 A	SEPIC inductor
D1	100-V 10-A Schottky diode	SEPIC Schottky diode
Q1	60-V, 25-A nMOSFET	SEPIC nMOSFET
Q2	60-V, 30-A pMOSFET	Power-line FET

9.2.3.3 Application Curves

See *Application Curves*

10 Power Supply Recommendations

The LP8863-Q1 is designed to operate from a car battery. The V_{IN} input must be protected from reverse voltage and voltage dump condition over 48 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected with long wires, additional bulk capacitance may be required in addition to normal input capacitor.

The voltage range for V_{DD} is 3 V to 5.5 V. A ceramic capacitor must be placed as close as possible to the VDD pin. The boost gate driver is powered from the CPUMP pins. A ceramic capacitor must be placed as close to the CPUMP pins as possible.

11 Layout

11.1 Layout Guidelines

図 76 shows a layout recommendation for the LP8863-Q1 used to illustrate the principles of good layout. This layout can be adapted to the actual application layout if and where possible. It is important that all boost components are close to each other and to the chip; the high-current traces must be wide enough. VDD must be as noise-free as possible. Place a V_{DD} bypass capacitor near the VDD and GND pins and ground it to a low-noise ground. A charge-pump capacitor, boost input capacitors, and boost output capacitors must be connected to PGND. Place the charge-pump capacitors close to the device. The main points to guide the PCB layout design:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to each other. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents follow the route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
  - For high frequency the copper area capacitance must be taken into account. For example, the copper area for the drain of boost nMOSFET is a tradeoff between capacitance and the cooling capacity of the components.
- GND plane must be intact under the high-current-boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting must be in the same direction in optimal case.
- Inductors must be placed so that the current flows in the same direction as in the current loops. Rotating the inductor 180° changes current direction.
- Use separate power and noise-free grounds. PGND is used for boost converter return current. Use a low-noise ground for more sensitive signals, like VDD bypass capacitor grounding as well as grounding the GND pins of the LP8863-Q1 device itself.
- Route boost output voltage (V_{OUT}) to LEDs from output capacitors not straight from the diode cathode.
- A small bypass capacitor (TI recommends a 39-pF capacitor) must be placed close to the FB pin to suppress high frequency noise
- VDD line must be separated from the high current supply path to the boost converter to prevent high frequency ripple affecting the chip behavior. A separate 1-µF bypass capacitor is used for the VDD pin, and it is grounded to noise-free ground.
- Capacitor connected to charge pump output CPUMP must have 10-µF capacitance, grounded by the shortest way to boost a switch-current-sensing resistor. This capacitor must be as close as possible to CPUMP pin. This capacitor provides a greater peak current for gate driver and must be used even if the charge pump is disabled. If the charge pump is disabled, the VDD and CPUMP pins must be tied together.
- Input and output capacitors need low-impedence grounding (wide traces with many vias to PGND plane).
- If two or more output capacitors are used, symmetrical layout must be used to get all capacitors working ideally.
- Input/output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable under certain load conditions. DC bias characteristics should be obtained from the component manufacturer; DC bias is not taken into account on component tolerance. TI recommends X5R/X7R capacitors.

11.2 Layout Example

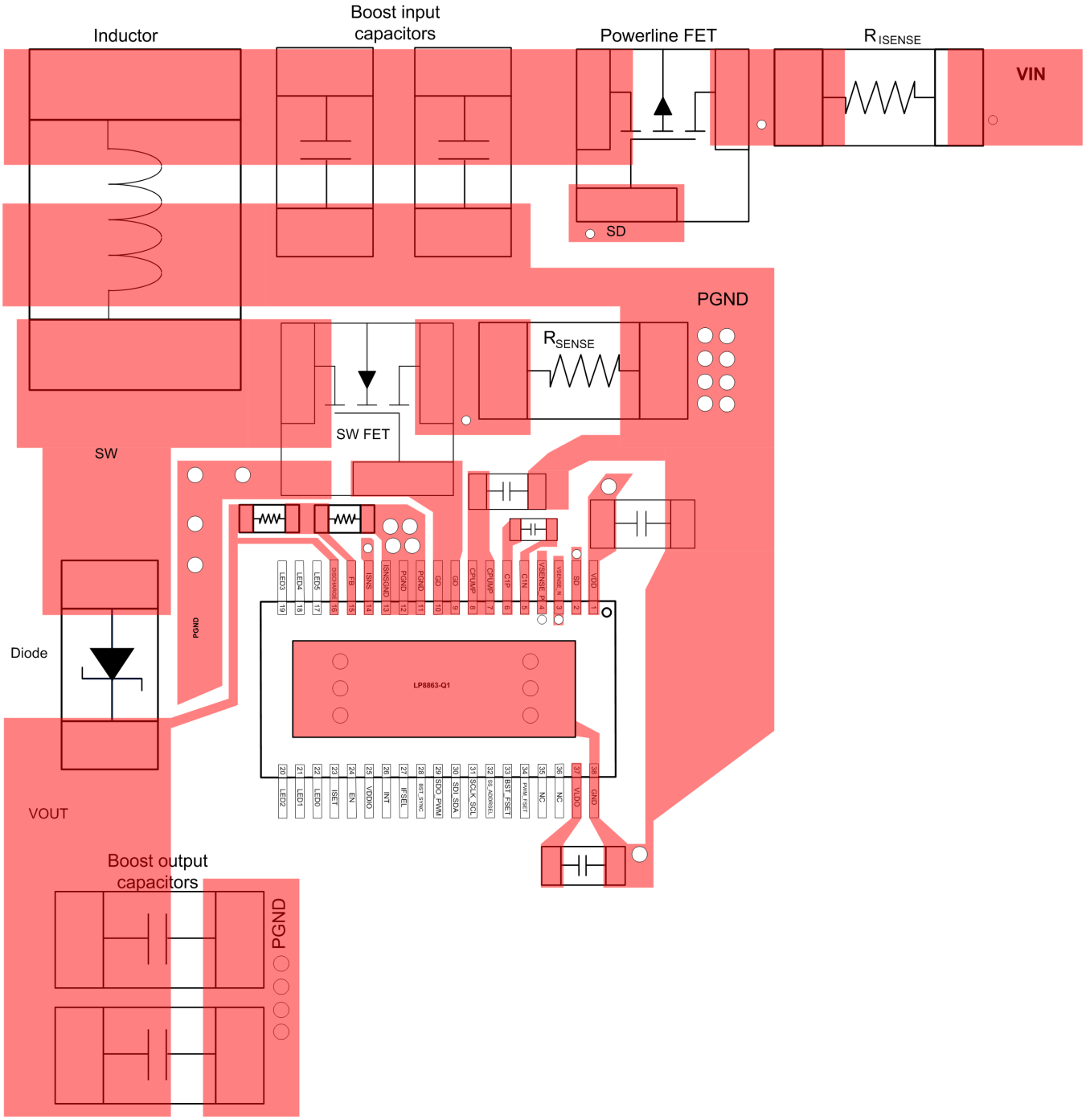


図 76. LP8863-Q1 Layout Guidelines

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8863ADCPRQ1	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LP8863AQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

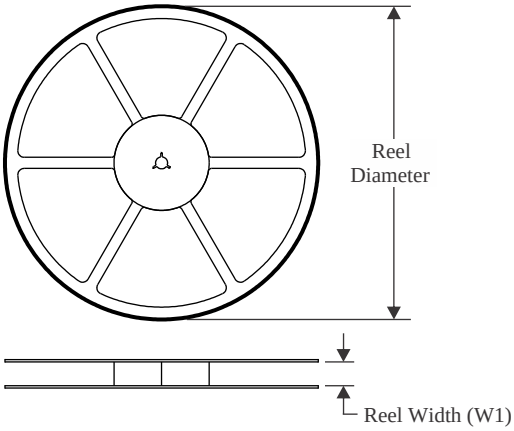
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

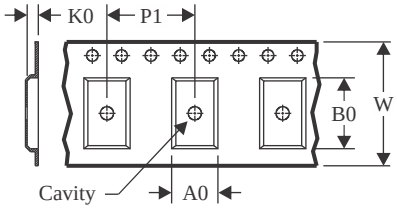
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

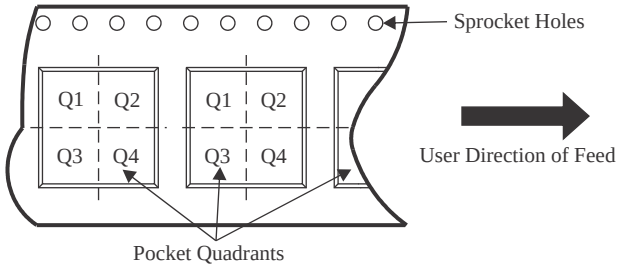


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

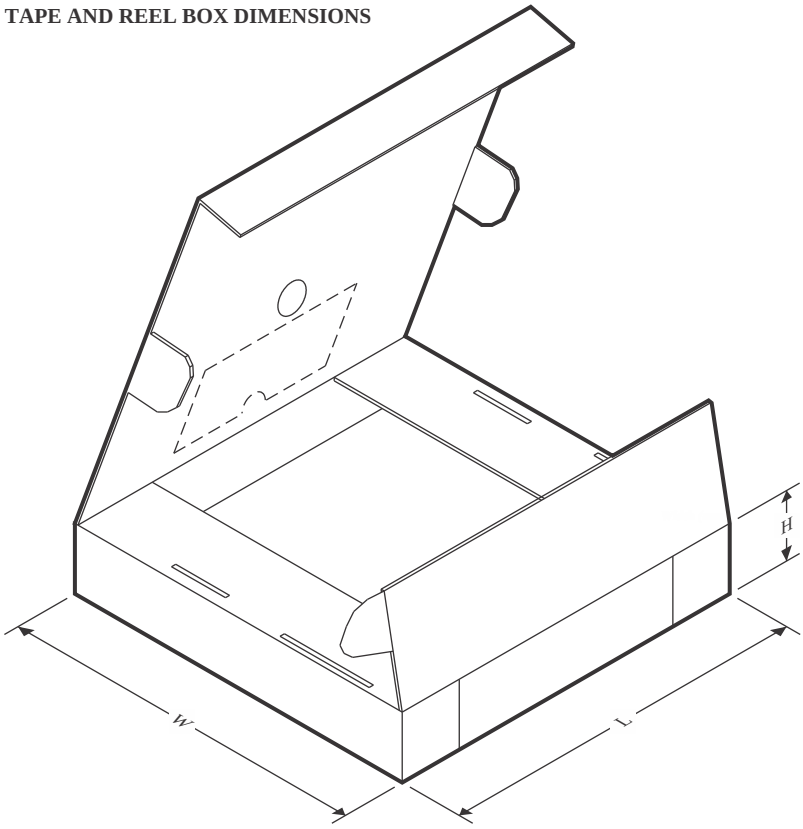
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8863ADCPRQ1	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8863ADCPRQ1	HTSSOP	DCP	38	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

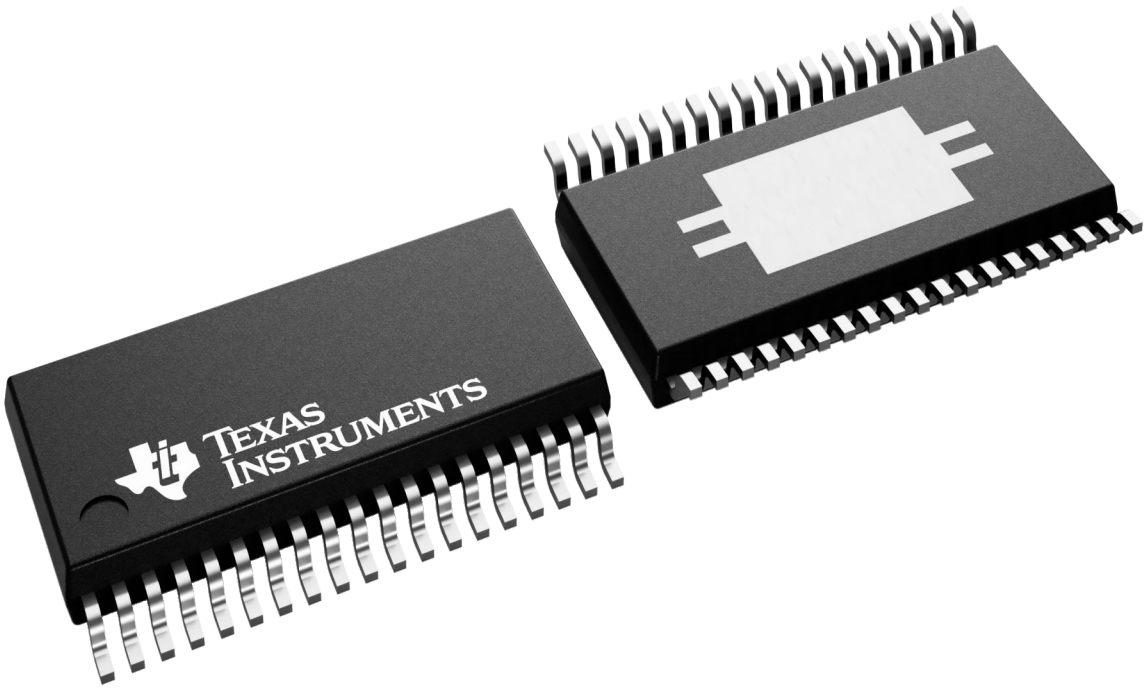
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

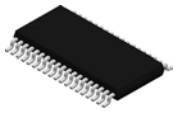
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

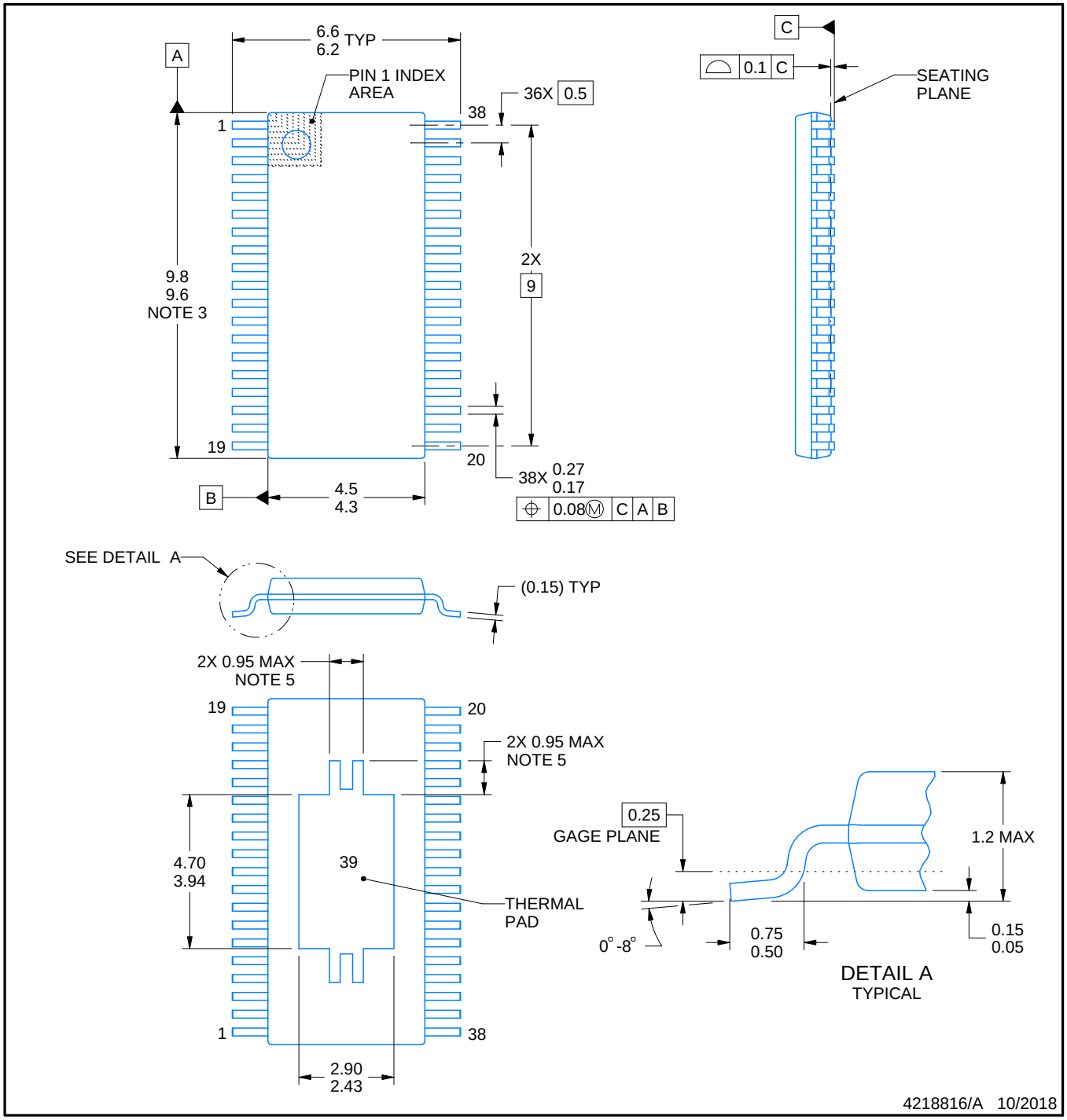
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

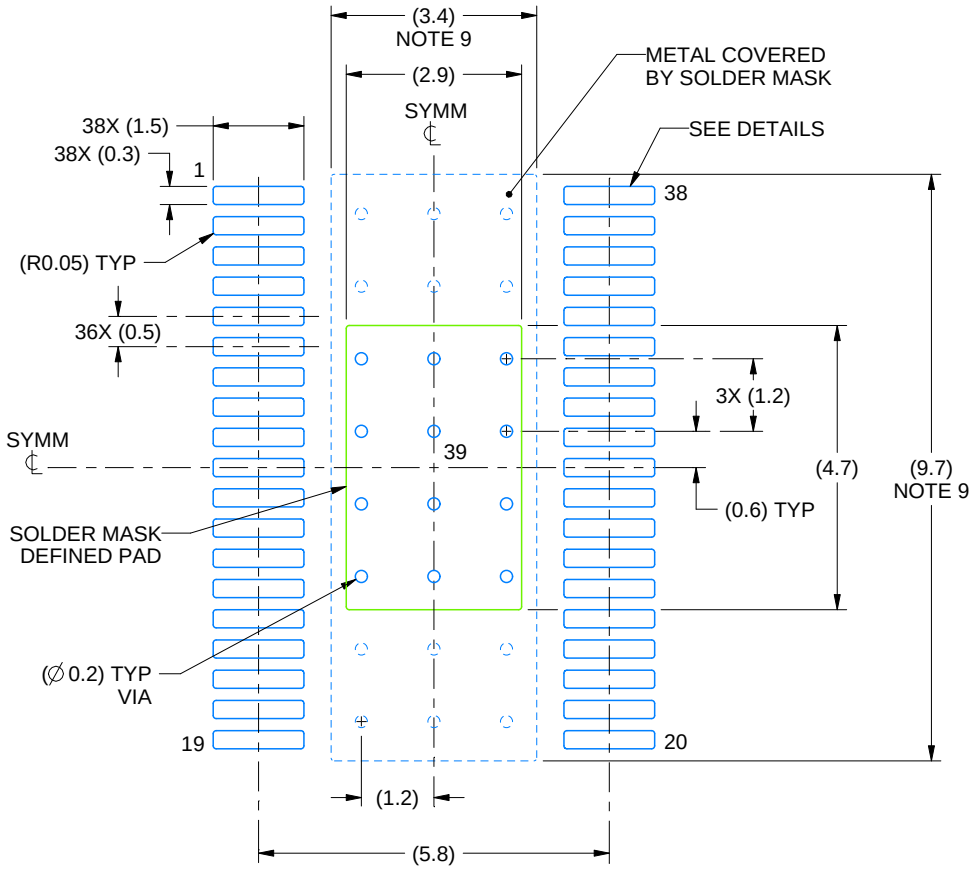
SMALL OUTLINE PACKAGE



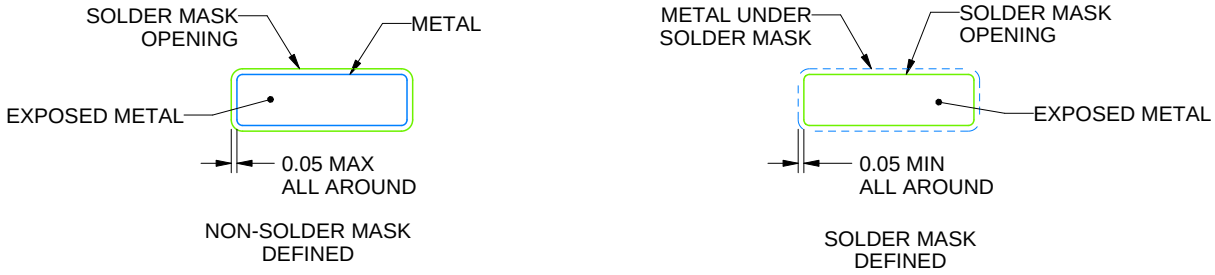
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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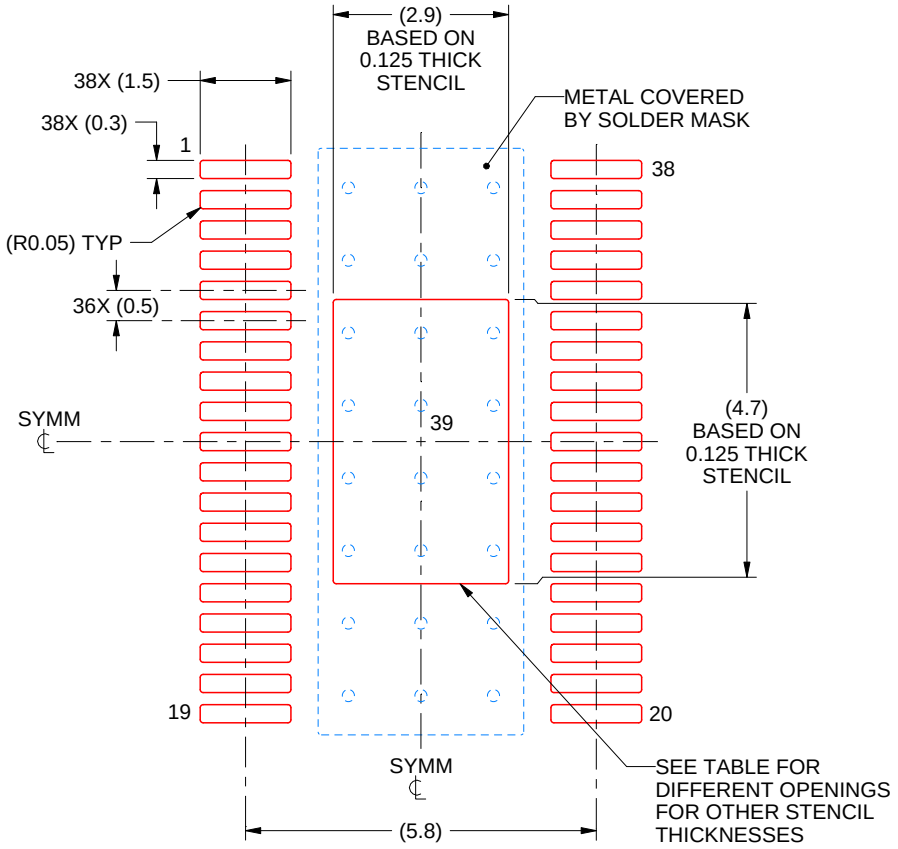
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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