LV14360 軽負荷時の効率が高い 60V 3A 降圧コンバータ

1 特長

- 4.3V～60V の入力範囲
- 3A の連続出力電流
- 動作時の静止電流：300μA
- 155mΩ のハイサイド MOSFET
- 電流モード制御
- 200kHz～2MHz の可変スイッチング周波数
- 外部クロックへの周波数同期
- 設計を容易にする内部補償
- 高いデューティ・サイクルでの動作をサポート
- 高精度イネーブル入力
- シャットダウン時電流：1μA
- 過熱 / 過電圧 / 短絡保護
- PowerPAD™ 付き 8 ピン HSOIC パッケージ

2 アプリケーション

- 産業用電源
- 通信機器とデータ通信モジュール
- V_{IN} が広い汎用レギュレーション

3 概要

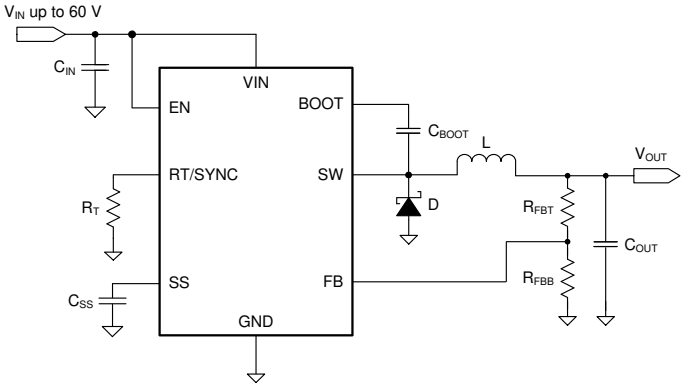
LV14360 は、ハイサイド MOSFET を内蔵した 60V、3A の降圧型レギュレータです。4.3V～60V という幅広い入力範囲により、産業用から車載向けまで、非レギュレーション電源からの電源調整を行うさまざまなアプリケーションに適しています。本レギュレータのスリープ・モードの静止電流は 300μA であり、バッテリ駆動システムに適しています。シャットダウン・モード電流も 1μA ときわめて低いことから、バッテリ駆動時間のさらなる延長が可能です。調整可能なスイッチング周波数の範囲が広いため、効率と外部部品のサイズを最適化できます。内部ループ補償により、ユーザーはループ補償を設計する煩雑な作業から解放されます。また、本デバイスの外付け部品の数も最小限で済みます。高精度のイネーブル入力により、レギュレータの制御とシステムの電源シーケンスが単純化されます。このデバイスには、サイクル単位の電流制限、熱センシング、過剰な消費電力によるサーマル・シャットダウン、出力過電圧保護などの保護機能も組み込まれています。

LV14360 は、熱抵抗を下げるための露出パッドを備えた 8 ピン、4.89mm × 3.9mm HSOIC パッケージで供給されます。

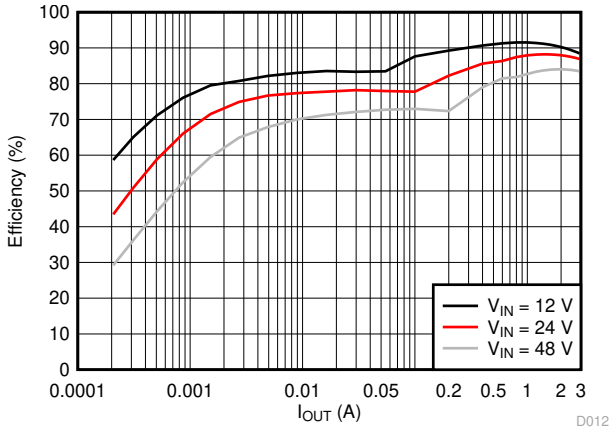
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
LV14360	HSOIC	4.89mm × 3.9mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ソフト・スタート (SS) オプションの概略回路図



効率と出力電流との関係
V_{OUT} = 5V、f_{sw} = 500kHz

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (August 2017) to Revision A (September 2020)	Page
• 最初の公開リリース	1
• 文書全体にわたって表、図、相互参照の採番方法を更新	1

5 Device Comparison Table

PART NUMBER	FEATURE
LV14360P	Power Good
LV14360S	Soft start

6 Pin Configuration and Functions

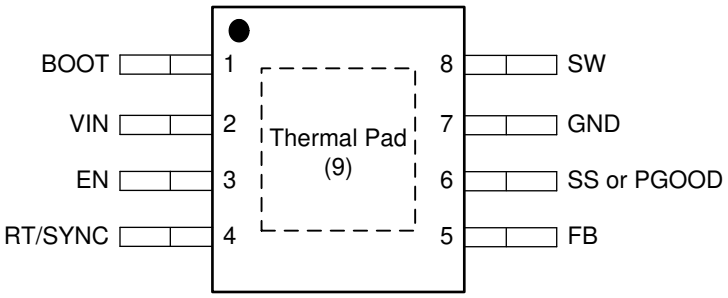


図 6-1. DDA Package 8-Pin HSOIC Top View

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	BOOT	P	Bootstrap capacitor connection for high-side MOSFET driver. Connect a high quality 0.1-µF capacitor from BOOT to SW.
2	VIN	P	Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and GND must be as short as possible.
3	EN	A	Enable pin with internal pullup current source. Pull below 1.2 V to disable. Float or connect to VIN to enable. Adjust the input undervoltage lockout with two resistors (see *セクション 8.3.6*).
4	RT/SYNC	A	Resistor timing or external clock input. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled, and the operating mode returns to frequency programming by resistor.
5	FB	A	Feedback input pin, connect to the feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
6	SS or PGOOD	A	SS pin for soft-start version, connect to a capacitor to set soft-start time. The PGOOD pin for power-good version, open-drain output for power-good flag, use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 7 V.
7	GND	G	System ground pin
8	SW	P	Switching output of the regulator. Internally connected to high-side power MOSFET. Connect to power inductor.
9	Thermal Pad	G	Major heat dissipation path of the die. Must be connected to ground plane on PCB.

(1) A = Analog, P = Power, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	VIN, EN to GND	–0.3	65	V
	BOOT to GND	–0.3	71	
	SS to GND	–0.3	5	
	FB to GND	–0.3	7	
	RT/SYNC to GND	–0.3	3.6	
	PGOOD to GND	–0.3	7	
Output voltages	BOOT to SW		6.5	V
	SW to GND	–3	65	
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2000	V
		Charged-device model (CDM) (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Buck regulator	VIN	4.3	60	V
	VOUT	0.8	50	
	BOOT		66	
	SW	–1	60	
	FB	0	5	
Control	EN	0	60	V
	RT/SYNC	0	3.3	
	SS	0	3	
	PGOOD to GND	0	5	
Frequency	Switching frequency range at RT mode	200	2000	kHz
	Switching frequency range at SYNC mode	250	2000	
Temperature	Operating junction temperature, T_J	–40	125	°C

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *セクション 7.5*.

7.4 Thermal Information

THERMAL METRIC (1) (2)		LV14360 DDA (HSOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Power rating at a specific ambient temperature T_A should be determined with a maximum junction temperature (T_J) of 125°C (see *セクション 7.3*).

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 4.3 V to 60 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4.3		60	V
UVLO	Under voltage lockout thresholds	Rising threshold	3.8	4	4.2	V
		Hysteresis		285		mV
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, T_A = 25°C, 4.3 V ≤ V_{IN} ≤ 60 V		1	3	µA
I_Q	Operating quiescent current (non- switching)	V_{FB} = 1 V, T_A = 25°C		300		µA
ENABLE (EN PIN)						
V_{EN_TH}	EN Threshold Voltage		1.05	1.20	1.38	V
I_{EN_PIN}	EN PIN current	Enable threshold 50 mV		–4.6		µA
		Enable threshold –50 mV		–1		
I_{EN_HYS}	EN hysteresis current			–3.6		µA
SOFT START						
I_{SS}	SS pin current	For external soft-start version only, T_A = 25°C		–3		µA
t_{SS}	Internal soft-start time	For power-good version only, 10% to 90% of FB voltage		4		ms
POWER GOOD (PGOOD PIN)						
V_{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		94%		
		POWER BAD (% of FB voltage)		92%		
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		109%		
		POWER GOOD (% of FB voltage)		107%		
V_{PG_HYS}	Power-good flag recovery hysteresis	% of FB voltage		2%		
I_{PG}	PGOOD leakage current at high level output	V_{PULLUP} = 5 V		10	200	nA
V_{PG_LOW}	PGOOD low level output voltage	I_{PULLUP} = 1 mA		0.1		V
$V_{IN\_PG\_MIN}$	Minimum V_{IN} for valid PGOOD output	V_{PULLUP} < 5 V at I_{PULLUP} = 100 µA		1.6	1.95	V

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = 4.3 V to 60 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage	T_J = 25°C	0.746	0.75	0.754	V
		T_J = –40°C to 125°C	0.735	0.75	0.765	V
HIGH-SIDE MOSFET						
R_{DS_ON}	On-resistance	V_{IN} = 12 V, BOOT to SW = 5.8 V		155	320	mΩ
HIGH-SIDE MOSFET CURRENT LIMIT						
I_{LIMT}	Current limit	V_{IN} = 12 V, T_A = 25°C, Open Loop	3.8	4.75	5.7	A
THERMAL PERFORMANCE						
T_{SHDN}	Thermal shutdown threshold			170		°C
T_{HYS}	Hysteresis			12		

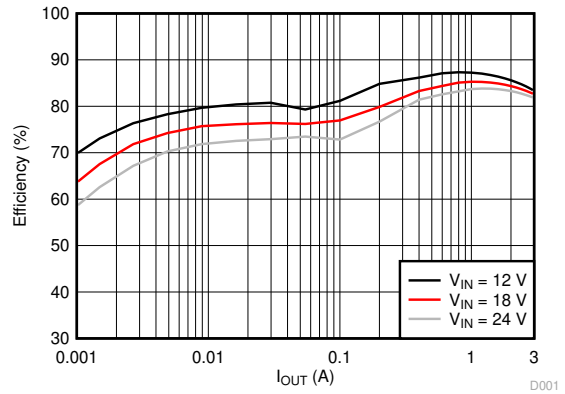
7.6 Switching Characteristics

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	R_T = 11.5 kΩ		1912		kHz
	Switching frequency range at SYNC mode		250		2000	
V_{SYNC_HI}	SYNC clock high level threshold		1.7			V
V_{SYNC_LO}	SYNC clock low level threshold				0.5	
T_{SYNC_MIN}	Minimum SYNC input pulse width	Measured at 500 kHz, V_{SYNC_HI} > 3 V, V_{SYNC_LO} < 0.3 V		30		ns
T_{LOCK_IN}	PLL lock in time	Measured at 500 kHz		100		µs
T_{ON_MIN}	Minimum controllable on time	V_{IN} = 12 V, BOOT to SW = 5.8 V, I_{Load} = 1 A		100		ns
D_{MAX}	Maximum duty cycle	f_{SW} = 200 kHz		90%		

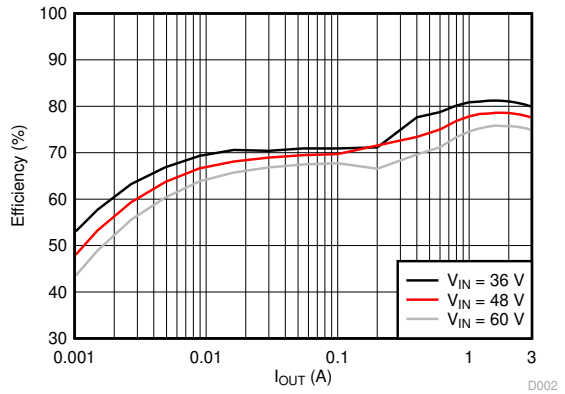
7.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, f_{SW} = 500 KHz, L = 8.2 µH, C_{OUT} = 2 × 47 µF, T_A = 25°C.



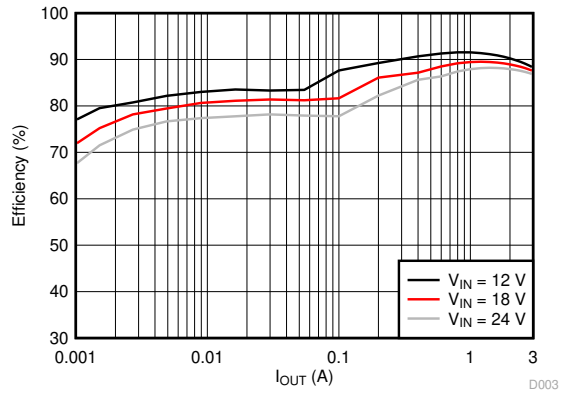
V_{OUT} = 3.3 V f_{SW} = 500 KHz

図 7-1. Efficiency vs Load Current



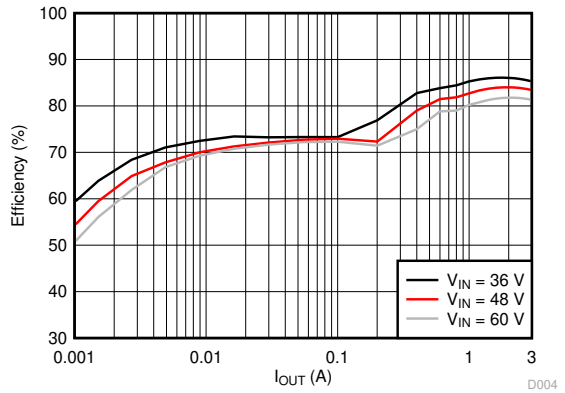
V_{OUT} = 3.3 V f_{SW} = 500 KHz

図 7-2. Efficiency vs Load Current



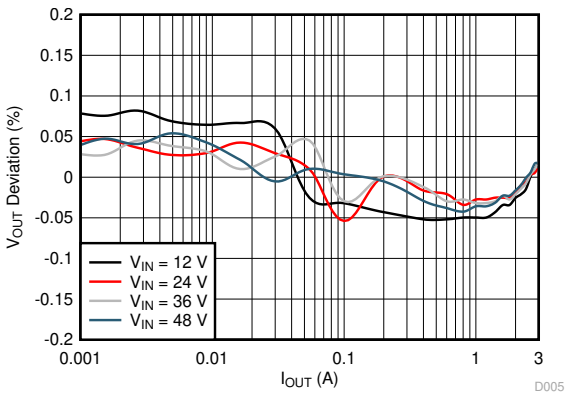
V_{OUT} = 5 V f_{SW} = 500 KHz

図 7-3. Efficiency vs Load Current



V_{OUT} = 5 V f_{SW} = 500 KHz

図 7-4. Efficiency vs Load Current



V_{OUT} = 5 V f_{SW} = 500 KHz

図 7-5. Load Regulation

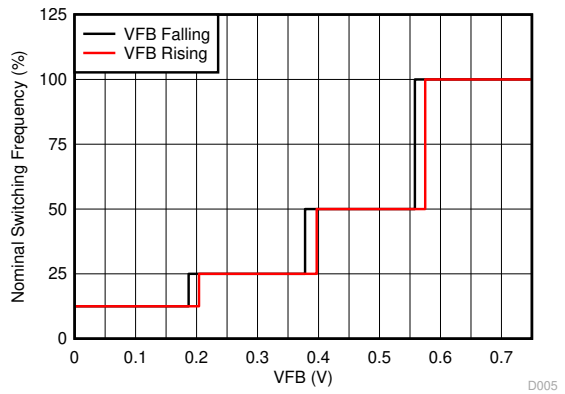
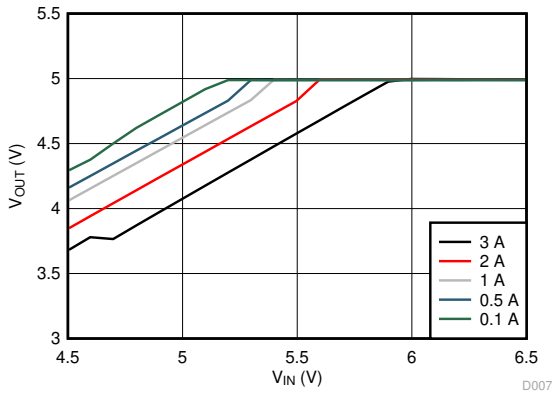
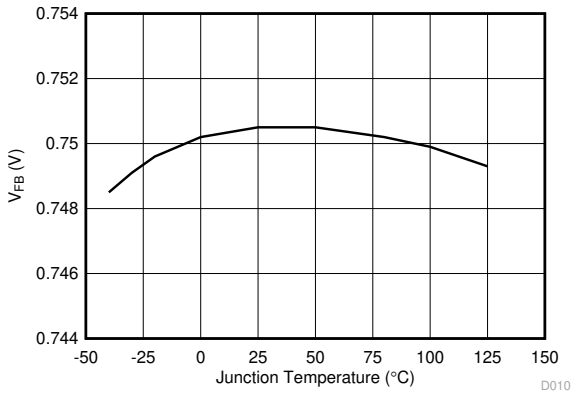


図 7-6. Frequency vs V_{FB}



V_{OUT} = 5 V f_{SW} = 500 KHz

図 7-7. Dropout Curve



V_{IN} = 12 V

図 7-8. Voltage Reference vs Junction Temperature

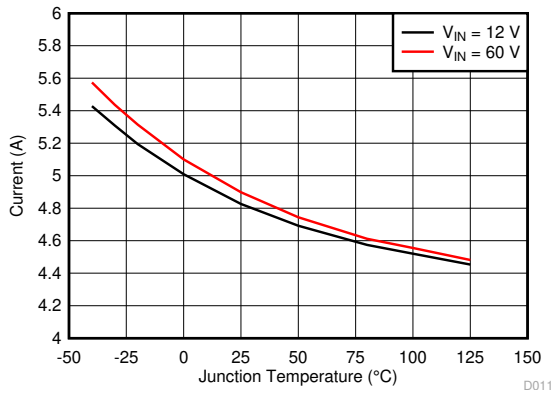
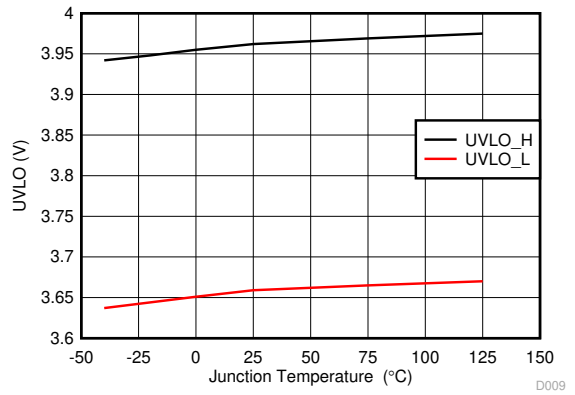


図 7-9. High-Side Current Limit vs Junction Temperature



I_{OUT} = 0 A

図 7-10. UVLO Threshold

8 Detailed Description

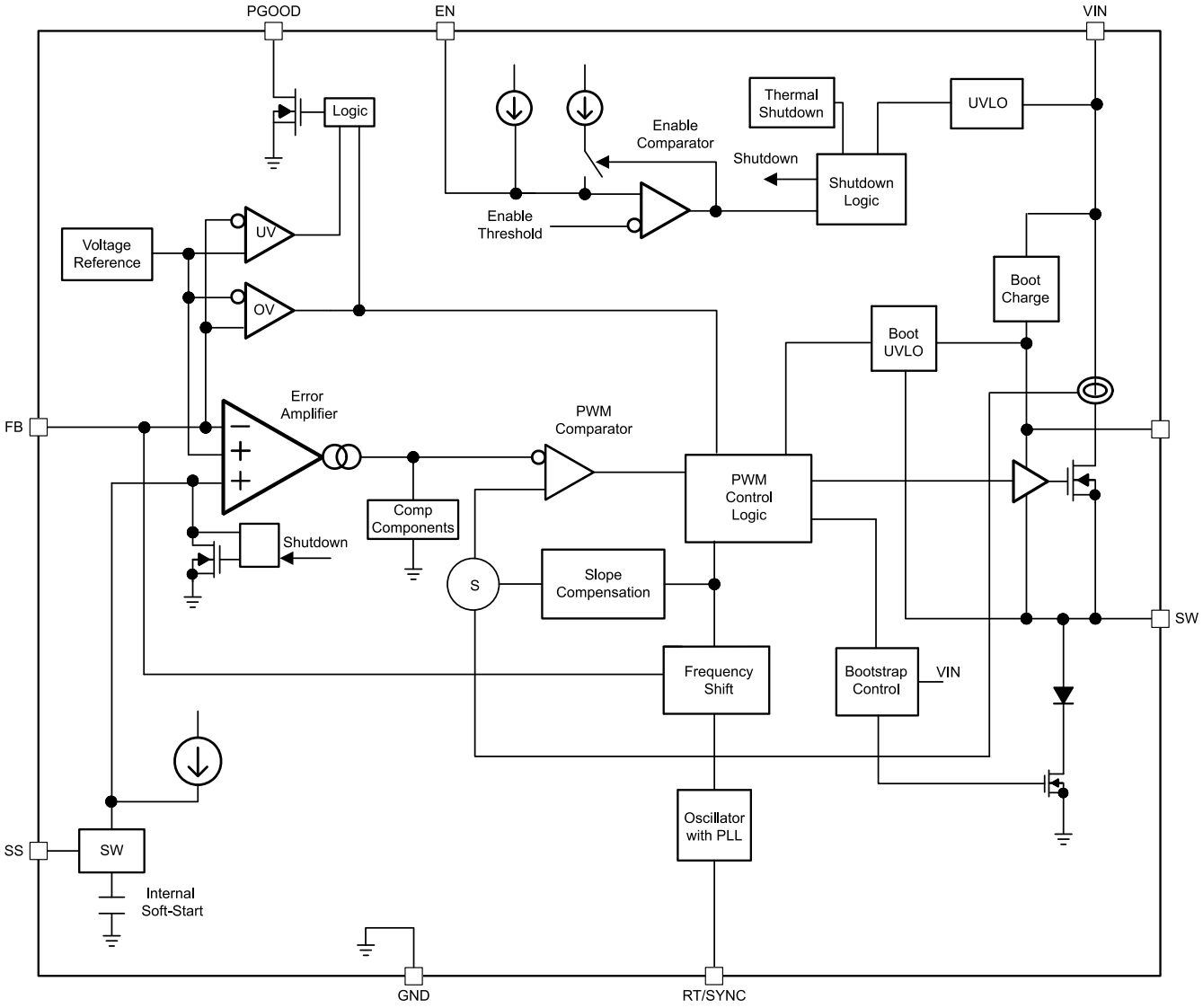
8.1 Overview

The LV14360 regulator is an easy-to-use step-down DC-DC converter that operates from a 4.3-V to 60-V supply voltage. The device integrates a 155-mΩ (typical) high-side MOSFET and is capable of delivering up to 3-A DC load current with exceptional efficiency and thermal performance in a very small solution size. The operating current is typically 300 µA under no load condition (not switching). When the device is disabled, the supply current is typically 1 µA. An extended family is available in 1-A and 2-A load options in pin-to-pin compatible packages.

The LV14360 implements constant frequency peak current mode control with sleep mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2 MHz by an external resistor R_T. The LV14360 is also capable of synchronization to an external clock within the 250-kHz to 2 MHz frequency range, which allows the device to be optimized to fit small board space at higher frequency, or high efficient power conversion at lower frequency.

Other features are included for more comprehensive system requirements, including precision enable, adjustable soft-start time, and approximate 90% duty cycle by BOOT capacitor recharge circuit. These features provide a flexible and easy-to-use platform for a wide range of applications. Protection features include over temperature shutdown, V_{OUT} overvoltage protection (OVP), V_{IN} undervoltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with frequency foldback.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LV14360 refers to セクション 8.2 and to the waveforms in 図 8-1. The LV14360 output voltage is regulated by turning on the high-side N-MOSFET with controlled ON time. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increases with linear slope ($V_{IN} – V_{OUT}$) / L. When the high-side switch is off, inductor current discharges through a freewheel diode with a slope of $–V_{OUT}$ / L. The control parameter of buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON-time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal Buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

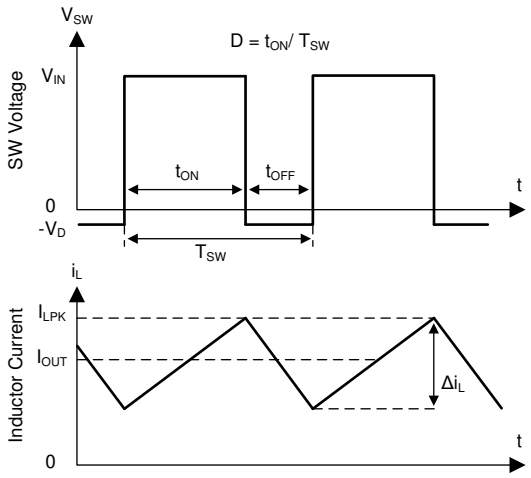


図 8-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LV14360 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At very light load, the LV14360 operates in sleep mode to maintain high efficiency and switching frequency will decrease with reduced load current.

8.3.2 Slope Compensation

The LV14360 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents subharmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

8.3.3 Sleep Mode

The LV14360 operates in sleep mode at light load currents to improve efficiency by reducing switching and gate-drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the current threshold of 300 mA, the device enters sleep mode. The sleep-mode current threshold is the peak switch current level corresponding to a nominal internal COMP voltage of 400 mV.

When in sleep mode, the internal COMP voltage is clamped at 400 mV and the high-side MOSFET is inhibited, and the device draws only 300 µA (typical) input quiescent current. Since the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the internal COMP voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts internal COMP voltage above 400 mV. The output voltage recovers to the regulated value, and internal COMP voltage eventually falls below the sleep-mode threshold at which time the device again enters sleep mode.

8.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The LV14360 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or greater for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the LV14360 operates at approximate 90% duty cycle. When the high-side MOSFET is continuously on for five or six switching cycles (five or six switching cycles for frequency lower than 1 MHz, and 10 or 11 switching cycles for frequency higher than 1 MHz) and the voltage from BOOT to SW drops below 3.2 V, the high-side MOSFET is turned off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor.

Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 90%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage, and the printed circuit board resistance.

8.3.5 Adjustable Output Voltage

The internal voltage reference produces a precise 0.75 V (typical) voltage reference over the operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or less divider resistors. Select the low side resistor R_{FBB} for the desired divider current and use 式 1 to calculate high-side R_{FBT}. Larger value divider resistors are good for efficiency at light load. However, if the values are too high, the regulator will be more susceptible to noise and voltage errors from the FB input current may become noticeable. R_{FBB} in the range from 10 kΩ to 100 kΩ is recommended for most applications.

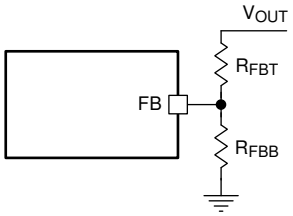


図 8-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} \times R_{FBB} \quad (1)$$

8.3.6 Enable and Adjustable Undervoltage Lockout

The LV14360 is enabled when the VIN pin voltage rises above 4 V (typical) and the EN pin voltage exceeds the enable threshold of 1.2 V (typical). The LV14360 is disabled when the VIN pin voltage falls below 3.715 V (typical) or when the EN pin voltage is below 1.2 V. The EN pin has an internal pullup current source (typically I_{EN} = 1 µA) that enables operation of the LV14360 when the EN pin is floating.

Many applications will benefit from the employment of an enable divider R_{ENT} and R_{ENB} in 図 8-3 to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

When EN terminal voltage exceeds 1.2 V, an additional hysteresis current (typically I_{HYS} = 3.6 µA) is sourced out of EN terminal. When the EN terminal is pulled below 1.2 V, I_{HYS} current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use 式 2 and 式 3 to calculate R_{ENT} and R_{ENB} for desired UVLO hysteresis voltage.

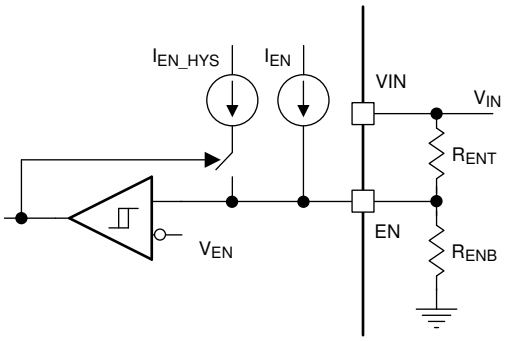


図 8-3. System UVLO By Enable Dividers

$$R_{ENT} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R_{ENB} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{ENT}} + I_{EN}} \quad (3)$$

where

- V_{START} is the desired voltage threshold to enable LV14360
- V_{STOP} is the desired voltage threshold to disable device
- I_{EN} = 1 µA
- I_{HYS} = 3.6 µA, typically

8.3.7 External Soft Start

The LV14360S has an external soft-start pin for programmable output ramp up time. The soft-start feature is used to prevent inrush current impacting the LV14360 and its load when power is first applied. The soft-start time can be programed by connecting an external capacitor C_{SS} from SS pin to GND. An internal current source (typically I_{SS} = 3 µA) charges C_{SS} and generates a ramp from 0 V to V_{REF}. The soft-start time can be calculated by 式 4:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (4)$$

The internal soft start resets while device is disabled or in thermal shutdown.

8.3.8 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the LV14360 can be programmed by the resistor RT from the RT/SYNC pin and GND pin. The RT/SYNC pin cannot be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use 式 5 or the curve in 図 8-4. 表 8-1 gives typical R_T values for a given f_{SW}.

$$R_T(k\Omega) = 42904 \times f_{SW}(kHz)^{-1.088} \quad (5)$$

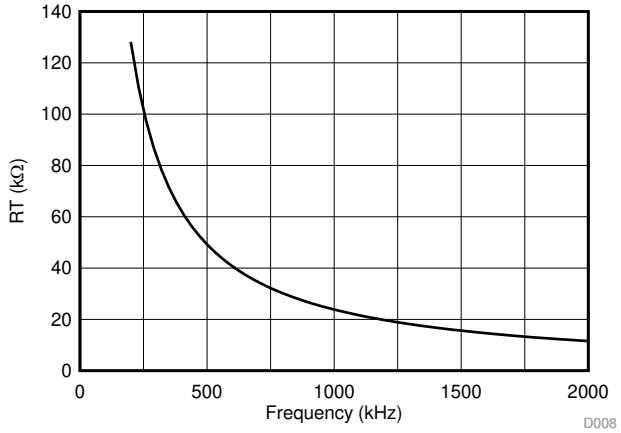


図 8-4. RT vs Frequency Curve

表 8-1. Typical Frequency Setting RT Resistance

f_{SW} (kHz)	R_T (kΩ)
200	133
350	73.2
500	49.9

表 8-1. Typical Frequency Setting RT Resistance (continued)

f_{SW} (kHz)	R_T (kΩ)
750	32.4
1000	23.2
1500	15.0
1912	11.5
2000	11

The LV14360 switching action can also be synchronized to an external clock from 250 kHz to 2 MHz. Connect a square wave to the RT/SYNC pin through either circuit network shown in 図 8-5. Internal oscillator is synchronized by the falling edge of external clock. The recommendations for the external clock include: high level no lower than 1.7 V, low level no higher than 0.5 V, and have a pulse width greater than 30 ns. When using a low impedance signal source, the frequency setting resistor R_T is connected in parallel with an AC coupling capacitor C_{COUP} to a termination resistor R_{TERM} (for example, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10-pF ceramic capacitor can be used for C_{COUP}. 図 8-6, 図 8-7, and 図 8-8 show the device synchronized to an external system clock.

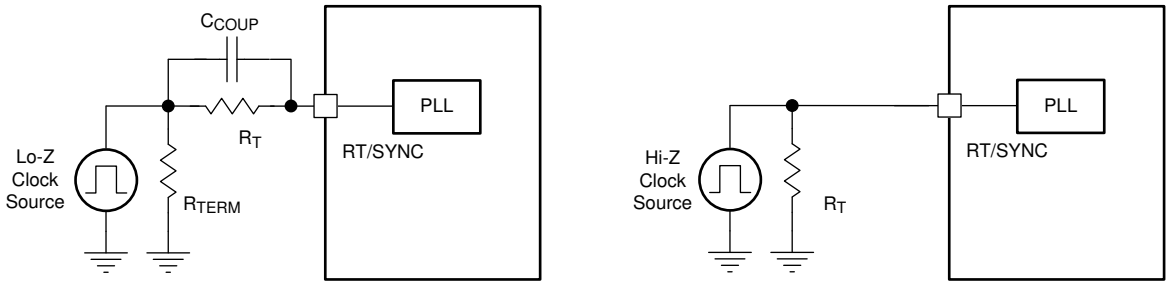


図 8-5. Synchronizing to an External Clock

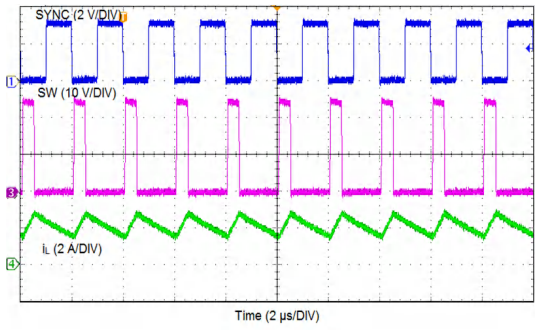


図 8-6. Synchronizing in CCM

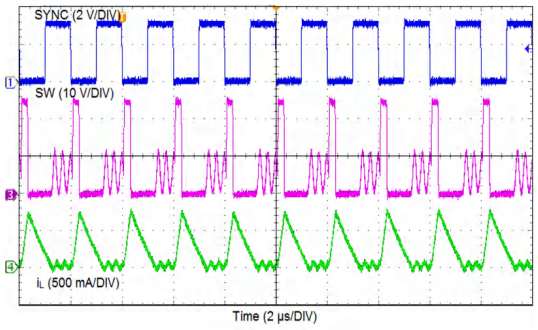


図 8-7. Synchronizing in DCM

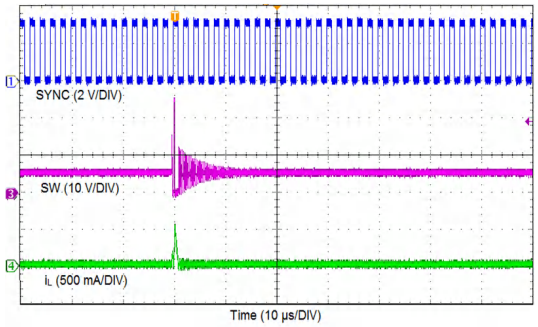


図 8-8. Synchronizing in Sleep Mode

式 6 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max)} = \frac{1}{t_{ON}} \times \left(\frac{I_{OUT} \times R_{IND} + V_{OUT} + V_D}{V_{IN\_MAX} - I_{OUT} \times R_{DS\_ON} + V_D} \right) \quad (6)$$

where

- I_{OUT} = Output current
- R_{IND} = Inductor series resistance
- V_{IN_MAX} = Maximum input voltage
- V_{OUT} = Output voltage
- V_D = Diode voltage drop
- R_{DS_ON} = High-side MOSFET switch on resistance
- t_{ON} = Minimum on-time

8.3.9 Power Good (PGOOD)

The LV14360P has a built-in power-good flag shown on the PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate DC voltage. Voltage seen by the PGOOD pin must never exceed 7 V. A resistor divider pair can be used to divide the voltage down from a higher potential. A typical range of pullup resistor value is 10 kΩ to 100 kΩ.

Refer to 図 8-9. When the FB voltage is within the power-good band, +7% above and –6% below the internal reference V_{REF} typically, the PGOOD switch is turned off, and the PGOOD voltage is pulled up to the voltage level defined by the pullup resistor or divider. When the FB voltage is outside of the tolerance band, +9% above or –8% below V_{REF} typically, the PGOOD switch is turned on, and the PGOOD pin voltage is pulled low to indicate power bad.

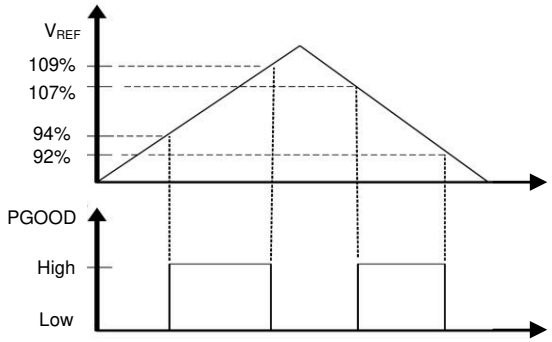


図 8-9. Power-Good Flag

8.3.10 Overcurrent and Short-Circuit Protection

The LV14360 is protected from overcurrent condition by cycle-by-cycle current limiting on the peak current of the high-side MOSFET. High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. See *セクション 8.2* for more details. The peak current of the high-side switch is limited by a clamped maximum peak current threshold which is constant. Thus, the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The LV14360 also implements a frequency foldback to protect the converter in severe overcurrent or short conditions. The oscillator frequency is divided by two, four, and eight as the FB pin voltage decrease to 75%, 50%, 25% of V_{REF}. The frequency foldback increases the off-time by increasing the period of the switching cycle, so that it provides more time for the inductor current to ramp down and leads to a lower average inductor current.

Lower frequency also means lower switching loss. Frequency foldback reduces power dissipation and prevents overheating and potential damage to the device.

8.3.11 Overvoltage Protection

The LV14360 employs an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. The OVP feature minimizes output overshoot by turning off the high-side switch immediately when FB voltage reaches to the rising OVP threshold, which is nominally 109% of the internal voltage reference V_{REF}. When the FB voltage drops below the falling OVP threshold which is nominally 107% of V_{REF}, the high-side MOSFET resumes normal operation.

8.3.12 Thermal Shutdown

The LV14360 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The high-side MOSFET stops switching when thermal shutdown activates. Once the die temperature falls below 158°C (typical), the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LV14360. When V_{EN} is below 1 V, the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 1 µA, typically. The LV14360 also employs UVLO protection. If V_{IN} voltage is below the UVLO level, the regulator is turned off.

8.4.2 Active Mode

The LV14360 is in active mode when V_{EN} is above the precision enable threshold and V_{IN} is above its UVLO level. The simplest way to enable the LV14360 is to connect the EN pin to VIN pin. This allows self start-up when the input voltage is in the operation range: 4.3 V to 60 V. See *セクション 8.3.6* for details on setting these operating levels.

In active mode, depending on the load current, the LV14360 is in one of three modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation
3. Sleep-mode when internal COMP voltage drop to 400 mV at very light load

8.4.3 CCM Mode

CCM operation is employed in the LV14360 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple will be at a minimum in this mode and the maximum output current of 3 A can be supplied by the LV14360.

8.4.4 Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the LV14360 operates in DCM. At even lighter current loads, sleep mode is activated to maintain high efficiency operation by reducing switching and gate-drive losses.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The LV14360 is a step-down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LV14360. This section presents a simplified discussion of the design process.

9.2 Typical Application

The LV14360 only requires a few external components to convert from wide voltage range supply to a fixed output voltage. A schematic of 5-V / 3-A application circuit is shown in 図 9-1. The external components have to fulfill the needs of the application, but also the stability criteria of the device control loop.

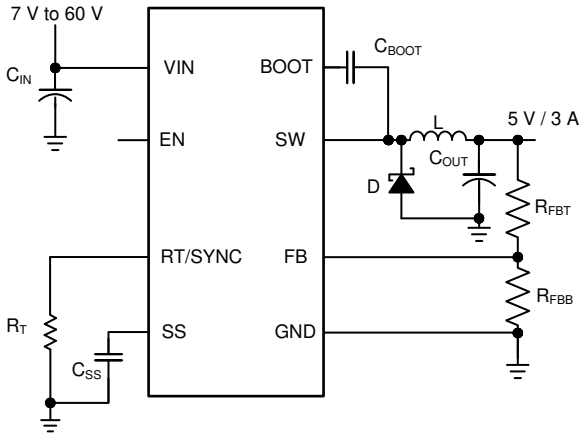


図 9-1. Application Circuit, 5-V Output

9.2.1 Design Requirements

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_{IN}	7 V to 60 V, typical 24 V
Output voltage, V_{OUT}	5 V
Maximum output current I_{O_MAX}	3 A
Transient response 0.3 A to 3 A	5%
Output voltage ripple	50 mV
Input voltage ripple	400 mV
Switching frequency f_{SW}	500 KHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Set-Point

The output voltage of LV14360 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. 式 7 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} \times R_{FBB} \tag{7}$$

Choose the value of R_{FBT} to be 100 kΩ. With the desired output voltage set to 5 V and the V_{FB} = 0.75 V, the R_{FBB} value can then be calculated using 式 7. The formula yields to a value 17.65 kΩ. Choose the closest available value of 17.8 kΩ for R_{FBB}.

9.2.2.2 Switching Frequency

For desired frequency, use 式 8 to calculate the required value for R_T.

$$R_T(k\Omega) = 42904 \times f_{SW}(kHz)^{-1.088} \tag{8}$$

For 500 KHz, the calculated R_T is 49.66 kΩ, and standard value 49.9 kΩ can be used to set the switching frequency at 500 KHz.

9.2.2.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 式 9 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} should be 20% to 40%. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{10}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. It also generates more conduction loss since the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.4. The minimum inductor value is calculated to be 7.64 µH, and a nearest standard value is chosen: 8.2 µH. A standard 8.2-µH ferrite inductor with a capability of 3-A RMS current and 6-A saturation current can be used.

9.2.2.4 Output Capacitor Selection

Choose the output capacitor or capacitors, C_{OUT}, with care since it directly affects the steady state output voltage ripple, loop stability, and the voltage overshoot and undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (11)$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (12)$$

The two components in the voltage ripple are not in-phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for three clock cycles to maintain the output voltage within the specified range. 式 13 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode cannot sink current so the energy stored in the inductor results in an output voltage overshoot. 式 14 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{3 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \quad (13)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L \quad (14)$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot

For this design example, the target output ripple is 50 mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 50 mV, and choose K_{IND} = 0.4. 式 11 yields ESR no larger than 41.7 mΩ and 式 12 yields C_{OUT} no smaller than 6 µF. For the target overshoot and undershoot range of this design, V_{US} = V_{OS} = 5% × V_{OUT} = 250 mV. C_{OUT} can be calculated to be no smaller than 64.8 µF and 6.4 µF by 式 13 and 式 14, respectively. In summary, the most stringent criteria for the output capacitor is 100 µF. For this design example, two 47-µF, 16-V, X7R ceramic capacitors with 5-mΩ ESR are used in parallel.

9.2.2.5 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage, the average diode current is lower. In this case, it is possible to use a diode with a lower average current rating, approximately (1 – D) × I_{OUT}, however, the peak current rating should be higher than the maximum load current. A 3-A rated diode is a good starting point.

9.2.2.6 Input Capacitor Selection

The LV14360 device requires high frequency input decoupling capacitor or capacitors and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7 µF to 10 µF. A high-quality ceramic capacitor type X5R or X7R with sufficient voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is

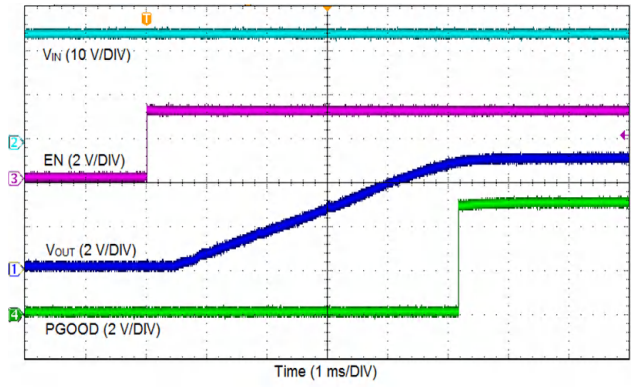
recommended. Additionally, some bulk capacitance can be required, especially if the LV14360 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 2.2-µF, X7R ceramic capacitors rated for 100 V are used. Use a 0.1-µF capacitor for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.7 Bootstrap Capacitor Selection

Every LV14360 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

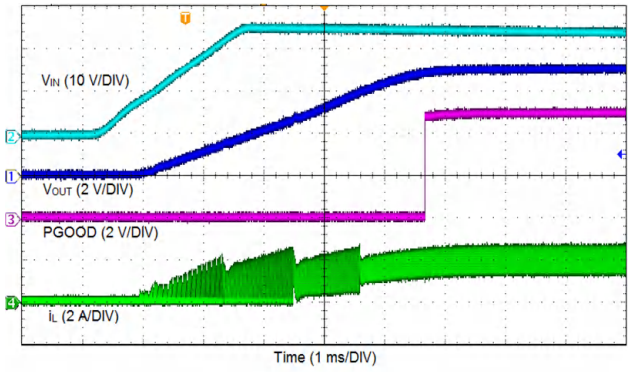
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, f_{SW} = 500 KHz, L = 8.2 µH, C_{OUT} = 2 × 47 µF, T_A = 25°C.



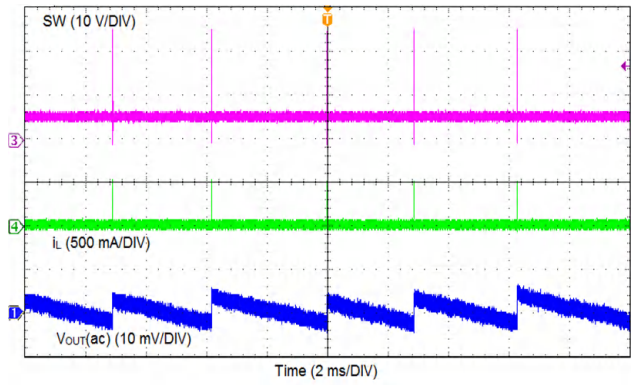
V_{OUT} = 5 V I_{OUT} = 2 A

図 9-2. Start-up by EN



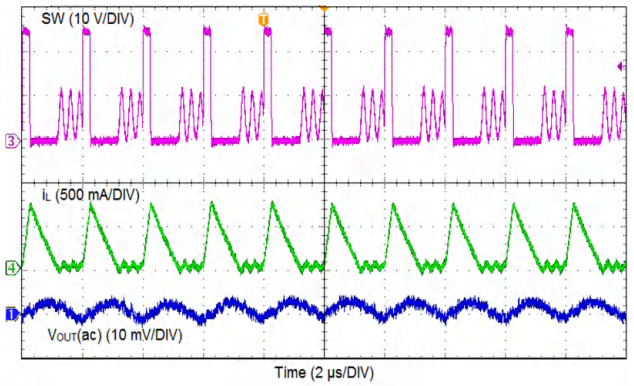
V_{OUT} = 5 V I_{OUT} = 2 A

図 9-3. Start-up By V_{IN}



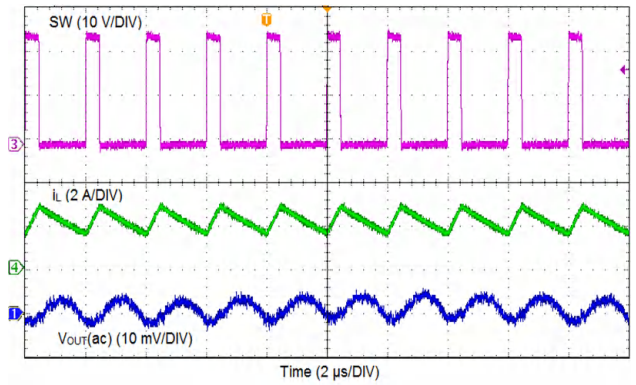
V_{OUT} = 5 V I_{OUT} = 0 A

図 9-4. Sleep Mode



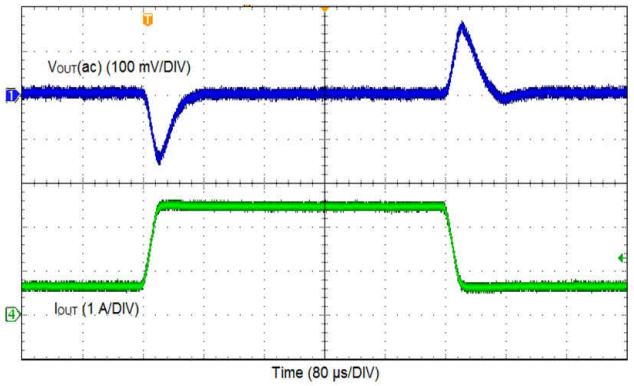
V_{OUT} = 5 V I_{OUT} = 200 mA

図 9-5. DCM Mode



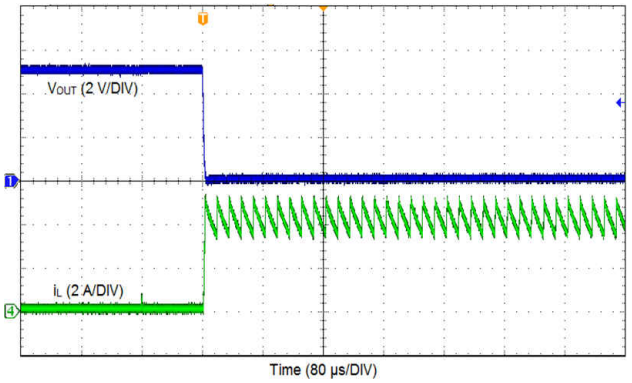
V_{OUT} = 5 V I_{OUT} = 2 A

図 9-6. CCM Mode



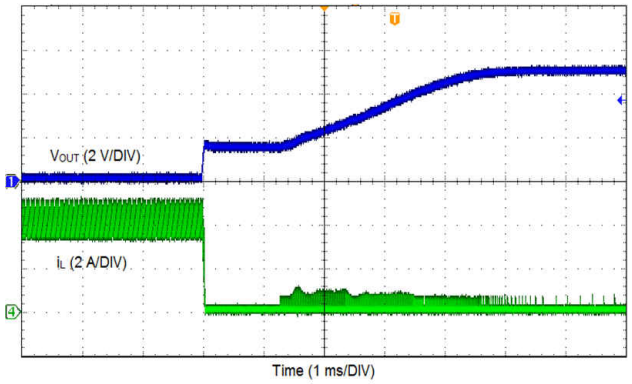
I_{OUT}: 20% → 80% of 3 A Slew rate = 100 mA/µs

図 9-7. Load Transient



V_{OUT} = 5 V

図 9-8. Output Short



V_{OUT} = 5 V

図 9-9. Output Short Recovery

10 Power Supply Recommendations

The LV14360 is designed to operate from an input voltage supply range between 4.3 V and 60 V. This input supply should be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LV14360 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV14360, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R_{FBT} and R_{FBB}, should be kept close to the FB pin. V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
2. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD.
3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. Place the output capacitor, C_{OUT} close to the junction of L and the diode D. Keep the L, D, and C_{OUT} trace as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, C_{IN}, and C_{OUT} should be as small as possible and tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations see *AN-1149 Layout Guidelines for Switching Power Supplies*.

11.2 Layout Example

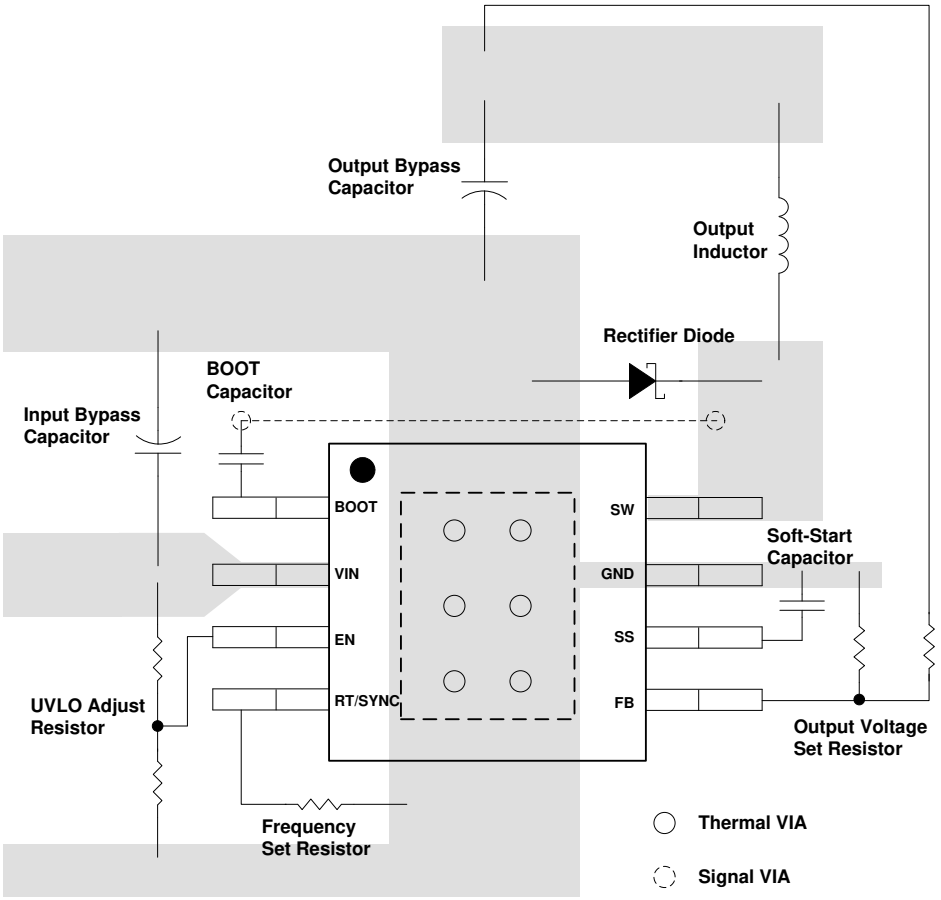


図 11-1. Layout

12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.3 Trademarks

PowerPAD™ is a trademark of TI.
TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.4 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LV14360PDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	14360P	Samples
LV14360SDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	14360S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

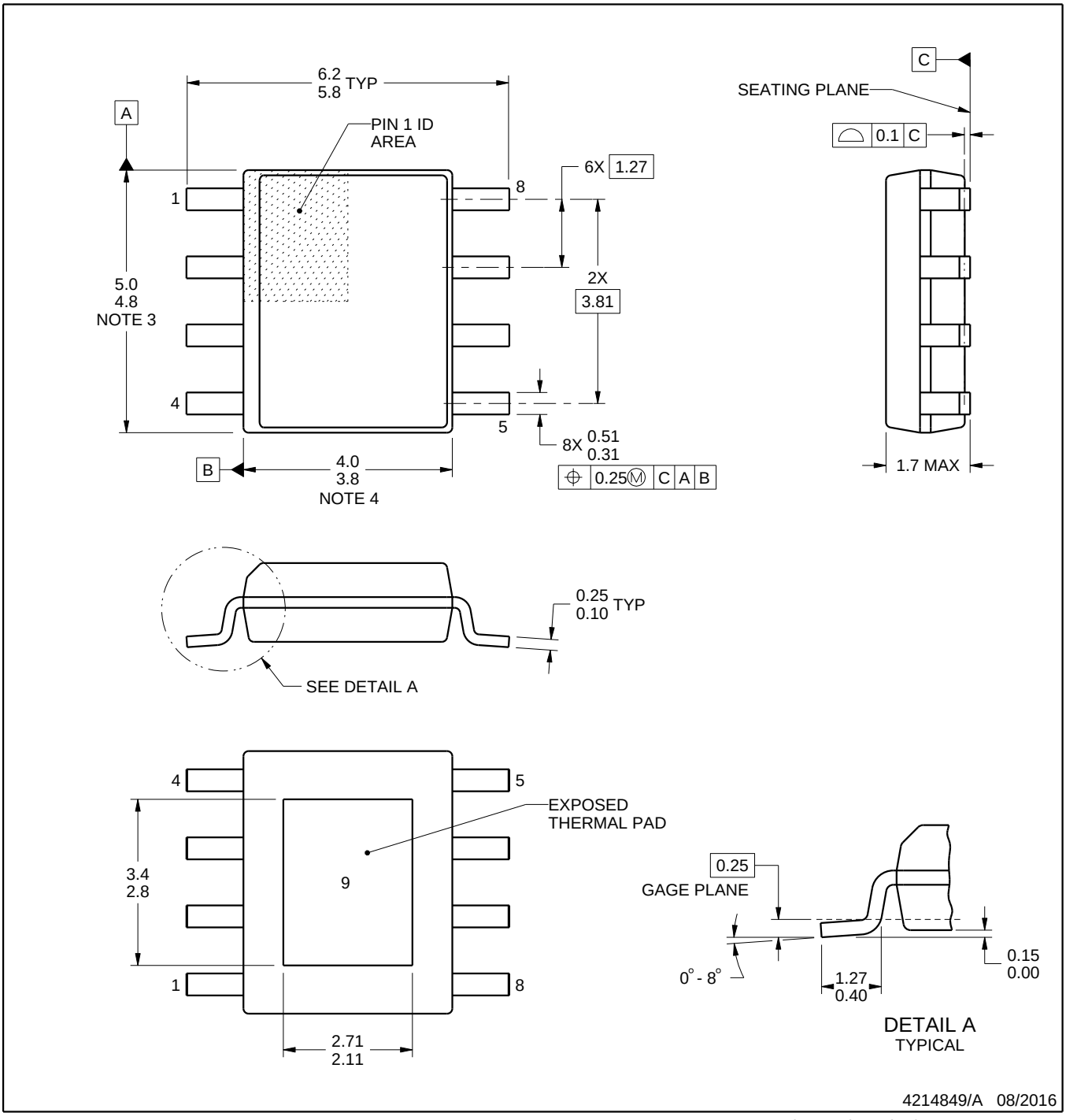
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

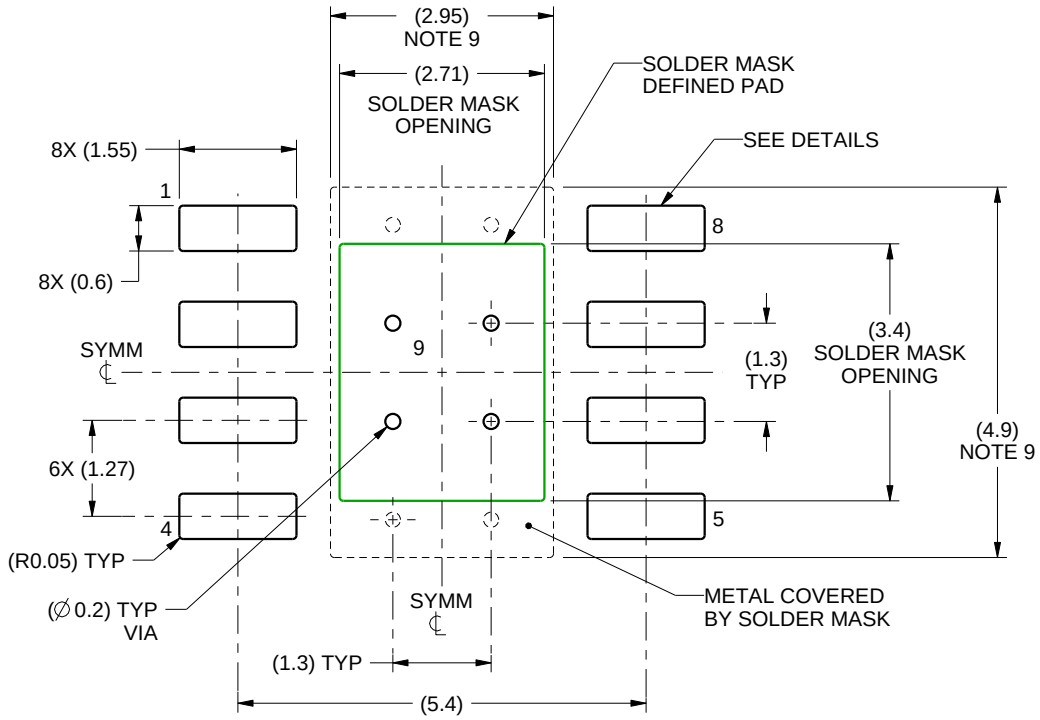
PLASTIC SMALL OUTLINE



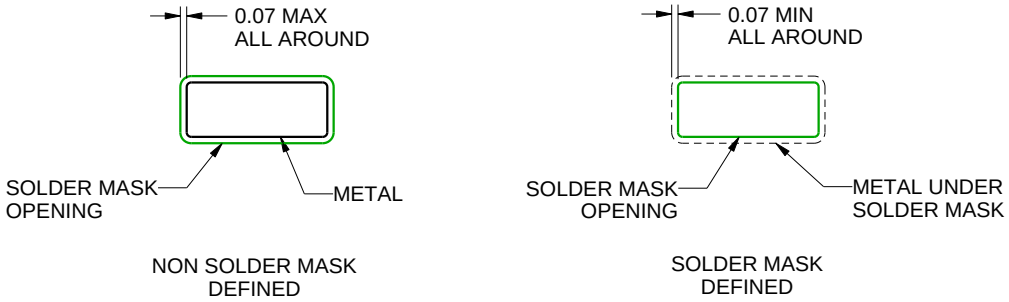
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

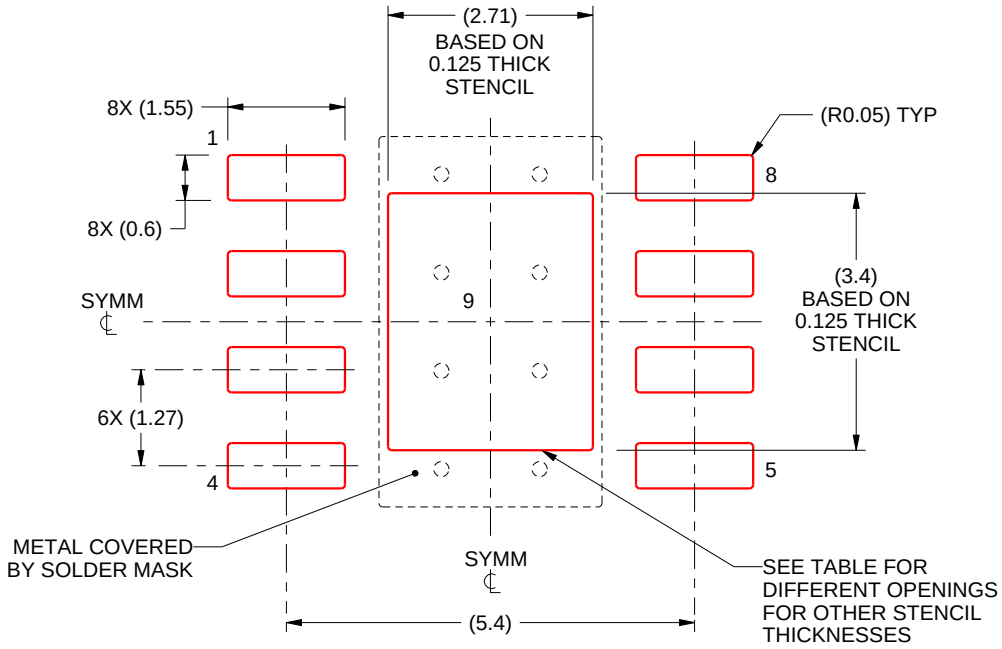
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

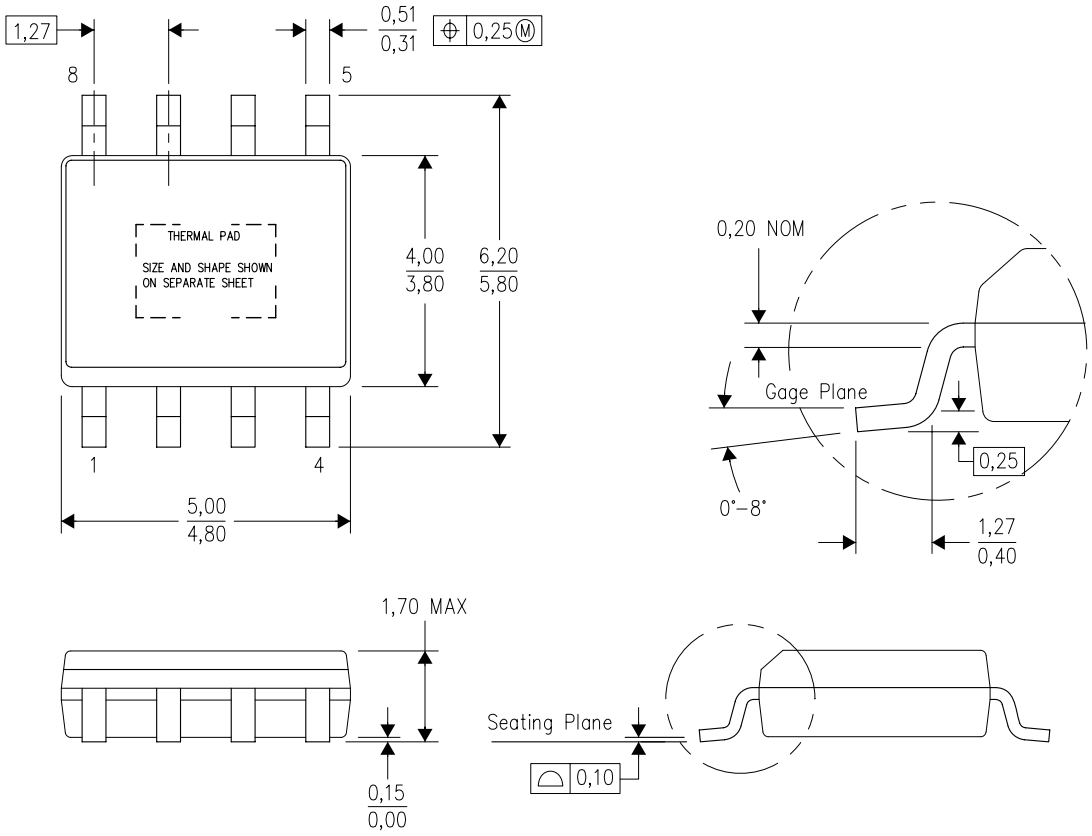
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

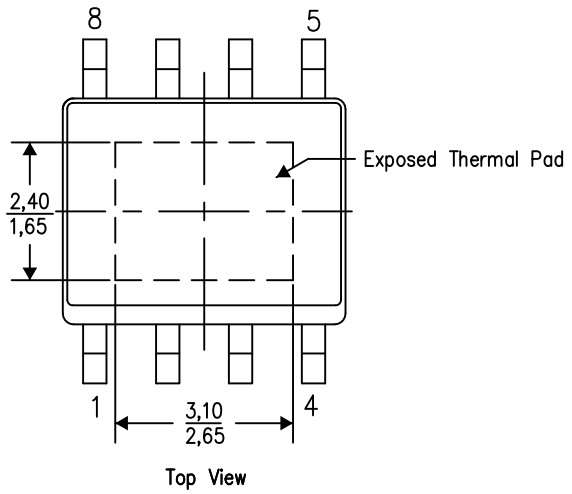
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



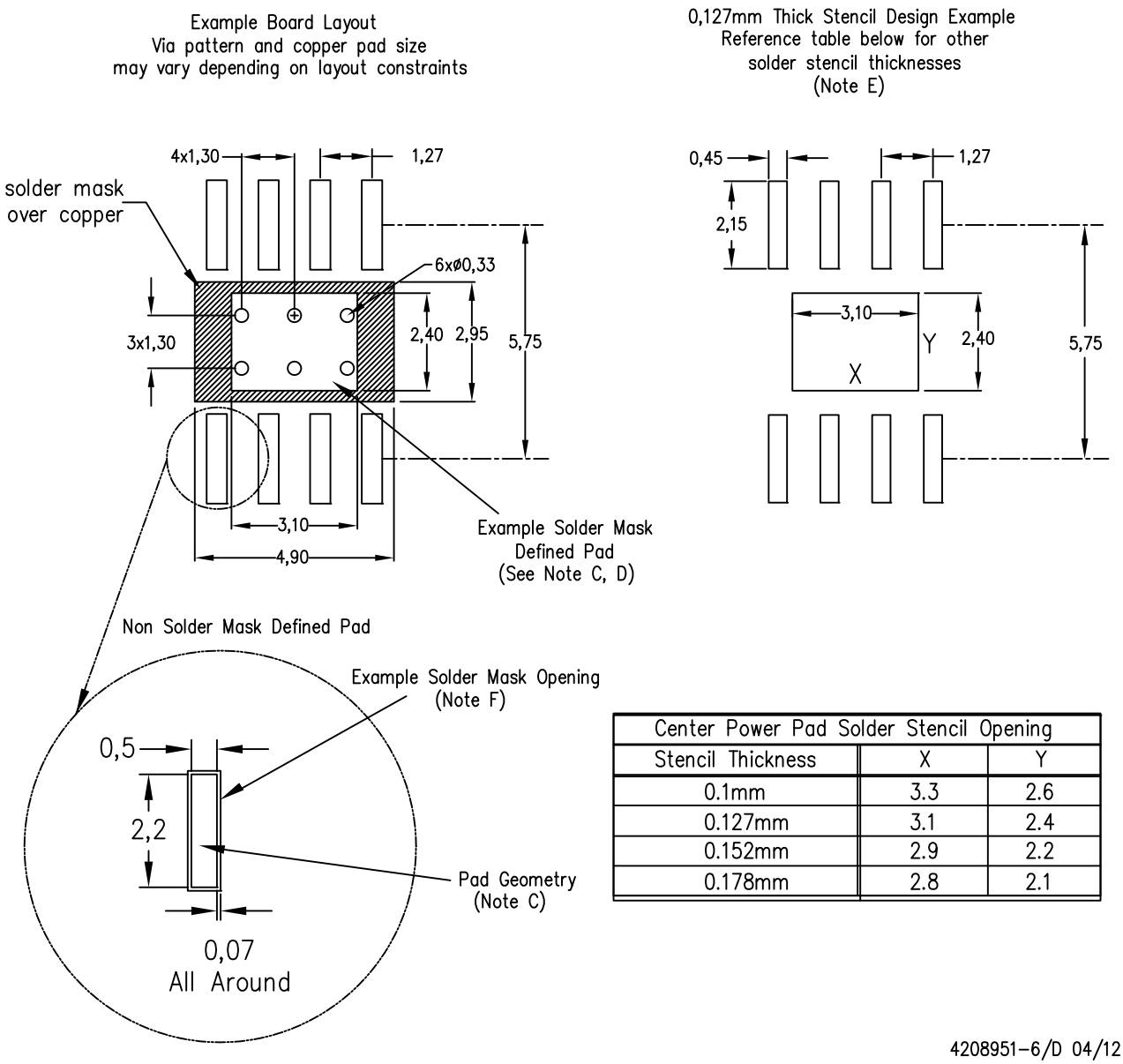
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265