

3V~5.5V、マルチチャネル RS-232 ライン・ドライバおよびレシーバ、 ±15kV ESD 保護

1 特長

- RS-232 バス・ピン用 ESD 保護機能
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC 61000-4-2、接触放電
 - ±15kV IEC 61000-4-2、エアギャップ放電
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V~5.5V の V_{CC} 電源で動作
- 最大 500kbit/s で動作
- 2つのドライバと2つのレシーバ
- 小さいスタンバイ電流 ...1 μ A 標準
- 外付けコンデンサ ...4 × 0.1 μ F
- 3.3V 電源で 5V ロジック入力を受容
- SNx5C3222E 代替の高速ピン互換デバイス (1Mbit/s)

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびネットワーク機器
- ノート PC
- ハンドヘルド機器

3 概要

MAX3222E は 2 つのライン・ドライバ、2 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。

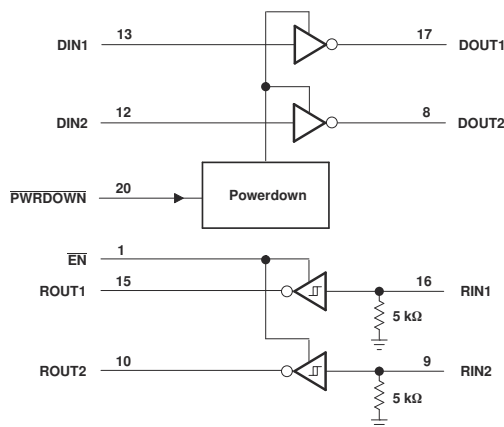
このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。このデバイスは最大 500kbit/s のデータ信号速度、最大 30V/ μ s のドライバ出力スlewレートで動作します。

MAX3222E は、パワーダウン (PWRDOWN) 入力を Low に設定してパワーダウン・モードにすることができます。この状態では電源からわずか 1 μ A しか流れ込みません。デバイスがパワーダウン・モードのとき、ドライバはハイ・インピーダンス状態になりますが、レシーバはアクティブのままです。また、パワーダウン・モード時には、オンボードのチャージ・ポンプがディセーブルになり、 $V+$ が V_{CC} に低下し、 $V-$ が GND に向かって上昇します。レシーバの出力は、イネーブル (\overline{EN}) を HIGH に設定することで、高インピーダンス状態に移行することもできます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
MAX3222E	DB (SSOP) (20)	10.2mm × 5.30mm
	DW (SOIC) (20)	15.4mm × 7.50mm
	PW (TSSOP) (20)	7.80mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ピン番号は、DB、DW、PW パッケージのものであります。

論理図 (正論理)



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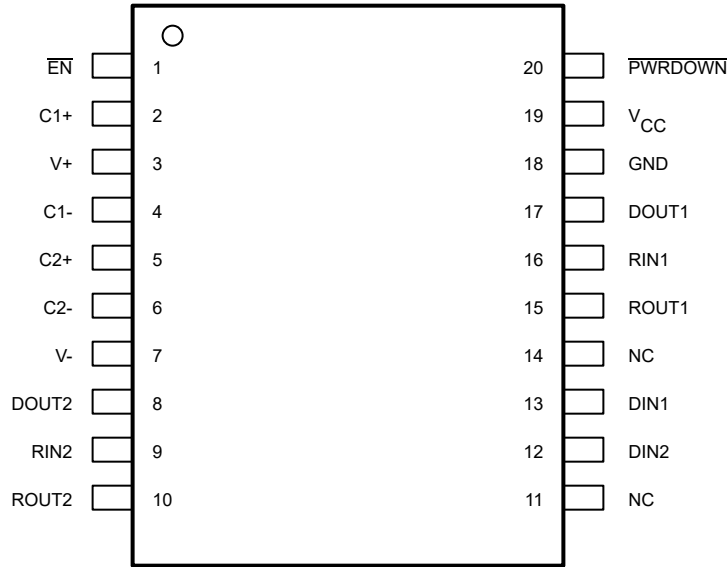
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2021) to Revision C (January 2023)	Page
• Changed the <i>ESD Ratings - IEC Specifications</i> table note to include the DB package.....	4
• Changed the values of $R_{\theta JA}$ in the <i>Thermal Information</i> table for the DB package.....	5

Changes from Revision A (September 2009) to Revision B (August 2021)	Page
• 「アプリケーション」の一覧を更新.....	1
• 「注文情報」表を削除.....	1
• 「製品情報」表、「ピン構成および機能」、「詳細説明」セクション、「アプリケーションと実装」セクションを追加.....	1
• Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i>	4
• Changed the <i>ESD Ratings</i> table.....	4
• Added the <i>ESD Ratings - IEC Specifications</i> table.....	4
• Added the <i>Thermal Information</i> table.....	5
• Changed the value of $R_{\theta JA}$ for PW package (previously in the <i>Absolute Maximum Ratings</i> table), and added additional thermal parameters for all packages in the <i>Thermal Information</i> table.....	5

5 Pin Configuration and Functions



Not to scale

图 5-1. DB, DW, or PW Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	2	—	Charge pump capacitor pin
C1-	4	—	Charge pump capacitor pin
C2+	5	—	Charge pump capacitor pin
C2-	6	—	Charge pump capacitor pin
DIN1	13	I	Driver logic input
DIN2	12	I	Driver logic input
DOUT1	17	O	RS-232 driver output
DOUT2	8	O	RS-232 driver output
EN	1	I	Receiver enable, active low
GND	18	—	Ground
NC	11,14	—	No internal connection
PWRDOWN	20	I	Driver disable, active low
RIN1	16	I	RS-232 receiver input
RIN2	9	I	RS-232 receiver input
ROUT1	15	O	Receiver logic output
ROUT2	10	O	Receiver logic output
V _{CC}	19	—	Power Supply
V+	3	—	Charge pump capacitor pin
V-	7	—	Charge pump capacitor pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	-0.3	6	V	
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V	
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V	
V+ – V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage range	Driver ($\overline{\text{EN}}$, PWRDOWN)	-0.3	6	V
		Receiver	-25	25	
V _O	Output voltage range	Driver	-13.2	13.2	V
		Receiver	-0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

ESD Ratings

			TYP	UNIT
V _(ESD)	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		RIN1, RIN2, DOUT1 and DOUT2 pins to GND	±15,000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	
		All pins except RIN1, RIN2, DOUT1 and DOUT2 pins		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

ESD Ratings - IEC Specifications

			TYP	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2, Contact Discharge ⁽¹⁾	±8,000	V
		IEC 61000-4-2, Air-Gap Discharge ⁽¹⁾	±15,000	
		RIN1, RIN2, DOUT1, DOUT2 pins		

- (1) For PW and DB packages only, a minimum of 1- μ F capacitor is required between V_{CC} and GND to meet the specified IEC 61000-4-2 rating.

6.2 Recommended Operating Conditions

See [9-1](#) and ⁽¹⁾

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, \overline{EN} , PWRDOWN	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, \overline{EN} , PWRDOWN			0.8	V
V_I	Driver and control input voltage	DIN, \overline{EN} , PWRDOWN	0		5.5	V
V_I	Receiver input voltage		-25		25	V
T_A	Operating free-air temperature	MAX3222EC	0		70	°C
		MAX3222EI	-40		85	

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		MAX3222E			UNIT
		DB (SSOP)	DW (SOIC)	PW (TSSOP)	
		20 Pins	20 Pins	20 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.0	58.0	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.2	30.0	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	29.6	45.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.3	7.7	3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.6	29.3	45.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.4 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current (\overline{EN} , PWRDOWN)			±0.01	±1	μA
I_{CC}	Supply current	No load, PWRDOWN at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, PWRDOWN at GND		1	10	μA

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = GND		5	5.4		V
V _{OL}	Low-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = V _{CC}		–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}			±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND			±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V	V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V					
r _o	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V		300	10M		Ω
I _{OZ}	Output leakage current	PWRDOWN = GND	V _{CC} = 3 V to 3.6 V, V _O = ±12 V			±25	μA
			V _{CC} = 4.5 V to 5.5 V, V _O = ±10 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.6 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽³⁾		MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate		C _L = 1000 pF, One DOUT switching,	R _L = 3 kΩ, See 7-1	250	500		kbit/s
t _{sk(p)}	Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF, See 7-2	R _L = 3 kΩ to 7 kΩ,		300		ns
SR(tr)	Slew rate, transition region (see 7-1)	R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V	C _L = 150 pF to 1000 pF	6		30	V/μs
			C _L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I _{OZ}	Output leakage current	EN = 1		±0.05	±10	µA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.8 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

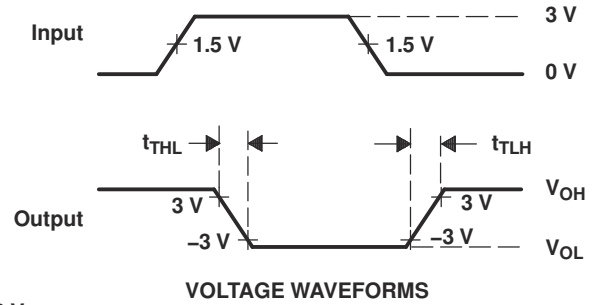
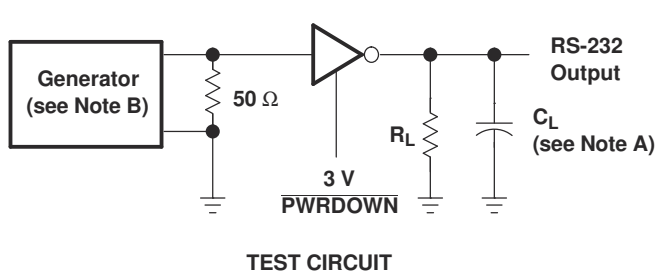
PARAMETER		TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See 7-3	300	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See 7-3	300	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4	200	ns
t _{sk(p)}	Pulse skew ⁽²⁾	See 7-3	300	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

(3) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

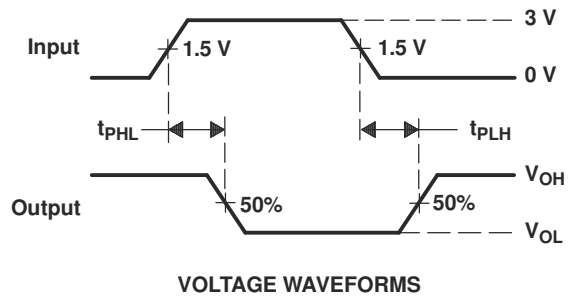
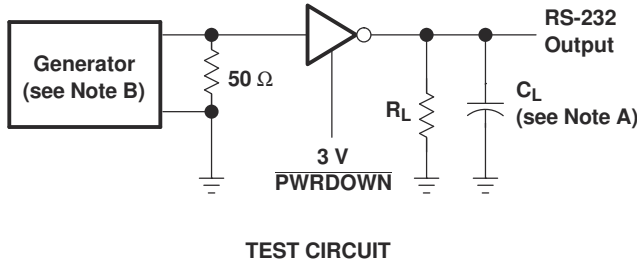
7 Parameter Measurement Information



$$SR(tr) = \frac{6 V}{t_{THL} \text{ or } t_{TLH}}$$

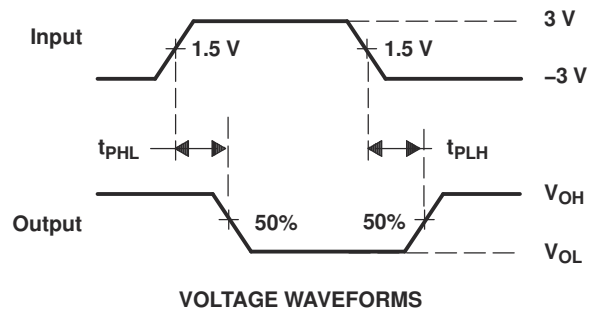
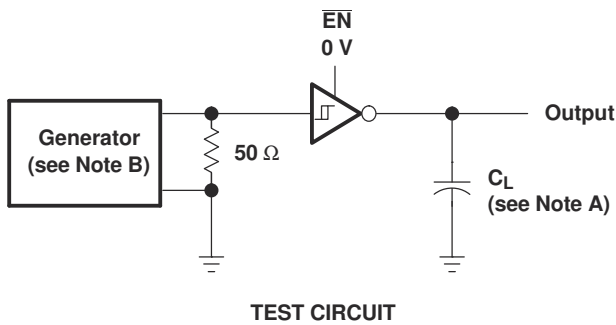
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-1. Driver Slew Rate



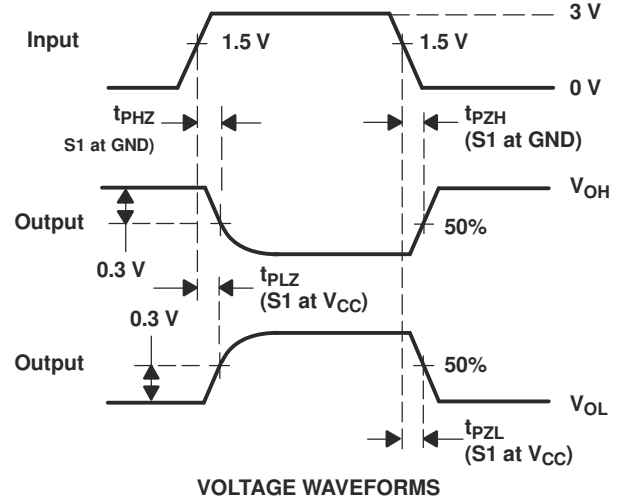
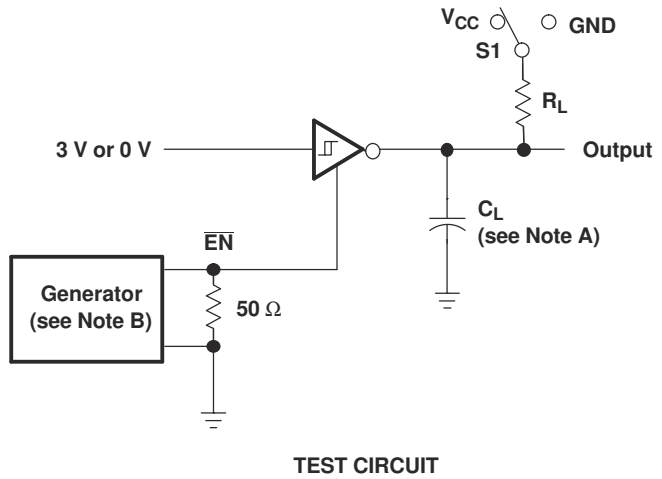
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-2. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-3. Receiver Propagation Delay Times

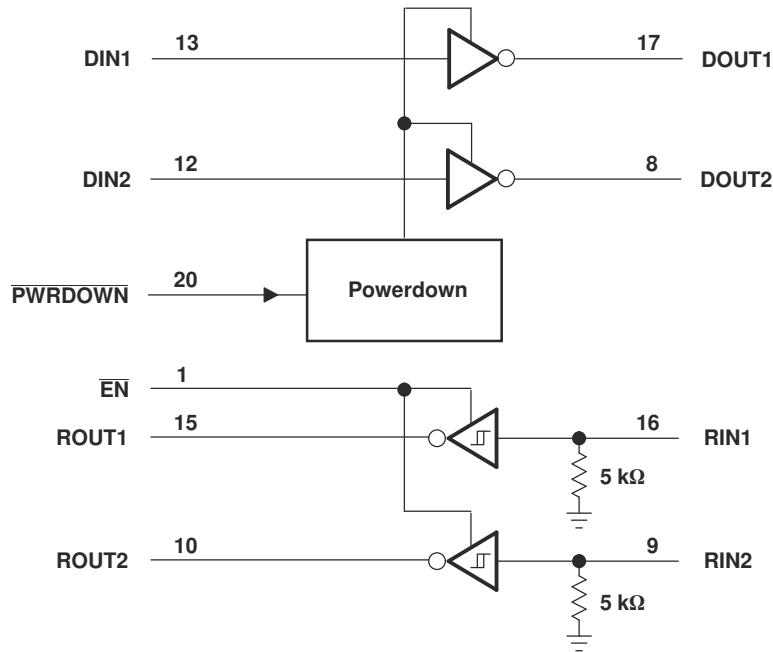


- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-4. Receiver Enable and Disable Times

8 Detailed Description

8.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

图 8-1. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

表 8-1. Function Table: Each Driver

INPUTS ⁽¹⁾		OUTPUT DOUT
DIN	PWRDOWN	
X	L	Z
L	H	H
H	H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Function Table: Each Receiver

INPUTS ⁽¹⁾		OUTPUT ROUT
RIN	EN	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

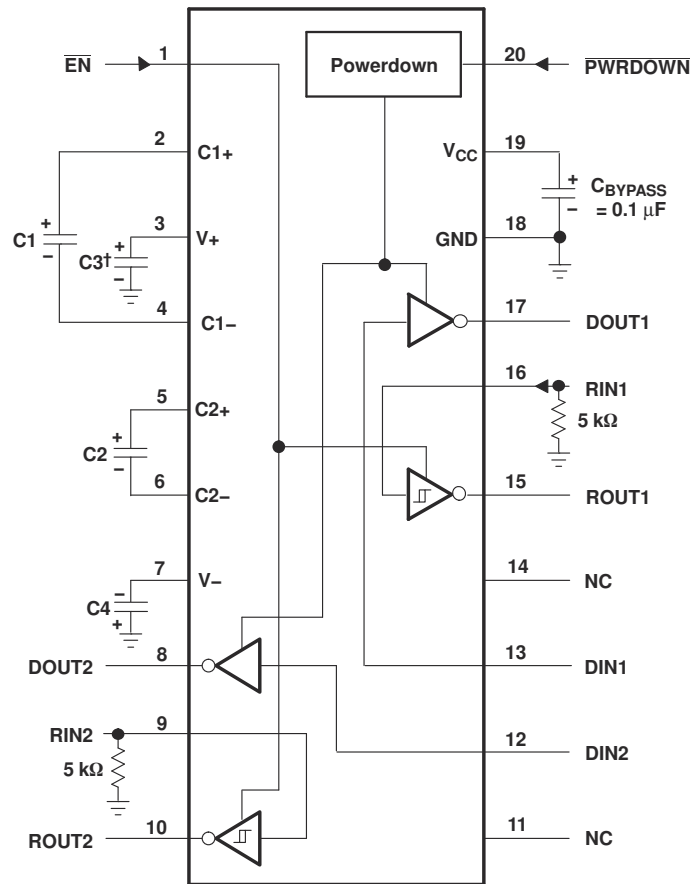
9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.2 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

图 9-1. Typical Operating Circuit and Capacitor Values

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

10.3 商標

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3222ECDB	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70	MP222EC	
MAX3222ECDBR	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70	MP222EC	
MAX3222ECDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	MAX3222EC	
MAX3222ECDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222EC	Samples
MAX3222ECPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP222EC	Samples
MAX3222EIDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI	Samples
MAX3222EIDGSR	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	222EI	Samples
MAX3222EIDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	MAX3222EI	
MAX3222EIDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222EI	Samples
MAX3222EIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP222EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3222ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3222ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
MAX3222EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3222EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3222EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3222ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222ECPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MAX3222ECPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MAX3222EIDBR	SSOP	DB	20	2000	356.0	356.0	35.0
MAX3222EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222EIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

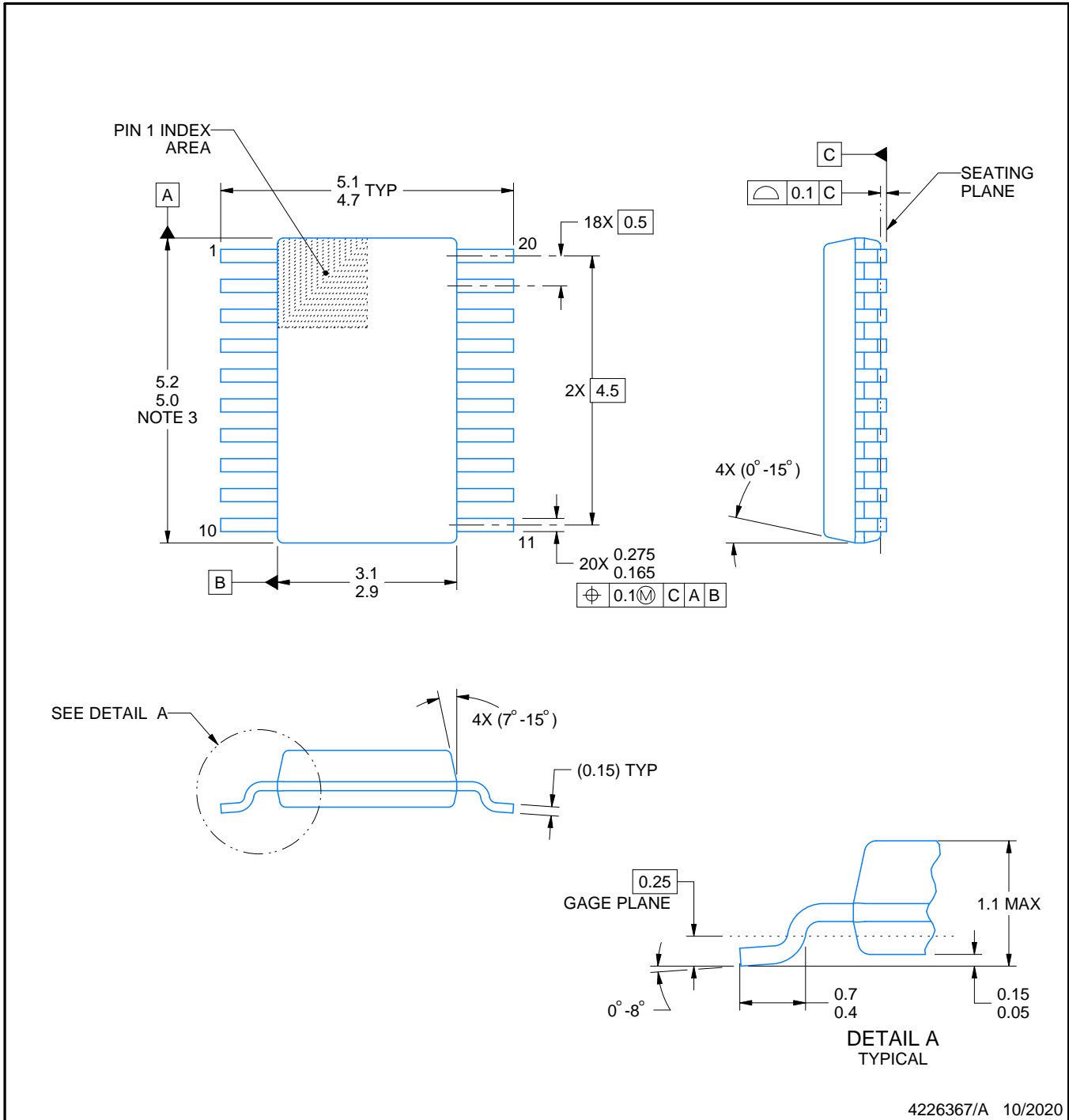
DGS0020A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

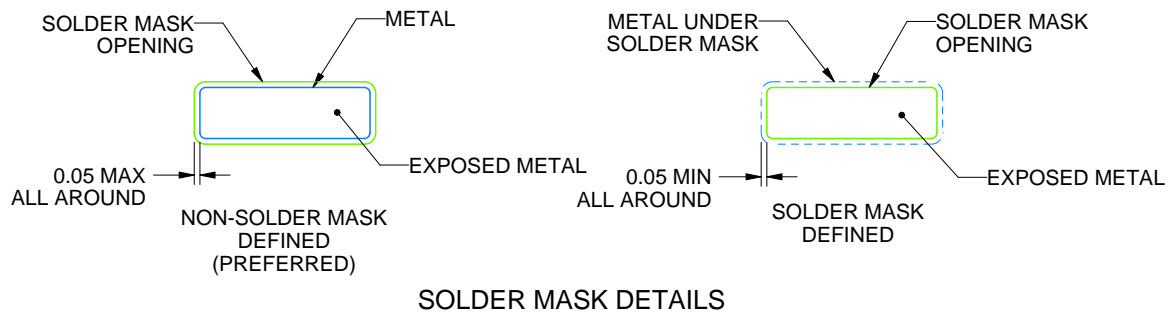
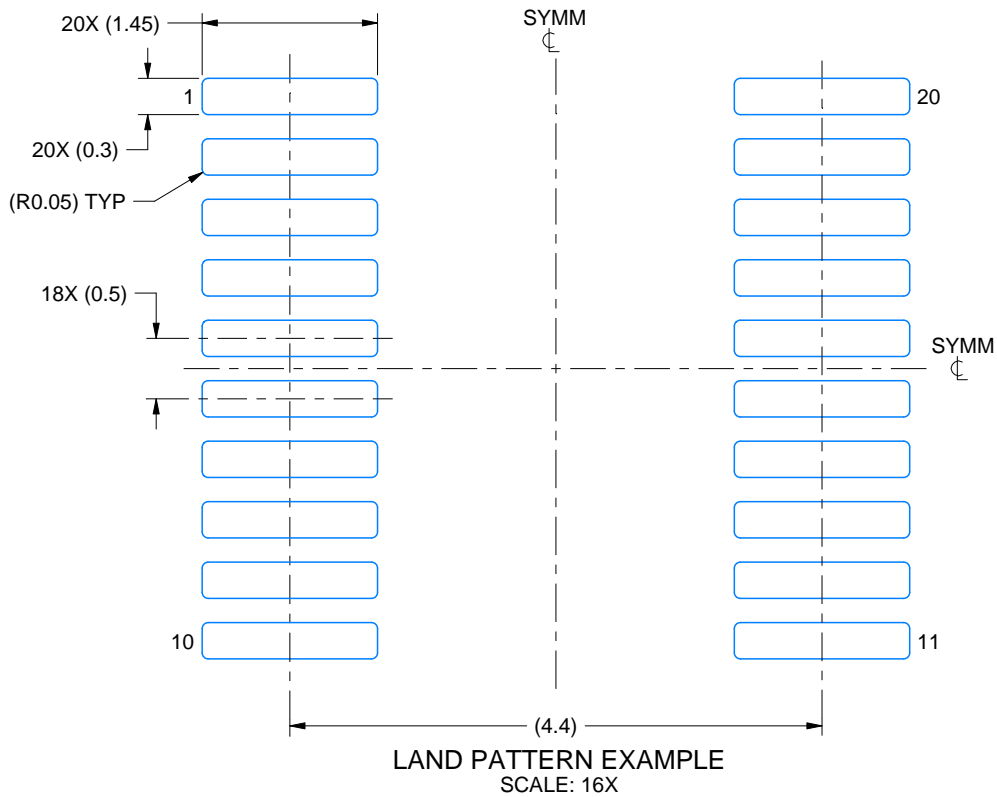
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

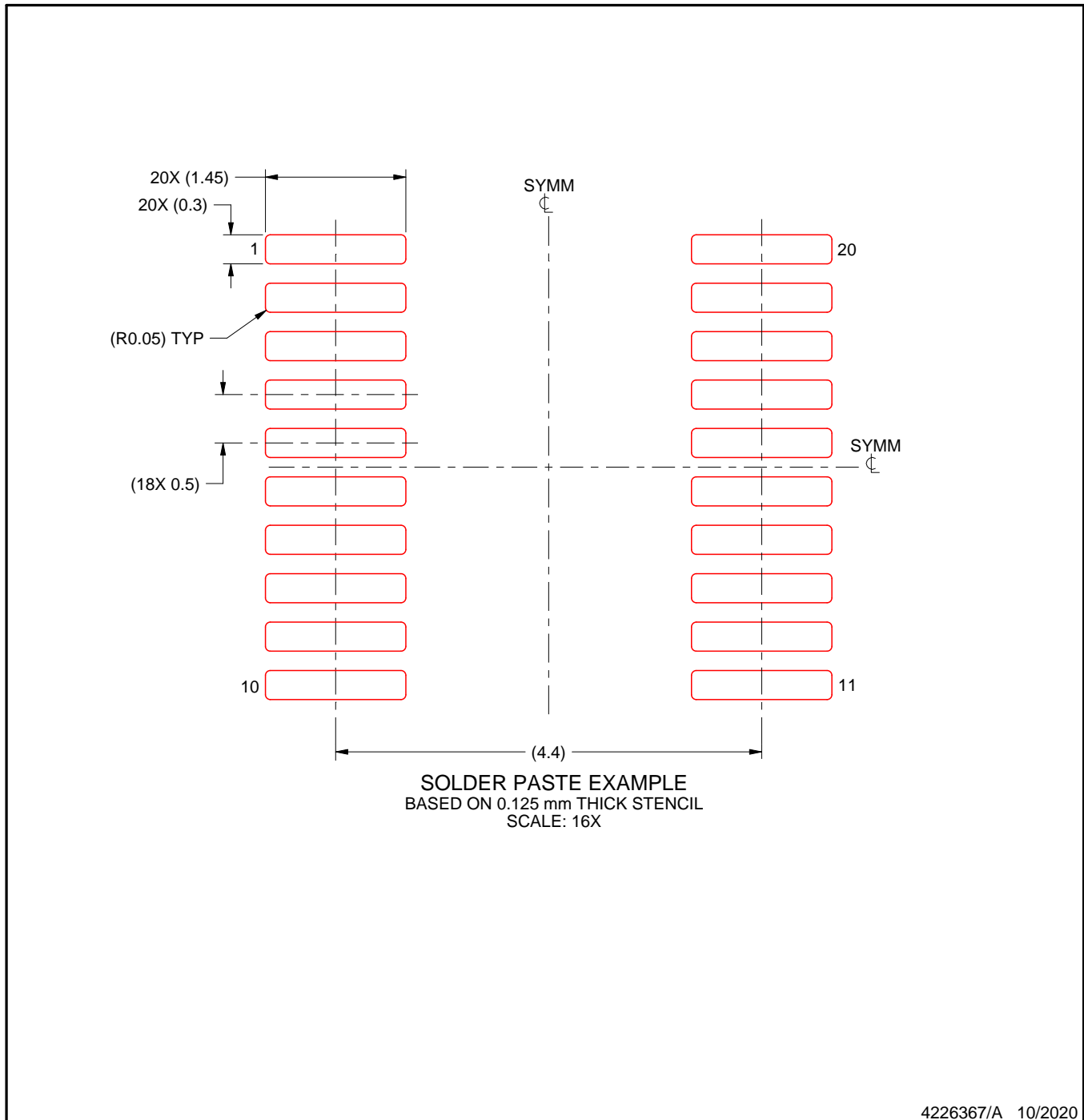
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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