

# MC3486 3 ステート出力搭載クワッド差動ライン・レシーバ

## 1 特長

- ANSI 規格 EIA/TIA-422-B および EIA/TIA-423-B と ITU 勧告 V.10 および V.11 の要件を満たす、または超える
- 3 ステート、TTL 互換出力
- 高速な遷移時間
- 5V 単一電源で動作
- Motorola™ MC3486 と交換可能なように設計

## 2 アプリケーション

- モータ・ドライブ
- ファクトリ・オートメーション / 制御

## 3 概要

MC3486 は、ANSI 規格 TIA/EIA-422-B および TIA/EIA-423-B および ITU 勧告 V.10 および V.11 の仕様を満たすように設計された、モノリシック・クワッド差動ライン・レシーバです。MC3486 には、TTL 互換出力を備えた 4 つの独立した差動入力ライン・レシーバがあります。出力は 3 ステート回路を利用して、適切な出力イネーブルが Low ロジック・レベルのとき、すべての出力で高インピーダンス状態を実現します。

MC3486 は、MC3487 クワッド差動ライン・ドライバと組み合わせると、最適な性能を発揮するよう設計されています。16 ピン・パッケージで供給され、5V 単一電源で動作します。

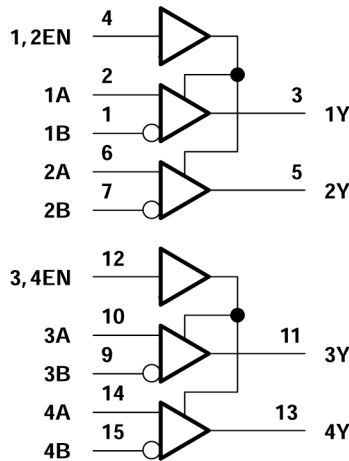
MC3486 は、0°C～70°Cでの動作が規定されています。

### パッケージ情報

| 部品番号   | パッケージ (1)    | パッケージ・サイズ (2)  |
|--------|--------------|----------------|
| MC3486 | D (SOIC, 16) | 19.3 × 9.4mm   |
|        | N (PDIP, 16) | 19.3 × 9.4mm   |
|        | NS (SOP, 16) | 10.2mm × 7.8mm |

(1) 詳細については、[セクション 10](#) を参照してください。

(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



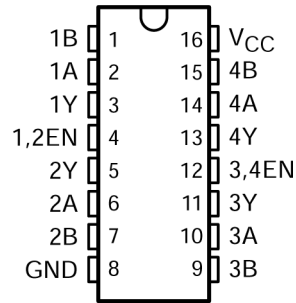
論理図 (正論理)




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## 4 Pin Configuration and Functions




**4-1. D, N, or NS Package  
(Top View)**

**表 4-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-----------------|-----|---------------------|---|
| NAME            | NO. |                     |   |
| 1B              | 1   | I                   | Channel 1 Differential Receiver Inverting Input     |
| 1A              | 2   | I                   | Channel 1 Differential Receiver Non-Inverting Input |
| 1Y              | 3   | O                   | Channel 1 Single Ended Output                       |
| 1,2 EN          | 4   | I                   | Active High Enable for Channels 1 and 2             |
| 2Y              | 5   | O                   | Channel 2 Single Ended Output                       |
| 2A              | 6   | I                   | Channel 2 Differential Receiver Non-Inverting Input |
| 2B              | 7   | I                   | Channel 2 Differential Receiver Inverting Input     |
| GND             | 8   | GND                 | Device GND  |
| 3B              | 9   | I                   | Channel 3 Differential Receiver Inverting Input     |
| 3A              | 10  | I                   | Channel 3 Differential Receiver Non-Inverting Input |
| 3Y              | 11  | O                   | Channel 3 Single Ended Output                       |
| 3,4 EN          | 12  | I                   | Active High Enable for Channels 3 and 4             |
| 4Y              | 13  | O                   | Channel 4 Single Ended Output                       |
| 4A              | 14  | I                   | Channel 4 Differential Receiver Non-Inverting Input |
| 4B              | 15  | I                   | Channel 4 Differential Receiver Inverting Input     |
| V <sub>CC</sub> | 16  | PWR                 | Device VCC (4.75 V to 5.25 V)                       |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                |  | MIN | MAX | UNIT |
|--------------------------------|--|-----|-----|------|
| $V_I$                          | Input voltage (A or B inputs)                                |     | ±15 | V    |
| $V_{ID}$ (see <sup>(2)</sup> ) | Differential input voltage                                   |     | ±25 | V    |
|                                | Enable input voltage   |     | 8   | V    |
| $I_{OL}$                       | Low-level output current                                     |     | 50  | mA   |
|                                | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |     | 260 | °C   |
| $T_{stg}$                      | Storage temperature range                                    | –65 | 150 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

### 5.2 Recommended Operating Conditions

|          |                                 | MIN  | NOM | MAX  | UNIT |
|----------|---------------------------------|------|-----|------|------|
| $V_{CC}$ | Supply voltage                  | 4.75 | 5   | 5.25 | V    |
| $V_{IC}$ | Common-mode input voltage       |      |     | ±7   | V    |
| $V_{ID}$ | Differential input voltage      |      |     | ±6   | V    |
| $V_{IH}$ | High-level enable input voltage | 2    |     |      | V    |
| $V_{IL}$ | Low-level enable input voltage  |      |     | 0.8  | V    |
| $T_A$    | Operating free-air temperature  | 0    |     | 70   | °C   |

### 5.3 Thermal Resistance Characteristics

| THERMAL METRIC <sup>(1)</sup> |  | D (SOIC) | N (PDIP) | NS (SOP) | UNIT |
|-------------------------------|--|----------|----------|----------|------|
|                               |  | 16-PINS  |          |          |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 84.6     | 60.6     | 88.5     | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 43.5     | 48.1     | 46.2     | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 43.2     | 40.6     | 50.7     | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.4     | 27.5     | 13.5     | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 42.8     | 40.3     | 50.3     | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | n/a      | n/a      | n/a      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER |   | TEST CONDITIONS  |                          |                      | MIN | MAX                 | UNIT          |    |
|-----------|---|--|--------------------------|----------------------|-----|---------------------|---------------|----|
| $V_{IT+}$ | Differential input high-threshold voltage | $V_O = 2.7\text{ V}$ ,   | $I_O = -0.4\text{ mA}$   |                      |     | 0.2                 | V             |    |
| $V_{IT-}$ | Differential input low-threshold voltage  | $V_O = 0.5\text{ V}$ ,   | $I_O = -8\text{ mA}$     |                      |     | -0.2 <sup>(1)</sup> | V             |    |
| $V_{IK}$  | Enable-input clamp voltage                | $I_I = -10\text{ mA}$  |                          |                      |     | -1.5                | V             |    |
| $V_{OH}$  | High-level output voltage                 | $V_{ID} = 0.4\text{ V}$ , See Note 4 and <a href="#">6-1</a>   | $I_O = -0.4\text{ mA}$ , |                      |     | 2.7                 | V             |    |
| $V_{OL}$  | Low-level output voltage                  | $V_{ID} = -0.4\text{ V}$ , See Note 4 and <a href="#">6-1</a>  | $I_O = 8\text{ mA}$ ,    |                      |     | 0.5                 | V             |    |
| $I_{OZ}$  | High-impedance-state output current       | $V_{IL} = 0.8\text{ V}$ ,                                      | $V_{ID} = -3\text{ V}$ , | $V_O = 2.7\text{ V}$ |     | 40                  | $\mu\text{A}$ |    |
|           |   | $V_{IL} = 0.8\text{ V}$ ,                                      | $V_{ID} = 3\text{ V}$ ,  | $V_O = 0.5\text{ V}$ |     | -40                 |               |    |
| $I_{IB}$  | Differential-input bias current           | $V_{CC} = 0\text{ V}$ or $2.25\text{ V}$ , Other inputs at 0 V |                          | $V_I = -10\text{ V}$ |     | -3.25               | mA            |    |
|           |   |  |                          | $V_I = -3\text{ V}$  |     | -1.5                |               |    |
|           |   |  |                          | $V_I = 3\text{ V}$   |     | 1.5                 |               |    |
|           |   |  |                          | $V_I = 10\text{ V}$  |     | 3.25                |               |    |
| $I_{IH}$  | High-level enable input current           | $V_I = 2.25\text{ V}$  |                          |                      |     | 100                 | $\mu\text{A}$ |    |
|           |   | $V_I = 2.7\text{ V}$   |                          |                      |     | 20                  |               |    |
| $I_{IL}$  | Low-level enable input current            | $V_I = -0.5\text{ V}$  |                          |                      |     | -100                | $\mu\text{A}$ |    |
| $I_{OS}$  | Short-circuit output current              | $V_{ID} = 3\text{ V}$ ,  | $V_O = 0$ ,              | See Note 5           |     | -15                 | -100          | mA |
| $I_{CC}$  | Supply current                            | $V_{IL} = 0$   |                          |                      |     | 85                  | mA            |    |

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
- (2) Refer to ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.
- (3) Only one output should be shorted at a time.

## 5.5 Switching Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST CONDITIONS         | MIN | TYP | MAX | UNIT |
|-----------|---|-------------------------|-----|-----|-----|------|
| $t_{PHL}$ | Propagation delay time, high- to low-level output | See <a href="#">6-2</a> |     | 28  | 35  | ns   |
| $t_{PLH}$ | Propagation delay time, low- to high-level output |                         |     | 27  | 30  | ns   |
| $t_{PZH}$ | Output enable time to high level                  | See <a href="#">6-3</a> |     | 13  | 30  | ns   |
| $t_{PZL}$ | Output enable time to low level                   |                         |     | 20  | 30  | ns   |
| $t_{PHZ}$ | Output disable time from high level               |                         |     | 26  | 35  | ns   |
| $t_{PLZ}$ | Output disable time from low level                |                         |     | 27  | 35  | ns   |

## 6 Parameter Measurement Information

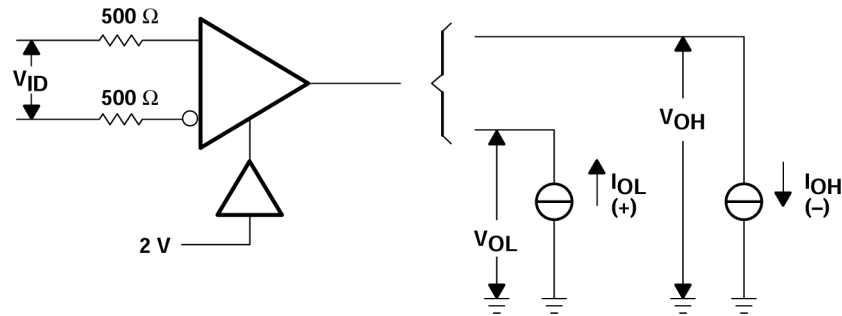
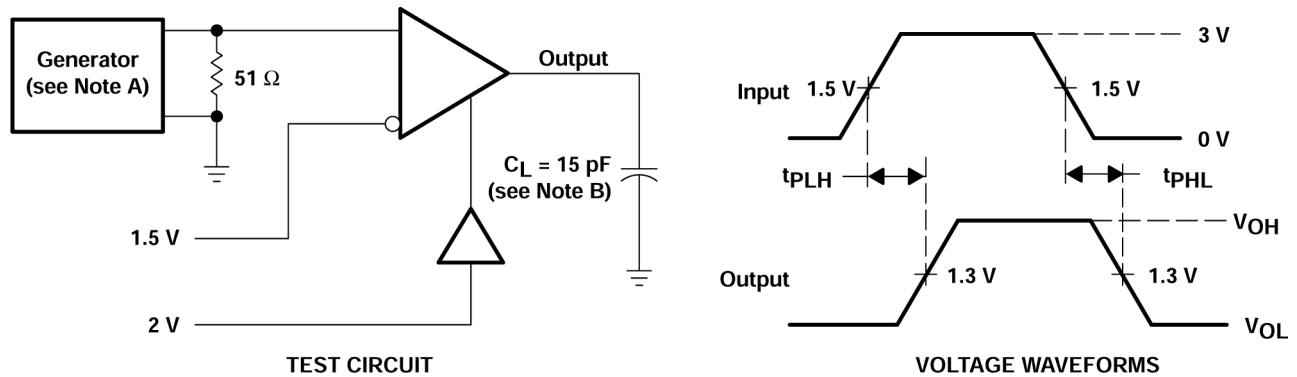
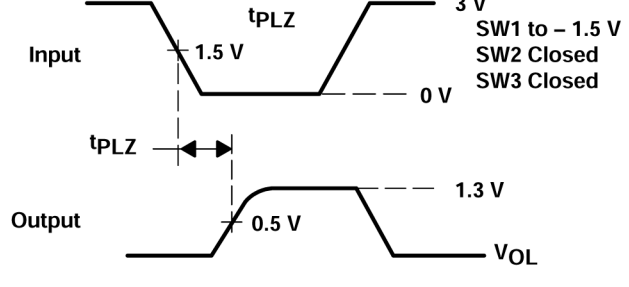
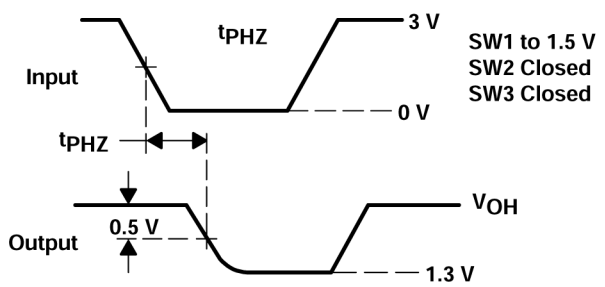
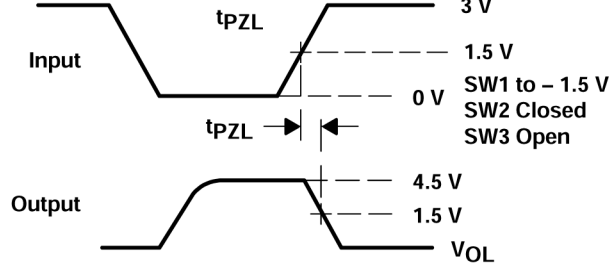
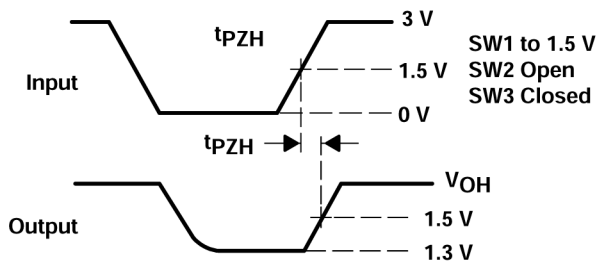
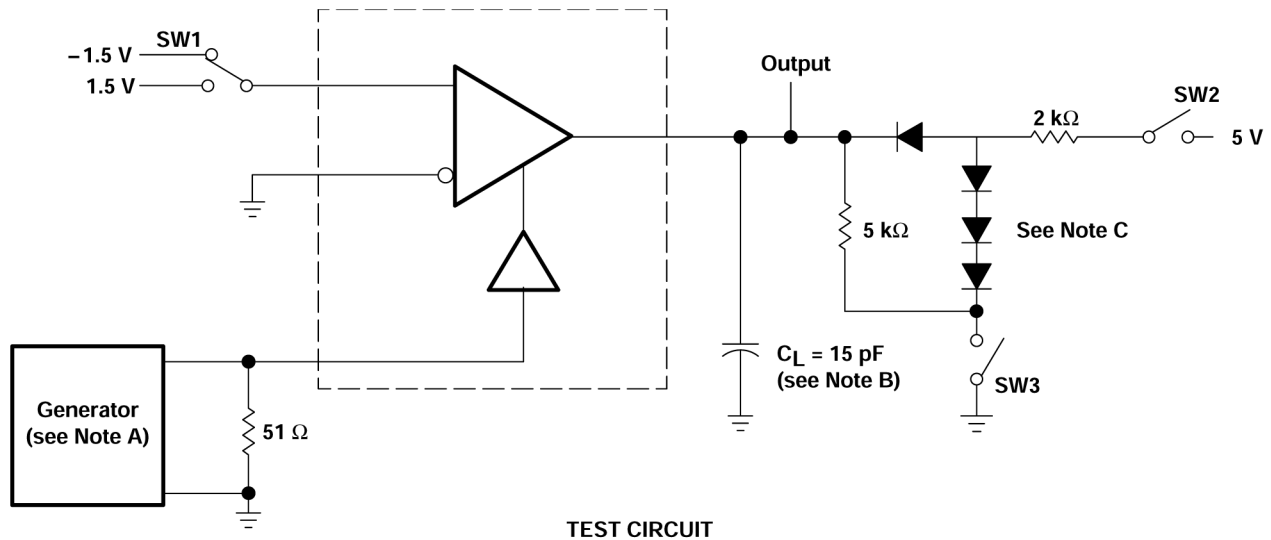


図 6-1.  $V_{OH}$ ,  $V_{OL}$



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns.
- B.  $C_L$  includes probe and stray capacitance.

図 6-2. Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t<sub>r</sub> ≤ 6 ns, t<sub>f</sub> ≤ 6 ns.
- B. C<sub>L</sub> includes probe and stray capacitance.
- C. All diodes are 1N916 or equivalent.

图 6-3. Test Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

| DIFFERENTIAL INPUTS                     | ENABLE <sup>(1)</sup> | OUTPUT |
|---|-----------------------|--------|
| A-B                                     |                       | Y      |
| $V_{ID} \leq 0.2\text{ V}$              | H                     | H      |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | H                     | ?      |
| $V_{ID} \leq -0.2\text{ V}$             | H                     | L      |
| Irrelevant                              | L                     | Z      |
| Open                                    | H                     | ?      |

(1) H = high level, L = low level, Z = high impedance (off), ? = indeterminate

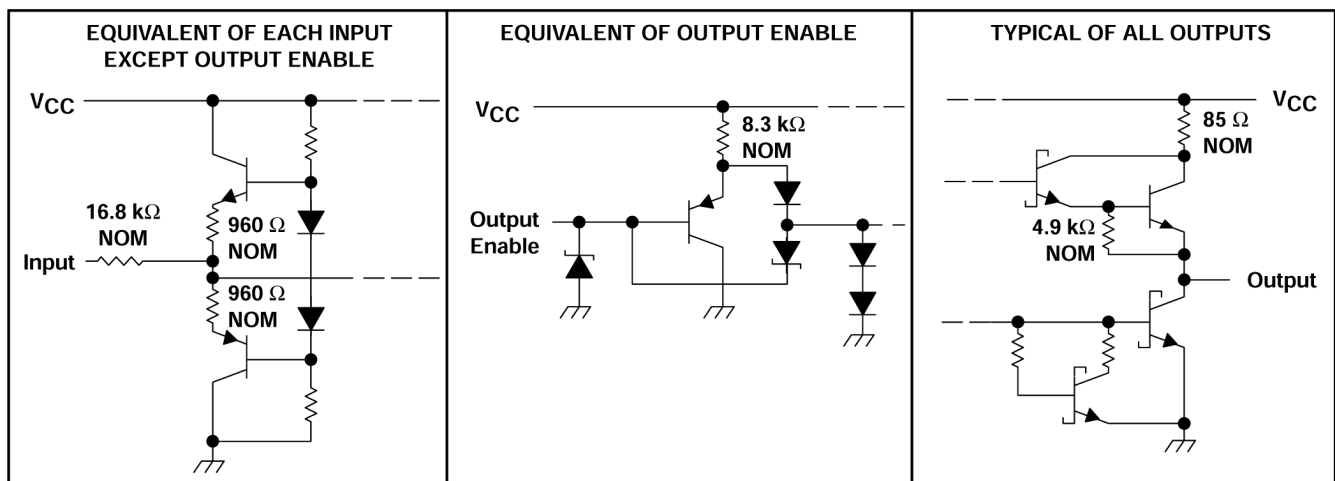


図 7-1. Schematics of Inputs and Outputs



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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### 8.3 商標

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TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (February 2002) to Revision D (October 2023) | Page |
|--|------|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....                                 | 1    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| MC3486D          | OBSOLETE      | SOIC         | D               | 16   |             | TBD             | Call TI                              | Call TI              | 0 to 70      | MC3486                  |         |
| MC3486DR         | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | MC3486                  | Samples |
| MC3486DRE4       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | MC3486                  | Samples |
| MC3486N          | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | MC3486N                 | Samples |
| MC3486NE4        | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | MC3486N                 | Samples |
| MC3486NSR        | ACTIVE        | SO           | NS              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | MC3486                  | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MC3486DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MC3486NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| MC3486DR  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| MC3486NSR | SO           | NS              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device    | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MC3486N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| MC3486N   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| MC3486NE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| MC3486NE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |





# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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