MCT8315Z センサ付き台形統合 FET BLDC モータードライバ

1 特長

- センサ付き台形波制御機能を内蔵した三相 BLDC モーター ドライバ
  - ホール センサを使った台形波 (120°) 整流
  - アナログまたはデジタル ホール入力をサポート
  - 設定可能な PWM 変調：同期 / 非同期
  - サイクル単位の電流制限により位相電流を制限
  - 最大 200kHz の PWM 周波数をサポート
  - アクティブ消磁により電力損失を低減
- 動作電圧：4.5V ~ 35V (絶対最大定格 40V)
- 高い出力電流能力：4A ピーク
- 低い MOSFET オンステート抵抗
  - T_A = 25℃で 275mΩ (標準値) の $R_{DS(ON)}$ (HS + LS)
- 低消費電力スリープ モード
  - V_{VM} = 24V、T_A = 25℃で 2.5µA (最大値)
- 内蔵の電流制限機能により外付け電流センス抵抗が不要
- 柔軟なデバイス構成オプション
  - MCT8315ZR：デバイスの構成とフォルト ステータスのための 5MHz、16 ビット SPI インターフェイス
  - MCT8315ZH：ハードウェア ピンを使った構成、降圧あり
  - MCT8315ZT：ハードウェア ピンを使った構成、降圧なし
- 1.8V、3.3V、5V の各ロジック入力に対応
- 3.3V/5V、200mA の降圧レギュレータを内蔵
- 3.3V、30mA の LDO レギュレータを内蔵
- 遅延補償によりデューティ サイクルの歪みを低減
- 各種保護機能を内蔵
  - 電源低電圧誤動作防止 (UVLO)
  - チャージ ポンプ低電圧 (CPUV)
  - 過電流保護 (OCP)
  - モーター ロック保護
  - 熱警告およびシャットダウン (OTW/TSD)
  - フォルト状態通知ピン (nFAULT)
  - SPI インターフェイスによるフォルト診断 (オプション)

2 アプリケーション

- ブラシレス DC (BLDC) モーター モジュール
- CPAP 機器
- プリンタ
- ロボット型掃除機
- 小型家電製品
- OA 機器
- ファクトリ オートメーションおよびロボティクス

3 概要

MCT8315Z は、12V/24V ブラシレス DC モーターを駆動するための、シングルチップでコード不要のセンサ付き台形波ソリューションを提供します。BLDC モーターを回転させるために外部マイコンは必要ありません。MCT8315Z は、3 つのハーフブリッジを内蔵し、40V の絶対最大定格、275mΩ (HS + LS) という低い $R_{DS(ON)}$ を備えており、高い電力駆動能力を実現できます。内蔵の電流制限機能により、起動時または高負荷状態時にモーター電流が制限されるので、外付けの検出抵抗は不要です。MCT8315Z は、出力電圧が調整可能な降圧レギュレータと LDO を備えており、外部回路への電力供給に使用できます。MCT8315Z は、位置をセンスするために 3 個のアナログ ホール コンパレータを統合しており、センサ搭載の台形波 BLDC モーター制御を実現できます。制御方式は、モーター電流制限動作から進角まで、ハードウェア ピンまたはレジスタ設定を使って詳細に設定できます。速度は、PWM 入力を使って制御できます。

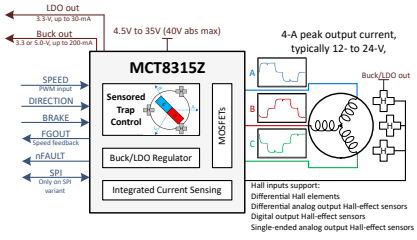
MCT8315Z には、電源低電圧誤動作防止 (UVLO)、過電圧保護 (OVP)、チャージ ポンプ低電圧 (CPUV)、過電流保護 (OCP)、過熱警告 (OTW)、過熱シャットダウン (PTSD) などの多くの保護機能が内蔵されており、デバイス、モーター、システムをフォルト イベントから保護します。フォルト状態は、nFAULT ピンで通知されます。

設計上の考慮事項とデバイス使用上の推奨事項については、Application Information を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
MCT8315ZR(3)	WQFN (32)	6 mm×4 mm
MCT8315ZH	WQFN (32)	6 mm×4 mm
MCT8315ZT(3)	WQFN (32)	6 mm×4 mm

(1) 詳細については、セクション 13 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) このデバイスはプレビュー版としてのみ供給されます。



概略回路図

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4 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial release.

5 Device Comparison Table

注

MCT8315ZR and MCT8315ZT variants are preview only, in pre-production status

DEVICE	PACKAGES	INTERFACE	BUCK REGULATOR
MCT8315ZR	32-pin WQFN (6x4 mm)	SPI	Yes
MCT8315ZH		Hardware	
MCT8315ZT		Hardware	No

表 5-1. MCT8315ZR vs MCT8315ZH vs MCT8315ZT configuration comparison

Parameters	MCT8315ZR (SPI variant)	MCT8315ZH(Hardware variant)	MCT8315ZT(Hardware variant, no buck)
PWM control mode settings	PWM_MODE (4 settings)	MODE pin (7 settings)	MODE pin (7 settings)
Slew rate settings	SLEW (4 settings)	SLEW pin (4 settings)	SLEW pin (4 settings)
Direction settings	DIR (2 settings)	DIR pin (2 settings)	DIR pin (2 settings)
DRVOFF pin configuration	DRV_OFF (2 settings)	Enabled	Enabled
Current limit threshold	ILIM pin: (AVDD/2 to AVDD/ 2-0.32)V	ILIM pin: (AVDD/2 to AVDD/ 2-0.32)V	ILIM pin: (AVDD/2 to AVDD/ 2-0.32)V
Current limit configuration	ILIM_RECIR (2 settings), PWM_100_DUTY_SEL	Recirculation fixed to Brake mode and PWM frequency for 100% duty fixed to 20 kHz	Recirculation fixed to Brake mode and PWM frequency for 100% duty fixed to 20 kHz
Lead angle	ADVANCE_LVL (8 settings)	ADVANCE pin (7 settings)	ADVANCE pin (7 settings)
Buck enable	BUCK_DIS (2 settings)	Enabled	N/A
Buck output	BUCK_SEL (4 settings)	Always set to 5-V	N/A
Buck configuration: power sequencing, current limit	BUCK_PS_DIS (2 settings) and BUCK_CL(2 settings)	Power sequencing enabled, current limit: 600 mA	N/A
FGOUT configuration	FGOUT_SEL (4 settings)	Fixed to 3x commutation frequency	Fixed to 3x commutation frequency
Motor lock configuration: mode, detection and retry timing	MTR_LOCK_MODE (4 settings), MTR_LOCK_TDET (4 settings), MTR_LOCK_RETRY (2 settings)	Enabled with 500-ms automatic retry time and detection time of 1000-ms	Enabled with 500-ms automatic retry time and detection time of 1000-ms
Active demagnetization	EN_AAR (2 settings) and EN_ASR (2 settings)	MODE pin (7 settings)	MODE pin (7 settings)
OCP configuration: Mode, level, deglitch time and retry time	OCP_MODE (2 settings) , OCP_LVL (2 settings) ,OCP_DEG (4 settings) and OCP_RETRY (2 settings)	Enabled with latched shutdown mode, level is fixed to 9-A with 0.6-µs deglitch time	Enabled with latched shutdown mode, level is fixed to 9-A with 0.6-µs deglitch time
Overvoltage protection configuration	OVP_EN (2 settings) , OVP_SEL (2 settings)	Enabled and level is fixed to 34-V (typ)	Enabled and level is fixed to 34-V (typ)
Driver delay compensation configuration	DLYCMP_EN (2 settings), DLY_TARGET (16 settings)	Disabled	Disabled
SDO pin configuration	SDO_MODE (2 settings)	N/A	N/A

6 Pin Configuration and Functions

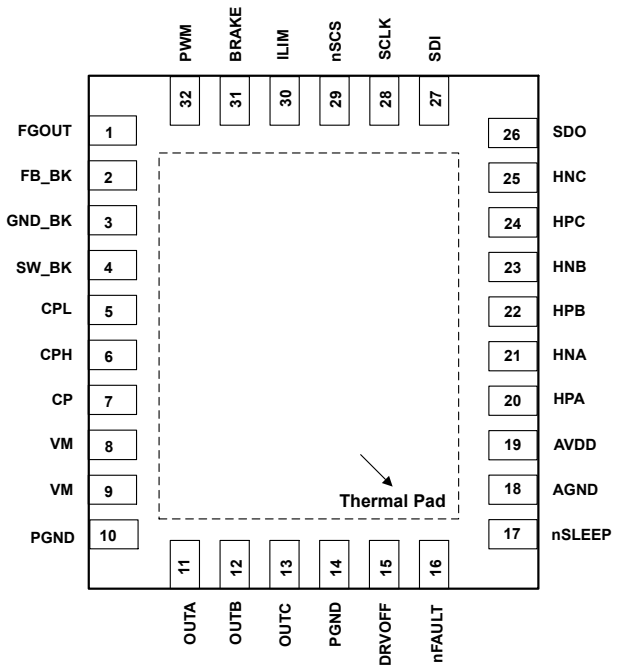

図 6-1. MCT8315ZR 32-Pin WQFN With Exposed Thermal Pad Top View

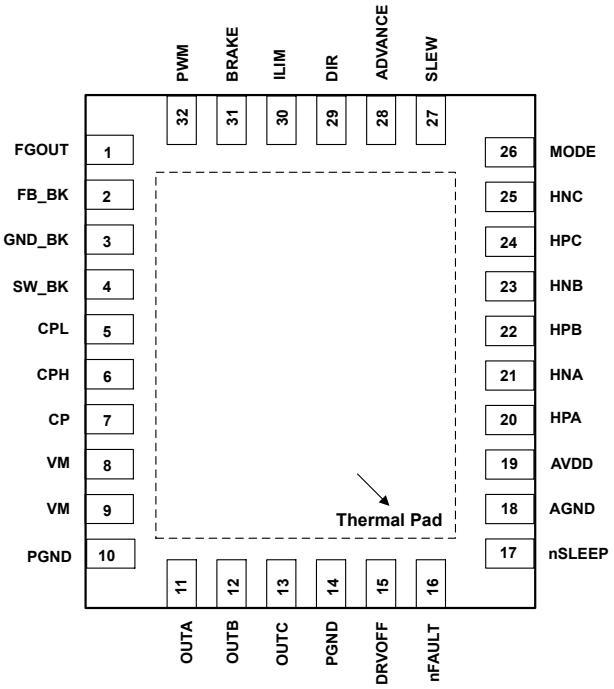

図 6-2. MCT8315ZH 32-Pin WQFN With Exposed Thermal Pad Top View

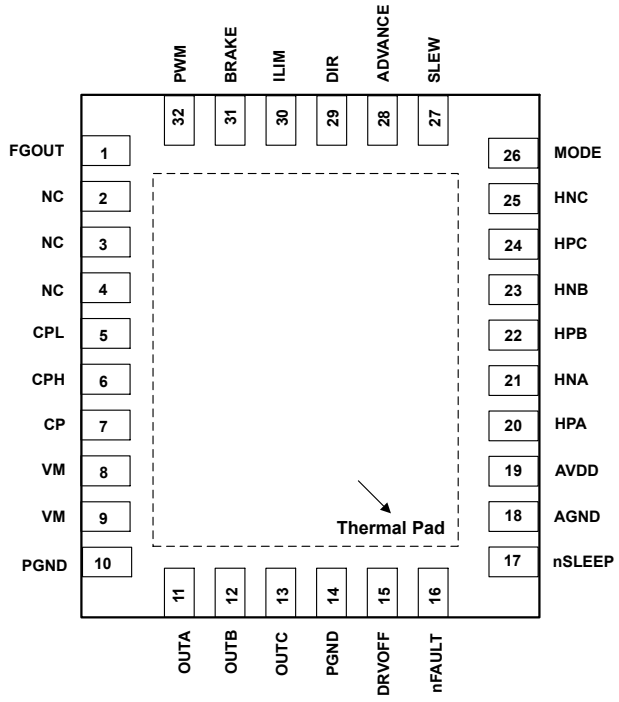

図 6-3. MCT8315ZT 32-Pin WQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN	32-pin package			TYPE[1]	DESCRIPTION
NAME	MCT8315ZR	MCT8315ZH	MCT8315ZT		
ADVANCE	—	28	28	I	Advance angle level setting. This pin is a 7-level input pin set by an external resistor.
AGND	18	18	18	GND	Device analog ground. Refer セクション 11.1 for connections recommendation.
AVDD	19	19	19	PWR O	3.3-V internal regulator output. Connect an X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30 mA externally.
BRAKE	31	31	31	I	High → Brake the motor by turning all low side MOSFETs ON Low → normal operation
CP	7	7	7	PWR O	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the CP and VM pins.
CPH	6	6	6	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	5	5	5	PWR	
DIR	—	29	29	I	Direction pin for setting the direction of the motor rotation to clockwise or counterclockwise.
DRVOFF	15	15	15	I	When this pin is pulled high, the six MOSFETs in the power stage are turned OFF making all outputs Hi-Z.
FB_BK	2	2	—	PWR I	Feedback for buck regulator. Connect to buck regulator output after the inductor/resistor.
FGOUT	1	1	1	O	Motor speed indicator output. Open-drain output requires an external pull-up resistor to 3.3-V to 5-V. It can be set to different division factor of Hall signals (see セクション 8.3.15)
GND_BK	3	3	3	GND	Buck regulator ground. Refer セクション 11.1 for connections recommendation.
HPA	20	20	20	I	Phase A hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPB	22	22	22	I	Phase B hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPC	24	24	24	I	Phase C hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNA	21	21	21	I	Phase A hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNB	23	23	23	I	Phase B hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNC	25	25	25	I	Phase C hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
ILIM	30	30	30	I	Set the threshold for phase current used in cycle by cycle current limit.
MODE	—	26	26	I	PWM input mode setting. This pin is a 7-level input pin set by an external resistor.
NC	—	—	2, 3, 4	—	Pins 2, 4: No connection, open Pin 3: Tie to PGND

表 6-1. Pin Functions (続き)

PIN	32-pin package			TYPE(1)	DESCRIPTION
NAME	MCT8315ZR	MCT8315ZH	MCT8315ZT		
nFAULT	16	16	16	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 3.3-V to 5-V. If external supply is used to pull-up nFAULT, make sure that it is pulled to >2.2-V on power up, or the device may enter test mode.
nSCS	29	—	—	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	17	17	17	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 20 to 40-µs low pulse can be used to reset fault conditions without entering sleep mode.
OUTA	11	11	11	PWR O	Half-bridge output A
OUTB	12	12	12	PWR O	Half-bridge output B
OUTC	13	13	13	PWR O	Half-bridge output C
PGND	10, 14	10, 14	10, 14	GND	Device power ground. Refer セクション 11.1 for connections recommendation.
PWM	32	32	32	I	PWM input for motor control. Set the duty cycle and switching frequency of the phase voltage of the motor.
SCLK	28	—	—	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	27	—	—	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	26	—	—	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SLEW	—	27	27	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor (Hardware devices).
SW_BK	4	4	—	PWR O	Buck switch node. Connect this pin to an inductor or resistor.
VM	8, 9	8, 9	8, 9	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with two 0.1-µF capacitors (for each pin) plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad				GND	Must be connected to AGND

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (GND_BK, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_M + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_M + 0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	6	V
Switching node pin voltage (SW_BK)	–0.3	V_M + 0.3	V
Analog regulator pin voltage (AVDD)	–0.3	4	V
Logic pin input voltage (BRAKE, DIR, DRVOFF, PWM, nSCS, nSLEEP, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO)	–0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			200	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			4	A
V_{IN}	Logic input voltage	BRAKE, DIR, DRVOFF, PWM, nSCS, nSLEEP, SCLK, SDI	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, SDO, FGOUT	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		5.5	V
I_{OD}	Open drain output current	nFAULT, SDO, FGOUT			5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		MCT8315ZR, MCT8315ZT, MCT8315ZH	UNIT
		WQFN (RRY)	
		32 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, nSLEEP = 0, T_A = 25 °C		1.5	2.5	µA
		nSLEEP = 0		2.5	5	µA
I_{VMS}	VM standby mode current (Buck regulator disabled)	nSLEEP = 1, PWM = 0, SPI = 'OFF', BUCK_DIS = 1;		4	10	mA
		V_{VM} > 6 V, nSLEEP = 1, PWM = 0, SPI = 'OFF', T_A = 25 °C, BUCK_DIS = 1;		4	5	mA
I_{VMS}	VM standby mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, PWM = 0, SPI = 'OFF', I_{BK} = 0, T_A = 25 °C, BUCK_DIS = 0;		5	6.5	mA
		nSLEEP = 1, PWM= 0, SPI = 'OFF', I_{BK} = 0, BUCK_DIS = 0;		6	10	mA
I_{VM}	VM operating mode current (Buck regulator disabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 1		10	13	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 1		18	21	mA
		nSLEEP =1, f_{PWM} = 25 kHz, BUCK_DIS = 1		11	15	mA
		nSLEEP =1, f_{PWM} = 200 kHz, BUCK_DIS = 1		17	24	mA
I_{VM}	VM operating mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		11	13	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		19	22	mA
		nSLEEP =1, f_{PWM} = 25 kHz, BUCK_DIS = 0; BUCK_PS_DIS = 0		12	16	mA
		nSLEEP =1, f_{PWM} = 200 kHz, BUCK_DIS = 0; BUCK_PS_DIS = 0		18	27	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA	3.1	3.3	3.465	V
I_{AVDD}	External analog regulator load				30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	3.6	4.7	5.2	V

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			1	ms
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b. 11b), 0 mA ≤ I_{BK} ≤ 200 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2)[1]		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 50 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2) [1]		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 40 mA		V_{VM}– I_{BK}*(R_{BK}+2)[1]		V
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA	4.6	5.0	5.4	
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 200 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2)[1]		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA	4.6	5.0	5.4	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 50 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2)[1]		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA	4.6	5.0	5.4	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 40 mA		V_{VM}– I_{BK}*(R_{BK}+2)[1]		V

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			200	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			200 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			50	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			50 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			40	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			40 – I_{AVDD}	mA
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz
V_{BK_UV}	Buck regulator undervoltage lockout (SPI Device)	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.2	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 01b	4.0	4.2	4.35	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.2	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 11b	4	4.2	4.35	V
V_{BK_UV}	Buck regulator undervoltage lockout (HW Device)	V_{BK} rising	4.2	4.4	4.55	V
V_{BK_UV}	Buck regulator undervoltage lockout (HW Device)	V_{BK} falling	4.0	4.2	4.35	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold	90	200	320	mV
I_{BK_CL}	Buck regulator current limit threshold (SPI Device)	BUCK_CL = 0b	360	600	900	mA
		BUCK_CL = 1b	80	150	250	mA
I_{BK_CL}	Buck regulator current limit threshold (HW Device)		360	600	900	mA
I_{BK_OCP}	Buck regulator overcurrent protection trip point		1.6	2.1	3	A
t_{BK_RETRY}	Overcurrent protection retry time		0.7	1	1.3	ms
LOGIC-LEVEL INPUTS (BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	Other Pins	1.5		5.5	V
		nSLEEP	1.6		5.5	V

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Input logic hysteresis	Other Pins	180	300	420	mV
		nSLEEP	95	250	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1.6		1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 5 V	10		30	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V	30		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	425	kΩ
		Other pins	70	100	130	kΩ
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		180	300	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–1		66	µA
R_{PU}	Input pullup resistance		80	100	130	kΩ
C_{ID}	Input capacitance			30		pF
FOUR-LEVEL INPUTS (SLEW)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.2*AVDD	V
V_{L2}	Input mode 2 voltage	Hi-Z	0.27*AVDD	0.5*AVDD	0.52*AVDD	V
V_{L3}	Input mode 3 voltage	47 kΩ +/- 5% tied to AVDD	0.62*AVDD	0.75*AVDD	0.88*AVDD	V
V_{L4}	Input mode 4 voltage	Tied to AVDD	0.97*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	70	100	130	kΩ
R_{PD}	Input pulldown resistance	To AGND	70	100	130	kΩ
SEVEN-LEVEL INPUTS (ADVANCE, MODE)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.06*AVDD	V
V_{L2}	Input mode 2 voltage	22 kΩ ± 5% to AGND	0.13*AVDD	0.15*AVDD	0.2*AVDD	V
V_{L3}	Input mode 3 voltage	100 kΩ ± 5% to AGND	0.27*AVDD	0.33*AVDD	0.38*AVDD	V
V_{L4}	Input mode 4 voltage	Hi-Z	0.47*AVDD	0.5*AVDD	0.52*AVDD	V
V_{L5}	Input mode 5 voltage	100 kΩ ± 5% to AVDD	0.62*AVDD	0.66*AVDD	0.7*AVDD	V
V_{L6}	Input mode 6 voltage	22 kΩ ± 5% to AVDD	0.8*AVDD	0.84*AVDD	0.88*AVDD	V
V_{L7}	Input mode 7 voltage	Tied to AVDD	0.97*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (FGOUT, nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA	2.2		5.5	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		275	295	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		285	305	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		415	455	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		425	465	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND	15	25	45	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin in Hi-Z	30	50	80	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	210	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD	130	200	315	V/us
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND	15	25	50	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin in Hi-Z	30	50	95	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	235	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD	130	200	345	V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			5	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time	V_{VM} = 24 V, SR = 25 V/µs, HS driver ON to LS driver OFF		1800	3400	ns
		V_{VM} = 24 V, SR = 50 V/µs, HS driver ON to LS driver OFF		1100	1550	ns
		V_{VM} = 24 V, SR = 125 V/µs, HS driver ON to LS driver OFF		650	1000	ns
		V_{VM} = 24 V, SR = 200 V/µs, HS driver ON to LS driver OFF		500	750	ns
t_{PD}	Propagation delay	V_{VM} = 24 V, PWM = 1 to OUTx transisition, SR = 25 V/µs		2000	4550	ns
		V_{VM} = 24 V, PWM = 1 to OUTx transisition, SR = 50V/µs		1200	2150	ns
		V_{VM} = 24 V, PWM = 1 to OUTx transisition, SR = 125 V/µs		800	1350	ns
		V_{VM} = 24 V, PWM= 1 to OUTx transisition, SR = 200 V/µs		650	1050	ns
t_{MIN_PULSE}	Minimum output pulse width	SR = 200 V/µs	600			ns
HALL COMPARATORS						

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ICM}	Input common mode voltage (Hall)		0.5		AVDD – 1.2	V
V_{HYS}	Voltage hysteresis (SPI Device)	HALL_HYS = 0	1.5	5	8	mV
		HALL_HYS = 1	35	50	80	mV
	Voltage hysteresis (HW Device)		1.5	5	8	mV
ΔV_{HYS}	Hall comparator hysteresis difference	Between Hall A, Hall B and Hall C comparator	–8		8	mV
$V_{H(MIN)}$	Minimum Hall differential voltage		40			mV
I_I	Input leakage current	HPX = HNX = 0 V	–1		1	µA
t_{HDG}	Hall deglitch time		0.6	1.15	1.7	µs
t_{E_HDG}	Hall enable deglitch time	During power up		1.4		µs
CYCLE-BY-CYCLE CURRENT LIMIT						
V_{ILIM}	Voltage on ILIM pin for cycle by cycle current limit		AVDD/2		AVDD/2–0.32	V
I_{LIMIT}	Current limit corresponding to ILIM pin voltage range		Current limit disabled		4	A
I_{LIM_AC}	Current limit accuracy(2)	I_{LIMIT} ≥ 1A	–14		14	%
t_{BLANK}	Cycle by cycle current limit blank time			5		µs
ADVANCE ANGLE						
θ_{ADV}	Advance Angle Setting (SPI Device)	ADVANCE_LVL = 000 b		0	1	°
		ADVANCE_LVL = 001 b	3	4	5	°
		ADVANCE_LVL = 010 b	6	7	8	°
		ADVANCE_LVL = 011 b	10	11	12	°
		ADVANCE_LVL = 100 b	13.5	15	16.5	°
		ADVANCE_LVL = 101 b	18	20	22	°
		ADVANCE_LVL = 110 b	22.5	25	27.5	°
		ADVANCE_LVL = 111 b	27	30	33	°
θ_{ADV}	Advance Angle Setting (HW Device)	Advance pin tied to AGND		0	1	°
		Advance pin tied to 22 kΩ ± 5% to AGND	3	4	5	°
		Advance pin tied to 100 kΩ ± 5% to AGND	10	11	12	°
		Advance pin in Hi-Z	13.5	15	16.5	°
		Advance pin tied to 100 kΩ ± 5% to AVDD	18	20	22	°
		Advance pin tied to 22 kΩ ± 5% to AVDD	22.5	25	27.5	°
		Advance pin tied to AVDD	27	30	33	°
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.3	4.4	4.5	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	5	7	µs

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.3	2.5	2.7	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	75	100	140	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.4	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 0b	5.5	9	12	A
		OCP_LVL = 1b	9	13	18	A
	Overcurrent protection trip point (HW Device)		5.5	9	12	A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.02	0.2	0.4	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.5	1.2	1.8	µs
		OCP_DEG = 11b	0.9	1.6	2.5	µs
	Overcurrent protection deglitch time (HW Device)		0.2	0.6	1.2	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
t_{MTR_LOCK}	Motor lock detection time (SPI Device)	MOTOR_LOCK_TDET = 00b	270	300	330	ms
		MOTOR_LOCK_TDET = 01b	450	500	550	ms
		MOTOR_LOCK_TDET = 10b	900	1000	1100	ms
		MOTOR_LOCK_TDET = 11b	4500	5000	5500	ms
t_{MTR_LOCK}	Motor lock detection time (HW Device)		900	1000	1100	ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (SPI Device)	MOTOR_LOCK_RETRY = 0b	450	500	550	ms
		MOTOR_LOCK_RETRY = 1b	4500	5000	5500	ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (HW Device)		450	500	550	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	155	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	15	20	30	°C
T_{TSD}	Thermal shutdown temperature (Buck)	Die temperature (T_J)	170	180	190	°C
T_{TSD_HYS}	Thermal shutdown hysteresis (Buck)	Die temperature (T_J)	15	20	30	°C
T_{TSD_FET}	Thermal shutdown temperature (FET)	Die temperature (T_J)	165	175	185	°C

7.5 Electrical Characteristics (続き)

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{TSD\_FET\_HYS}$	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	15	20	30	°C

(1) R_{LBK} is resistance of inductor L_{BK}
(2) Current limit accuracy depends on blanking time, motor parameters and VM

7.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

7.7 SPI Secondary Device Mode Timings

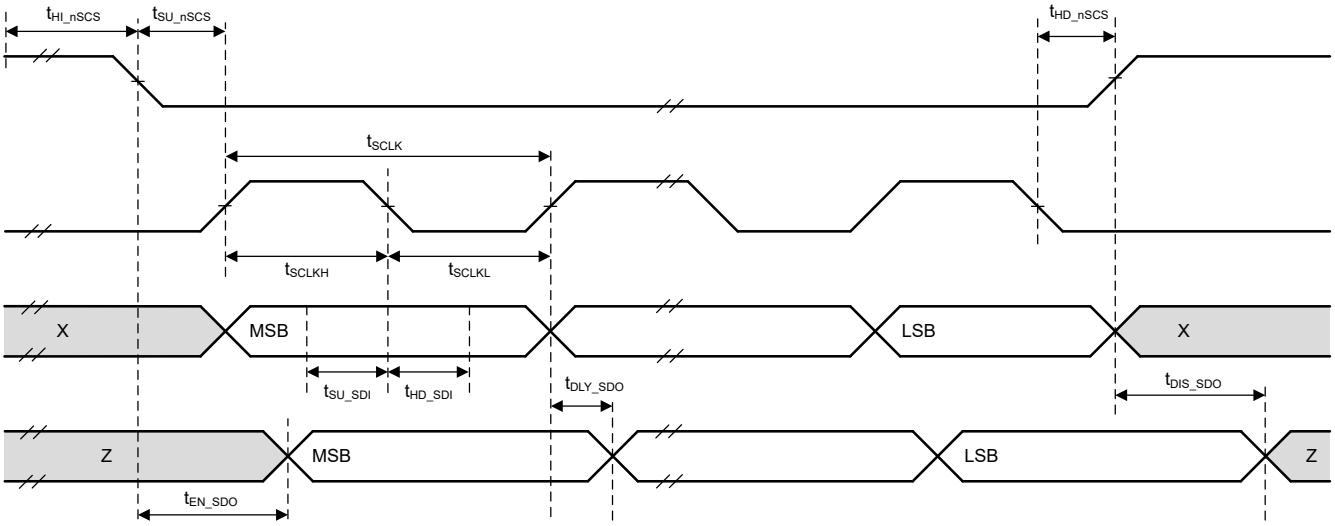

図 7-1. SPI Secondary Device Mode Timing Diagram

7.8 Typical Characteristics

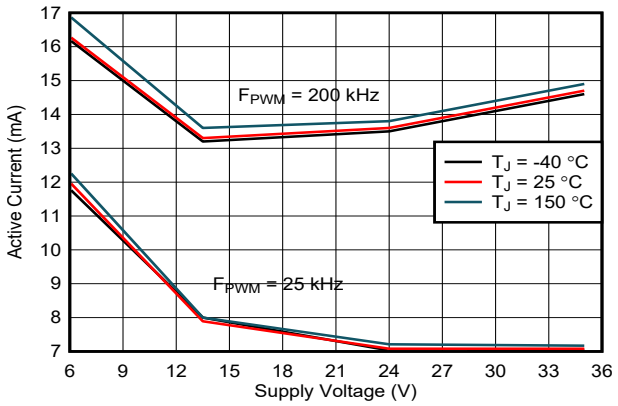

図 7-2. Supply current over supply voltage

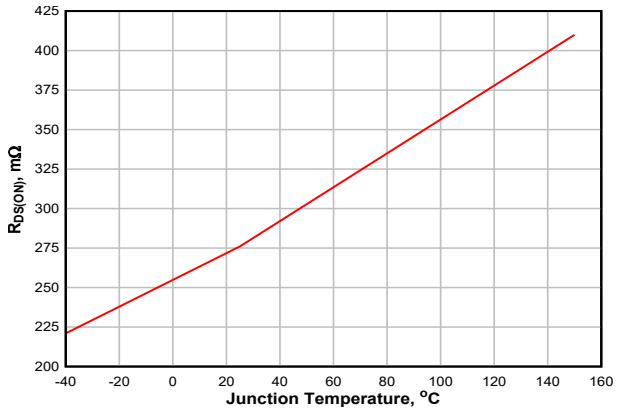

図 7-3. $R_{DS(ON)}$ (high and low side combined) for MOSFETs over temperature

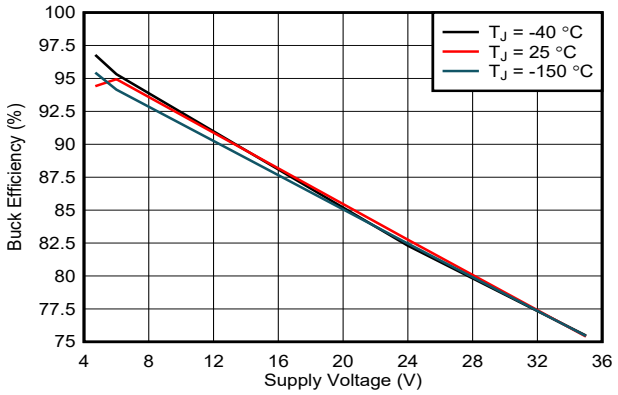

図 7-4. Buck regulator efficiency over supply voltage

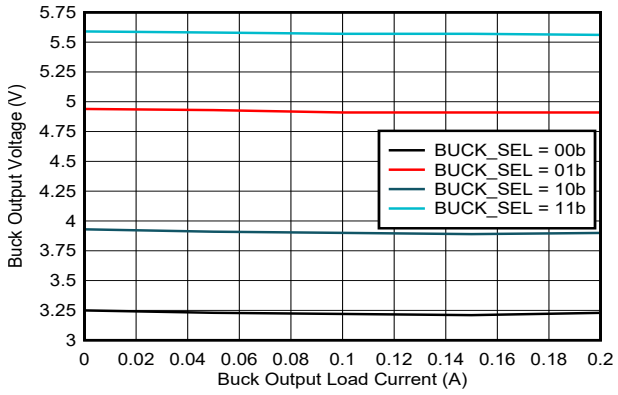

図 7-5. Buck regulator output voltage over load current

8 Detailed Description

8.1 Overview

The MCT8315Z device is an integrated 275-mΩ (high-side + low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, linear regulator and buck regulator for external loads. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external microcontroller. Alternatively, hardware interface (pin) variants allow for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events and dv/dt parasitic turn-on of the internal power MOSFETs.

The MCT8315Z device integrates three-phase sensored trapezoidal commutation using analog or digital hall sensors for position detection.

In addition to the high level of device integration, MCT8315Z provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator UVLO and overtemperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI variant.

The MCT8315ZR, MCT8315ZT and MCT8315ZH devices are available in a 0.5-mm pin pitch, WQFN surface-mount package. The WQFN package size is 6 mm × 4 mm.

8.2 Functional Block Diagram

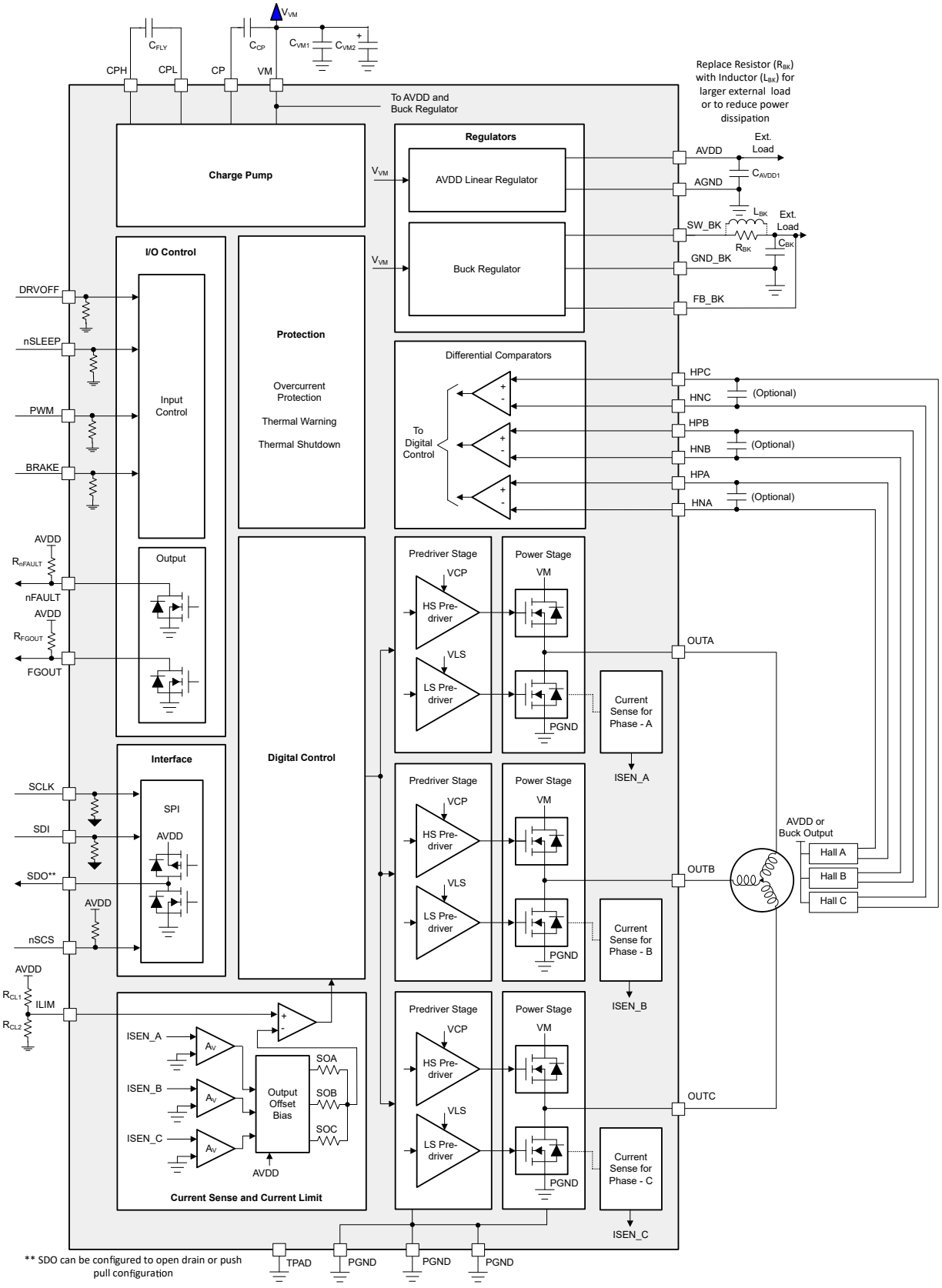

図 8-1. MCT8315ZR Block Diagram

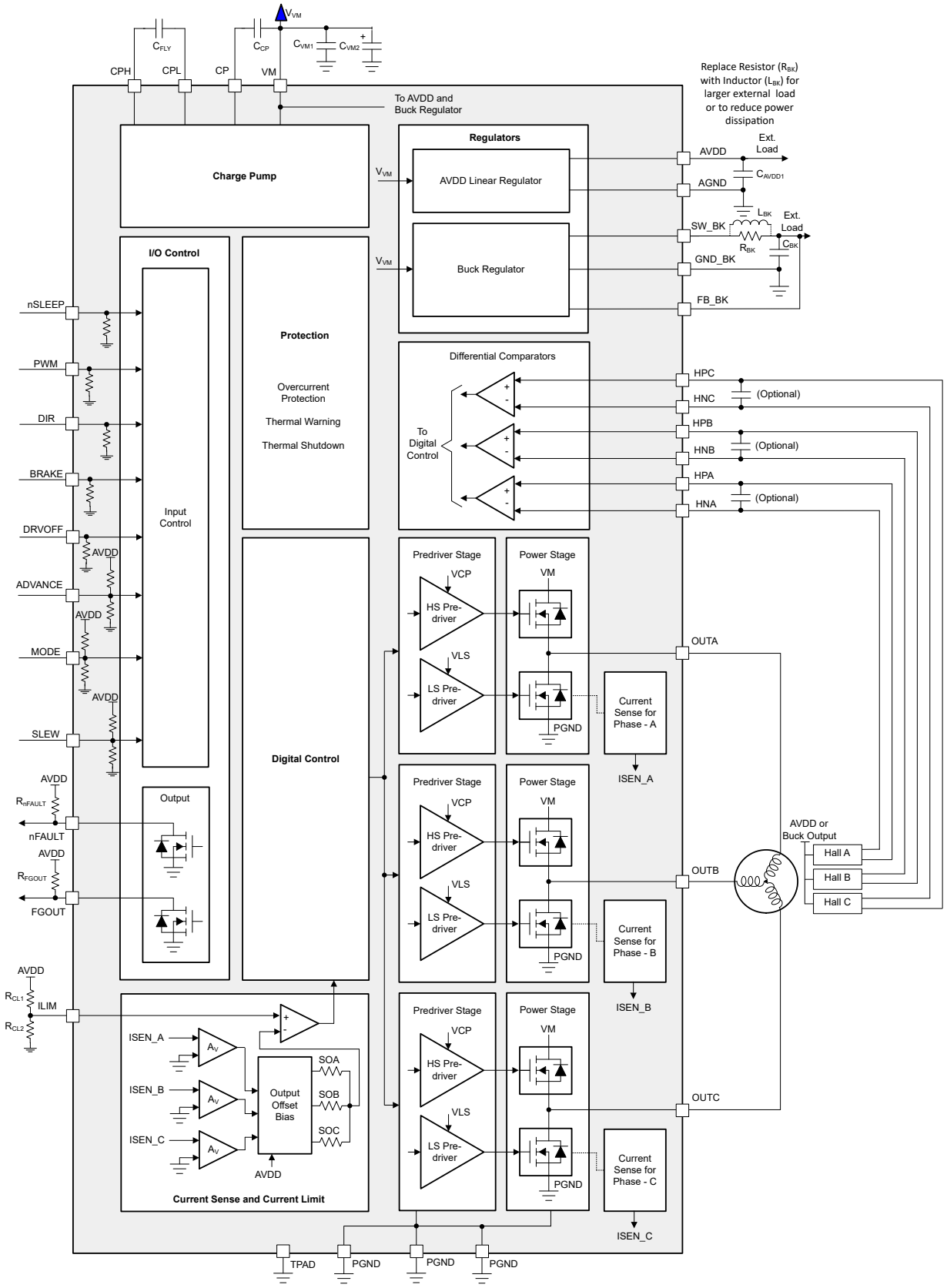

図 8-2. MCT8315ZH Block Diagram

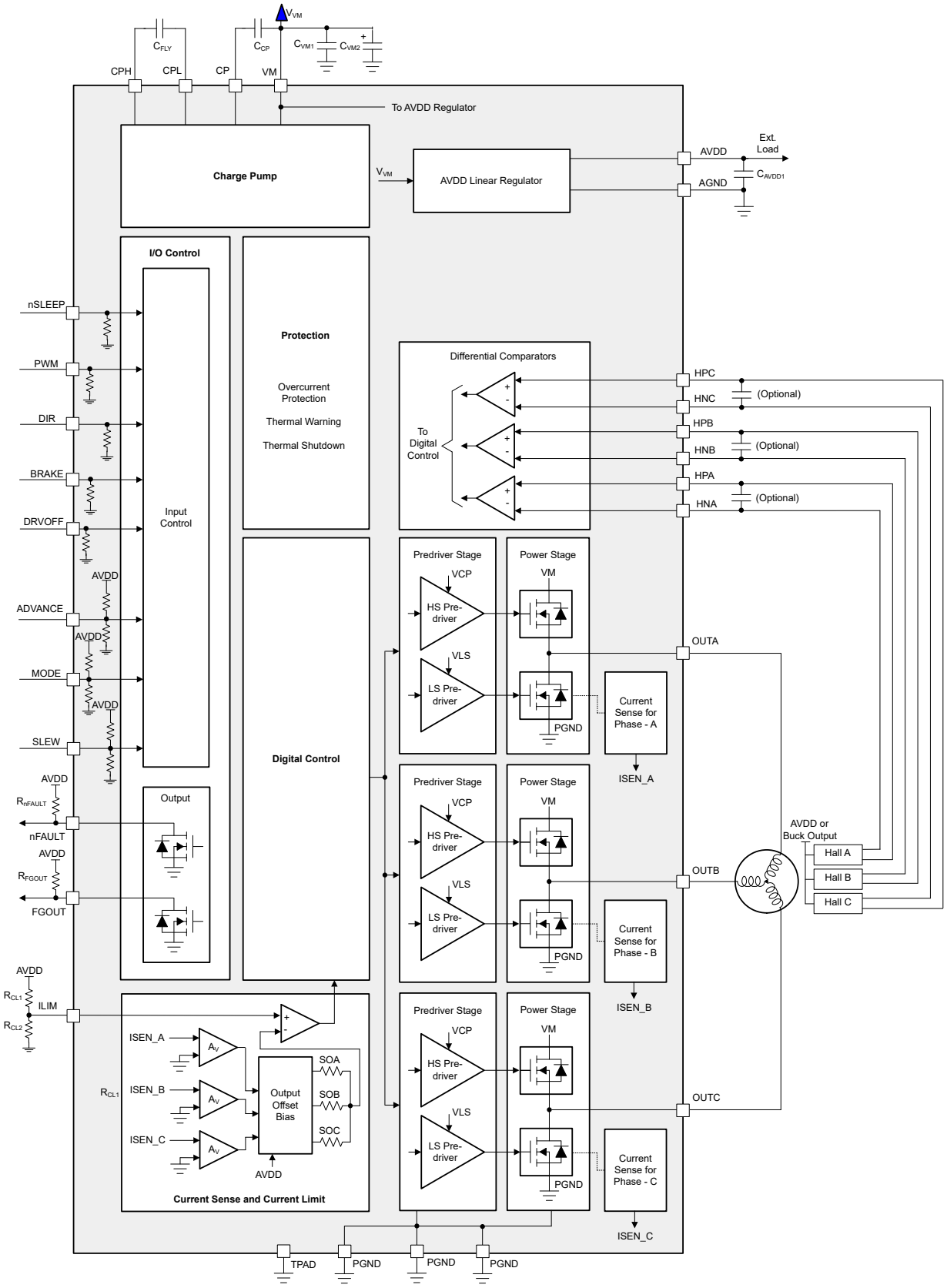

図 8-3. MCT8315ZT Block Diagram

8.3 Feature Description

表 8-1 lists the recommended values of the external components for the driver.

表 8-1. MCT8315Z External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-µF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 1.3-µF at 3.3-V across operating temperature.
C_{BK}	FB_BK	GND_BK	X5R or X7R, 22-µF, buck-output rated capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
L_{BK}	SW_BK	FB_BK	Output inductor
R_{nFAULT}	VCC	nFAULT	5.1-kΩ, Pullup resistor
R_{MODE}	MODE	AGND or AVDD	MCT8315Z hardware interface
R_{SLEW}	SLEW	AGND or AVDD	MCT8315Z hardware interface
$R_{ADVANCE}$	ADVANCE	AGND or AVDD	MCT8315Z hardware interface
C_{ILIM}	ILIM	AGND	X5R or X7R, 0.1-µF, AVDD-rated capacitor (optional)

注

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, ensure that it is pulled to >2.2V on power up or the device will enter internal test mode.

8.3.1 Output Stage

The MCT8315Z device consists of an integrated 275-mΩ (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase H-bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The device has two VM motor power-supply pins which are to be connected together to the motor-supply voltage.

8.3.2 PWM Control Mode (1x PWM Mode)

The MCT8315Z family of devices provides seven different control modes to support various commutation and control methods. The MCT8315Z device provides a 1x PWM control mode for driving the BLDC motor in trapezoidal current-control mode. The MCT8315Z device uses 6-step block commutation tables that are stored internally. This feature lets a three-phase BLDC motor be controlled using a single PWM sourced from a simple controller. The PWM is applied on the PWM pin and determines the output frequency and duty cycle of the half-bridges.

The MCT8315Z family of devices supports both analog and digital hall inputs by changing mode input setting. Differential hall inputs should be connected to HPx and HNx pins (see 図 8-4). Digital hall inputs should be connected to the HPx pins while keeping the HNx pins floating (see 図 8-5).

The half-bridge output states are managed by the HPA, HNA, HPB, HNB, HPC and HNC pins in analog mode and HPA, HPB, HPC in digital mode which are used as state logic inputs. The state inputs are the position feedback of the BLDC motor. The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) as shown below

表 8-2. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	Analog Hall Input	Asynchronous	ASR and AAR Disabled
Mode 2	Connected to AGND with R_{MODE1}	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to AVDD with R_{MODE2}	Analog Hall Input	Synchronous	ASR and AAR Enabled
Mode 6	Connected to AVDD with R_{MODE1}	Digital Hall Input	Synchronous	ASR and AAR Enabled
Mode 7	Connected to AVDD			

注

Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set PWM to a low level before changing the PWM_MODE register.

8.3.2.1 Analog Hall Input Configuration

図 8-4 shows the connection of Analog Hall inputs to the driver. Analog hall elements are fed to the hall comparators, which zero crossing is used to generate the commutation logic.

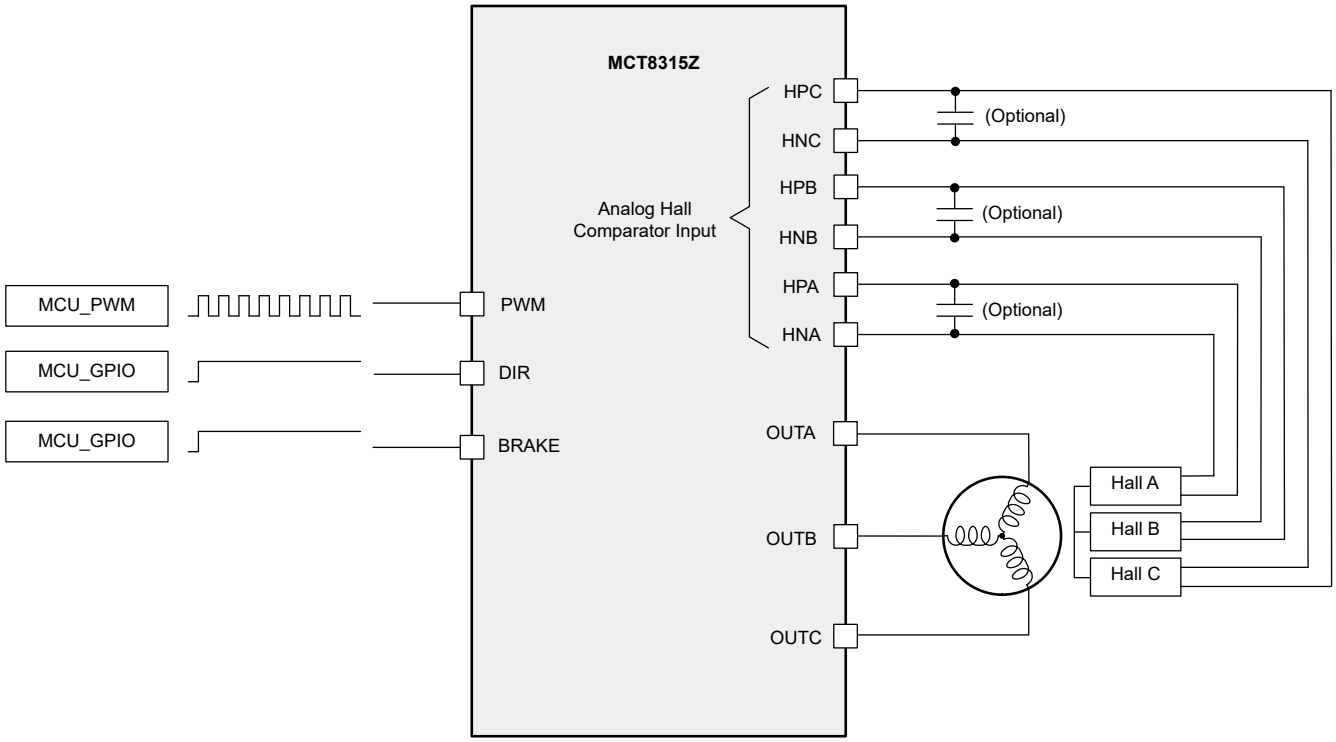

図 8-4. 1x PWM Mode with Analog Hall Input

注

Texas Instruments recommends motor direction (DIR) change when the motor is stationary.

8.3.2.2 Digital Hall Input Configuration

図 8-5 shows the connection of Digital Hall inputs to the driver.

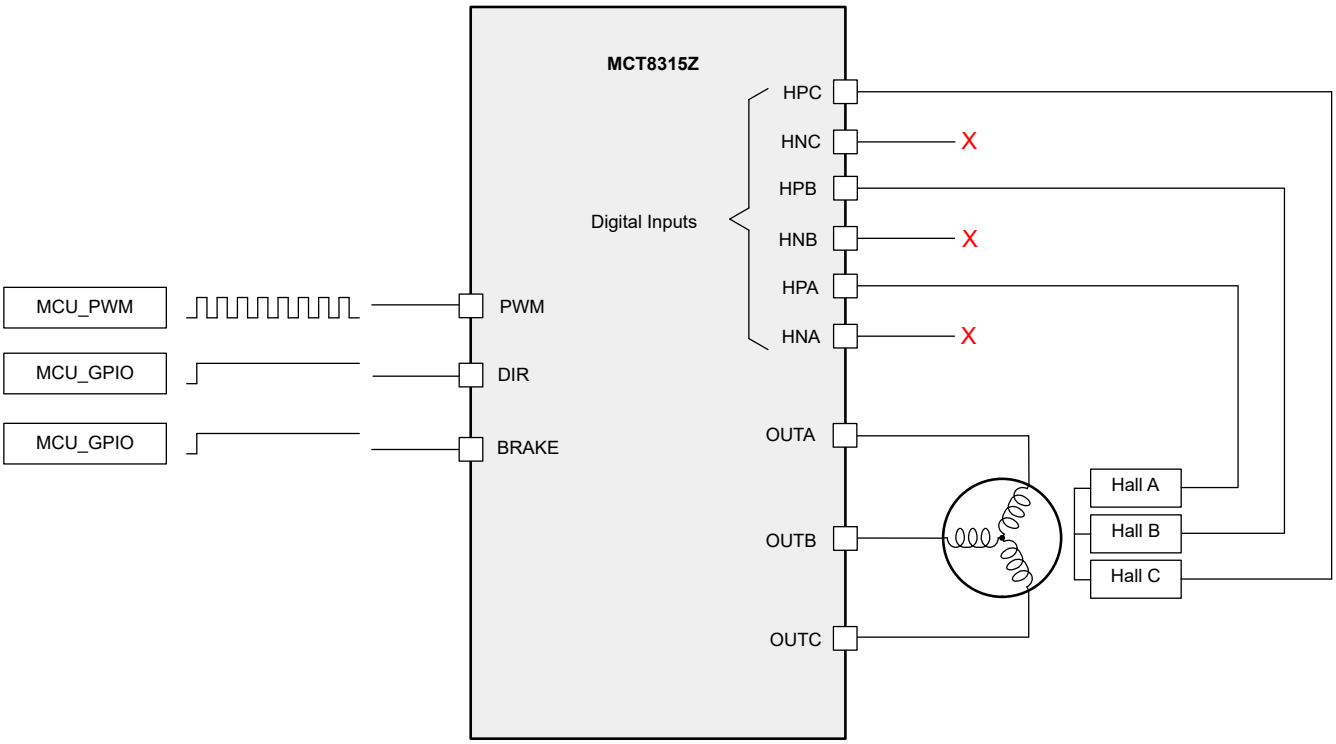

図 8-5. 1x PWM Mode with Digital Hall Input

8.3.2.3 Asynchronous Modulation

The DIR pin controls the direction of BLDC motor in either clockwise or counter-clockwise direction. Tie the DIR pin low if this feature is not required.

The BRAKE input halts the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled high. This brake is independent of the states of the other input pins. Tie the BRAKE pin low if this feature is not required.

表 8-3 shows the configuration in 1x PWM mode with asynchronous modulation.

表 8-3. Asynchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

8.3.2.4 Synchronous Modulation

表 8-4 shows the configuration in 1x PWM mode with synchronous modulation.

表 8-4. Synchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

8.3.2.5 Motor Operation

図 8-6 and 図 8-7 shows the BLDC motor commutation with direction setting (DIR) as 0 and 1 respectively.

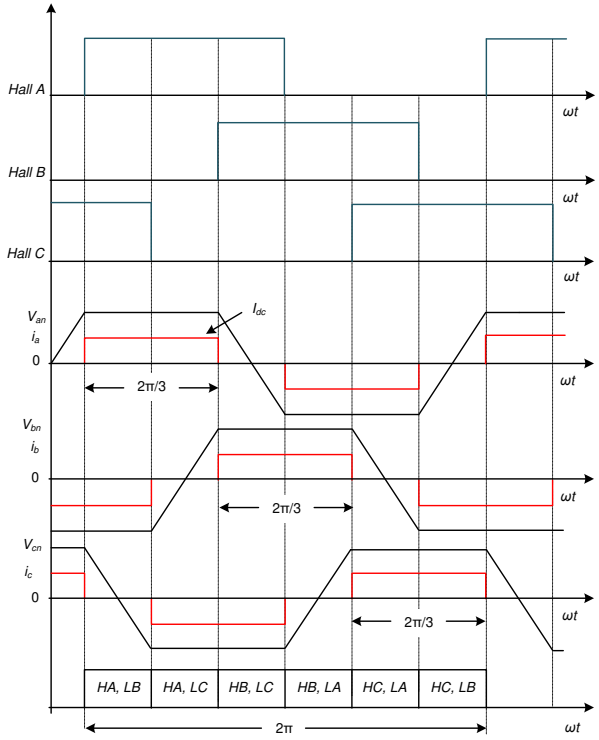

図 8-6. BLDC Motor Commutation with DIR = 0

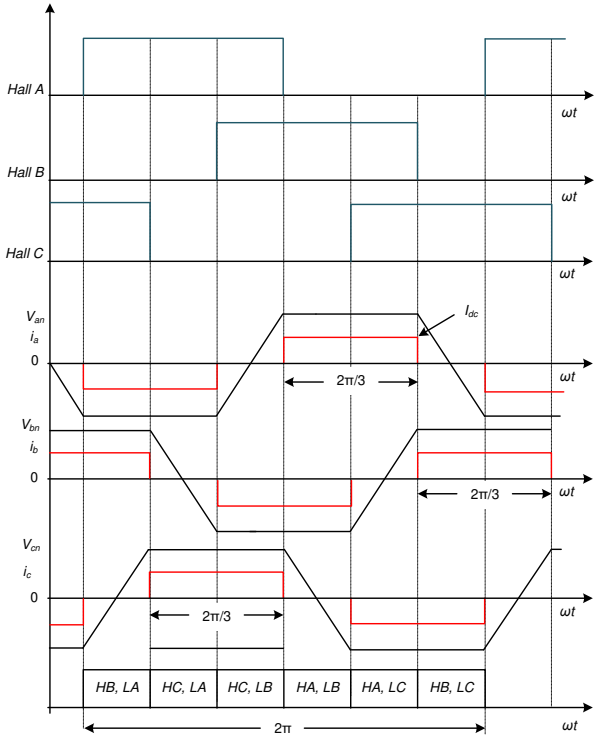

図 8-7. BLDC Motor Commutation with DIR = 1

8.3.3 Device Interface Modes

MCT8315Z supports two different interface modes (SPI and hardware) to provide either flexibility or simplicity to users. The two interface modes share the same pins (except pins 26-29) allowing the different versions to be largely pin-to-pin compatible. This compatibility allows application designers to evaluate with one interface variant and switch to another with minimal modifications to their design.

8.3.3.1 Serial Peripheral Interface (SPI)

The SPI variant supports a serial communication bus that allows an external microcontroller to send and receive data with MCT8315Z. This allows the external microcontroller to configure device settings and read detailed fault information. The SPI interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin can be configured to either open-drain or push-pull through SDO_MODE.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the MCT8315Z.

For more information on the SPI, see the セクション 8.5 section.

8.3.3.2 Hardware Interface

Hardware variant uses three resistor-configurable inputs (in the place of SPI pins) which are ADVANCE, MODE and SLEW.

This variant allows the application designer to configure the critical device settings by tying each pin to logic high or logic low or leave it floating or pull-up to logic high or pull-down to logic low with a suitable resistor. This eliminates the requirement for an SPI bus from the external microcontroller to configure MCT8315Z. General fault information can still be obtained through the nFAULT pin. The voltage levels on the configurable pins (ADVANCE, SLEW and MODE) are detected only once during power-up and used for device configuration - any subsequent change in the voltage of these pins does not affect the device configuration till a subsequent power reset.

- The MODE pin configures the PWM control mode.
- The SLEW pin configures the slew rate of the output voltage.
- The ADVANCE pin configures the lead angle of the output with respect to hall signals.

For more information on the hardware interface, see the *セクション 8.3.10* section.

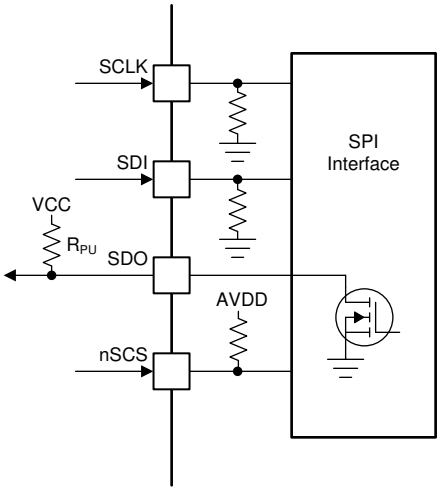

図 8-8. MCT8315ZR SPI Interface

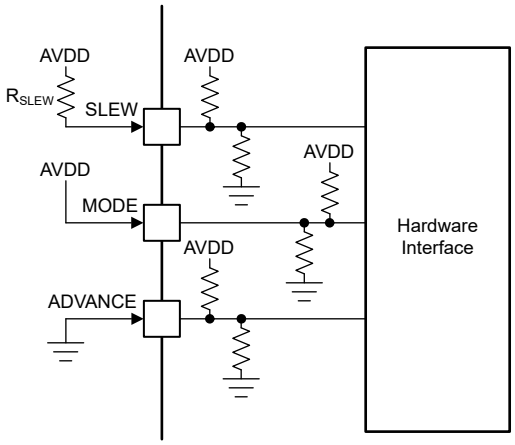

図 8-9. MCT8315ZT/H Hardware Interface

8.3.4 Step-Down Mixed-Mode Buck Regulator

The MCT8315Z has an integrated mixed-mode buck regulator to supply regulated 3.3-V or 5.0-V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4.0-V or 5.7-V for supporting the extra headroom for external LDO for generating a 3.3-V or 5.0-V supplies. The output voltage of the buck converter is set by BUCK_SEL bits in the MCT8315ZR device (SPI variant). The output voltage of the buck converter in MCT8315ZH (hardware variant) is always set to 5.0-V.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

To disable the buck regulator, set the BUCK_DIS bit to 1b in MCT8315ZR (SPI variant). The buck regulator cannot be disabled in MCT8315ZH (hardware variant). MCT8315ZT has no buck regulator.

注

If the buck regulator is unused in MCT8315ZH, the buck pins SW_BK, GND_BK, and FB_BK cannot be left floating or connected to ground. The buck regulator components L_{BK}/R_{BK} and C_{BK} must be connected in hardware.

表 8-5. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD})	Max output current from Buck (I_{BK})	Buck current limit	AVDD power sequencing
Inductor - 47 µH	3.3-V or 4.0-V or 5.0-V or 5.7-V	30 mA	200 mA	600 mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 47 µH	5.0-V or 5.7-V	30 mA	200 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0)
Inductor - 22 µH	3.3-V or 4.0-V or 5.0-V or 5.7-V	30 mA	50 mA	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 22 µH	5.0-V or 5.7-V	30 mA	50 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)
Resistor - 22 Ω	3.3-V or 4.0-V or 5.0-V or 5.7-V	30 mA	40 mA	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Resistor - 22 Ω	5.0-V or 5.7-V	30 mA	40 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)

8.3.4.1 Buck in Inductor Mode

The buck regulator in MCT8315Z device is primarily designed to support low inductance of 47 µH and 22 µH inductors. The 47 µH inductor allows the buck regulator to operate up to 200 mA load current support, whereas the 22 µH inductor limits the load current to 50 mA.

図 8-10 shows the connection of buck regulator in inductor mode.

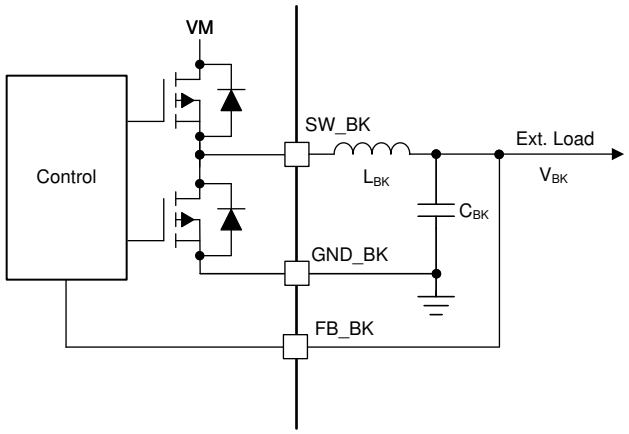

図 8-10. Buck (Inductor Mode)

8.3.4.2 Buck in Resistor mode

If the external load requirements is less than 40 mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

図 8-11 shows the connection of buck regulator in resistor mode.

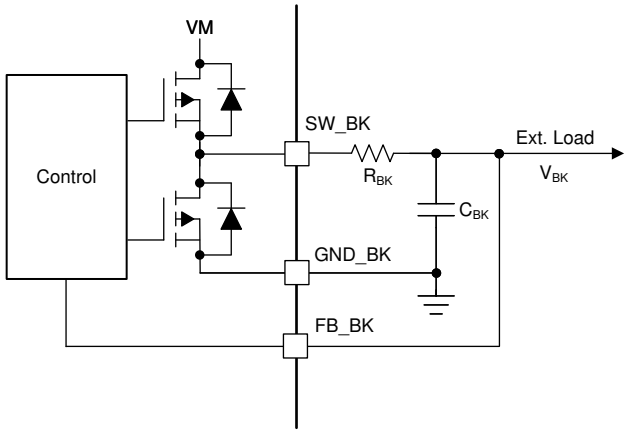

図 8-11. Buck (Resistor Mode)

8.3.4.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to fed to external LDO to generate standard 3.3 V or 5.0 V output rail with higher accuracies. The buck output voltage should be configured to 4 V or 5.5 V to provide for a extra headroom to support the external LDO for generating 3.3 V or 5 V rail as shown in 図 8-12.

This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

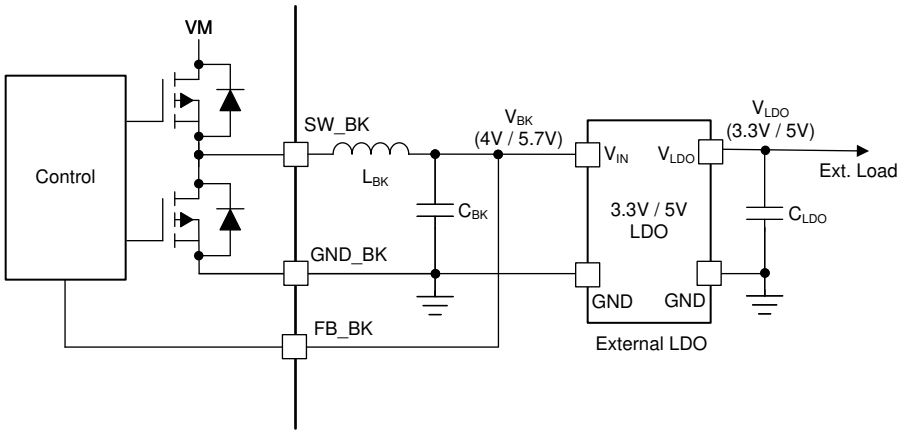

図 8-12. Buck Regulator with External LDO

8.3.4.4 AVDD Power Sequencing on Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce power dissipation internally. The power sequencing mode allows on-the-fly changeover of LDO power supply from DC mains (VM) to buck output (VBK) as shown in 図 8-13. This sequencing can be configured through the BUCK_PS_DIS bit. Power sequencing is supported only when buck output voltage is set to 5.0 V or 5.7 V.

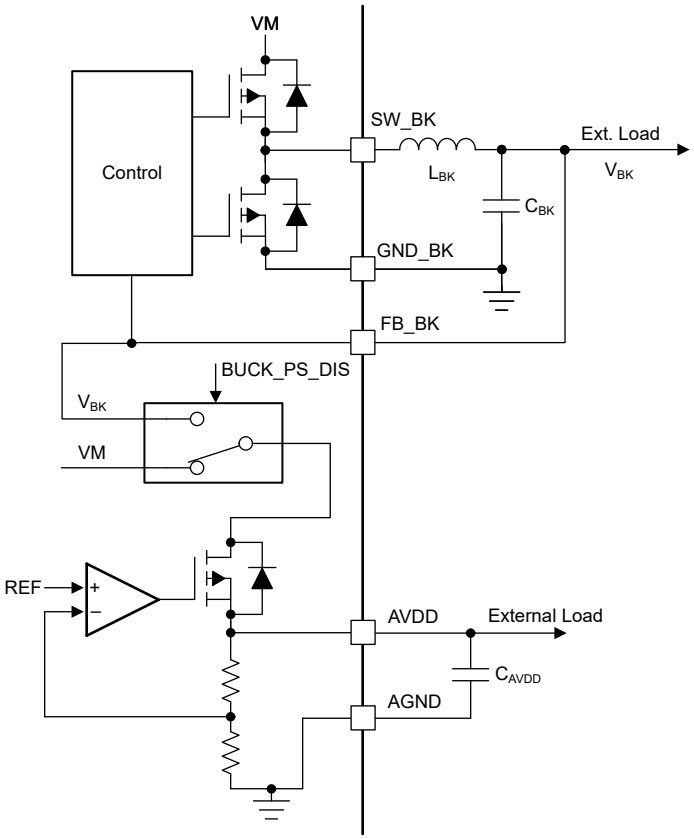

図 8-13. AVDD Power Sequencing on mixed mode Buck Regulator

8.3.4.5 Mixed mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and turna off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. 図 8-14 shows the architecture of the buck and various control/protection loops.

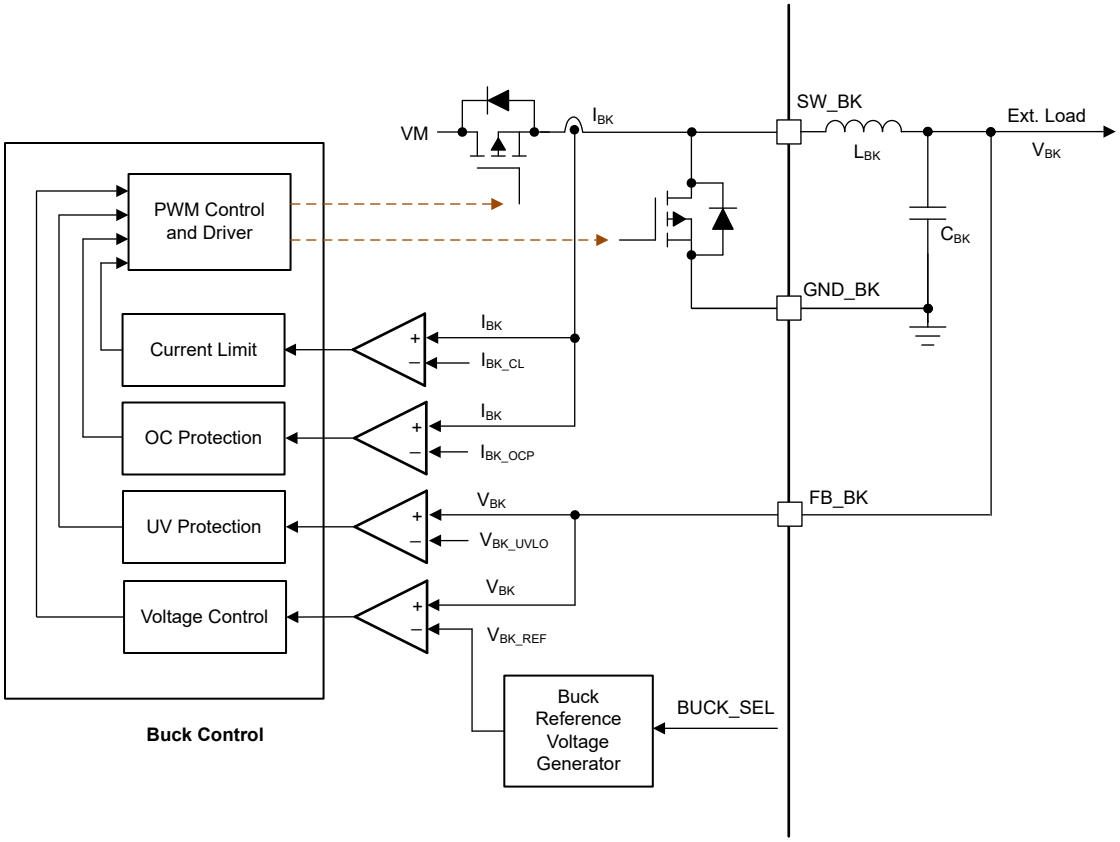

図 8-14. Buck Operation and Control Loops

8.3.5 AVDD Linear Voltage Regulator

A 3.3-V linear regulator is integrated into the MCT8315Z family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30 mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3 V.

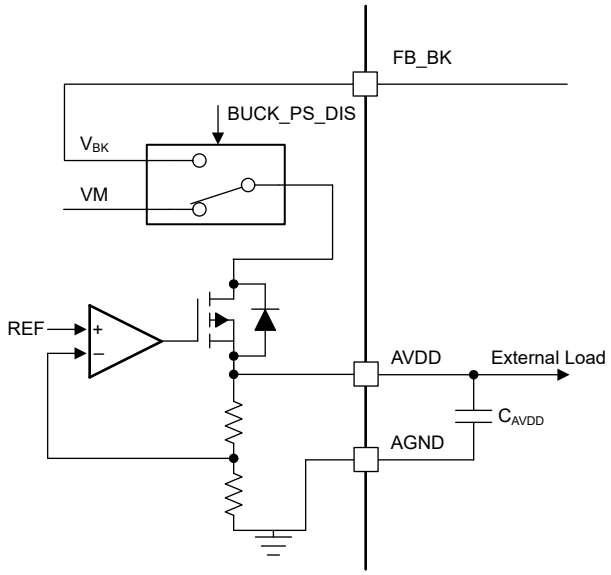

図 8-15. AVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PS_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in a LDO power dissipation as shown in 式 2.

$$P_{LDO} = (V_{VM} - V_{AVDD}) \times I_{AVDD} = (24 - 3.3)V \times 20mA = 414mW \quad (2)$$

Use 式 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PS_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

For example, at a V_{FB_BK} of 5 V, drawing 20 mA out of AVDD results in a LDO power dissipation as shown in 式 4.

$$P_{LDO} = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} = (5 - 3.3)V \times 20mA = 34mW \quad (4)$$

8.3.6 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The MCT8315Z integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See 図 8-1, 図 8-2, 図 8-3, セクション 6 and セクション 8.3 for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low.

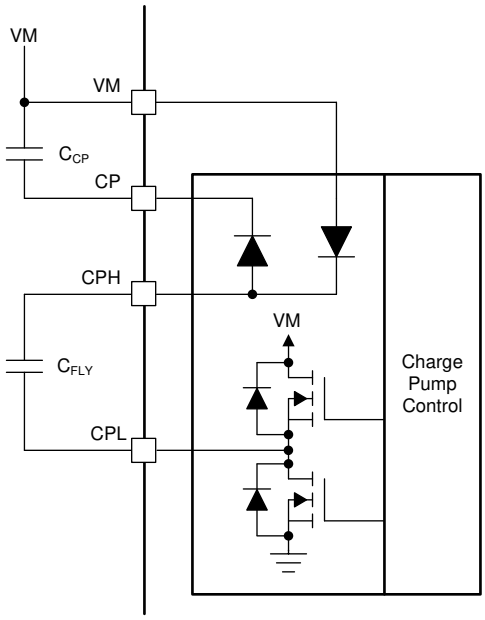

図 8-16. MCT8315Z Charge Pump

8.3.7 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in 図 8-17.

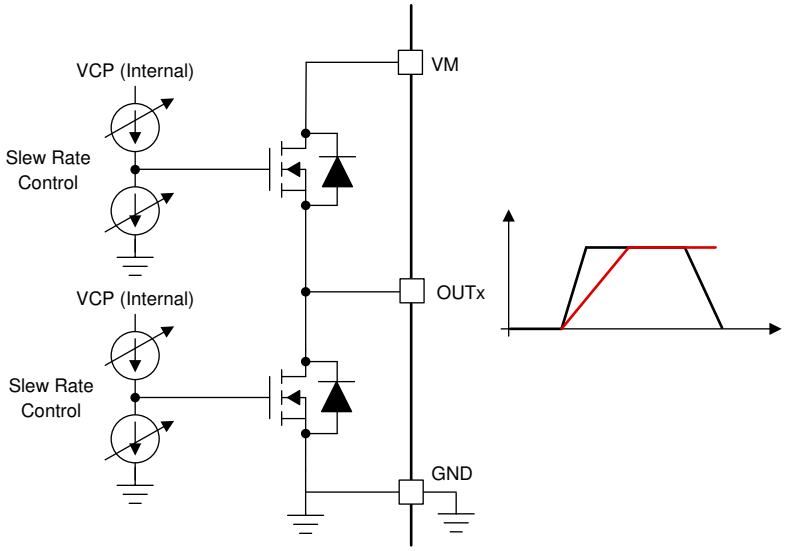

図 8-17. Slew Rate Circuit Implementation

The slew rate can be adjusted by the SLEW pin in hardware variant or by using the SLEW bits in SPI variant. Four slew rate settings are available : 25-V/µs, 50-V/µs, 125-V/µs or 200-V/µs. The slew rate is calculated by the rise time and fall time of the voltage on OUTx pin as shown in 図 8-18.

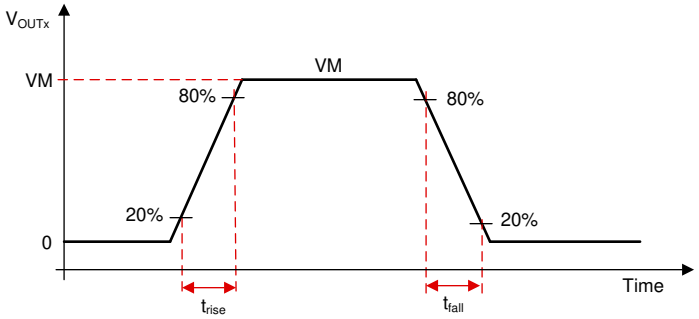

図 8-18. Slew Rate Timings

8.3.8 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, MCT8315Z avoids shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge (or vice-versa) as shown in 図 8-19 and 図 8-20.

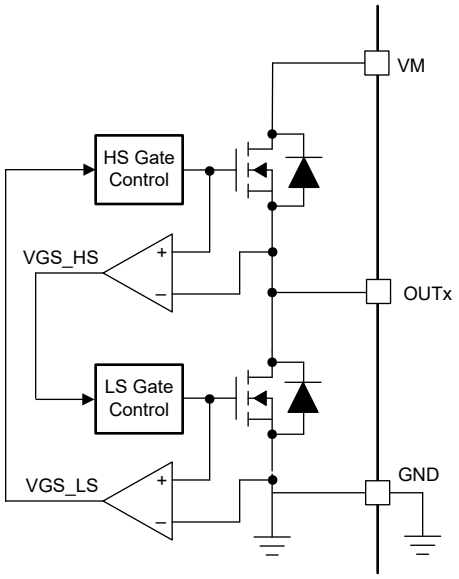

図 8-19. Cross Conduction Protection

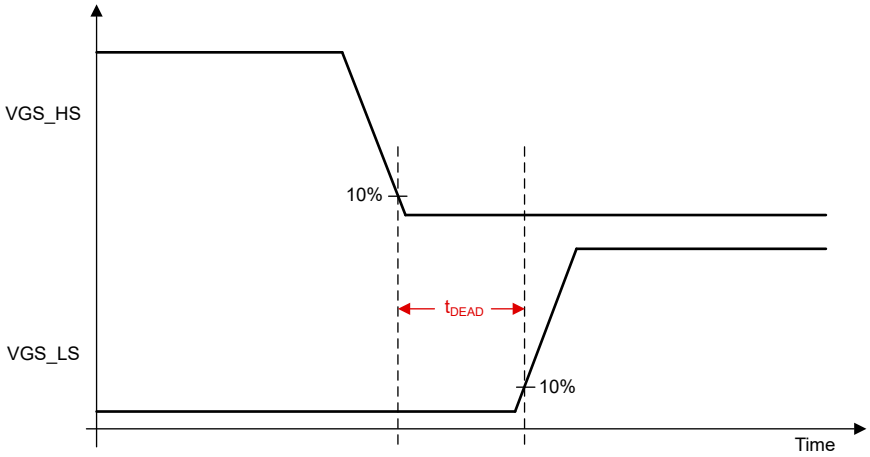

図 8-20. Dead Time

8.3.9 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage. This time has three parts consisting of the digital input deglitcher delay, analog driver, and comparator delay.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

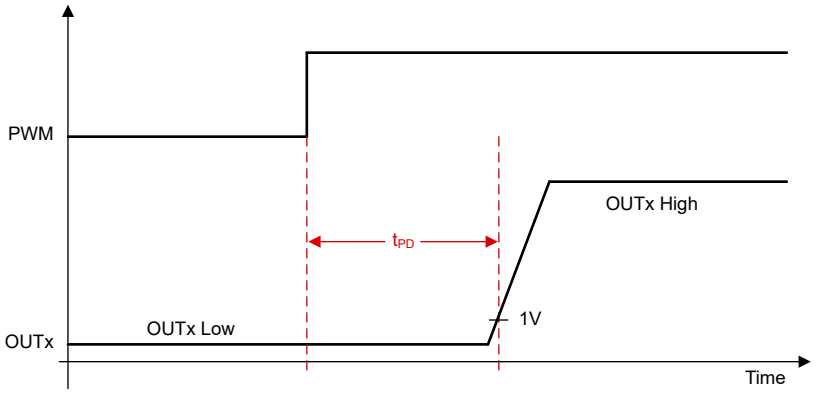

図 8-21. Propagation Delay Timing

8.3.9.1 Driver Delay Compensation

MCT8315Z monitors the propagation delay internally and adds a variable delay on top of it to provide fixed delay as shown in 図 8-22 and 図 8-23. Delay compensation feature reduces uncertainty caused in timing of current measurement and also reduces duty cycle distortion caused due to propagation delay.

The fixed delay is summation of propagation delay (t_{PD}) caused to internal driver delay and variable delay (t_{VAR}) added to compensate for uncertainty. The fixed delay can be configured through DLY_TARGET register. Refer 表 8-6 for recommendation on configuration for DLY_TARGET for different slew rate settings.

Delay compensation is only available in SPI variant MCT8315Z and can be enabled by configuring DLYCMP_EN and DLY_TARGET. It is disabled in hardware variant MCT8315Z.

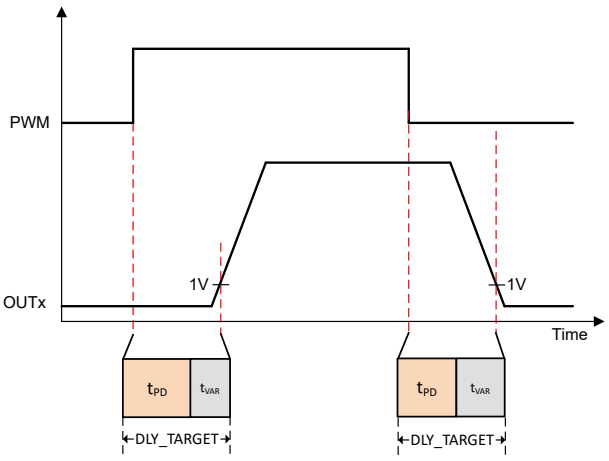

図 8-22. Delay Compensation with current flowing out of phase

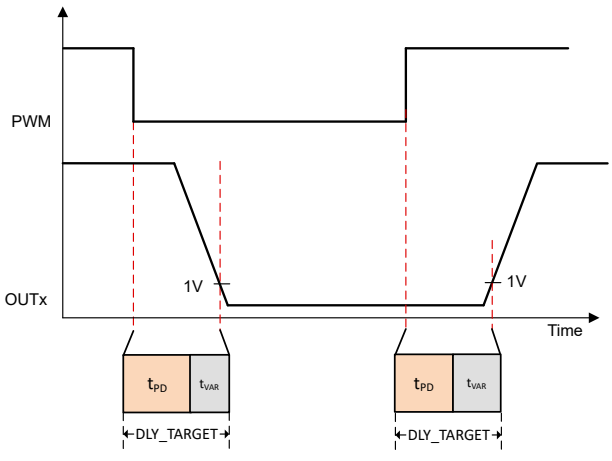

図 8-23. Delay Compensation with current flowing into the phase

表 8-6. Delay Target Recommendation

SLEW RATE	DLY_TARGET
200 V/µs	DLY_TARGET = 0x5 (1.2 µs)
125 V/µs	DLY_TARGET = 0x8 (1.8 µs)
50 V/µs	DLY_TARGET = 0xB (2.4 µs)
25 V/µs	DLY_TARGET = 0xF (3.2 µs)

8.3.10 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

8.3.10.1 Logic Level Input Pin (Internal Pulldown)

図 8-24 shows the input structure for the logic level pins, BRAKE, DIR, DRVOFF, nSLEEP, PWM, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

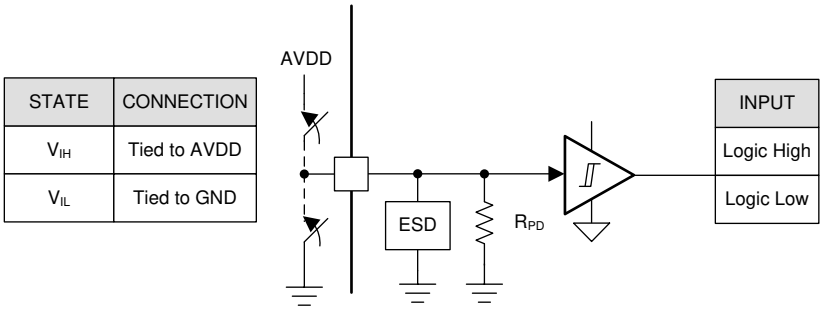

図 8-24. Logic-Level Input Pin Structure

8.3.10.2 Logic Level Input Pin (Internal Pullup)

図 8-25 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

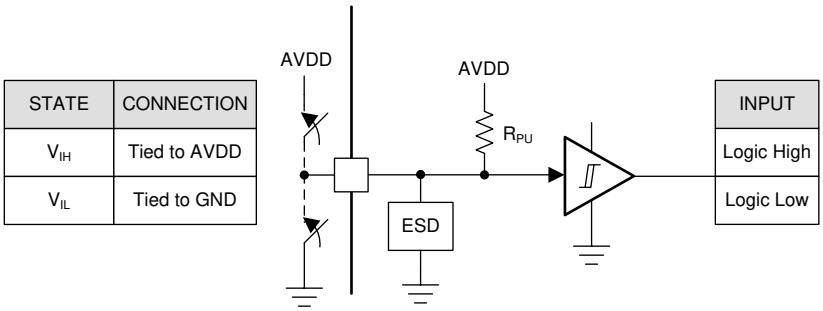

図 8-25. Logic nSCC

8.3.10.3 Open Drain Pin

図 8-26 shows the structure of the open-drain output pins, nFAULT, FGOUT and SDO in open drain mode. The open-drain output requires an external pullup resistor to function properly.図 8-26 also shows the status table of nFAULT pin during different device state.

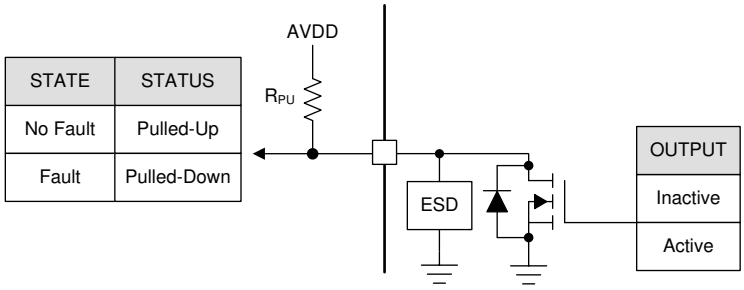

図 8-26. Open Drain

8.3.10.4 Push Pull Pin

図 8-27 shows the structure of SDO in push-pull mode.

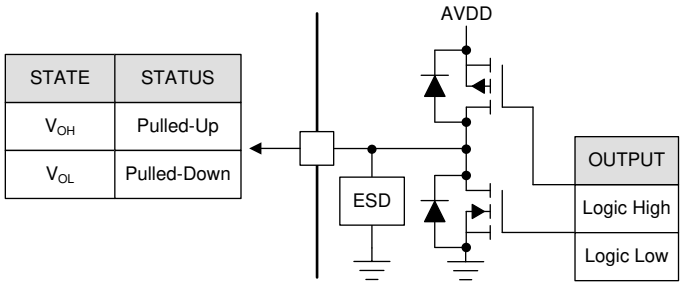

図 8-27. Push Pull

8.3.10.5 Four Level Input Pin

図 8-28 shows the structure of the four level input pin, SLEW on hardware interface devices. The input can be set with an external resistor.

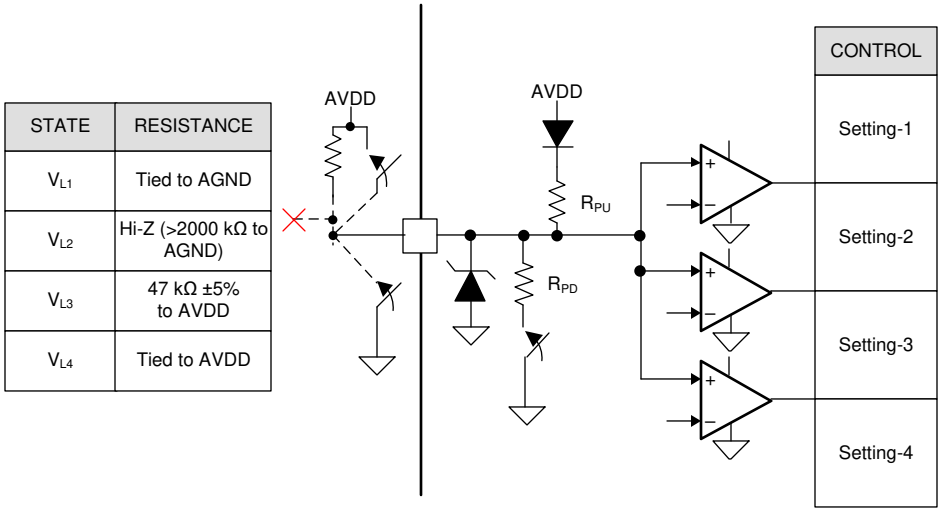

図 8-28. Four Level Input Pin Structure

8.3.10.6 Seven Level Input Pin

図 8-29 shows the structure of the seven level input pins, ADVANCE and MODE, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{L1}	Tied to AGND
V_{L2}	22 kΩ ± 5% to AGND
V_{L3}	100 kΩ ± 5% to AGND
V_{L4}	Hi-Z (>2000 kΩ to AGND)
V_{L5}	100 kΩ ± 5% to AVDD
V_{L6}	22 kΩ ±5% to AVDD
V_{L7}	Tied to AVDD

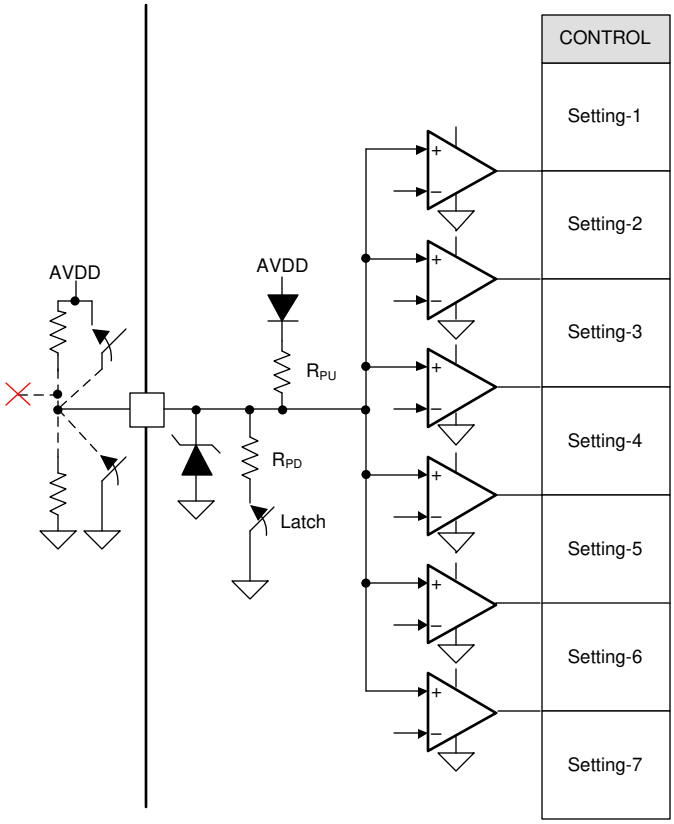

図 8-29. Seven Level Input Pin Structure

8.3.11 Active Demagnetization

MCT8315Z family of devices has smart rectification features (active demagnetization) which decreases power losses in the device by reducing diode conduction losses. When this feature is enabled, the device automatically turns ON the corresponding MOSFET whenever it detects diode conduction. This feature can be configured with the MODE pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in sections below.

注

In SPI device variants both bits, EN_ASR and EN_AAR needs to set to 1 to enable active demagnetization.

The MCT8315Z device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS comparator compares with the ground (0-V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization feature.

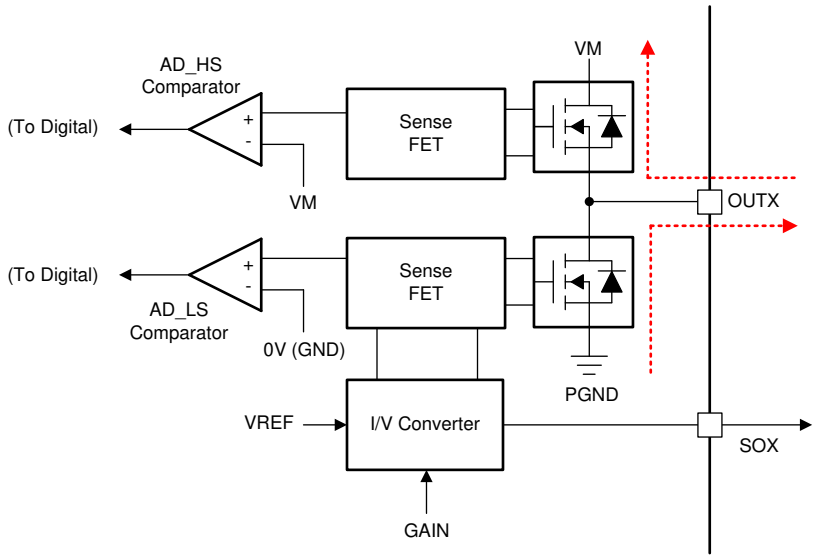

図 8-30. Active Demagnetization Operation

表 8-7 shows the configuration of ASR and AAR mode in theMCT8315Z device.

表 8-7. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	ASR and AAR configuration	Hall Configuration	Modulation	ASR and AAR Mode
Mode 1	Connected to AGND	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Asynchronous	ASR and AAR Disabled
Mode 2	Connected to AGND with R_{MODE1}	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Asynchronous	ASR and AAR Disabled
Mode 3	Connected to AGND with R_{MODE2}	EN_ASR = 0, EN_AAR = 0	Analog Hall Input	Synchronous	ASR and AAR Disabled
Mode 4	Hi-Z	EN_ASR = 0, EN_AAR = 0	Digital Hall Input	Synchronous	ASR and AAR Disabled
Mode 5	Connected to AVDD with R_{MODE2}	EN_ASR = 1, EN_AAR = 1	Analog Hall Input	Synchronous	ASR and AAR Enabled

表 8-7. PWM_MODE Configuration (続き)

MODE Type	MODE Pin (Hardware Variant)	ASR and AAR configuration	Hall Configuration	Modulation	ASR and AAR Mode
Mode 6	Connected to AVDD with R_{MODE1}	EN_ASR = 1, EN_AAR = 1	Digital Hall Input	Synchronous	ASR and AAR Enabled
Mode 7	Connected to AVDD				

8.3.11.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

8.3.11.1.1 Automatic Synchronous Rectification in Commutation

図 8-31 shows the operation of active demagnetization during the BLDC motor commutation. As shown in 図 8-31 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in 図 8-31 (b), the HC switch is turned on, whereas the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in 図 8-31 (c).

Similarly the operation of high-side FET is realized in 図 8-31 (d), (e) and (f).

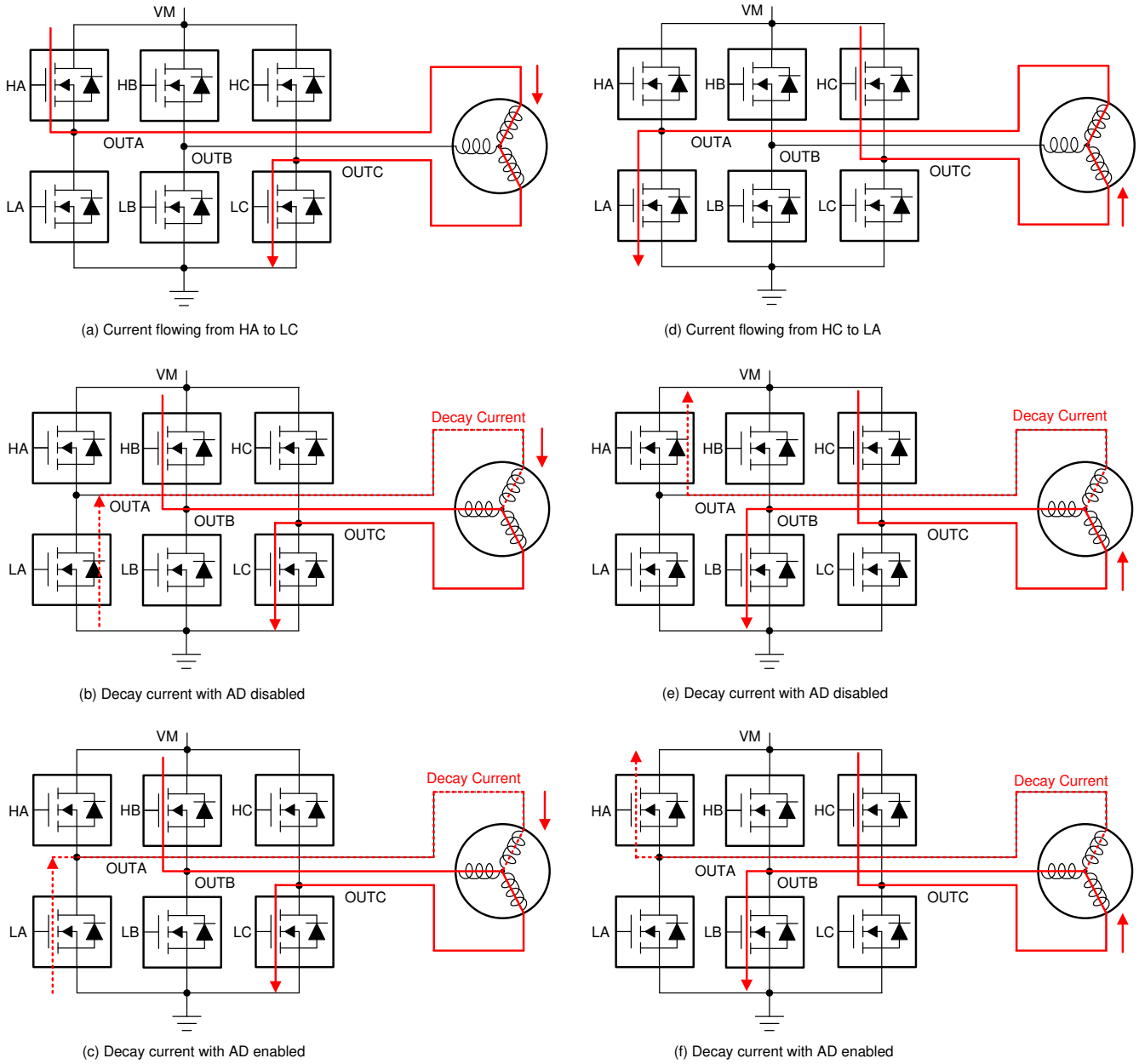

図 8-31. ASR in BLDC Motor Commutation

図 8-32 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

図 8-32 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demagnetization comparator threshold and delays.

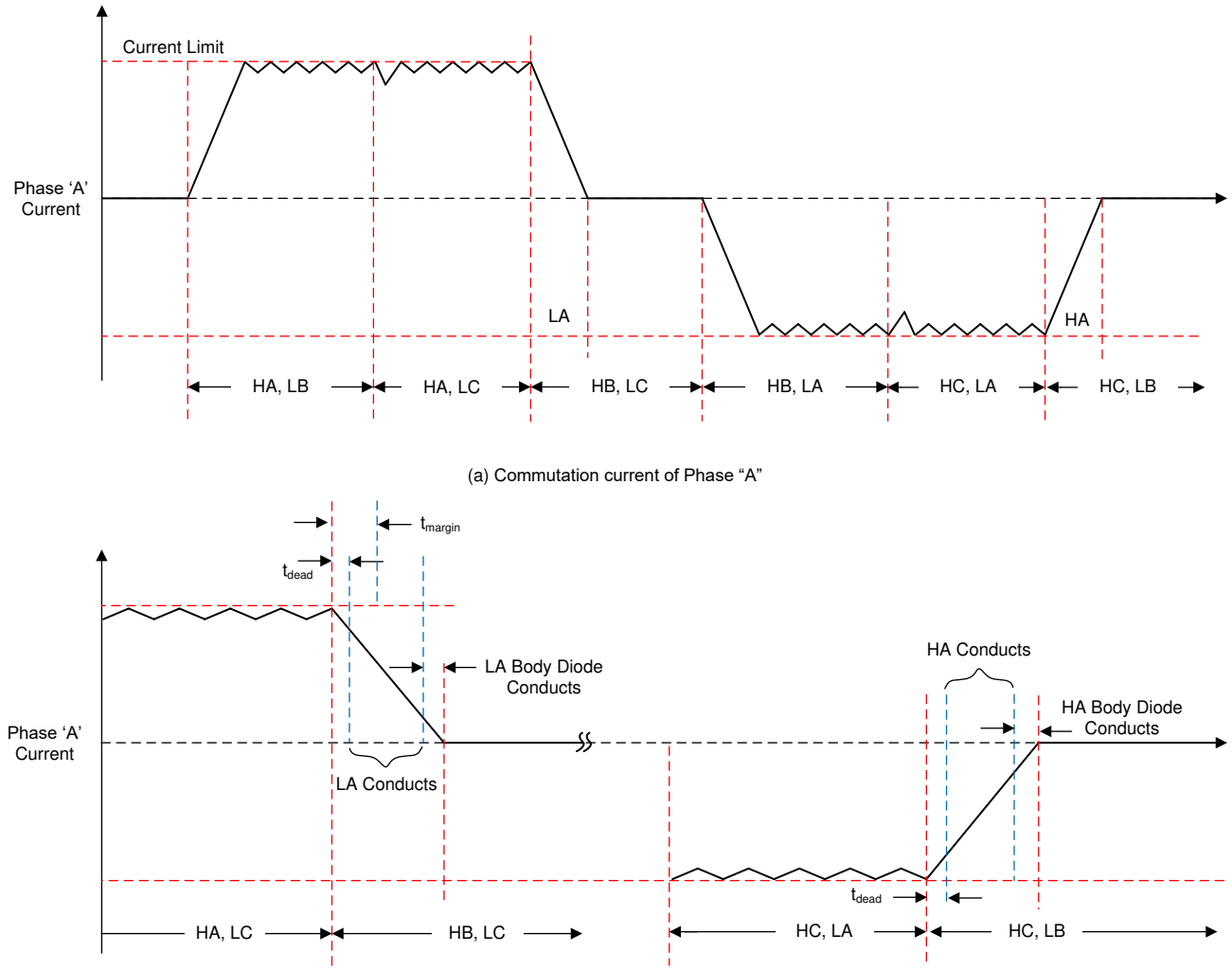

図 8-32. Current Waveforms for ASR in BLDC Motor Commutation

8.3.11.1.2 Automatic Synchronous Rectification in PWM Mode

図 8-33 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

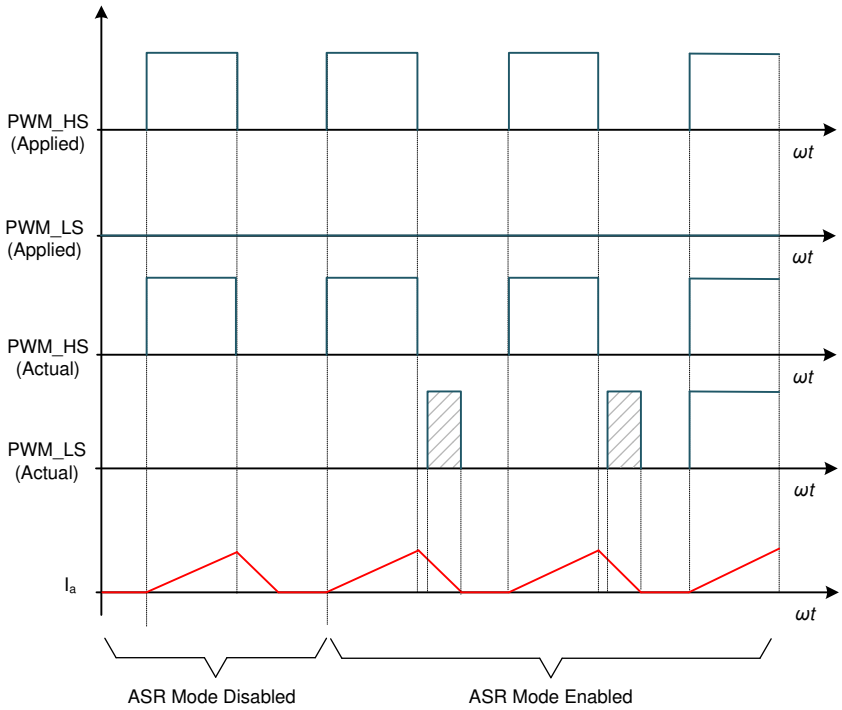

図 8-33. ASR in PWM Mode

8.3.11.2 Automatic Asynchronous Rectification Mode (AAR Mode)

図 8-34 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

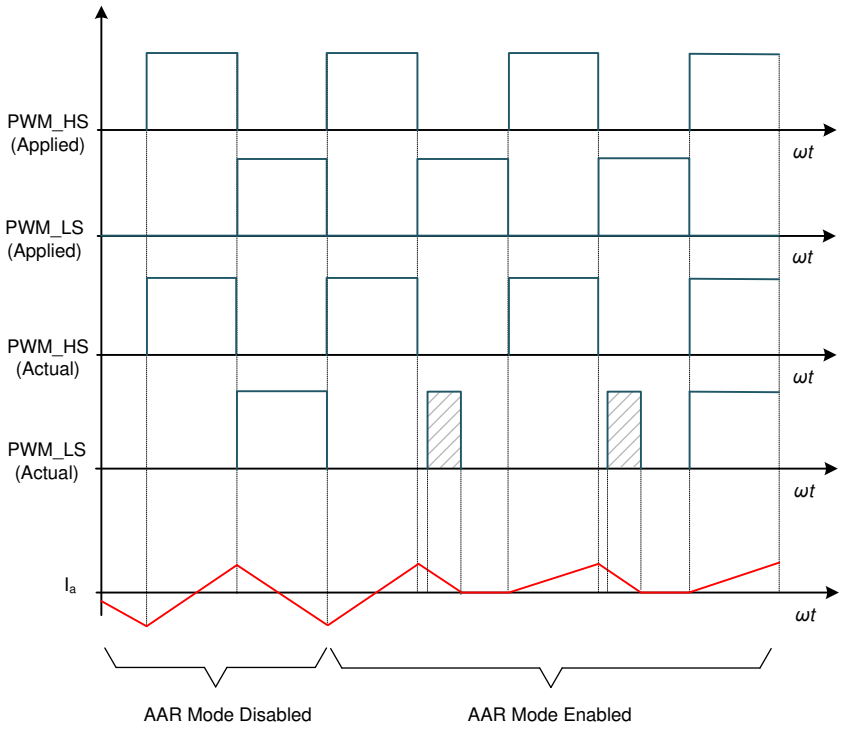

図 8-34. AAR in PWM Mode

8.3.12 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFET exceeds the I_{LIMIT} current. This feature restricts motor current to less than the I_{LIMIT}.

The current-limit circuitry utilizes the current sense amplifier output of the three phases and compares that voltage with the voltage at ILIM pin. 図 8-35 shows the implementation of current limit circuitry. As shown in this figure, the output of current sense amplifiers is combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage V_{ILIM} applied at ILIM pin to realize the current limit implementation. The relation between current sensed on OUTX pin and V_{MEAS} threshold is given as:

$$V_{MEAS} = \left({}^{V_{AVDD}}/_{2}\right) - \left((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3\right) \quad (5)$$

where

- AVDD is 3.3-V LDO output
- OUTX is current flowing into the low-side MOSFET
- GAIN is 0.24-V/A

The I_{LIMIT} threshold can be adjusted by configuring ILIM pin between AVDD/2 to (AVDD/2 - 0.32) V. AVDD/2 is minimum value and when it is applied on ILIM pin cycle by cycle current limit is disabled, whereas maximum threshold of 4-A can be configured by applying (AVDD/2 - 0.32) V on ILIM pin.

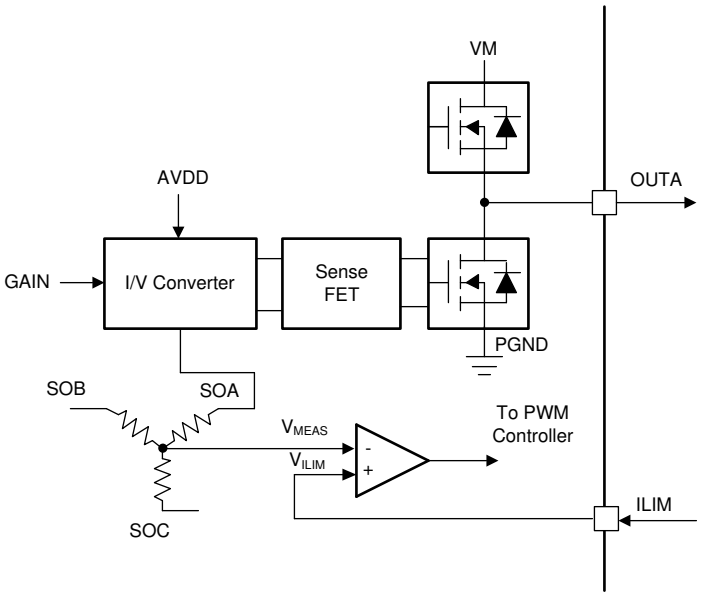

図 8-35. Current Limit Implementation

When the current limit threshold is hit, the high-side FET is disabled until the beginning of the next PWM cycle as shown in 図 8-36. The low-side FETs can operate in brake mode or Hi-Z mode by configuring the ILIM_RECIR bit in the SPI device variant.

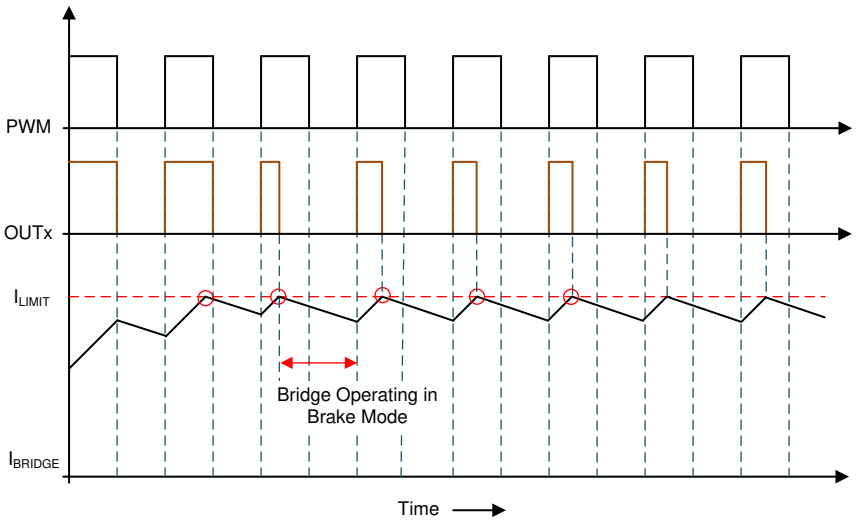

図 8-36. Cycle-by-Cycle Current-Limit Operation

In the MCT8315Z device, when the current limit activates in synchronous rectification mode, the current recirculates through the low-side FETs while the high-side FETs are disabled as shown in 図 8-37

Moreover, when the current limit activates in asynchronous rectification mode, the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled as shown in 図 8-38

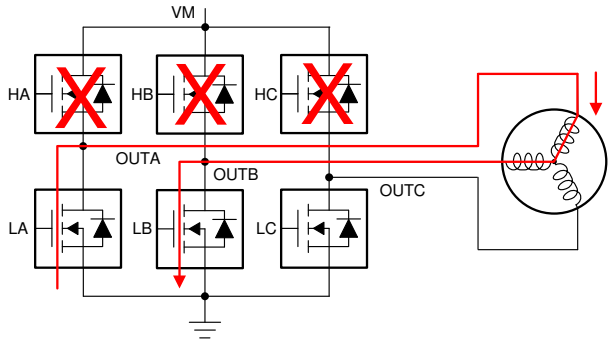

図 8-37. Brake State

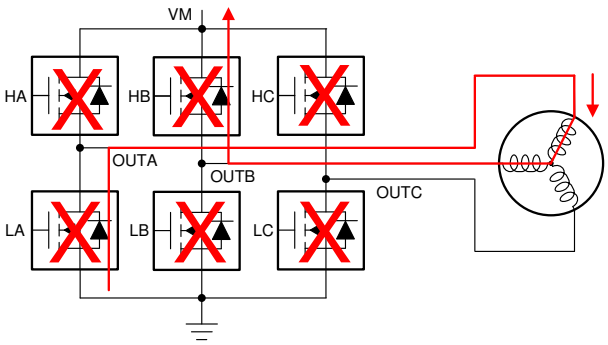

図 8-38. Coast State

注

The current-limit circuit is ignored immediately after the PWM signal goes active for a short blanking time to prevent false trips of the current-limit circuit.

注

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

8.3.12.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, MCT8315Z has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant MCT8315Z, this internal PWM clock can be configured to either 20 kHz or 40 kHz through PWM_100_DUTY_SEL. In HW variants, MCT8315Z PWM internal clock is set to 20 kHz. 図 8-39 shows operation with 100 % duty cycle.

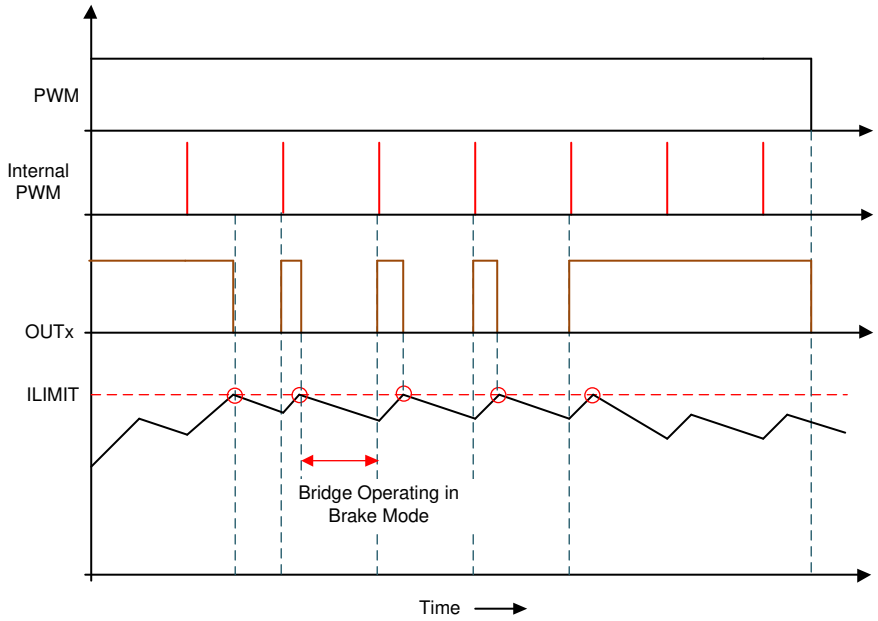

図 8-39. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

8.3.13 Hall Comparators (Analog Hall Inputs)

Three comparators are provided to process the raw signals from the Hall-effect sensors to commutate the motor. The Hall comparators sense the zero crossings of the differential inputs and pass the information to digital logic. The Hall comparators have hysteresis, and their detect threshold is centered at 0-V. The hysteresis is defined as shown in 図 8-40.

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of t_{HDG} after sensing a valid transition. Ignoring these transitions for the t_{HDG} time prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, adding capacitors between the positive and negative inputs of the Hall comparators may be required. The ESD protection circuitry on the Hall inputs implements a diode to the AVDD pin. Because of this diode, the voltage on the Hall inputs should not exceed the AVDD voltage.

Because the AVDD pin is disabled in sleep mode (nSLEEP inactive), the Hall inputs should not be driven by external voltages in sleep mode. If the Hall sensors are powered externally, the supply to the Hall sensors should be disabled if the MCT8315Z device is put into sleep mode. In addition, the Hall sensors' power supply should be powered up after enabling the motor otherwise an invalid Hall state may cause a delay in motor operation.

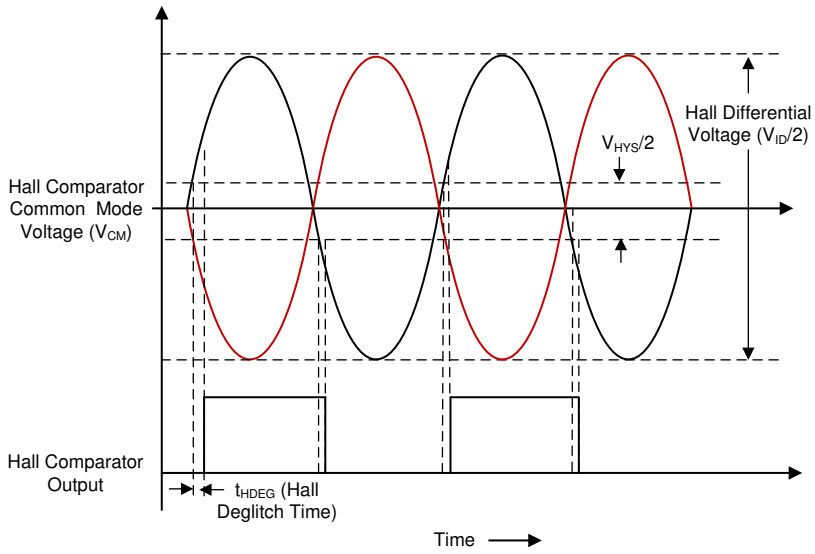

図 8-40. Hall Comparators Operation

8.3.14 Advance Angle

The MCT8315Z includes an advance angle feature to advance the commutation by a specified electrical angle based on the voltage on the ADVANCE pin (in HW device variant) or the ADVANCE_LVL bits (in SPI variant). 図 8-41 shows the operation of advance angle feature.

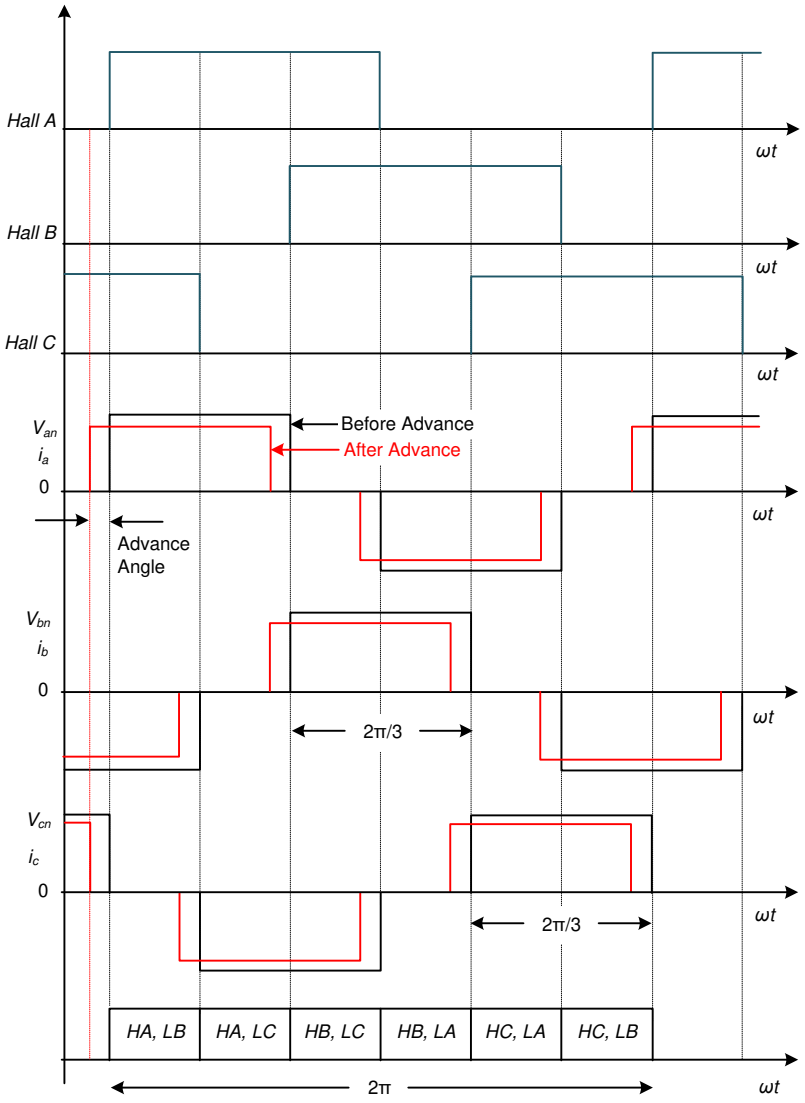

図 8-41. Advance Angle

8.3.15 FGOUT Signal

The MCT8315Z device also has an open-drain FGOUT signal that can be used for closed-loop speed control of a BLDC motor. This signal includes the information of all three Hall-elements inputs as shown in 図 8-42. In the MCT8315ZR (SPI variant), FGOUT can be configured to be a different division factor of Hall signals as shown in 図 8-42. In the MCT8315ZH/T (hardware variant), the default mode is FGOUT_SEL = 00b.

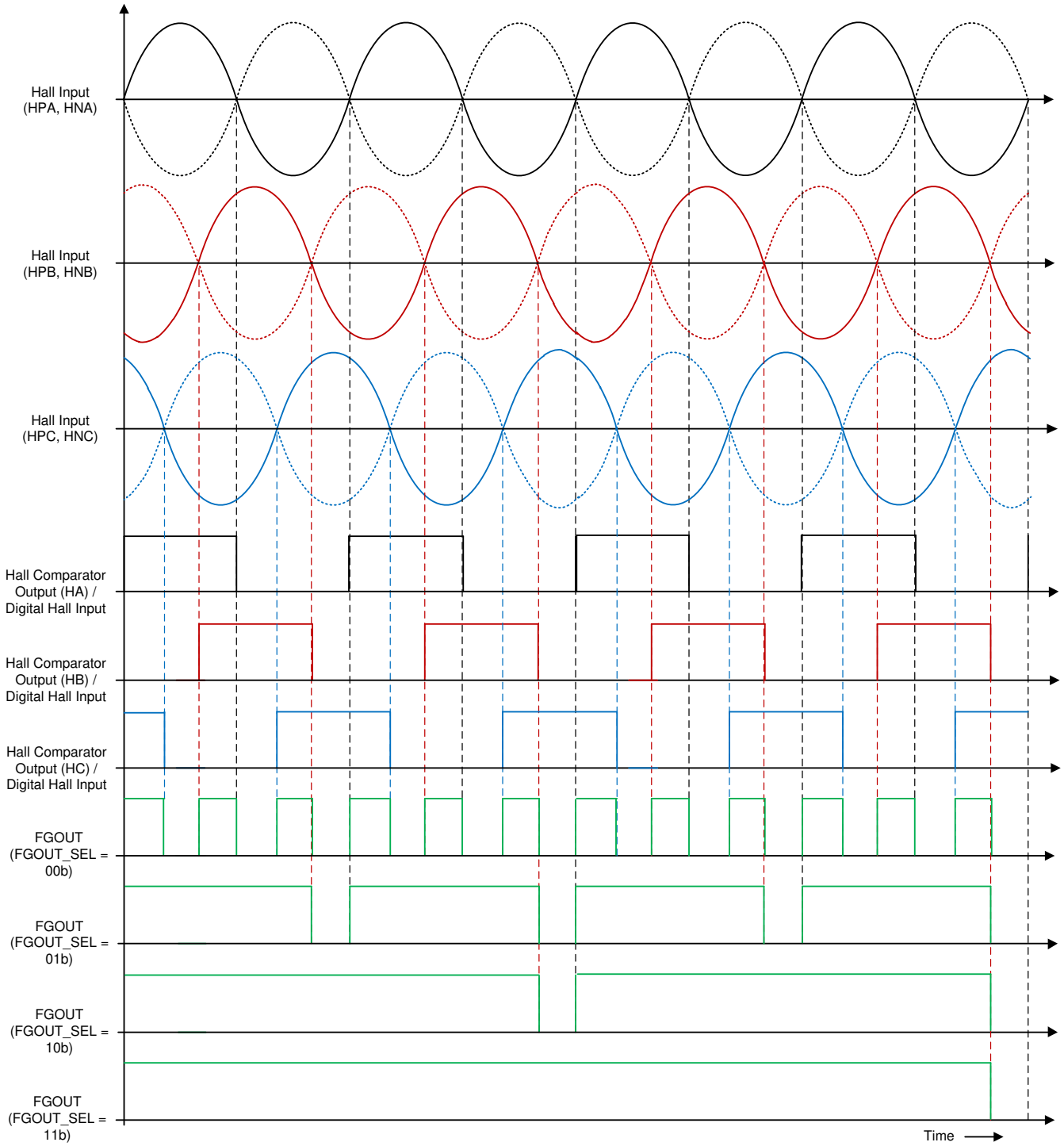

図 8-42. FGOUT Signal

8.3.16 Protections

The MCT8315Z devices are protected against VM, AVDD, charge pump and buck undervoltage, VM overvoltage, buck and FET overcurrent, motor lock, SPI and OTP error and over temperature events. 表 8-8 summarizes various faults details.

表 8-8. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	LOGIC	RECOVERY
VM undervoltage (NPOR)	V_{VM} < V_{UVLO} (falling)	—	—	Hi-Z	Disabled	Automatic: V_{VM} > V_{UVLO} (rising) CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
AVDD undervoltage (NPOR)	V_{AVDD} < V_{AVDD_UV} (falling)	—	—	Hi-Z	Disabled	Automatic: V_{AVDD} > V_{AVDD_UV} (rising) CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
Buck undervoltage (BUCK_UV)	V_{FB_BK} < V_{BK_UV} (falling)	—	nFAULT	Active	Active	Automatic: V_{FB_BK} > V_{BUCK_UV} (rising) CLR_FLT, nSLEEP Reset Pulse (BUCK_UV bit)
Charge pump undervoltage (VCP_UV)	V_{CP} < V_{CPUV} (falling)	—	nFAULT	Hi-Z	Active	Automatic: V_{VCP} > V_{CPUV} (rising) CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
Overvoltage Protection (OVP)	V_{VM} > V_{OVP} (rising)	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b	nFAULT	Hi-Z	Active	Automatic: V_{VM} < V_{OVP} (falling) CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	I_{PHASE} > I_{OCP}	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
Buck Overcurrent Protection (BUCK_OCP)	I_{BK} > I_{BK_OCP}	—	nFAULT	Active	Active	Retry: t_{BK_RETRY}
SPI Error (SPI_FLT)	SCLK fault and ADDR fault	SPI_FLT_REP = 0b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
		SPI_FLT_REP = 1b	None	Active	Active	No action
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, nSLEEP Reset Pulse
Motor Lock (MTR_LOCK)	No hall signals > $t_{MTR\_LOCK\_TDET}$	MTR_LOCK_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Pulse (MTR_LOCK bit)
		MTR_LOCK_MODE = 01b	nFAULT	Hi-Z	Active	Retry: $t_{MTR\_LOCK\_RETRY}$
		MTR_LOCK_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		MTR_LOCK_MODE = 11b	None	Active	Active	No action
Thermal warning (OTW)	T_J > T_{OTW}	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: T_J < T_{OTW} – T_{OTW_HYS} CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (TSD)	T_J > T_{TSD}	—	nFAULT	Hi-Z	Active	Automatic: T_J < T_{TSD} – T_{TSD_HYS}
Thermal shutdown (TSD_FET)	T_J > T_{TSD_FET}	—	nFAULT	Hi-Z	Active	Automatic: T_J < T_{TSD_FET} – $T_{TSD\_FET\_HYS}$ CLR_FLT, nSLEEP Pulse (OTS bit)

8.3.16.1 VM Supply Undervoltage Lockout (NPOR)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in 図 8-43. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

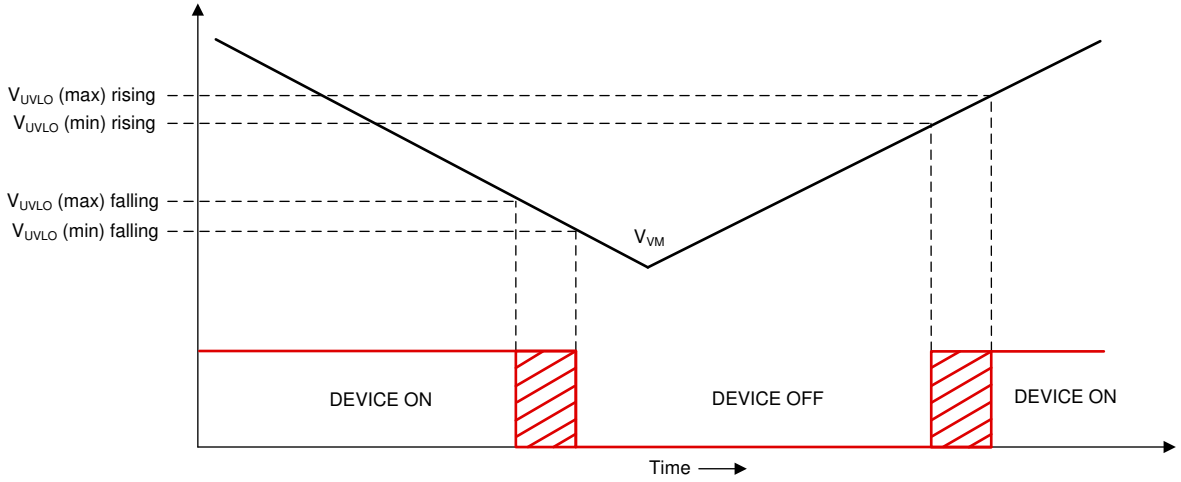

図 8-43. VM Supply Undervoltage Lockout

8.3.16.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.16.3 Buck Undervoltage Lockout (BUCK_UV)

If at any time the voltage on VFB_BK pin falls lower than the V_{BK_UV} threshold, the nFAULT pin is driven low and the BK_FLT bit in IC_STAT register is set while the driver FETs, charge pump, and digital logic control continue to operate normally. The FAULT and BUCK_UV bits are also latched high in the status registers. Normal operation starts again (buck regulator operation and the nFAULT pin is released) when the buck undervoltage condition clears. The BK_FLT and BUCK_UV bits stay set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.16.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and VCP_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

8.3.16.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and OVP bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin

reset pulse (t_{RST}). Setting the OVP_EN bit high on the SPI devices enables this protection feature. The OVP threshold is programmable on the SPI variant and can be set to 22-V or 34-V based on the OVP_SEL bit. In hardware variant, the OVP protection is always enabled and set to a 34-V threshold.

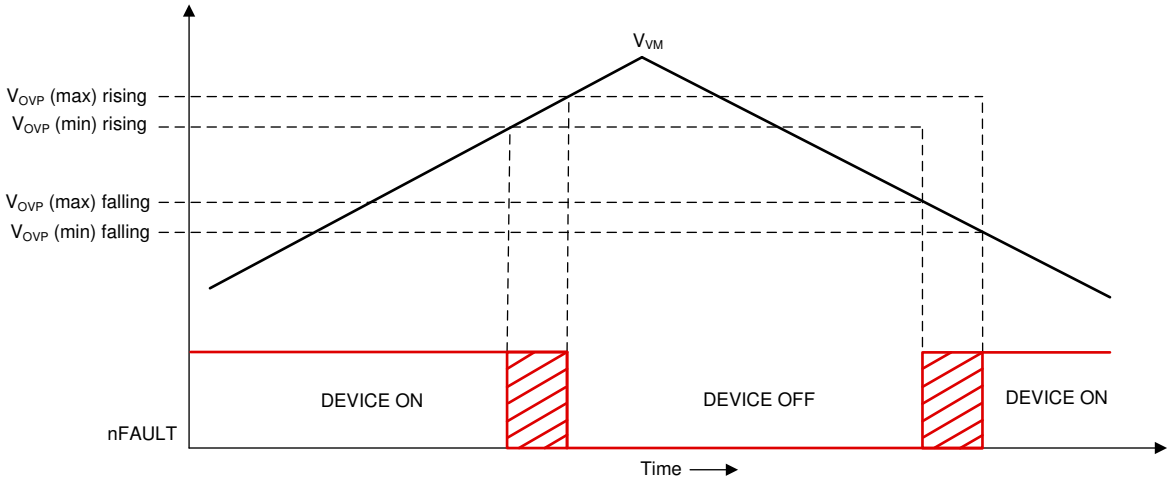

図 8-44. Over Voltage Protection

8.3.16.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is fixed at 9-A threshold, the t_{OCP_DEG} is fixed at 0.6-µs, and the OCP_MODE bit is configured for latched shutdown. On SPI devices, the I_{OCP} threshold is set through OCP_LVL, the t_{OCP_DEG} is set through the OCP_DEG, and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

8.3.16.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

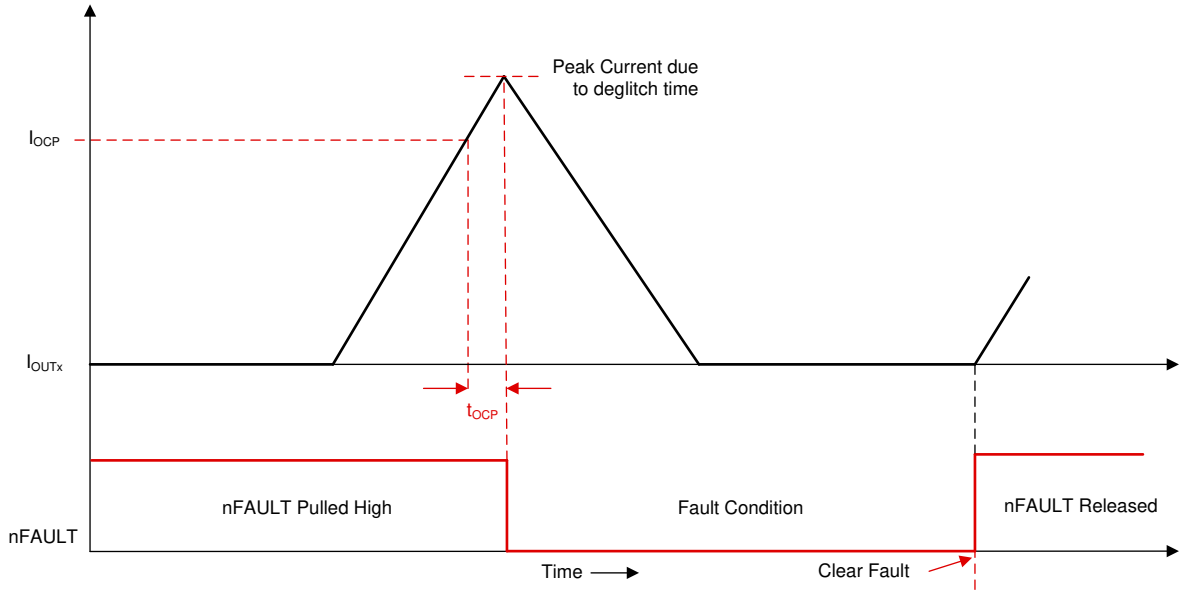

図 8-45. Overcurrent Protection - Latched Shutdown Mode

8.3.16.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

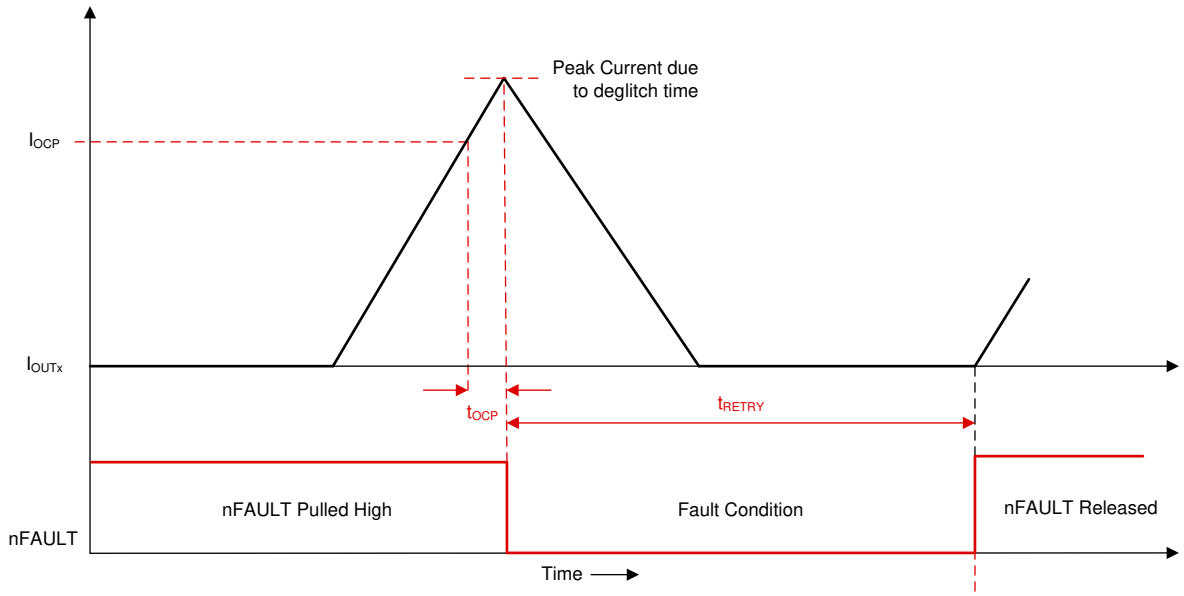

図 8-46. Overcurrent Protection - Automatic Retry Mode

8.3.16.7 Buck Overcurrent Protection

A buck overcurrent event is sensed by monitoring the current flowing through buck regulator's FETs. If the current across the buck regulator FET exceeds the I_{BK_OCP} threshold for longer than the t_{BK_OCP} deglitch time, an OCP event is recognized. The buck OCP mode is configured in automatic retry setting. In this setting, after

a buck OCP event is detected, all the buck regulator's FETs are disabled and the nFAULT pin is driven low. The FAULT, BK_FLT, and BUCK_OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{BK_RETRY} time elapses. The FAULT, BK_FLT, and BUCK_OCP bits stay latched until the t_{BK_RETRY} period expires.

8.3.16.8 Motor Lock (MTR_LOCK)

During motor is in lock condition the hall signals will be not available, so a Motor Lock event is sensed by monitoring the hall signals. If the hall signals are not present for for longer than the t_{MTR_LOCK}, a MTR_LCK event is recognized and action is done according to the MTR_LOCK_MODE bits. On hardware interface devices, the t_{MTR_LOCK} threshold is set to 1000-ms, and the MTR_LOCK_MODE bit is configured for latched shutdown. On SPI devices, the t_{MTR_LOCK} threshold is set through the MTR_LOCK_TDET register and the MTR_LOCK_MODE bit can operate in four different modes: MTR_LOCK latched shutdown, MTR_LOCK automatic retry, MTR_LOCK report only, and MTR_LOCK disabled.

8.3.16.8.1 MTR_LOCK Latched Shutdown (MTR_LOCK_MODE = 00b)

After a motor lock event in this mode, all FETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.16.8.2 MTR_LOCK Automatic Retry (MTR_LOCK_MODE = 01b)

After a motor lock event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the $t_{MTR\_LOCK\_RETRY}$ time elapses. The FAULT and MTR_LOCK bits stay latched until the $t_{MTR\_LOCK\_RETRY}$ period expires.

8.3.16.8.3 MTR_LOCK Report Only (MTR_LOCK_MODE= 10b)

No protective action occurs after a MTR_LOCK event in this mode. The motor lock event is reported by driving the nFAULT pin low and latching the FAULT and MTR_LOCK bits high in the SPI registers. The MCT8315Z continues to operate as usual. The external controller manages the motor lock condition by acting appropriately. The reporting clears (nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.16.8.4 MTR_LOCK Disabled (MTR_LOCK_MODE = 11b)

No action occurs after a MTR_LOCK event in this mode.

8.3.16.8.5

注

The motor lock detection scheme requires the PWM off-time (t_{PWM_OFF}) to be lower than the motor lock detection time (t_{MTR_LOCK})

8.3.16.9 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the IC status (IC_STAT) register and OTW bit in the status register is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW} - T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}).

8.3.16.10 Thermal Shutdown (OTSD)

MCT8315Z has 2 die temperature sensor for thermal shutdown, one of them near FETs and other one in other part of die.

8.3.16.10.1 OTSD FET

If the die temperature near FET exceeds the trip point of the thermal shutdown limit (T_{TSD_FET}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

8.3.16.10.2 OTSD (Non-FET)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the buck regulator disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Functional Modes

8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the MCT8315Z family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, current sense amplifiers are disabled, buck regulator (if present) is disabled, the charge pump is disabled, the AVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

注

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

注

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, make sure that it is pulled to >2.2 V on power up or the device will enter internal test mode.

8.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, AVDD regulator, buck regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the MCT8315Z family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT bit to 1b in the SPI variant or issuing a reset pulse to the nSLEEP pin on either variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall within the t_{RST} time window or else the device will start the complete shutdown sequence (low power sleep mode). The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

8.4.2 DRVOFF

MCT8315Z has capability to disable pre-driver and MOSFETs bypassing the digital through DRVOFF pin. When DRVOFF pin is pulled high, all six MOSFETs are disabled (Hi-Z). If nSLEEP is high when the DRVOFF pin is high, the charge pump, AVDD regulator, buck regulator, and SPI bus are active and any driver-related faults such as OCP will be inactive. DRVOFF pin independently disables MOSFETs which will stop motor commutation irrespective of status of PWM, HPx and HNx pins.

注

Since DRVOFF pin independently disables the MOSFETs bypassing digital logic, it can trigger fault detection resulting in nFAULT getting pulled low.

8.5 SPI Communication

8.5.1 Programming

On MCT8315Z SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in secondary mode and connects to a controller. The SPI input data (SDI) word consists of a 16-bit word, with a 6-bit address and 8 bits of data. The SPI output consists of 16 bit word, with a 8 bits of status information (STAT register) and 8-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

8.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 6 address bits, A (bits B14 through B9)
- Parity bit, P (bit B8). Parity bit is set such that the SDI input data word has even number of 1s and 0s
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits are status bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

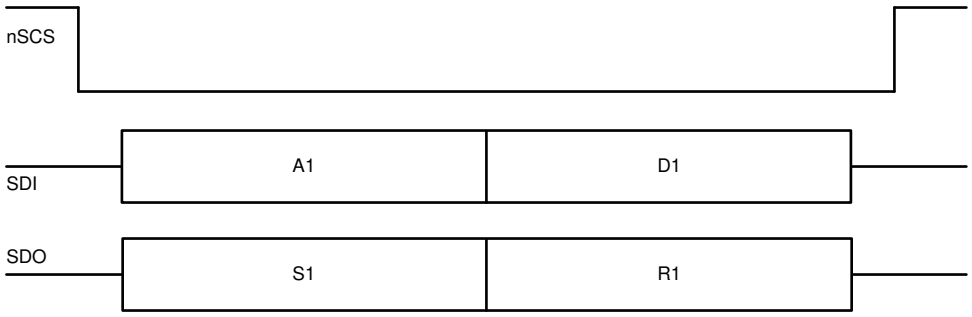

図 8-47.

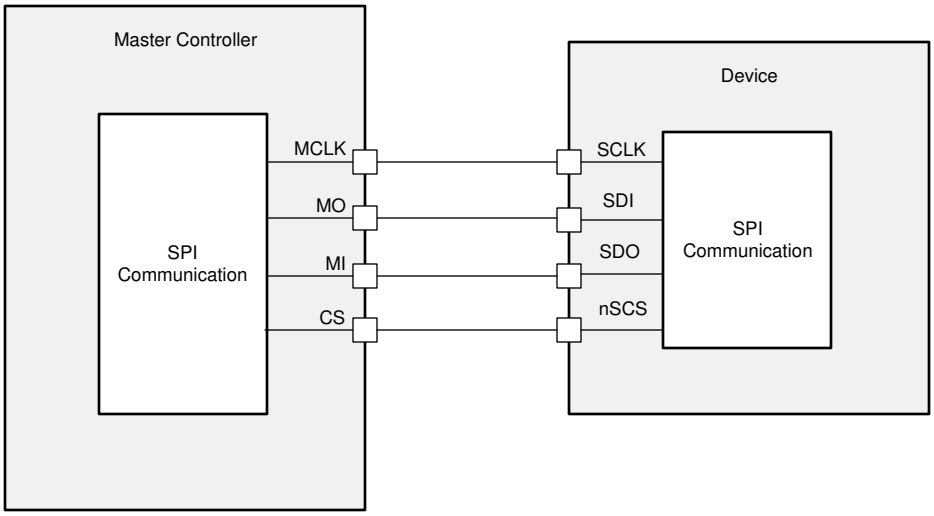

図 8-48.

表 8-9. SDI Input Data Word Format

R/W	ADDRESS						Parity	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A5	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0

表 8-10. SDO Output Data Word Format

STATUS								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0

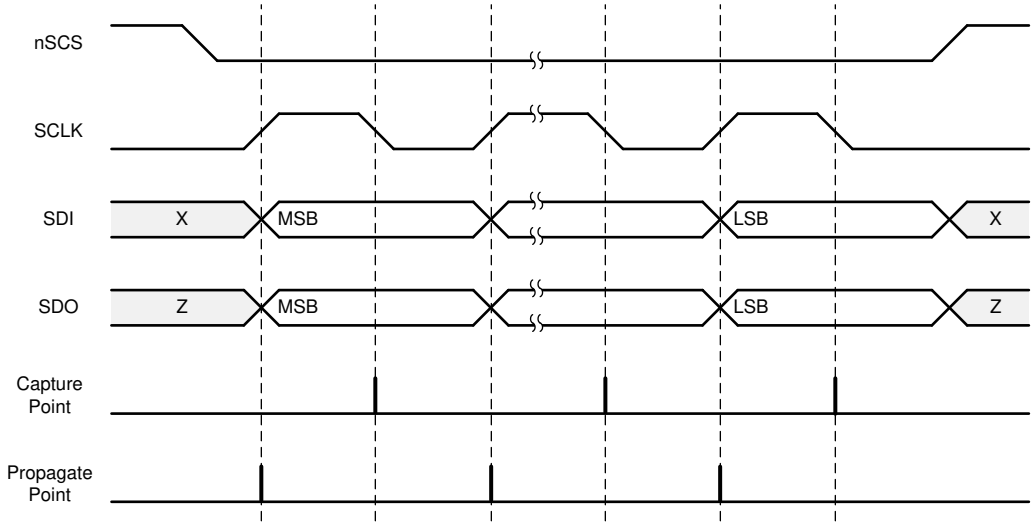

図 8-49. SPI Secondary Timing Diagram

SPI Error Handling

SPI Frame Error (SPI_SCLK_FLT: If the nSCS gets deasserted before the end of 16-bit frame, SPI frame error is detected and SPI_SCLK_FLT bit is set in STAT2. The SPI_SCLK_FLT status bit is latched and can be cleared when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse

SPI Address Error (SPI_ADDR_FLT): If an invalid address is provided in the ADDR field of the input SPI data on SDI, SPI address error is detected and SPI_ADDR_FLT bit in STAT2 is set. Invalid address is any address that is not defined in Register Map i.e. address not falling in the range of address 0x0 to 0xC. The SPI_ADDR_FLT status bit is latched and can be cleared when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse

8.6 Register Map

8.6.1 STATUS Registers

表 8-11 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in 表 8-11 should be considered as reserved locations and the register contents should not be modified.

表 8-11. STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC Status Register	IC Status Register	セクション 8.6.1.1
1h	Status Register 1	Status Register 1	セクション 8.6.1.2
2h	Status Register 2	Status Register 2	セクション 8.6.1.3

Complex bit access types are encoded to fit into small table cells. 表 8-12 shows the codes that are used for access types in this section.

表 8-12. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 IC Status Register (Offset = 0h) [Reset = 00h]

IC Status Register is shown in 表 8-13.

Return to the Summary Table.

表 8-13. IC Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MTR_LOCK	R	0h	Motor Lock Status Bit 0h = No motor lock is detected 1h = Motor lock is detected
6	BK_FLT	R	0h	Buck Fault Bit 0h = No buck regulator fault condition is detected 1h = Buck regulator fault condition is detected
5	SPI_FLT	R	0h	SPI Fault Bit 0h = No SPI fault condition is detected 1h = SPI Fault condition is detected
4	OCP	R	0h	Over Current Protection Status Bit 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
3	NPOR	R	0h	Supply Power On Reset Bit 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
2	OVP	R	0h	Supply Overvoltage Protection Status Bit 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
1	OT	R	0h	Overtemperature Fault Status Bit 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device Fault Bit 0h = No fault condition is detected 1h = Fault condition is detected

8.6.1.2 Status Register 1 (Offset = 1h) [Reset = 00h]

Status Register 1 is shown in 表 8-14.

Return to the Summary Table.

表 8-14. Status Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	OTW	R	0h	Overtemperature Warning Status Bit 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
6	OTS	R	0h	Overtemperature Shutdown Status Bit 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
5	OCP_HC	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
4	OCL_LC	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
3	OCP_HB	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
2	OCP_LB	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
1	OCP_HA	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
0	OCP_LA	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA

8.6.1.3 Status Register 2 (Offset = 2h) [Reset = 00h]

Status Register 2 is shown in 表 8-15.

Return to the Summary Table.

表 8-15. Status Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	OTP_ERR	R	0h	One Time Programmability Error 0h = No OTP error is detected 1h = OTP Error is detected
5	BUCK_OCP	R	0h	Buck Regulator Overcurrent Status Bit 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected
4	BUCK_UV	R	0h	Buck Regulator Undervoltage Status Bit 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
3	VCP_UV	R	0h	Charge Pump Undervoltage Status Bit 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
2	SPI_PARITY	R-0	0h	SPI Parity Error Bit 0h = No SPI parity error is detected 1h = SPI parity error is detected
1	SPI_SCLK_FLT	R	0h	SPI Clock Framing Error Bit 0h = No SPI clock framing error is detected 1h = SPI clock framing error is detected
0	SPI_ADDR_FLT	R	0h	SPI Address Error Bit 0h = No SPI address fault is detected (due to accessing non-user register) 1h = SPI address fault is detected

8.6.2 CONTROL Registers

表 8-16 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in 表 8-16 should be considered as reserved locations and the register contents should not be modified.

表 8-16. CONTROL Registers

Offset	Acronym	Register Name	Section
3h	Control Register 1	Control Register 1	セクション 8.6.2.1
4h	Control Register 2	Control Register 2	セクション 8.6.2.2
5h	Control Register 3	Control Register 3	セクション 8.6.2.3
6h	Control Register 4	Control Register 4	セクション 8.6.2.4
7h	Control Register 5	Control Register 5	セクション 8.6.2.5
8h	Control Register 6	Control Register 6	セクション 8.6.2.6
9h	Control Register 7	Control Register 7	セクション 8.6.2.7
Ah	Control Register 8	Control Register 8	セクション 8.6.2.8
Bh	Control Register 9	Control Register 9	セクション 8.6.2.9
Ch	Control Register 10	Control Register 10	セクション 8.6.2.10

Complex bit access types are encoded to fit into small table cells. 表 8-17 shows the codes that are used for access types in this section.

表 8-17. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WAPU	W APU	Write Atomic write with password unlock
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 Control Register 1 (Offset = 3h) [Reset = 00h]

Control Register 1 is shown in 表 8-18.

Return to the Summary Table.

表 8-18. Control Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	REG_LOCK	R/WAPU	0h	Register Lock Bits 0h = No effect unless locked or unlocked 1h = No effect unless locked or unlocked 2h = No effect unless locked or unlocked 3h = Write 011b to this register to unlock all registers 4h = No effect unless locked or unlocked 5h = No effect unless locked or unlocked 6h = Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x03h bits 2-0. 7h = No effect unless locked or unlocked

8.6.2.2 Control Register 2 (Offset = 4h) [Reset = 80h]

Control Register 2 is shown in 表 8-19.

Return to the Summary Table.

表 8-19. Control Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5	SDO_MODE	R/W	0h	SDO Mode Setting 0h = SDO IO in Open Drain Mode 1h = SDO IO in Push Pull Mode
4-3	SLEW	R/W	0h	Slew Rate Settings 0h = Slew rate is 25 V/µs 1h = Slew rate is 50 V/µs 2h = Slew rate is 125 V/µs 3h = Slew rate is 200 V/µs
2-1	PWM_MODE	R/W	0h	Device Mode Selection 0h = Asynchronous rectification with analog Hall 1h = Asynchronous rectification with digital Hall 2h = Synchronous rectification with analog Hall 3h = Synchronous rectification with digital Hall
0	CLR_FLT	W1C	0h	Clear Fault 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

8.6.2.3 Control Register 3 (Offset = 5h) [Reset = 46h]

Control Register 3 is shown in 表 8-20.

Return to the Summary Table.

表 8-20. Control Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	PWM_100_DUTY_SEL	R/W	0h	Frequency of PWM at 100% Duty Cycle 0h = 20KHz 1h = 40KHz
3	OVP_SEL	R/W	0h	Overvoltage Level Setting 0h = VM overvoltage level is 34-V 1h = VM overvoltage level is 22-V
2	OVP_EN	R/W	1h	Overvoltage Enable Bit 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
1	SPI_FLT_REP	R/W	1h	SPI Fault Reporting Disable Bit 0h = SPI fault reporting on nFAULT pin is enabled 1h = SPI fault reporting on nFAULT pin is disabled
0	OTW_REP	R/W	0h	Overtemperature Warning Reporting Bit 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

8.6.2.4 Control Register 4 (Offset = 6h) [Reset = 10h]

Control Register 4 is shown in 表 8-21.

Return to the Summary Table.

表 8-21. Control Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	DRV_OFF	R/W	0h	Driver OFF Bit 0h = No Action 1h = Hi-Z FETs
6	OCP_CBC	R/W	0h	OCP PWM Cycle Operation Bit 0h = OCP clearing in PWM input cycle change is disabled 1h = OCP clearing in PWM input cycle change is enabled
5-4	OCP_DEG	R/W	1h	OCP Deglitch Time Settings 0h = OCP deglitch time is 0.2 µs 1h = OCP deglitch time is 0.6 µs 2h = OCP deglitch time is 1.2 µs 3h = OCP deglitch time is 1.6 µs
3	OCP_RETRY	R/W	0h	OCP Retry Time Settings 0h = OCP retry time is 5 ms 1h = OCP retry time is 500 ms
2	OCP_LVL	R/W	0h	Overcurrent Level Setting 0h = OCP level is 9 A 1h = OCP level is 13 A
1-0	OCP_MODE	R/W	0h	OCP Fault Mode 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Reserved 3h = Reserved

8.6.2.5 Control Register 5 (Offset = 7h) [Reset = 00h]

Control Register 5 is shown in 表 8-22.

Return to the Summary Table.

表 8-22. Control Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	ILIM_RECIR	R/W	0h	Current Limit Recirculation Settings 0h = Current recirculation through FETs (Brake Mode) 1h = Current recirculation through diodes (Coast Mode)
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	EN_AAR	R/W	0h	Active Asynchronous Rectification Enable Bit 0h = AAR mode is disabled 1h = AAR mode is enabled
2	EN_ASR	R/W	0h	Active Synchronous Rectification Enable Bit 0h = ASR mode is disabled 1h = ASR mode is enabled
1-0	RESERVED	R/W	0h	Reserved

8.6.2.6 Control Register 6 (Offset = 8h) [Reset = 00h]

Control Register 6 is shown in 表 8-23.

Return to the Summary Table.

表 8-23. Control Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R-0	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	BUCK_PS_DIS	R/W	0h	Buck Power Sequencing Disable Bit 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled
3	BUCK_CL	R/W	0h	Buck Current Limit Setting 0h = Buck regulator current limit is set to 600 mA 1h = Buck regulator current limit is set to 150 mA
2-1	BUCK_SEL	R/W	0h	Buck Voltage Selection 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V
0	BUCK_DIS	R/W	0h	Buck Disable Bit 0h = Buck regulator is enabled 1h = Buck regulator is disabled

8.6.2.7 Control Register 7 (Offset = 9h) [Reset = 00h]

Control Register 7 is shown in 表 8-24.

Return to the Summary Table.

表 8-24. Control Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R-0	0h	Reserved
4	HALL_HYS	R/W	0h	Hall Comparator Hysteresis Settings 0h = 5 mV 1h = 50 mV
3	BRAKE_MODE	R/W	0h	Brake Mode Setting 0h = Device operation is braking in brake mode 1h = Device operation is coasting in brake mode
2	COAST	R/W	0h	Coast Bit 0h = Device coast mode is disabled 1h = Device coast mode is enabled
1	RESERVED	R/W	0h	Reserved
0	DIR	R/W	0h	Direction Bit 0h = Motor direction is set to clockwise direction 1h = Motor direction is set to anti-clockwise direction

8.6.2.8 Control Register 8 (Offset = Ah) [Reset = 00h]

Control Register 8 is shown in 表 8-25.

Return to the Summary Table.

表 8-25. Control Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FGOUT_SEL	R/W	0h	Electrical Frequency Generation Output Mode Bits 0h = FGOUT frequency is 3x commutation frequency 1h = FGOUT frequency is 1x of commutation frequency 2h = FGOUT frequency is 0.5x of commutation frequency 3h = FGOUT frequency is 0.25x of commutation frequency
5	RESERVED	R-0	0h	Reserved
4	MTR_LOCK_RETRY	R/W	0h	Motor Lock Retry Time Settings 0h = 500 ms 1h = 5000 ms
3-2	MTR_LOCK_TDET	R/W	0h	Motor Lock Detection Time Settings 0h = 300 ms 1h = 500 ms 2h = 1000 ms 3h = 5000 ms
1-0	MTR_LOCK_MODE	R/W	0h	Motor Lock Fault Options 0h = Motor lock causes a latched fault 1h = Motor lock causes an automatic retrying fault 2h = Motor lock is report only but no action is taken 3h = Motor lock is not reported and no action is taken

8.6.2.9 Control Register 9 (Offset = Bh) [Reset = 00h]

Control Register 9 is shown in 表 8-26.

Return to the Summary Table.

表 8-26. Control Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	ADVANCE_LVL	R/W	0h	Phase Advance Setting 0h = 0° 1h = 4° 2h = 7° 3h = 11° 4h = 15° 5h = 20° 6h = 25° 7h = 30°

8.6.2.10 Control Register 10 (Offset = Ch) [Reset = 00h]

Control Register 10 is shown in 表 8-27.

Return to the Summary Table.

表 8-27. Control Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R-0	0h	Reserved
4	DLYCMP_EN	R/W	0h	Driver Delay Compensation enable 0h = Disable 1h = Enable
3-0	DLY_TARGET	R/W	0h	Delay Target for Driver Delay Compensation 0h = 0 µs 1h = 0.4 µs 2h = 0.6 µs 3h = 0.8 µs 4h = 1 µs 5h = 1.2 µs 6h = 1.4 µs 7h = 1.6 µs 8h = 1.8 µs 9h = 2 µs Ah = 2.2 µs Bh = 2.4 µs Ch = 2.6 µs Dh = 2.8 µs Eh = 3 µs Fh = 3.2 µs

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The MCT8315Z can be used to drive Brushless-DC motors. The following design procedure can be used to configure the MCT8315Z.

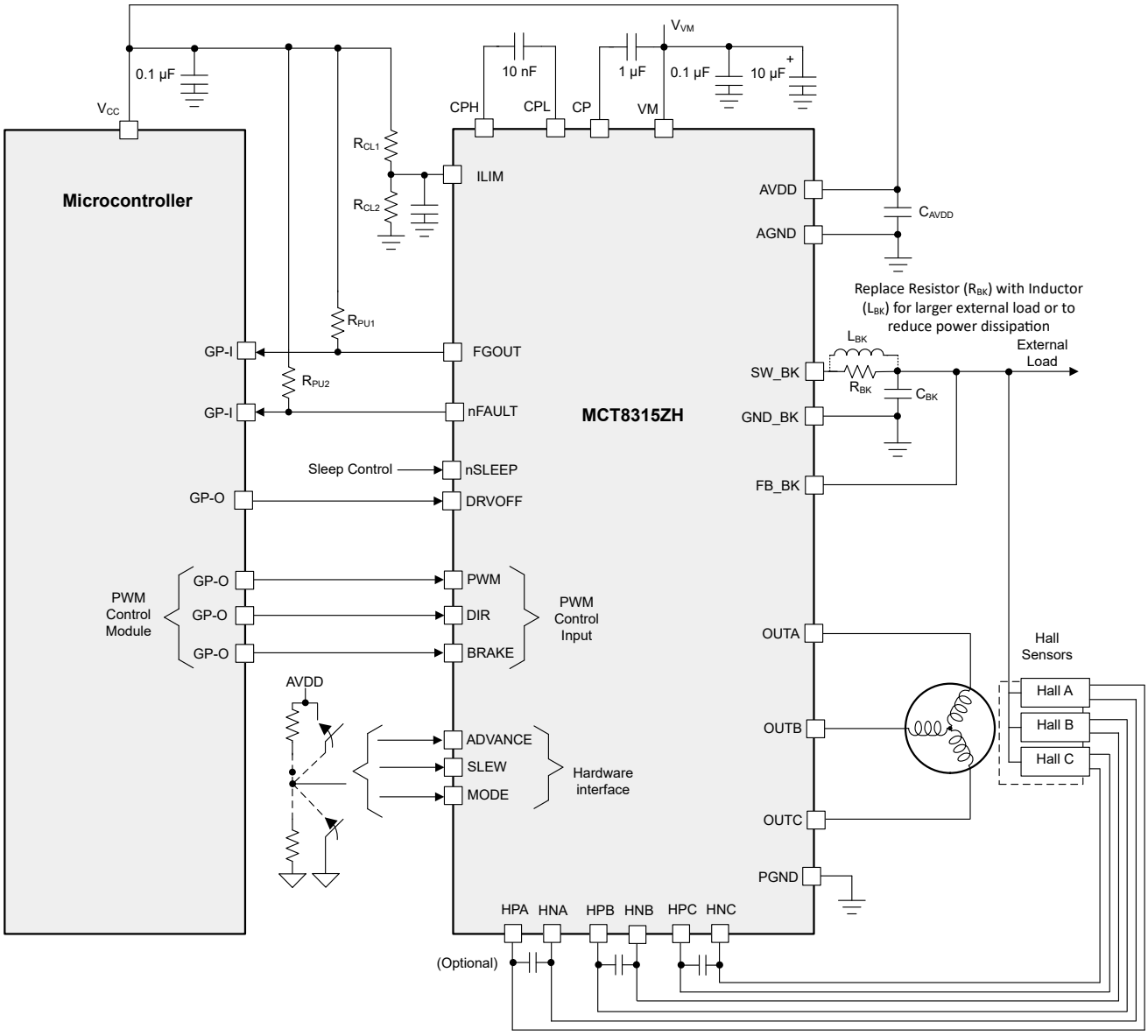

図 9-1. Primary Application Schematics for MCT8315ZH (hardware variant with buck)

注

For MCT8315ZT (hardware variant without buck), pins 2 and 4 should be left open (floating) while pin 3 should be tied to PGND.

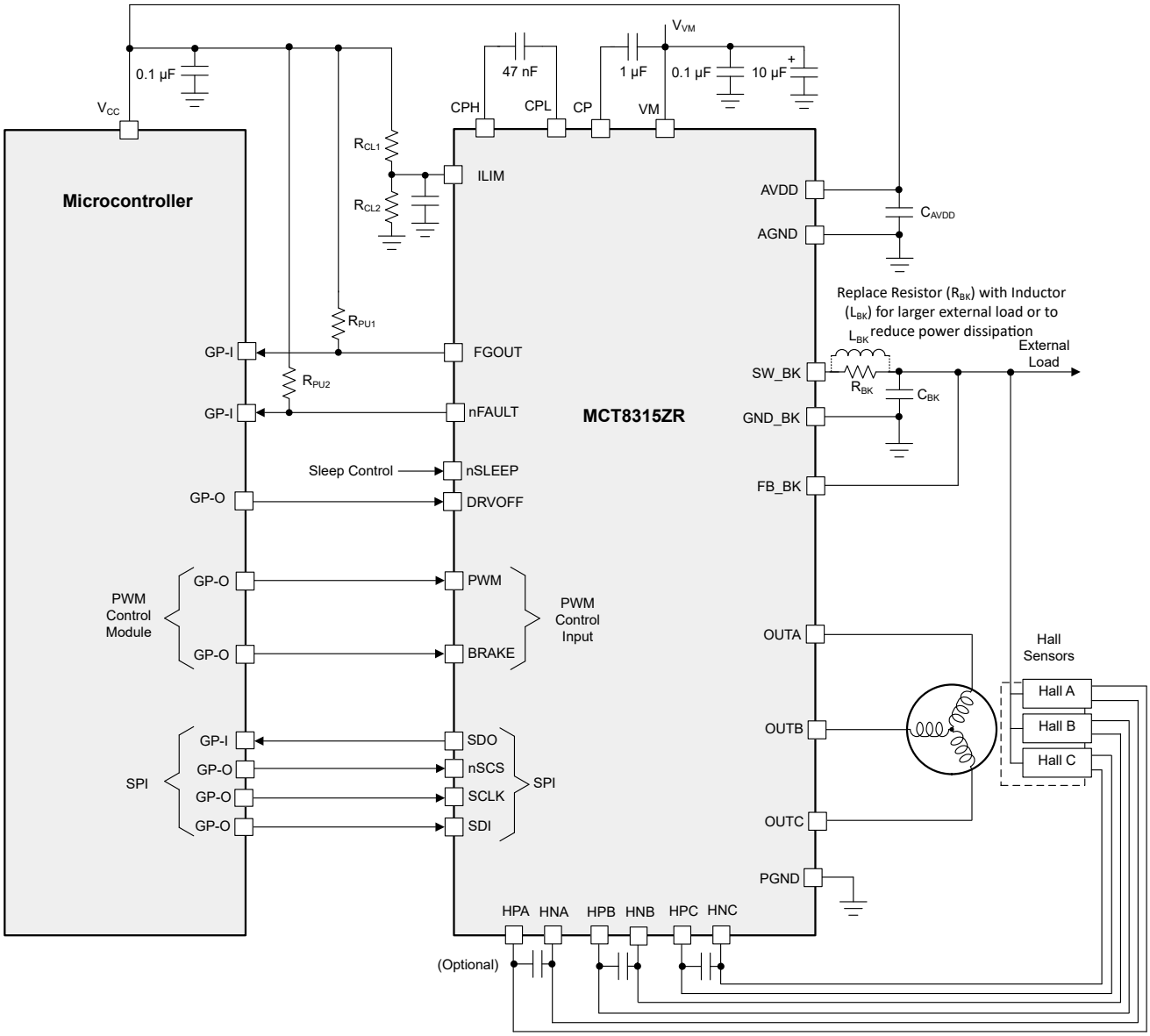

図 9-2. Primary Application Schematics for MCT8315ZR (SPI variant)

9.2 Hall Sensor Configuration and Connection

The combinations of Hall sensor connections in this section are common connections.

9.2.1 Typical Configuration

The Hall sensor inputs on the MCT8315Z device can interface with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal. To use this type of sensor, the AVDD regulator can be used to power the Hall sensor. 図 9-3 shows the connections.

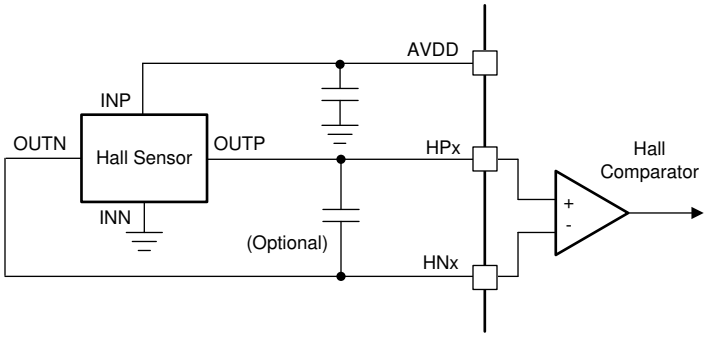

図 9-3. Typical Hall Sensor Configuration

Because the amplitude of the Hall-sensor output signal is very low, capacitors are often placed across the Hall inputs to help reject noise coupled from the motor. Capacitors with a value of 1 nF to 100 nF are typically used.

9.2.2 Open Drain Configuration

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the MCT8315Z device, with the addition of a few resistors as shown in 図 9-4.

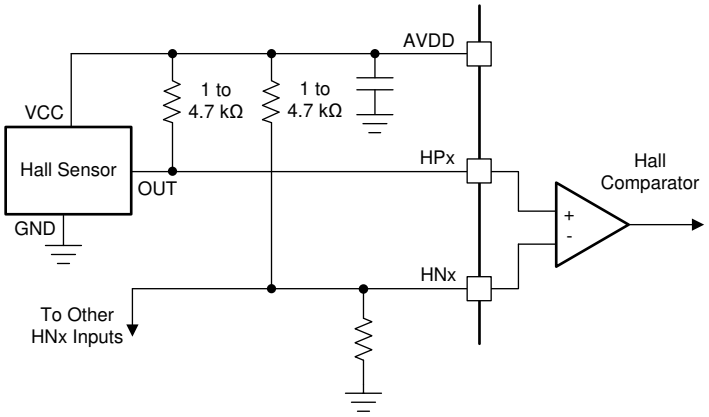

図 9-4. Open-Drain Hall Sensor Configuration

The negative (HNx) inputs are biased to AVDD / 2 by a pair of resistors between the AVDD pin and ground. For open-collector Hall sensors, an additional pullup resistor to the AVDD pin is required on the positive (HPx) input. Again, the AVDD output can usually be used to supply power to the Hall sensors.

9.2.3 Series Configuration

Hall elements are also connected in series or parallel depending upon the Hall sensor current/voltage requirement. 図 9-5 shows the series connection of Hall sensors powered via the MCT8315Z internal LDO (AVDD). This configuration is used if the current requirement per Hall sensor is high (>10 mA)

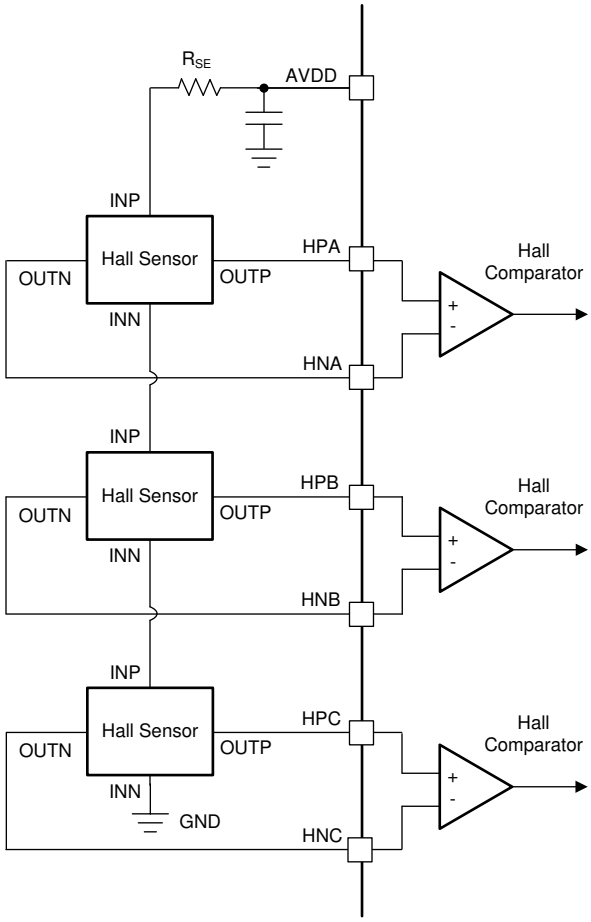

図 9-5. Hall Sensor Connected in Series Configuration

9.2.4 Parallel Configuration

図 9-6 shows the parallel connection of Hall sensors which is powered by the AVDD. This configuration can be used if the current requirement per Hall sensor is low (<10 mA).

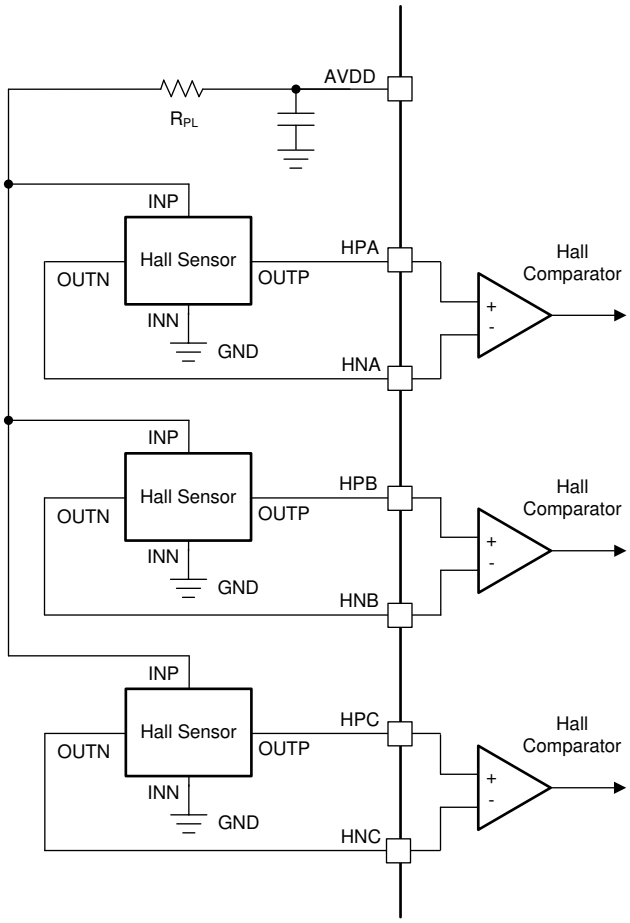

図 9-6. Hall Sensors Connected in Parallel Configuration

9.3 Typical Applications

9.3.1 Three-Phase Brushless-DC Motor Control With Current Limit

In this application, the MCT8315Z is used to drive a brushless-DC motor with current limit up to 100% duty cycle. The following design procedure can be used to configure the MCT8315Z in current limit mode.

9.3.1.1 Detailed Design Procedure

表 9-1 lists the example input parameters for the system design.

表 9-1. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	24 V
Motor peak current	I_{PEAK}	2 A
PWM Frequency	f_{PWM}	50 kHz
Slew Rate Setting	SR	200 V/µs
Buck regulator output voltage	V_{BK}	3.3 V

9.3.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V or 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. Operating at lower voltages generally allows for more accurate control of phase currents. The MCT8315Z functions down to a supply of 4.5V. A higher operating voltage also corresponds to a higher obtainable rpm. The MCT8315Z allows for a range of possible operating voltages because of a maximum VM rating of 40 V.

9.3.1.1.2 Using Active Demagnetization

Active demagnetization reduces power losses in the device by turning on the MOSFETs automatically when the body diode starts conducting to reduce diode conduction losses. It is used in trapezoidal commutation when switching commutation states (turning a high-side MOSFET off and another high-side MOSFET on while keeping a low-side MOSFET on). Active demagnetization is enabled when EN_ASR and EN_AAR bits are set in the SPI variant or MODE pin is set to Mode 5, Mode 6, or Mode 7 in the H/W variant.

When switching commutation states with active demagnetization disabled, dead time is inserted and the low-side MOSFET's body diode conducts while turning another high-side MOSFET on to continue sourcing current through the motor. This conduction period causes higher power losses due to the forward-bias voltage of the diode and slower dissipation of current. 図 9-7 shows the body diode conducting when switching commutation states.

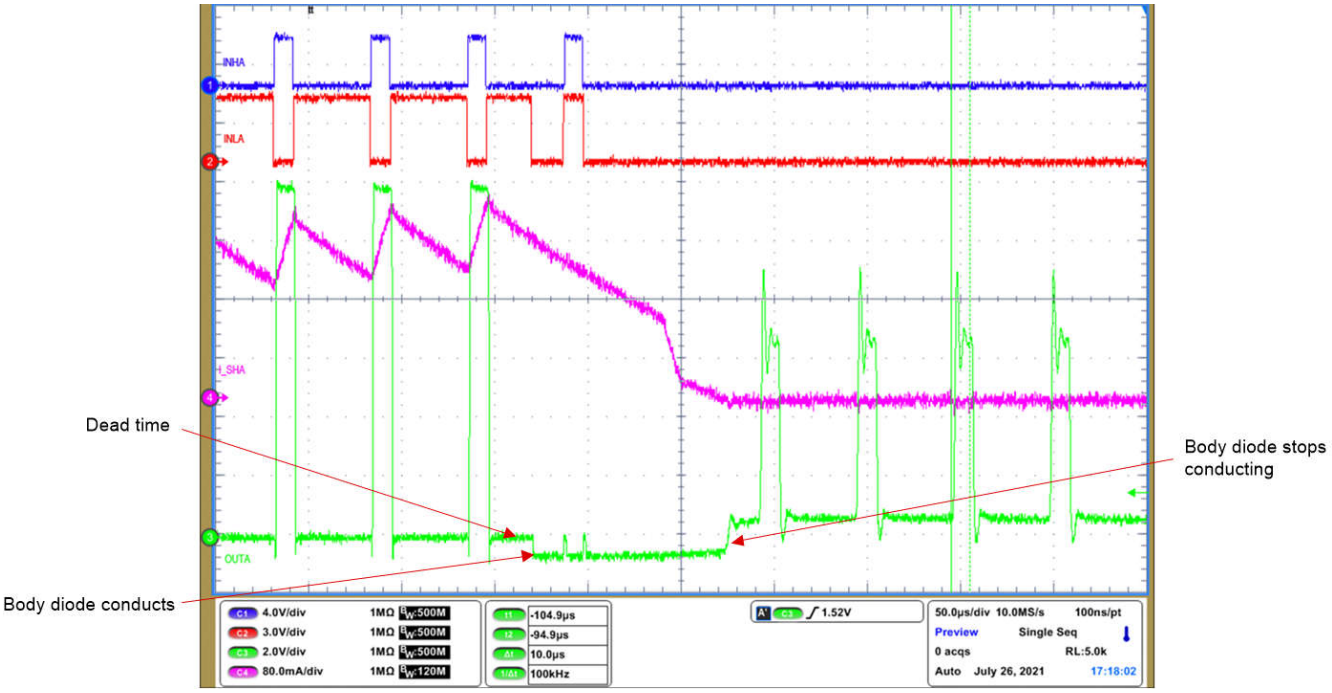

図 9-7. Active demagnetization disabled in MCT8315Z

When active demagnetization is enabled, the AD_HS and AD_LS comparators detect when the sense FET voltage is higher or lower than the programmed threshold. After the dead time period, if the threshold is exceeded for a fixed amount of time, the body diode is conducting and the logic core turns the low-side FET on to provide a conduction path with smaller power losses. Once the V_{DS} voltage is below the comparator threshold, the MOSFET turns off and current briefly conducts through the body diode until the current completely decays to zero. This is shown in 図 9-8.

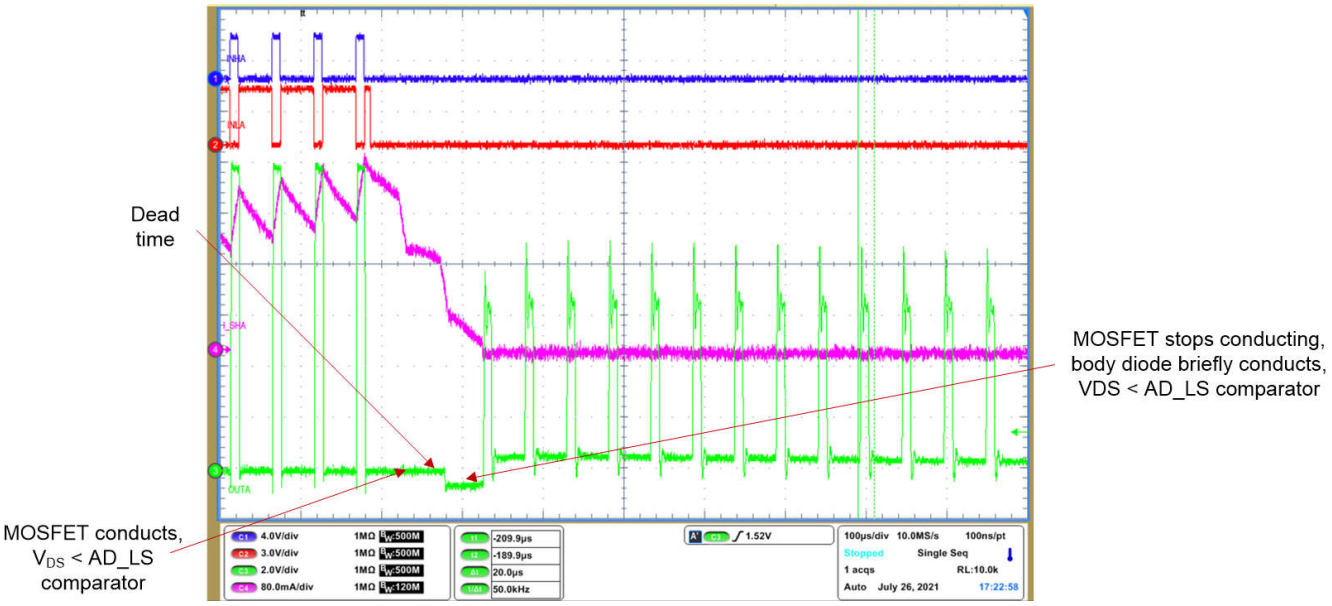

図 9-8. Active demagnetization enabled in MCT8315Z

9.3.1.1.3 Using Delay Compensation

Differences in delays of dead time and propagation delay can cause mismatch in the output timings of PWMs, which can lead to duty cycle distortion. To accommodate differences in propagation delay between various input conditions, the MCT8315Z integrates a Delay Compensation feature.

Delay Compensation is used to match delay times for currents going into and out of phase by adding a variable delay time (t_{var}) to match a preset target delay time. This delay time is configurable in SPI devices, and it is recommended in the datasheets to choose a target delay time that is equal to the propagation delay time plus the driver dead time (t_{pd} + t_{dead}).

For an example of Delay Compensation implementation, please visit the Delay and Dead Time in Integrated MOSFET Drivers application note.

9.3.1.1.4 Using the Buck Regulator

In MCT8315Z, the buck regulator components must be populated whether the buck is used or unused.

If unused, Resistor Mode should be configured by placing a small value resistor of 22-Ω for R_{BK} and a 10-V rated, 22-µF capacitor for C_{BK} to minimize board space and reduce component cost. To disable the buck regulator, set the BUCK_DIS in the SPI variant. The buck cannot be disabled in the Hardware variant.

If the buck regulator is used, either the Inductor or Resistor Mode can be selected. Inductor Mode allows a 22-µH or 47-µH inductor be used for L_{BK}. C_{BK} is recommended to be 22-µF. Make sure an appropriate inductor is chosen to allow for maximum peak saturation current at a 20% inductance drop since the buck can supply up to 600-mA external current.

Resistor Mode allows for power to be dissipated in an external resistor if the load requirement is less than 40-mA. Make sure the resistor is rated for the power dissipation required at worst case VM voltage dropout. See 式 6, 式 7, and 式 8 to calculate the resistor power rating required for a 24-V rated system, 3.3V buck output voltage, and 20-mA load current.

$$P_{R_{BK}} > (V_M - V_{BK}) \times I_{BK} \tag{6}$$

$$P_{R_{BK}} > (24V - 3.3V) \times 20mA \tag{7}$$

$$P_{R\_BK} > 0.434W \tag{8}$$

9.3.1.1.5 Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the MCT8315Z from power losses, use 式 9. Note that the thermal resistance θ_{JA} depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[℃] = P_{loss}[W] \times \theta_{JA}\left[\frac{℃}{W}\right] + T_A[℃] \tag{9}$$

The table below shows summary of equations for calculating each loss in the MCT8315Z.

表 9-2. MCT8315Z Power Losses

Loss type	Equation
Standby power	$P_{standby} = V_{PVDD} \times I_{PVDDS}$
GVDD CP mode (PVDD < 18V)	$P_{LDO} = 2 \times V_{PVDD} \times I_{GVDD} - V_{GVDD} \times I_{GVDD}$
GVDD LDO mode (PVDD > 18V)	$P_{LDO} = (V_{PVDD} - V_{GVDD}) \times I_{GVDD}$
AVDD LDO	$P_{LDO} = (V_{PVDD} - V_{AVDD}) \times I_{AVDD}$

9.3.1.2 Application Curves

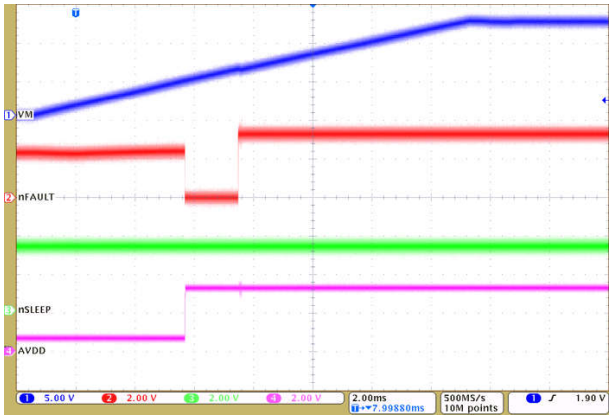

図 9-9. Device Powerup with VM

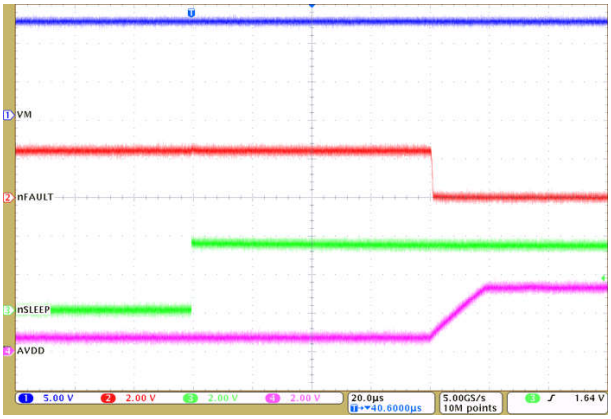

図 9-10. Device Powerup with nSLEEP

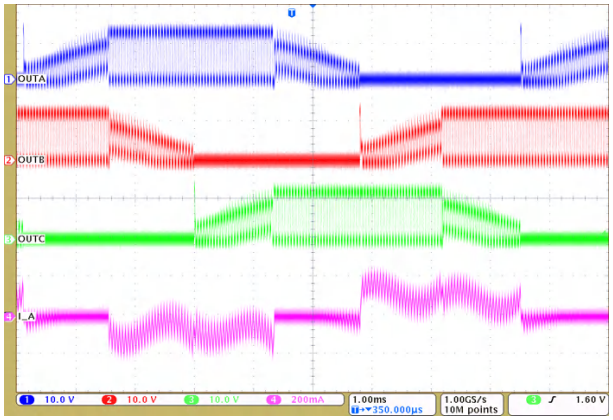

図 9-11. Driver PWM Operation

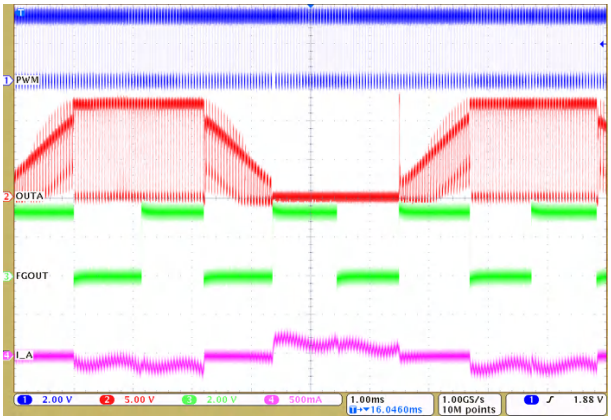

図 9-12. Driver PWM Operation with FGOUT

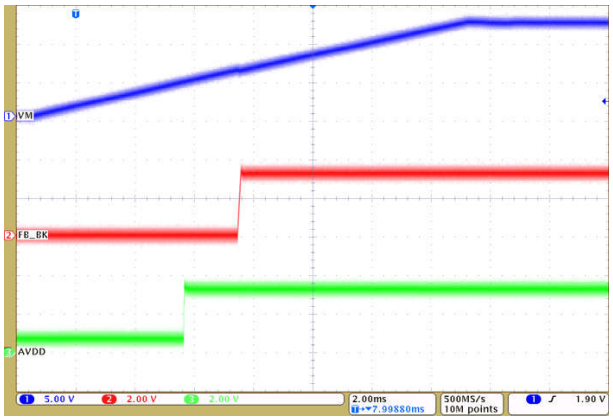

図 9-13. Power Management

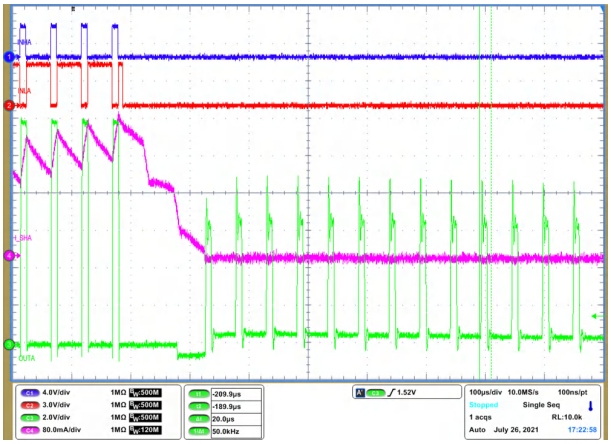

図 9-14. Driver PWM with Active Demagnetization (ASR and AAR)

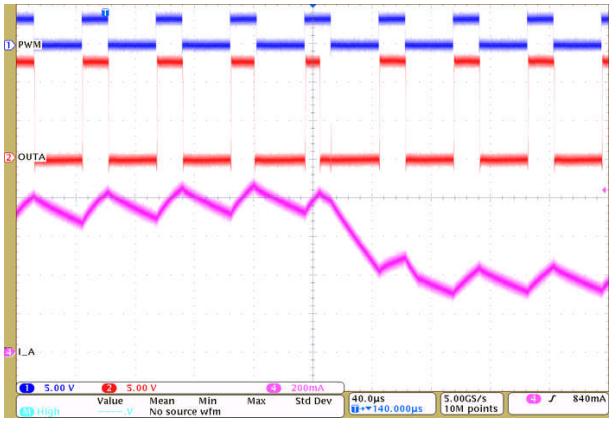

図 9-15. Driver PWM Operation with Current Limit

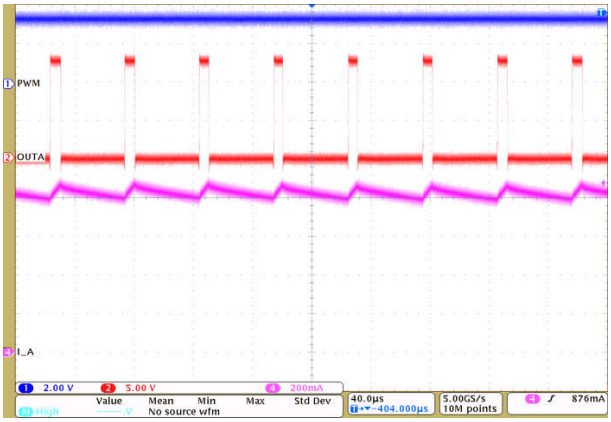

図 9-16. Driver 100% Operation with Current Chopping

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

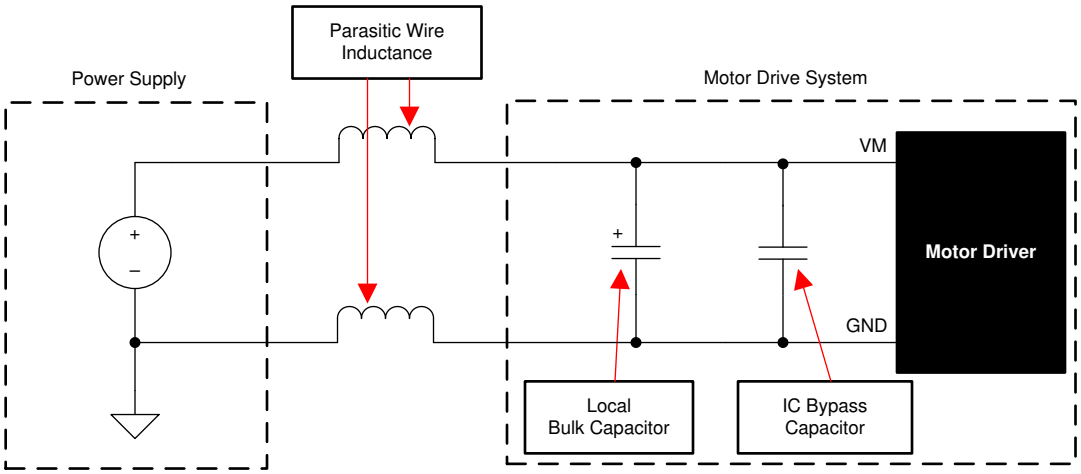

図 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump, AVDD, and VREF capacitors should be ceramic and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Make sure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the power loss that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BK and FB_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BK trace as much as possible to allow for faster load switching.

図 11-1 shows a layout example for the MCT8315Z.

11.2 Layout Example

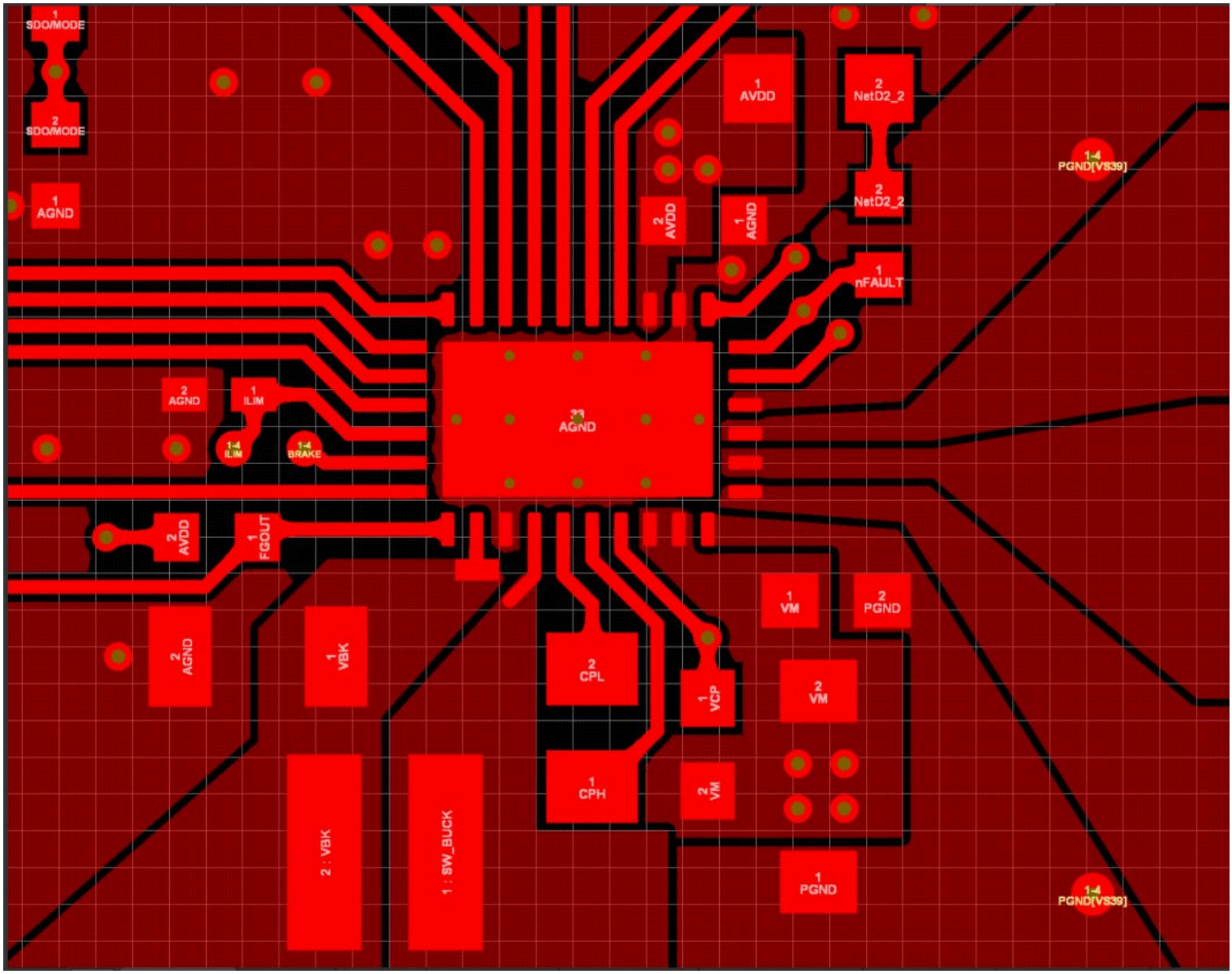

図 11-1. Recommended Layout Example for MCT8315Z

11.3 Thermal Considerations

The MCT8315Z has thermal shutdown (TSD) as previously described. A die temperature in excess of 165°C (min.) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Power Dissipation

The power loss in MCT8315Z include standby power losses, LDO and Buck power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in MCT8315Z. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and their duration into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that RDS,ON increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

A summary of equations for calculating each loss is shown below for trapezoidal control.

表 11-1. MCT8315Z Power Losses for Trapezoidal Control

Loss type	Trapezoidal
Standby power	$P_{standby} = VM \times I_{VM\_TA}$
LDO (from VM)	$P_{LDO} = (VM - V_{AVDD}) \times I_{AVDD}$
FET conduction	$P_{CON} = 2 \times I_{RMS(trap)} \times R_{ds,on(TA)}$
FET switching	$P_{SW} = I_{PK(trap)} \times V_{PK(trap)} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = I_{RMS(trap)} \times V_{diode} \times t_{diode} \times f_{PWM}$
Buck	$P_{BK} = 0.97 \times V_{BK} \times I_{BK}$

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Visit the MCT8315ZH-EVM Tool Page*
- *Download the BLDC Integrated MOSFET Thermal Calculator tool*
- *Calculating Motor Driver Power Dissipation*, SLVA504
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Sensored 3-Phase BLDC Motor Control Using MSP430*, SLAA503
- *Understanding Motor Driver Current Ratings*, SLVA505

12.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントを エキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.3 Trademarks

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12.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MCT8315Z0HRRYR	ACTIVE	WQFN	RRY	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MCT8315 Z0HRRY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

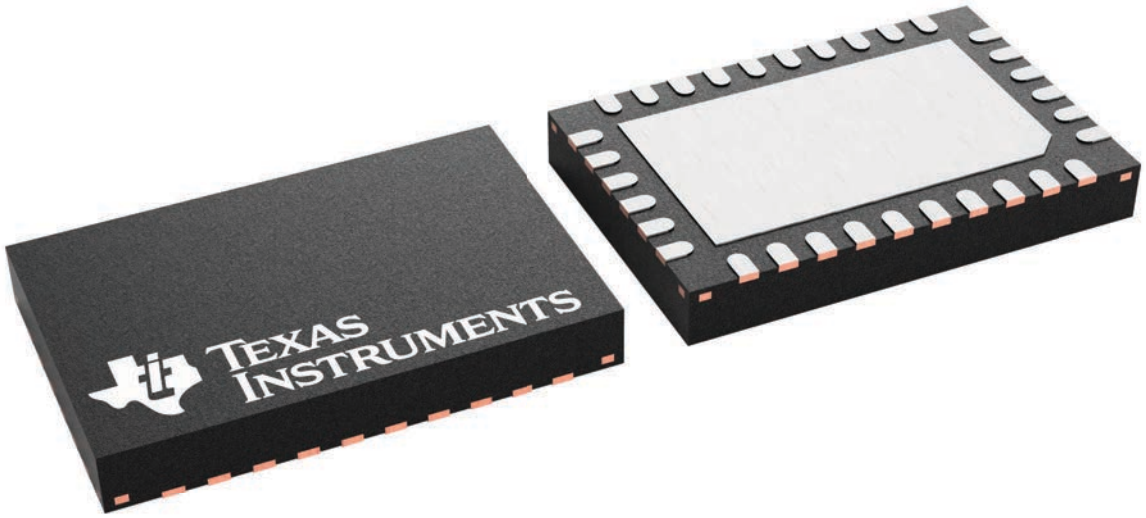
RRY 32

WQFN - 0.8 mm max height

4 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



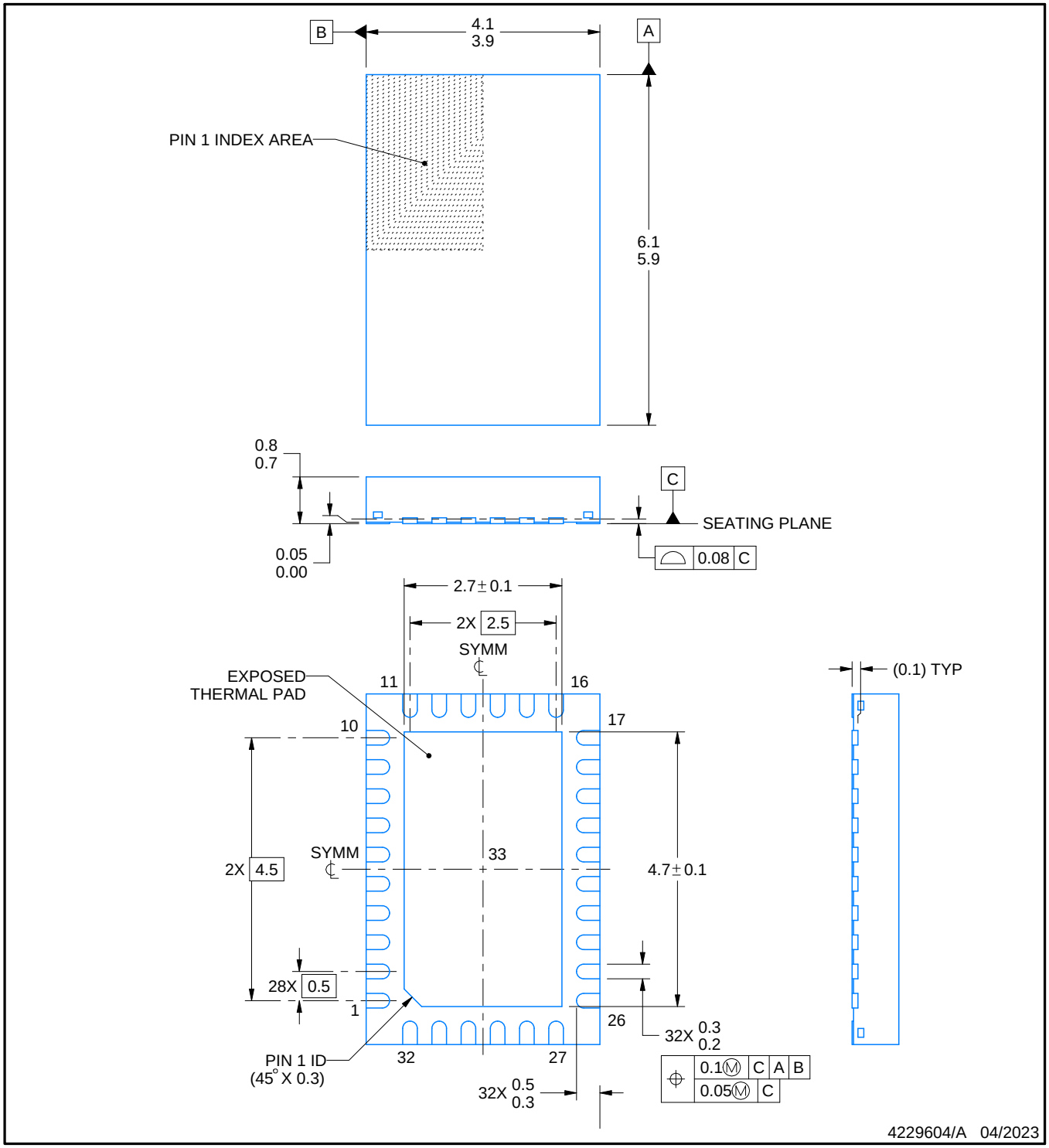
4229624/A

PACKAGE OUTLINE

RRY0032B

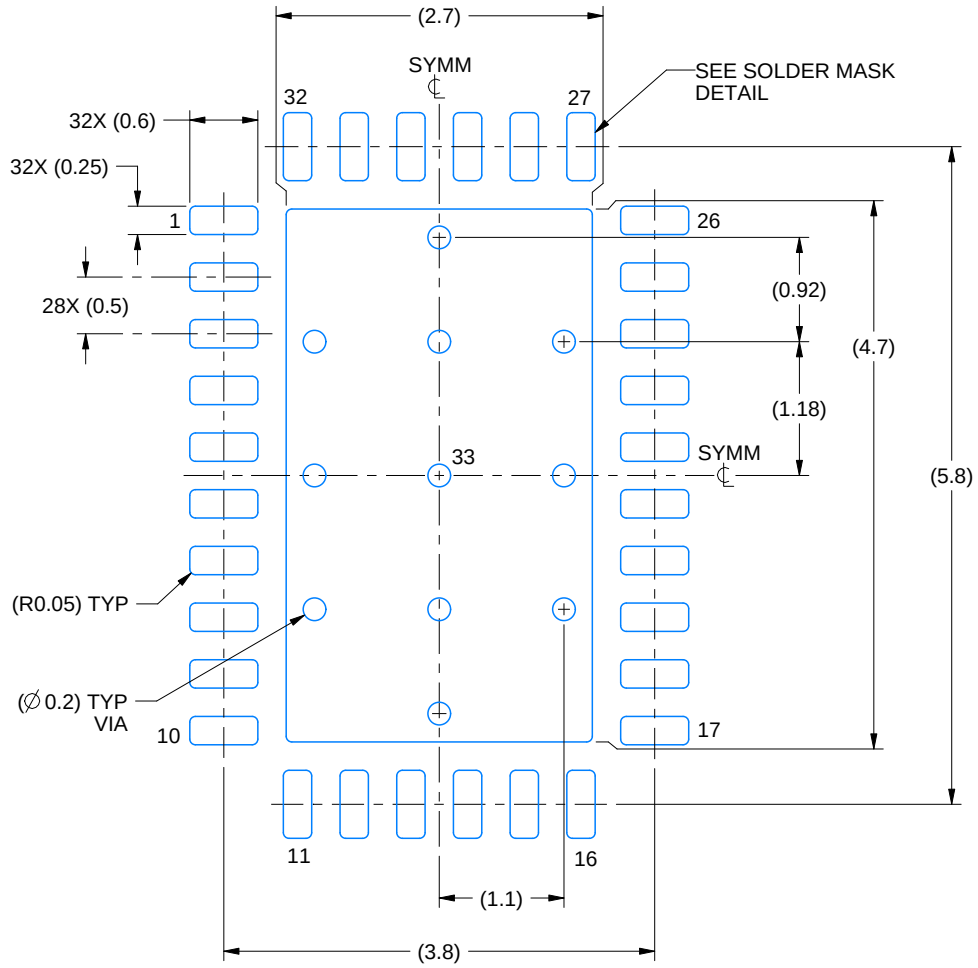
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

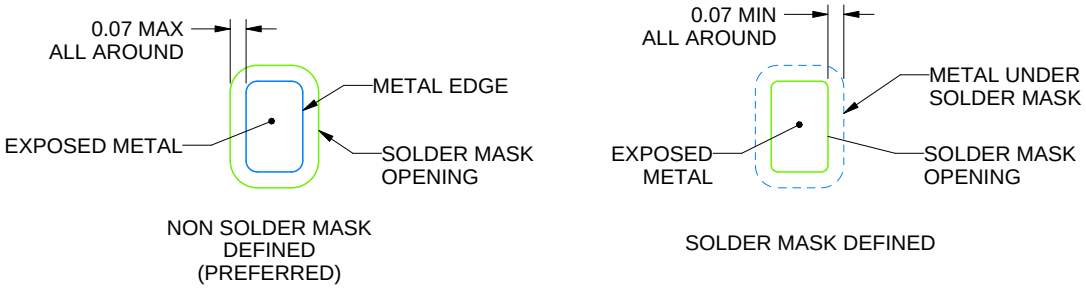


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

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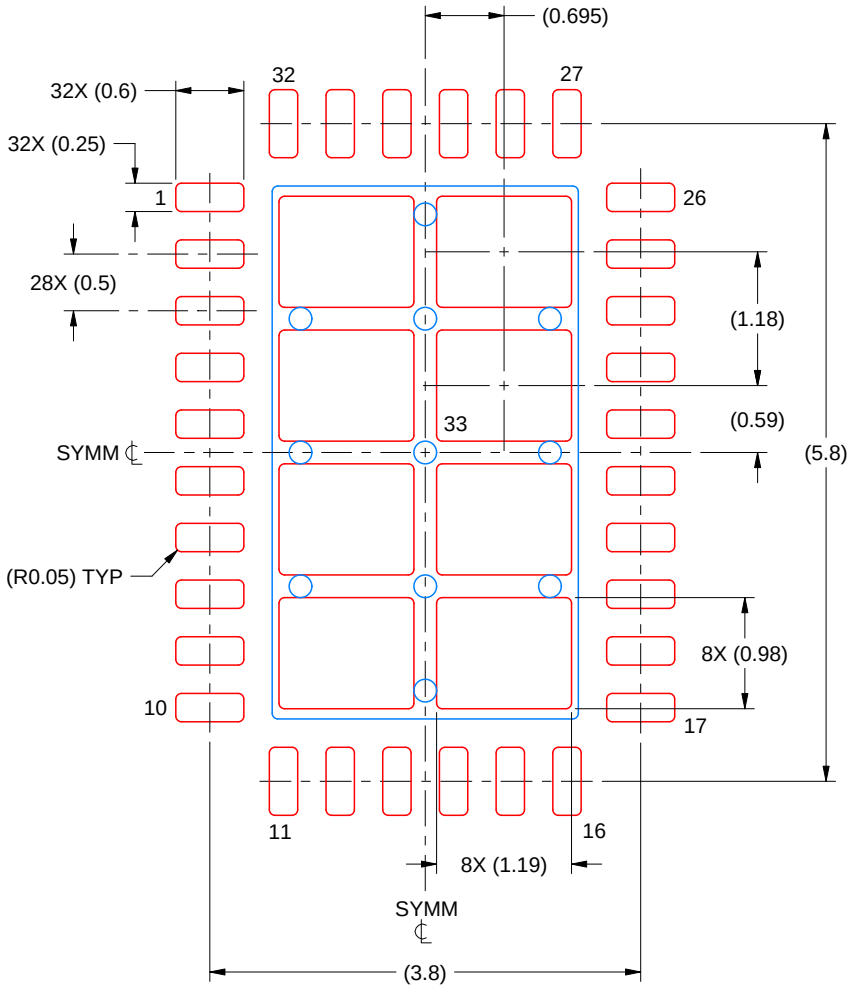
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 33
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265